Partial Discharge Mitigation in Power Modules using an Automation-Driven Design Rule Development Method

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Microelectronics-Photonics

by

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August 2023
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Abstract

Power modules used for the conversion and conditioning of electrical power for applications like electric vehicles, more-electric aircraft, the power grid, etc., are largely designed manually by engineers. Design automation of power modules is starting to gain recognition as a timely and necessary alternative to intuitive manual design and fabrication. With increasing need for wide bandgap materials that can operate at higher voltages, and the need to make modules more compact, hazards like electrical breakdown are more likely. Partial discharge (PD) is a silent and invisible precursor to electrical breakdown. It is compounded with compaction, creating a potential for electrical breakdown and catastrophic failure of the module package. Instead of being the limiting factor, or even a hazard, power module packages need to keep pace with the advancements being made in wide bandgap technology. While the automation of power module design is still new, and research and standards on PD in power modules are limited, this dissertation is a significant step in designing for high voltage operation while assessing tradeoffs against module compaction in an electronic design automation tool.

This dissertation describes a method of systematically accounting for partial discharge in power modules using a unique approach where improvements to a module layout are determined in terms of design rules. Trace gaps, in this method, are designed to be functions of operating voltage, substrate and encapsulant material choice, and layer thicknesses of the substrate. These design rules are based on simulations that are validated by physical PD experiments. Furthermore, filleting is performed on the final layouts to further reduce PD by reducing the E-field concentrations by a third. This methodology has been implemented in PowerSynth, an in-house hardware-validated electronic design automation tool that performs electro-thermal and mechanical layout optimization.

Before the implementation of this work, layouts were agnostic to PD. From the contribution of this work, the layouts now generated by the tool are PD-mitigated, with a maximum operating voltage for each layer stack. Below the rated voltage, the user can choose multiple voltage-trace gap trade off options for the layout. Demonstrating this implementation in this work shows that the user can achieve either a 24% improvement in voltage level, or a 20% improvement in area reduction, or a trade-off combination of the two. As layouts increase in complexity, these improvements will likely grow.

The implementation of this work allows room for growth by allowing customized PD data libraries from various manufacturing lines to inform design rules much like a process design kit in the field of integrated circuit design. The designer using PowerSynth can: 1.) Use default libraries for design rules, or 2.) Perform their own simulations to augment the existing PD data library according to the method presented here, or 3.) Fabricate their own test structures and design corresponding simulations to develop their own complete PD data library and import it to PowerSynth. The manufacturable modules resulting from this tool are thus designed to be practical and reliable for high voltage operation.

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Acknowledgments

I would like to thank God for leading me through this humble path of growth, challenging and comforting me, guiding me, bringing the right people into my life who have blessed me through this journey, and for helping me persevere and finish.

I thank God for my parents who have made sacrifices so I can be here, the many teachers who have educated me over the years, my dear friends who have prayed for me and supported me through this journey, some great mentors who advised me, my brother who helped me through some hard times, and all my colleagues who have helped me with this work.

I would like to thank Prof. Matt Gerner for his intentionality in discussing my research with me and guiding me, Ms. Michel LaCrue for the countless hours of providing me with writing accountability, Dr. David Huitink for helping me gain confidence in the statistics of my data, Dr. Greg Salamo for reviewing the Physics in my paper, and Dr. Shannon Davis and Ms. Renee Hearon for their encouragement and guidance through the many hurdles of grad school.

I would like to thank Dr. Mantooth, my advisor, for his gracious support, patience, and overall encouragement in helping me graduate, the PowerSynth team, the packaging team, NCREPT staff, and Dr. Huitink's team for their support, the POETS ecosystem for providing me with opportunities to present my work, Dr. Yue Zhao, for his collaboration with the partial discharge test equipment, and my colleagues, peers and professors who helped me: Prof. Chris Farnell, Dr. Yuxiang Chen, Tristan Evans, Dr. Ange Iradukunda, Dr. Mahsa Montazeri, David Gonzalez, Dr. Riya Paul, Michael Mastalish, Anna Corbitt, Collin Ruby, and lab safety partners.

I would like to especially thank my friends Taylor, Gina, Liz, Alison, Gift, Ellie, David, the Foors, the Gerners, the Stilwells, the Sergeants, and my church community for praying for me consistently. I thank God for continuing to lead me in the path he has prepared for me.

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List of published papers

Parts of Chapter 1 and 2 were originally published as:

S. Mukherjee, T. M. Evans, D. R. Huitink and H. A. Mantooth, “A Partial Discharge Inception Voltage Modeling Approach,” in IEEE Open Journal of Power Electronics, vol. 4, pp. 148-160, 2023, doi: 10.1109/OJPEL.2023.3241853.

Parts of Chapter 1 and 4 were originally published as:

S. Mukherjee, Y. Peng and H. A. Mantooth, “General Equation to Determine Design Rules for Mitigating Partial Discharge and Electrical Breakdown in Power Module Layouts,” 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Suita, Japan, 2020, pp. 1-6, doi: 10.1109/WiPDAAsia49671.2020.9360263, and

S. Mukherjee, T. Evans, B. Narayanasami, Q. Le, A. I. Emon, A. Deshpande, F. Luo, Y. Peng, S. Pytel, T. Vrotsos and H. A. Mantooth, “Toward Partial Discharge Reduction by Corner Correction in Power Module Layouts,” 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, Italy, 2018, pp. 1-8, doi: 10.1109/COMPEL.2018.8459973.

Chapter 1. Introduction

Power modules find utility in various sectors such as grid-level power conversion, transportation electrification, space exploration, etc. But in a competitive market, they also need to be innovated on. Technologically, wide bandgap (WBG) semiconductors like SiC have advanced significantly over the past couple of decades. It is well known that they offer higher speed, temperature, and breakdown strength compared to silicon, and are therefore finding use for power conversion in applications like electric vehicles, hybrid electric aircraft, etc. However, the lack of packaging innovation for these devices impedes the advancements offered by WBG technology [1]–[5]. Thus, there is a great push towards advancing power module optimization and packaging innovation to harness the complete utility offered by WBG devices.

One limitation of power module packaging is its reliability. With high speed and high power density power conversion come side-effects like thermal coupling [5]–[10], mechanical instability [7], [8], [11], [12], electromagnetic interference [8], [13], etc. A slightly lesser-known effect is called partial discharge, which is now becoming a greater concern [5]–[8], [10], [11] as modules become more compact than ever before.

According to IEC 60270, the international standard on high-voltage test techniques, partial discharge (PD) "is a *localized* electrical breakdown in an insulating material that does not fully bridge the gap between the electrodes." A *breakdown* fully bridges the gap between two electrodes, but a partial discharge is a breakdown in a spatially localized area. Continuous PD can eventually lead to a breakdown. Partial discharge inception voltage (PDIV) "is the applied voltage at which repetitive PDs of a pre-specified quantity/threshold are first observed in the test object, when the voltage applied to the object is gradually increased from a lower value at which no PDs are observed" [14]. First, this section gives a background on PD in power modules, and

the physical phenomena of PD. Then, the general modeling attempts, the stochastic nature of PD, and measurement methods are discussed. After that, this section explains PD mitigation strategies in power modules and the technology gap that is addressed in the rest of this dissertation.

1.1 Partial discharge (PD) in power modules

PD is commonly found in the insulating materials of cables [15]–[18], and motor and transformer winding insulation [19]–[26]. It can happen in solid, liquid, or gas. Common PD sites include bubbles in transformer oil (liquid), laminations of winding insulation material (solid), interfaces of conducting and insulating material (solid), on the surface of insulating discs used in transmission lines (air) called corona, etc. It is also found in power modules [5], [19], [27]–[34], [8], [34]–[41] due to the ever-decreasing trace gaps between conductors in module layouts.

Figure 1 shows a power module building block which includes a DBC substrate, devices, interconnect, encapsulant, and a baseplate on the other side. The two insulating materials are the ceramic and the encapsulant. These materials are electrically stressed when there is a high voltage applied across the two metal traces on the top with the trace on the other side grounded. The gap between the two traces on the top is called the trace gap. The interface that forms along the edge of the metal where the metal, ceramic and encapsulant meet is called the triple point (TP) and this is the most common location for PD to occur. There are triple points wherever three materials meet.

Some of the samples tested in this work were imaged under a microscope. Figure 1 (a) and (b) are a couple of those photos. Figure 1 (b) shows a carbonized track that resulted from stressing the encapsulant too much, resulting in PD that eventually led to breakdown across the

ceramic surface. In this case, the encapsulant was just air. The dielectric strength of air is 3 kV/mm. The trace gap shown in this example is 1 mm, and the ceramic is 0.6 mm thick. Figure 1 (c) shows the same degradation happening when the encapsulant is a commonly used dielectric gel, where electrical breakdown happened not long after PD inception. The result rendered the encapsulant material unusable. Zhang's team [42], [43] also observed similar patterns as the ones shown in Figure 1. While liquid and gas insulators are self-healing, solids get damaged progressively until catastrophic breakdown. This makes it more urgent to determine a way to design for PD mitigation in power modules as they are typically encapsulated with a solid dielectric.

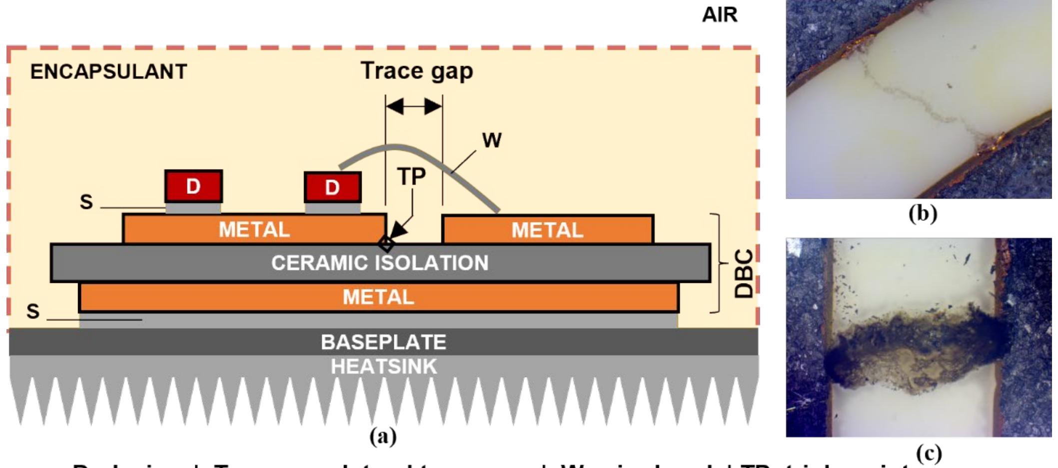


Figure 1. (a) Trace-gap and triple point (TP) in a power module building block template cross-section, (b) Optical microscope image of carbonized tracks caused by electrical discharge in a 1 mm trace-gap that was unencapsulated, and (c) encapsulated.

Several researchers have commented on the need to address PD in power modules [4], [5], [35], [36], [44]. Dimarino noted that power modules designed to operate at high voltages of 3.3 kV and above are not tested for PD [5]. This is concerning since PDIV would limit the operating voltage of the module. Figure 2 shows the evolution of PD next to an IGBT device

where there was a bubble in the gel encapsulant between the AlN substrate and a metal terminal. The bubble grew as PD progressed and eventually there was a breakdown [45]. While PD does not always immediately cause a breakdown, the continuation of PD beyond the PDIV starts the slow and steady degradation process of the material, sacrificing the reliability of the entire module.

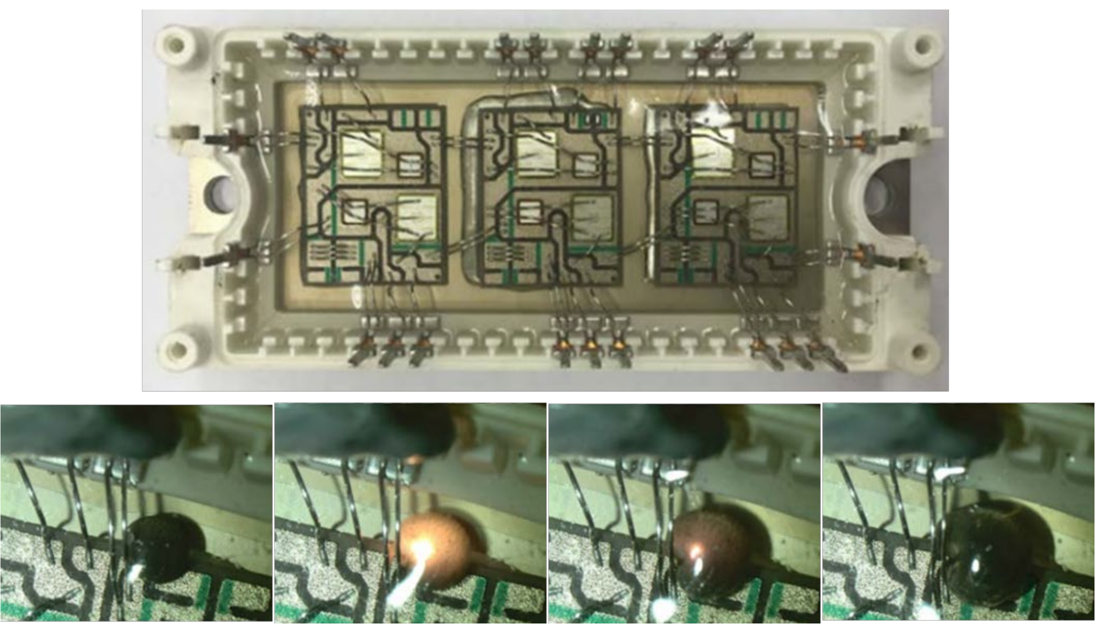


Figure 2. IGBT power module with evolution of PD in a bubble in the encapsulant [45].

Some of the corona camera images used in this work revealed PD leading to breakdown soon after the inception of PD (Figure 3). The figure shows the test sample on the left, and two images of the progression of breakdown on the right. The PD happened in the encapsulant between the two metal traces that were stressed with a potential difference of 13 kV.

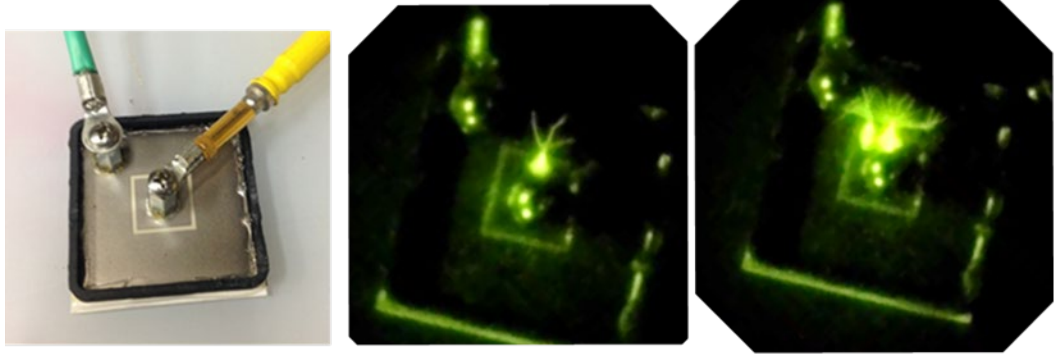


Figure 3. PD leading to breakdown in an encapsulant between two metal traces of a passive power module test coupon.

Progressive PD is a silent precursor to electrical breakdown and can lead to catastrophic damage if it goes undetected. This can cause, at best, a significant down-time to remove and replace the damaged part from an adequately protected circuit, or at worst, a sustained arc that can cause severe consequences. To prevent such hazards, one must account for PD at the design stage instead of trying to detect it during system operation and needing to replace a damaged module.

1.2 Physical phenomenon

An electrical discharge is fundamentally plasma. It can be seen in nature as lightening, or the Aurora Borealis (Northern Lights). In a high enough electric field, free electrons can be accelerated to impact the outer electrons of atoms. These free electrons come from background radiation or electrons pushed to the ionization energy of gas present in the region. When these outer orbit electrons are knocked off, it causes the rest of the atom to become a positive ion and create more free electrons, which then proceed to cause more impact ionization, eventually resulting in a chain reaction, or an avalanche breakdown. Figure 4 shows an avalanche breakdown mechanism.

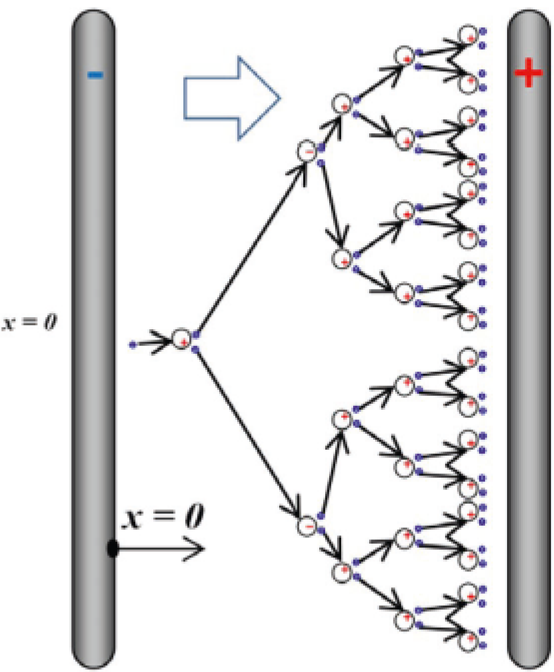


Figure 4. Avalanche breakdown of gas between two electrodes under electrical stress [46].

Since the presence of atoms in an electric field allows the avalanche process to begin, a perfect vacuum is the best insulation material. In a non-vacuum situation, each free electron travels a certain distance under the influence of the electric field before hitting an atom. This distance is called the mean free path of the electron. Friedrich Paschen first stated the relationship between pressure, mean free path, and breakdown voltage. He stated that the breakdown voltage of hydrogen varies with the product of pressure p and mean free path d as shown in Figure 5. This is famously called Paschen's curve [46].

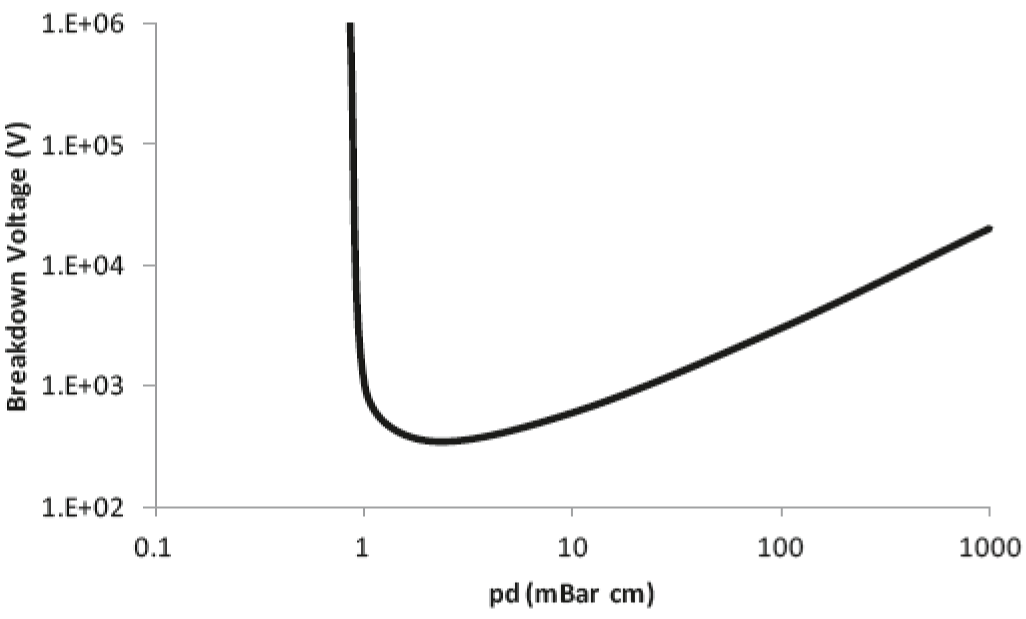


Figure 5. Paschen's curve for hydrogen showing how breakdown voltage varies with the pressure and mean free path of electrons [46].

This curve is significant as it shows that PDIV would dangerously decrease for electrical equipment that operate at high altitudes where the pressure is much lower than atmospheric pressure. Engineers must account for this in the design of power modules that go into air and space application equipment. Conversely, submarine applications will see an increase in the PDIV compared to that of atmospheric level equipment.

An electrical discharge can be initiated in localized regions of high electric field (E-field) where the E-field in the region becomes high enough to cause electron avalanches. The ionized gas created is plasma. In air or liquid, these discharges are usually self-healing, but in a solid insulation material, plasma, which is chemically reactive, can damage the insulation material. These discharges can then propagate into the bulk insulation medium given the right conditions such as field gradient, leading to a catastrophic failure. Plasma contains fast moving ions that can also damage the electrodes by sputtering [46].

Figure 6 shows current-voltage characteristics as the voltage between parallel plate electrodes is increased, showing the various regimes of discharges [46]. This shows that the voltage current relationship in various discharges is non-linear. PD happens below the breakdown voltage and is typically several μA to hundreds of μA. So, it is mostly in the dark discharge region. Because PD is invisible, it is difficult to detect. Several detection methods are discussed later.

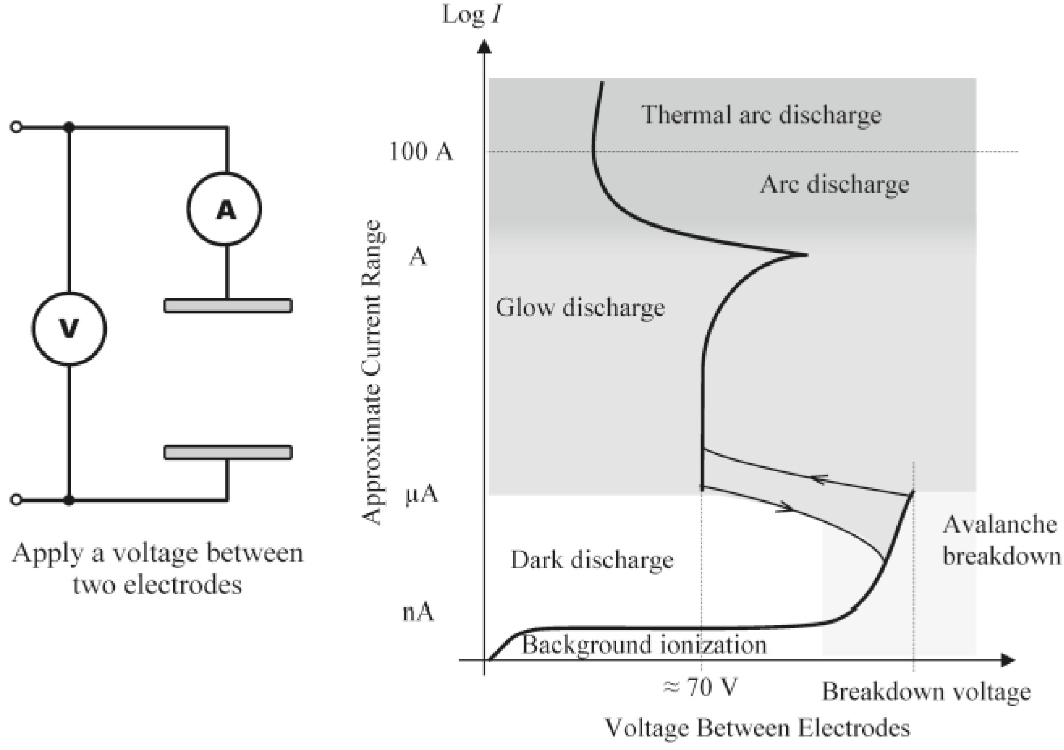


Figure 6. I-V characteristics of a typical electrical discharge between two parallel plate electrodes [46].

1.3 Main factors that affect PD

PD is affected by many factors. Two important factors are the electrode configuration and imperfections in the dielectric:

1.3.1 Electrode configuration:

Any electrode-pair with a potential difference will have imaginary electric field lines and equipotential lines associated with it. In a parallel plate capacitor, these lines are straight, and the E-field (E) in the dielectric is uniform, and is the ratio of the voltage (V) across the conductors and the distance (d) between the conductors, $E = V/d$. This is not the case for a non-parallel plate capacitor. Figure 7 shows a point-plane electrode-pair configuration. Due to the geometry of the pointed electrode, the equipotential field lines get bunched up near the tip of the electrode. The local E-field near the tip is much higher than the E-field in the bulk insulation material. If or when this *local* E-field exceeds the dielectric strength of the *bulk* insulation material, local discharges will start in that high-field region. The discharge will remain localized near the tip because the E-field decreases significantly as we move away from the tip and into the bulk material. Since the E-field near the tip is greater than the dielectric strength of the insulation, but the E-field away from the tip is not greater than the dielectric strength of the insulation, the discharge can not propagate much into the bulk of the insulation material and remains localized near the tip.

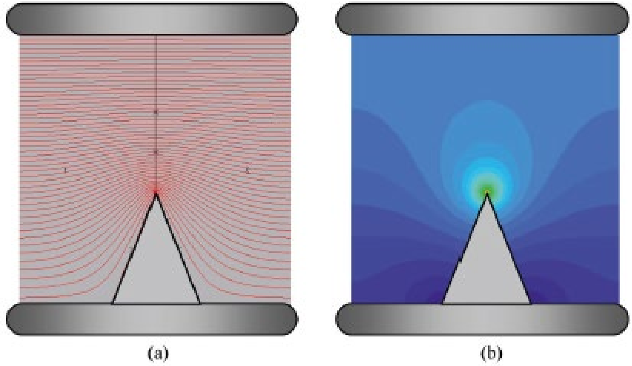


Figure 7. Point-plane electrode configuration with (a) equipotential field lines, and (b) E-field concentration around the electrode tip [46].

The reason why E-field gets bunched up near the tip of sharp electrodes is due to the accumulation of charges preferentially at sharper corners over straight edges. The surface charge density at those sharp corners helps us quantify the E-field in the insulation material adjacent to the sharp corners. Consider Figure 8 where the conducting surfaces of an electrode at potential V, meet with an opening angle β. P is a point that is a distance of ρ away from the corner. Point P is where the E-field is measured.

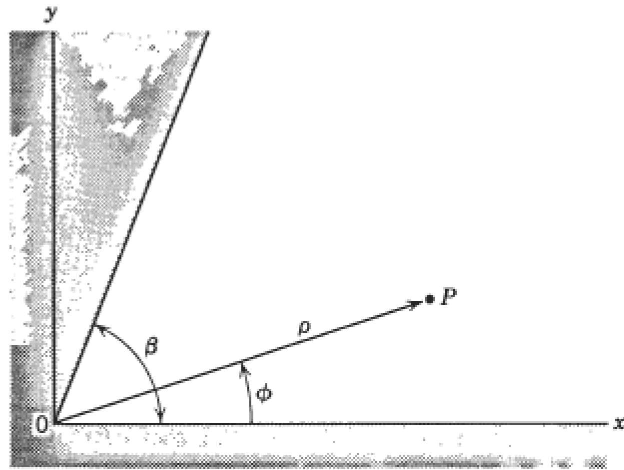


Figure 8. A corner of opening angle β formed by the intersection of two conducting planes of a conductor (in grey) [47].

The charge densities at ϕ = 0 and ϕ = β for a fixed ρ are equal and approximately:

$$\sigma(\rho) = \frac{E_\varphi(\rho, 0)}{4\pi} \approx -\frac{a_1}{4\beta}\,\rho^{\left(\frac{\pi}{\beta}\right)-1} \tag{1}$$

Where:

σ is the charge density,

ρ is the distance from the corner,

E_φ is the electric field component in the φ direction of the polar (ρ, φ) coordinate system,

a_1 is a constant from the derivation of (1) detailed in Reference [47].

The surface charge density near the "corner" varies with the distance from the corner as $\rho^{\left(\frac{\pi}{\beta}\right)-1}$, where β is the opening angle of the corner. Figure 9 depicts various opening angles of β and the corresponding surface charge density as a function of the distance from the corner, ρ.

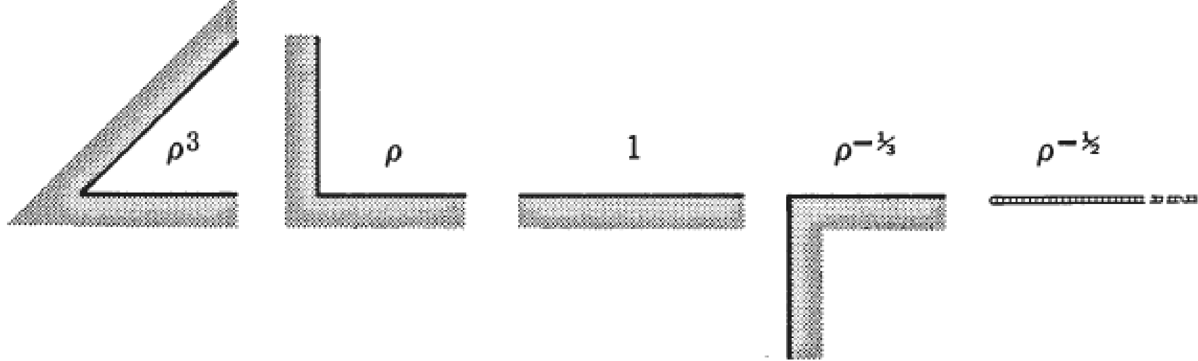


Figure 9. Surface charge density as a function of distance from the corner, shown for various cases of opening angles, β = π/4, π/2, π, 3π/2, 2π [47].

The larger the opening angle (large β), the smaller the exponent on ρ, which means that charge density becomes singular as ρ → 0. Therefore, charges tend to accumulate at the corners by a large extent. That means the field right next to the tip of a pointy electrode is extremely high. This is also the reason why lightening rods are so effective! This 2D problem extends to 3D in a similar way, and the charge density is even greater. Equation (2) shows how the E-field in the adjacent insulator is affected similarly as the charge density in the conductor.

$$E = \frac{-\alpha\pi}{\beta}\,\rho^{\left(\frac{\pi}{\beta}\right)-1} \tag{2}$$

1.3.2 Imperfections in the dielectric

Insulating materials are not physically perfect. They may have voids, or they may have material interfaces where either two insulating materials meet, or where an insulator and conductor meet, or have contaminants (conducting or insulating). These regions can become

charge accumulation sites. In the case of a void, Figure 10 [48] shows how equipotential lines concentrate in the void due to the lower permittivity in the void compared to that in the bulk insulation material. In this lower permittivity region, the dielectric might be air, which has a dielectric strength of 3.0 kV/mm. This means that the void can only sustain an E-field of up to 3 kV/mm. Beyond 3 kV/mm, the air in the void will break down. The typical dielectric strength of an insulation material is between 10-30 kV/mm. Even if the E-field in the bulk material is only 2 kV/mm, the higher concentration of E-field inside the void which has a much lower dielectric strength, will cause a discharge to occur in the void when the E-field in the void exceeds the dielectric strength of the material that is in the void.

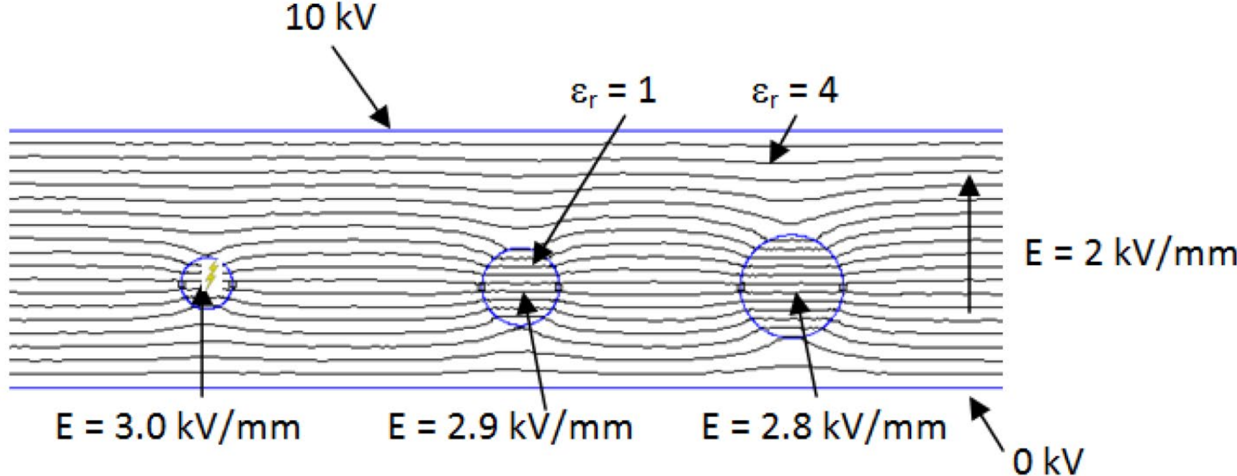


Figure 10. Insulation material model with three voids of different sizes [48].

1.4 Modeling PD

PD has been modeled in a few ways [49]–[60]. While there is no perfect way to do so, some of the methods explored are briefly discussed here. From the electrical point of view there is the three capacitor model, also called the ABC model, that describes the voids in the dielectric as a different capacitor than the bulk dielectric. From the more E-field perspective, there are a few models. Pederson's model considers volume and surface charge density, Conductance model

considers current density, Niemeyer's model considers avalanche and streamer propagation, Plasma model considers fluid equations, and the Numerical simulation model [61]–[66] considers temporal and spatial distribution of electrons and ions and gives the field as a function of pressure and cavity size. It uses fluid equations for electrons and ions including impact ionization, drift, diffusion, attachment, and recombination. All these models have different angles of approaching the modeling problem and while it does give insight into the behavior of PD, which is already hard to predict, there are many factors not included in the models. Pederson's model does not account for time. In the Conductance model, the gas conductivity doesn't accurately model PD. In Niemeyer's model, the E-field is assumed to be uniform inside the void. And in the Plasma model, the PD memory effect is not accounted for. By far the most used model is the three capacitance model, discussed next.

One way to think about field enhancement is to consider the void and the bulk material as capacitors. A void can create a capacitive voltage divider as shown in the equivalent circuit in Figure 11 (a) where C_V is the capacitance of the void, C_X and C_Y are the bulk capacitances between the void and electrode on either side. Since capacitance is directly proportional to the permittivity of the material ($C=\varepsilon A/d$), and a void has a much lower permittivity than that of the insulator, the capacitance of the void is much less than the capacitance of the insulating material. Since voltage across an insulator is inversely proportional to the capacitance of the insulator ($V = Q/C$), there is a much higher potential difference across the void than across the bulk/solid insulating material. In Figure 11 (b), the voltage across C_{air}, where C_{air} and $C_{insulator}$ are in series, is over a shorter distance and therefore, the E-field in C_{air} ($E=V/d$) is much higher than if there were no insulator at all! This is why it is very important to fully fill the gap between two electrodes and not leave any air gap. If an air gap is left, this will cause a breakdown in C_{air}

which can be a partial discharge to the surface of the insulator, or a full breakdown through the insulator.

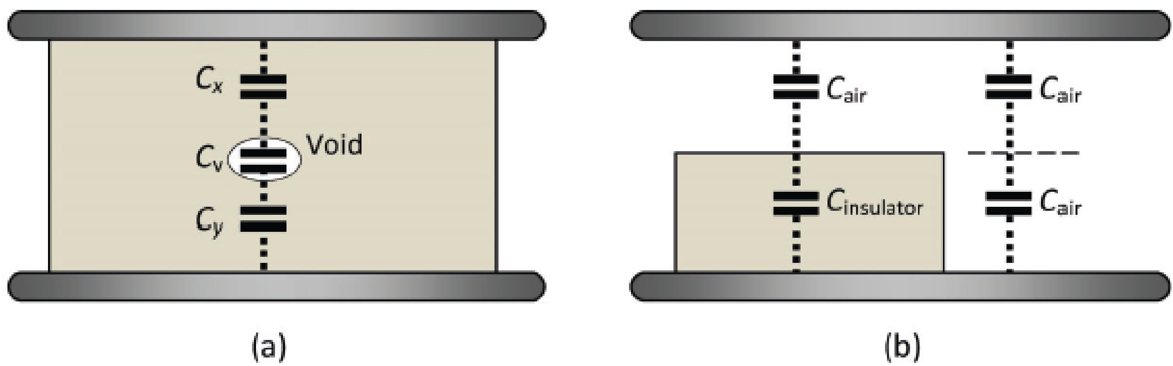


Figure 11. Voids create capacitive voltage division, which enhances the field in the void.

While all these models give us a way to visualize and model PD for computational tools, they don't account for the stochastic nature of PD. PD is stochastic [67], [68] and there are many factors that can contribute to a PD inception that can not or are not easily controlled and therefore hard to build a model around and predict. For example, since charges accumulate at sharp corners, a highly polished conducting surface would have to be perfectly polished to avoid charges collecting at any micro asperity that may remain. For an unpolished surface, PD would likely occur at the sharpest asperities. But when there are many, the choice for the path of least resistance might depend more on the gap between traces, the lack of impurities in the material, the permittivity of the material, the dielectric strength of the material, the change of these material properties at the interface of different materials, etc. The voltage at which PD occurs could be influenced by environmental factors like temperature, pressure, humidity, electromagnetic interference, lightning in the atmosphere, etc. It is also influenced by the voltage profile (DC, AC, dv/dt, etc.) and any power surges. These factors are randomly occurring, and thereby largely unpredictable and difficult to model. Due to this stochastic nature of PD,

empirical tests must be performed and through statistical analysis, conclusions can be derived with a level of confidence.

1.5 PD detection and measurement methods

There are different ways to detect PD [69]. Figure 12 shows some of these options [70]–[73].

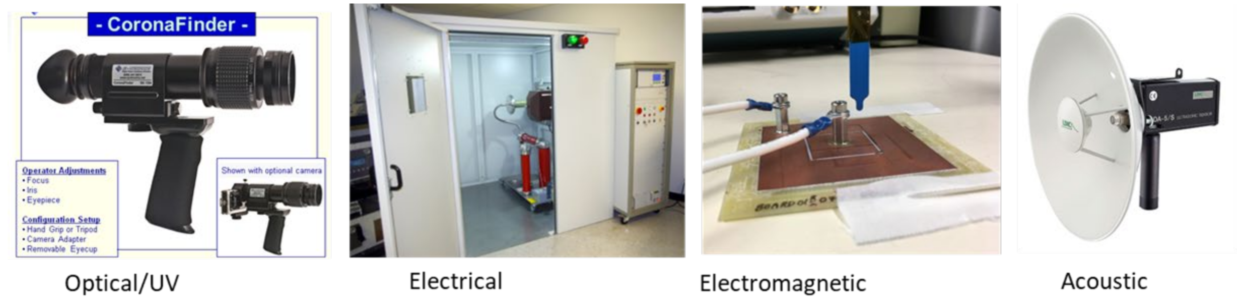


Figure 12. Some of the ways of detecting PD [70]–[73].

PD emits ultraviolet radiation which is visible using a UV detection camera or a corona camera. This method was used to evaluate PD for some of the samples in this work using equipment at the Army research lab [74]. An example set up is shown in Figure 13 where a Syntronics corona finder camera and a Go Pro are set up in a dark room above the sample under test. A Glassman programmable power supply (0-30 kV, 0-400 μA) is used with LabView software to detect leakage current at various voltage levels and determine PDIV.

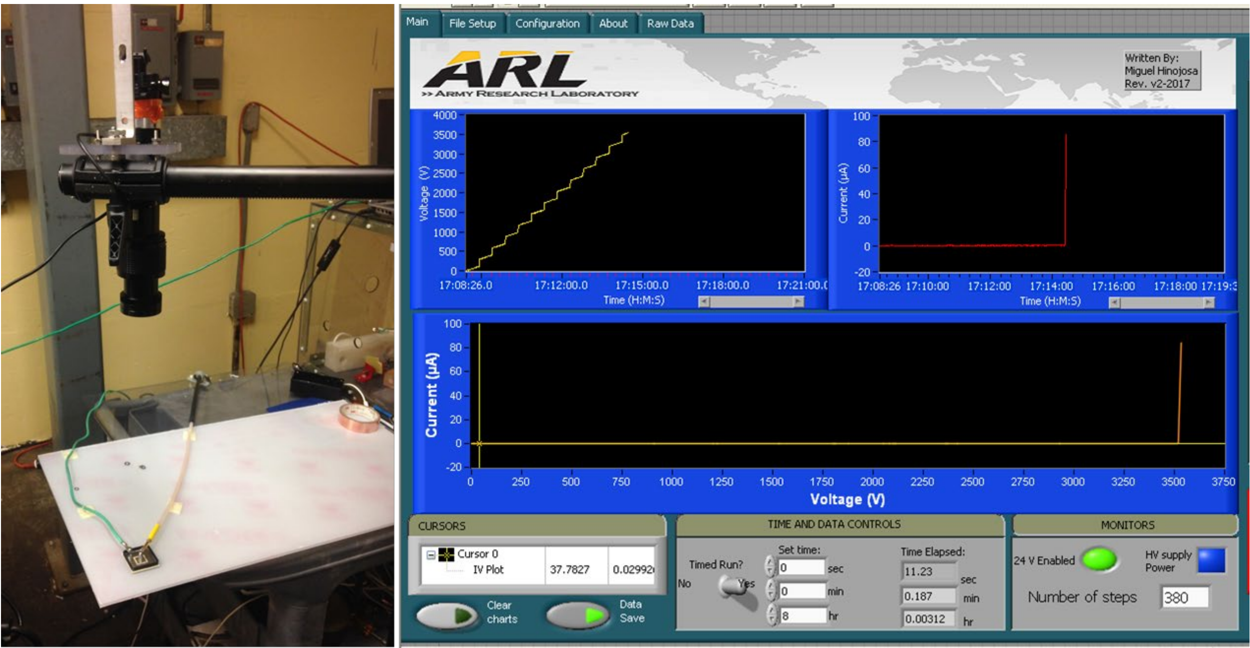


Figure 13. Optical PD test setup at ARL [74].

Another method to capture PD is through the detection of ultra high frequency electromagnetic wave emission using RF probes. A faraday cage can be used to isolate the radiation emitted from the sample and not capture environmental radiation of the spectrum of interest.

PD also emits energy in terms of sound. These sound like little crackling sounds, sometimes heard next to a transmission or distribution line. Corona often occurs on the insulation discs of transmission lines. An acoustic sensor or corona camera can help detect these occurrences.

The most reliable method of detection and quantification is the electrical method detailed in [75], and is also used as the basis for developing PD measurement related standards [14], [76], and implemented by PD measurement equipment manufacturers like MPS, Phenix and Omicron Energy. The main idea is based on the three capacitor model. When PD occurs, a certain number of charges are involved. The circuit is designed such that a capacitor provides the charge needed

for the partial discharge. Sensitive equipment is used to calculate the current in the circuit over the duration of the discharge, and thus determine the charge supplied by the capacitor to fulfill the discharge that occurs in the sample under test or the PD source. This is called the apparent charge. Measuring the apparent charge gives us the closest estimate to the actual charges spent in the discharge. Most of the work in this dissertation is based on this technique. Specialized equipment like those provided by Omicron or MPS can be used for this purpose, or an HFCT can be calibrated and used for high frequency current detection following by integration over time. If the voltage profile is AC, PD tests should be done according to the standards [14], [76]. Figure 14 shows the AC voltage profile required for the test to be IEC 61287 compliant [76]. Here, charge is measured in the last five seconds of the 30s dwell time. A pass/fail criterion is usually provided by the manufacturer. According to IEC 61287, this is typically 10 pC for components and 50 pC for sub-assemblies [76]. The 10 pC threshold was also used by Wolfspeed for PD testing of power module test structures (described in Chapter 4).

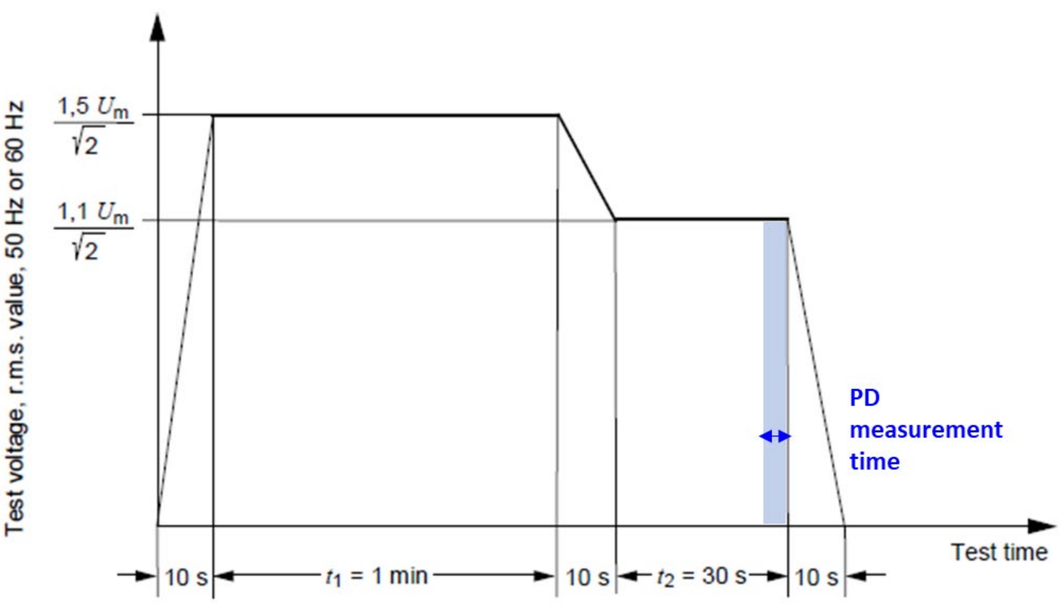


Figure 14. AC voltage profile for AC PD tests according to IEC 61287 [76].

1.6 PD mitigation in power modules

1.6.1 Current strategies

Several research groups have considered PD in power modules [5], [8], [10], [12], [30]–[32], [35]–[37], [39]–[43], [77]. A good power module design accounts for creepage and clearance between the power terminals that are used for connections outside the power module. For PD prevention inside the power module, many researchers have rightly looked into E-field focusing at the triple point [29]–[31], [35]–[37], [40]–[43], [78].

The general practices to mitigate PD at the design stage include substrate stacking [5], guard rings [5], gap extension between the copper edge and the ceramic edge [39], metal layer protrusion past the ceramic edge [36], coatings for field grading [36], stacked substrate patterning [79], and corner filleting [80].

1.6.1.1 Increasing the ceramic thickness

Since E-field in a dielectric is inversely proportional to the thickness of the dielectric, increasing ceramic thickness has an obvious benefit in reducing E-field in the ceramic isolation. Bayer, et al analyzed this effect through simulations of E-field at four different strategic points in a template DBC substrate. They established that E-field near the triple point is roughly inversely proportional to d^0.55 where d is the thickness of the ceramic [40]. The thickest ceramic is about 1 mm and is used as a standard for most applications. The tradeoff here is increased thermal resistance.

1.6.1.2 Substrate stacking

One of the methods for reducing E-field at the triple point is substrate stacking. Dimarino [5] used this method for her 10 kV SiC module. Two 1 mm AlN substrates were stacked, and the middle metal layer was connected to the DC bus midpoint (Figure 15). This reduced E-field at

the triple point by more than 50% compared to a single substrate design. This increased the PDIV of the SiC power module by 53%, allowing it to be operational at 10 kV.

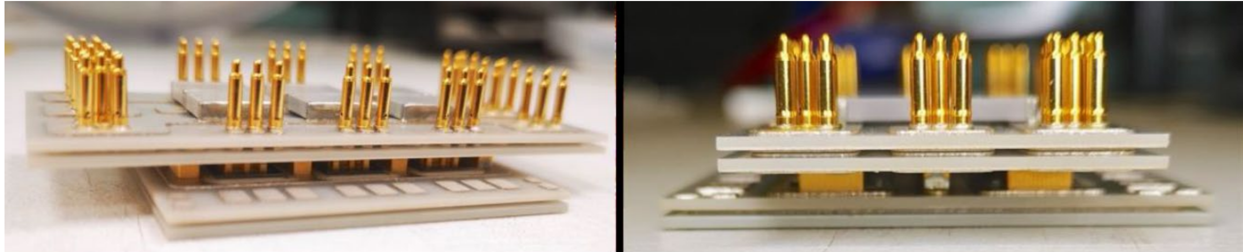


Figure 15. 10 kV SiC MOSFET module prototypes [5].

Deshpande [81] found that stacking many layers of substrates as shown in Figure 16 reduced E-field by 60% compared to that of a single substrate. There is also a diminishing return with the stacking of three layers. Stacking also helped reduce common mode noise.

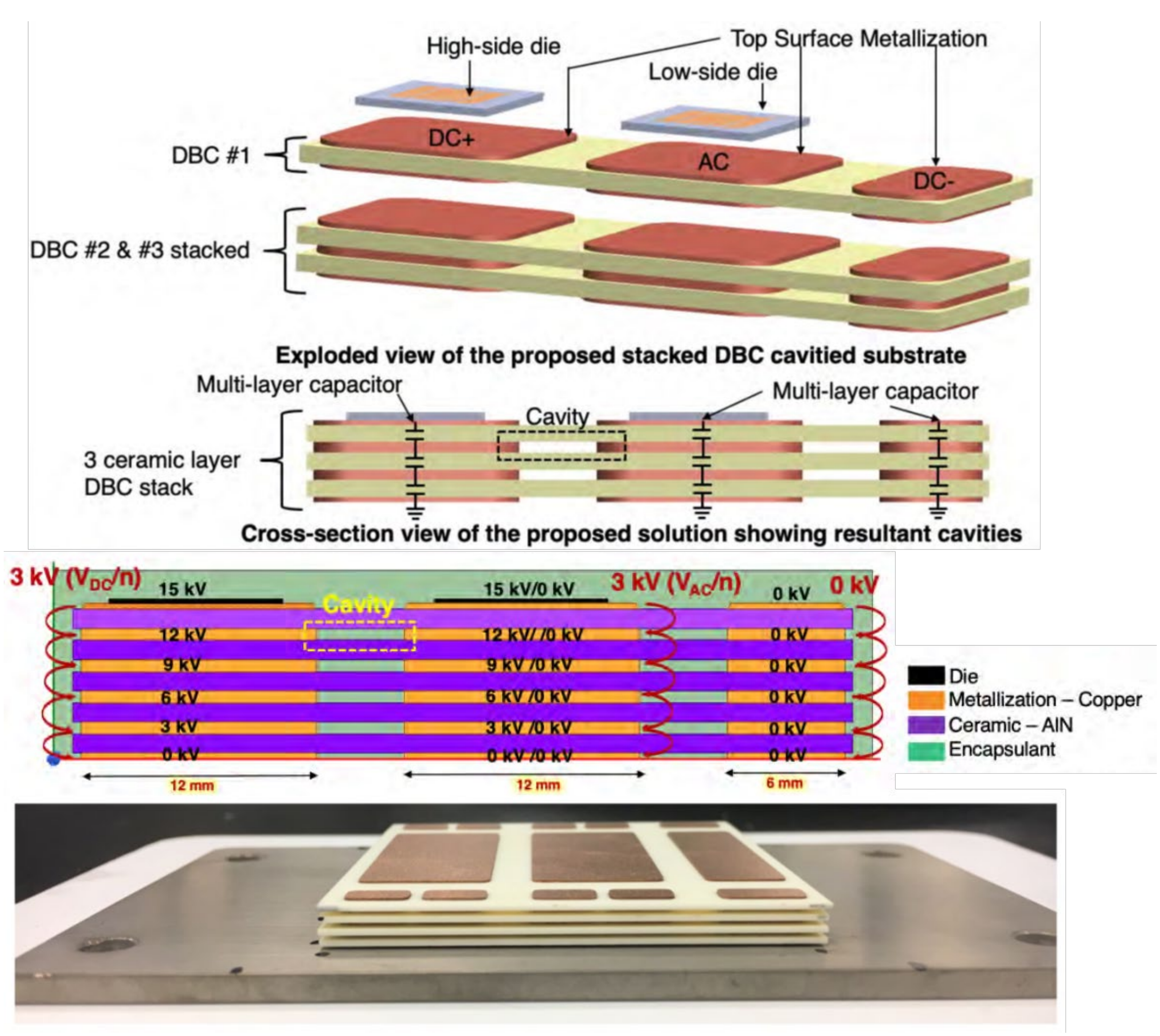


Figure 16. Stacked substrates [81].

1.6.1.3 Stacked substrate patterning

Li, et al [79] used stacked substrates as the default design to build a case for the patterning of the middle layer to help alleviate PD further. The PD tests revealed a 33% improvement in PD for the patterned substrate stack compared to the unpatterned substrate stack.

1.6.1.4 Filleting

Filleting is a standard practice in industry to reduce E-field concentration near sharp corners [82] that exacerbate PD. Several examples of filleted layout traces by various power

module designers are shown in Figure 17. Filleting is also known to reduce stress concentration [83]. But filleting is done as a custom feature for each module's layout; it is not standardized, and the designer must apply these fillets manually at the design stage in a 3D modeling software.

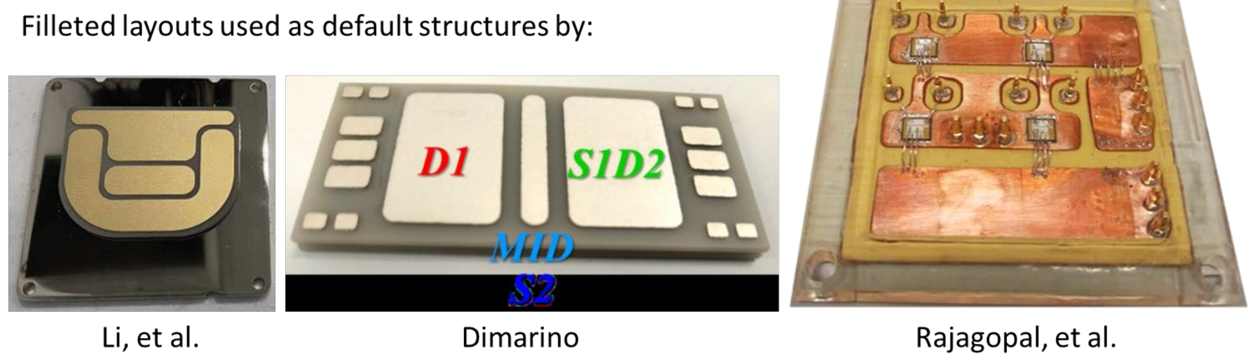


Figure 17. Examples of fillets used in power module layouts [5], [79], [84].

Promoting the cause for a Package Assembly Design Kit (ADK) that is analogous to the Process Design Kit (PDK) commonly used in integrated circuit design, Park, from Cadence, noted in his presentation at the IMPAS conference that "advanced filleting and trace widening" among other things, would be a part of the layout features needed in the ADK [85]. These kits help modern EDA tool flows maintain design rule check decks for integrated circuit design. From these examples, one can observe that though fillets are highly recommended features, they are not currently standardized into any EDA tools.

1.6.1.5 Metal layer offset and protruding metal layer

Researchers at Virginia Tech [36] experimented with changing the size of the copper on the top vs. on the bottom in the lateral dimension parallel to the face of the ceramic-metal interface such that there would be an offset in the triple points at the top side and the bottom side (Figure 18). They found that keeping the top metal layer larger than the bottom metal layer reduces E-field near the top triple point by about 12%.

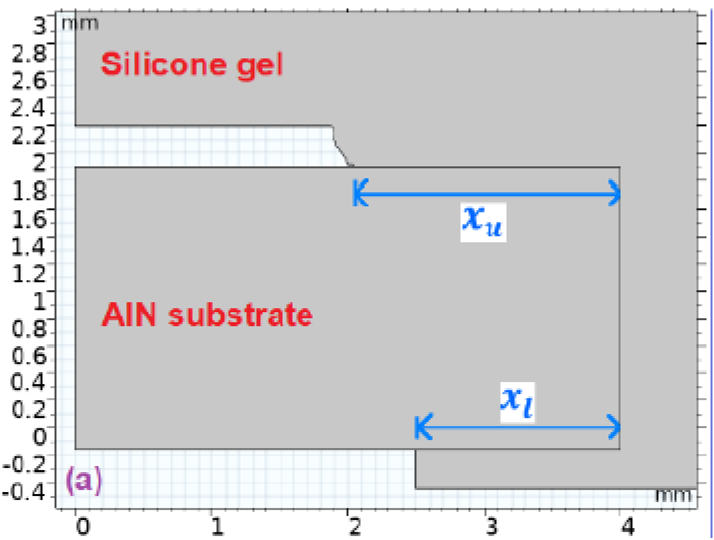


Figure 18. Metal offset between top and bottom layers [36].

Protruding the metal layers past their triple point with the ceramic by adding solder to the edge of the metal, Tousi, et al. found that the E-field in the encapsulant and ceramic were both much higher than the base case where the metal was not protruded. They concluded that geometric modifications were not enough, and field grading was required.

1.6.1.6 Field grading

Tousi, et al. [36] also simulated the application of a field-dependent coating (FDC) as shown in Figure 19. E-field in the encapsulant reduced significantly (about 30%) compared to the case without any coating.

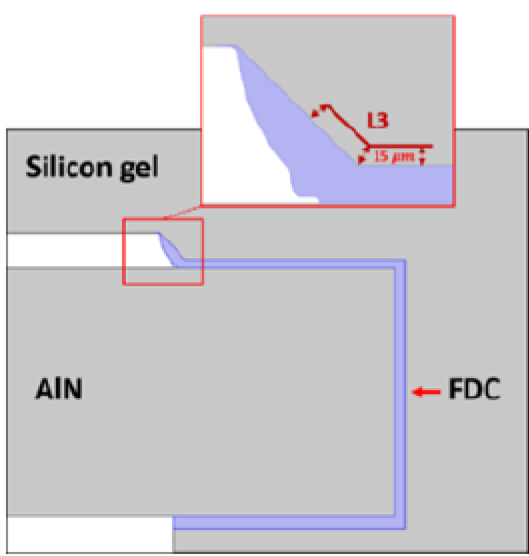


Figure 19. Field dependent coating applied over the triple point and E-field measured at L3 [36].

1.7 The technology gap and how to address it – key contribution and scope

All these methods and intuitive practices for mitigating E-field and PD in power modules are good, but there are no design rules codifying these practices. Since the power module physical design process is automated [3], [86], PD rules need to be accounted for in module design automation. This work is a step toward providing a methodology or approach to account for PD systematically in the design automation of power modules.

One way to design for PD prevention is to consider PDIV as a maximum voltage constraint in the design process of power modules. For cases where the voltage class is already fixed, the material and layout choices can be adjusted. In Very Large Scale Integration (VLSI), design rule checks (DRCs) and process design kits (PDK) are commonplace for the rapid and reliable design of integrated circuits. For power modules, PD-related DRCs can be employed in an analogous fashion, and the voltage class for each material set can be saved in a manufacturing design kit (MDK) library. It is therefore essential to quantify PDIV. And to do so, one must first understand how to model PDIV.

Modeling PDIV is challenging because PD is non-deterministic. A lot of fundamental scientific work has been done in understanding the PD phenomenon at the physical level [46], [54], [61], [67], [87]–[89], especially in modeling the electric field (E-field) inside voids of various geometries. However, PD is stochastic in nature [67], [68] and this is one of the key modeling challenges addressed in this work.

The other modeling challenge is the singularity at the triple point (TP), where it is difficult for a computational tool to converge on an E-field value. There is a high potential difference between the ceramic isolation and the lateral trace gap. Theoretically, E-field concentrates at the triple point due to: 1) Field lensing caused by the change in the dielectric constant of the materials at the TP [46], and 2) Accumulation of charges at the sharp geometric asperities [47] at the TP. Sharp corners are caused by a) active metal brazing, b) the concave profile created by wet chemical etching, and c) the geometry of the corner itself. Researchers have navigated around the convergence issue either by using 2D E-field simulations or by keeping the measurement point (MP) a fixed distance away from the TP [5], [35], [40]–[42], [90]. 2D models can be too simplistic as they do not account for the depth factor, and the fixed distance solution can be challenging if the measurement point (MP) is inside the trace-gap, a variable feature. The convergence issue is overcome in this work in a novel way that is accurate and validated by experiments.

Many of the existing PD-modeling and mitigation efforts consider PD only in the ceramic isolation material of a power module. Since there is a high potential difference across the ceramic isolation material, a breakdown is certainly possible if the isolation layer is not thick enough to withstand the E-field or there are significant defects present. However, the lateral trace gap is also a common site for PD, since a high potential difference exists in the trace gap,

especially when these gaps are being reduced to meet density demands. Experiments done by the authors and corroborated in the literature [42] have shown that breakdown can happen in the trace-gap (Figure 1) even in the presence of a metal plane on the backside of the DBC. The effect of the lateral trace gap on the PDIV of the module is a technology gap that is being addressed in this work.

To date, there are no standardized DRCs developed to prevent PD inside power modules, except for preliminary work done by author based on 2D computational models [77]. In this work, a way to navigate the convergence issues at the triple point singularity while still capturing the effects of the trace gap dimension was found. This was done by considering charge density instead of E-field. An initial charge density vs. trace gap curve-fit model for a simple power module template structure through finite element analysis was developed. In the work presented in this dissertation, a more accurate 3D version of the model was developed in terms of PDIV vs. trace gap that was experimentally validated. Such a relationship addresses the urgent need to formulate PD design rules for power module design.

The key contribution of this dissertation is to provide a method of automating the application of knowledgeable and validated PD-aware layout design rules in an EDA tool for power module optimization. This includes an approach to model PDIV and quantify a voltage class and corresponding trace gap for any chosen substrate-encapsulant layer stack system. Specifically, this includes:

a. a unique way to measure surface charge density through 3D FEA simulations that avoids the challenges of measuring E-field at the triple point,
b. equations to estimate PDIV from surface charge density simulation results,
c. calibration of the PDIV model through experimental results using analysis of the

stochastic nature of PD across multiple identical samples,

d. experimental validation of the trend of diminishing returns in the PDIV vs. trace gap relationship observed in the prediction model, and

e. quantification of the point of diminishing returns in terms of a voltage level and minimum trace gap, validated by experiments.

Furthermore, this method has been implemented in PowerSynth, the in-house built EDA tool for power module layout optimization, and the method is scaled to allow the end user of the tool to change the calibration factor based on their custom manufacturing rules, the PDIV data library for a unique substrate-encapsulant system or layer stack, and the addition of dielectric coating for field grading. These aspects are implemented into the tool's manufacturing design kit much like a PDK for an IC design process. With the implementation of PDIV-based design rules, the user can know what voltage a layout can operate at, and the optimum voltage-spacing combination for a given layer stack and layout.

The calibrated simulations were scaled to include PDIV in the ceramic as well as the encapsulant to determine which one fails first. Such information gives the user insight into how to improve their module's layer stack to achieve higher voltage levels, more compact layouts, or both. A PDIV vs. trace gap plot for the encapsulant and the ceramic is generated for the user to make insightful decisions.

These contributions enable the development of design rules for power modules specific to PD mitigation. The methodology used to develop the PDIV model paves the way for the future development of more comprehensive design rules that can be added into the MDK as power module architectures mature.

The scope of this work is limited to:

- Simple trace geometry with a parallel trace gap, not the diagonal gap between one corner of a trace to that of another or a curved trace.
- Vertical-trace-etch face instead of the concave wet-etch profile, to ease calculations and avoid numerical convergence issues.
- Finding the *voltage* at which PD begins instead of the exact *location* where it happens.
- A calibration factor that validates the simulation template, manufacturing method, and testing method, but not each individual simulation for all combinations of materials and geometries (that would take a significant amount of time and is not the main point of this work).

Ideas for broadening the scope is this work are provided in the future work section of Chapter 5.

Finally, layout solutions that were exported from PowerSynth to external tools like Ansys Electronics Desktop are now filleted for maximum PD mitigation. Instead of needing to do them manually, the geometry of the layout is evaluated, and fillets are sized correctly and applied. The filleting practice is thus more standardized than before, and automated, so the user does not have to manually fillet each trace edge of a complex layout, saving significant design time.

The main contributions of this dissertation are divided into chapters: a unique PDIV modeling approach (Chapter 2), automation-driven layout trace-gap design rule development approach and implementation in PowerSynth (Chapter 3), and fillet implementation automated in PowerSynth (Chapter 4). Future work ideas are listed in the final chapter (Chapter 5).

Chapter 2. Partial Discharge Inception Voltage Modeling Approach

This chapter goes into the details of the modeling process of PDIV, and the validation of the model using physical PD tests. First, the overview of the modeling process is presented using a block diagram, which is then expanded in the subsequent sections. This includes the explanation for the modeling approach through 3D FEA simulations and application of physics equations to derive PDIV, followed by the calibration of the model through experiments on physical test coupons, which validate the model.

2.1 PDIV Modeling Approach Overview

The methodology presented in this work is a way to model PDIV vs. trace gap for any combination of:

- Technology (substrate and encapsulant combination) and
- Manufacturing process.

This approach involves determining the PDIV vs. trace gap relationship computationally using the PDIV model and then validating the relationship experimentally. Calibrating the computational model to PDIV lab test results using a calibration factor will validate the relationship. A couple of closed-form equations are used to model PDIV computationally. These equations take surface charge density values extracted from 3D FEA simulations of a simple DBC-encapsulant test structure and transform the values into PDIV. The calibration factor predicts the voltage at which PD begins relative to the theoretical breakdown voltage.

The approach to model PDIV is summarized in Figure 20. A patterned and encapsulated DBC test coupon is simulated in ANSYS Maxwell, a 3D FEA software. The trace gap (tg) is varied, and the surface charge density (Q_{surf}) is recorded for each trace gap. Q_{surf} is then transformed into PDIV using appropriate material properties such as dielectric constant (ε_r) and

dielectric strength (E_{DS}). The predicted PDIV values ($PDIV_{PRE}$) are in terms of the calibration factor, ***k***, which predicts PDIV as a fraction of the theoretical breakdown voltage. The ***k***-value incorporates practical aspects that can not be simulated such as material defects, manufacturing-related artifacts, excitation profile, and environmental aspects. The simulated DBC test coupon is then built physically with multiple identical samples for each trace gap to perform a statistical analysis. PDIV tests at 10 pC charge level are conducted on all the samples, and a Weibull statistical analysis is performed to determine the characteristic PDIV ($PDIV_{EXP}$) for each trace gap.

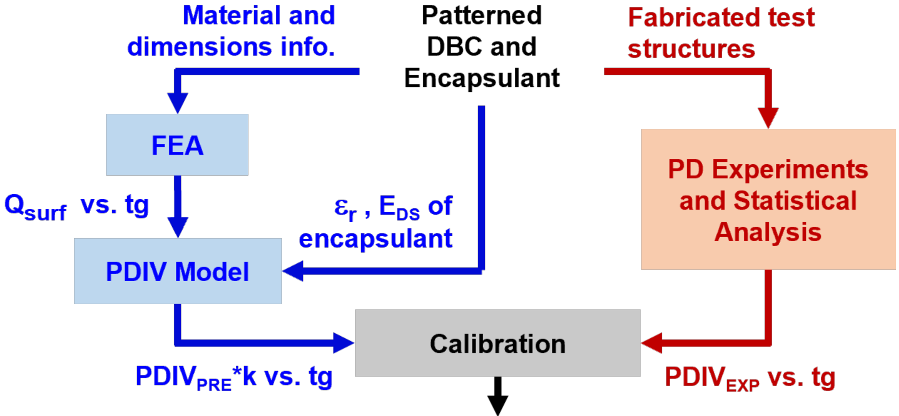


Figure 20. Overview of the PDIV modeling methodology

Juxtaposing the predicted PDIV vs. trace gap curve with the experimental PDIV vs. trace gap curve, the ***k***-value can be found through regression analysis to close the offset. This work demonstrates this methodology using the example of a 12/25/12 mil alumina DBC and Dow Corning 3-6635 dielectric gel built in a university cleanroom facility.

Once the PDIV model is validated, the PDIV vs. trace gap curve can be used to determine the voltage class and trace gap design rules for the technology and manufacturing process selected. The PDIV vs. trace gap curve shows an expected trend of diminishing returns, which is

validated through experiments. There is a point past which increasing the trace gap further will not have any PD-related benefit. This point of diminishing returns is quantified in terms of the trace gap and the corresponding PDIV value. For reliable operation, module voltage must not exceed this PDIV value.

2.2 PDIV Model Derivation from Surface Charge Density Simulations

A modified power module building block was modeled in ANSYS Maxwell 3D simulation software, and a surface-charge density-based PDIV model was derived. The 3D model geometry designed for the simulations matched the samples that were to be fabricated.

2.2.1 Test Structure Design, 3D Model Geometry and Excitation

Figure 21 and Figure 22 show the test structure used for modeling partial discharge in the encapsulant material, and the specific measurements of the sample to be built for simulations and physical testing.

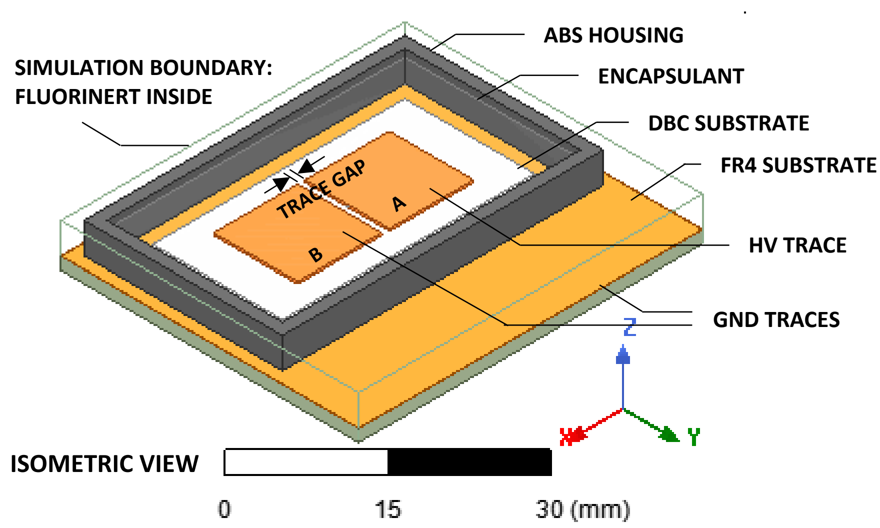


Figure 21. Isometric view of a 3D model of the power module test structure

The DBC (12/25/12 mil Cu-Al_2O_3-Cu) from Figure 1Figure 1 was attached to the top of a single-sided copper-clad FR4 board to allow easy access for electrical connection to the backside

of the DBC when performing physical tests. A plastic housing was attached to the FR4 board surrounding the DBC to hold the gel encapsulant. The encapsulant used for simulations and experiments was Dow Corning 3-6635 dielectric gel. The remainder of the region inside the simulation boundary was assigned the dielectric fluid material chosen for experiments: 3M's fluorinert FC-3283.

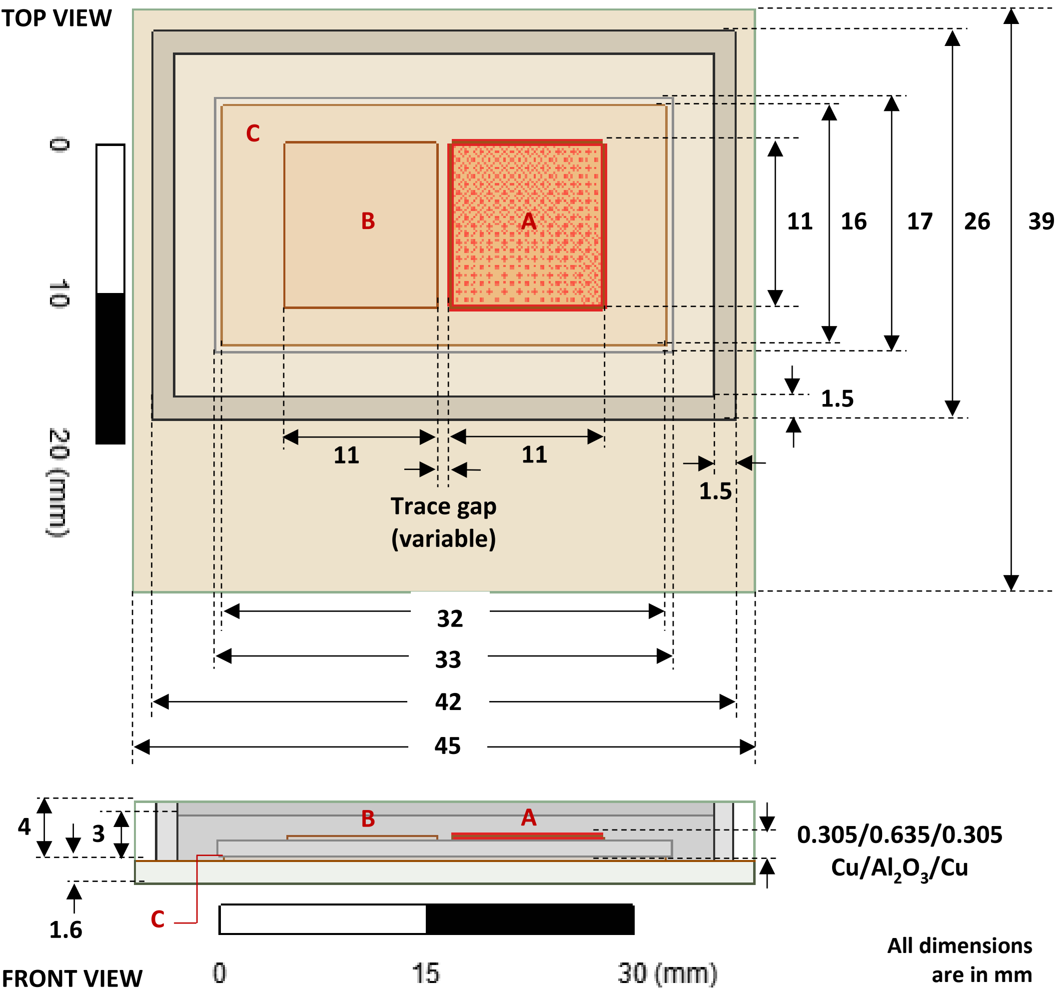


Figure 22. Top view and front view of the power module building block 3D model prepared for simulations.

The traces in Figure 21 and Figure 22 are marked A, B, and C. Traces B and C were held at ground potential, while Trace A was connected to a variable voltage with respect to ground.

The voltage excitation on Trace A is the stimulus, and all responses, such as E-field in the trace-gap and surface charge density on the trace, are directly proportional to this excitation. Because of this relationship, the voltage was kept constant at 1 kV. Since the gap between the traces is measured in mm and the dielectric strength of materials is measured in kV/mm, the excitation on Trace A was measured in kV for ease of calculations.

2.2.2 PDIV Derivation from Simulations

The spatial point in the 3D model geometry where the response is measured is called the measurement point (MP). PD is stochastic and its actual location, onset voltage, exact magnitude, etc. are random. Because of its stochastic nature, it is impossible to predict exactly where PD will occur. The purpose of this work is to derive a working approximation of the *voltage* at which PD will begin, discussed next, without spatially locating the PD event exactly. However, there is general wisdom about where PD is likely to occur, and the measurement point location was chosen accordingly, and is described later in this section.

2.2.2.1 PDIV Determination from Local E-Field

Most industrial designs factor in a safety margin based on the breakdown voltage of the materials the insulation is made of. Since PD happens before breakdown, this margin may or may not incorporate PDIV. But it should be incorporated because, as shown before, PD is a silent and destructive phenomenon, and progressive PD leads to breakdown. Each insulation material has a dielectric strength prescribed in its datasheet, which tells us that under ideal conditions, if the E-field in the material exceeds that threshold, the material will break down. Often, with simple geometries, the breakdown voltage can be predicted using the $V_{BD}=E*d$ equation where E is the dielectric strength of the insulation material, d is the thickness of the insulation material between two parallel conducting plates, and V_{BD} is the breakdown voltage.

This only works for uniform E-fields. E-field in the insulation material may not be uniform. E-field may concentrate in certain regions due to various factors including intentional geometric features, geometric defects, material defects, etc. There is also a back side metal that influences the E-field distribution. The local E-field in an encapsulant material near a sharp metal edge or in a void inside an encapsulant is much higher than the E-field in the bulk of the insulation material. This is due to the concentration of surface charges at sharp corners [47] and the resulting E-field nearby, and due to the reduced permittivity in the void of the encapsulant compared to the bulk encapsulant, respectively. These regions become PD nucleation sites, and a much lower voltage across the insulation material would drive breakdown in those specific regions. Finding the voltage at which the E-field in these nucleation sites exceeds the bulk dielectric strength of the material is important in determining a better safety margin that incorporates the likelihood of PD. When the material breaks down only in a small local region of the larger insulation, it is a partial discharge. In this work, E_{LOCAL} is defined as the E-field in such local regions of interest for a 1 kV applied voltage, E_{DS} as the uniform dielectric strength of the bulk insulation material (as prescribed in its datasheet), and $V_{BD,LOCAL}$ as the applied voltage that pushes E_{LOCAL} to the E_{DS} threshold of the material, causing a local breakdown. We express this as:

$$V_{BD,LOCAL} = E_{DS}/(E_{LOCAL}/1kV) \quad \text{Equation 2.1}$$

This local breakdown is essentially a partial discharge because it does not bridge the gap between the conductors. PD is a precursor to the actual breakdown of the entire encapsulant material, but $V_{BD,LOCAL}$ is a theoretical value based on simulations of perfect materials and geometries, and can not be considered as the PDIV. Also, the E_{DS} value in the datasheet is based on ideal conditions; the actual dielectric strength of the material is much lower. Therefore, a practical assessment to help calibrate PDIV is needed. In this work, PDIV is assumed to be

proportional to and a fraction of the theoretical breakdown voltage, $V_{BD,LOCAL}$, and needs to be accounted for in the safety margin. This is expressed as:

$$PDIV = \boldsymbol{k} * V_{BD,LOCAL} \qquad \text{Equation 2.2}$$

where $\boldsymbol{k}$ is the proportionality constant or calibration constant that represents the fraction of the local theoretical breakdown voltage at which partial discharge inception practically occurs. It incorporates physical aspects of materials and manufacturing, as well as operational factors such as the excitation profile and the environment. These factors are discussed in a later section.

In this study, E_{LOCAL} was derived from the surface charge density on the adjacent metal trace, described later. In the following section, the decision on where to reliably measure a response is described.

2.2.2.2 Measurement point location determination

As mentioned before, E-field in the encapsulant is not uniform. It concentrates near sharp metal corners and in voids. Voids are randomly found in the encapsulant whereas sharp corners exist by design. Therefore, it is easier to model sharp corners and edges. The etched profile of DBC traces contains sharp edges. Charges accumulate here, and the E-field in the encapsulant adjacent to these sharp edges is much higher than the E-field in the bulk encapsulant.

The TP is the most likely location for PD as shown in literature [46], [47]. However, in this work, the authors did not place the MP at or very close to the TP, or even in the trace gap, because: 1) the E-field and surface charge density at geometric sharp corners of conductors are theoretically *infinitely* high [47], 2) the gradients of E-field and surface charge density *near* geometric corners and triple points are extremely high, and 3) the mesh density at sharp corners is extremely high and inversely proportional to the trace gap size. The MP must be chosen carefully so that it reflects the effect of design parameters like trace gap on the E-field at the TP

without being dominated by singularity effects of the physical phenomenon or numerical effects from the changing mesh density. To accommodate all these constraints, the authors avoided putting the MP in the trace gap within the insulating material, but rather on a conductive surface, away from any triple points, and in a place where the mesh density would be relatively more constant with the change of the trace gap while registering the effect of the trace gap. To get more consistent values by reducing the error due to the way the simulation works, the MP location was adjusted. Considering these constraints, the general location to place the measurement point, therefore, is on the vertical face of the higher potential trace that is next to the trace gap. To avoid the effect of singularities and to have a common reference point instead of one that changes with the design, the location chosen for this work for the MP is in the middle of the vertical face of the higher potential trace, facing the gap (Trace A in Figure 23). This location for MP also offers versatility for various more complex designs including flip-chip or multi-layer geometries.

Since the MP is on a conductor (Figure 24), surface charge density is the appropriate direct parameter to be measured, from which E-field can be derived. This derivation is described in the next section. The mesh around the MP is indirectly controlled. It is driven by the maximum number of mesh elements, the minimum size of the elements, and the convergence criteria. Performing a mesh analysis, these factors were varied for a 0.1 mm trace gap. Once a stable charge density output was reached, the mesh settings were kept the same for all other simulations of trace-gap variation. Controlling the mesh using these driving factors, any changes in the surface charge density response were primarily due to changes in the design parameter (trace gap) instead of the numerical noise.

There are limitations in representing PD through simulations. PD is usually assumed to

be at the TP. But since simulations cannot predict the exact location where PD will happen because simulations cannot predict material defects, we must assume that PD will happen either in the encapsulant or in the ceramic close to the metal trace, and that the onset of PD is at a fraction of the theoretical breakdown voltage of that material. Even if breakdown happens at the TP, the E-field at the MP is still proportionate to the E-field in the TP according to simulations in this work. So, the simulations can capture the trend, if not the exact value. That is why the proportionality constant, ***k***, is used to account for factors beyond the scope of this work and lab tests are used to calibrate simulation results with experimental data. The experiments validate the trend predicted by the simulations. The ***k***-value can depend on the manufacturing quality of the materials which cannot be predicted by simulations.

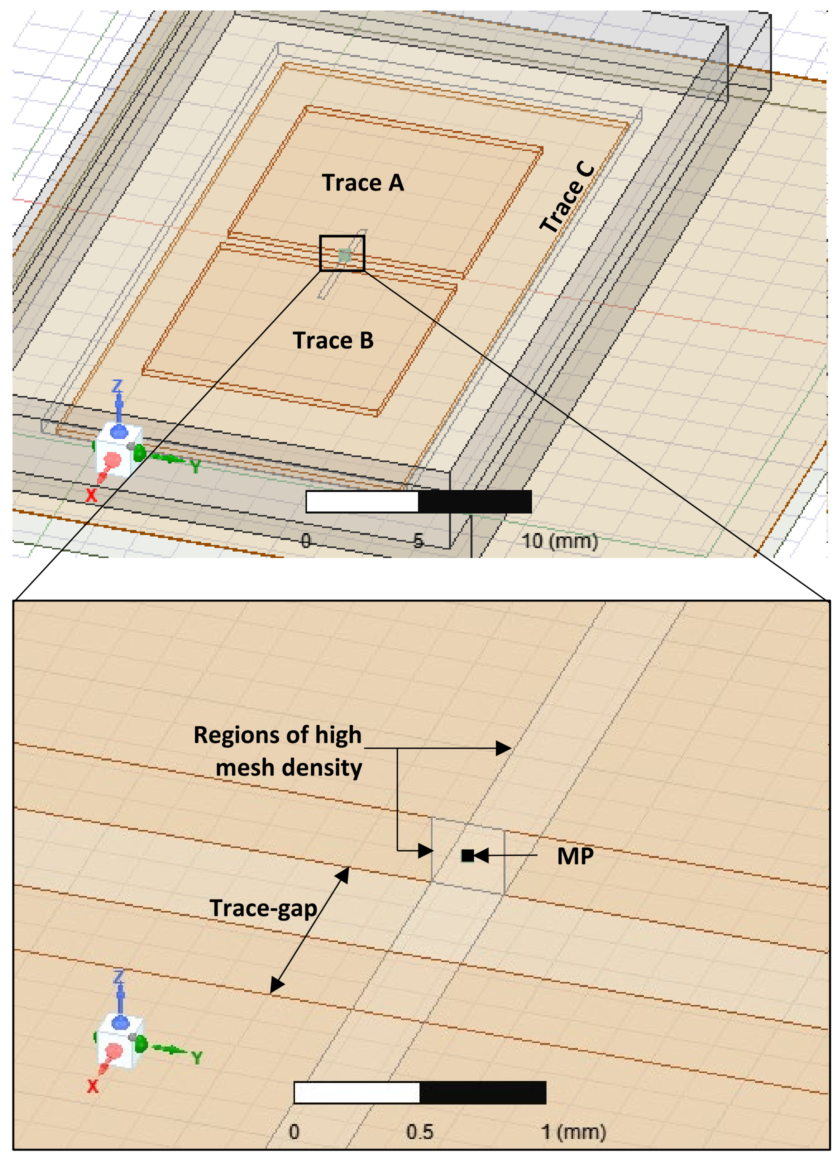


Figure 23. Location of the MP in the 3D model and a close-up of the MP location.

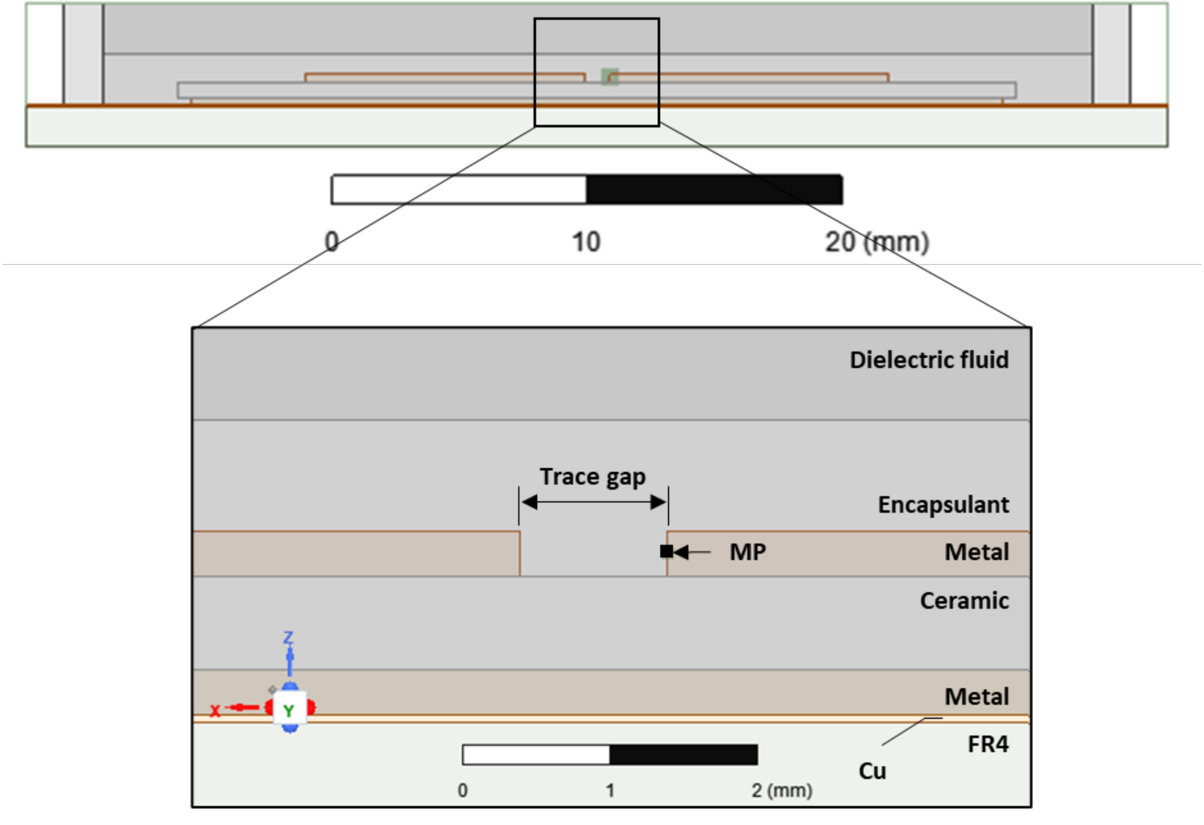


Figure 24. Cross-section of the x-z plane of the module model (Figure 23), showing a close up of the location of the MP and the layer stack up.

2.2.2.3 Local Electric Field Derivation from Surface Charge Density

According to Gauss's law, the electric flux across any closed surface is proportional to the net electric charge enclosed by that surface. Assuming a small bounding box is drawn around the MP, the net flux perpendicular to the box is equal to the net charge enclosed by the box. The physical meaning of the differential form of Gauss's law relates electric field to charge distribution. Using this concept, one can derive that the local E-field in the insulating material adjacent to the MP is proportional to the surface charge density over the conducting surface bounded by the imaginary box. Equation 2.3 shows this relationship, where Q_{surf} is the surface charge density at the MP in C/m^2, E_{LOCAL} is the calculated E-field in the insulating material

adjacent to the MP in kV/mm, $\varepsilon_0\varepsilon_0$ is the permittivity of free space in F/m, and ε_r ε_r is the relative permittivity of the encapsulant material. This is the response for an excitation of 1 kV.

$$E_{LOCAL} = Q_{surf}/(\varepsilon_0\ \varepsilon_r) \qquad \text{Equation 2.3}$$

E_{LOCAL} is directly proportional to the excitation voltage, V_a. As V_a increases, E_{LOCAL} scales proportionately. As discussed before, the V_a for which E_{LOCAL} reaches the threshold E-field of E_{DS} is called the $V_{BD,LOCAL}$. For electrical reliability, V_a must stay well below the $V_{BD,LOCAL}$ threshold. In fact, it must stay below the PDIV threshold where partial discharges of a fixed charge level (typically 10 pC) begin. The ***k***-value in Equation 2.2 determines how far below $V_{BD,LOCAL}$ the PDIV threshold should be.

Another way to look at the ***k***-value is as a ratio of the PD strength of the material and the breakdown strength of the material. Equation 2.4 shows one way to relate the E-fields. It is analogous to Equation 2.2 where ***k*** is a ratio of the local breakdown voltage to the PD inception voltage of the material. Depicting it this way emphasizes that there is a threshold E-field below the traditional dielectric strength of the material, and this is the threshold being proposed as a design constraint in this work.

$$E_{PD} = \boldsymbol{k} * E_{DS} \qquad \text{Equation 2.4}$$

The ***k***-value is a derating factor that is dependent on many factors including materials and manufacturing processes, simulation settings such as mesh density, and environmental factors such as temperature and pressure, etc. It helps calibrate the simulation settings to the experimental results for a specific material set, manufacturing process, excitation profile, and environment. The ***k***-value thus determined can be transferable for reasonably similar materials, processes, excitation and environment. And, for a significantly different material set, manufacturing process, excitation profile and environment, the methodology presented in this

work can be used to determine an appropriate ***k***-value. This "***k***" is the same as the one in Equation 2.2.

This work shows an example of how to determine the ***k***-value for a simple test structure where the design parameter (in this case, trace gap) changes, while the materials remain the same, and the manufacturing, environmental factors, and simulation settings remain mostly the same, though not perfectly controlled since that is outside the scope of this work. The ***k***-value accounts for mesh differences across data sets to relate the simulated E-field values to the practical breakdown strength.

FEA simulations were performed to determine the surface charge density at the MP. The local E-field was then derived from it using Equation 2.3. The local breakdown voltage is determined by comparing the local E-field to the dielectric strength of the material, as in Equation 2.1. Finally, the PDIV is determined by using hypothetical values of ***k*** applied to the local breakdown voltage, and later calibrated using experiments.

2.2.2.4 Simulation Parameters

Table 1 shows the various parameters that were varied and by how much. Some of the parameters affect the layout, while others affect the technology (the vertical stack of materials). Trace-gap is a parameter that affects the layout, and its limits define the design rules for the trace gap. The layer stack Figure 21. Isometric view of a 3D model of the power module test structure is usually pre-set by the user in the MDK before layout options are explored. For this example, a 12-25-12 mil Cu-Al_2O_3-Cu DBC and a Dow Corning 3-6635 dielectric gel were used as the technology. Their physical properties are mentioned in Table 1. The same materials were used for physical experiments to calibrate the ***k***-value. For the scope of this work, the trace-gap was varied between 0.1 mm to 8.0 mm, and the surface charge density was recorded as the response.

In the physical experiments, trace gap was varied between 1 mm and 3 mm to compare the trend of PDIV between the simulated and experimental cases.

Table 1. Simulation Parameters

Parameter	Unit	Value or range	Category
Trace gap	mm	0.1 to 8	Layout design rule
Voltage	kV	1	Stimulus
Ceramic thickness, t_c	mm	0.635	Technology
Encapsulant relative permittivity, ε_{rEnc}	-	2.83	Technology
Ceramic relative permittivity, ε_{rCer}	-	9.8	Technology
Metal layer thickness, t_m	mm	0.3048	Technology
Surface charge density	C/m^2	-	Response

2.2.2.5 Limitations

The simulations do not explicitly account for temperature, pressure, or other environmental factors. They only consider factors like trace gap and material thickness, and geometric features that are part of the designable parameters.

2.2.3 Simulation Results and PDIV Calculation

Constants were set as mentioned in Table 1, and the trace gap was varied. The surface charge density value on the MP was recorded. Figure 25 depicts the surface charge density field plot and mesh density around the MP for a 1 mm trace gap. Using 20 kV/mm as the breakdown strength of the dielectric gel (E_{DS}) [91], Equations 2.3, 2.1, and 2.2 were applied to obtain PDIV in terms of the calibrating factor, k, as shown in Table 2. PDIV vs. trace gap was plotted for various ***k***-values in Figure 26.

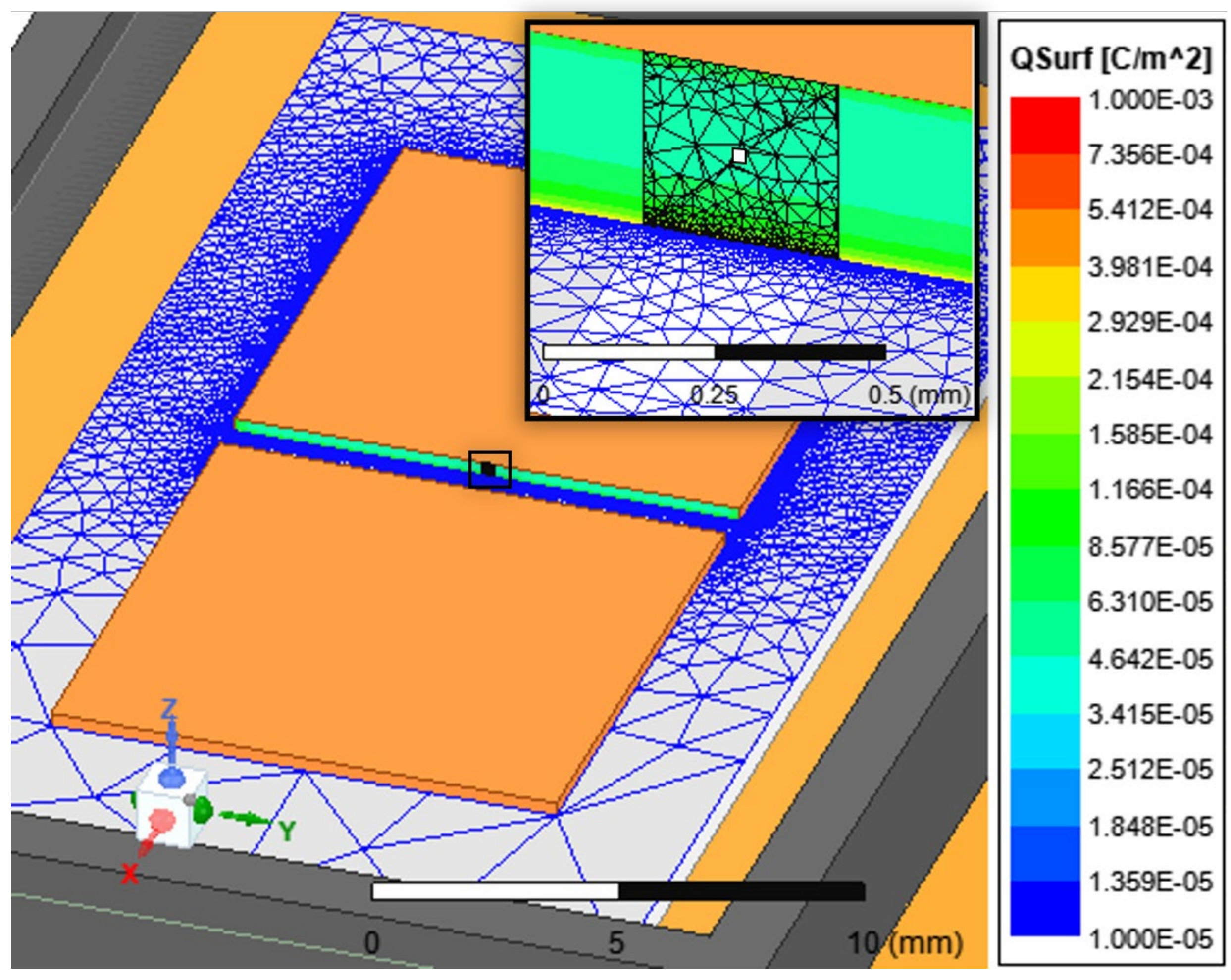


Figure 25. Mesh and surface charge density near the measurement point for a 1mm trace gap; inset: close up of the measurement point.

Table 2. $PDIV_{PRE}$ derived from Simulation Results of Q_{surf} for Various Trace-Gaps for a 12/25/12 alumina DBC with Dow Corning 3-6635 Gel Encapsulant

Trace-gap (mm)	Q_{surf} ($\mu C/m^2$)	E_{calc} (kV/mm)	PDIV (kV)
1.0	54.0720	2.16	9.27 * ***k***
2.0	51.0926	2.04	9.81 * ***k***
3.0	50.9806	2.04	9.83 * ***k***

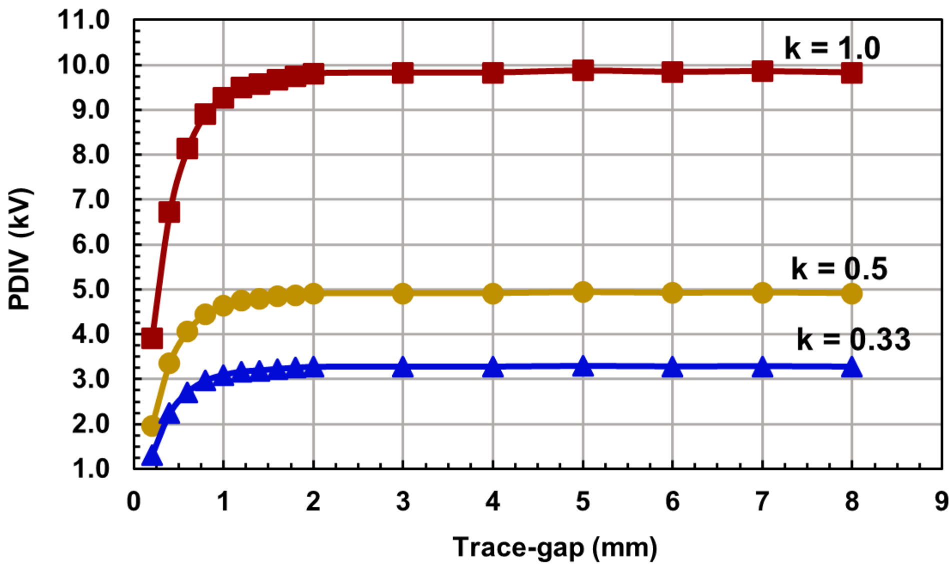


Figure 26. PDIV vs. trace gap results derived from the PDIV prediction model for a 12/25/12 alumina DBC with Dow Corning 3-6635 gel encapsulant for various k-values.

The plot shows that as the trace gap increases, PDIV increases. This makes sense because E-field and surface charge density are inversely proportional to the gap between the conductors. However, according to the simulations, beyond a particular trace gap, there is practically no impact on the PDIV as the PDIV reaches almost a steady state. This, too, makes sense, as factors besides the trace gap dominate beyond this point.

Since PDIV constrains the operating voltage, increasing the trace gap past this point has no benefit in terms of the operating voltage. Conversely, decreasing the trace gap below this point has significant implications for the operating voltage. This point of diminishing returns is specific to the technology and processes and must be determined experimentally. The next step in the methodology is to determine the ***k***-value experimentally for the chosen technology set and manufacturing process.

2.3 PDIV Experiments

To calibrate the PDIV model derived from simulations and validate the PDIV vs. trace

gap trend, three different trace gap variations were chosen to be built and tested for PDIV at a 10 pC PD threshold. One of these points (1 mm trace-gap) was in the rising region of the curve in Figure 24, while the other two (2 mm and 3 mm trace gaps) were in the steady-state region. Ten samples for each design variation were tested and analyzed statistically using Weibull plots according to IEC 62539 [92]. The experimental and predicted PDIV values were compared to determine the ***k***-value. This section describes the design and fabrication of test samples, test setup, test results, and statistical analysis. The next section will use the results from this section and the previous section to calibrate the simulations and validate the modeling approach.

2.3.1 Test Structure Design

Ten identical samples of each variation on a design parameter need to be built for statistical analysis. For the three trace gaps, the total number of samples would be 30. The 3D model that was simulated was originally designed with physical fabrication and experimental validation in mind. The main feature is the trace gap. The traces themselves need to only be large enough to hold the terminals on which voltage is applied. Zinc-Plated Brass Female Threaded Hex Standoffs [93] were chosen as the terminal type, and their diameter largely determined the width and length of the traces. Figure 27 shows the general structure to be built. To keep some additional gap between the parts of the terminals that stick out in the air, some tolerance was added to the trace length and width. To keep sufficient overhang of the ceramic compared to the metal edge on both sides of the ceramic, which prevents surface tracking over the ceramic edge, the copper pullback distance was 5.5 mm on each side for a 1 mm trace gap. This would vary depending on the trace gap, since all other dimensions are constrained. For the 3mm trace gap samples, the copper pullback distance would be 4.5 mm on either side.

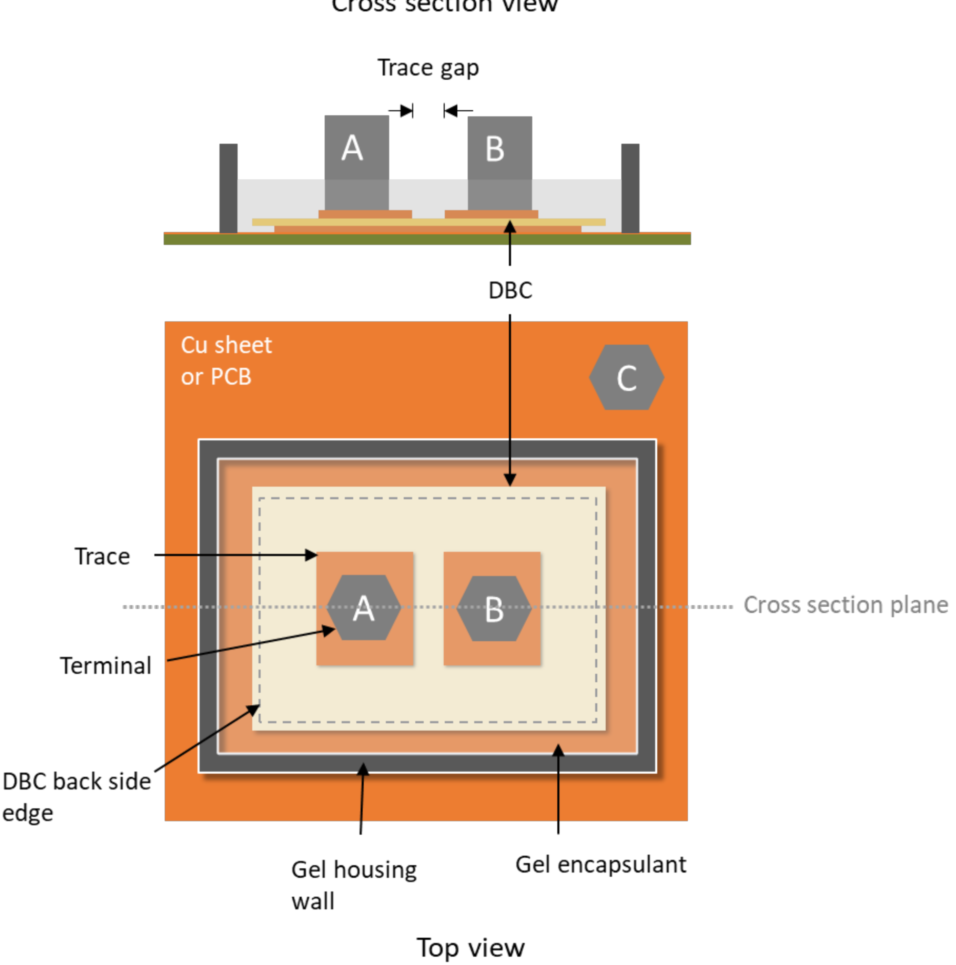


Figure 27. Rendition of the sample to be designed with leads

The specific steps to design the samples are detailed in the Appendix H. The DBC etch pattern is designed in AutoCAD, later to be printed on a photomask. The FR4 baseboard cutouts are measured out in an AutoCAD file for space budgeting. The gel housing is designed in SolidWorks for printing later using a 3D printer.

2.3.2 Test Structure Fabrication and Assembly

The test structure fabrication includes the following steps, and they are detailed in Appendix I:

- Preparation of FR4 baseboard for each sample (Appendix I.1)

- Patterning and etching of DBC test samples (Appendix I.2)
- Attachment of base and terminals (Appendix I.3)
- Encapsulation of the trace gap and DBC with dielectric gel (Appendix I.4).

The steps for patterning and etching the DBC test samples are outlined in Table 3 and the step by step instructions for the patterning process are provided in the appendix.

Table 3. Overview of the dry film photolithography, DBC pattern etching, and dicing process

Step no.	Action	Materials and equipment needed
1	Print photomask pattern	Photoplot transparency sheet, photoplot printer, AutoCAD design.
2	Prepare equipment	Chemcut spray etcher, UV light exposure unit, dry film laminator.
3	Laminate DBC master cards	Dry film photoresist, brown paper, DBC master cards, laminator, IPA, lint-free wipes.
4	Expose dry film laminated DBC master cards to UV	Photomask, laminated DBC master cards, clear tape, UV light exposure unit
5	Develop dry film photoresist on DBC master cards	Exposed DBC master cards, developer solution, developer tank with agitator, IPA, lint-free wipes.
6	Etch developed DBC master cards	Dry film developed DBC master cards, Chemcut spray etcher.
7	Strip dry film photoresist off DBC master cards	Etched DBC master cards, dry film stripper solution, IPA, lint-free wipes, storage container.
8	Dice DBC master cards to get DBC samples	DBC master cards, dicing machine and dicing blades, wafer mounter.

Some of the final samples once built are shown in Figure 28.

Figure 28. Samples after the dielectric gel curing process, and ready for testing.

2.3.3 Test setup and execution

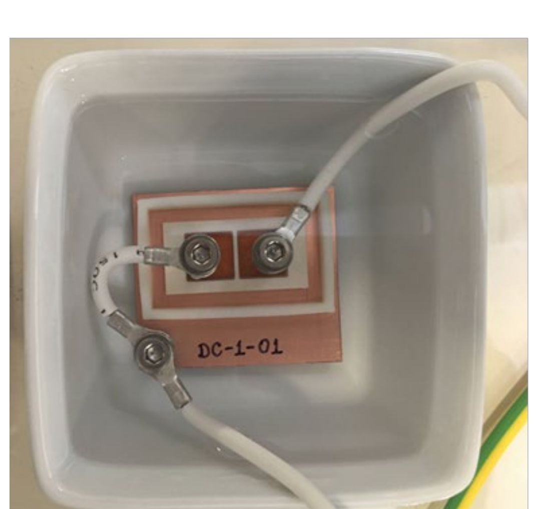
The purpose of these tests was to measure the partial discharge inception voltage (PDIV) for various "identical" test samples under "identical" test conditions for a 10pC threshold. The data was then used for statistical analysis for reliability assessment. Where the various fabricated samples and test conditions were not perfectly identical, the difference was accounted for in the statistical spread of the data, which also incorporated the stochastic nature of PD.

The thirty prepared samples (which included ten samples of 1 mm trace gap, 10 samples of 2 mm trace gap, and ten samples of 3 mm trace gap) were stressed by high voltage progressively until they reached their PD inception voltage and the PDIV of each sample was recorded. Before testing, a test plan was prepared which included the description of the device under test, the design of the circuit for testing, equipment setup, program for the power supply to deliver the desired excitation profile, and the execution plan of the PD test. Then the test was performed according to the execution plan. These steps are detailed in Appendix J.

2.3.3.1 Device Under Test (DUT)

The samples built were the "device" to be tested using the PD test equipment. The DUT was first connected to the terminals, then gently placed in the clean ceramic bowl, avoiding too much tension on the terminals through the cables since they are delicate. Before testing, fluorinert dielectric fluid 3M FC-3283 [94] was poured into the bowl in enough quantity to fully submerge the sample including its terminals. The dielectric fluid is one among many measures to prevent arc formation across the terminals. It has a dielectric strength of >40 kV over a gap of 0.1" which is roughly equivalent to 20 kV/mm. Figure 29 (left) shows one of the samples connected to the HV cables and submerged in fluorinert. One of the traces on the top is shorted to the back side of the DBC as shown by the short wire that connects the two terminals. These

two terminals were then connected to earth ground while the other terminal is connected to the positive side of the capacitor. These connections are explained in the next section.



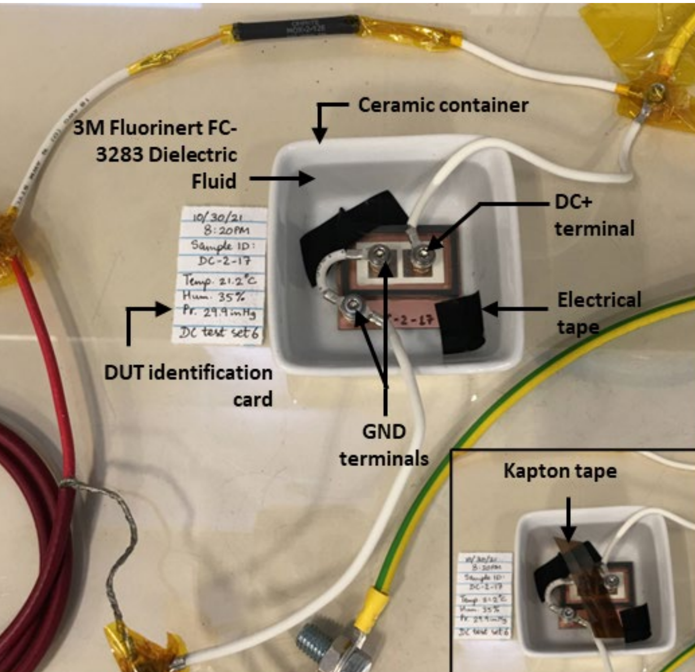


Figure 29. Device Under Test (DUT): example sample in dielectric fluid and connected to the HV and GND terminals (left), and example sample taped to container (right).

Fluorinert evaporates quickly, so an extra amount was used to ensure the sample would remain submerged even after some of the fluorinert evaporated. Practically, when pre-tests were performed on dummy samples, it was found that the samples would float. Due to tension on the wires and buoyancy in the fluid, the sample was taped down using electrical tape. Figure 29 (right) shows another sample held down in a ceramic bowl by electrical tape so that it does not float in the high-density fluid.

A kapton tape was used between the two terminals for additional protection also shown in the figure. With insulation from the dielectric fluid and the kapton tape, the likelihood of arcing across the terminals or tracking along the insulation material is eliminated. This is to ensure that the design feature being tested is the only feature being stressed. For practical modules, typically

the outermost insulation material used for packaging is grooved to increase the creepage distance. Also, terminals are placed far apart to increase the clearance distance. For this work, however, the test coupons were made without the case so that the effect of the *trace gap* alone on PDIV could be quantified for the given material set and programmed as a layout constraint in the automation tool's design rules.

It is good to check the capacitance of the DUT to ensure it is much smaller than the coupling capacitor being used in the circuit. A 1 nF coupling capacitor is being used in this circuit, and the DUT capacitance was 23 pF between the traces on the top side and 30 pF between the top and bottom trace. This is sufficiently lower than that of the coupling capacitor so that no additional capacitors are needed. An RLC meter was used to measure the capacitance of the DUT.

2.3.3.2 PD test circuit design

The PD test circuit was designed for DC tests and it was based on the DC PD testing application note [95] published by Omicron, the manufacturer of the PD test equipment, correspondences with the Omicron equipment sales engineers, and inspiration from AC PD test related standards such as the IEC 60270 [14] and IEC 61287 [76].

A note on DC vs. AC testing: AC tests are applicable if the power supplied is AC. Since the labs at the time did not have an AC HV power supply that would go beyond 5 kV, but a DC HV power supply that would go beyond 5 kV, DC tests were performed instead of AC. This was beneficial since DC tests would give more conservative results for PDIV as PD in the context of DC applied voltage is more severe. This is because there is a natural relaxation of the insulation material being stressed at the zero crossing inherent in any AC excitation twice per cycle, which is missing for DC excitation. Instead, the magnitude of PD is greater in DC while the frequency

of discharges is less compared to that in AC, and they are obviously not periodic the way they are in AC. Also, for AC testing, there is a specific voltage profile to be used as specified in the IEC 61287, but there is no such standard voltage profile for DC testing [76]. Hence, a DC test voltage profile was designed based on inspiration from the AC test. The challenge with DC testing is the lack of periodicity and inherent repetition that an AC waveform allows. The voltage needs to dwell at a fixed DC voltage level for a sufficient time to allow the sample to be stressed long enough for a discharge to occur, but short enough to maintain a practical overall experimental time duration. With the right adjustments to the test circuit, and consistency across all tests, the DC circuit was implemented for testing all samples built for PDIV measurement.

The DC PD test circuit provided in the application note is shown in Figure 30. A high voltage resistor was added for voltage division and input voltage sensing, according to Omicron's suggestion. The block labelled "filter" in Figure 30 is an inductive filter to filter out PD from the source if the source has a lot of noise. Because the PD levels from the power supply used for the tests were less than the prescribed amount (detailed in Appendix J.3), a current limiting resistor was used instead. Figure 31 shows the final circuit designed for the DC PD tests with a 1 GΩ voltage dividing resistor and a 100 MΩ current limiting resistor.

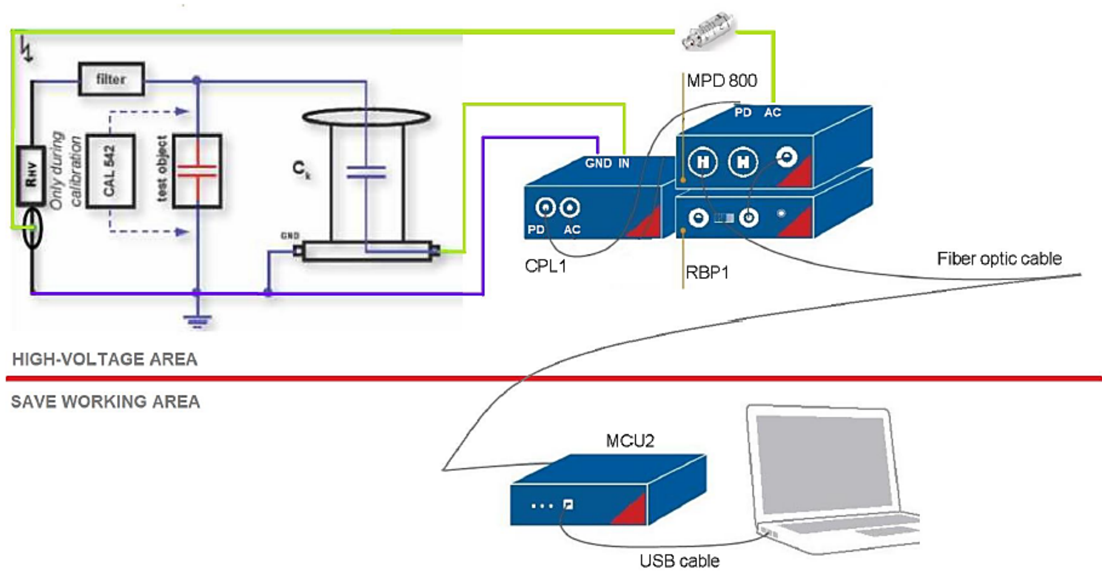


Figure 30. DC test circuit diagram prescribed by Omicron [95].

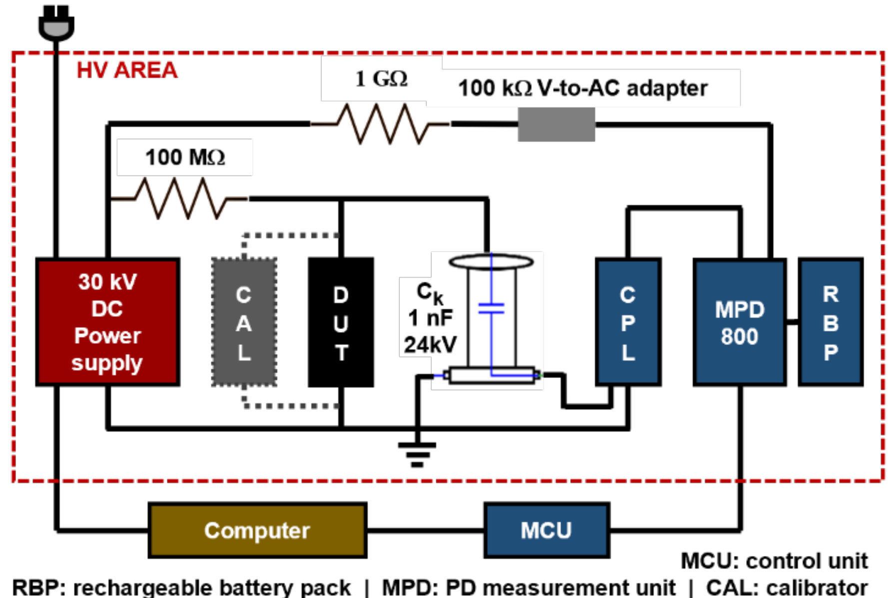


Figure 31. Circuit schematic for the partial discharge test setup using Omicron's MPD 800 PD measurement unit.

In Figure 31, the high voltage (HV) region is marked off. Increasing voltage is applied to the DUT and coupling capacitor with a pre-determined ramp rate. The coupling capacitor stores most of the charge and supplies the high energy needed in the DUT in the event of a partial

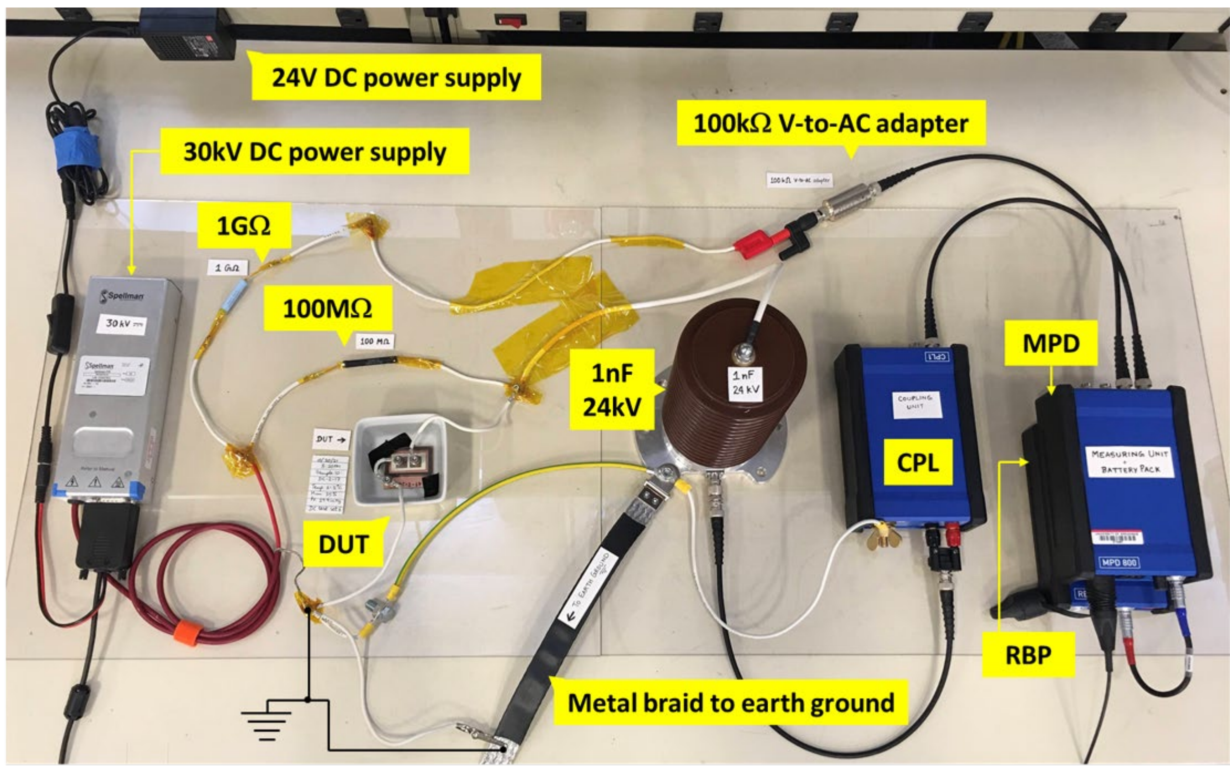
discharge. Omicron's equipment mathematically integrates the current supplied by the coupling capacitor to the DUT over time to calculate the apparent charge supplied during the partial discharge and stores this information along with the voltage at which the discharge occurred. The calibrator part of the circuit is dotted because it is only connected during calibration and then removed for the PD test.

The 100 MΩ current limiting resistor was chosen to be large enough to limit the breakdown current in the event of a breakdown, but small enough to maintain a reasonable rise time for the charging of the coupling capacitor so that it closely tracks the source voltage, but not so small that it contributes to the adverse effects of a high dv/dt or di/dt that may influence the PD measurement and keep the test from identifying the PDIV accurately. The effect of dv/dt and di/dt are important and should be considered in a separate study. This has been listed in the future works ideas section. A 100 MΩ current limiting resistor would limit the breakdown current of a 30 kV power supply to a maximum current of 0.3 mA and would limit the rise time to 100 ms. A 100 MΩ, 4W resistor was chosen for this purpose.

The 1 GΩ resistor was chosen to be able to read the source voltage at the MPD unit without connecting the MPD unit directly to the power supply. The voltage divider formed by the 1 GΩ resistor and the 100 kΩ resistor dropped the voltage across the 100 kΩ resistor to $1/10000^{th}$ the source voltage value which was read by the MPD unit. When voltage calibration is performed, this factor is accounted for. The HV resistor value was found based on knowing that the 100 kΩ V-to-AC adaptor can withstand a maximum of 140 V. This means the HV resistor value should be at least 14 MΩ. A 1 GΩ, 5 W resistor was chosen for this purpose and was used to calibrate the circuit for accurate voltage measurement.

2.3.3.3 PD test setup

The HV area of the circuit schematic from Figure 31 is physically laid out as shown in Figure 32, and its connection to the rest of the circuit (the low voltage side) is shown in Figure 34. The metal braid must be connected to a solidly grounded earth ground plate as shown in Figure 33.



DUT: device under test | CPL: coupling unit | MPD: PD measuring unit | RBP: rechargeable battery pack

Figure 32. High voltage side of the PD test bench.

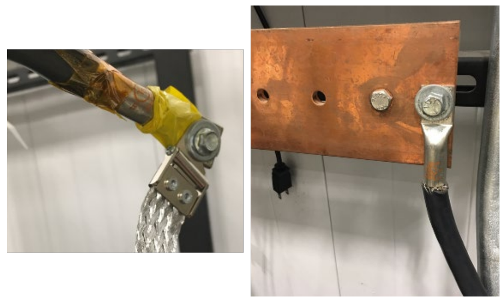


Figure 33. Metal braid connection to earth ground plate.

Omicron's MPD 800 PD tester was used to measure PD in the DUT and determine the PDIV. This equipment is specially designed for PD tests as it is sensitive enough to detect discharges much smaller than 1 pC and fast enough to detect the PD inception voltage. For safety, the HV section of the test bench was kept isolated from the control bench. In Figure 34, this section is marked off with dashed lines. The MPD 800 is connected to a rechargeable battery pack marked RBP in the figure. PD signals were transmitted from the MPD 800 to the control unit (MCU) through fiber optic cables, and the real-time discharges were shown graphically on the monitor and recorded as text files. The MCU is placed on the low voltage desk (the control table) shown in Figure 34.

The HV capacitor used for the test was MCC-124 from Omicron, which is a 1 nF, 24 kV capacitor [96]. This was used as a coupling capacitor. It is designed for PD testing as it is PD-free itself. It is charged by the power supply and when a PD occurs in the DUT, the high energy required for the discharge is drawn from the capacitor which can supply the required charge immediately. Omicron's coupling unit (CPL) is connected to this capacitor and measures the current in the circuit and the duration of the discharge pulse. The MPD 800 then calculates the apparent charge of the PD event by mathematically integrating the current supplied by the coupling capacitor to the DUT over time to determine the magnitude of the PD. The equipment automatically stores the charge information alongside the voltage at which the PD occurred. PDIV in this case is the voltage at which a discharge of 10 pC happens for the first time.

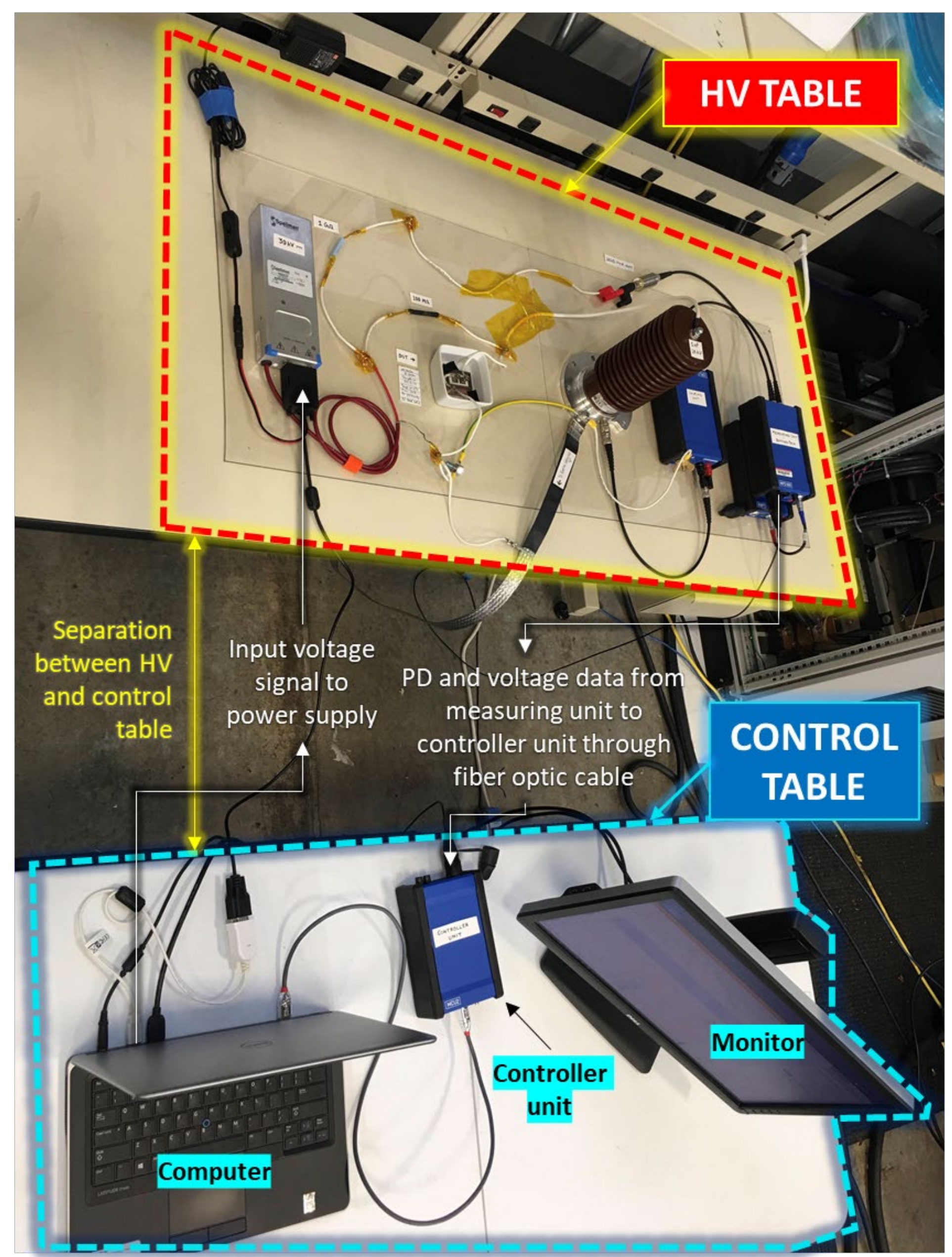


Figure 34. PD test setup with separate benches for the HV and LV areas.

10 pC is the recommended value for component level structures according to IEC 61287 [76]. The equipment was calibrated to measure PD accurately using Omicron MPD 800’s calibrator (CAL). The calibrator injects a known amount of charge (10 pC, for example), and the measurement unit measures it accurately by applying a correction factor as needed. The

maximum noise level for this test structure was less than 4 pC. IEC 60270 [14] recommends the noise level be no greater than half of the PD magnitude to ensure that the PD signal can be clearly distinguished from the noise. So, the noise level for a 10 pC measurement must be below 5 pC. This was ensured during each test.

A 30 kV 0.33 mA DC power supply from Spellman [97] with less than 4 pC of noise was used to supply the high voltage needed to stress the samples up to their PD inception voltage. It was connected to a 24 V DC supply and programmed through LabView. A 15W D-plug connected it to the computer on the other table. The unit is contained in an earthed case with a screened HV output cable and the HV output cable was terminated safely by connecting it to the node that connects to the two resistors in parallel as shown in Figure 32. The ground wire was connected to a node that connects to the metal braid which is connected to earth ground. A physical switch was used as an additional measure of safety to turn ON/OFF the power supply. This switch connected the Spellman power supply to a 24 V DC supply which gets power from a wall socket. To disconnect the Spellman power supply, one can flip the physical switch off, remove the 24 V DC supply from the wall socket, or switch off power to the entire test bench by flipping the power switch on the table (since the “wall” socket supplies power to individual tables). For safety, all the above steps, except the last one, were used.

The LabView program used to communicate with and control the Spellman power supply was pre-programmed. The front panel interface of the program is shown in Figure 165. When run, the program communicates with the Spellman power supply and turns it on or off. Voltage was applied with a pre-determined ramp rate. Figure 35 shows the voltage profile that was used. This profile was programmed into the LabView interface for the power supply.

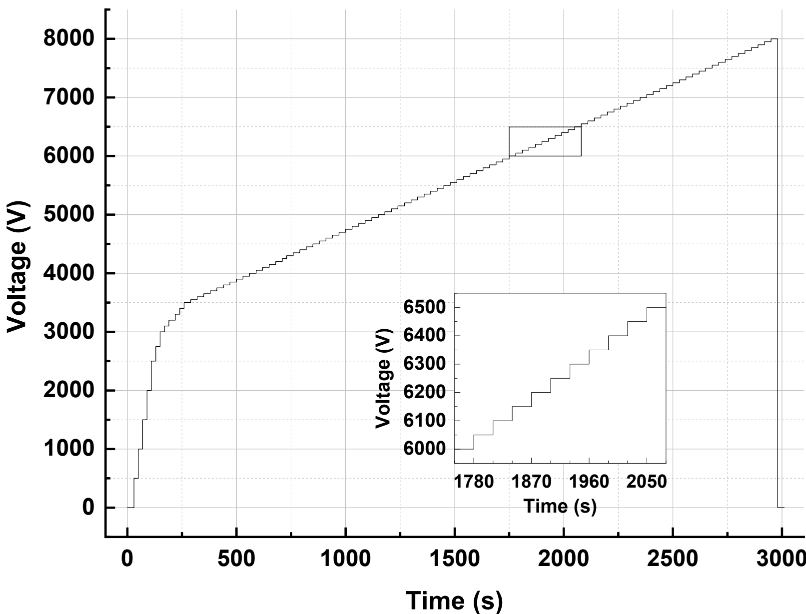


Figure 35. Voltage profile for energizing the DUT; inset: profile close-up.

The profile was designed so that the sample would be stressed at different voltage levels incrementally and dwell at each voltage level long enough to capture a PD signal if any, but to not dwell for so long that the total time of the test would be very long. Thirty seconds was chosen as the dwell time at each voltage level and a few seconds were lost in rise and fall time. Thirty seconds was chosen based on an example provided by the DC PD test application note from Omicron [95] where PD signals could be captured reasonably within a 30 second time frame. A few dummy samples were made and tested prior to testing the final set of 30 samples. This was done to test the equipment and also to get an idea about the typical PDIV that can be expected. Since all the PDIV values were above 4 kV, the profile was built to not dwell for long at the lower voltage levels and to increase rapidly between 0 V to 3 kV. Then by 3.5 kV, it would hold a steady increment rate and dwell time of 100 V/minute and 30 seconds, respectively. The profile was designed to drop to 0 V after reaching 8 kV. For some instances, if a sample was exhibiting a lot of PD beyond a certain voltage level, the voltage was brought to zero using the

LabView interface. More detail on how the LabView program communicated with the Spellman power supply is provided in Appendix J.1.

2.3.3.4 Test execution

Testing was conducted at the National Center for Reliable Electric Power Transmission (NCREPT), the University of Arkansas' high-power test facility. Note on safety: Since these were high voltage tests, several safety precautions were in place. These are listed in Appendix J.2. Once the PD bench test was set up, the following steps were followed to run the test. A brief version is listed here. The detailed steps are provided in Appendix J.3.

1. Connect DUT to HV terminals. Connect the MPD 800 to the battery pack.
2. Measure the general background noise. Figure 36 shows the layout of the MPD 800 PD test software's screen where the noise and PD signal are measured.

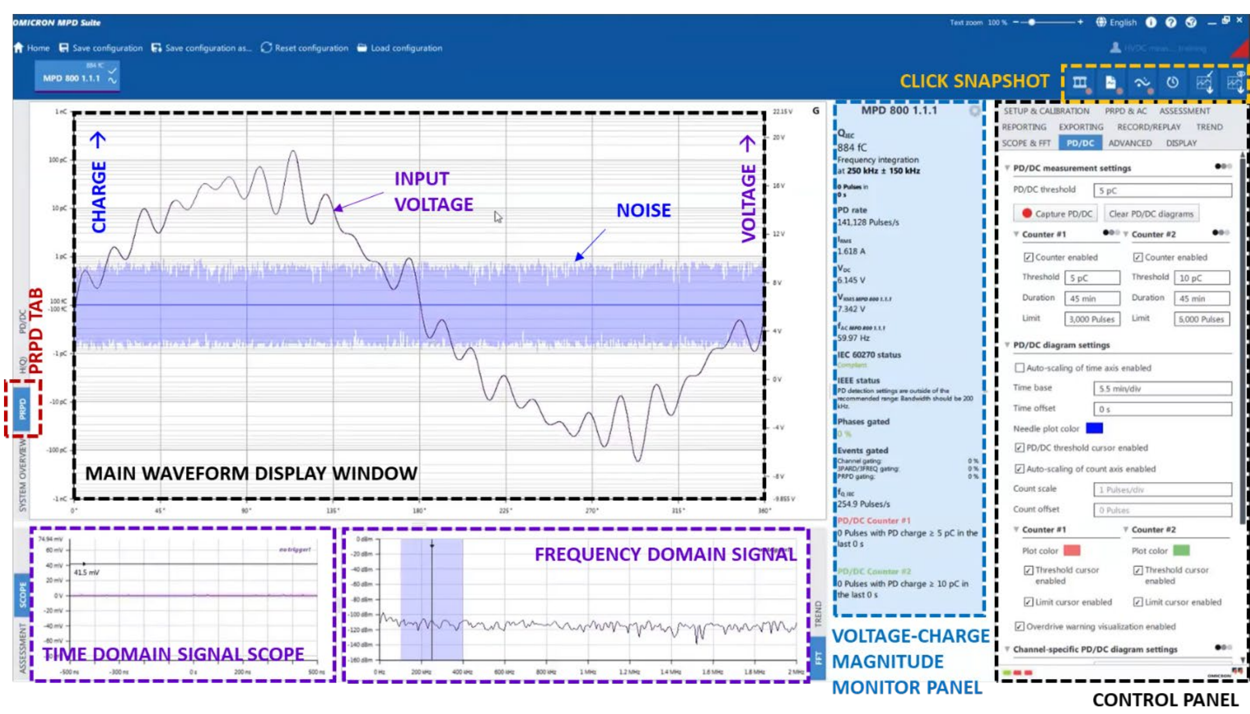


Figure 36. Main screen for PD measurement on the Omicron MPD 800 software.

3. Prep the LabView program with the correct voltage profile.

4. Measure the noise from the power supply.
5. Calibrate voltage (do this only when a new test setup is used).
6. Calibrate charge (do this each time the test setup or DUT capacitance changes). Figure 37 shows the charge calibration window where a 10 pC charge calibration is being performed. The noise floor and 10 pC charge are easily distinguishable.
7. Run voltage program and measure PDIV.
    a. Set the PD/DC threshold to 10 pC.
    b. Prep the software for data collection.
    c. Apply voltage: On LabView, turn off the Manual mode and let the program run.
    d. Observe data: On the MPD software, watch the PD/DC plot and the monitor panel to observe V_{DC} when charge level exceeds 10 pC. The total test time for each sample was almost an hour.
    e. Once there are numerous PD signatures beyond the threshold level of 10 pC, one may stop the test using the LabView program.
8. Save data.
9. Wait and safely discharge the capacitor and switch off the power supply. Carefully remove the DUT.

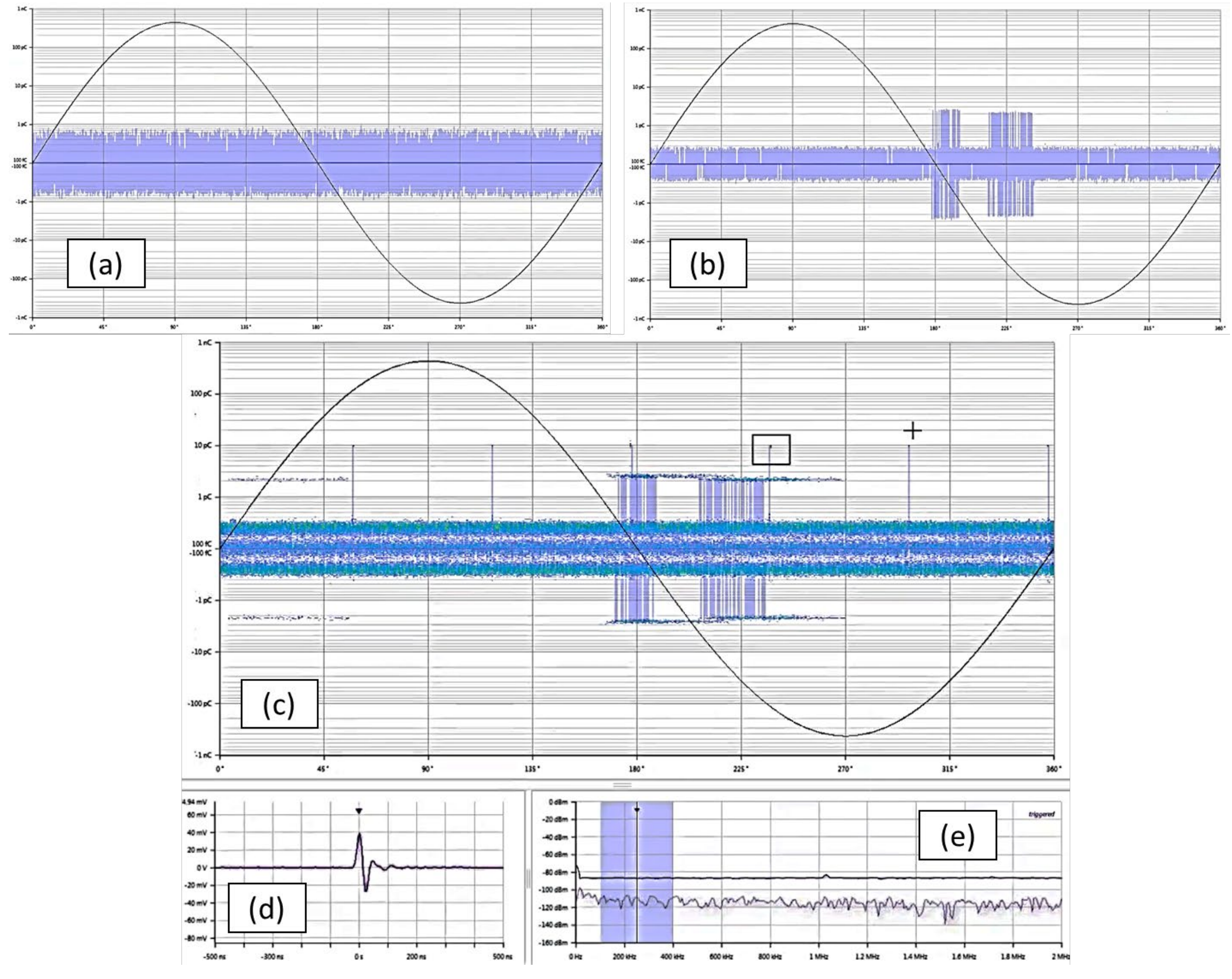


Figure 37. Signal and noise during the calibration process: (a) background noise without power supply, (b) noise including power supply, (c) 10 pC signal from calibrator unit against the noise floor.

2.3.4 Test results

Since PD is stochastic in nature, a statistical method needs to be used to determine PDIV over a given set of identical samples. IEC 62539 [92] recommends using the Weibull method for statistical analysis. A sample size of 10 is considered sufficient [92]. This work and others [90], [44] have used this standard successfully to make reliability predictions.

In the physical test, PD signals were captured over time as voltage was increased. An example graph of the raw data for one of the 1 mm trace gap test coupons is shown in Figure 38

where the purple graph with its axis on the left reads the voltage level at a certain time, and the blue needle points with their axis on the right read the charge level. Both the voltage and charge are shown on the same time scale. The raw data for each data set included two excel sheets: one with voltage vs. time information, and one with charge vs. time for all charge levels greater than 10 pC (the threshold set). For this test, the PDIV was 6.83 kV, where the needle point graph shows the first needle point to cross the 10 pC threshold.

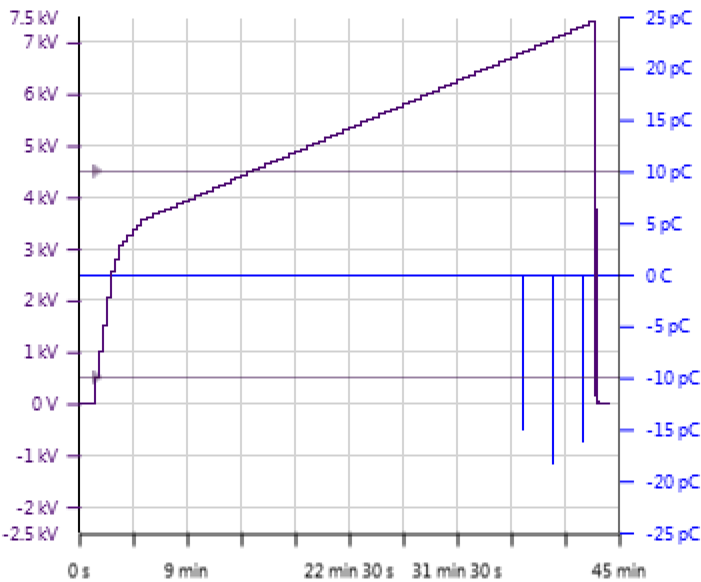


Figure 38. PD raw data for one of the 1 mm test structures showing PDIV of 6.83 kV.

From the data generated, the voltage at which the charge increases past the threshold of 10 pC for the first time is recorded as the PDIV. Table 4 lists the PDIV of all the thirty samples tested.

Table 4. PDIV raw data collected from PD tests for all thirty samples.

1 mm samples		2 mm samples		3 mm samples	
Sample	PDIV value (kV)	Sample	PDIV value (kV)	Sample	PDIV value (kV)
DC-1-01	3.156	DC-2-01	5.957	DC-3-01	6.723
DC-1-02	6.978	DC-2-02	4.85	DC-3-02	5.091
DC-1-03	5.245	DC-2-03	5.754	DC-3-03	6.672
DC-1-04	4.378	DC-2-04	7.131	DC-3-04	4.4
DC-1-05	6.875	DC-2-05	4.123	DC-3-05	6.978
DC-1-06	6.824	DC-2-06	6.927	DC-3-06	5.296
DC-1-07	6.825	DC-2-07	5.703	DC-3-07	5.448
DC-1-08	4.48	DC-2-08	7.589	DC-3-08	7.233
DC-1-09	4.737	DC-2-09	6.45	DC-3-09	5.5
DC-1-10	5.805	DC-2-10	6.366	DC-3-10	7.335

This data is analyzed in the next section.

2.3.5 Statistical analysis

A Weibull distribution is much like a Normal distribution where the data is centered around a mean value, with most of the values being close to the mean value and some values further away from the mean on either side. The difference is: in a Normal plot, the distribution is balanced around the mean, but in a Weibull distribution, one side is skewed. This is because the Weibull distribution is used for reliability data where there may be more likelihood of failure on one end of the curve than on the other, as is seen in lifetime predictions. Outliers end up close to the 1st—10th or 90th—99th percentiles of the curve, just like in a Normal distribution. But most of the data is centered around not the 50th percentile but the 63rd percentile, due to the skewness of the curve. One may refer the NIST handbook [98] or other resources for more information about

the various statistical distributions and their differences, and how to calculate percent failure manually. The Weibull distribution is widely used in industry and academia to plot and describe various reliability data, include PD data, and is recommended for use by the IEC standard on statistical analysis of electrical breakdown data [92].

OriginLab, a data analysis and statistical analysis software was used to process the data into Weibull plots. This can be done manually, but in this case was automated by the software: The PDIV values were ranked, and their corresponding percent failure value determined based on their position in the ranked list and the sample size, as described in the NIST handbook [98]. OriginLab lists out the data: The PDIV values for the 1, 2, and 3 mm samples and their corresponding percentiles (or percent failure) is given in Table 5, Table 8, Table 11, respectively. The software then plots these results on Weibull probability plots, as shown in Figure 39, Figure 40, and Figure 41. Each dot represents the PDIV value of a single sample.

Origin determines a best fit reference line (the red straight line in the Weibull plots) through these points, and the PDIV value for any percent failure can be determined. The data points that form the reference line are given in Table 6, Table 9, and Table 12 for the 1 mm, 2 mm, and 3 mm data sets, respectively.

The PDIV value for the 63% failure point on this line represents the characteristic value or the scale value of the Weibull plot, which is mentioned on the Weibull plots. In some ways this is analogous to the mean value of a normal distribution, but because it is not at the 50th percentile, it is not called the "mean." In lifetime prediction contexts, this value is typically called the "characteristic life." The characteristic value is discussed more later in this section.

The curved lines in the Weibull plots are the 95% confidence bound lines of the data. So, for the 2 mm trace-gap Weibull probability plot, there is 95% confidence that the PDIV

characteristic value is between 6.1 kV and 7.1 kV. The estimated PDIV values at the lower and upper confidence limits for the 1, 2, and 3 mm data sets are listed in Table 7, Table 10, and Table 13, respectively. For higher confidence levels, the voltage interval becomes larger. 95% confidence is typical for lifetime predictions for reliability analysis.

Table 5. Weibull percent failure of the PDIV data for the 1 mm sample set.

PDIV (kV)	Percent Failure
3.156	6.09756
4.378	15.85366
4.48	25.60976
4.737	35.36585
5.245	45.12195
5.805	54.87805
6.824	64.63415
6.825	74.39024
6.875	84.14634
6.978	93.90244

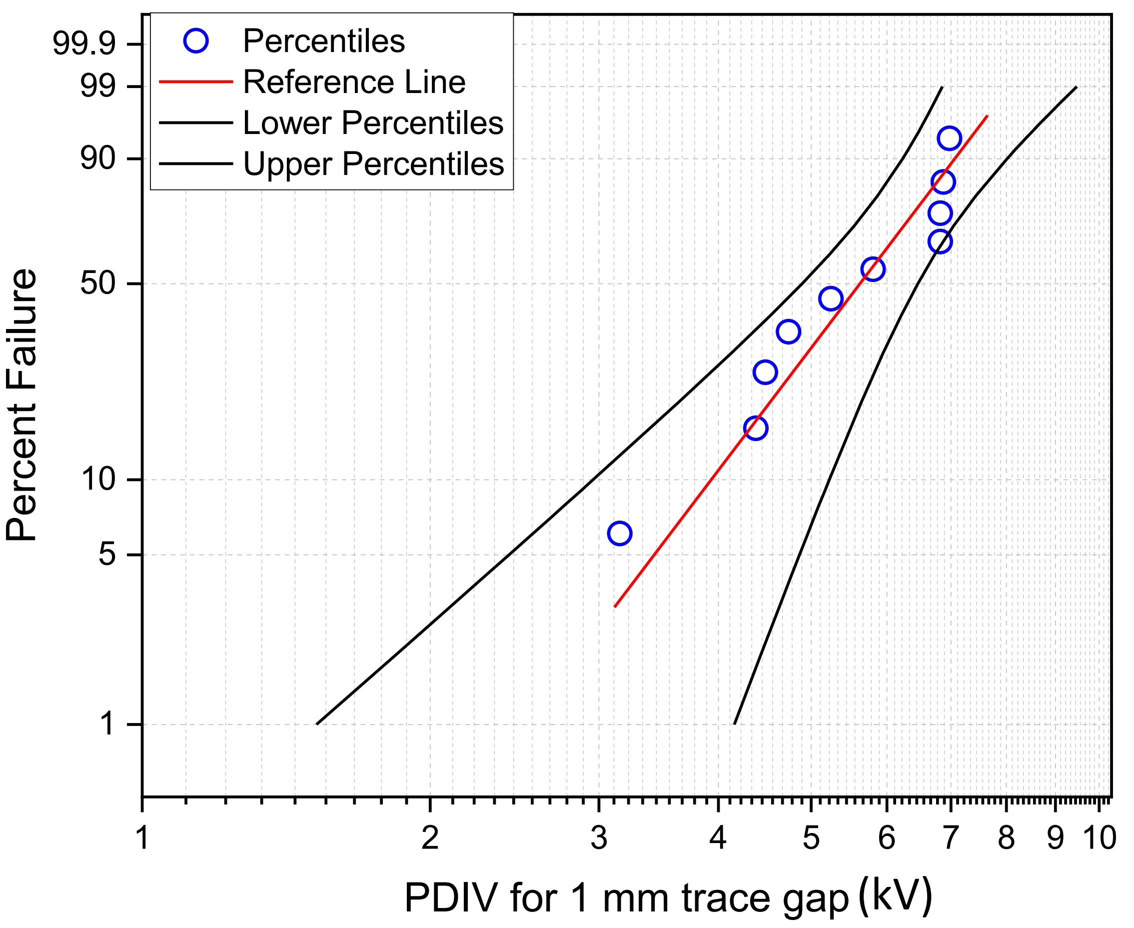


Figure 39. Weibull probability plot of PDIV (kV) for 1 mm trace gap.

Table 6. Reference line end points for the 1 mm data set Weibull plot.

PDIV (kV)	Percent Failure
3.11411	3.04878
7.6465	96.95122

Table 7. 95% confidence interval values in terms of PDIV for the 1 mm sample data set at various Weibull percentiles

Weibull percentiles	95% confidence band	
	Lower percentile PDIV (kV)	Upper percentile PDIV (kV)
1	1.52115	4.15618
2	1.85586	4.44241
3	2.08538	4.62144
4	2.26574	4.75454
5	2.41677	4.86172
6	2.54802	4.95217
7	2.66491	5.03088
8	2.77085	5.10089
9	2.86811	5.16418
10	2.95831	5.22215
20	3.64007	5.64553
30	4.12977	5.94754
40	4.53442	6.20952
50	4.89241	6.46336
60	5.22352	6.7314
70	5.54196	7.03873
80	5.86467	7.42755
90	6.23145	8.01017
91	6.27477	8.09136
92	6.32044	8.18009
93	6.36907	8.27822

Table 7 (Cont.)

Weibull percentiles	Lower percentile PDIV (kV)	Upper percentile PDIV (kV)
94	6.42154	8.38839
95	6.47917	8.51467
96	6.54409	8.66366
97	6.62016	8.84746
98	6.71558	9.09227
99	6.85467	9.47777

Table 8. Weibull percent failure of the PDIV data for the 2 mm sample set.

PDIV (kV)	Percent Failure
4.123	6.09756
4.85	15.85366
5.703	25.60976
5.754	35.36585
5.957	45.12195
6.366	54.87805
6.45	64.63415
6.927	74.39024
7.131	84.14634
7.589	93.90244

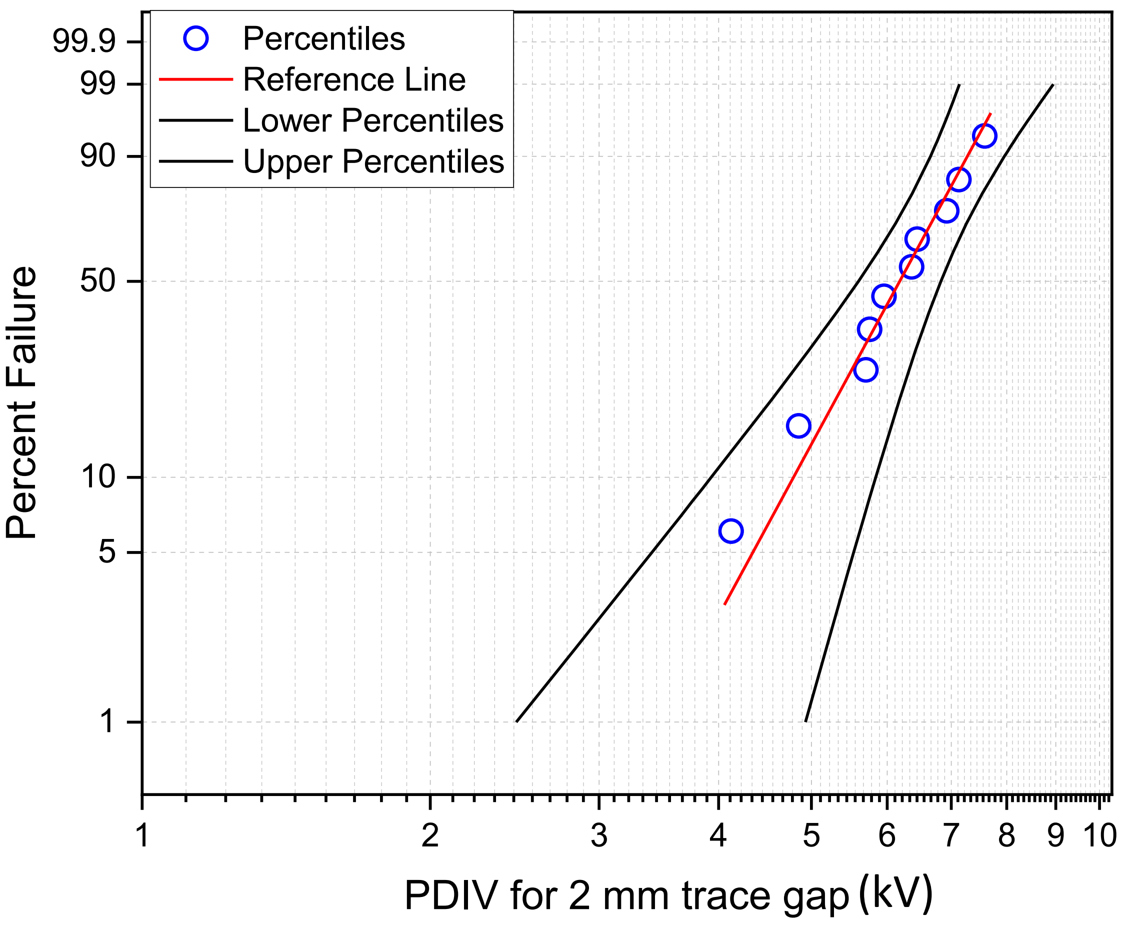


Figure 40. Weibull probability plot of PDIV (kV) for 2 mm trace gap.

Table 9. Reference line end points for the 2 mm data set Weibull plot.

PDIV (kV)	Percent Failure
4.05539	3.04878
7.69891	96.95122

Table 10. 95% confidence interval values in terms of PDIV for the 2 mm sample data set at various Weibull percentiles

Weibull percentiles	95% confidence band	
	Lower percentile PDIV (kV)	Upper percentile PDIV (kV)
1	2.45871	4.92913
2	2.82862	5.17821
3	3.07084	5.33185
4	3.25567	5.44505
5	3.4071	5.5356
6	3.53644	5.61159
7	3.64998	5.67741
8	3.7516	5.73573
9	3.84389	5.78826
10	3.92865	5.83621
20	4.54652	6.18195
30	4.96923	6.42366
40	5.30764	6.62978
50	5.60009	6.82608
60	5.86584	7.0295
70	6.11813	7.25792
80	6.37157	7.5403
90	6.65792	7.95244
91	6.69164	8.009
92	6.72717	8.07061
93	6.76497	8.13848

Table 10 (Cont.)

Weibull percentiles	95% confidence band	
	Lower percentile PDIV (kV)	Upper percentile PDIV (kV)
94	6.80572	8.21439
95	6.85043	8.30101
96	6.90075	8.4027
97	6.95961	8.52742
98	7.0333	8.69235
99	7.1404	8.94945

Table 11. Weibull percent failure of the PDIV data for the 3 mm sample set.

PDIV (kV)	Percent Failure
4.4	6.09756
5.091	15.85366
5.296	25.60976
5.448	35.36585
5.5	45.12195
6.672	54.87805
6.723	64.63415
6.978	74.39024
7.233	84.14634
7.335	93.90244

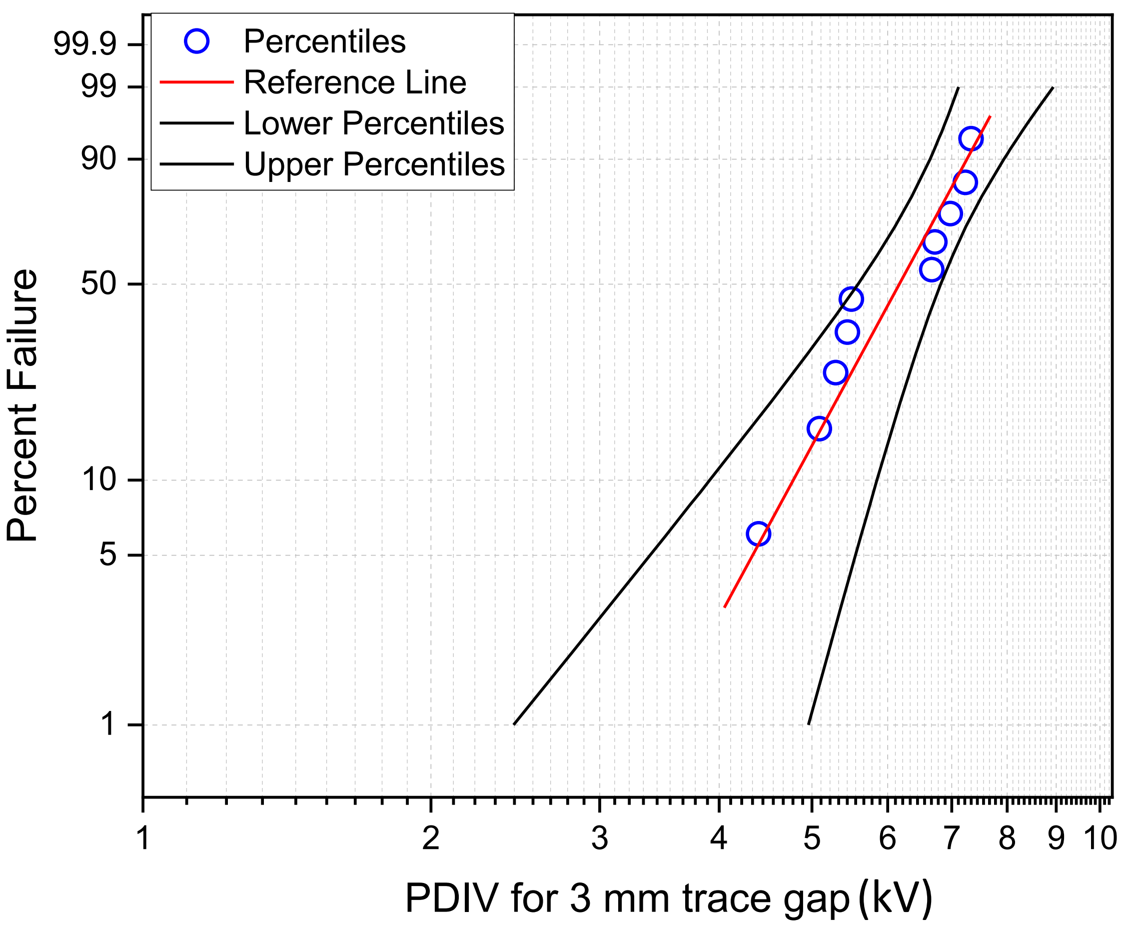


Figure 41. Weibull probability plot of PDIV (kV) for 3 mm trace gap.

Table 12. Reference line end points for the 3 mm data set Weibull plot.

PDIV (kV)	Percent Failure
4.05027	3.04878
7.68131	96.95122

Table 13. 95% confidence interval values in terms of PDIV for the 3 mm sample data set at various Weibull percentiles

Weibull percentiles	95% confidence band	
	Lower percentile PDIV (kV)	Upper percentile PDIV (kV)
1	2.43927	4.95831
2	2.80873	5.20268
3	3.05085	5.35329
4	3.2357	5.46419
5	3.3872	5.55287
6	3.51664	5.62726
7	3.63029	5.69169
8	3.73205	5.74875
9	3.82448	5.80015
10	3.90939	5.84706
20	4.5288	6.18517
30	4.95305	6.42158
40	5.29289	6.62342
50	5.58662	6.81608
60	5.85334	7.01642
70	6.10603	7.24244
80	6.35889	7.52336
90	6.6428	7.93557
91	6.6761	7.99228
92	6.71114	8.05407
93	6.74839	8.12218

Table 13 (Cont.)

Weibull percentiles	95% confidence band	
	Lower percentile PDIV (kV)	Upper percentile PDIV (kV)
94	6.78851	8.19837
95	6.83249	8.28535
96	6.88191	8.38751
97	6.93967	8.51285
98	7.01188	8.67866
99	7.11665	8.93723

The characteristic PDIV values (or scale values) for the 1, 2, and 3 mm samples are listed in Table 14. For the 1 mm sample set, the characteristic value is 6.03 kV. This means that 63% of the samples are likely to reach their PDIV by 6.03 kV for a 10 pC PD threshold level. The characteristic values of the 2 mm and 3 mm trace gap Weibull plots are 6.50 and 6.48 kV, respectively. This means that the general trend of PDIV over trace-gap is the same as shown in Figure 26, where PDIV first increases with trace gap and stays steady beyond a particular trace gap. In this case, PDIV reaches a steady-state by a 2 mm trace-gap. The chosen data nodes (1 mm, 2 mm, 3 mm) sufficiently cover the gamut of manufacturing possibilities, because 1: More data nodes (such as 1.5 mm) will not eliminate the stochastic nature of PDIV; 2. The manufacturing error of 0.1 mm will become significant when testing more data points, example: the difference between 1.0 mm and 1.5 mm may be too close to differentiate because the manufactured gaps may be 1.1 mm and 1.4 mm; and 3. This is a reasonable expectation for the volume of fabrication and testing at a university research fabrication facility.

Table 14. Weibull scale and shape parameters for 1, 2, and 3 mm trace-gap samples

Trace-gap	Scale	Shape
1 mm	6.03 kV	5.26
2 mm	6.50 kV	7.37
3 mm	6.48 kV	7.38

The natural dispersion of data is due to the stochastic nature of PD and is accounted for by the Weibull method of determining a characteristic value or scale value and a spread quantity (called the shape parameter). The Weibull plots in Figure 39, Figure 40, and Figure 41 show some spread in the data for each trace gap set, quantified by the shape parameter. This parameter is analogous to the inverse of the standard deviation of a normal distribution. The higher the slope of the reference line, the larger the shape value and the narrower the data spread. The shape values of the 1 mm, 2 mm, and 3 mm trace gap samples are 5.26, 7.37, and 7.38 (Table 14). The data spread is narrower for both the 2 mm and 3 mm data sets, compared to the 1 mm sample set. A large spread is the expected nature of reliability data. It can be attributed primarily to the stochastic nature of PD, and secondarily to some differences in manufacturing since no two samples can be perfectly identical. Numerous other factors can cause differences. Analyzing each is outside the scope of this work, but may be pursued in the future, and some of these ideas are discussed in the Future Work section of Chapter 5. Despite these differences, there is a trend in the characteristic values over the three design variations for a large enough sample size.

2.4 Calibration and Validation of PDIV simulations with experiments

The predicted PDIV values from Table 2 that were represented in terms of ***k*** can now be compared to the experimental values to determine the ***k***-value. Table 15 and Table 16 show how the characteristic values from experiments are applied to obtain the best ***k***-value for the PDIV

model (***k***=0.65 for 1 mm, and ***k***=0.66 for 2 mm and 3 mm). ***k*** = 0.66 yielded the best fit for the PDIV model due to its lowest average error across all trace gaps and the least sum of squared residuals.

Table 15. Determining ***k***-values using experimental results

Trace-gap (mm)	PDIV (kV) from Table 2 (Model)	PDIV (kV) (Experiment)	k
1	9.27 * ***k***	6.03	0.65
2	9.81 * ***k***	6.50	0.66
3	9.83 * ***k***	6.48	0.66

Table 16. Determining the best ***k***-value for the model

Trace-gap (mm)	PDIV (kV) (Experiment)	PDIV (kV) (Model)		|%Error|	
		k=0.65	***k***=0.66	***k***=0.65	***k***=0.66
1	6.03	6.0214	6.1141	0.1420	1.3943
2	6.50	6.3726	6.4709	1.9604	0.4521
3	6.48	6.3868	6.4848	1.4418	0.0745
Average |% error|				1.1814	0.6403
Sum of squared residuals				0.0250	0.0080

Figure 42 shows the predicted and experimental PDIV vs. trace gap curves overlayed on each other. The error bars represent the 95% confidence level on the characteristic value. The experimental values follow the diminishing returns trend seen with the prediction model. The values show a close match with ***k***=0.66 for all the trace gaps.

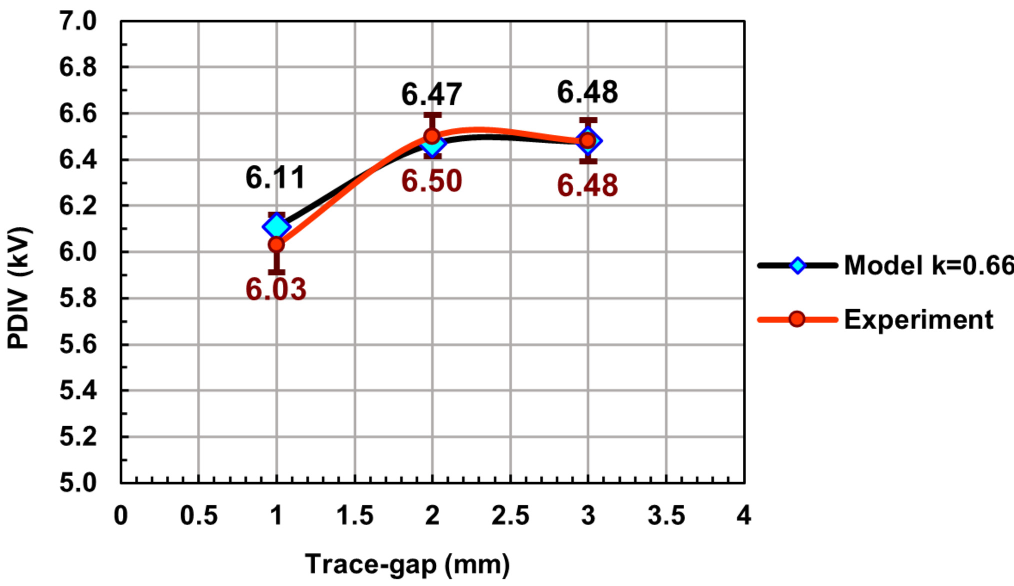


Figure 42. Experimental PDIV values overlayed on the prediction model with ***k***=0.66 showing an excellent match for all trace gaps tested.

Figure 43 shows the calibrated PDIV prediction model with ***k***=0.66 for intermediate trace gap values. The point of diminishing returns is at 2 mm with a PDIV limit of 6.5 kV. This model informs us that for a 12/25/12 mil alumina DBC with Dow Corning 3-6635 gel encapsulant, the maximum operating voltage should be limited to 6.5 kV to prevent PD above 10 pC. Increasing the trace gap beyond 2 mm offers no additional benefit in terms of PD mitigation or increased operating voltage. It also means that below 2 mm, the max operating voltage should be reduced significantly. Considering these factors, 2 mm is the optimum trace gap to be maintained for maximum voltage benefit.

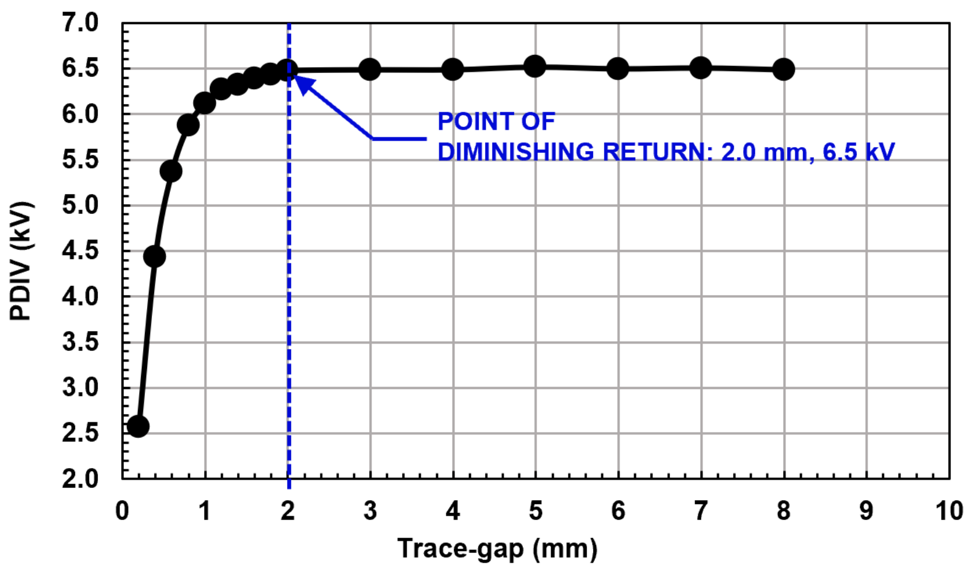


Figure 43. PDIV vs. trace gap prediction model expanded to include more trace gaps showing the diminishing returns trend and diminishing returns point at 2.0 mm and 6.5 kV.

This model, with its unique ***k***-value, is applicable for the chosen material set and manufacturing process. The ***k***-value *may* be different for a different material set and would likely be different for a different manufacturing process and must be determined experimentally. The *methodology* presented here can be used to determine a model for predicting PDIV vs. trace gap for any technology and manufacturing process. If the manufacturing process does not change, and the *type* of materials used in the layer stack remain the same, the same ***k***-value may be used. For example, if substrate samples of a different thickness or material (aluminum nitride instead of alumina) were made, but they were processed the same way as mentioned in the Fabrication section, the same ***k***-value could be used. However, if an LTCC substrate which has a completely different fabrication method, is used, then a different ***k***-value ought to be obtained through the calibration of simulations and experiments. The next chapter explores part of the material domain that can be covered by the same k-value obtained in this chapter and presents PDIV for those materials.

PDIV increases with increasing trace gap because surface charge density and E-field reduce with increasing trace gap. Beyond a particular trace gap, other factors may dominate, and the charge density and E-field concentrate in those parts of the test structure. Sometimes, this can be the ceramic material where the least resistance path for PD changes from the lateral trace gap to the vertical gap through the ceramic. This is discussed in the next chapter. Regardless, the PDIV keeps reducing following an inverse square law relationship as in Coulomb's law (this was also evident in the experiments conducted by Wang, et al. [90]). Any further increase in the trace gap has no significant effect on the PDIV. That is why it is being called the diminishing returns point. Figure 43 clarifies that there is a point of diminishing return beyond a particular trace gap for any given technology and this point can be quantified using the methodology demonstrated.

It is important to note that the encapsulant and the ceramic material's dielectric constant and dielectric strength are other factors that come into play in determining the preferred path for partial discharge to happen. Which factor dominates is discussed in the next chapter, along with details on how this is implemented in a layout generation tool and applied to the modification of existing design rules for the layouts.

The modeling approach presented in this chapter can be extended to incorporate PDIV in the ceramic material. This would enable characterizing PD in not just various encapsulant materials but also various ceramic materials and assess the combination effect of encapsulant-ceramic pair. The next chapter shows examples of various encapsulant-ceramic combinations.

This k-value obtained from the calibration process explained in this chapter can be applied to simulation results of various layer stack materials to develop a more comprehensive library of technology-PDIV data sets. The automation of this process, and how the results are stored and used in PowerSynth is described in the next chapter.

As the trace gap is extended beyond a certain point, PDIV remains steady at the same voltage. This is because of the inverse square of distance law of electrostatic force. And in some cases, beyond a certain gap, even before PDIV in the encapsulant reaches steady state, another part of the module geometry becomes the weakest link for PD inception. The only other insulating material in the bare module geometry is the ceramic isolation. PD finds its least resistant path either through the encapsulant or the ceramic. The two materials compete in this case to allow or prevent PD.

In this chapter, PD inception in the ceramic is quantified in a similar way as PD inception in the encapsulant was quantified in the previous chapter. Various substrate materials, such as Al_2O_3, AlN and Si_3N_4, and various encapsulants are characterized for PDIV prediction for various trace gaps through simulations that were calibrated in the previous chapter. This explores the material domain (but not exhaustively) that is typical for layer stacks. These aspects are covered in the first section of this chapter.

The results obtained from the calibrated simulations, which constitute the PDIV vs. trace-gap list for the encapsulant and the ceramic for each layer stack set, are stored in a library from which PowerSynth can look up key information like the maximum operating voltage for a given layer stack, its corresponding optimum trace gap, and the PDIV vs. trace gap trade-off curves for both the encapsulant and ceramic material, compared to each other. The points of these curves determine the recommended trace gap for any given voltage. The optimum trace gap for any layer stack and voltage level is recommended and saved as the design rule constraint for PD-mitigated high voltage operation. The user may choose to trade-off voltage for a more compact trace gap. The effects of a more conservative design rule set are discussed. The implementation

and automation of this process in PowerSynth, the EDA tool, is detailed in this chapter. These ideas are covered in the data library development and implementation sections.

Since high precision industrial processes typically have higher manufacturing consistency than a university lab process, samples taken off an industrial production line would have a smaller statistical spread in PDIV test results. Manufacturers can use the method presented in the previous chapter to determine a more appropriate ***k***-value for their high-yield processes if desired, and use the adjusted ***k***-value in PowerSynth to adjust the PDIV values calculated. This adjusts the design rules accordingly. While the default ***k***-value would remain 0.66 for all research lab prototyping processes as calibrated in the previous chapter, this chapter details also how the implementation of this methodology in PowerSynth accounts for changes in the ***k***-value. This is discussed in the section on scalability.

For layer stacks, materials, or manufacturing processes that are significantly different from those presented in the previous chapter, a user may employ the modeling approach in the previous chapter to define their own custom simulations, define their own experiments to calibrate and validate those simulations, and store the resulting data in a custom data library in PowerSynth. This chapter details how such custom PDIV libraries, that may be specific to an organization, were implemented in PowerSynth. Manufacturers and researchers can characterize their novel materials, stack-ups, and processes using the method described in the previous chapter, and store and use their results in the ever-growing manufacturing design kit library, as described in this chapter. These ideas are covered in the section on scalability.

Results discussed in this chapter include examples of PDIV in various encapsulant materials, in various ceramic materials, and their comparison that leads to key design decisions for trace gap and operating voltage. Layout solutions with and without PD design rules are

compared, and their effect on layout metrics is discussed. Finally, results also include the implementation of the ability to add custom k-values and custom PDIV libraries in PowerSynth. The implementation is tested for four unique layout designs, discussed in this chapter.

3.1 PDIV vs. gap in Ceramic and Encapsulant

3.1.1 Modeling PDIV in the ceramic

To measure charge density on the ceramic side of the triple point, an additional measurement point was placed on the ceramic-metal interface of the higher voltage metal trace as shown in Figure 44 and Figure 45. The location of MPside is ½ the thickness of the metal

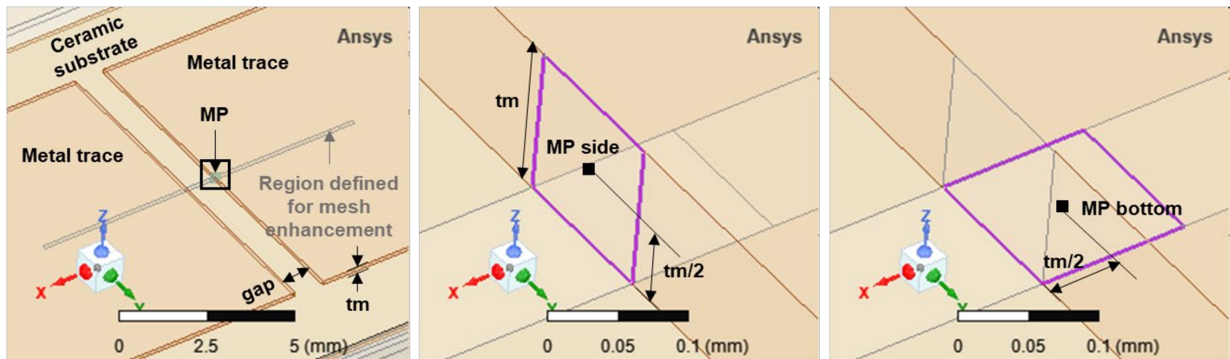


Figure 44. 3D view of trace-gap and general location of Measurement Point (MP) (left) and the close up of the MP location on the encapsulant-metal interface (middle) and on the ceramic-metal interface (right).

trace in the z-direction from the triple point. As the metal thickness (tm) changes, the location of MP is updated such that MPside is always in the middle of the vertical face of the metal trace. Similarly, the location of MPbottom updates so that it is always the same distance away from the TP as MPside is from the TP. The only difference is that MPbottom is on the x-y plane while MPside is on the y-z plane in the images shown in Figure 44.

Charge density is measured at both these points (Qs or Qside, and Qb or Qbottom) and stored in a data library. PDIV at the ceramic side is calculated the same way PDIV is calculated

on the encapsulant side, except the relative permittivity and dielectric strength used are that of the ceramic. PDIV vs gap for the ceramic is then plotted and compared to the PDIV vs gap for the encapsulant.

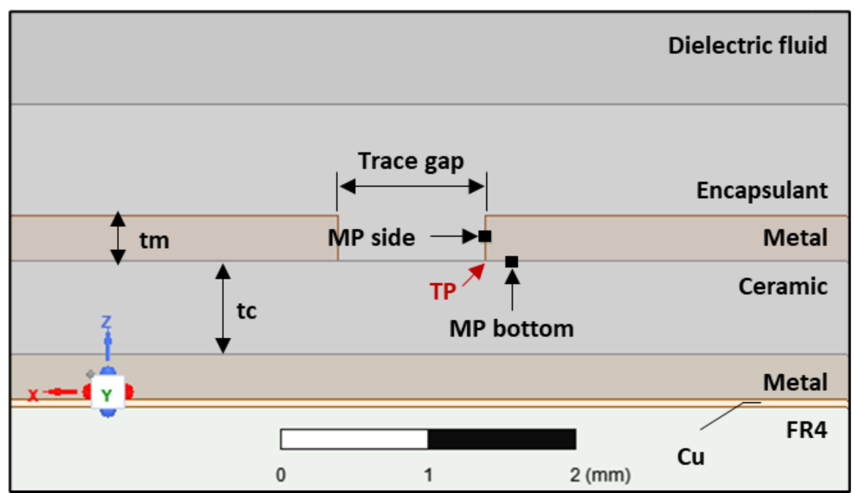


Figure 45. Location of MPside and MPbottom.

3.1.2 Comparing PDIV vs. gap in the ceramic and in the encapsulant

For the case tested in Chapter 2, which has a layer stack of 12/25/12 mil alumina DBC (0.3/0.64/0.3 mm) with a Dow Corning 3-6635 gel encapsulant, the PDIV vs gap curves for the encapsulant and the ceramic are shown in Figure 46. As can be observed from Figure 46, the encapsulant is the weaker material than the ceramic for this layer stack since it has the lower PDIV than the ceramic at all trace gaps. This means that it has PD inception at a lower voltage than the ceramic. It has a maximum PDIV of 6.5 kV, while the ceramic has a maximum PDIV of 6.7 kV. The lower of the two is taken as the PDIV of this layer stack system because it is compromised first. So, the maximum PDIV for this layer stack is 6.5 kV.

The diminishing returns point of this layer stack is ~6.5 kV and 2 mm since the PDIV reaches a steady value after 2 mm. Below 2 mm, there is significant change in PDIV as trace gap is increased up to about 1 mm. This is the fast-rising region of the curve. Between 1 and 2 mm,

there is little change in voltage as trace gap is increased, and beyond 2 mm, there is almost no change in voltage. In the rising regions of the curve, one can determine the voltage-trace gap trade-off. For a 6 kV module, the trace gap must be kept at least 0.9 mm. At 1 mm, the module can go up to only 6.1 kV for a PD-informed design.

Another critical piece of information is the voltage handling capability of the minimum gap. The minimum gap is determined by the manufacturing limit. For DBC wet etching, this is 0.5 mm. At 0.5 mm, the PDIV for the 12/25/12 mil alumina DBC with Dow 3-6635 gel is 4.8 kV, as observed in Figure 46. This is information that was not available before this work. Now, one can determine the voltage handling capability of any minimum gap layout based on this layer stack.

Being able to compare the encapsulant and the ceramic like this is useful in determining which material needs to be changed if the voltage performance needs to be improved. In this case

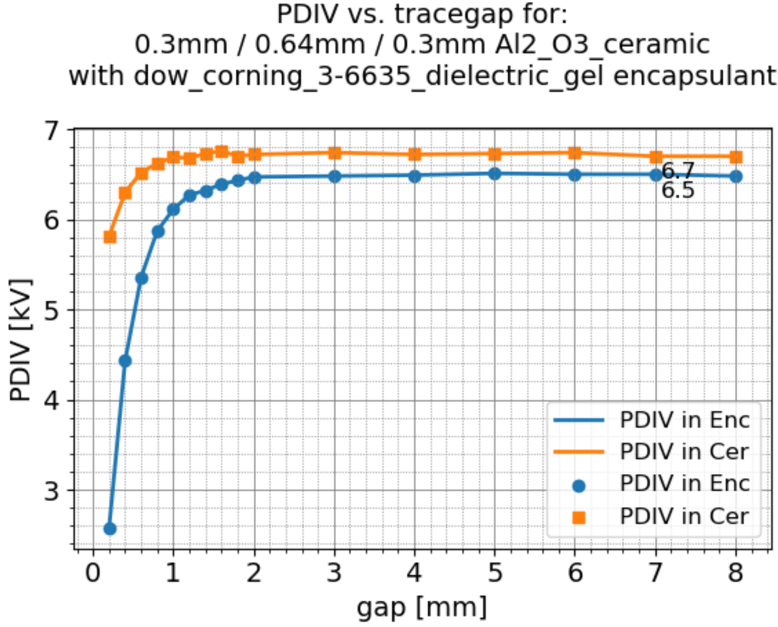


Figure 46. PDIV vs. gap for 12/25/12 alumnia with Dow 3-6635 gel.

we cannot operate at a voltage level above 6.5 kV without upgrading the encapsulant since the

encapsulant is the weaker of the two materials.

3.1.3 Effect of changing module materials

Although the list is not exhaustive, Table 17 provides various options for encapsulants. Every encapsulant material comes with a relative permittivity and a dielectric strength, as a pair (they cannot be separated). For the options given, relative permittivity (rp) does not change much (with some exceptions), but the dielectric strength does. E-field scales linearly with dielectric strength. Choosing the material with the highest dielectric strength, in this case it is the Wacker 612 dielectric gel, one must then compare the PDIV vs. gap of the existing ceramic to that of the new encapsulant. Wacker 612 has a relative permittivity of 2.7 and a dielectric strength of 23 kV/mm.

Table 17. Encapsulant material options with their relative permittivity (rp) and their dielectric strength (Eds).

Encapsulant material name	relative permittivity	dielectric strength [kV/mm]
Dow corning 3-6635	2.83	20
Dow Corning 3-6636	2.85	16
Sylgard 184	2.72	19
Sylgard 527	2.85	15
Simcosil 971 TC	6.1	10
Simcosil 987 GR	2.8	45
Dow Corning 3-4133	2.87	19
Dow Corning 3-4150	2.85	15
Dow Corning 3-4154	2.87	18
Dow Corning 3-4170	2.85	20
Dow Corning 3-4190	2.86	19
Dow Corning 3-4680	2.75	16

Table 17 (Cont.)

Encapsulant material name	relative permittivity	dielectric strength [kV/mm]
Dow Corning 3-4207	2.85	17
Dow Corning 3-4222	2.64	14
Dow Corning 3-4237	2.96	19
Dow Corning 3-4241	2.6	17
Wacker 612	2.7	23

With the update of the encapsulant, the PDIV comparison is shown in Figure 47.

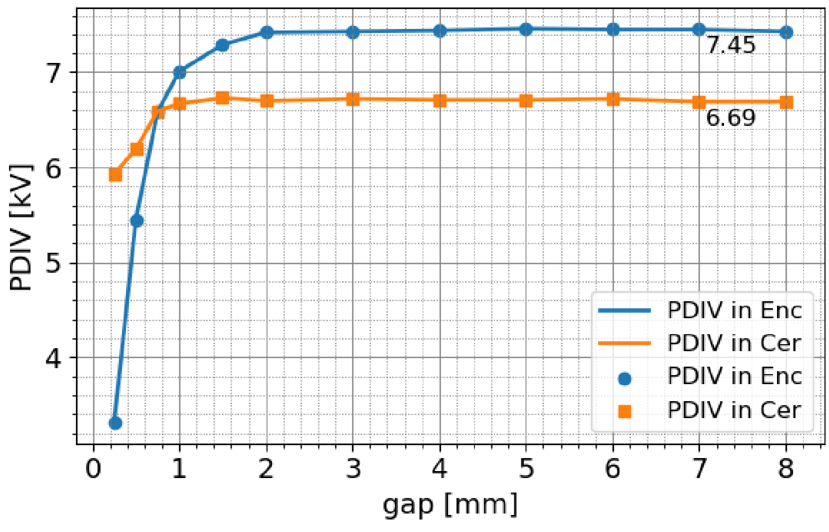


Figure 47. PDIV vs. gap for 12/25/12 alumina with Wacker 612 encapsulant.

Comparing Figure 46 and Figure 47, one can see that the Encapsulant PDIV curve has shifted to a steady value of 7.65 kV, crossing over the ceramic PDIV curve at ~ 0.7 mm and 6.6 kV. The overall PD-free voltage handling capability of the layer stack has now improved from 6.5 kV to about 6.7 kV. This is an example of how one may upgrade a layer stack based on

information provided by the PDIV vs. gap curves. In Figure 47, at trace gaps below 0.7 mm, the encapsulant is the material that would be compromised first and is therefore the determining material for establishing the layer stack's PDIV. Beyond 0.7 mm, it is the ceramic that is the weaker material that determines the PDIV of the layer stack. So, these curves are very useful in determining which material to upgrade based on which has the lower PDIV at a certain trace gap.

To operate at a higher voltage than 6.7 kV, one must upgrade the ceramic material either by increasing its thickness, or the material choice, which would impact the relative permittivity and dielectric strength. Various options to choose from are provided in Table 18.

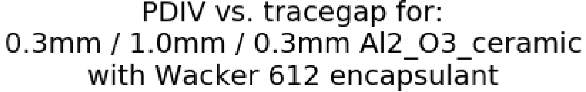
Table 18. Substrate options

		Copper thickness (tm)						
Ceramic	Ceramic thickness (tc)	5 mil =0.127 mm	8 mil =0.2 mm	9.8 mil =0.25 mm	12 mil =0.3 mm	15.7 mil =0.4 mm	19.7 mil =0.5mm	31.5 mil =0.8 mm
Al_2O_3 rp =9.8 Eds =20 kV/mm	10 mil = 0.25mm	X	X					
	12.6 mil = 0.32mm	X	X	X	X			
	15 mil = 0.38mm	X	X	X	X			
	19.7 mil = 0.5mm	X	X	X	X	X		
	25 mil = 0.64mm	X	X	X	X			
	40 mil = 1mm	X	X	X	X			
AlN rp =8.8 Eds =20 kV/mm	15 mil = 0.38mm	X	X					

Table 18 (Cont.)

		Copper thickness (tm)						
Ceramic	Ceramic thickness (tc)	5 mil =0.127 mm	8 mil =0.2 mm	9.8 mil =0.25 mm	12 mil =0.3 mm	15.7 mil =0.4 mm	19.7 mil =0.5mm	31.5 mil =0.8 mm
	25 mil = 0.64mm	X	X	X	X			
	40 mil = 1mm	X	X	X	X			
Si_3N_4 rp =7.8 Eds =15 kV/mm	10 mil = 0.25mm				X		X	X
	12.6 mil = 0.32mm				X		X	X

Since alumina substrate already has a high relative permittivity, in this example, the thickness of the ceramic is increased from 0.64 to 1 mm (~40 mil). The resulting PDIV vs. gap



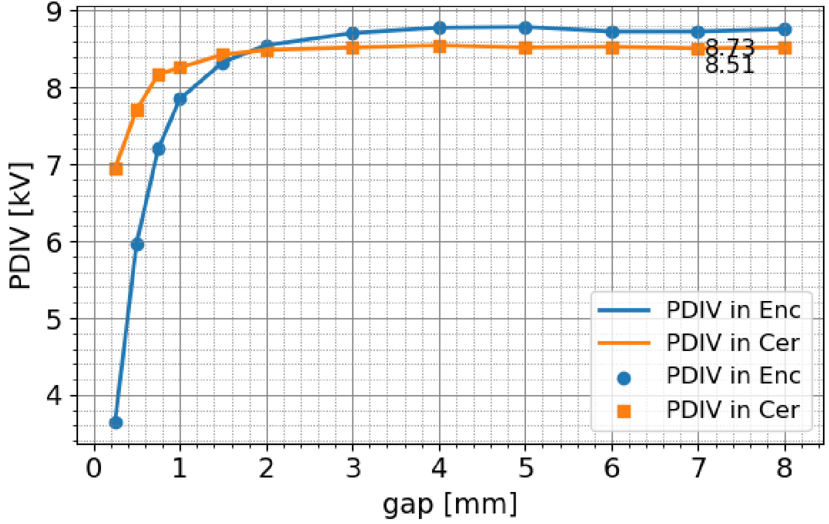


Figure 48. PDIV vs. gap for 12/40/12 alumina with Wacker 612 encapsulant.

curve is shown in Figure 48. Increasing the ceramic thickness increased the PDIV of the ceramic from 6.7 kV in Figure 47 to 8.51 kV in Figure 48. There is again a crossover of the curves at ~ 1.8 mm and 8.5 kV where at lower voltages, the encapsulant is the compromising material, and at higher voltages, it is the ceramic. One can also observe that in general, for any trace-gap, a higher PD-free voltage can be achieved, and for any voltage level, a smaller trace gap can be achieved. Information like this is very helpful to module designers when choosing materials and layout designs.

3.2 Data library development for software implementation

With the mindset of implementation in an EDA tool like PowerSynth, a large data library for numerous possible encapsulant-substrate combinations were simulated according to the calibrated simulations from chapter 2. Keeping all simulation settings the same, trace gap was varied between 0.25 to 1.5 in steps and the PDIV was recorded for more than 190 combinations of encapsulant-ceramic substrate properties. These included practical material sets chosen from Table 17 and Table 18, as well as hypothetical material properties that would aid in the interpolation of materials not included in Table 17 and Table 18 so that any material properties in between those explicitly simulated can be found with ease.

Each material set included four different parameters: the relative permittivity of the encapsulant (rpE), the relative permittivity of the ceramic (rpC), the thickness of the ceramic (tc), and the thickness of the metal (tm). Table 19 lists the values of these four parameters whose every combination was simulated and their charge density results recorded for trace gaps: 0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8 mm. These trace gaps were chosen as such to have enough data points in the rising regions of the PDIV vs. gap curves to be able to determine the diminishing returns point with some degree of accuracy without an overwhelmingly long

simulation time. For trace gaps beyond 2 mm, most PDIV curves reached steady state, and thus, only an increment of 1 mm was selected. The trace gap data set was extended to 8 mm to clearly depict the diminishing returns and steady state of PDIV beyond a certain trace gap. Table 20 shows an example of how these values were combined.

Table 19. Parameter values chosen for forming combinations for simulation

Parameter	Values chosen
rpE	1, 3, 5
rpC	6, 8, 10
tc	0.25, 0.5, 0.75, 1.0, 1.25, 1.5
tm	0.1, 0.2, 0.3, 0.4
gap	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8

Table 20. Combinations of values simulated for the four parameters and gap

rpE	rpC	tc (mm)	tm (mm)	gap (mm)
1	6	0.25	0.1	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
1	6	0.25	0.2	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
1	6	0.25	0.3	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
1	6	0.25	0.4	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
1	6	…	0.1	0.25, …, 8
1	6	…	…	0.25, …, 8
1	6	…	0.4	0.25, …, 8
1	6	1.5	0.1	0.25, …, 8
1	6	1.5	…	0.25, …, 8
1	6	1.5	0.4	0.25, …, 8
1	8	0.25	0.1	0.25, …, 8

Table 20 (Cont.)

rpE	rpC	tc (mm)	tm (mm)	gap (mm)
1	8	…	…	0.25, …, 8
1	8	1.5	0.4	0.25, …, 8
1	10	0.25	0.1	0.25, …, 8
1	10	…	…	0.25, …, 8
1	10	1.5	0.4	0.25, …, 8
3	6	0.25	0.1	0.25, …, 8
3	…	…	…	0.25, …, 8
3	10	1.5	0.4	0.25, …, 8
5	6	0.25	0.1	0.25, …, 8
5	…	…	…	0.25, …, 8
5	10	1.5	0.4	0.25, …, 8

The values combined in Table 20 may not be feasible in practice but are simulated to aid in the interpolation process for potential practical cases that may not be considered explicitly. These combinations also help test the effect of various changes in the values of the parameters on PDIV, to test extreme hypothetical cases, and to offer a large data set from which to form an interpolation function. Table 21 shows the practical cases that are explicitly simulated.

Table 21. Exact values simulated of the four parameters and gap

rpE	rpC	tc (mm)	tm (mm)	gap (mm)
2.7	7.8	0.32	0.3	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
2.7	7.8	0.32	0.8	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
2.83	8	0.635	0.3048	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8

Table 21 (Cont.)

rpE	rpC	tc (mm)	tm (mm)	gap (mm)
2.83	9.8	0.25	0.3048	0.2, 0.4, 0.6, 0.8, 1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 3, 4, 5, 6, 7, 8
2.83	9.8	0.381	0.203	0.2, 0.4, 0.6, 0.8, 1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 3, 4, 5, 6, 7, 8
2.83	9.8	0.5	0.3048	0.2, 0.4, 0.6, …, 2.0, 3, 4, …, 8
2.83	9.8	0.635	0.2	0.2, 0.4, 0.6, …, 2.0, 3, 4, …, 8
2.83	9.8	0.635	0.3048	0.2, …, 8
2.83	9.8	0.635	0.4	0.2, …, 8
2.83	9.8	0.75	0.3048	0.2, …, 8
2.83	9.8	1.016	0.127	0.2, …, 8
2.83	9.8	1.5	0.3048	0.2, …, 8
2.83	10	0.635	0.3048	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
2.83	11	0.635	0.3048	0.25, 0.5, 0.75, 1.0, 1.5, 2, 3, 4, 5, 6, 7, 8
2.96	9	0.381	0.127	0.25, …, 8.0
2.96	9.8	0.254	0.127	0.25, …, 8.0
2.96	9.8	0.381	0.3048	0.25, …, 8.0
1	9.8	0.635	0.3048	0.25, …, 8.0
3	9.8	0.635	0.3048	0.25, …, 8.0
5	9.8	0.635	0.3048	0.25, …, 8.0

Tm=0.1 was added later since occasionally a 0.127 mm tm would be used but this was not part of the original dataset. To help the interpolator find data to interpolate with, tm=0.1 was simulated for a combination of rpE=1 and 5, rpC=6 and 10, tc=0.25 and 1.5, and all gap values. This was done to optimize between design space exploration and simulation computation time. It

would be good to simulate tm=0.1 for all the other values of the other parameters to make the data library more robust with a more comprehensive data set. In fact, any additional data points added to the data library will make the interpolation function more robust because the interpolation will be as good as the data it is interpolating from. The current library is already extensive and spans a large design space. And it can be made stronger.

Figure 49 shows the spectrum of values simulated and juxtaposed to the range of practical values to show that the simulated range encompasses all practical values encountered. If a material property is requested that has not been explicitly simulated, the interpolation function

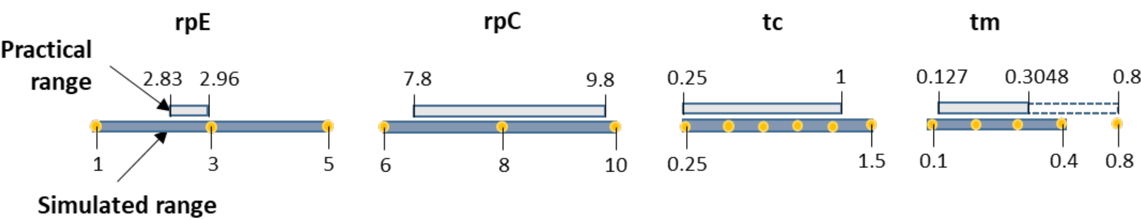


Figure 49. Practical and simulated range of parameter values.

should be able to interpolate for it based on the range of simulated results that are in the data library. How this data will be used is part of the discussion in the next section.

3.3 Implementation of adjusted design rules in PowerSynth EDA tool – methodology

Some of the layouts in PowerSynth are shown in Figure 50 to help visualize them. There has so far been no information as to what voltage level these layouts can operate at. The implementation methodology presented in this section will enable the user to determine the voltage level for each layout generated by the tool and determine the layout's design rules for a given voltage level and layer stack.

PowerSynth's layouts are based on a corner stitch data structure that represents the location of every trace in the layout in relation to its neighboring traces and the layout boundary.

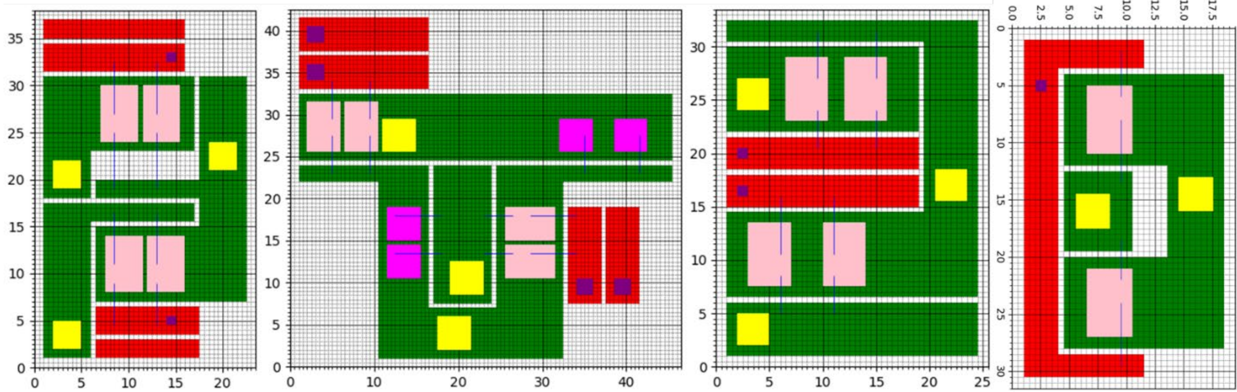


Figure 50. Example power module layouts in PowerSynth

Corresponding constraint graphs quantify the specific gap or distance required between neighboring traces and the layout boundary. This work has been described in a previous publication [99] and an example of a layout building block from it is provided in Figure 52. The constraint graphs are made of nodes and edges, where the nodes are the relative coordinates in a cartesian plane, and the edges are the magnitude of the size of the element that is occupying the space between two nodes. Some of these edges are labeled “S” and these are the gaps between traces that are of interest for this work. Each edge has a weight associated with it. It is this weight that must be edited to edit the gap between two elements. So, the objective of this work is to be able to update the weight of the edges marked “S” based on the voltage reliability for a material set.

3.3.1 Default design constraints – existing and unaltered

By default, the smallest weight that can be assigned for this edge gap is determined by the manufacturing limit of the trace gap. For a chemical wet etching process, this limit is set to 0.5 mm. The layouts shown in Figure 50 all have 0.5 mm gaps. A constraint file is exposed to the user where all minimum and default spacings may be entered [100]. A snapshot of this constraint file is shown in Figure 51 with the relevant trace gaps highlighted for the discussion in this section.

The highlighted values in the constraint file are what is used as the gap between layouts. These are called the “Design Constraints.” Here 0.5 mm is the default gap between two power traces and two signal traces and between power and signal traces. This constraint file is saved in the test case library and its file path is provided in the macro script of the test case that is run

layout.csv

Min Dimensions	EMPTY	power_trace	signal_trace	bonding wire pad	power_lead	signal_lead	MOS
Min Width	1	2	2	1	3	1	4
Min Height	1	2	2	1	3	1	6
Min Extension	1	2	2	1	3	1	6
Min Spacing	EMPTY	power_trace	signal_trace	bonding wire pad	power_lead	signal_lead	MOS
EMPTY	0.5	0.5	0.5	0.5	0.5	0.5	0.5
power_trace	0.5	0.5	0.5	0.5	0.5	0.5	0.5
signal_trace	0.5	0.5	0.5	0.5	0.5	0.5	0.5
bonding wire pad	0.5	0.5	0.5	2	0.5	0.5	0.5
power_lead	0.5	0.5	0.5	0.5	0.5	0.5	0.5
signal_lead	0.5	0.5	0.5	0.5	0.5	0.5	0.5
MOS	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Min Enclosure	EMPTY	power_trace	signal_trace	bonding wire pad	power_lead	signal_lead	MOS
EMPTY	1	1	1	1	1	1	1
power_trace	1	1	1	1	1	1	1
signal_trace	1	1	1	1	1	1	1
bonding wire pad	1	1	1	1	1	1	1
power_lead	1	1	1	1	1	1	1
signal_lead	1	1	1	1	1	1	1
MOS	1	1	1	1	1	1	1

Figure 51. Default constraint file with minimum trace gaps

when the PowerSynth program is executed. The constraint file can either be generated in PowerSynth or loaded by the user by saving it at the location specified. Which option is chosen is determined by another flag called “New.” A snapshot of the macro script for one of the test cases is shown in Figure 53. Line 8 gives the user the ability to enter the location where the constraint file is saved.

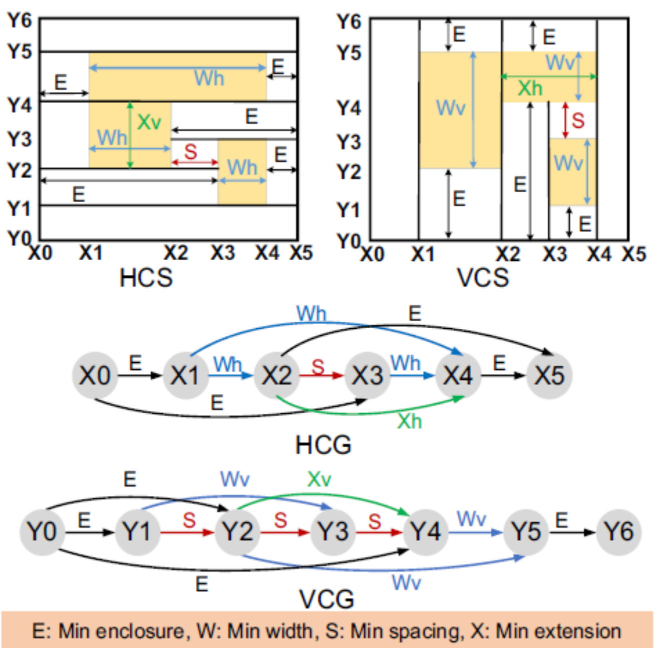


Figure 52. Horizontal and vertical corner stiched planes (above) and their corresponding constraint graphs (below) [100].

3.3.2 Design constraints for high voltage operation – arbitrary rules replaced

Line 21 in Figure 53 enables the user to edit a flag called "Reliability-awareness," which determines whether to use the default constraint file or a modified constraint file. When the reliability flag is set to "0," the default design constraints are used as shown in Figure 51. When the flag is set to "1" or "2," the structure of the constraint file is updated with additional rows that allow the user to specify the voltage present on each trace and a voltage difference vs. minimum spacing list from which the program determines what the gap should be instead of the default values, based on voltage differences calculated internally. An example of this edited constraint file corresponding to reliability-awareness flag = 2 is shown in Figure 54. In the existing architecture of the tool, the "Voltage Difference" column and the "Minimum Spacing" column are manually edited by the user.

```
1 # Input scipts:
2 Layout_script: ./balancing.txt
3 Bondwire_setup: ./balancing_bondwire.txt
4 Layer_stack: ./layer_stack_2.csv
5 Parasitic_model: ./mutual_impact.rsmdl
6 Fig_dir: ./Figs_New
7 Solution_dir: ./Solutions_New
8 Constraint_file: ./layout_1.csv
9 Trace_Ori: ./Trace_ori.txt
10
11 # Layout Generation Set up:
12 # Options -- 0: layout generation, 1:single layout evaluation, 2:layout optimization
13 # Layout Modes -- 0: minimum size, 1:variable size, 2:fixed size, 3:fixed size with fixed locations
14 # Reliability-awareness==0,1,2 #0: no reliability constraints, 1: worst case consideration, 2: average case
15 # if New ==1 constraint file is required to setup if ==0 constraint file will be reloaded
16 # if Plot_Solution==1, all solutions will be plot and saved in the Fig_dir.
17 # if Flexible_Wire==0: horizontal/vertical wire bond is considered, else: flexible connection is considered.
18 # if Default_PD_Datalib== 1: use the default PD library; 0: use the custom library but without filler material.
19 # PDIV_k: 0.66 is the default. The user can specify their own k-value here.
20 # PDIV_ss_tol: when the slope of the PDIV vs tracegap curve reaches below this value, the diminishing returns
   point is determined.
21 Reliability-awareness: 0
22 Default_PD_Datalib: 0
23 PDIV_k: 0.66
24 PDIV_ss_tol: 0.1
25 New: 0
26 Plot_Solution: 1
27 Flexible_Wire: 0
28 Option: 0
29 Layout_Mode: 0
30 Floor_plan: 40,70
31 Num_of_layouts: 20
```

Figure 53. Example macro script showing reliability awareness flag and constraint file location.

Based on the voltage levels mentioned on each trace, the program calculates what the voltage difference is across a gap. This calculation is detailed in [99] and is provided as a table-figure here in Figure 55. There are two ways to calculate voltage difference: "Average Case" and "Worst Case." "Worst case" is chosen when the reliability-awareness flag is set to "1" and "Average case" is chosen when the flag is set to 2. The average case calculations account for the frequency and phase shift of the voltage levels and present the most accurate reflection of the voltage difference present across a trace gap at any time.

Once the voltage difference is calculated, it is looked up in the constraint file under the "Voltage Difference" section and the "Minimum Spacing" is returned. In the existing implementation of the tool, if the voltage difference being looked up is not found, the program presents an error. This means the user would have to calculate all voltage differences that might occur in the layout ahead of time and populate this table accordingly. It is difficult for a user to

know what voltages to list and what the corresponding appropriate gap is. Even better, this step can be automated. The implementation method presented in the next section discusses this.

layout.csv

Min Dimensions	EMPTY	power_trace	signal_trace	bonding wire pad	power_lead	signal_lead	MOS
Min Width	1	2	2	1	3	1	4
Min Height	1	2	2	1	3	1	6
Min Extension	1	2	2	1	3	1	6
Min Spacing	EMPTY	power_trace	signal_trace	bonding wire pad	power_lead	signal_lead	MOS
EMPTY	0.5	0.5	0.5	0.5	0.5	0.5	0.5
power_trace	0.5	0.5	0.5	0.5	0.5	0.5	0.5
signal_trace	0.5	0.5	0.5	0.5	0.5	0.5	0.5
bonding wire pad	0.5	0.5	0.5	2	0.5	0.5	0.5
power_lead	0.5	0.5	0.5	0.5	0.5	0.5	0.5
signal_lead	0.5	0.5	0.5	0.5	0.5	0.5	0.5
MOS	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Min Enclosure	EMPTY	power_trace	signal_trace	bonding wire pad	power_lead	signal_lead	MOS
EMPTY	1	1	1	1	1	1	1
power_trace	1	1	1	1	1	1	1
signal_trace	1	1	1	1	1	1	1
bonding wire pad	1	1	1	1	1	1	1
power_lead	1	1	1	1	1	1	1
signal_lead	1	1	1	1	1	1	1
MOS	1	1	1	1	1	1	1
Voltage Specification							
Component Name	DC magnitude	AC magnitude	Frequency (Hz)	Phase angle (degree)			
T1.4	0	0	10000	0			
T2.4	7.5	12.5	10000	0			
T3.4	10000	10000	10000	0			
T4.4	0	0	0	0			
T6.4	20000	0	0	0			
T7.4	10007.5	10012.5	10000	0			
T8.4	10000	10000	10000	0			
Current Specification							
Component Name	DC magnitude	AC magnitude	Frequency (Hz)	Phase angle (degree)			
T1.4	0	0	0	0			
T2.4	0	0	0	0			
T3.4	0	0	0	0			
T4.4	0	0	0	0			
T6.4	0	0	0	0			
T7.4	0	0	0	0			
T8.4	0	0	0	0			
Voltage Difference	Minimum Spacing						
0	0.5						
20	0.5						
19980	5						
20000	5						
20005	5						
20020	5						
Current Rating	Minimum Width						
0	2						

Figure 54. Constraint file with reliability constraints; inset: trace labels for voltage assignment.

Waveform	Sync	Average Case	Worst Case
DC-DC/AC	-	$\|A_1 - A_2\| + \|B_2\|$	$\|A_1 - A_2\| + \|B_2\|$
AC-AC $f_1 = f_2$	$\theta_1 = \theta_2$	$\|A_1 - A_2\| + \|B_1 - B_2\|$	$\|A_1 - A_2\| + \|B_1\| + \|B_2\|$
	$\theta_1 \neq \theta_2$	$\|A_1 - A_2\| + \sqrt{{B_1}^2 + {B_2}^2 - 2B_1B_2cos(\theta_1 - \theta_2)}$	
AC-AC	$f_1 \neq f_2$	$\|A_1 - A_2\| + \|B_1\| + \|B_2\|$	

Figure 55. Voltage difference calculation formula.

After the voltage difference is found in the list and the minimum spacing value is obtained, a constraint graph edge is formed that represents the spacing between traces, which then informs the layout geometry. However, currently, this list of minimum spacings is arbitrarily chosen. And here lies the purpose of this work, which is to inform design rules with not arbitrary but knowledgeable numbers based on 3D simulations that have been validated, and to have the program generate these values.

3.3.3 From the layer stack to the PDIV vs. gap curve

In the methodology implemented and described in this section, the layer stack of the module plays a critical role in determining the voltage handling capability of the layout. So, the voltage difference – minimum spacing list is informed by the layer stack. The program determines how to populate the list based on the layer stack input by the user. This way, the user does not need to know what voltage values to list, or their corresponding trace gaps.

An example power module layer stack was shown in Figure 1. Information for the various layers is input to PowerSynth in a csv format through its file path that is provided in the macro script (Figure 53). Figure 56 shows an example layer stack's information.

The row outlined in blue represents the encapsulant material, which was newly added to incorporate the effect of the dielectric material in the module's voltage handling capability. Previously, the tool did not have any information regarding the encapsulant; it was encapsulant-

layer_stack_2.csv

ID	Name	Width	Length	Thickness	Material	Type	Electrical
1	B1	50	80	1	copper	p	F
2	M1	42	72	0.3	copper	p	G
3	D1	40	70	0.64	Al2_O3_ceramic	p	D
4	I1	40	70	0.3	copper	p	S
5	C1	40	70	0.18	silicon	a	C
6	E1	50	80	3	dow_corning_3-6635_dielectric_gel	p	D

Figure 56. Example layer stack information input to PowerSynth with encapsulant information included.

agnostic. Now, with the addition of the encapsulant, one may derive electrical isolation capability at the interconnect level.

The information in the layer stack that is relevant for this discussion is highlighted. The material names are used as keys to lookup material properties from a material database stored in a location accessible to the user and editable. Figure 57 shows a snapshot of the material library,

Materials.csv

name	thermal_c	spec_heat	density	electrical	rel_permit	dielec_str	rel_perme	q3d_id	young_mc	poissons_	thermal_e	spe
dow_corning_3-6635_dielectric_gel					2.83	20						
dow_corning_3-4170					2.85	20						
Sylgard_184					2.72	19						
dow_corning_3-4190					2.86	19						
dow_corning_3-4237					2.96	19						
Wacker_612					2.7	23						
dow_corning_3-4241					2.6	17						
Fields Metal	18.9	300	7900									
vacuum					1			vacuum				
pec				1.00E-30				pec				
perfect conductor				1.00E-30				perfect conductor				
Al2_O3_ceramic	35	850	3960		9.8	20		Al2_O3_ce	3.70E+11	0.22	8.10E-06	
Si3_N4_ceramic					7.8	15						
Al_N	120	734.3	3250		8.8	20		Al_N	3.05E+11		5.20E-06	
filler_compound1					3	25						
steel_stainless	13.8	480	8055	9.09E-07				steel_stai	1.95E+11	0.3	1.08E-05	
zinc	115.5	389	7140	5.99E-08				zinc	1.15E+11	0.33	6.35E-05	
nickel	90	444	8900	6.90E-08			600	nickel	2.10E+11	0.35	1.30E-05	
beryllium	190	1824	1848	4.00E-08			1.000001	beryllium	3.00E+11	0.03	9.20E-06	
solder	48	167	8000	1.43E-07				solder	6.9E+10	0.4	1.59E-06	
tin								tin				
titanium	21	522	4500	5.49E-07			1.00018	titanium	1.15E+11	0.33	8.30E-06	
brass	111	162	8600	6.67E-08				brass	1.00E+11	0.34	3.39E-05	

Figure 57. Partial snapshot of the materials database.

with newly added rows of encapsulants and ceramic isolation materials marked in blue, and other relevant materials for this discussion marked in dark grey. The “dielec_str” column was added to input the dielectric strength of a material in kV/mm. Given a layer stack, PowerSynth can look up the relative permittivity of the ceramic isolation material and the encapsulant material, and the dielectric strength of both of those materials too.

Every layer stack has a unique PDIV vs. gap curve-set as shown before in Figure 46, Figure 47, and Figure 48. Given a layer stack, PowerSynth should be able to create the corresponding PDIV vs. gap curve. To do so, it needs to:

1. translate the data library to a dataframe.
2. lookup the layer stack parameters in a dataframe where the simulation results are stored and return the charge density vs. gap information.
3. calculate the PDIV and determine the diminishing return point.
4. plot the PDIV vs. gap results for both the ceramic and the encapsulant.

All simulated results of charge density for the parameter values listed in Table 20 and Table 21 are consolidated into a growing data library and stored as a csv file like the one shown in Figure 58, which is read into PowerSynth as a data frame. The figure shows only a small subset of the library. The actual library at the time of this writing holds over 2300 records comprising roughly more than 190 unique layer stacks. This library is named the “default_PD_datalib”, henceforth referred to as the PD data library. Its file path is provided to the tool the same way the materials database path is provided: through a settings.py file. The parameters listed in Table 20 and Table 21 correspond to the rpE, rpC, tc_mm, and tm_mm columns in the simulated data library. The charge density columns are labelled Qside_uCperM2 and Qbottom_uCperM2 in the data library. They have units of $\mu C/m^2$, and tc_mm and tm_mm

are in millimeters, and gap_mm is also in mm.

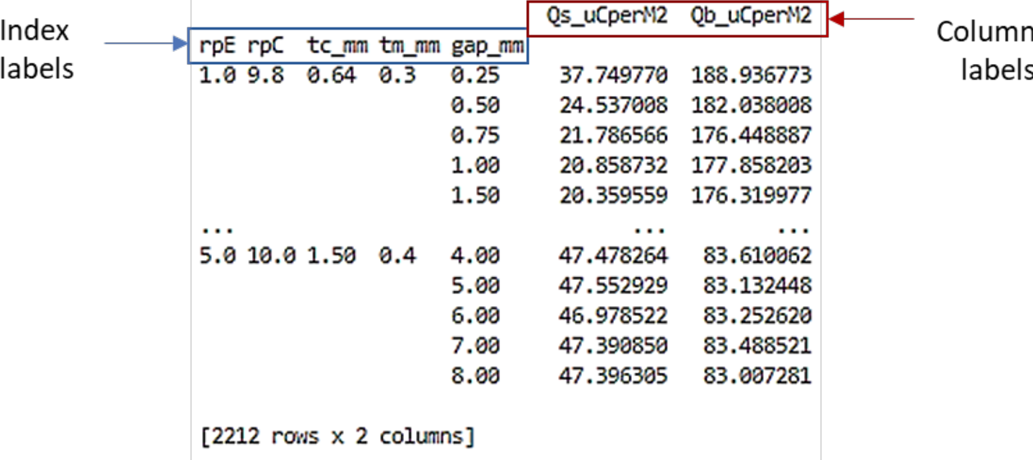
default_PD_datalib.csv

	A	B	C	D	E	F	G
1	rpE	rpC	tc_mm	tm_mm	gap_mm	Qside_uCperM2	Qbottom_uCperM2
354	1	6	0.25	0.1	0.25	62.92106594	466.0427202
355	1	6	0.25	0.1	0.5	58.29215898	475.7958341
356	1	6	0.25	0.1	0.75	57.59494078	474.5022407
357	1	6	0.25	0.1	1	57.80824769	476.0821529
358	1	6	0.25	0.1	1.5	57.29216887	475.7970228
359	1	6	0.25	0.1	2	57.46666591	473.1137273
360	1	6	0.25	0.1	3	58.01699152	476.859405
361	1	6	0.25	0.1	4	56.85931756	474.543524
362	1	6	0.25	0.1	5	57.54071364	476.1120859
363	1	6	0.25	0.1	6	57.37141581	472.5053507
364	1	6	0.25	0.1	7	57.4986496	479.4145972
365	1	6	0.25	0.1	8	57.69453281	474.4502943
366	1	6	0.25	0.2	0.25	45.9092698	393.0153002
367	1	6	0.25	0.2	0.5	38.17357158	388.5174826
368	1	6	0.25	0.2	0.75	37.33945504	387.940709
369	1	6	0.25	0.2	1	37.54298553	385.7846191
370	1	6	0.25	0.2	1.5	36.98797493	388.6416986
371	1	6	0.25	0.2	2	37.22462687	389.6170672
372	1	6	0.25	0.2	3	37.22997494	388.5358623
373	1	6	0.25	0.2	4	37.01230264	389.8295224
374	1	6	0.25	0.2	5	37.12207718	389.2510405
375	1	6	0.25	0.2	6	37.15363046	389.0683584
376	1	6	0.25	0.2	7	37.21838685	389.371994
377	1	6	0.25	0.2	8	37.00580999	389.5847056
378	1	6	0.25	0.3	0.25	40.19662306	360.7364969
379	1	6	0.25	0.3	0.5	30.25741267	360.9160528
380	1	6	0.25	0.3	0.75	28.4414572	359.761371
381	1	6	0.25	0.3	1	28.31296576	358.9395036
382	1	6	0.25	0.3	1.5	28.04156804	360.0522322
383	1	6	0.25	0.3	2	28.10775543	358.4571279
384	1	6	0.25	0.3	3	28.21076753	359.6421995
385	1	6	0.25	0.3	4	28.10708537	358.956573
386	1	6	0.25	0.3	5	28.1784556	360.6959479
387	1	6	0.25	0.3	6	28.15649717	359.0989868
388	1	6	0.25	0.3	7	28.17638875	358.2199009
389	1	6	0.25	0.3	8	28.09833855	358.8163403
390	1	6	0.25	0.4	0.25	37.70311571	347.4702542
391	1	6	0.25	0.4	0.5	25.87970844	346.3085856
392	1	6	0.25	0.4	0.75	23.67363203	346.1025834
393	1	6	0.25	0.4	1	23.09155558	346.3602366
394	1	6	0.25	0.4	1.5	23.04245568	346.290397
395	1	6	0.25	0.4	2	22.89003746	346.9448435
396	1	6	0.25	0.4	3	22.79291338	346.9782531
397	1	6	0.25	0.4	4	22.77952897	346.8502024
398	1	6	0.25	0.4	5	22.84474822	346.0870023
399	1	6	0.25	0.4	6	22.62791029	347.2584402
400	1	6	0.25	0.4	7	22.46255082	346.2696092

Figure 58. Snippet of the raw data library of charge density vs. gap for various parameter values that were simulated.

3.3.3.1 PD data library to dataframe

Dataframes are basically like tables one may use in a structured query language with heterogenous data types. The pre-built Pandas library in python has a Dataframe class for data science applications and manipulating N-dimensional data. A dataframe is composed of rows and columns where some of the columns may be used as indexes. For this work, the PD data library csv file was read into PowerSynth using a Pandas csv reader method that automatically stores the information into a dataframe. An example of the PD data library loaded as a dataframe is shown in Figure 59. Here, the four parameters of the layer stack and the gap together form the index, and the rest of the columns are for the charge density results corresponding to the index.

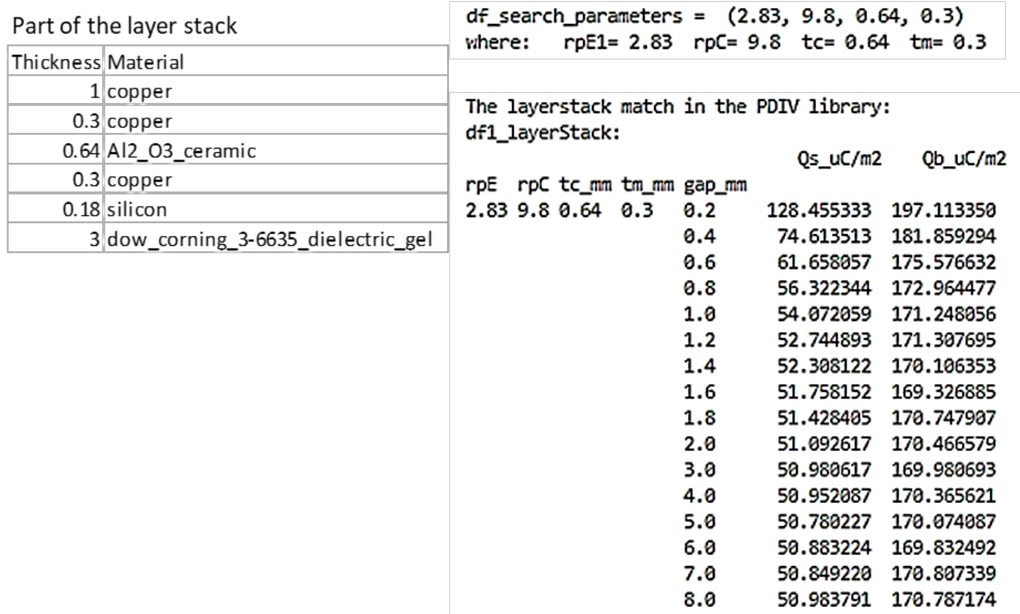



```
                              Qs_uCperM2  Qb_uCperM2
rpE rpC  tc_mm tm_mm gap_mm
1.0 9.8  0.64  0.3   0.25      37.749770  188.936773
                     0.50      24.537008  182.038008
                     0.75      21.786566  176.448887
                     1.00      20.858732  177.858203
                     1.50      20.359559  176.319977
...                                  ...         ...
5.0 10.0 1.50  0.4   4.00      47.478264   83.610062
                     5.00      47.552929   83.132448
                     6.00      46.978522   83.252620
                     7.00      47.390850   83.488521
                     8.00      47.396305   83.007281

[2212 rows x 2 columns]
```

Figure 59. PD data library read into PowerSynth as a dataframe.

3.3.3.2 Layer stack search in the dataframe

The layer stack parameters were extracted from the layer stack table (Figure 56) and used as a key to search for the corresponding Q vs gap information in the dataframe, using dataframe.loc[], a built-in way to return all columns for a given index. If a direct match of the layer stack was found in the index of the PD data frame, those rows of the dataframe were saved as another dataframe for further processing. Figure 60 shows an example of the search



Part of the layer stack

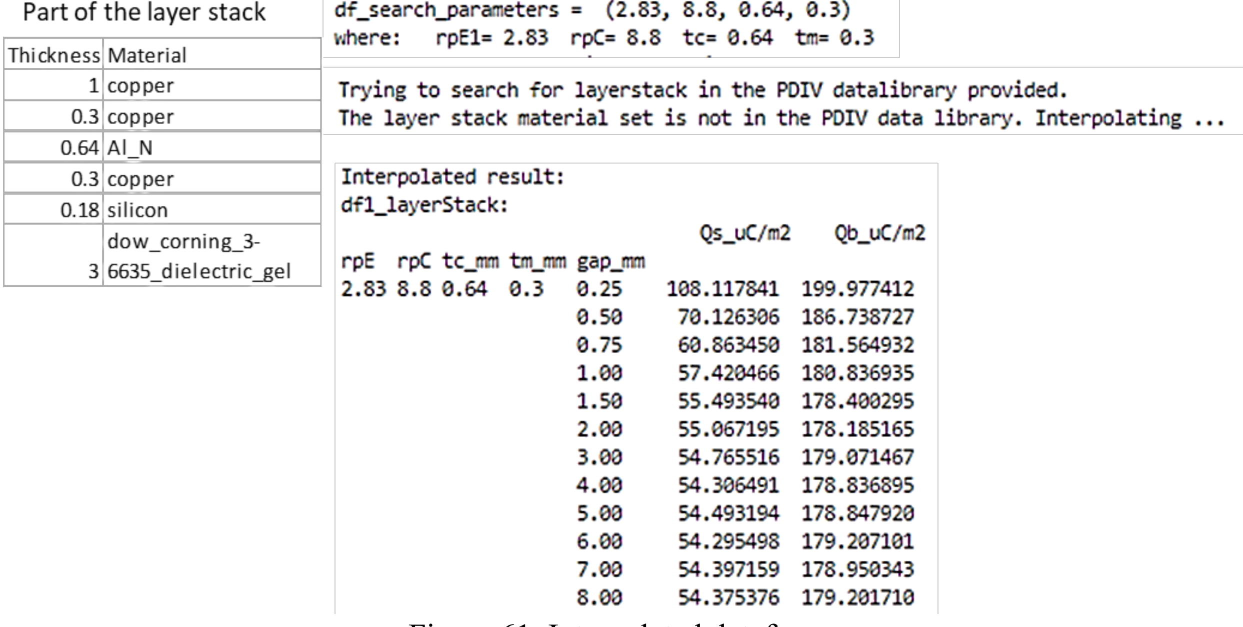
Thickness	Material
1	copper
0.3	copper
0.64	Al2_O3_ceramic
0.3	copper
0.18	silicon
3	dow_corning_3-6635_dielectric_gel

```
df_search_parameters =  (2.83, 9.8, 0.64, 0.3)
where:   rpE1= 2.83  rpC= 9.8  tc= 0.64  tm= 0.3

The layerstack match in the PDIV library:
df1_layerStack:
                                   Qs_uC/m2    Qb_uC/m2
rpE  rpC tc_mm tm_mm gap_mm
2.83 9.8 0.64  0.3   0.2      128.455333  197.113350
                     0.4       74.613513  181.859294
                     0.6       61.658057  175.576632
                     0.8       56.322344  172.964477
                     1.0       54.072059  171.248056
                     1.2       52.744893  171.307695
                     1.4       52.308122  170.106353
                     1.6       51.758152  169.326885
                     1.8       51.428405  170.747907
                     2.0       51.092617  170.466579
                     3.0       50.980617  169.980693
                     4.0       50.952087  170.365621
                     5.0       50.780227  170.074087
                     6.0       50.883224  169.832492
                     7.0       50.849220  170.807339
                     8.0       50.983791  170.787174
```

Figure 60. Layer stack parameter match in the PDIV dataframe index.

parameters and the dataframe returned from running a search for those parameters.

If the layer stack parameters are not found in the index of the dataframe, then an interpolation function is run to generate a result. Scipy python module's linearNDInterpolator was used for interpolation. An example with interpolation is shown in Figure 61.



Part of the layer stack

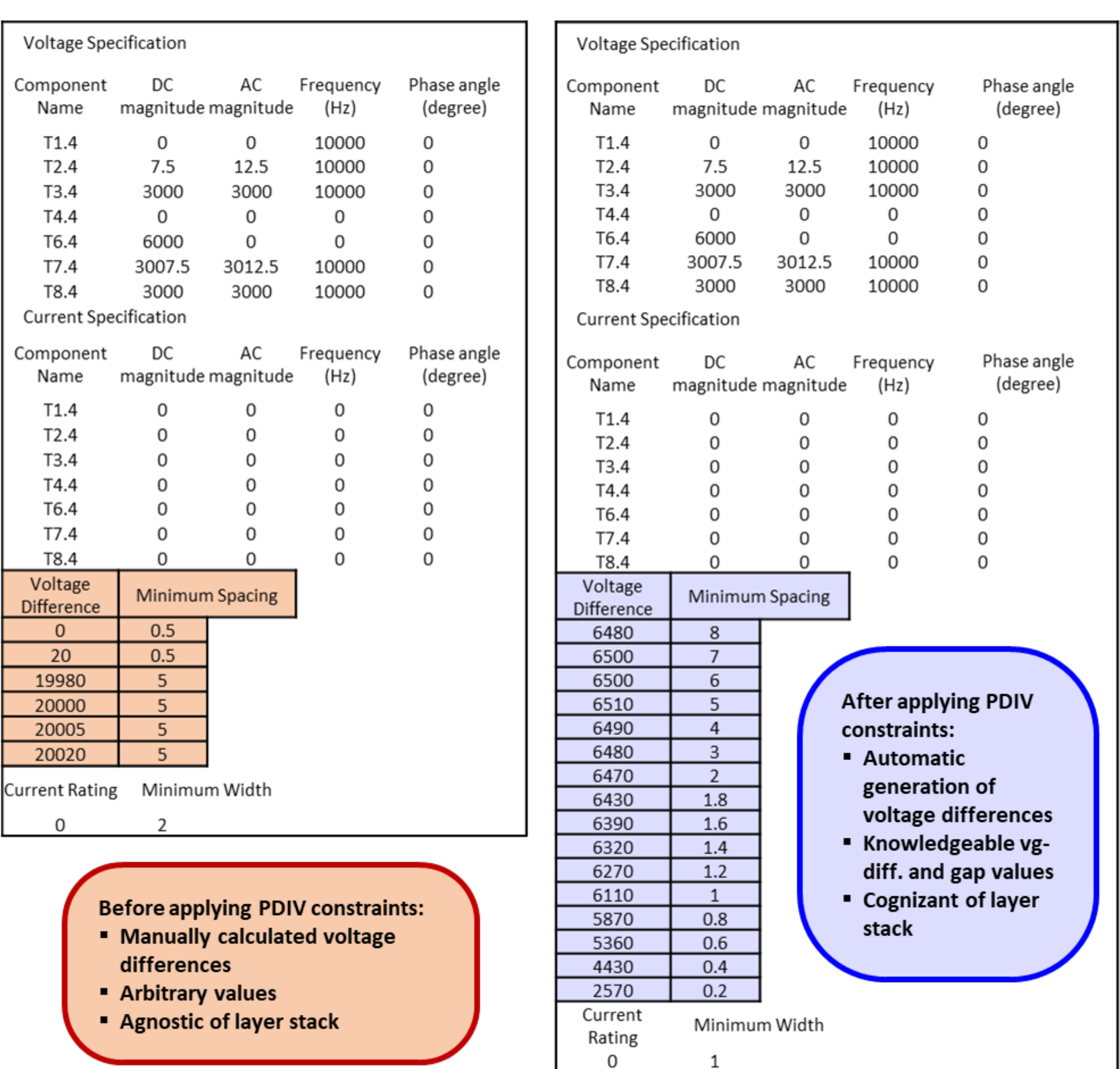
Thickness	Material
1	copper
0.3	copper
0.64	Al_N
0.3	copper
0.18	silicon
3	dow_corning_3-6635_dielectric_gel

```
df_search_parameters =  (2.83, 8.8, 0.64, 0.3)
where:   rpE1= 2.83  rpC= 8.8  tc= 0.64  tm= 0.3

Trying to search for layerstack in the PDIV datalibrary provided.
The layer stack material set is not in the PDIV data library. Interpolating ...

Interpolated result:
df1_layerStack:
                                   Qs_uC/m2    Qb_uC/m2
rpE  rpC tc_mm tm_mm gap_mm
2.83 8.8 0.64  0.3   0.25     108.117841  199.977412
                     0.50      70.126306  186.738727
                     0.75      60.863450  181.564932
                     1.00      57.420466  180.836935
                     1.50      55.493540  178.400295
                     2.00      55.067195  178.185165
                     3.00      54.765516  179.071467
                     4.00      54.306491  178.836895
                     5.00      54.493194  178.847920
                     6.00      54.295498  179.207101
                     7.00      54.397159  178.950343
                     8.00      54.375376  179.201710
```

Figure 61. Interpolated dataframe.

3.3.3.3 PDIV calculation and DRP determination

Once the correct Q vs. gap information is found in the PD data library, PowerSynth computes the PDIV according to the equations presented in Chapter 2, for both the encapsulant and the ceramic. Then it finds the lesser of the two and populates a new column with that PDIV and updates the Voltage Difference – Minimum Spacing part of the constraint file (highlighted in Figure 62). The next step is to calculate the diminishing return point of PDIV vs. gap.



Before applying PDIV constraints

Voltage Specification

Component Name	DC magnitude	AC magnitude	Frequency (Hz)	Phase angle (degree)
T1.4	0	0	10000	0
T2.4	7.5	12.5	10000	0
T3.4	3000	3000	10000	0
T4.4	0	0	0	0
T6.4	6000	0	0	0
T7.4	3007.5	3012.5	10000	0
T8.4	3000	3000	10000	0

Current Specification

Component Name	DC magnitude	AC magnitude	Frequency (Hz)	Phase angle (degree)
T1.4	0	0	0	0
T2.4	0	0	0	0
T3.4	0	0	0	0
T4.4	0	0	0	0
T6.4	0	0	0	0
T7.4	0	0	0	0
T8.4	0	0	0	0

Voltage Difference	Minimum Spacing
0	0.5
20	0.5
19980	5
20000	5
20005	5
20020	5

Current Rating	Minimum Width
0	2

After applying PDIV constraints

Voltage Specification

Component Name	DC magnitude	AC magnitude	Frequency (Hz)	Phase angle (degree)
T1.4	0	0	10000	0
T2.4	7.5	12.5	10000	0
T3.4	3000	3000	10000	0
T4.4	0	0	0	0
T6.4	6000	0	0	0
T7.4	3007.5	3012.5	10000	0
T8.4	3000	3000	10000	0

Current Specification

Component Name	DC magnitude	AC magnitude	Frequency (Hz)	Phase angle (degree)
T1.4	0	0	0	0
T2.4	0	0	0	0
T3.4	0	0	0	0
T4.4	0	0	0	0
T6.4	0	0	0	0
T7.4	0	0	0	0
T8.4	0	0	0	0

Voltage Difference	Minimum Spacing
6480	8
6500	7
6500	6
6510	5
6490	4
6480	3
6470	2
6430	1.8
6390	1.6
6320	1.4
6270	1.2
6110	1
5870	0.8
5360	0.6
4430	0.4
2570	0.2

Current Rating	Minimum Width
0	1

Figure 62. Layout.csv before and after PDIV design rule implementation.

This is done by calculating the slope of the PDIV vs. gap curve of the lesser of the two PDIV curves (for the encapsulant and the ceramic) and finding at what point the curve reaches close to zero slope. To determine how close is close, a tolerance is set on the steady state value determination that the user can edit in the macro file and a slope magnitude column is added to the dataframe. Some of these computations are added as columns to the dataframe and an example is shown in Figure 63. In order to easily extract the voltage and gap at which the slope reaches below the tolerance level, the gap column was taken out of the index list and made a regular column.

```
df1_layerStack_reindexed:
                          gap_mm    Qs_uC/m2    Qb_uC/m2  PDIVenc_kV  PDIVcer_kV  PDIV_kV  abs_slope
rpE  rpC tc_mm tm_mm
2.83 9.8 0.64  0.3          0.2  128.455333  197.113350        2.57        5.81     2.57        NaN
               0.3          0.4   74.613513  181.859294        4.43        6.30     4.43       9.30
               0.3          0.6   61.658057  175.576632        5.36        6.52     5.36       4.65
               0.3          0.8   56.322344  172.964477        5.87        6.62     5.87       2.55
               0.3          1.0   54.072059  171.248056        6.11        6.69     6.11       1.20
               0.3          1.2   52.744893  171.307695        6.27        6.68     6.27       0.80
               0.3          1.4   52.308122  170.106353        6.32        6.73     6.32       0.25
               0.3          1.6   51.758152  169.326885        6.39        6.76     6.39       0.35
               0.3          1.8   51.428405  170.747907        6.43        6.70     6.43       0.20
               0.3          2.0   51.092617  170.466579        6.47        6.72     6.47       0.20
               0.3          3.0   50.980617  169.980693        6.48        6.74     6.48       0.01
               0.3          4.0   50.952087  170.365621        6.49        6.72     6.49       0.01
               0.3          5.0   50.780227  170.074087        6.51        6.73     6.51       0.02
               0.3          6.0   50.883224  169.832492        6.50        6.74     6.50       0.01
               0.3          7.0   50.849220  170.807339        6.50        6.70     6.50       0.00
               0.3          8.0   50.983791  170.787174        6.48        6.70     6.48       0.02

self.PDIV_ss_tol: 0.1
DRP_vg_gap (kV, mm):  (6.47, 2.0)
```

Figure 63. Computations made on the dataframe for PDIV and DRP.

The DRP is then determined based on the magnitude change in the slope of the PDIV vs gap curve, and the steady state tolerance (PDIV_ss_tol Figure 63). The algorithm to determine when the PDIV vs gap curve reaches a steady state value is to choose the last gap *after* which the PDIV slope magnitude stays under the tolerance value twice in a row. In this example, the steady state tolerance is set to 0.1, and this is customizable in the macro file. Looking at the abs_slope

column, the value reaches under 0.1 for the first time when gap = 3.0 mm and it stays below 0.1 for 4.0 mm (the next data point). The data point right after this transition happens, is gap = 2.0 mm. So, we choose 2.0 mm, 6.47 kV as the diminishing return point, as shown at the bottom of Figure 63. The DRP in terms of the voltage and the trace gap are listed at the bottom of the figure, as computed in the tool.

3.3.3.4 PDIV vs. gap plot for the layer stack

The PDIVenc_kV column and the PDIVcer_kV column is plotted against the gap_mm column. The user can gain a lot of useful insight into how the encapsulant and ceramic compare in terms of PDIV and gap for the given layer stack from this plot. This plot can be accessed in the figure directory whose filepath is mentioned in the macro file. Some examples of these plots were shown in figures before (Figure 46, Figure 47, and Figure 48). Figure 46 is the plot that results from the dataframe shown in Figure 63.

To summarize the approach of the PDIV design rule implementation so far, PowerSynth is now able to input the entire PD data library as a dataframe and find the correct subset of the dataframe given a layer stack. Then it can compute PDIV for both the encapsulant and the ceramic and plot them against trace gap and determine the diminishing return point. The next section explores how the DRP values are used in the program.

3.3.4 Maximum voltage allowance and DRP application

The maximum voltage allowance ensures the maximum voltage that the system can operate at is compatible with the layer stack chosen, and the diminishing returns point helps the program know where to limit the increase of tracegap for maximum voltage benefit.

As seen in Figure 46, Figure 47, and Figure 48 before, there is a maximum voltage level for each layer stack. Once PowerSynth finds the voltage difference from the user's input of

voltage levels on each trace, the program first compares it to the maximum of the voltages in the PDIV_kV column of the dataframe for that layer stack. If the voltage difference between the traces is higher than the highest voltage the layer stack can sustain, the program quits with a message informing the user of the limitation and advising them to upgrade the layer stack, with recommendation on how to do so. If the voltage difference between the traces is less than the highest voltage the layer stack can sustain, then the program finds the associated gap_mm for the PDIV_kV, interpolating if an exact match is not found.

Finally, the program compares the gap found to the DRP gap. If the gap found exceeds the DRP gap, the program limits the gap value to the DRP gap, since there would be no voltage benefit to increasing the gap beyond the diminishing return point. The final value becomes the edge weight for the Edge object that is created and would subsequently be part of the constraint graph of the final layout generated.

Therefore, instead of populating the edge weight with the default constraint of 0.5 mm spacing, or an arbitrarily chosen value from the reliability constraints, which are often extremely large (like, 5 mm), PowerSynth now populates the edge weight with a knowledgeable value informed from charge density simulations that have been validated, and influenced by the layer stack materials and geometry, and the voltages present on the traces. The end result is a layout that is optimized for voltage level and compactness. The next section is a discussion of the layouts generated as a result of this work.

3.4 Implementation Results

The goal of this implementation work has been to provide a framework for adjusting layout design rules for PD-free operation. This is so that PowerSynth can qualify layouts generated to be electrically reliable in terms of being PD-mitigated. Applying these adjusted gap

rules to layouts help us compare various layouts for their PD-informed voltage handling capability and physical size tradeoff. In the process, one may optimize a layout for voltage and spacing. PowerSynth can now:

1. quantify the PD-informed voltage rating of layouts being generated,
2. generate layouts for PD-informed operation at various voltage levels for a given layer stack,
3. quantify the maximum operating voltage possible for a layer stack and determine the optimum trace gap for that voltage level.
4. provide information on how to upgrade the layer stack to better optimize voltage and spacing.

These features are demonstrated in this section through the following examples.

3.4.1 Voltage rating for a layout with default design rules

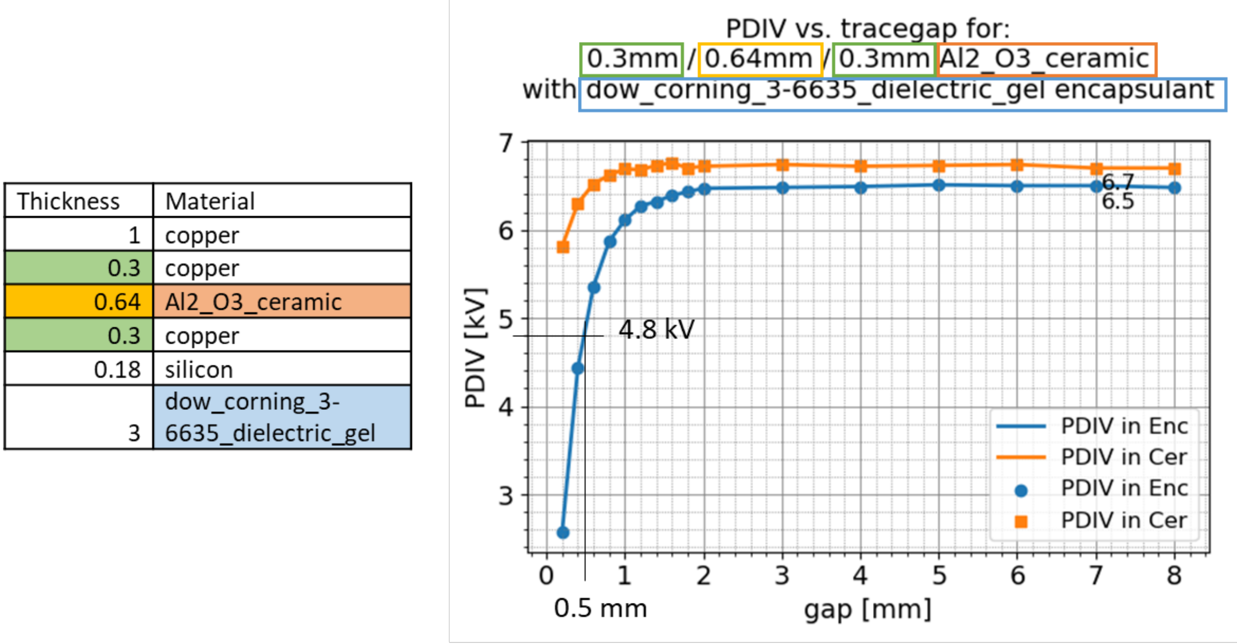
Consider the following layer stack and the minimum sized layout (Figure 64) that has default design rules where all gaps are set to 0.5 mm, the manufacturing limit for DBC etching. Previously, there was no way to know what voltage this layout and layer stack combination could operate at safely without much PD. But with the PD-informed design rule implementation, considering the layer stack and the default trace gap, one can look at the PDIV vs. trace gap curve (Figure 65) and determine the PD-minimized voltage handling capability of this layout. In this case, at 0.5 mm, the PDIV is 4.8 kV. This is the maximum voltage this layer stack and layout combination can sustain without much PD. This is useful information that was not available before. Knowing this can help aid design safety decisions. From the curve generated, module designers can also see that there may be other voltage-spacing options possible. This is explored in the next section.

Thickness	Material
1	copper
0.3	copper
0.64	Al2_O3_ceramic
0.3	copper
0.18	silicon
3	dow_corning_3-6635_dielectric_gel

Starting point layout:

Default design rule: 0.5mm spacing between traces (manufacturing limit)

Figure 64. Default design rule layout for the 12/25/12 alumina layer stack with Dow 3-6635 gel.



Thickness	Material
1	copper
0.3	copper
0.64	Al2_O3_ceramic
0.3	copper
0.18	silicon
3	dow_corning_3-6635_dielectric_gel

Figure 65. PDIV vs. gap curves for the 12/25/12 alumina layer stack with Dow 3-6635 gel.

3.4.2 Voltage-spacing solutions for the same layer stack

Figure 66 shows some examples of various layout options possible at different points on the PDIV vs. gap curve for the same layer stack. The highest voltage that can be obtained with this layer stack is 6.47 kV as shown in the curve since this is the diminishing return point. Its corresponding layout is shown in the figure as Layout D.

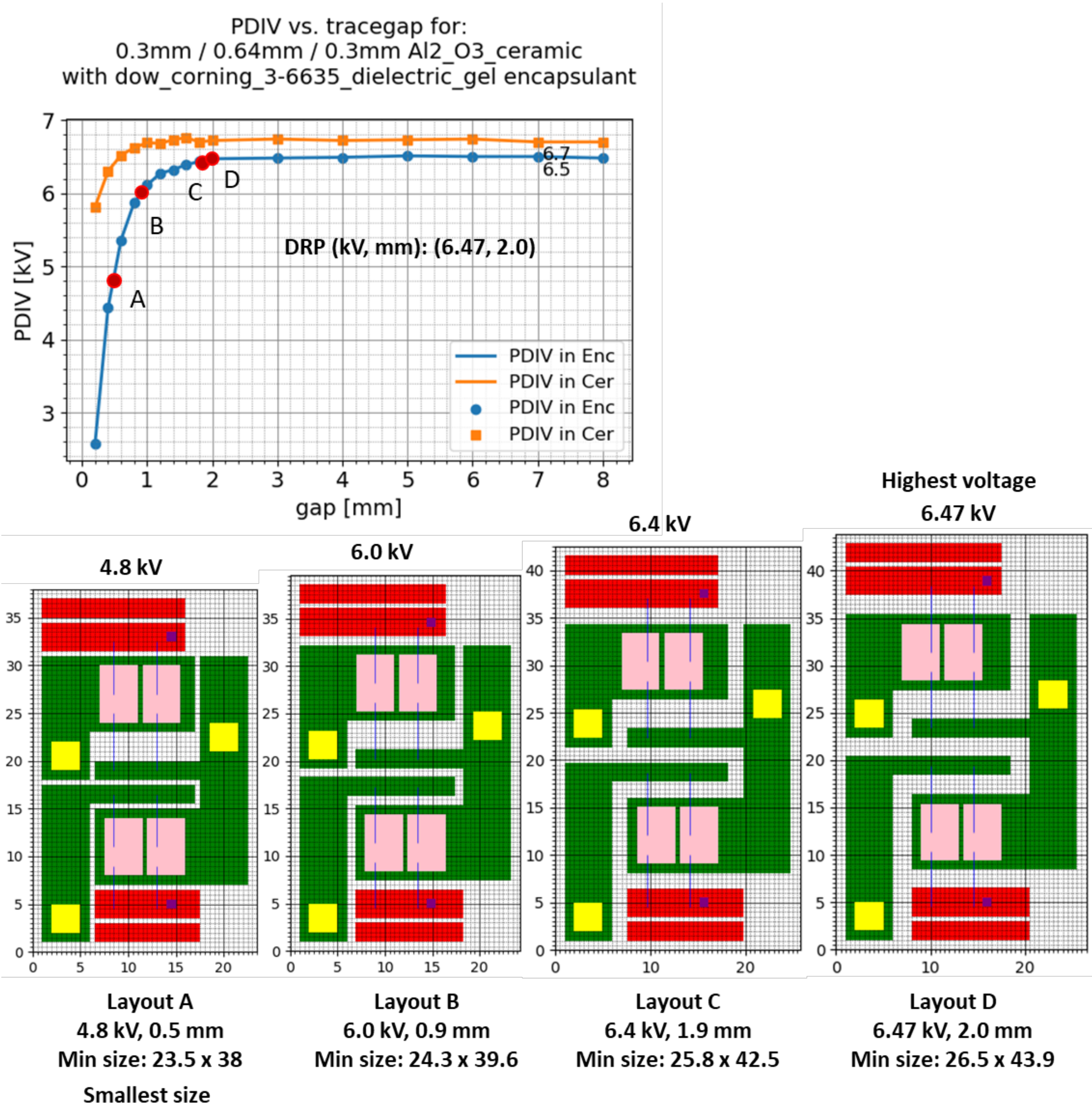


Figure 66. Layout options for the 12/25/12 alumina layer stack with Dow 3-6635 gel.

3.4.3 Voltage-spacing options for an upgraded layer stack

As discussed in Sections 3.1.2 and 3.1.3, the encapsulant is the material that is compromised at a lower voltage in Figure 66, with a voltage cap of 6.47 kV. Upgrading the encapsulant to one that has better voltage handling capability, such as the Wacker 612, the layouts obtained can operate at higher voltages and are more compact for same voltage (Figure 67). Note that above 0.8 mm, the ceramic becomes the material with the lower PDIV.

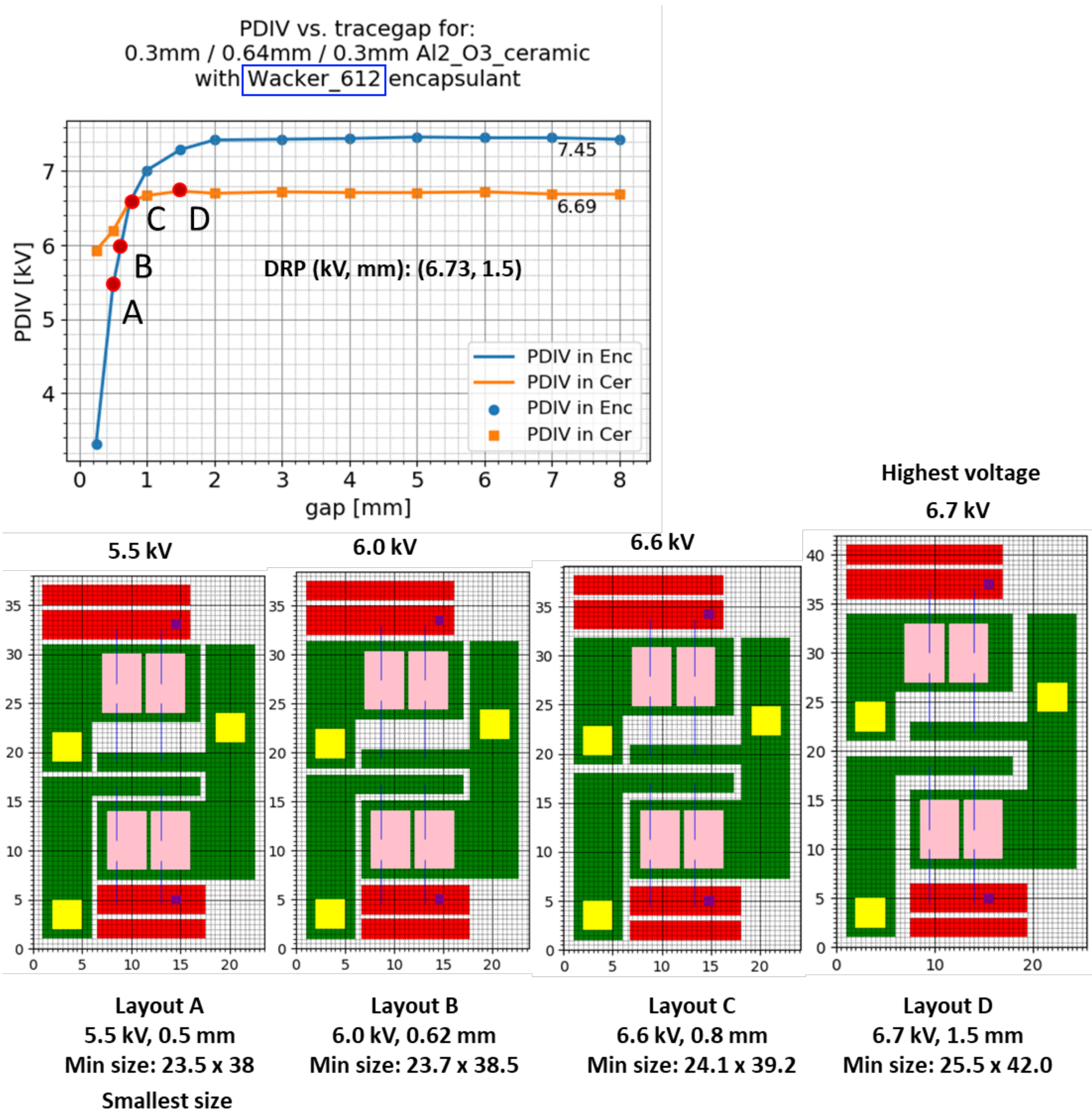


Figure 67. Layout options for the 12/25/12 alumina layer stack with Wacker 612 gel.

3.4.4 Comparison of the effect of upgrading the layer stack

3.4.4.1 Constant spacing

Changing the encapsulant from the Dow gel to the Wacker gel moved the PDIV vs. gap curve in a way that one can obtain a higher voltage while keeping the layout size the same. Figure 68 compares the two layouts. With the Dow gel, the minimum size layout can operate at a maximum of 4.8 kV, whereas with the Wacker gel, it is 5.5 kV. That's a 15% improvement and is useful information for power module designers to have.

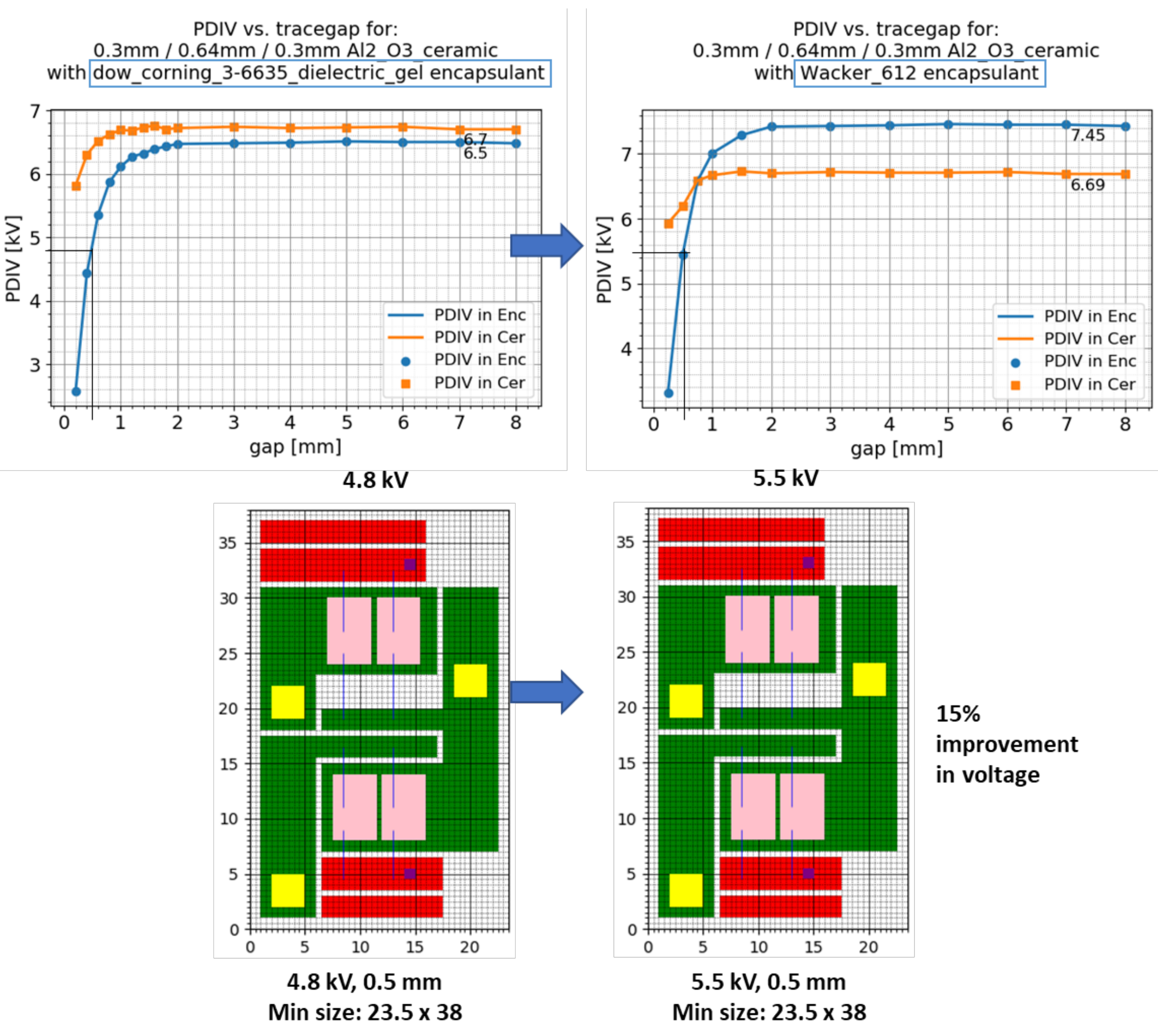


Figure 68. Effect of upgrading the encapsulant on the minimum size layout.

Another example of the effect of this upgrade on layouts of the same size is shown in Figure 69. Here, both layouts have gaps of 0.8 mm, and there is a 13% improvement in the maximum voltage level they can operate at.

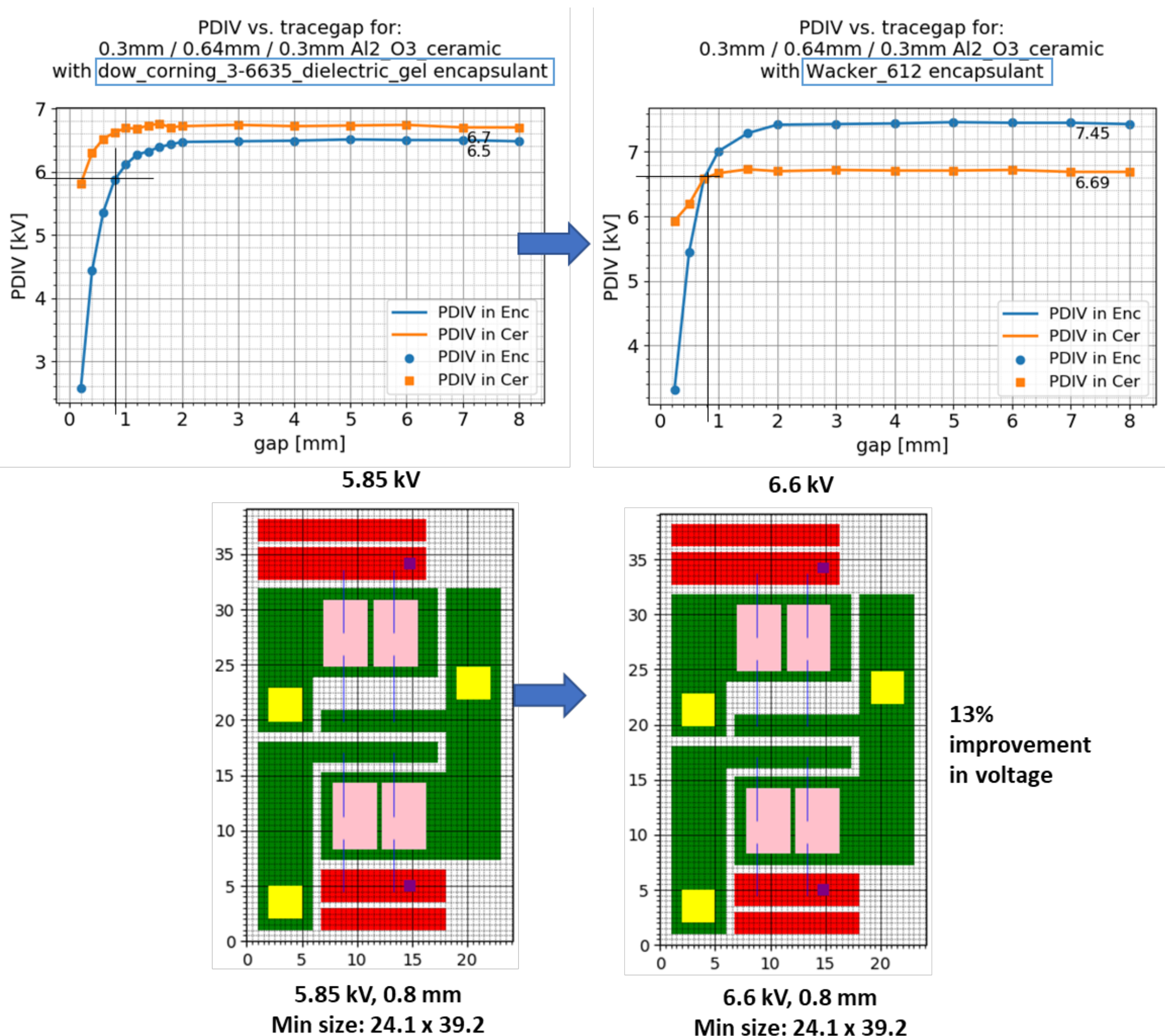


Figure 69. Effect of upgrading the encapsulant on layouts of the same size.

3.4.4.2 Constant voltage

Another way to look at the effect of the layer stack upgrade on layouts is by comparing the level of compactness for a constant voltage level. Figure 70 shows two examples that depict this, one with a 20% improvement in area reduction, and the other with a 5% improvement.

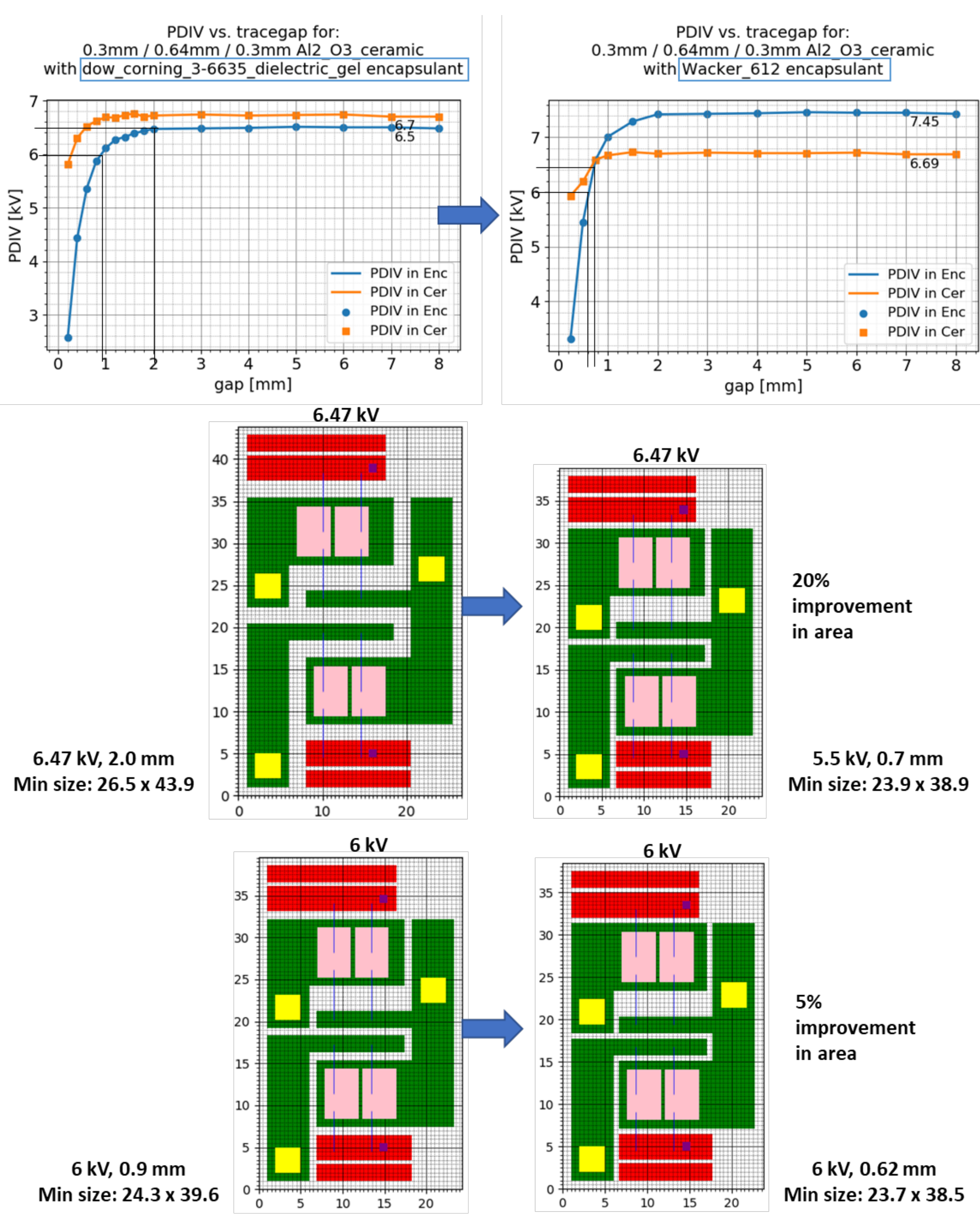


Figure 70. Effect of upgrading the encapsulant on layouts of the same voltage handling capability.

3.4.5 Further upgrading the layer stack

The layer stack with the Wacker gel improved the voltage handling prospects, but the combined layer stack is still limited to a maximum voltage handling capability of 6.7 kV, with the ceramic being the material that would be compromised first at higher trace gaps. To improve the voltage prospects further, the ceramic material must be improved as discussed before in Section 3.1.3 using Table 18. Figure 71 shows some of the layouts possible with this upgrade.

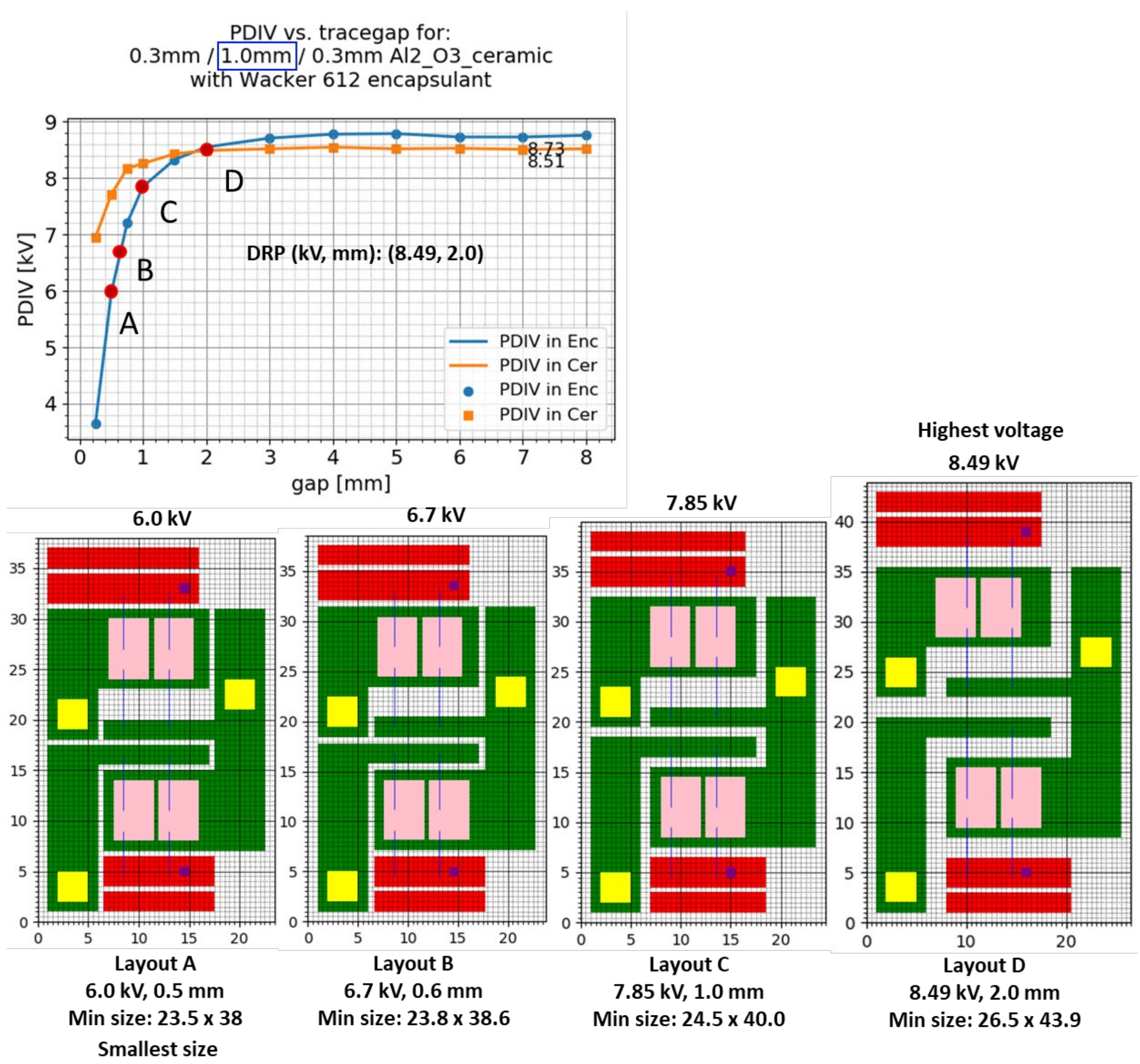


Figure 71. Layout options for the 12/40/12 alumina layer stack with Wacker 612 gel.

Figure 72 shows the effect of choosing a thicker ceramic on layouts of the same size, with the Wacker gel. For the minimum size layout, voltage capability increases 9%, and for the 1.5mm gap layout, it increases 24%.

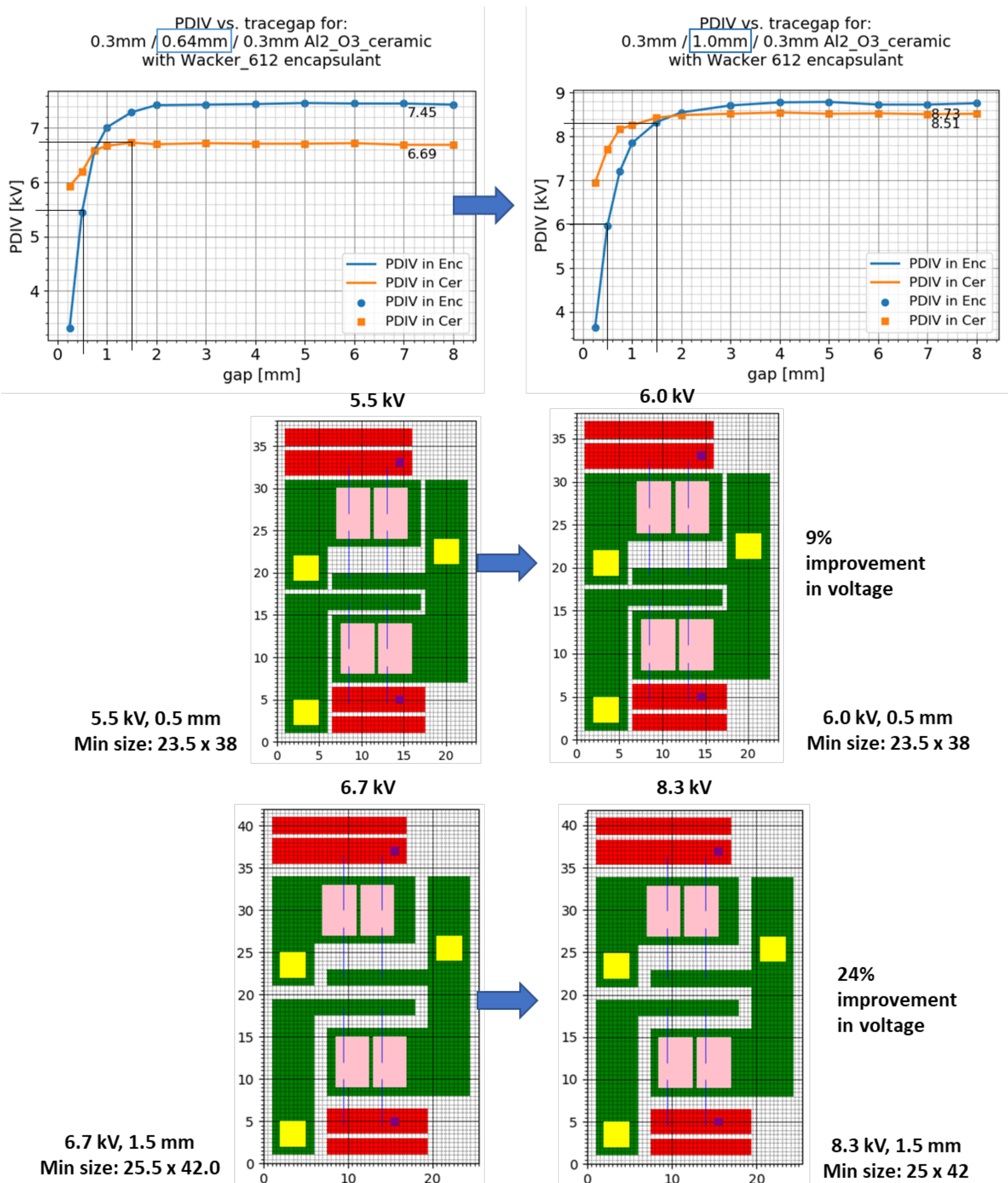


Figure 72. Effect of increasing the ceramic thickness on layouts of the same size.

Figure 73 shows the effect of choosing a thicker ceramic on layouts that have the same voltage handling capability. Layouts were made up to 14% more compact.

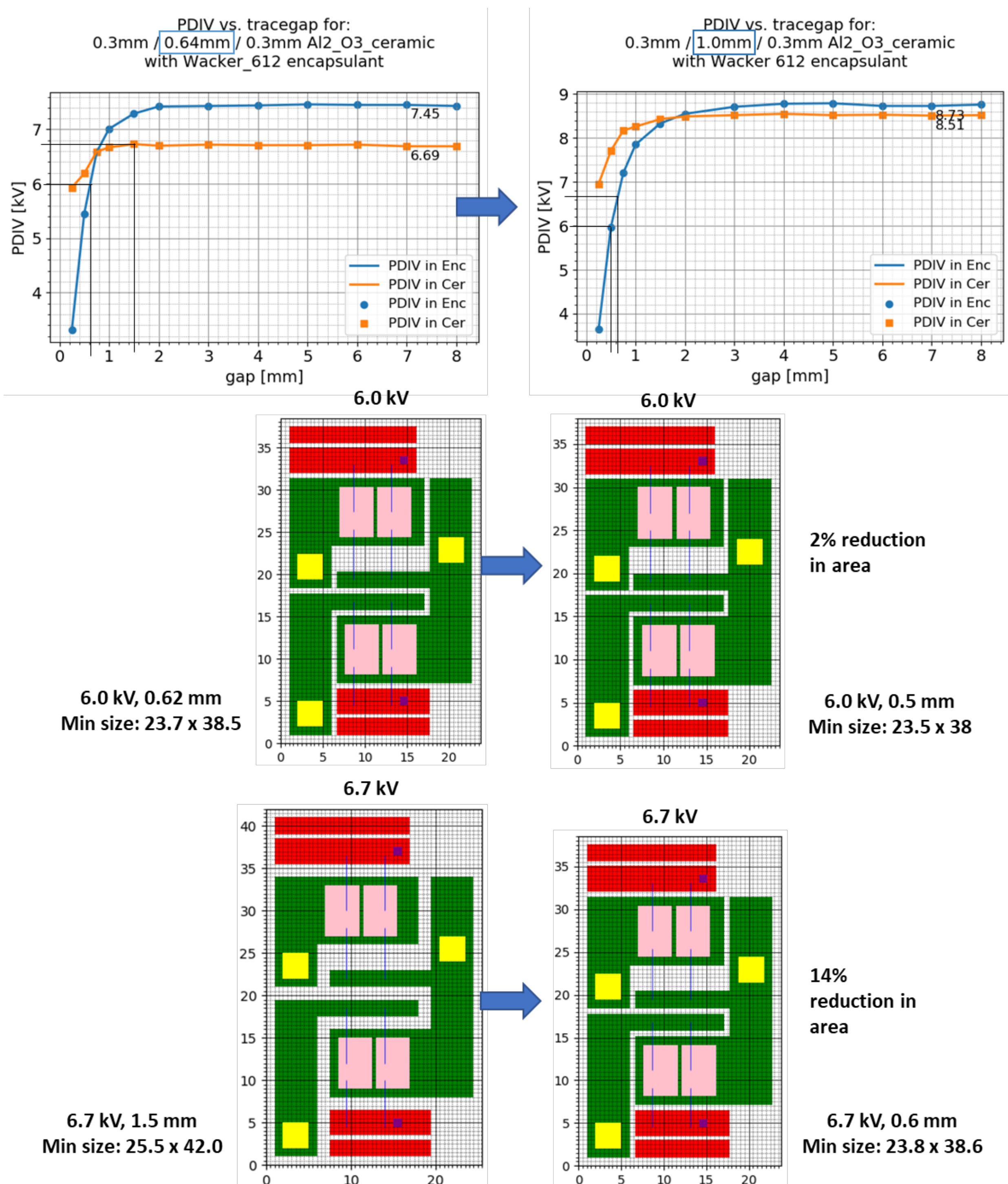


Figure 73. Effect of increasing the ceramic thickness on layouts of the same voltage handling capability.

3.4.6 Summary of implementation tested on other layout designs

The implementation for adjusting the design rules based on the PDIV has been tested for other layout designs as well. Shown here is one such example showing the effect of changing the ceramic thickness (Figure 74). Layouts A and D, B and E, and C and F can be compared because

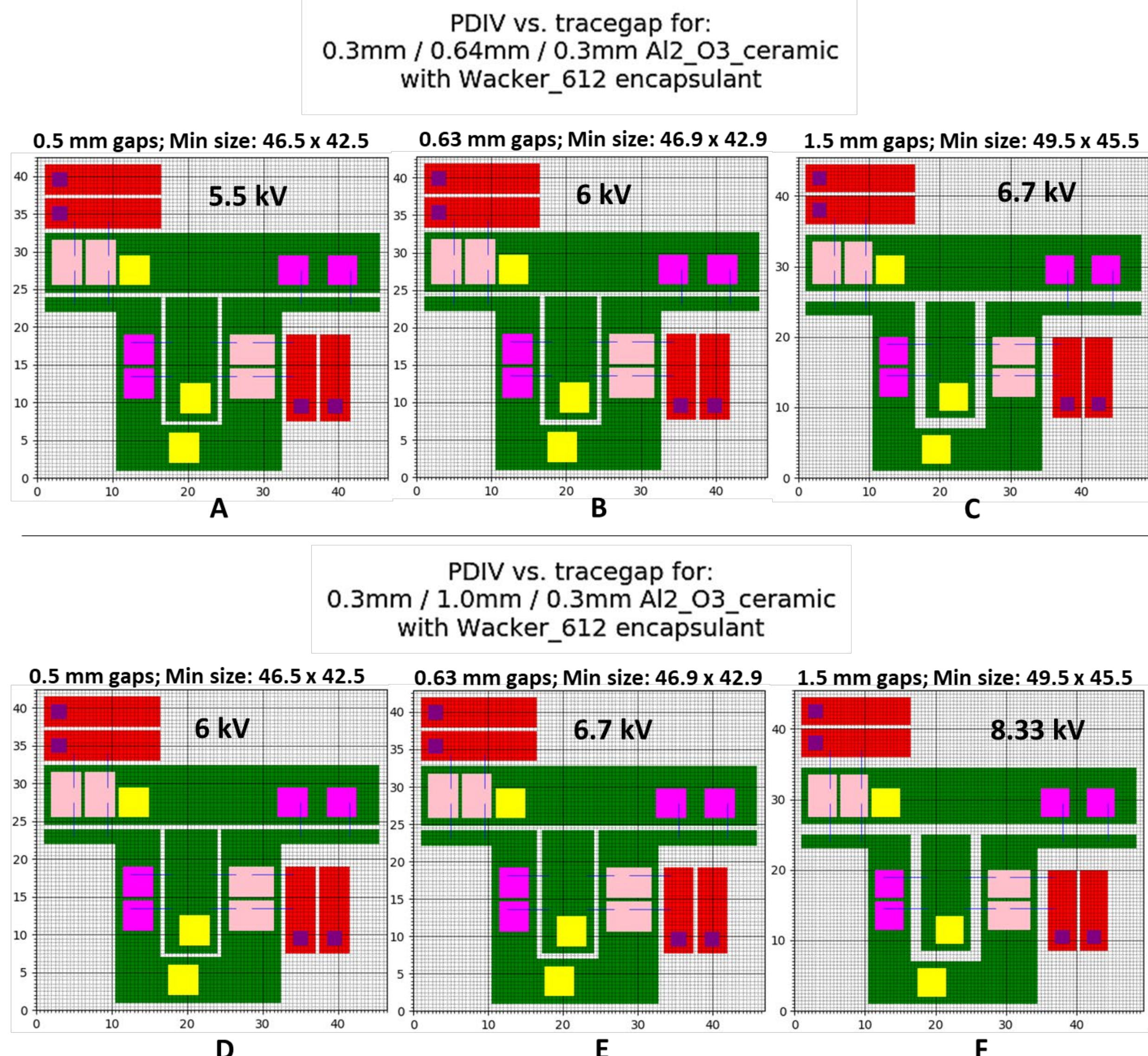


Figure 74. Effect of changing ceramic thickness on another layout design's PD-aware design rules.

their gaps are the same. Increasing the ceramic thickness increases voltage handling capability. Layouts B and D, and C and E can be compared because their voltage levels are the same.

Increasing the ceramic thickness reduces the gap size in this case, allowing a more compact layout option. Note that the layouts are scaled to fit the page, so they can't be visually compared. Based on the improvements made from this implementation, a module designer can now optimize either for the voltage capability or the layout compactness.

3.5 Scalability aspects

3.5.1 Custom k-value

PowerSynth allows the user to enter any custom k-value in the list of parameters in the macro file of the program. A snapshot of the macro file is shown in Figure 75, highlighting the PDIV_k parameter. The default value used is 0.66 based on the calibration done for this work.

```
1  # Input scipts:
2  Layout_script: ./balancing.txt
3  Bondwire_setup: ./balancing_bondwire.txt
4  Layer_stack: ./layer_stack_2.csv
5  Parasitic_model: ./mutual_impact.rsmdl
6  Fig_dir: ./Figs_New
7  Solution_dir: ./Solutions_New
8  Constraint_file: ./layout_1.csv
9  Trace_Ori: ./Trace_ori.txt
10
11 # Layout Generation Set up:
12 # Options -- 0: layout generation, 1:single layout evaluation, 2:layout optimization
13 # Layout Modes -- 0: minimum size, 1:variable size, 2:fixed size, 3:fixed size with fixed locations
14 # Reliability-awareness==0,1,2 #0: no reliability constraints, 1: worst case consideration, 2: average case
15 # if New ==1 constraint file is required to setup if ==0 constraint file will be reloaded
16 # if Plot_Solution==1, all solutions will be plot and saved in the Fig_dir.
17 # if Flexible_Wire==0: horizontal/vertical wire bond is considered, else: flexible connection is considered.
18 # if Default_PD_Datalib== 1: use the default PD library; 0: use the custom library but without filler material.
19 # PDIV_k: 0.66 is the default. The user can specify their own k-value here.
20 # PDIV_ss_tol: when the slope of the PDIV vs tracegap curve reaches below this value, the diminishing returns
   point is determined.
21 Reliability-awareness: 2
22 Default_PD_Datalib: 0
23 PDIV_k: 0.66
24 PDIV_ss_tol: 0.1
25 New: 0
26 Plot_Solution: 1
27 Flexible_Wire: 0
28 Option: 0
29 Layout_Mode: 0
30 Floor_plan: 40,70
31 Num_of_layouts: 20
```

Figure 75. Macro script where the k-value can be updated.

As mentioned in Chapter 2, the ***k***-value is "the proportionality constant or calibration constant that represents the fraction of the local theoretical breakdown voltage at which partial

discharge inception practically occurs." The "local theoretical breakdown voltage" is the voltage at which the E-field in a small location in the material exceeds the prescribed dielectric strength of the bulk material as mentioned in its datasheet. The ***k***-value incorporates practical aspects that can not be simulated such as material defects, manufacturing-related artifacts, excitation profile, and environmental aspects.

If any of the above factors changes significantly, the simulations need to be re-calibrated as done in Chapter 2. This would have to be done at the user end and the adjusted k-value can be entered in the software, keeping the implementation structure the same but allowing flexibility to incorporate another manufacturing line's influence on PDIV estimates. The k-value represents what percent of the breakdown voltage does PD begin. The k-value could depend on multiple factors and experimentally determining all these factors is outside the scope of this work but could be excellent future work. For this work, an experimentally determined k-value for a specific substrate technology and manufacturing process was used to illustrate the process of modeling for PDIV and experimentally validating it with a factor for calibration, then using the model for extrapolating PDIV for similar materials and manufacturing processes, to make design decisions for power modules.

In this work, the encapsulation was processed manually, whereas in industry, it is often a machine that is automated to target the delivery of the gel encapsulant in a way that does not introduce bubbles, something that is hard to control in a manual process. There may be numerous other ways that defects are introduced in a manual process that may affect the PD levels. With every new manufacturing line, it would be wise to recalibrate the k-value. It is not expected to change drastically, and the default values may still be used for comparative analysis of module layouts, but for precision and to determine more accurate PDIV numbers, k-value re-calibration

is advised. The re-calibrated k-value can be entered into the macro file as the PDIV_k parameter, and the program will apply it to all PDIV calculations. In this case, the PD data library will remain the same; only the k-value will change.

3.5.2 Customizable PD data library

For layer stacks, materials, or manufacturing processes that are significantly different from those presented in the previous chapter, a user may employ the modeling approach in the previous chapter to not just find their own k-value, but also define their own custom simulations, define their own experiments to calibrate and validate those simulations, and store the resulting data in a custom data library in PowerSynth. Such custom PDIV libraries, which may be specific to an organization, can be implemented in PowerSynth. A user-defined PD data library can be incorporated in the technology library of PowerSynth's manufacturing design kit. The custom PD data library can be stored in the same location as the default PD data library; its file path can be specified in the settings file (Figure 76), and a flag in the macro file that tells the program whether to look for a custom PD library or use the default library (Figure 77). There is a single settings file for all test cases. This is where file paths to various technology libraries are entered.

Manufacturers and researchers can characterize their novel materials, stack-ups, and

```
1  # Settings and Paths
2  DEFAULT_TECH_LIB_DIR: ./tech_lib
3  LAST_ENTRIES_PATH: ./export_data/app_data/last_entries.p
4  TEMP_DIR: ./export_data/temp
5  CACHED_CHAR_PATH: ./export_data/cached_thermal
6  MATERIAL_LIB_PATH: ./tech_lib/Material/Materials.csv
7  DEFAULT_PD_DATALIB_PATH: ./tech_lib/Material_PDIV_DesignRules/default_PD_datalib.csv
8  CUSTOM_NOFILLER_PD_DATALIB_PATH: ./tech_lib/Material_PDIV_DesignRules/custom_nofiller_PD_datalib.csv
9  CUSTOM_FILLER_PD_DATALIB_PATH: ./tech_lib/Material_PDIV_DesignRules/custom_filler_PD_datalib.csv
10 EXPORT_DATA_PATH: ./export_data
11 GMSH_BIN_PATH: ./gmsh-2.7.0-Windows
12 ELMER_BIN_PATH: ./Elmer_8.2-Release/bin
13 ANSYS_IPY64: C:/Program Files/AnsysEM/AnsysEM18.2/Win64/common/IronPython
14 FASTHENRY_FOLDER: ./FastHenry
15 MANUAL: ./PowerSynth_User_Manual.pdf
```

```
Name
..
custom_filler_PD_datalib.csv
custom_nofiller_PD_datalib.csv
default_PD_datalib.csv
```

Figure 76. settings.py file where the default and custom PD data library file paths are entered.

```
1 # Input scipts:
2 Layout_script: ./balancing.txt
3 Bondwire_setup: ./balancing_bondwire.txt
4 Layer_stack: ./layer_stack_2.csv
5 Parasitic_model: ./mutual_impact.rsmdl
6 Fig_dir: ./Figs_New
7 Solution_dir: ./Solutions_New
8 Constraint_file: ./layout_1.csv
9 Trace_Ori: ./Trace_ori.txt
10
11 # Layout Generation Set up:
12 # Options -- 0: layout generation, 1:single layout evaluation, 2:layout optimization
13 # Layout Modes -- 0: minimum size, 1:variable size, 2:fixed size, 3:fixed size with fixed locations
14 # Reliability-awareness==0,1,2 #0: no reliability constraints, 1: worst case consideration, 2: average case
15 # if New ==1 constraint file is required to setup if ==0 constraint file will be reloaded
16 # if Plot_Solution==1, all solutions will be plot and saved in the Fig_dir.
17 # if Flexible_Wire==0: horizontal/vertical wire bond is considered, else: flexible connection is considered.
18 # if Default_PD_Datalib== 1: use the default PD library; 0: use the custom library but without filler material.
19 # PDIV_k: 0.66 is the default. The user can specify their own k-value here.
20 # PDIV_ss_tol: when the slope of the PDIV vs tracegap curve reaches below this value, the diminishing returns
   point is determined.
21 Reliability-awareness: 2
22 Default_PD_Datalib: 0
23 PDIV_k: 0.66
24 PDIV_ss_tol: 0.1
25 New: 0
26 Plot_Solution: 1
27 Flexible_Wire: 0
28 Option: 0
29 Layout_Mode: 0
30 Floor_plan: 40,70
31 Num_of_layouts: 20
32 Seed: 10
```

Figure 77. Macro file where default PD data library flag can be set.

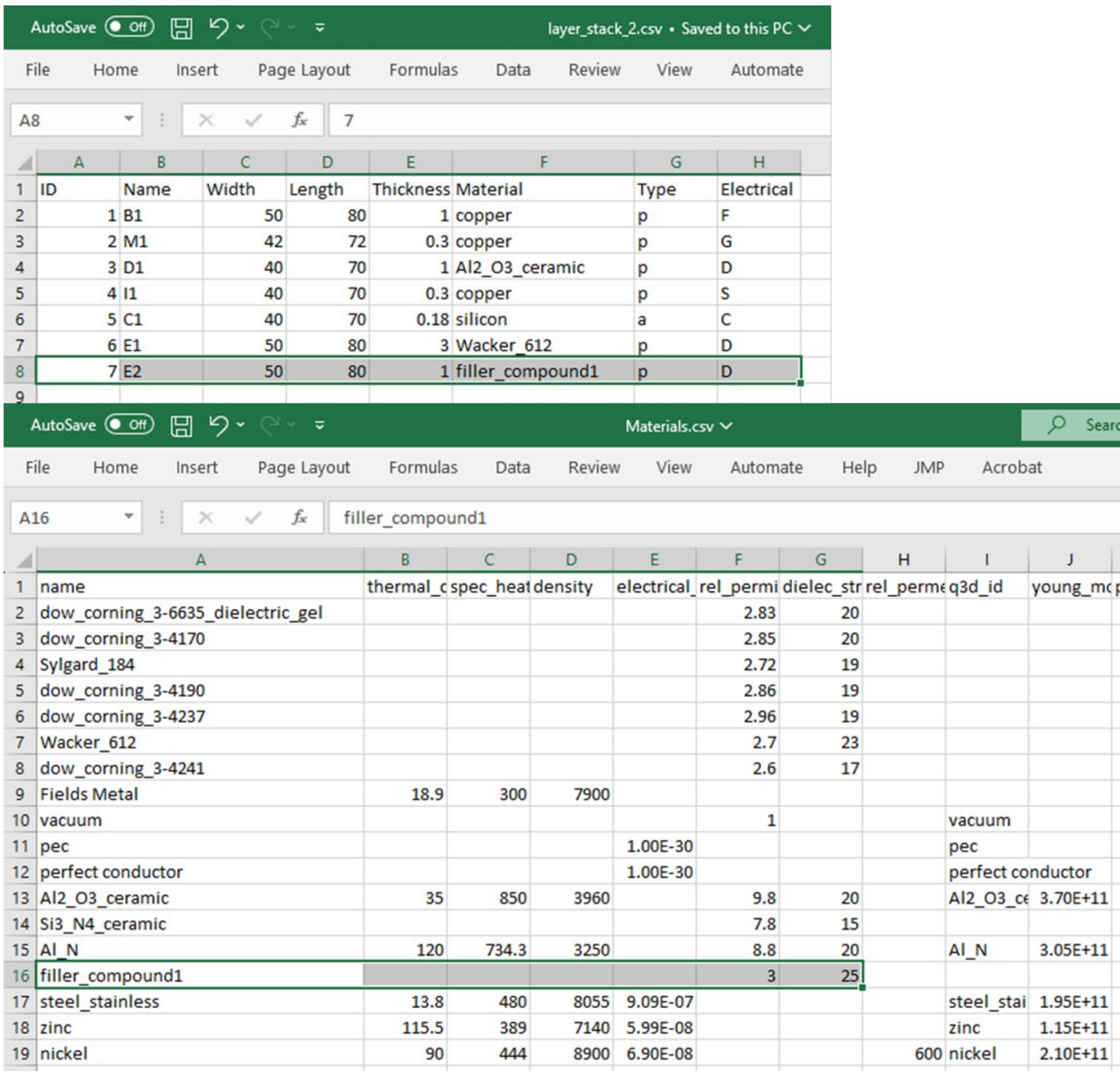
processes using the method described in the previous chapter, and store and use their results in the ever-growing manufacturing design kit library.

3.5.3 Dual-encapsulant system

To be able to incorporate research efforts around field grading by applying coating or multiple encapsulant materials, PowerSynth can now work with dual-encapsulant systems. For this, the user would have to characterize their own filler material if it is novel, otherwise, use a commercial material for a filler encapsulant and an outer encapsulant. In the layer stack, the filler material would be labelled E2 and the outer material would be labelled E1 (Figure 78). Any material mentioned in the layer stack must map exactly to the name of a material in the Materials.csv library, and its electrical properties must be provided. A custom PD library would have to be used that is specifically designed for a dual-encapsulant system, where the first

column is the relative permittivity of the filler material (rpE2), and the second column is the relative permittivity of the outer encapsulant material (rpE1). This is shown in Figure 79.

A template library for the dual encapsulant system has been provided where the filler material and the outer encapsulant material have the same properties. This would have to be



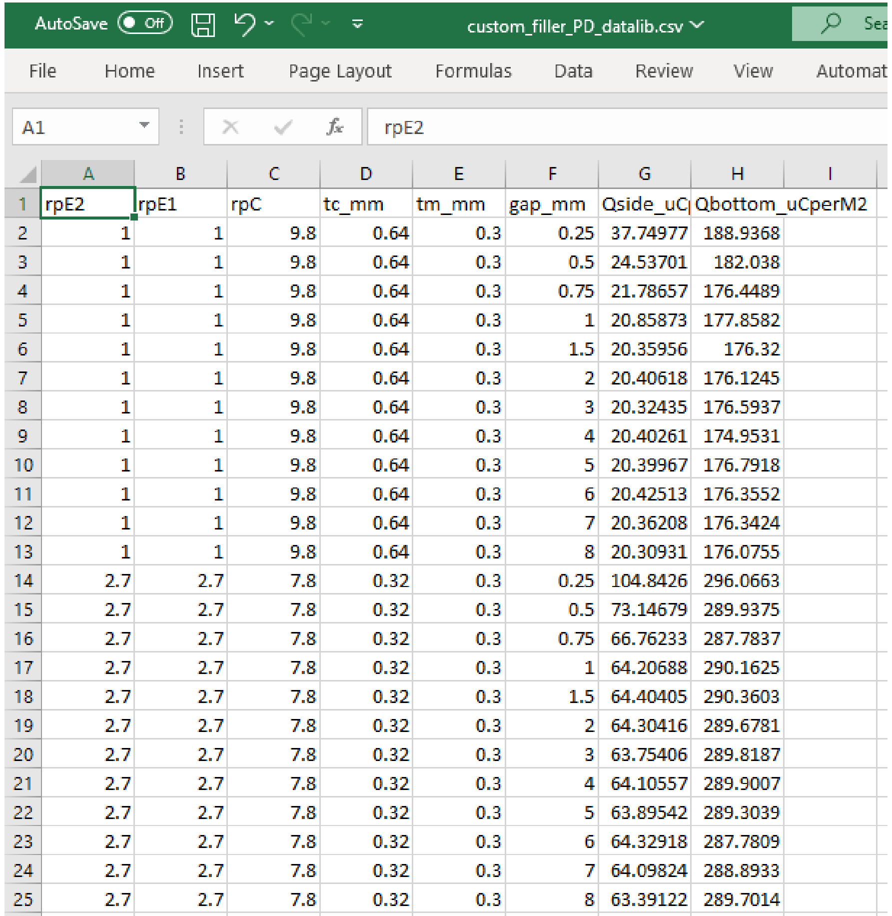
layer_stack_2.csv

	A	B	C	D	E	F	G	H
1	ID	Name	Width	Length	Thickness	Material	Type	Electrical
2	1	B1	50	80	1	copper	p	F
3	2	M1	42	72	0.3	copper	p	G
4	3	D1	40	70	1	Al2_O3_ceramic	p	D
5	4	I1	40	70	0.3	copper	p	S
6	5	C1	40	70	0.18	silicon	a	C
7	6	E1	50	80	3	Wacker_612	p	D
8	7	E2	50	80	1	filler_compound1	p	D

Materials.csv

	A	B	C	D	E	F	G	H	I	J
1	name	thermal_c	spec_heat	density	electrical_	rel_permi	dielec_str	rel_perme	q3d_id	young_mc
2	dow_corning_3-6635_dielectric_gel					2.83	20			
3	dow_corning_3-4170					2.85	20			
4	Sylgard_184					2.72	19			
5	dow_corning_3-4190					2.86	19			
6	dow_corning_3-4237					2.96	19			
7	Wacker_612					2.7	23			
8	dow_corning_3-4241					2.6	17			
9	Fields Metal	18.9	300	7900						
10	vacuum					1			vacuum	
11	pec				1.00E-30				pec	
12	perfect conductor				1.00E-30				perfect conductor	
13	Al2_O3_ceramic	35	850	3960		9.8	20		Al2_O3_ce	3.70E+11
14	Si3_N4_ceramic					7.8	15			
15	Al_N	120	734.3	3250		8.8	20		Al_N	3.05E+11
16	filler_compound1					3	25			
17	steel_stainless	13.8	480	8055	9.09E-07				steel_stai	1.95E+11
18	zinc	115.5	389	7140	5.99E-08				zinc	1.15E+11
19	nickel	90	444	8900	6.90E-08			600	nickel	2.10E+11

Figure 78. Layer stack with filler encapsulant material and the corresponding material properties in the material library.



	rpE2	rpE1	rpC	tc_mm	tm_mm	gap_mm	Qside_uC	Qbottom_uCperM2
2	1	1	9.8	0.64	0.3	0.25	37.74977	188.9368
3	1	1	9.8	0.64	0.3	0.5	24.53701	182.038
4	1	1	9.8	0.64	0.3	0.75	21.78657	176.4489
5	1	1	9.8	0.64	0.3	1	20.85873	177.8582
6	1	1	9.8	0.64	0.3	1.5	20.35956	176.32
7	1	1	9.8	0.64	0.3	2	20.40618	176.1245
8	1	1	9.8	0.64	0.3	3	20.32435	176.5937
9	1	1	9.8	0.64	0.3	4	20.40261	174.9531
10	1	1	9.8	0.64	0.3	5	20.39967	176.7918
11	1	1	9.8	0.64	0.3	6	20.42513	176.3552
12	1	1	9.8	0.64	0.3	7	20.36208	176.3424
13	1	1	9.8	0.64	0.3	8	20.30931	176.0755
14	2.7	2.7	7.8	0.32	0.3	0.25	104.8426	296.0663
15	2.7	2.7	7.8	0.32	0.3	0.5	73.14679	289.9375
16	2.7	2.7	7.8	0.32	0.3	0.75	66.76233	287.7837
17	2.7	2.7	7.8	0.32	0.3	1	64.20688	290.1625
18	2.7	2.7	7.8	0.32	0.3	1.5	64.40405	290.3603
19	2.7	2.7	7.8	0.32	0.3	2	64.30416	289.6781
20	2.7	2.7	7.8	0.32	0.3	3	63.75406	289.8187
21	2.7	2.7	7.8	0.32	0.3	4	64.10557	289.9007
22	2.7	2.7	7.8	0.32	0.3	5	63.89542	289.3039
23	2.7	2.7	7.8	0.32	0.3	6	64.32918	287.7809
24	2.7	2.7	7.8	0.32	0.3	7	64.09824	288.8933
25	2.7	2.7	7.8	0.32	0.3	8	63.39122	289.7014

Figure 79. Custom PD data library with filler encapsulant material.

updated by the user with actual (or simulated) values. The default PD data library flag in the macro file must be set to 0 (Figure 77), and the settings file must have the file path to the custom PD data library with filler material (Figure 76). PowerSynth will fetch this library when it finds a material with "E2" as its name in the layer stack.

3.6 Summary

Earlier when PowerSynth generated a layout, there was no knowledge of what voltage level it could operate at. Now, with the implementation of PDIV-based design rules, one may know not only what voltage a layout can operate at, but also the optimum voltage-spacing combination for a given layer stack and layout. PowerSynth can now generate layouts that are

capable of operating at specific voltage levels and have appropriately adjust design rules for those voltage levels in terms of trace gaps. This addition to the tool makes it more competitive in the power module design marketplace.

Chapter 4. Partial Discharge Mitigation by Trace-Filleting

Charges accumulate at sharp corners and can become the nucleation site for a potentially catastrophic discharge, as described in chapter 1. That is why significant effort goes into avoiding sharp corners in any high voltage application to prevent unwanted discharges. Power module designers fillet all sharp corners as a best practice in industry. Since most modules are custom designed by a human, fillets are highly customized.

As the design process of power module design becomes more automated, it is important to design automation tools that can more comprehensively address reliability issues, including electrical reliability issues such as partial discharge. To design for PD-prevention, trace gaps, materials, and voltage levels are some of the aspects that can be modified, as seen in the previous chapters. One of the other aspects is the implementation of fillets. A contribution of this work is to incorporate the automation of fillets in PowerSynth, the EDA tool for power module design optimization. This chapter covers the need and benefit of filleting power module traces, how this need was addressed by implementing fillets in PowerSynth, including the automation of fillet sizes.

Note that the experimental work done for this chapter pre-dated the work done for Chapter 2, using equipment, fabrication resources, and knowledge available at the time. Some of the drawbacks of the experimental procedures are presented here and were later addressed in the work done for Chapter 2, and additional ideas are discussed in the future works section in the next chapter.

4.1 Adverse effects of sharp corners and the need and benefit of filleting

The theoretical equations for charge density (σ) and electric field (E) as a function of distance from the corner (ρ) at which the E-field is observed, and the opening angle of the corner

(β), as discussed in Chapter 1 and reproduced here, show how E-field and charge density are affected by the shape of the conductor. The sharper the corner angle, the higher the charge density at the corner and the resulting E-field in the insulating material.

$$\sigma(\rho) = \frac{E_{\varphi}(\rho, 0)}{4\pi} \approx -\frac{\alpha_1}{4\beta}\,\rho^{\left(\frac{\pi}{\beta}\right)-1} \tag{1}$$

$$E = \frac{-\alpha\pi}{\beta}\,\rho^{\left(\frac{\pi}{\beta}\right)-1} \tag{2}$$

Adverse electrical effects such as PD and breakdown are more likely at sharper corners for this reason, and thus it is important to address sharp corners. In this work, fillets were used to assess the improvement over sharp corners. Simulations performed agreed with the theory of reduced E-field and charge density at corners when filleted. This section describes some of the simulations done and experiments conducted to confirm this point.

4.1.1 Simulations

4.1.1.1 E-field and charge density

In power modules, it has been observed that electric field concentrates at edges of traces and corners, especially at the triple point of a DBC metallization. The E-field in the layout of an example switching position of a power module was simulated in ANSYS Maxwell 3D (Figure 80). A voltage of 2 kV was applied between the DC+ and output leads (OFF mode). The gate was at the same potential as the output lead. The maximum electric field in this case was 6 kV/mm at the trace corner, and 1 kV/mm at other parts of the trace. A commercial dielectric gel was assigned as the insulating material [101]. It is also seen that chamfering or filleting the corner reduces the E-field in that region to about half. In this case, filleting reduced the maximum field in the gap to almost half of the original value (from 6 kV/mm to 3.1 kV/mm).

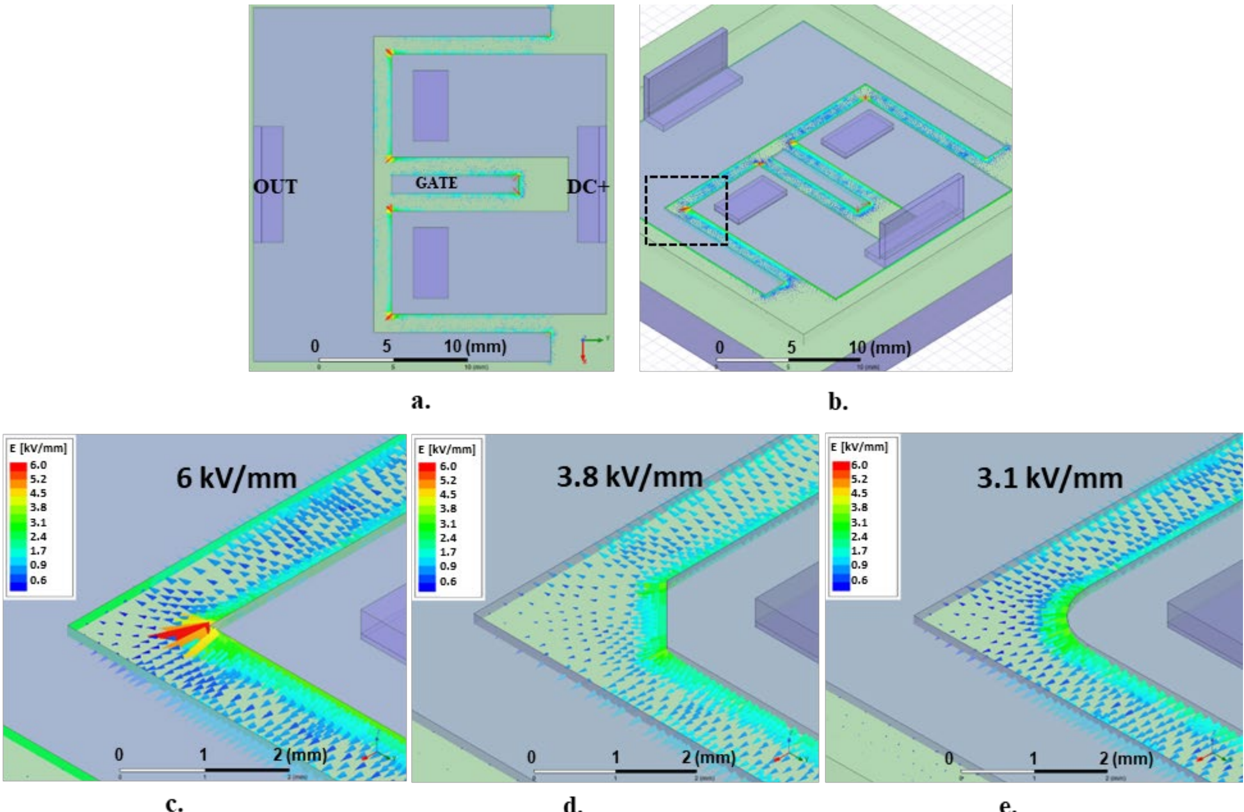


Figure 80. Electric field between drain, source and gate traces for layout showing (a) top view, (b) isometric view, with (c) a 90º outer corner, (d) a chamfered outer corner, and (e) a filleted outer corner.

Charge density also reduces as fillets are applied (Figure 81 and Figure 82). These simulations showed a maximum charge density at the same 90º corner to be 170 pC/mm^2 compared to 10 pC/mm^2 at the straight regions. Filleting lowers charge density at these corners, which then reduces the electric field intensity across the insulator. Figure 81 shows the charge density map (pC/mm^2). There is high charge concentration at the sharp corners of the high voltage trace, and filleting reduces the charge concentration from 170 pC/mm^2 to 140 pC/mm^2.

Charge density is reduced to about 54% of its original value with a 0.5 mm fillet and is further reduced when the fillet radius is 1.0 mm. The general trend is in accordance with theoretical predictions of E-field and charge density in the vicinity of a sharp corner.

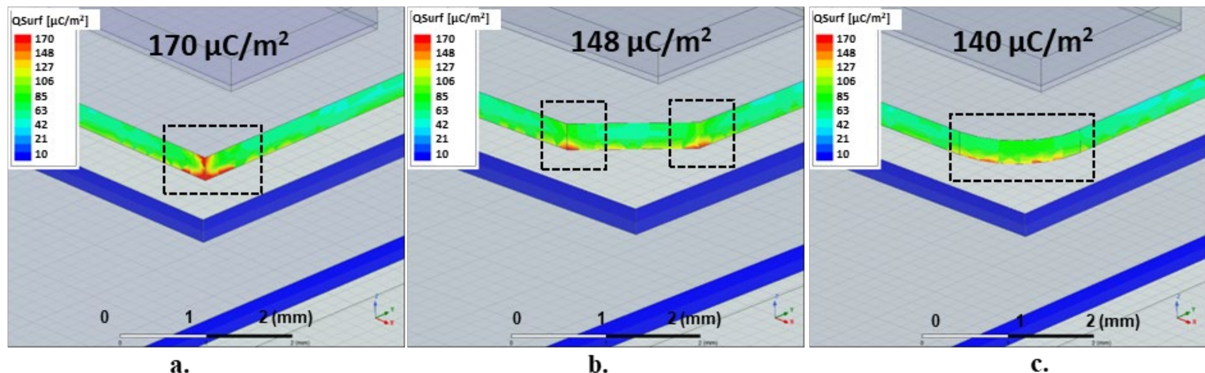


Figure 81. Surface charge density at the edge of a trace for the layout with (a) a 90º outer corner, (b) a chamfered outer corner, and (c) a filleted outer corner.

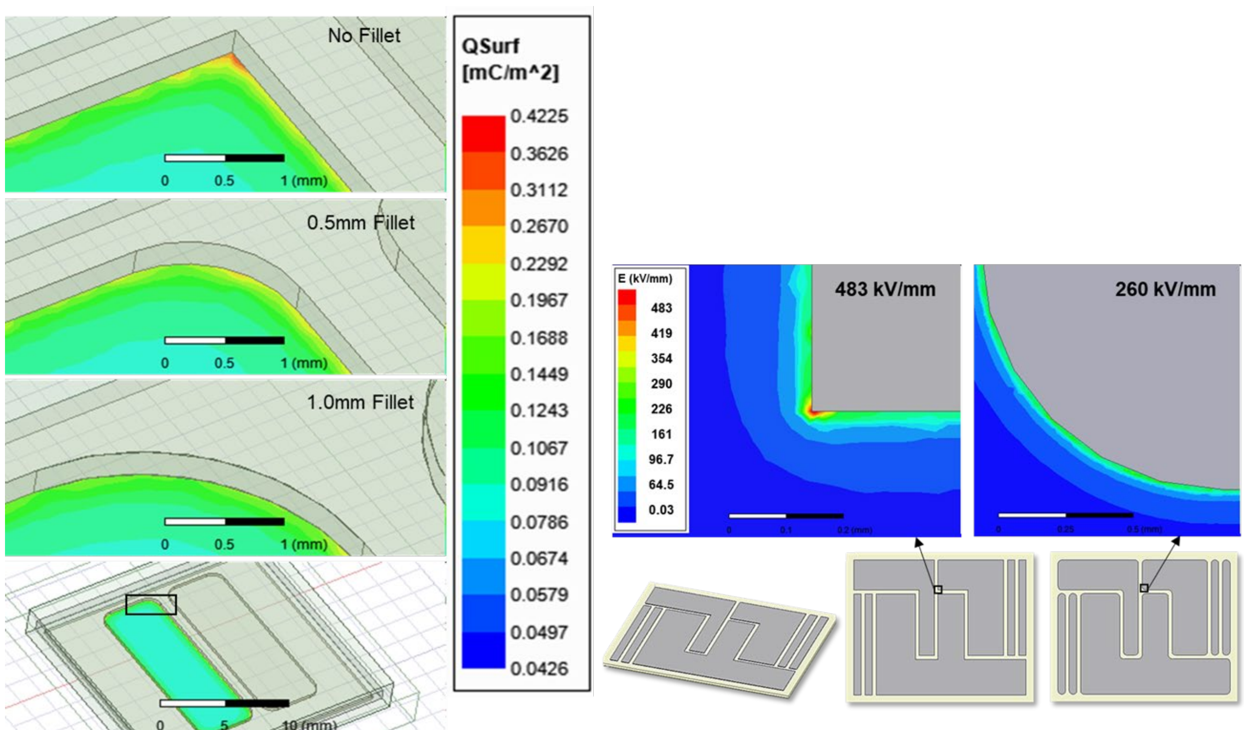


Figure 82. Charge density variation with fillet size.

4.1.1.2 Current density

Another detrimental effect of keeping sharp corners is current crowding. High current density can cause joule heating of the conductor, exacerbating electro-migration and making the placement of nearby devices difficult. Migration issues were found in sintered-silver die attaches

operating at high temperatures [102]-[103]. FEA simulations showed current crowding at corners reduced to less than a third of the original value when fillets were used and current density reduce to two-third its original value (Figure 83).

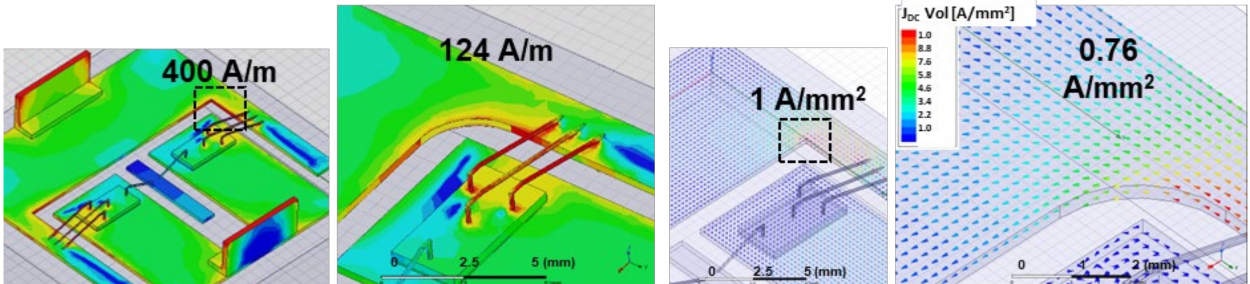


Figure 83. Effect of filleting: AC surface current density reduction (left) and DC current density reduction (right).

4.1.1.3 Trace gap reduction

Figure 84a shows a 3D model of two simple traces with sharp corners and 10kV potential difference between them across a gap of 2.04 mm. For the example shown, when the corners of

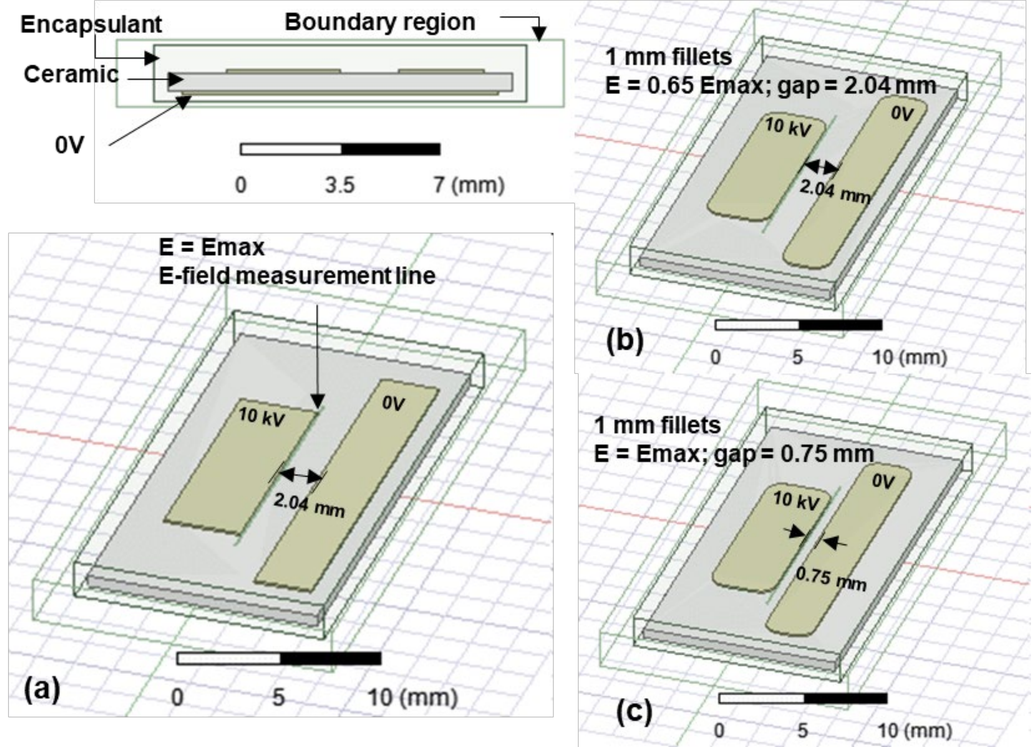


Figure 84. Effect of filleting on E-field and trace-gap.

both traces were filleted 1 mm (Figure 84b), the E-field near the triple point reduced by 65%. This means the trace gap could be reduced to 0.75mm (Figure 84c) before the E-field would reach the value it had for the sharp cornered case. Thus, filleting can save space and make the module safer for high voltage operations.

4.1.1.4 Mechanical Stress

Fillets also have a mechanical advantage (Figure 85 and Figure 86). Delamination often happens at sharp corners due to coefficient of thermal expansion mismatch between metal and ceramic parts due to thermal loading. Thermo-mechanical stress simulations of a patterned DBC substrate were performed in Ansys Workbench and it confirmed that stress was concentrated at sharp corners. Filleting those corners distributed the stress more evenly and reduced the stress at the corners by 18%. Figure 85 lists the parameters for the simulations. Figure 86 shows the geometry used, the thermal map, and the resulting stress distribution. The maximum stress was at the sharp corner, and it was 301 MPa. The simulations were repeated for the filleted case, and the maximum stress reduced to 247 MPa (Figure 87), an 18% reduction.

Steady state thermal simulation	**Structural simulation**
Ambient temperature = 22 C	Ambient temperature = 22 C
Parameters: Internal heat generation of top side traces = 2×10^9 W/m^3 Convective heat transfer coefficient of back side copper = 1000 W/m^{2}C	**Parameters:** Body temperature map
Solution: Body temperature map	**Solution:** Equivalent stress map

Figure 85. Parameters for the thermo mechanical stress simulation in ANSYS Workbench.

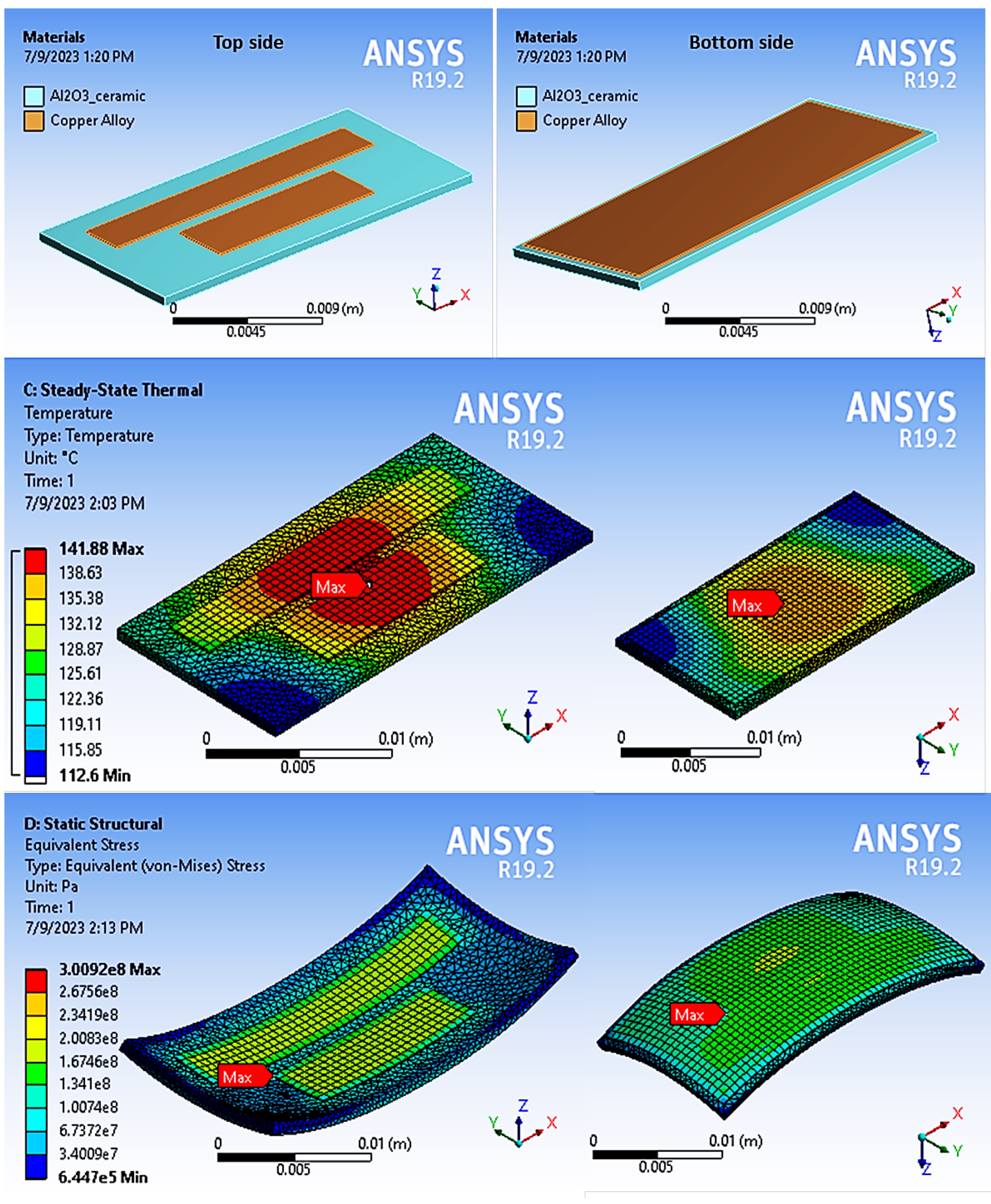


Figure 86. Thermo-mechanical stress simulations for sharp cornered traces on a DBC: geometry (top), thermal map (middle), and stress distribution (bottom).

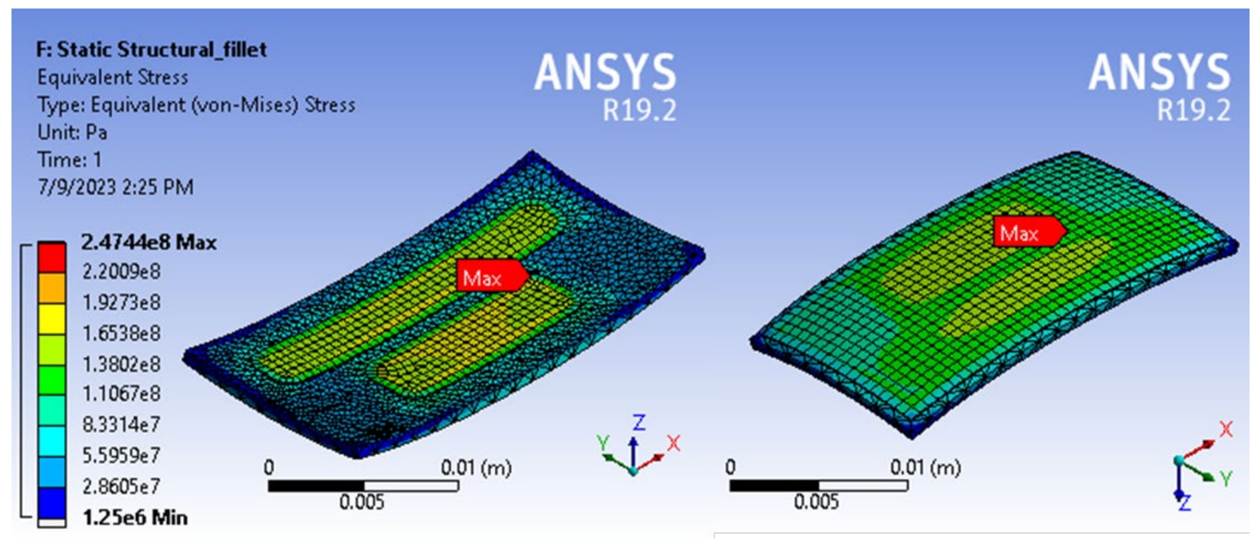


Figure 87. Thermo-mechanical stress distribution for filleted traces on a DBC.

4.1.2 Experiments

4.1.2.1 Breakdown voltage experiments on FR4 samples

To get a baseline of the expected improvement in the breakdown voltage when converting a sharp corner to a fillet, test coupons were designed such that a square would represent the worst-case scenario, while a circle would be the extent to which the square trace can be filleted, i.e. the best-case scenario. Similar sets were created for trace gaps ranging from 0.25 mm to 1.25 mm. These were milled out using a CNC machine with a minimum tool tip size of 127 µm (5.0 mil). A single-sided copper-clad FR4 substrate was used to make the test structures. An example set of test coupons after milling is shown in Figure 88.

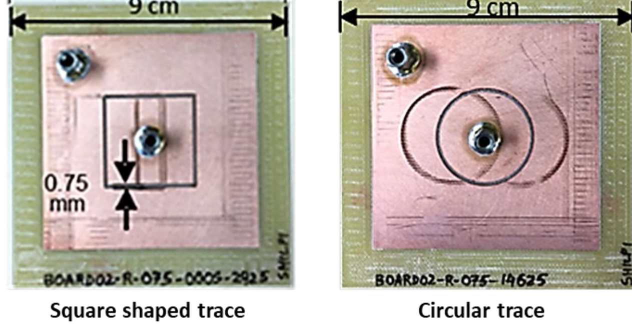


Figure 88. A square trace and a cuircular trace after milling.

The size of the test coupons was intentionally kept large to ensure the high potential terminals were far apart, significantly far compared to the trace-gap. Terminals were then soldered on using solder paste. A hi-pot tester (Valhalla Scientific's 5880A Dielectric Analyzer) capable of supplying up to 5 kVAC was used to supply high voltage AC (60 Hz) to the test structures. The test setup is shown in Figure 89. A 15 kVDC cable was used to connect the hi-pot terminals and the test coupon terminals.

The hi-pot was operated under the 'Automatic AC Dielectric Strength Function' setting with the following operating criteria:

- Voltage limit: variable depending on the test (typically between 1000 V and 2500 V)
- Voltage ramp rate: 10 V/s
- Current limit: 10 μA
- Minimum current 0.0 mA
- Dwell time: 10 seconds

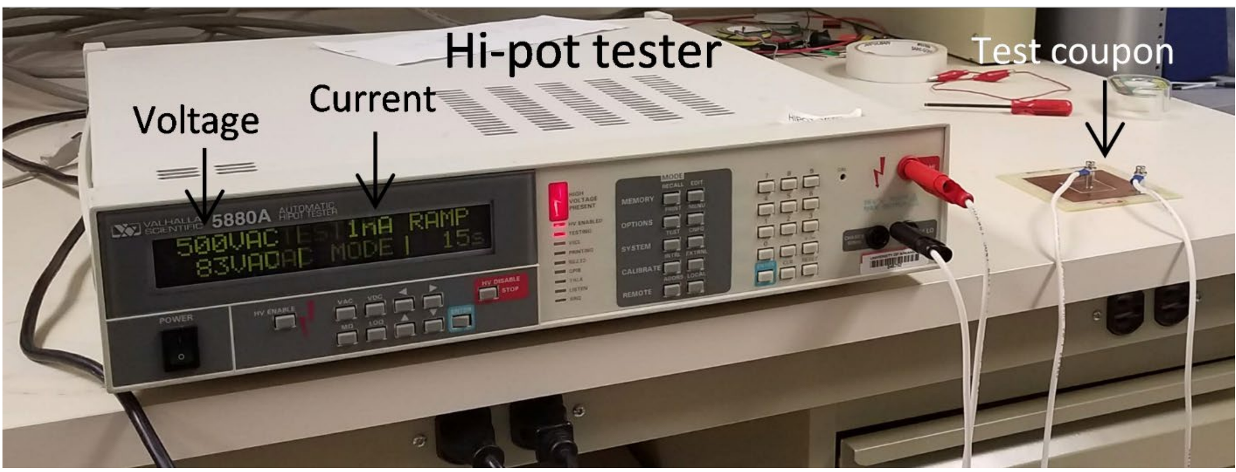


Figure 89. Test setup for AC voltage breakdown tests.

- Operating frequency: 60 Hz
- Current sense: TOTAL (as opposed to real or apparent)

The voltage being supplied, the leakage current through the gap, and the time remaining of the test could be read off the hi-pot's display. Leakage current was plotted against the supplied voltage for each set of test coupons (both square and circle) and is shown in Figure 90 to Figure 93. There were five sets differentiated by trace spacing: 1.25 mm, 1.00 mm, 0.75 mm, 0.50 mm, and 0.25 mm.

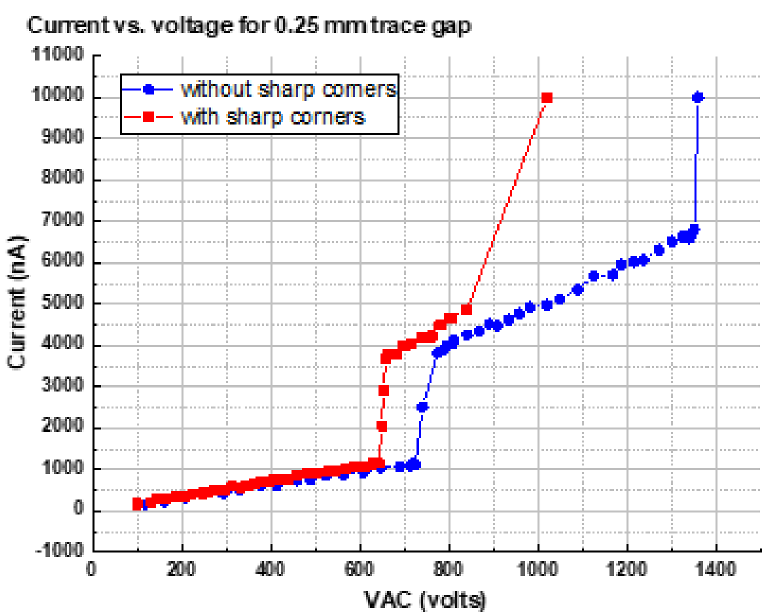


Figure 90. Current vs. voltage for 0.25 mm trace gap samples.

Note that the sudden rise of current from 1 μA to 4 μA occurred during all tests, and the authors attribute this to a likely change in the current sensing circuit within the hi-pot due to a change in the range of current being measured. The sudden rise was also accompanied by an audible click within the instrument.

The more interesting data points are toward the higher end of the voltage range, where the sample being tested approaches breakdown in air. Since the current limit was set to 10 μA, the hi-pot test was terminated either when 10 μA was reached or when an arc was detected (default

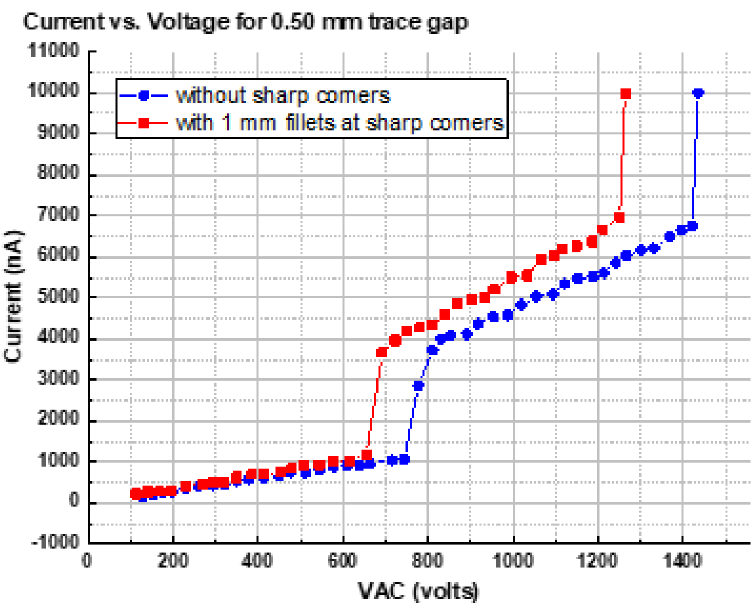


Figure 91. Current vs. voltage for 0.50 mm trace gap samples.

safety setting to prevent catastrophic damage to the test object). It can be observed that the circular trace performed better than the square trace for each set of test cases and performed significantly better than the square for most of the cases. The differences are quantified in Table

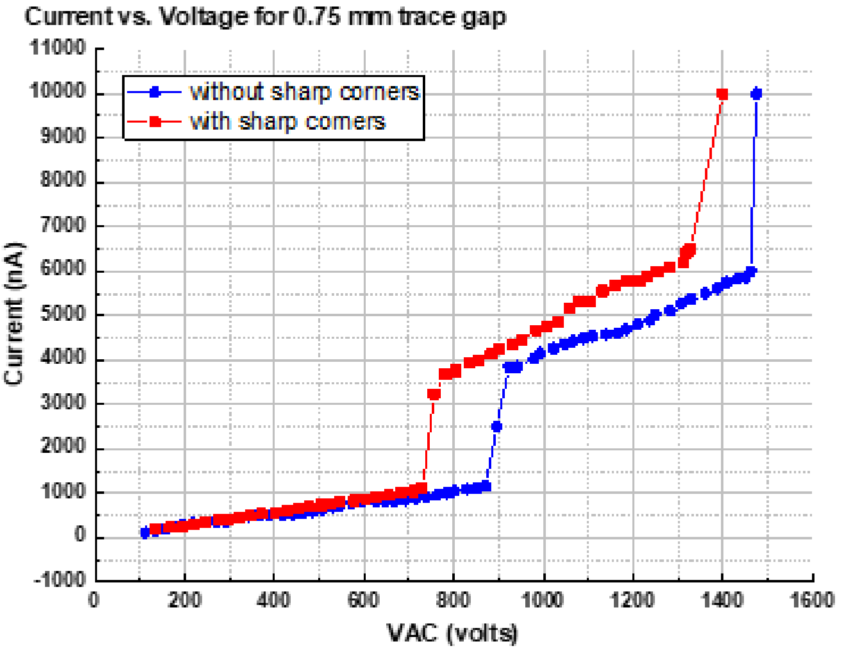


Figure 92. Current vs. voltage for 0.75 mm trace gap samples.

22. Going from a sharp-cornered trace to a maximum filleted trace shows a 14 to 33% increase in the breakdown voltage. For an application, if PD is the critical condition for avoiding higher voltages, filleting might allow operation at 14% higher voltage levels, adding to the safety margin, thus increasing reliability in terms of arc prevention.

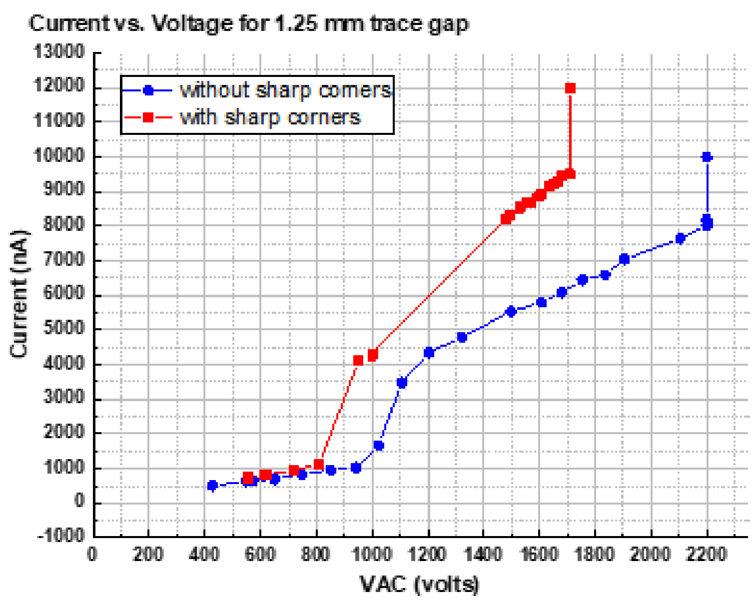


Figure 93. Current vs. voltage for 1.25 mm trace gap samples.

Table 22. Summary of Breakdown Voltage and Leakage Current Results

Voltage levels (V)		Test coupon spacing				
		0.25 mm	0.50 mm	0.75 mm*	1.00 mm	1.25 mm
Arc or 10 µA	S	**1021**	**1263**	**1400**	**1465**	**1712**
	C	**1360**	**1435**	**1475**	**1757**	**2200**
	%	+33	+14	+5	+20	+29
5 µA	S	850	910	1050	1045	1080
	C	1030	1040	1250	1070	1380
	%	+21	+14	+19	+2	+27

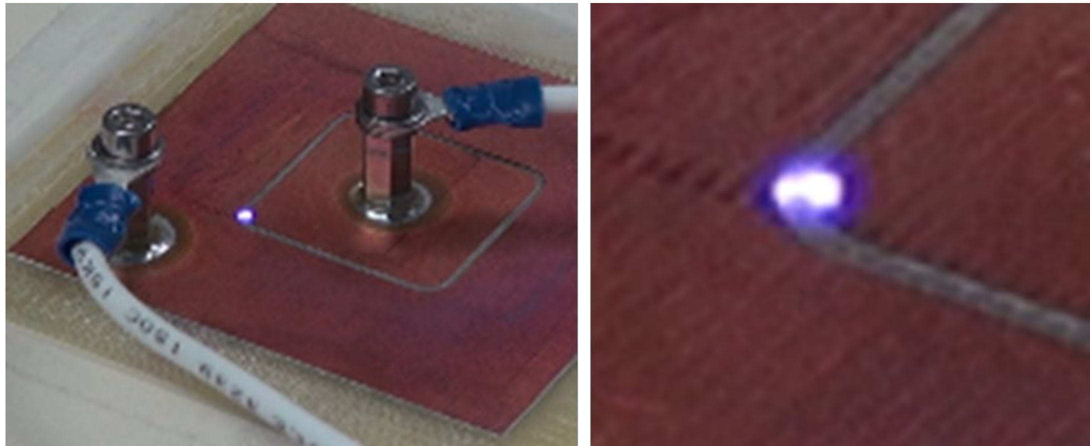


Figure 94. Breakdown at the corner.

Note that there is minor difference between the breakdown voltages of the square and circular test coupons for the 0.75 mm spacing case. This is because the sharp cornered trace on the original test coupon was damaged in the machining process and had to be replaced by a test coupon that was square but filleted 1 mm on all corners. Thus, the breakdown strength was affected. For a different 0.75 mm set, fillet sizes were increased from 0 mm to 2 mm to 3 mm. 1293 V was the breakdown voltage of the sharp trace, 1495 V for the trace with 2 mm fillets, and 1539 V for the 3.0 mm fillet. The trend was as expected. Sparks for sharp cornered traces occurred first at the sharp corner. An example is shown in Figure 94. A channel was formed between the traces during the breakdown.

From experiments, an average of 20% increase in the breakdown voltage was observed when converting a square shaped trace into a circular-shaped trace with its diameter the same as the side length of the square. The smallest trace gap case showed the maximum impact (33%) in terms of increase in breakdown voltage, going from 1021 V for the square trace to 1360 V for the circular trace. For the case of incremental fillet sizes, there is an upward trend going from 1293 V for a sharp-cornered trace, to 1495 V for a 2.0 mm fillet and 1539 V for a 3.0 mm fillet,

suggesting increased improvement for larger fillets, but a diminishing return eventually.

4.1.2.2 PD inception voltage experiments on DBC samples

The FR4 samples did not have a back-side metal. Therefore, the potential difference was only across the lateral trace gap. Secondly, the copper on FR4 was patterned by milling, a process that introduced machining debris into the trace gap. The samples were cleaned before testing. However, it is still better to use a process that is inherently cleaner. Also, the process of milling can introduce metallic asperities on the trace edges, while a chemical patterning process would likely not. To introduce back side metal as it is a more realistic scenario, and to have a cleaner fabrication process, DBC samples were etched out using a chemical wet-etch process as described in Chapter 2. Square and circle patterns were etched out like the ones on FR4 to test the effect of sharp corners and the lack thereof on PD inception voltage.

Surface roughness was measured using a Keyence VK-X260K microscope (Figure 95). The vertical face of the copper trace was measured. The mechanically milled out copper traces had an average surface roughness of 1.78 μm, while the chemically etched out copper traces had a surface roughness of 1.05 μm. The chemical etch process had a smoother surface. In HV applications, all surfaces are polished to be smooth to avoid charge accumulation. Chemical etching is clearly the better option compared to mechanical milling. Even though for trace gaps as small as 0.5 mm a one micron roughness is orders of magnitude smaller than the trace gap and is therefore not extremely significant, if manufacturing methods someday allow extremely small trace gaps, roughness will become a more significant consideration in power module fabrication.

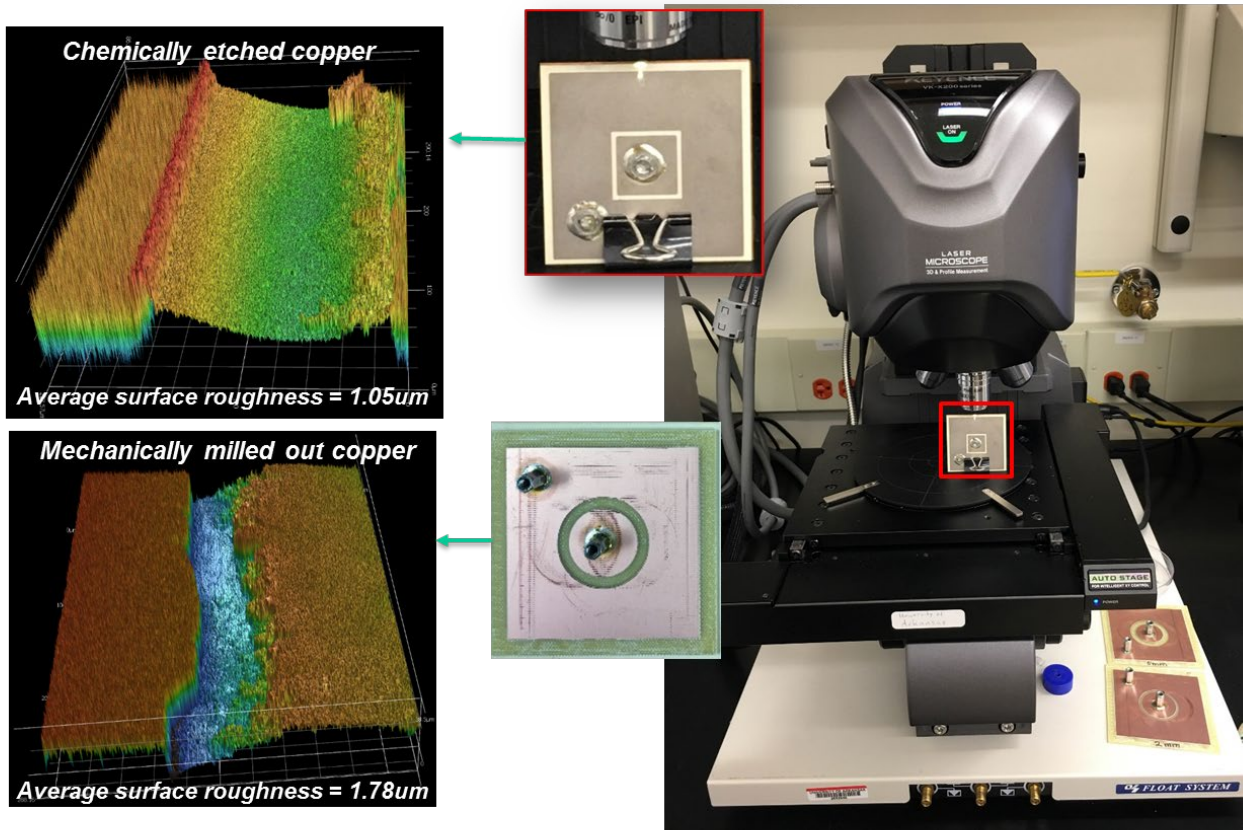


Figure 95. Surface roughness measurement of milled out copper vs. chemically etched copper.

Twelve 5/25/5 mil Ni-plated alumina DBC samples were fabricated, with six of them having square trace gaps (90 degree corners) and six with circular trace gaps (i.e. no sharp corners). The DBCs were patterned using the Chemcut, like the procedure described in Chapter 2. Three of the six in each set had a trace gap of 1 mm, while the other had a gap of 2 mm. Two of the three were encapsulated in a silicone gel. The patterned DBC is shown in Figure 96.

Some of the samples had bubbles in the encapsulant. Though they were tested, they were disregarded from the analysis. All samples were tested with an MPS 60 kV PD Tester owned and operated by Wolfspeed according to IEC 61287 and EN 50178 standards for AC testing.

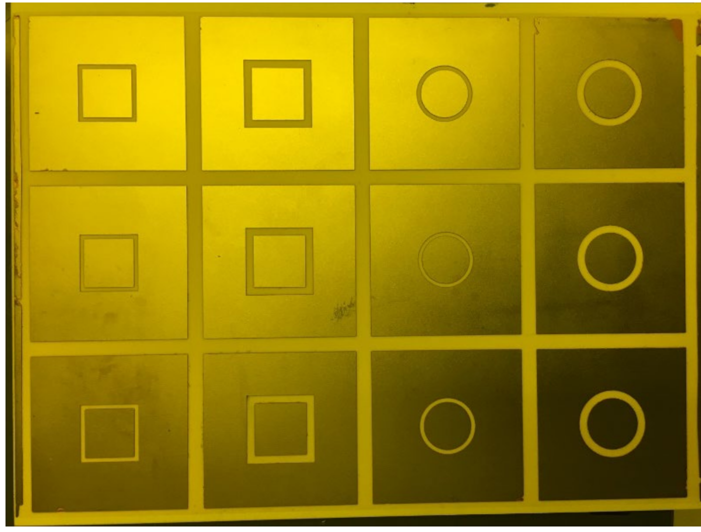


Figure 96. DBC samples for etching and PDIV testing.

The test voltage profile is shown in Figure 97. Voltage was increased up to the test voltage of 20 kV and allowed to dwell for 10 seconds before PD was measured. In most cases, breakdown happened before the system reached 20 kV. The voltage over time and discharges over time were recorded. The voltage at which charges reached a level of 10 pC was recorded as the PDIV. The breakdown voltage was also recorded.

The hysteresis loop for PD inception voltage and PD extinction voltage is shown in Figure 98. Once PD inception voltage is reached, to extinguish PD, the voltage must not just be brought below the PD inception voltage, but further below the extinction voltage which is lower

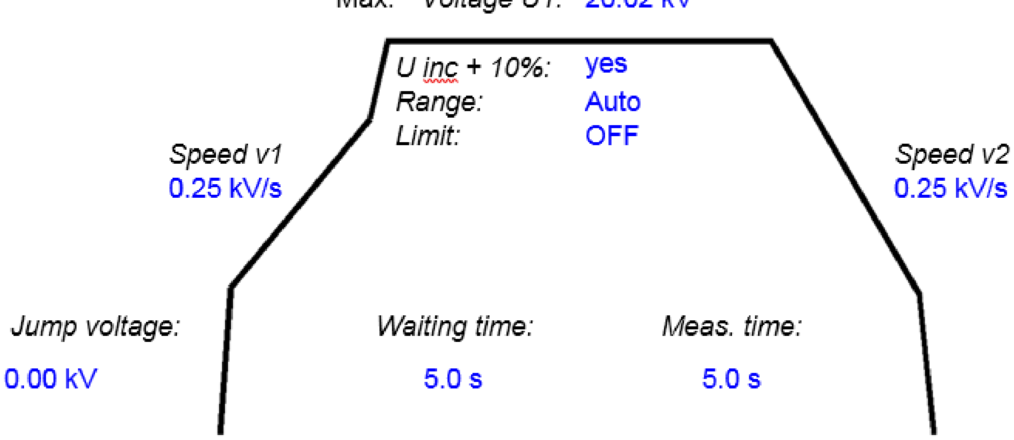


Figure 97. AC voltage test profile for PD testing with Wolfspeed’s MPS 60 kV PD tester .

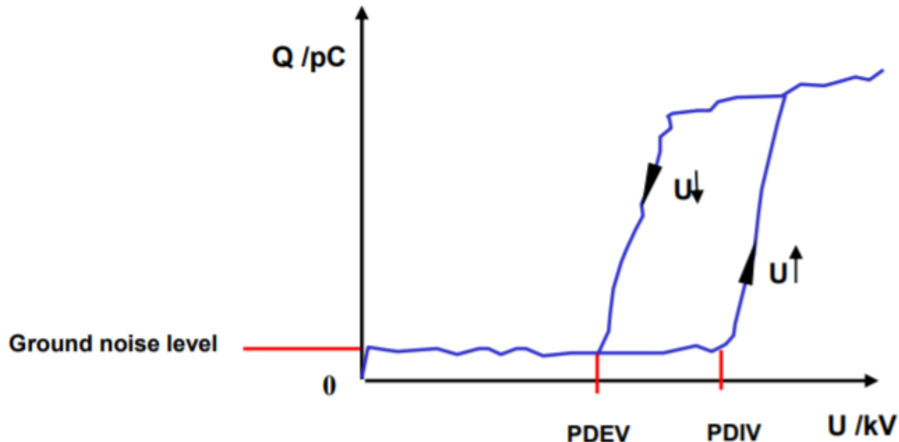
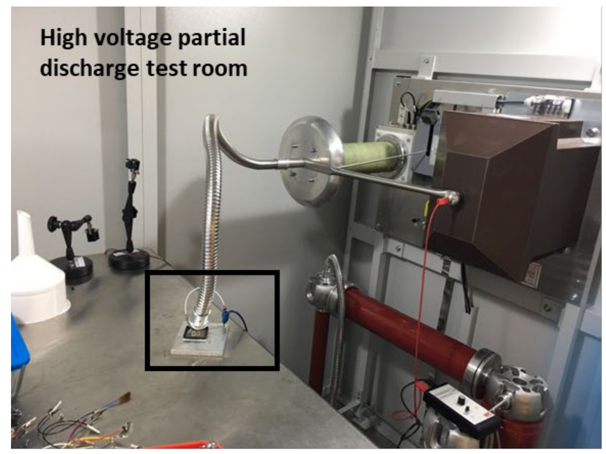


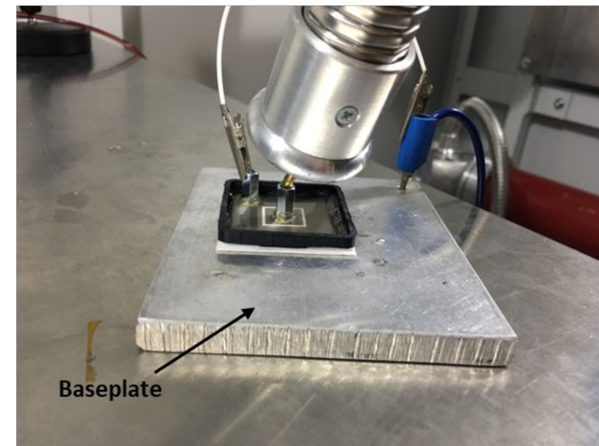
Figure 98. PD inception and extinction voltage hysteresis loop depiction.

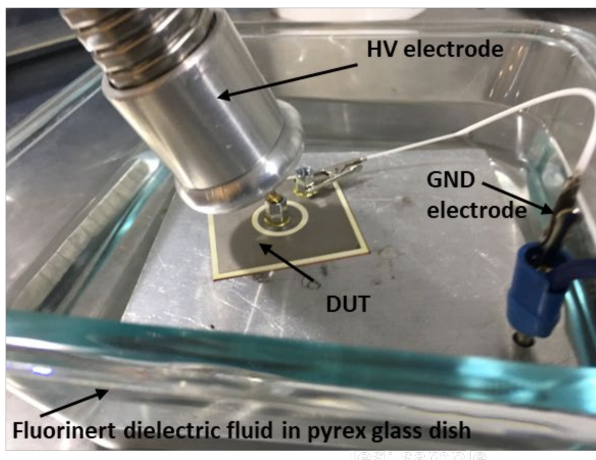
than the inception voltage as shown in the curve.

The test equipment with some of the samples connected is shown in Figure 99 [104]. Circular and square trace samples that were encapsulated in gel were tested in air. Circular and square trace samples that were not encapsulated in gel were submerged in fluorinert dielectric fluid. The entire test was conducted inside a walk-in test chamber that would be locked and isolated for the high voltage test.

The PDIV results for the various samples (except the ones with bubbles in the trace gap) were tabulated as shown in Figure 101. And the raw data of voltage over time and charge over time was plotted for each sample as shown in Figure 100 (for the 1mm trace gaps) and Figure 102 (for the 2mm trace gaps). The graphs are shown with variable scale to emphasize the magnitude of PD close to the breakdown voltage. PDIV was determined as the voltage at which the PD level crossed the threshold of 10 pC. In both cases, the important thing to note is that PD







Charge
calibrator

Figure 99. Test samples connected to the MPS 60 kV PD tester at Wolfspeed.

inception voltage was lower for the samples that had sharp corners compared to the samples that didn't have intentionally sharp corners. For a couple of cases, the 2 mm trace gaps had worse PDIV than the 1 mm trace gaps. This can be attributed to the fact that the samples were not encapsulated and could thus be contaminated in the trace gap region before testing. PD is also stochastic. This is why multiple identical samples ought to be built and tested to get an average that is more reliable. This is why the later tests that were done for the analysis in Chapter 2 had ten identical samples off which an average and data spread was determined. Nevertheless, in this sample set, there is consistency in the improvement shown going from a non-filleted trace to a filleted one. There was between 5% to 21% improvement when traces were filleted.

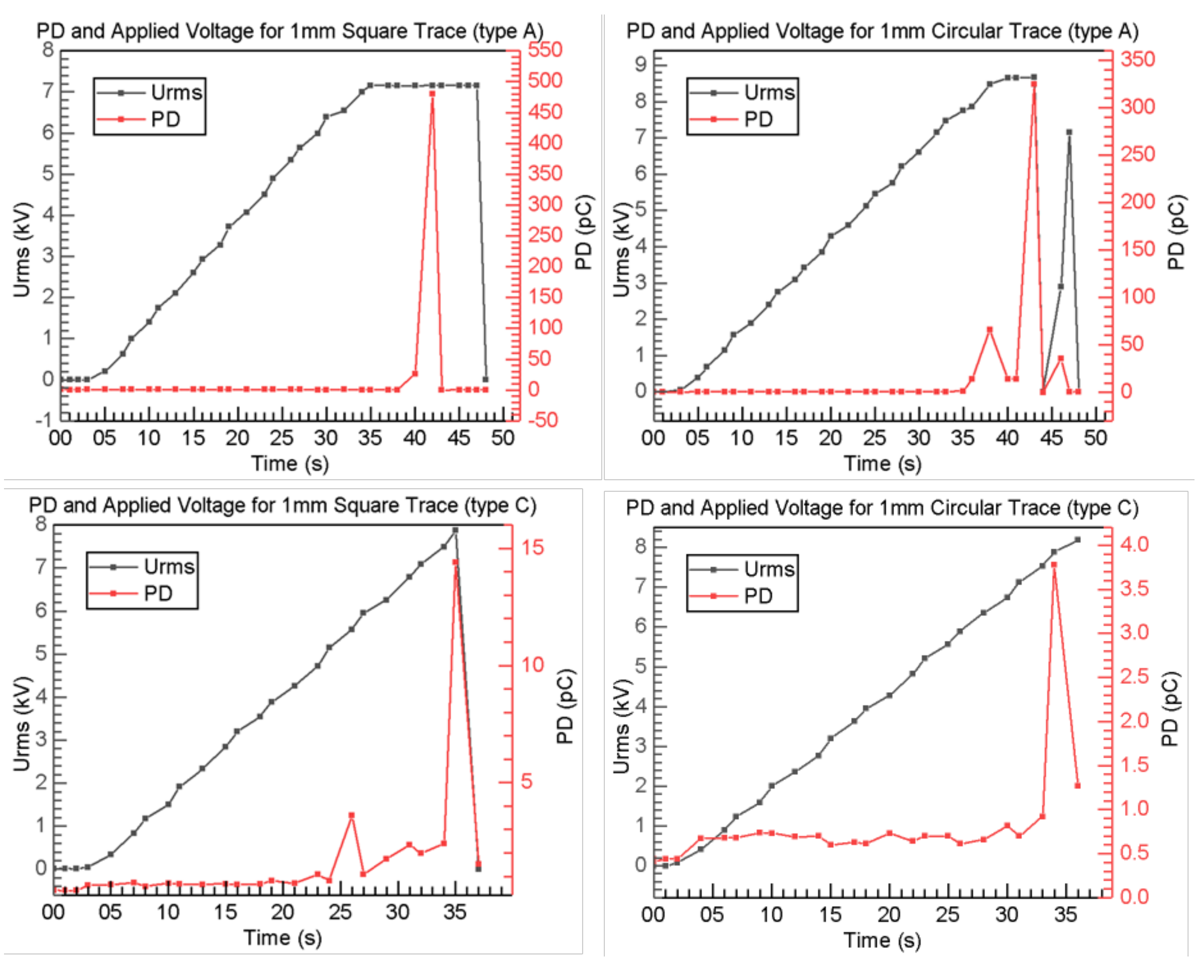
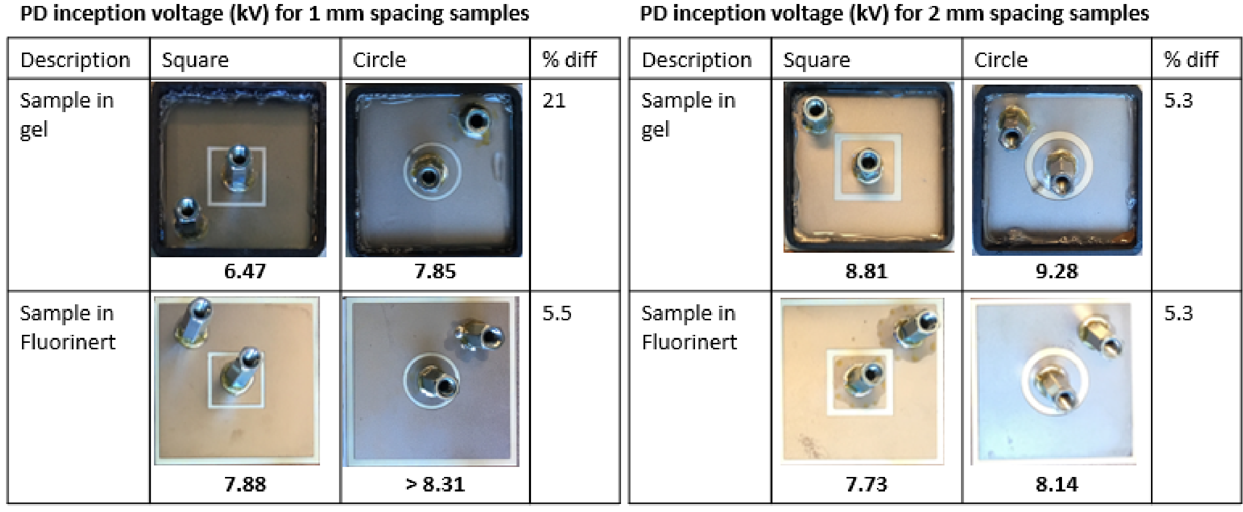


Figure 100. Voltage and charge plotted over time for the square trace samples (left) and the circular trace samples (right) for the 1 mm trace gap sample set.



PD inception voltage (kV) for 1 mm spacing samples

Description	Square	Circle	% diff
Sample in gel	6.47	7.85	21
Sample in Fluorinert	7.88	> 8.31	5.5

PD inception voltage (kV) for 2 mm spacing samples

Description	Square	Circle	% diff
Sample in gel	8.81	9.28	5.3
Sample in Fluorinert	7.73	8.14	5.3

Figure 101. Comparison of square vs. circular traces in terms of PDIV.

The raw data shows how after a certain PD level, the sample undergoes breakdown, as shown by the sudden peaks in the PD curves and subsequent drop in the voltage. PDIV was recorded for all the samples and while the voltage kept increasing, PD kept increasing until there was breakdown. This happened for almost all the samples well below the rated test voltage of 20 kV.

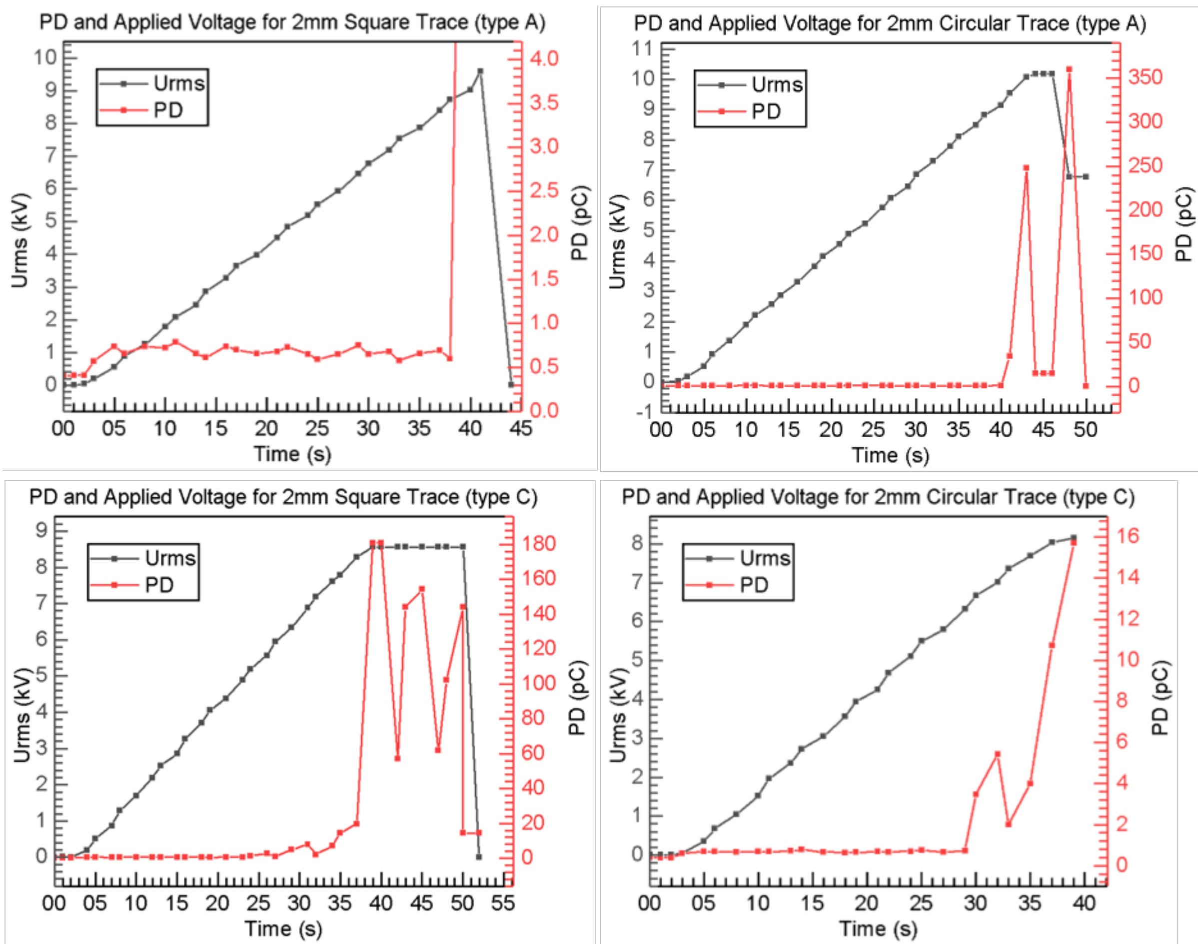


Figure 102. Voltage and charge plotted over time for the square trace samples (left) and the circular trace samples (right) for the 2 mm trace gap sample set.

These tests, though with minimal samples, showed a strong trend of PDIV improvement for the samples that had a circular trace, suggesting that fillets help alleviate PD. The future work section in the next chapter describes ideas for further experimentation to help determine trends related to fillets and their sizes. For implementing fillets in an EDA tool like PowerSynth, the

extent of these experiments was sufficient to show that there is indeed a benefit to filleting traces intentionally.

4.2 Natural and designed fillets

One way of mitigating PD is to use high quality insulating materials. Another way is to alter the geometry of the electrodes where PD occurrence is predicted. The simulations and experiments presented in the previous section showed the effect of trace corner geometries for two main cases: one for a sharp cornered trace with no intentional fillet, and another for a circular trace with no intentional sharp corner. This section discusses naturally occurring vs. intentionally designed fillets.

After performing the tests mentioned in the previous section, some of the square trace samples were observed under a microscope to determine how sharp the corners really are. A wet-etch process etches the copper at the corners more than the copper at the edges, creating a natural

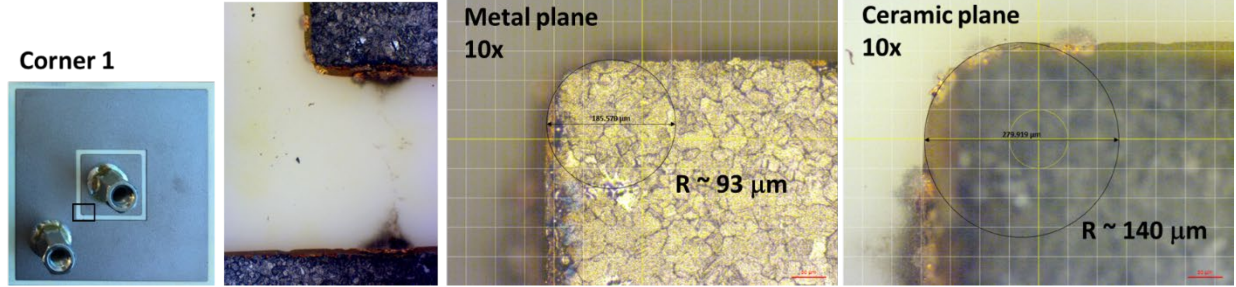


Figure 103. Natural fillet radius measurement using microscope.

fillet as shown in Figure 103. A microscope was used to measure the radius of the fillet at the metal plane and at the ceramic plane. The etching process creates a feather at the edges of the metal-ceramic interface (the triple point) due to the isotropic nature of the etching process. That is why the fillet radius at the metal layer is different from the fillet radius at the ceramic layer. In this example, the fillet radius is 93 microns at the metal layer, and 140 microns at the ceramic

layer. The expected feather size (how much the metal extends on the ceramic interface layer compared to at the top face of the metal layer due to the wet-etch profile) is provided by DBC manufacturing companies [105]. The feather size is dependent on the metal thickness.

The microscope image in Figure 103 also shows the corner where the PD eventually led to breakdown. There is a visible track on the surface of the ceramic in the trace gap connecting the high voltage trace to the low voltage trace and this point was close to the corner. The other samples did not necessarily register a visible track close to the corner, most likely because this too is a stochastic process. Determining the location of PD and breakdown could be a good investigation for future work and is outside the scope of this discussion. Figure 104 shows the natural fillet sizes for the other three corners of the test coupon shown in Figure 103.

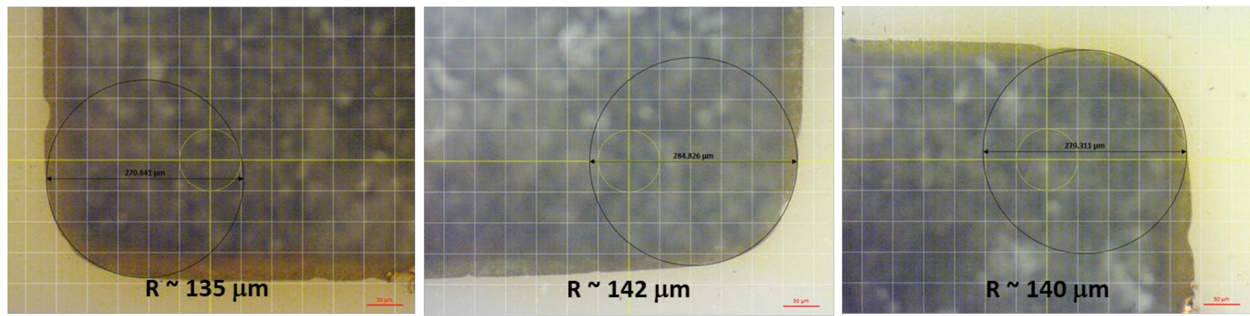


Figure 104. Fillet radii measured for the other corners.

The average natural fillet size appears to be 0.15 mm. Typically, in industry, fillets are *designed* to be much larger than the natural fillets to really get the benefit of filleted corners. These are more likely to be in the order of 0.5 to 1 mm. So, one can not just rely on natural fillets, but one must design them when building a power module layout. In the implementation of fillets in PowerSynth, fillets were designed to have a radius of a third of the trace feature size of the entire layout. This means that the thinnest trace determined the fillet size for the entire layout. This feature can be further parameterized to consider individual traces, and this is described in the future work section.

4.3 Implementation in PowerSynth

4.3.1 Existing post-optimization layout export feature

PowerSynth is a layout optimization tool, optimizing power module layouts for electrical, thermal, and mechanical reliability aspects. The main objective is to get the user to a reasonably optimized solution in much less time than it would take to arrive at a solution using commercial FEA tools. And once a solution is ready, the user would usually want to export these to the FEA tools for further analysis, validation, building of prototypes using geometry files, etc.

Figure 105 shows the PowerSynth EDA tool architecture with export connectivity to external tools like ANSYS, SolidWorks, EMPro, etc. A module has a layer stack that the user provides information about, as described in previous chapters. One of the layers is the interconnect layer. This is the top layer of the metal that is patterned to form traces. The location and size of these traces are optimized by the tool and the optimum solutions are presented to the user as images saved in a pre-specified location. Three variations of an example layout design of

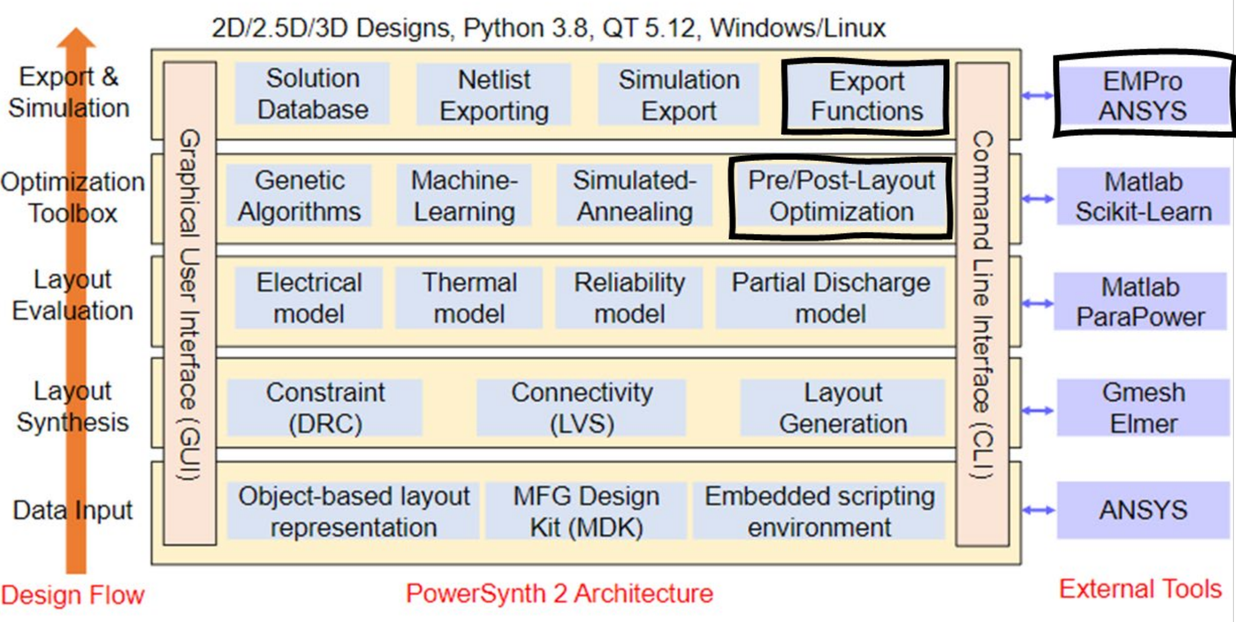


Figure 105. PowerSynth architecture

a half bridge generated by PowerSynth are shown as examples of this is shown in Figure 106.

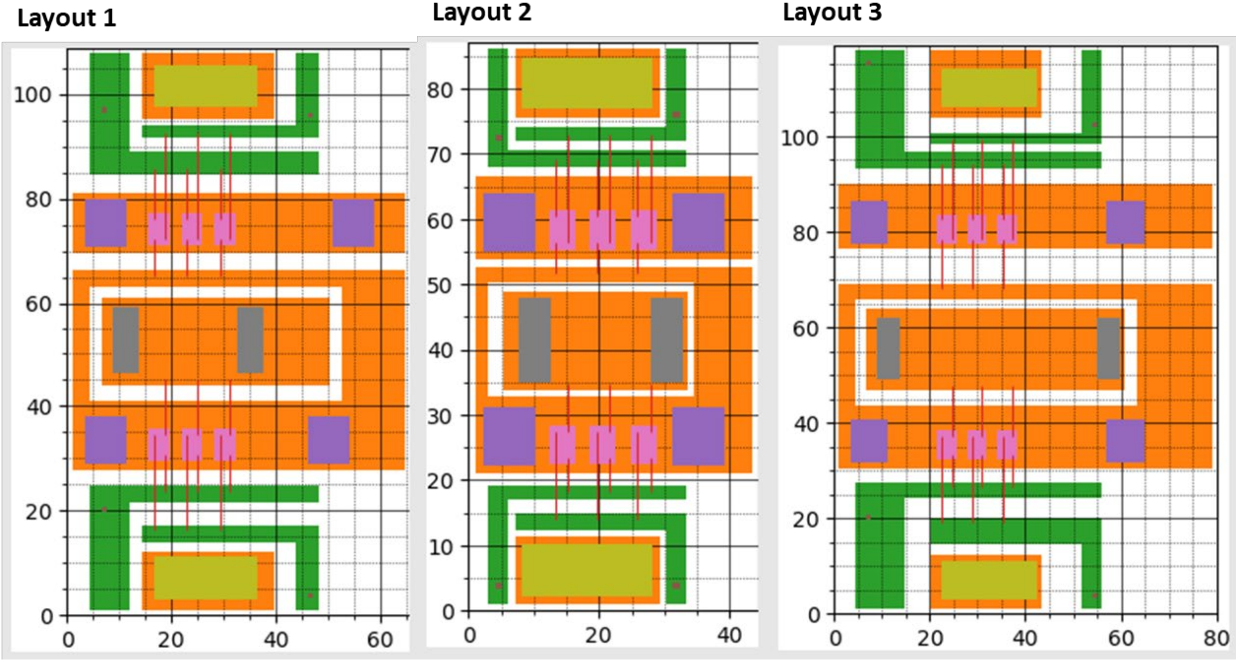


Figure 106. Example layout solution output images in PowerSynth.

The layouts in PowerSynth are built using a corner stitch data structure to determine the location of layout components and a constraint graph data structure to define the sizes and gaps of the components. A CornerStitchSolution object represents a layout solution generated in PowerSynth. This contains module data, such as details of every interconnect layer. These are stored in a ModuleDataCornerStitch object. In most cases for 2D designs, there is only one interconnect layer. For every interconnect layer, the ModuleDataCornerStitch object stores a dictionary of all the islands on the interconnect layer. Islands are a group of traces that are physically connected. The dictionary stores a list of islands and the names of the traces that make up the island.

4.3.1.1 PowerSynth export features

If an export to any external tool is requested by the user, PowerSynth copies all solutions

and their data to another object that is accessible to all export functions. Each solution is stored in a PSSolution object. Among other things, PSSolution objects contain a list of ModuleDataCornerStitch objects as well as a list of features where each feature is stored as a PSFeature object. Each PSFeature object includes a list of layers of the layer stack, their geometry information, their sub-level traces and their geometry information. Using the PSSolution and PSFeature objects, PowerSynth is able to export material and geometry information to external tools like ANSYS, Solidworks, EMPro, Matlab, ParaPower, etc.

4.3.1.2 ANSYS import feature

Tools like Ansys allow the recording of text files while operating the tool in order to document the actions taken in the tool. If the same script is later executed within Ansys, the same sequence of actions are carried out. Using this, designers can code action sequences in Ansys. This was used early on in the evolution of PowerSynth to develop the building of a script that would build the PowerSynth layout geometry in Ansys. This was done using Visual Basic

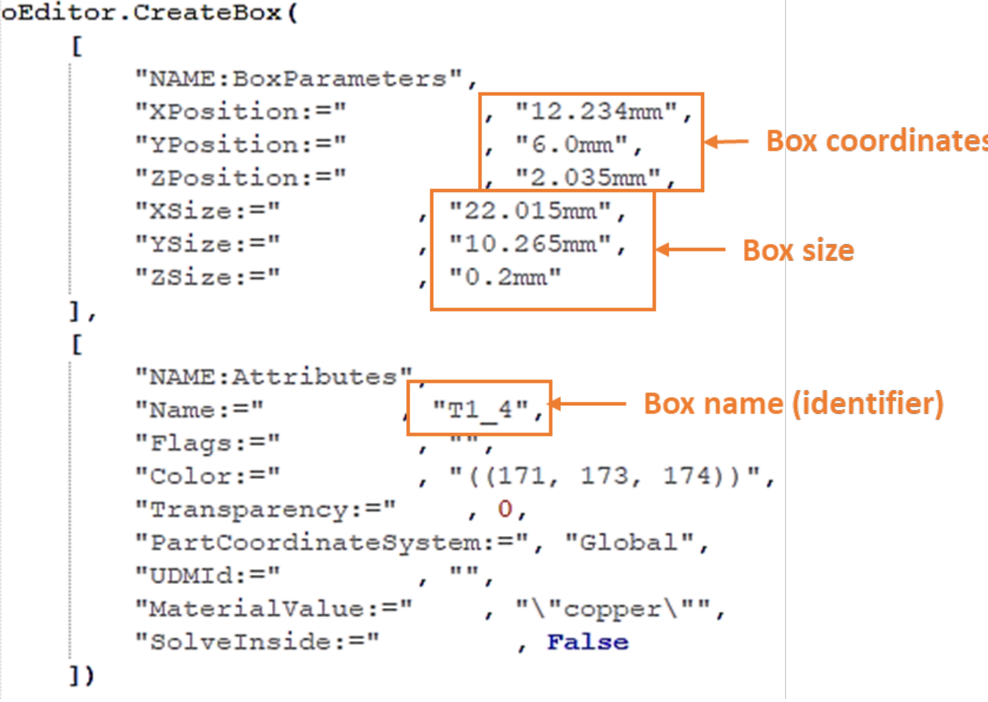


Figure 107. ANSYS ironpython script for creating a box geometry.

Scripts. More recently this has been implemented using ironpython. Figure 107 is an example of an ironpython script to build a box in Ansys, one of the fundamental building blocks for power module structures. The box is identified by its name.

4.3.1.3 PowerSynth solution export to ANSYS

A series of such box-building scripts can be concatenated in PowerSynth to develop the entire power module, using dimension and material information from the PowerSynth solution and layer stack data. The existing API in PowerSynth facilitates the collection of relevant data and builds the script to develop the power module in Ansys. For the three examples shown in Figure 137, the interconnect layer was built in Ansys using this scripting method and the 3D model is shown in Figure 108, Figure 109, and Figure 110.

Notice that the layout contains islands of individual traces that are adjacent but not united

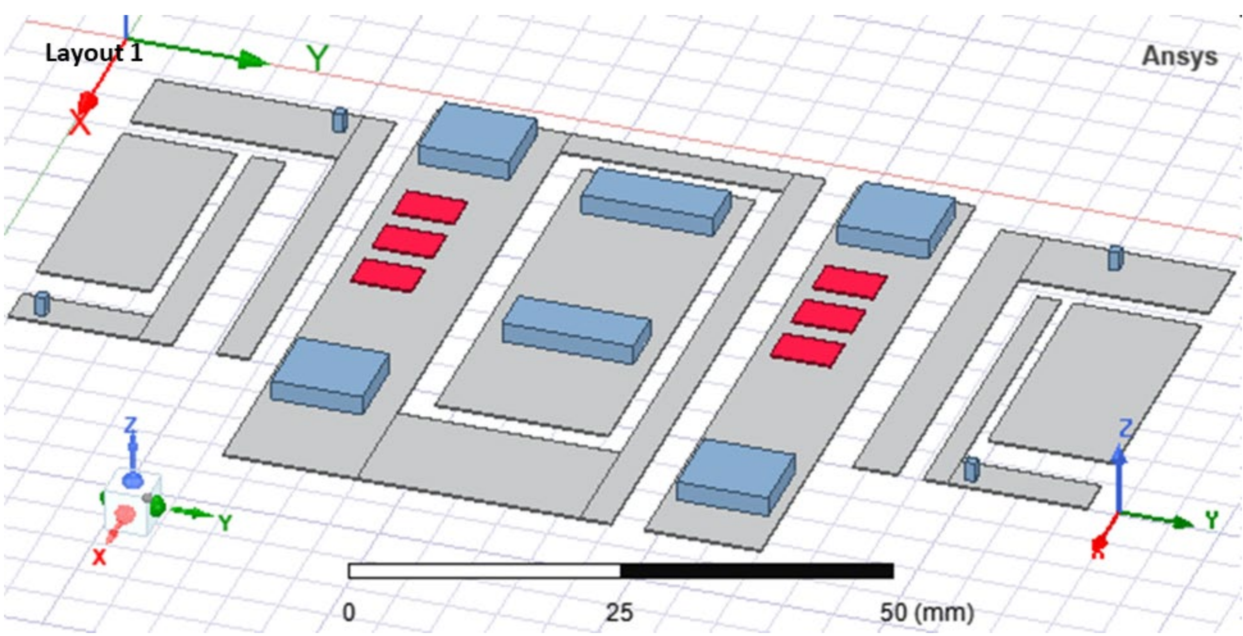


Figure 108. PowerSynth layout 1 from Figure 106 exported to Ansys.

as one object. Also note that the trace have sharp corners. The objective of this contribution was to figure out how to fillet all sharp corners and implement the same into the existing structure of

Ansys export script generation.

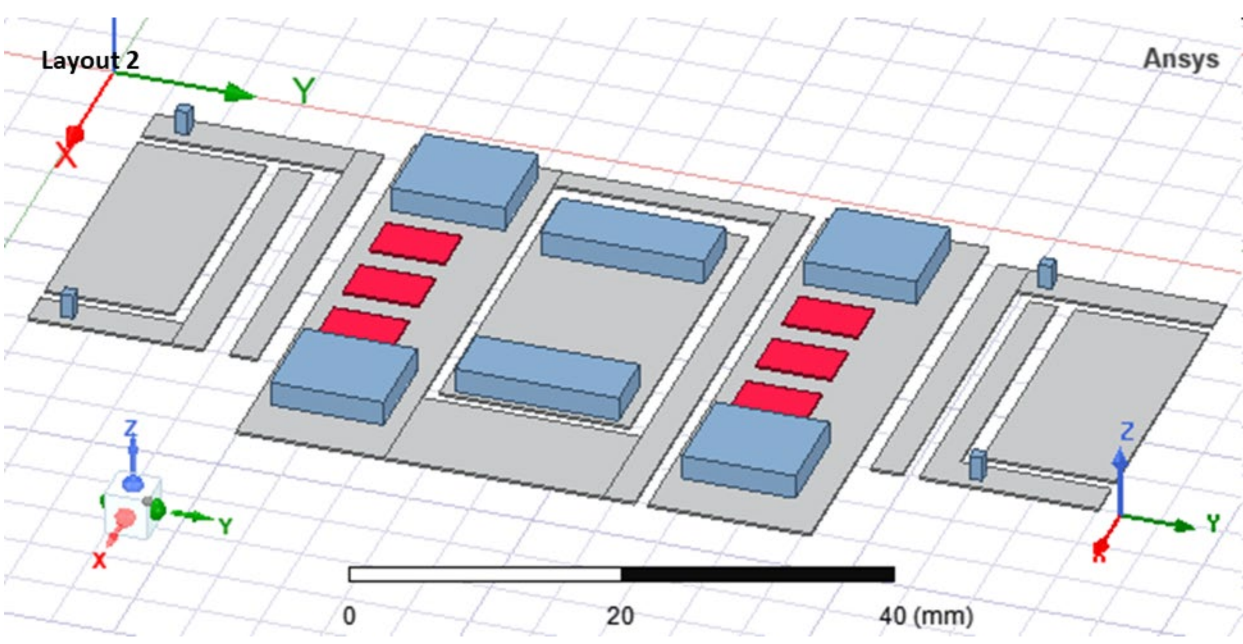


Figure 109. PowerSynth layout 2 from Figure 106 exported to Ansys.

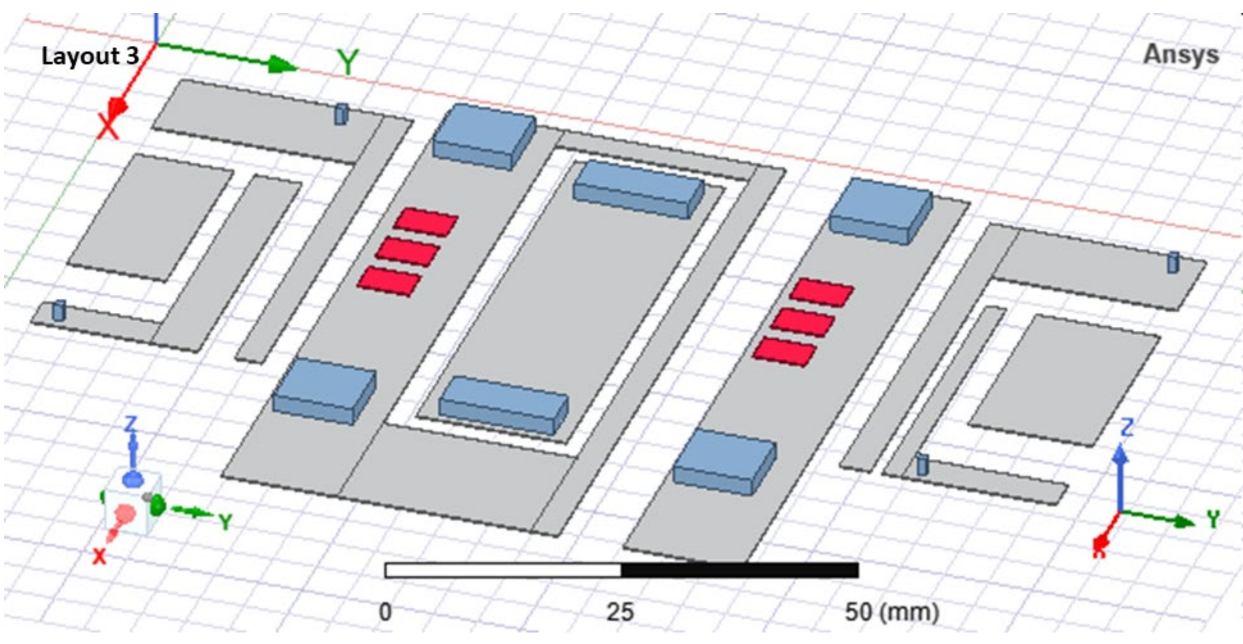


Figure 110. PowerSynth layout 3 from Figure 106 exported to Ansys.

4.3.2 Fillet implementation to the ANSYS export API

4.3.2.1 Challenges in fillet application automation

Fillets in Ansys are executed by selecting an edge to be filleted and applying the fillet command to it. Figure 111 shows how this is done in the Ansys GUI. For a few boxes, it is not

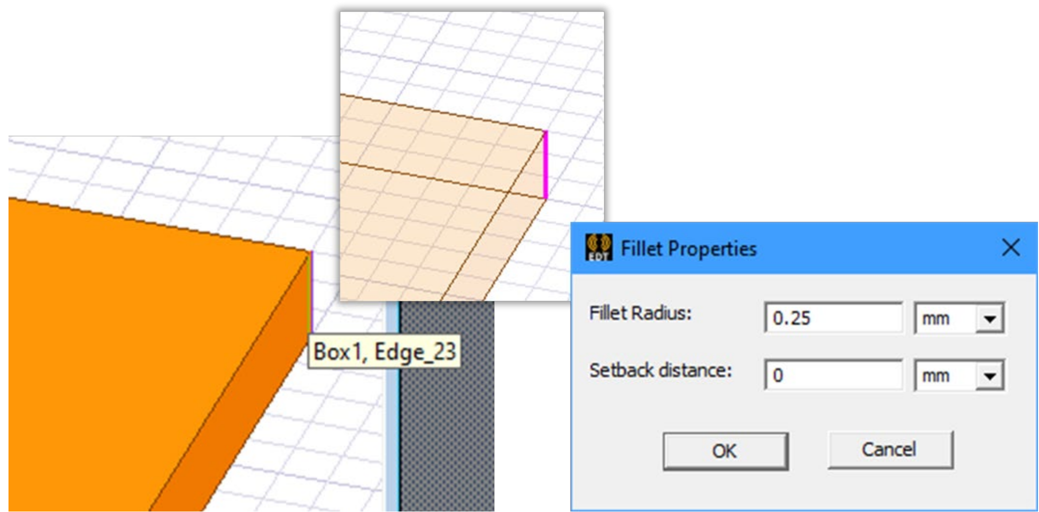


Figure 111. Filleting an edge of a box in Ansys using GUI.

difficult to use the GUI to apply fillets. However, for more complex layouts, it would take a long time to identify and fillet each corner of each trace. In many cases, traces must be united and then filleted to avoid situations like the one shown in Figure 112. Therefore, fillet application

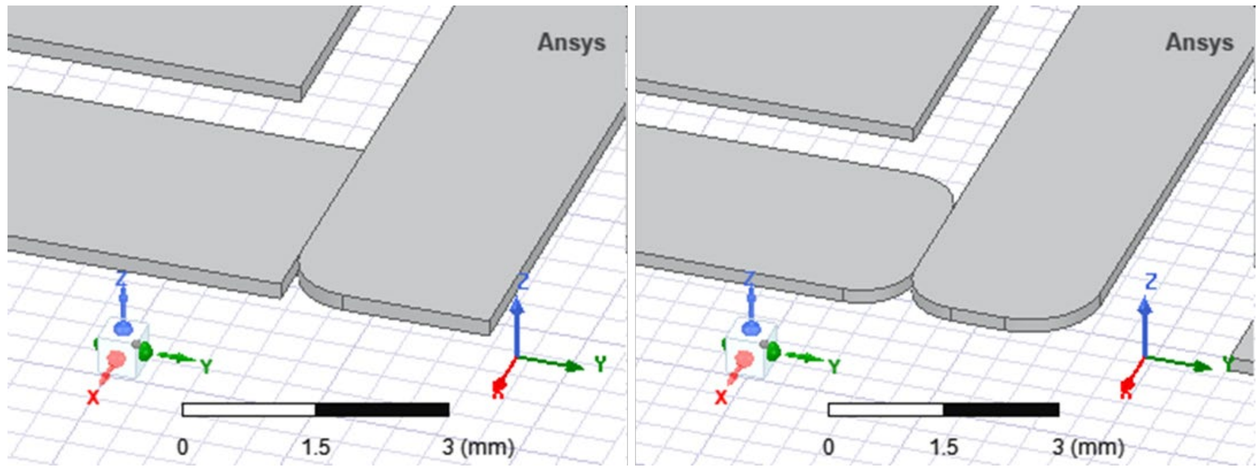


Figure 112. Incorrect fillets when traces are not united.

must be automated.

To automate fillet application using a script, there must be a one to one mapping between the edges of the geometry in PowerSynth to the edges of the geometry exported to Ansys. This was accomplished using a template script like the one shown in Figure 113, and the following information was edited in it: the box name, the edge number, and the fillet radius. Each edge is identified by a number. The edge number of the edge to be filleted must be specified, and the box

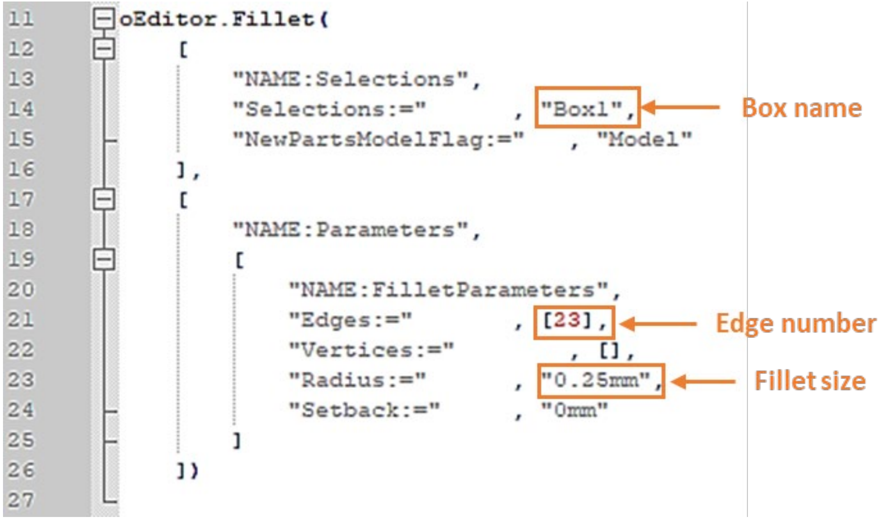


Figure 113. Macro script template for generating a fillet on a box edge.

that the edge resides on must also be identified. This is easy to do using the Ansys GUI as shown earlier (Figure 111) but challenging using scripts because it is not easy to predict what the edge number will be for a box. And how boxes will be labelled. If a box name is not intentionally provided, Ansys labels them as ‘Box1’, ‘Box2’, ‘Box3’, etc. in the order that they were built. So, one must find out the sequence of the build. These are some of the challenges in implementing the automation of fillets using scripts. Nevertheless, once the build order, labeling, and numbering methods are figured out, the benefits far outweigh the costs.

4.3.2.2 Implementation algorithm

For this work, first, the method that Ansys uses to number all edges was discovered.

Considering the generic example in Figure 114 it was seen that the edge numbers assigned to the vertical edges of ‘Box1’ were 21, 22, 23, and 24. Drawing another box and observing its edge numbers showed that they were labelled 49, 50, 51, and 52. Drawing multiple boxes one after another and observing their edge numbers revealed a pattern. Edge group 21-24 were 28 in count apart from edge group 49-52. Every subsequent edge group was 28 counts apart from its

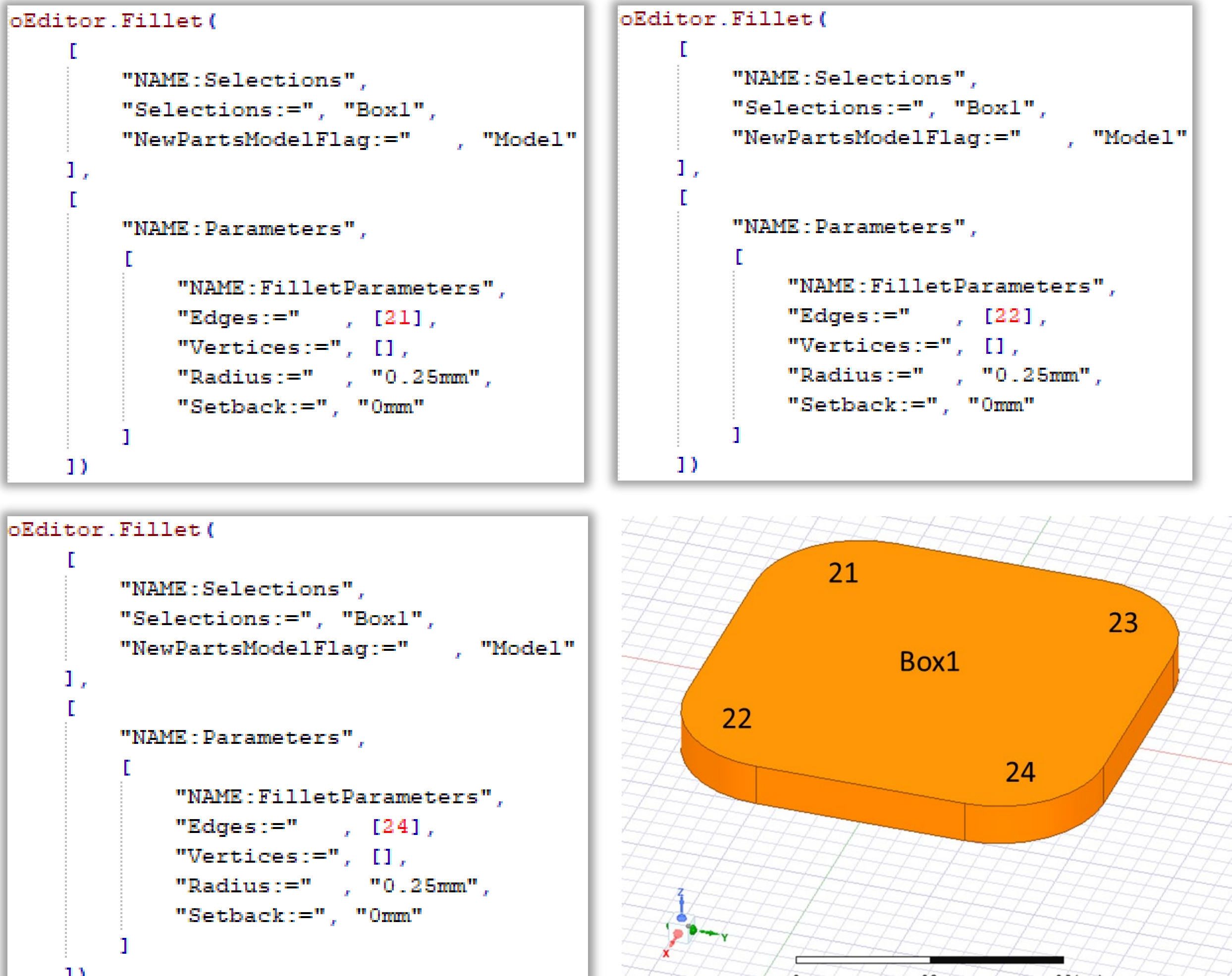


Figure 114. Edge numbers of the fillted edges of the first box created in Ansys EDT and their fillet scripts.

previous edge group.

Another pattern was revealed. Within each edge group, Ansys assigns edges in a certain order based on x-y coordinates. The edge that has the least x and y coordinates gets the first edge

number of the group. The next number goes to the edge that is furthest in the x-direction but with the same y-value. The one after that has the furthest y-value, but the same x-value as the first edge. And the last edge number of the group is assigned to the one that has the highest x and y coordinate values. This applies to all edges that are parallel to the z-axis. Finding these two patterns was critical to the implementation of this code. Figure 115 shows boxes and their edge

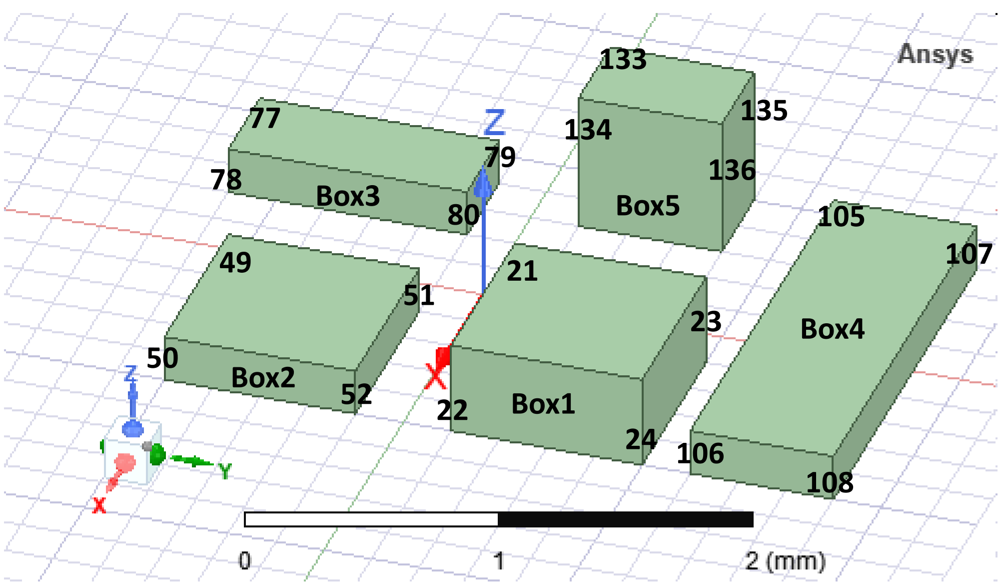


Figure 115. Edge and box labeling pattern detected in Ansys.

labels showing this pattern.

The next challenge was to determine the box number that the edge that was to be filleted belonged to. In PowerSynth, boxes for the Ansys macro script were already labeled by their correlating PowerSynth trace number according to the trace layout in Figure 116. The ".4" at the end of each trace name refers to the layer number in the layer stack. The 4th layer is the interconnect layer that contains the traces of the layout (the first layer is the baseplate).

Edges that belong on a trace that is not connected to any other trace physically are the easiest to fillet. The scripts shown in Figure 114 are good examples of these. However, traces that are connected to other traces are more difficult to fillet. This is because:

- The traces need to be united first and when boxes in Ansys are united, the unit becomes a single object that takes on the name of one of the traces that were part of it, thereby losing part of their original identity as an individual trace and making it more difficult to identify them for filleting purposes.
- Once these traces are united, some of their edges are lost since they become part of the straight edge formed during the uniting process. The fillet function must not be applied to these former edges. So, care must be taken to identify the valid edges that need filleting *after* the uniting process.

The two issues above were addressed. First, it was found out that when two traces are united, the trace that was selected first, its name becomes the name of the united trace. When using a macro script, an array of trace names is passed that need to be united. The resulting trace

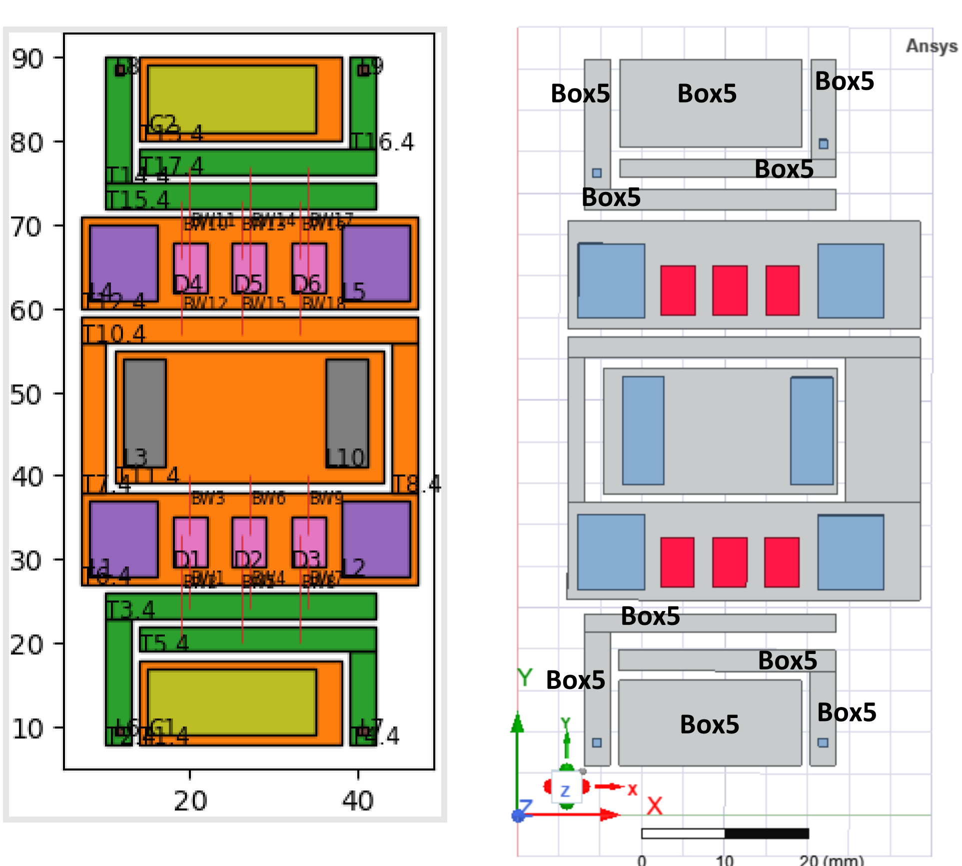


Figure 116. Trace name map between initial layout and Ansys exported layout.

group takes on the name of the first trace mentioned in the array. Knowing this, a dictionary was created in PowerSynth to store the names of trace groups that would be united, and the name that would result of the united trace group, called an island in PowerSynth. The information needed was borrowed from the Island objects in PowerSynth, which contained, among other things, a list of traces in the island. This was then used in the unite script, a template for which is shown in Figure 117. To find out which edges intersect other edges, so that they are not filleted, a trace-

```
print ("Unite traces:", "T6_4,T7_4,T8_4,T10_4")
oEditor.Unite(
    [
        "NAME:Selections",
        "Selections:="      , "T6_4,T7_4,T8_4,T10_4"
    ],
    [
        "NAME:UniteParameters",
        "KeepOriginals:="   , False
    ])
```

Figure 117. Ansys script for uniting four traces.

edge dictionary was created where only non-duplicate edges were listed, by first counting the occurrence of each edge's coordinates and discarding any that had the same coordinates.

Once the names of traces that need to be united are found, each set of names of traces to be united can be sent to a script template as parameters, and the resulting script lines can be concatenated (or appended) to the existing macro script for the entire layout. Figure 118 shows the output of uniting all traces that belong to an island and Figure 119 shows an example ironpython macro script for uniting four of the traces from Figure 116. Once traces are united, the correct edges need to be filleted. The algorithm used to find the trace names and edge numbers, and to fillet those edges is given in Figure 120.

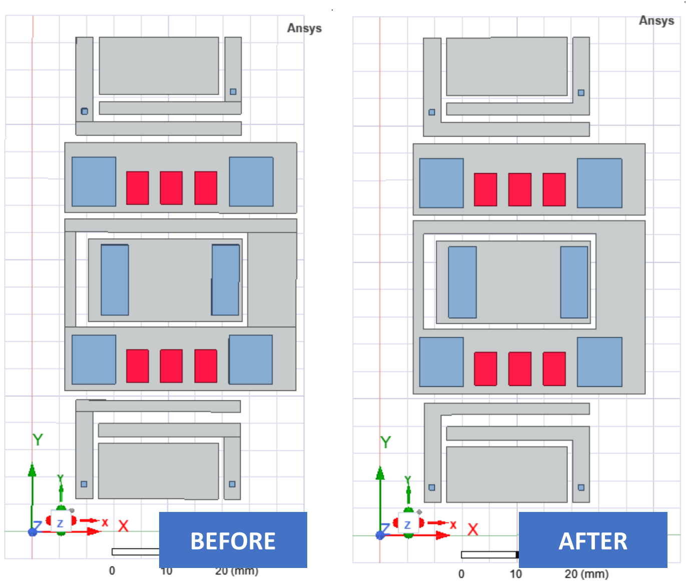


Figure 119. Output of uniting traces using ironpython script.

```
trace_list = T7_4,T8_4,T10_4,T6_4
existing_output_script += Unite.format(trace_list)
```

```
Unite='''
print ("Unite traces:", "{0}")
oEditor.Unite(
    [
        "NAME:Selections",
        "Selections:="        , "{0}"
    ],
    [
        "NAME:UniteParameters",
        "KeepOriginals:="    , False
    ])
'''
```

```
print ("Unite traces:", "T6_4,T7_4,T8_4,T10_4")
oEditor.Unite(
    [
        "NAME:Selections",
        "Selections:="        , "T6_4,T7_4,T8_4,T10_4"
    ],
    [
        "NAME:UniteParameters",
        "KeepOriginals:="    , False
    ])
```

Figure 118. Ironpython example for generating macro script for uniting four traces.

```
for each PowerSynth_solution:
# initialize dictionaries:
    island_trace_dictionary = {}
    trace_edgeID_dictionary = {}
    edge_coordinates_dictionary = {}
    coord_trace-edge_dict = {}
    trace_edgelist_dict = {}
    max_edgeID = 21 # because the first box built in Ansys has edge ID starting from 21,
                    # and the script starts out by building traces, then devices, etc.
    if fillet_layout_flag is True:
        for each interconnect_layer in the solution:
            for each island:
                map island name to a list of the traces in the island
                and save it in the island_trace_dictionary
    for each feature in the solution:
        box = AnsysEM_Box() object # existing code to initialize box script
        if fillet_layout_flag is True:
            if the the feature is a trace:
                edge_list = [max_edgeID, max_edgeID+1, max_edgeID+2, max_edgeID+3]
                map trace name to edge_list and save it in the trace_edgeID_dictionary
                trace_edgeID_dictionary[trace_name] = edge_list
                max_edgeID += 28 # because there are 28 edge numbers per object
                for each edge in edge_list:
                    map edgeID to (x,y) coordinates of the edge
                    and save it to the edge_coordinates_dictionary
                collect size of each trace in a list # to later determine the thinnest trace
        write script to build the box in Ansys # existing code to build a box
    if fillet_layout_flag is True:
        fillet_radius = one third of the thinnest trace in the entire layout
        for each island in the island_trace_dictionary:
            if there is more than one trace in the island:
                make an array of those traces, and
                write script to unite those traces # new script added to unite traces
        create a unique_coordinate_list.
        for each coordinate in the edge_coordinates_dictionary:
            if the coordinate is unique, save it to the unique_coordinate_list
        for each coordinate in the unique_coordinate_list:
            map the coordinate to (trace_name, edgeID) and save it in the coord_trace-edge_dict.
        for each coordinate in the coord_trace-edge_dict:
            if the trace is part of an island:
                replace the trace name with the name of the leading trace in the island.
        for each (trace_name, edgeID) in the coord_trace-edge_dict:
            group all edgeIDs by trace, mapping them in the trace_edgelist_dict
            # new script added to fillet traces:
            write script to fillet (trace, edgeID_list) from the trace_edgelist_dict
```

Figure 120. Pseudocode to unite and fillet traces with unique edges.

4.3.2.3 Implementation results

For the initial layouts shown in Figure 108, Figure 109, and Figure 110, the filleted layouts built from this work are shown in Figure 121. Each solution's traces were filleted with its own unique fillet radius based on the thinnest trace in that layout solution.

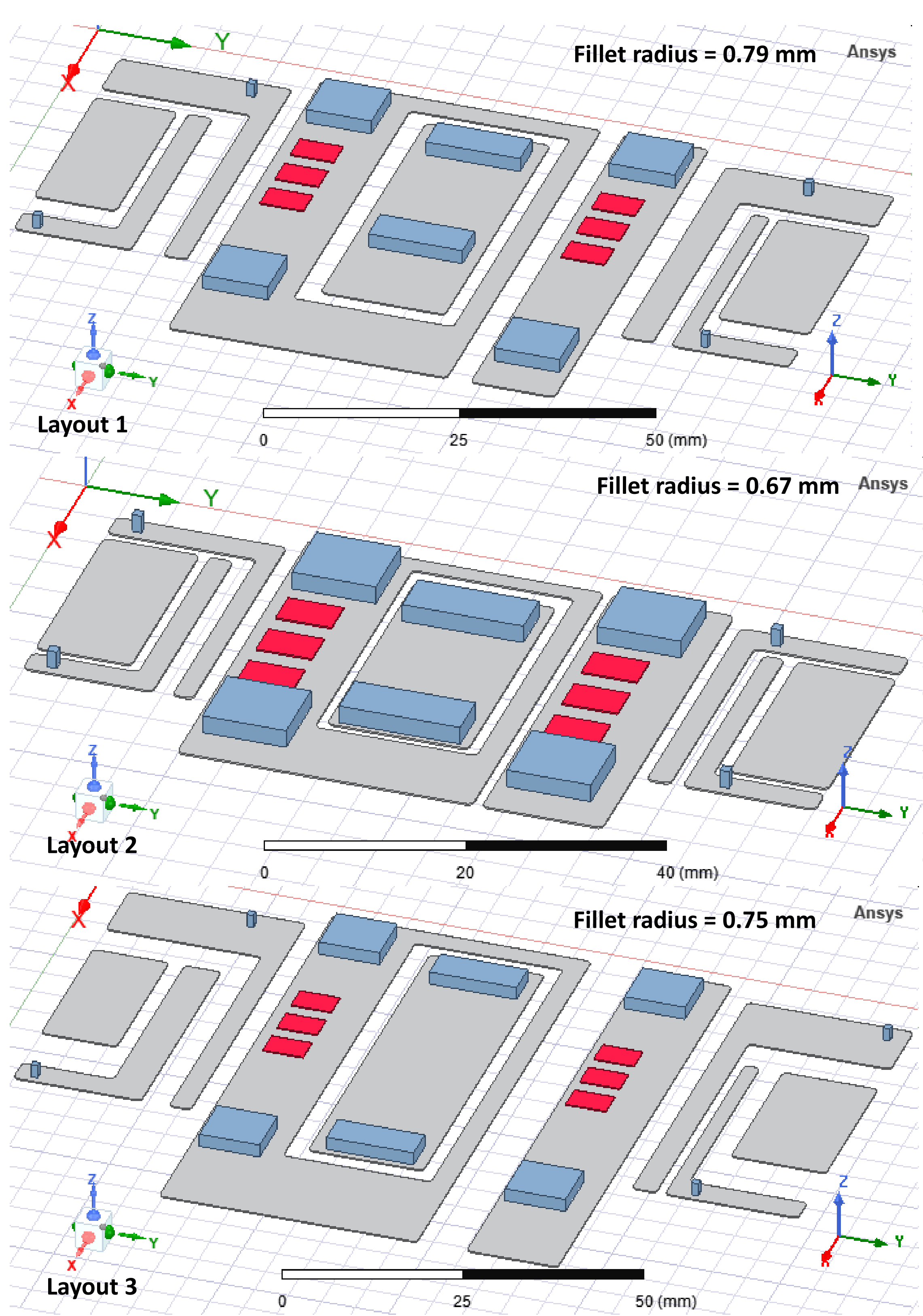


Figure 121. Filleted layout results in Ansys.

Chapter 5. Conclusion and Future Work Ideas

5.1 Conclusion

A novel charge density-based PDIV vs. trace-gap modeling approach was developed, and a voltage class and optimum trace gap quantified for a DBC-encapsulant technology that was validated through PD tests. For a 12/25/12 alumina DBC with Dow Corning 3-6635 dielectric gel, the voltage class was 6.5 kV, and the trace gap was 2 mm. It was seen that extending the trace gap beyond 2 mm did not change the PDIV; it remained steady at 6.5 kV. This point of diminishing returns is a critical piece of information. It indicates the maximum operating voltage for PD prevention and the corresponding optimum trace gap to the designer. For smaller trace gaps, the serious trade-off with voltage is evident.

The methodology presented in this work included the derivation of PDIV from surface charge density simulations. The simulations creatively avoided the challenges presented by E-field-related singularity problems. The prediction model was then experimentally calibrated through statistical analysis, validating the PDIV modeling method and the PDIV vs. trace-gap trend.

Once calibrated for a given manufacturing line, the calibrated simulations to determine PDIV were used for simulating other packages that would use a similar manufacturing process. The calibrated simulation template thus developed was used to simulate numerous cases for comparison and implementation in PowerSynth, an EDA tool.

An extensive library of PDIV results was generated for various materials and geometries of substrate-encapsulant combinations. For a different manufacturing process, such as an industrial one that has much higher precision, or a completely different method of manufacturing or assembling the modules, the simulations need to be re-calibrated using the method shown in

Chapter 2. This would have to be done at the user end and the adjusted calibration factor (called k-value in the chapter) can be entered in the software, keeping the implementation structure the same but allowing flexibility to incorporate another manufacturing line's influence on PDIV estimates. This is exactly the flexibility that is enabled by the MDK. For a significant departure of the package structure from the one presented in this work, the methodology presented here can be re-used to re-develop simulations, calibrate them, and enter the new PDIV data library in the architecture provided in PowerSynth through this work. The work also incorporated flexibility to allow a dual-encapsulant system where a coating material is used for field grading.

This work also considered the automation of fillet generation for filleting critical corners of power module layout traces. Fillets were shown to reduce E-field at the corner by 65%, allowing modules to be more compact. Layout geometries exported to ANSYS Electronics Desktop now include filleted traces. This enables users to skip a manually tedious step in the design process of power module prototyping. These implementation details were discussed in Chapter 4.

In sum, while there is ongoing foundational work in understanding and modeling the complicated physics of partial discharge and the engineering of various PD mitigation strategies, there are no hardware-validated rules or standards codifying the likelihood of PD in native trace gaps or automating any of the PD mitigation strategies like filleting. This work is pioneering the movement toward a reliability-based DRC paradigm specific to partial discharge prevention inside power modules using automation tools. This is the right time to build and use automation tools to meet the growing demands of semiconductor manufacturing, and this work presents part of the framework on which future work can be built.

5.2 Future work

Numerous future work ideas have emerged from this work. A non-exhaustive listing is provided here, where each sub-item could be an individual research topic:

1. Cost analysis could be included in the study. Substrates and encapsulants vary in cost based on material choice. Incorporating this would give engineers who are building modules an idea of the cost effectiveness of their design decisions, especially when considering trade-offs. For example, the Dow 3-6635 gel has a dielectric strength of 20 kV/mm and costs $103/kg, whereas the Wacker 612 gel with dielectric strength of 23 kV/mm costs $116/kg, for bulk orders. For ceramics, there is no trade-off between electrical properties and cost: 1.) Alumina with better dielectric properties than aluminum nitride is also the cheaper of the two; 2.) Thicker ceramics offer better isolation and cost the same as thinner ceramics; and 3.) Thicker metal layers on ceramics are safer from a PD perspective and are less expensive to manufacture than very thin metal layers. The trade-off for ceramics is in their thermal property (AlN can withstand higher temperatures and has higher heat conductivity than Al_2O_3), which is encompassed in the electro-thermal optimization process of PowerSynth. Cost of a substrate is mostly affected by whether the substrate has electroplated Ni and/or Au on it or not, which affects solderability and attachment reliability, and are outside the scope of this study on PD but could be assessed for a separate study on general attachment reliability. Also, AlN is more expensive than Al_2O_3 because of its thermal properties. The cost of an encapsulant or ceramic material can be included in the material library as a "property" or in a separate cost library that also includes cost of substrates and encapsulants in general.
2. Since AlN is the better ceramic choice for thermal reasons, but alumina is the preferred

choice for electrical performance, electrical reliability (low PD likelihood), as well as cost, it might be good to incorporate low PDIV and cost as performance metrics in the optimization tool.

3. The PD test conditions could include factors like:
    a. Voltage profiles, such as:
        i. AC, testing the effect of frequency
        ii. Pulsed DC, testing the effect of switching frequency
        iii. Rise time and fall time effects, or dv/dt effects
    b. Environmental conditions, such as:
        i. Pressure – this is critical for applications that encounter low pressure, such as aircrafts operating at a high altitude in the atmosphere, because PD can suddenly increase below a certain pressure * (mean free path) according to Paschen's curve shown in Figure 5.
        ii. Temperature
        iii. Humidity
4. The PD test samples could be varied to assess the effect of factors like:
    a. Dual-encapsulant system
    b. Substrates like LTCC and HTCC
    c. Stacked substrates
    d. Filleted traces
    e. Surface roughness, or the effect of electrode polishing
    f. Various trace patterns (like corner to corner, corner to straight edge, etc.)
5. Design rules could be developed for the other PD mitigation strategies.

6. Incorporating phase resolved partial discharge (PRPD) signature patterns for AC PD tests could provide more information about the cause and location of PD, however the stochastic nature of PD might dominate.
7. The implementation in the EDA tool could include the Weibull analysis and additionally allow the user to choose a reliability percentile other than the default ~63% defined as the characteristic value percentile.
8. Surface tracking, and creepage and clearance rules could be further developed using PD tests, and cabinet level design rules could be implemented in a tool like PowerSynth, scaling up the possibilities of EDA.
9. A more detailed study on current crowding and how fillets help alleviate adverse effects like electromigration at concave corners could be done. The effect of ambient temperature and internally generated heat could be included in this.
10. Novel materials, such as encapsulants with heat transfer dopants or trace gap coating materials could be characterized for PD prevention or dielectric ability using the PD test equipment and the test plan used in the work for Chapter 2.
11. One might assess the mechanical and thermal tradeoffs for having an encapsulant material.
12. Implementing an export feature for ANSYS and other tools that includes the encapsulation method and applying this to the filleted traces could be done.
13. Fillet sizes could be customized to the size of each trace. For the current work, the fillet size is based on the smallest trace width among all traces in the layout and that size is applied to all fillets. Caveat: the concave corners would need to be filleted with adjacent traces in mind since a concave corner, when filleted, fills up negative space instead of

creating negative space. The filled up negative space might overlap an adjacent trace. This must be checked if implementing custom fillets for each trace. Customized filleting also changes the tracegap in an undesirable way at a concave corner.

14. One might assess how design rules for trace gaps must be adjusted based on fillets generated, and the impact of filleting on compactness. Preliminary work on this was done and mentioned in Chapter 4, but more extensive work with several examples of fillet-adjusted trace gap in complete layouts could benefit the community.
15. A solution browser-like interface for PD-aware layouts could be developed to allow the user of PowerSynth to browse different layout solutions and its voltage-compactness tradeoff in a single window.
16. Fillets could be applied to the export of PowerSynth to other tools like SolidWorks, or more standard STL files.
17. DBCs sold by various manufacturers could be characterized for PDIV. Various substrate technologies could be characterized and compared. Different sizes of DBCs by the same manufacturer could be characterized as well.
18. At a higher level, standards need to be developed for DC PD testing. Existing standards only cover AC PD tests. The DC tests for this work were based on the PD test equipment manufacturing company's manuals and examples.

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Appendix A: Description of Research for Popular Publication

In a race to build the fastest, smallest, and most powerful electronics for the power circuitry of electric vehicles, real estate comes at a premium because every mile per gallon counts. With that in mind, power module designers are pushing the limits of electronic module compaction while driving high power loads through the packaged semiconductor devices in them. While the devices themselves are promoted as being able to operate at high voltages, high temperatures, and have a low spatial footprint, the packages they reside in are not upgraded accordingly, limiting the capability of the entire module. Even if there is a possibility of high speed or high power density, the materials and compaction would limit the overall module's operating voltage capability. This is because of a silent killer called partial discharge, which is an invisible local spark that slowly degrades insulation material, and eventually leads to short circuit and failure of the module, risking the safety of the larger system around the module.

Researchers at the University of Arkansas have developed a method to account for the voltage limit of these advanced modules in the constantly evolving landscape of electronic design automation, an innovation of its own. With this work, they hope to move the industry toward adoption of more reliable practices in the design and development of power modules, even from the design stage, considering as many competing design factors as possible. The in-house built tool called PowerSynth is leading the race in electronics design automation of power module optimization. And it now incorporates hardware validated design rules for partial discharge awareness in power modules.

Appendix B: Executive Summary of Newly Created Intellectual Property

A method to model partial discharge inception voltage for various combinations of power module substrate-encapsulant pairs was found and implemented in an electronic design automation tool in terms of spatial design rules. This solution to the PD mitigation problem creatively addresses the convergence issues at the triple point of a power module. It also focuses on the more practical PD inception voltage instead of the charge quantity. As mentioned in the front matter, part of this work has been published as:

S. Mukherjee, T. M. Evans, D. R. Huitink and H. A. Mantooth, "A Partial Discharge Inception Voltage Modeling Approach," in IEEE Open Journal of Power Electronics, vol. 4, pp. 148-160, 2023, doi: 10.1109/OJPEL.2023.3241853.

And the rest of this work will likely be submitted soon to a journal for publication.

Another intellectual property is the automatic application of fillets to all power module layout solutions exported to Ansys, one the most used 3D finite element analysis tools in industry for electrical, thermal, and mechanical simulations. This code also determines the optimal fillet size to be used on all traces of the layout. This work will likely be submitted to a journal or conference in the near future.

Both automation aspects come at a critical time when there is a great push to build new semiconductor fabrication facilities to meet manufacturing demands.

Appendix C: Potential Patent and Commercialization Aspects of Listed Intellectual Property Items

Instead of patenting and/or commercializing the intellectual property created in this research, it will be disclosed through the publishing of the work in leading journals in the field of power electronics. The PowerSynth software is open-sourced. The code implemented in the software as a result of this dissertation will be a future release.

Appendix D: Broader Impact of Research

D.1 Applicability of Research Methods to Other Problems

Research methods used in this work are designed to be scaled up for various manufacturing plants. It can also be used for general hardware validation of any design rule development process that relies on empirical testing of stochastic processes. Many of these examples are provided in the Future Works section of Chapter 5.

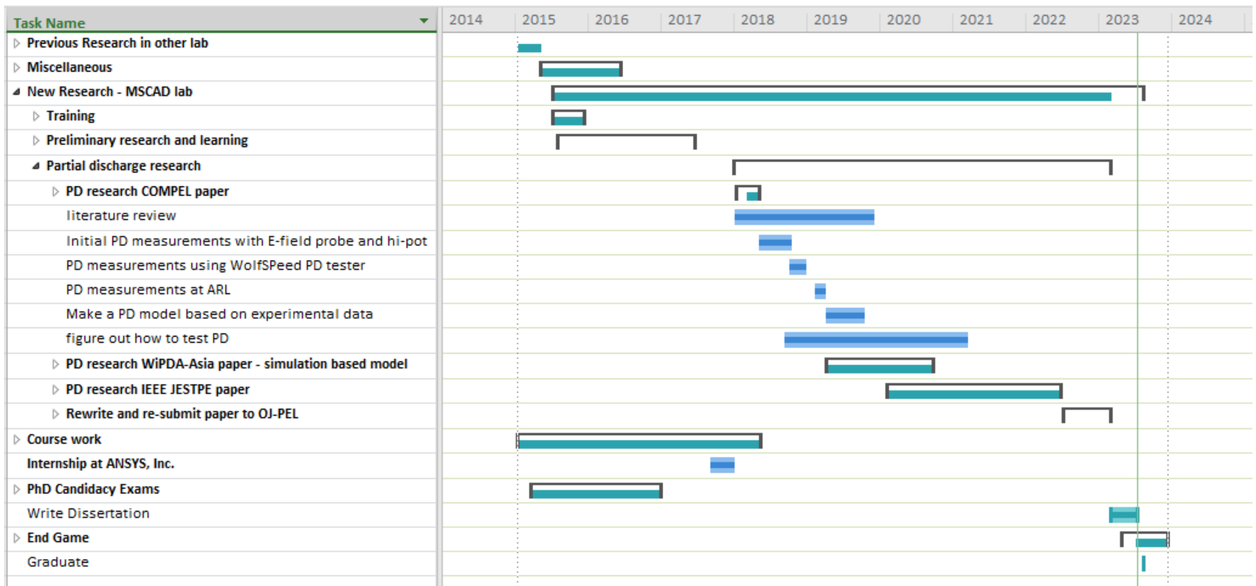
D.2 Impact of Research Results on U.S. and Global Society

The Unites States is going through large growth in semiconductor manufacturing and is investing in human resources to develop the large scale fabrication facilities being built. This is the critical time to standardize the design process of semiconductor device packaging. With multiple designers working in separate companies, there is a great need to build standards so that assembly is more aligned across platforms. The research in this work is geared to help this growing industry standardize its design automation processes for the power electronics sector. This research is drawing its inspiration from the already successful and mature integrated circuit design sector.

D.3 Impact of Research Results on the Environment

The design automation presented in this work eliminates the need for extensive prototyping and potential mistakes in manufacturing. Using a few experiments to validate many simulations, this computational tool presents no environmental hazards, rather, it renders potentially hazardous trial and error practices unnecessary by the use of software.

Appendix E: Microsoft Project for PhD Microelectronics and Photonics Degree Plan



Appendix F: Identification of all Software Used in Research and Dissertation Generation

Computer #1:
Model Number: Dell XPS 13 9370
Serial Number: 5WZCSN2
Location: Laptop
Owner: Shilpi Mukherjee

Computer #2:
Name: eleg-c210Ma01w1.ddns.uark.edu
Model: Dell
Location: CSRC 210.01
Owner: Dr. Alan Mantooth

Software #1:
Name: Microsoft Office 365
Purchased by: University of Arkansas

Software #2:
Name: Ansys Electronics Desktop
Purchased by: Dr. Alan Mantooth

Software #3:
Name: Origin
Purchased by: Dr. Yarui Peng

Software #4:
Name: PowerSynth
Owner: Dr. Alan Mantooth and the PowerSynth team, co-owner

Software #5:
Name: Omicron MPD 800
Purchased by: Dr. Alan Mantooth and Dr. Yue Zhao

Software #6:
Name: LabView
Owner: NCREPT

Appendix G: All Publications Published, Submitted and Planned

- S. Mukherjee, T. M. Evans, D. R. Huitink and H. A. Mantooth, "A Partial Discharge Inception Voltage Modeling Approach," in IEEE Open Journal of Power Electronics, vol. 4, pp. 148-160, 2023, doi: 10.1109/OJPEL.2023.3241853.

- S. Mukherjee, Y. Peng and H. A. Mantooth, "General Equation to Determine Design Rules for Mitigating Partial Discharge and Electrical Breakdown in Power Module Layouts," 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Suita, Japan, 2020, pp. 1-6, doi: 10.1109/WiPDAAsia49671.2020.9360263.

- S. Mukherjee, T. Evans, B. Narayanasami, Q. Le, A. I. Emon, A. Deshpande, F. Luo, Y. Peng, S. Pytel, T. Vrotsos and H. A. Mantooth, "Toward Partial Discharge Reduction by Corner Correction in Power Module Layouts," 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, Italy, 2018, pp. 1-8, doi: 10.1109/COMPEL.2018.8459973.

- S. Mukherjee *et al.*, "Partial discharge mitigation in power modules by trace fillet automation." (planned submission, title subject to change)

- S. Mukherjee *et al.*, "A partial discharge aware power module design approach." (planned submission, title subject to change)

Appendix H: Test Structure Design Instructions

H.1 DBC etch pattern design in AutoCAD

The pattern to be etched on the DBC using dry film photolithography was first designed in AutoCAD and then printed onto a photoplot plastic sheet. The design with its dimensions is shown in Figure 122 and the legend for each layer is shown in Figure 123. The photoplot transparency sheet boundaries are marked in green. The dimensions of the physical DBC are annotated in orange. The physical DBC is about 127 mm x 178 mm. Each blue square represents the trace islands, and they are all 11 mm x 11 mm. Each yellow rectangle represents the copper on the back side of each sample. In Figure 124 there is a 1 mm gap between two adjacent samples where the dicing lines are. Thirty five samples could fit into one master card with some space to spare. Two master cards were etched together for a total of 70 samples to allow tolerance for samples with defects and have extra for contingency. Fitting the maximum number of samples in each card is most cost effective. Samples with various trace gaps were distributed throughout the board to even out any imbalances in the etching process, in case one part of the substrate gets etched more than the other, since it is not a perfect process. Trace gaps for some of the samples are marked in Figure 124. Note that all layers were aligned to the alignment marks that are on the layer for the photoplot page margins to ensure the pattern of the bottom side of the DBC aligns with the pattern on the top side of the DBC.

An individual sample's dimensions are depicted in Figure 124 (right) where the boundary of the ceramic is marked by the dice lines of the DBC sample in magenta and is 33 mm x 17mm. The 23 mm x 39 mm rectangle and the 27 mm x 43 mm rectangle mark the boundaries of the plastic housing that forms the walls of the well which will hold the encapsulating gel. This gives a 3 mm gap between the housing and the DBC. The 40 mm x 46 mm lines mark the FR4 base

board boundary. Note that an additional 0.5 mm space was added to the copper base board on each side for easier sample handling during the assembly process as discovered during test runs. So, the base board size increased from 39 mm x 45 mm (Figure 22) to 40 mm x 46 mm (Figure 124).

The top side copper layer and the bottom side copper layer are shown in Figure 125. Once the pattern outline is ready, the parts that will get etched are hatched. These will be covered in black ink. The figure shows the top copper layer in blue and bottom copper layer in yellow, and their corresponding hatched portions in black where the copper is to be etched away. Copper is etched away where it is dark because that is where the negative photoresist would not be exposed to light, and it would not harden. Therefore, when the photoresist is developed, the portions that were not hardened under the mask would wash away, whereas the portions that were exposed to light would remain, covering the copper in that region from being etched by the chemicals in the next step. The hatched pattern was printed using the photoplot printer ensuring the black ink would be on the matte side of the transparency. Intentional gaps in the copper pattern especially at the edges of the master card on the back side allowed for easy alignment of the dicing blade and ensured there was a clear dicing track; metal in a dicing track can affect the dicing blade adversely. This gap is seen in the yellow pattern in Figure 125.

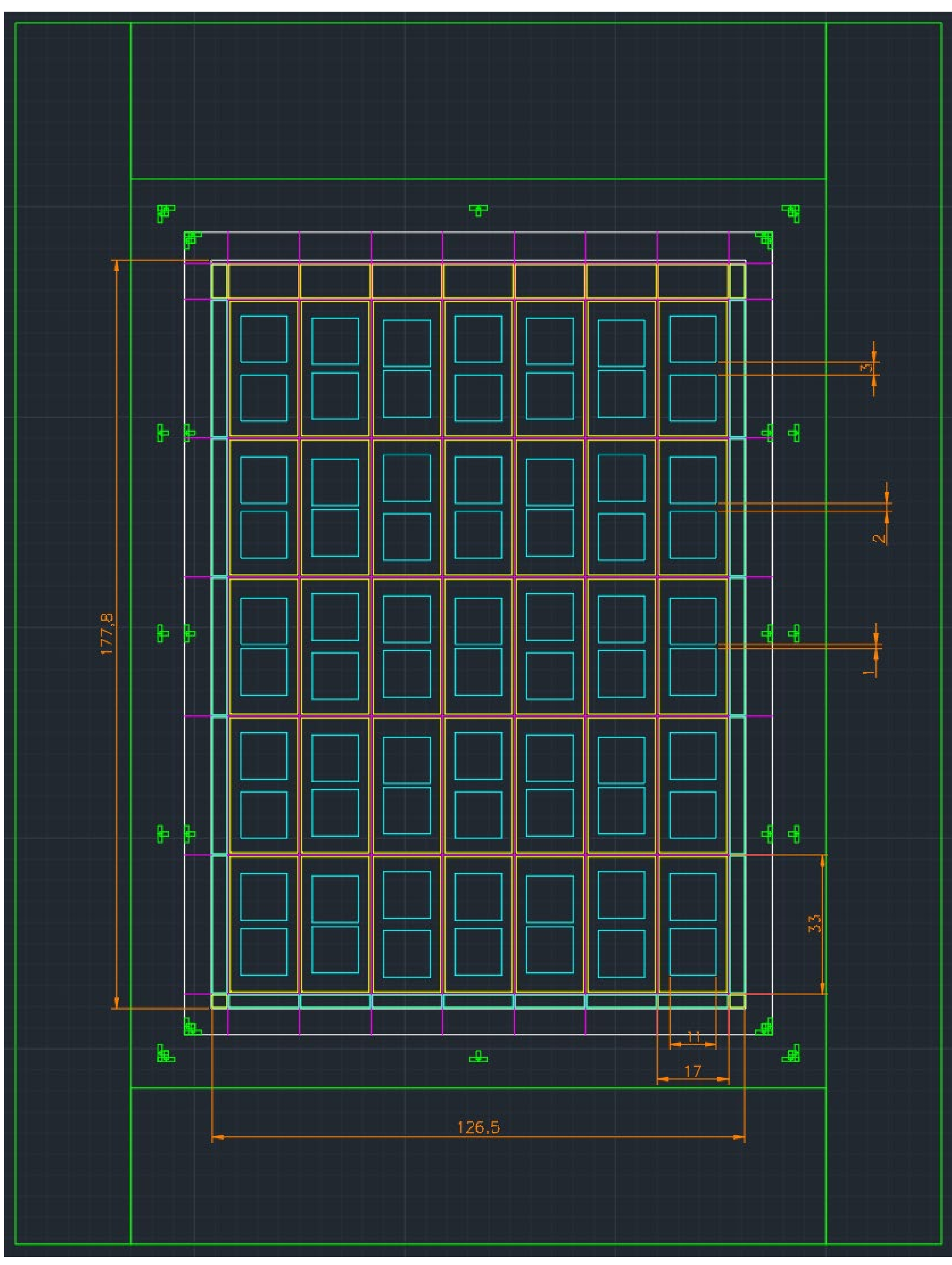


Figure 122. AutoCAD drawing of all layers of the patterns including top side copper, bottom side copper, and dicing lines.

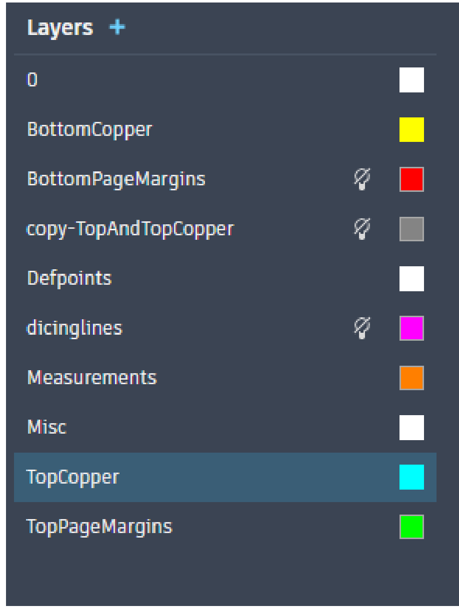


Figure 123. Color legend of all the layers of the DBC pattern design in AutoCAD.

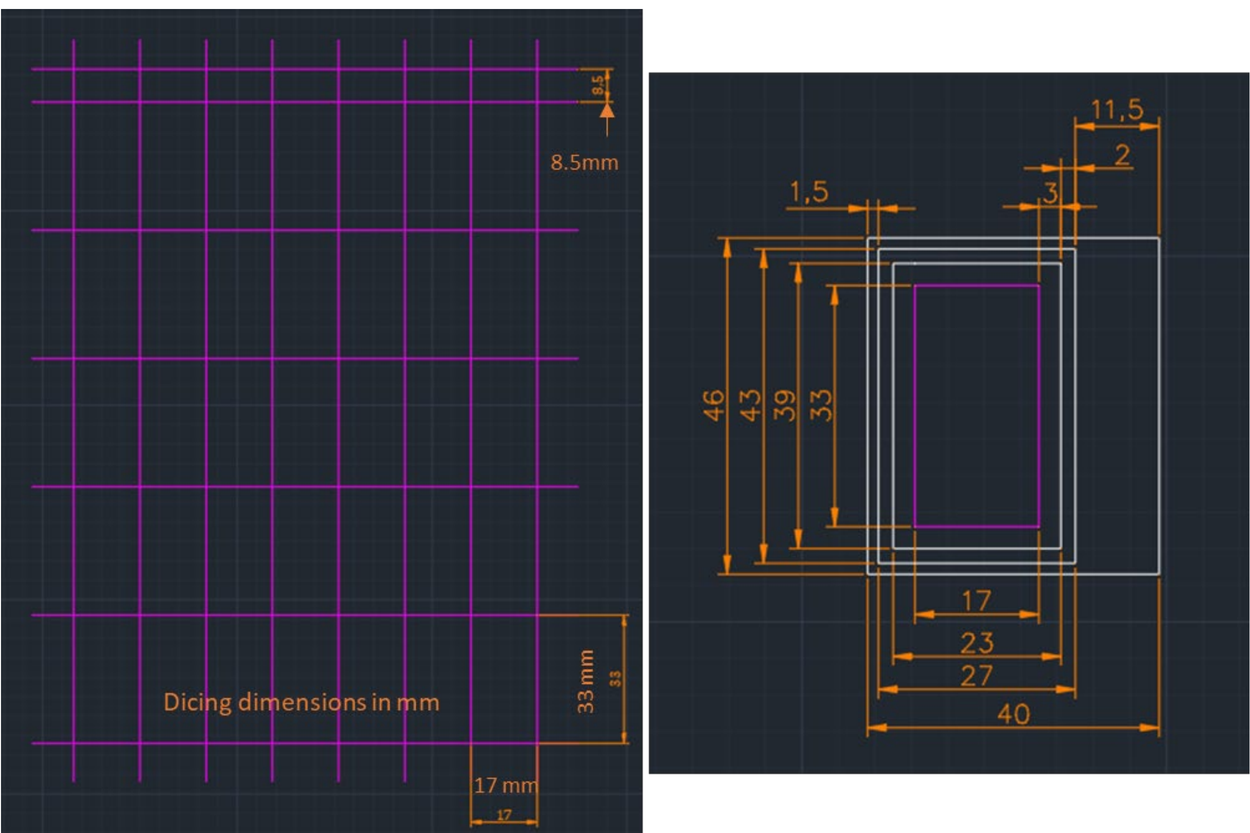


Figure 124. Dicing lines of the DBC master card (left) and dimensions of an individual diced sample in the context of the assembled sample (right).

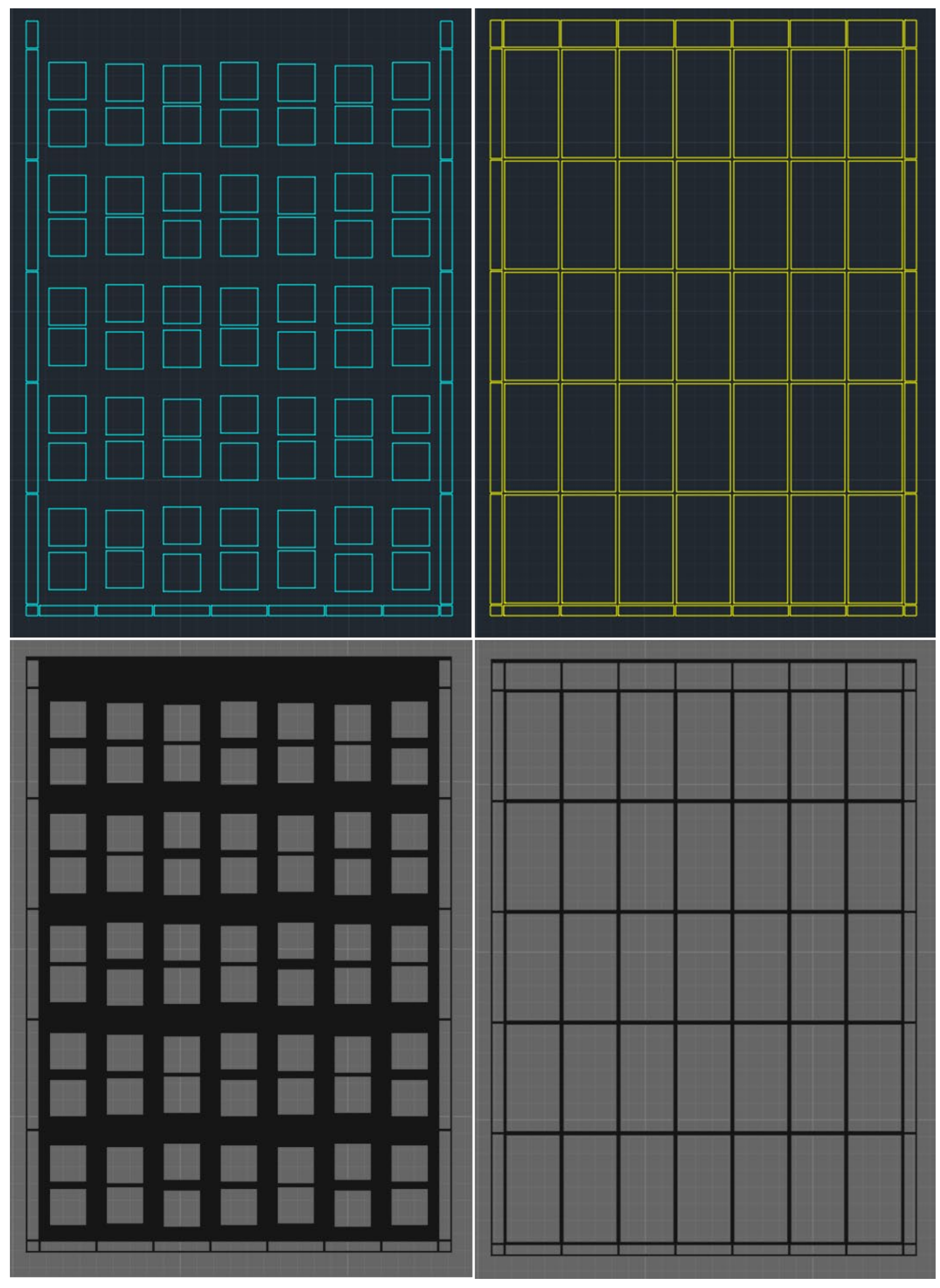


Figure 125. Top copper layer (blue) and bottom copper layer (yellow) outlines in AutoCAD with corresponding hatches where copper is to be removed.

H.2 FR4 baseboard space budgeting

Single-sided copper clad FR4 was used to provide connection to the backside of the DBC sample in a way that the terminal could still be placed facing up, instead of sticking out the back and needing additional mechanical support for keeping the sample upright, and to avoid a complex gel application and curing process. Five single-sided copper clad FR4 boards were obtained that were roughly 9” x 6” in size (exactly: 226 mm x 152 mm). Each board was divided up to fit as many individual (40 mm x 46 mm) copper base board samples as possible as shown in Figure 126. This was done in AutoCAD. A 1 mm gap was left between the samples to accommodate the blade size during the cut.

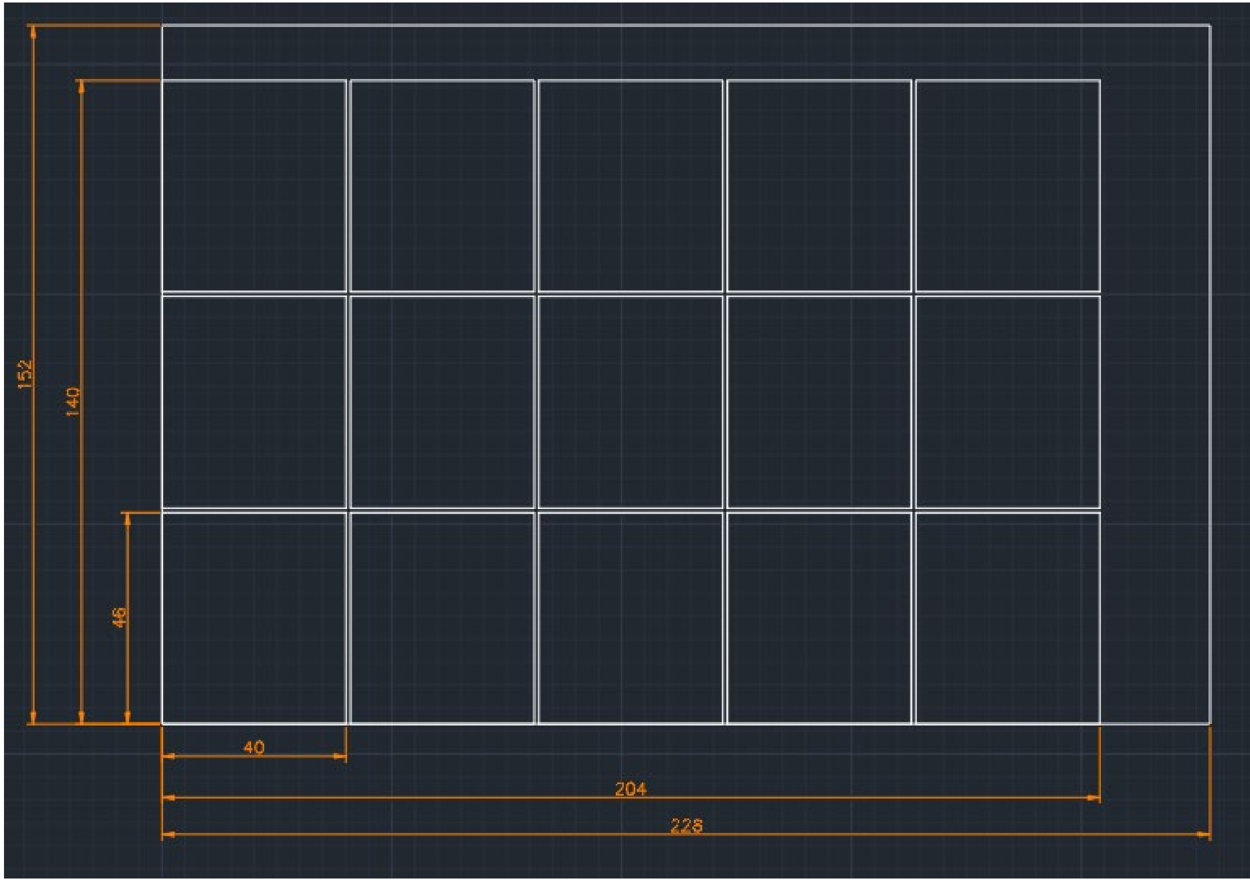


Figure 126. Space budgeting and dimensions of FR4 copper baseboard samples on a copper clad FR4 master card.

H.3 Housing design in SolidWorks

The encapsulating gel that covers the trace gap is a high viscosity fluid that needs to be contained until it can be cured into a solid phase. A well was designed for this purpose that would hold this liquid. The four walls of the well would sit on top of the copper baseboard and it would surround the DBC sample with a 3 mm gap between the edge of the DBC and the well wall. Since the encapsulant curing temperature is 100C, the walls can be made of ABS plastic, a common material used in 3D printers. The walls were made 2 mm thick to allow enough surface area to stick to the copper-FR4 baseboard and prevent too much bending. The simple STL file was designed in SolidWorks with dimensions as shown in Figure 127.

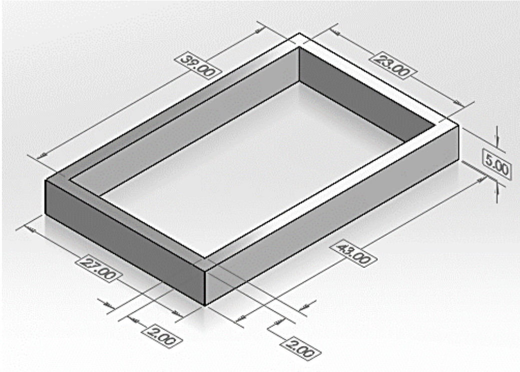


Figure 127. Dimensions of encapsulant gel containment box designed in SolidWorks for 3D printing.

Appendix I: Test Structure Fabrication and Assembly Instructions

I.1 Preparation of FR4 baseboard for each sample

For the sample shown in Figure 21, single-sided copper clad FR4 boards were obtained and cut to the dimensions shown in Figure 126. The dimensions of the master cards were 6” x 9” with thickness of 0.007” or 0.18 mm. A Microlux Mini Tilt Arbor Table Saw as shown in Figure 128 was used to cut the FR4 boards to dimension with a 1 mm tolerance.

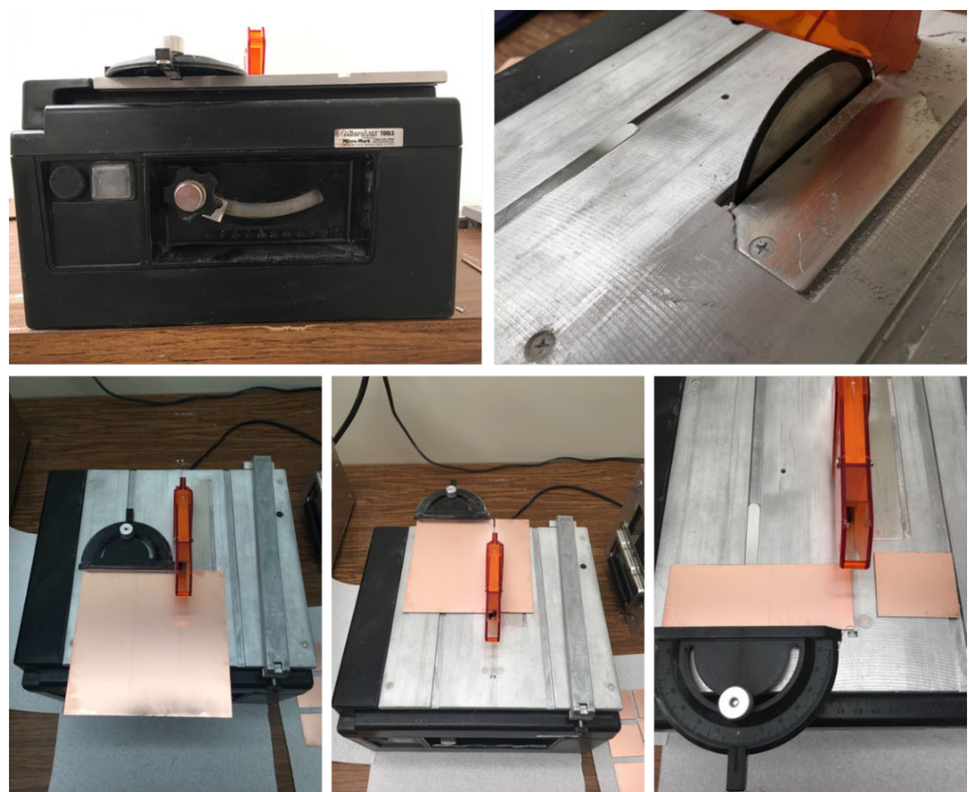


Figure 128. FR4 cutting saw

Once cut, the saw dust was cleaned off the samples. Then a vernier caliper was used to mark the location and dimension where the DBC would be attached onto the FR4 (Figure 129). Once marked, these samples were stored until the DBC test coupons were ready to be attached. A total of 60 samples were cut keeping a few extra for contingency.

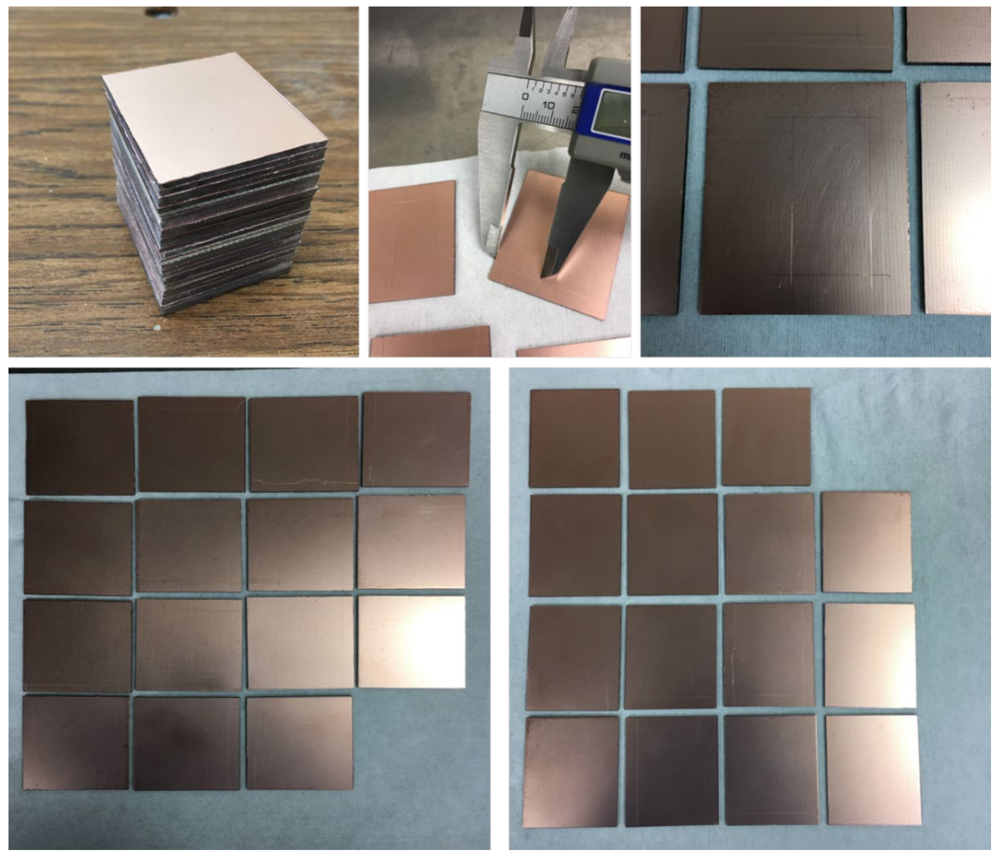


Figure 129. FR4 baseplate after cutting and while marking.

I.2 Patterning and etching of DBC test samples

DBC substrates were bought from Remtec. Three 12/25/12 mil copper-alumina-copper DBC master cards were bought. The design pattern shown in the photoplots in was etched on these substrates using a Chemcut machine where ferric chloride selectively etched the copper metal on both sides without affecting the alumina ceramic. The places where copper was not to be etched was protected by a dry film. Dry film photolithography was used to develop the dry film to stick only to the places where copper was to be protected from the etchant. After completing the etching process, the substrates were diced according to the dice line pattern in Figure 124 and the samples were stored for attachment to the FR4 base boards cut previously. Here are the detailed steps:

Step 1: Photomask printing

For this step, a printer that can print on photoplot paper was used. Photoplot paper is like plastic transparency sheet where one side has a matte finish and the other side is shiny. The AutoCAD design (Figure 124) of the copper layer pattern on both sides was printed on the matte-finished side of the photoplot transparency. Alternatively, this can also be printed by HiDEC staff. An image of the printed photomasks is shown in Figure 130.

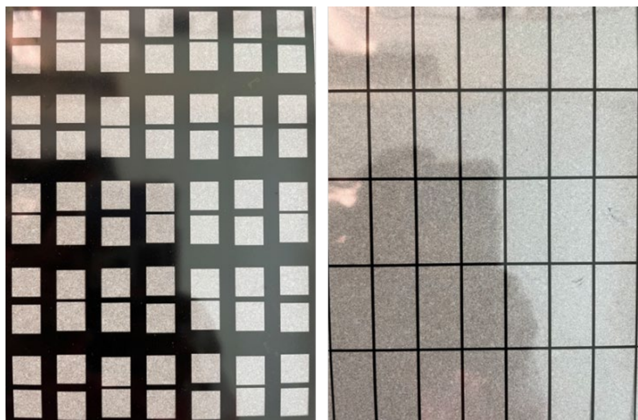


Figure 130. Printed photomasks top side (left) and bottom side (right).

Step 2: Equipment preparation

The Chemcut spray etcher (Chemcut 2315 Spray Etch System, Figure 131) needs about an hour to heat up. This is about how much time it can take to develop DBC master cards that need to be etched. So, it is a good idea to turn on the chemcut before starting the photolithography process. Before powering on the chemcut, check its water level in the back through the brown window. If it looks empty, fill it with water. Then, power on the chemcut by pressing the START button. The control panel of the Chemcut is shown in Figure 132. Press the ETCH PUMP ON/OFF button to toggle the etch pump on. Check the upper and lower spray pressure gauges to ensure they are above 30 psi Figure 133). If not, contact the staff. Press the ETCH HEAT ON/OFF button to turn on the heat. Set ETCH TEMPERATURE to 125 °F.

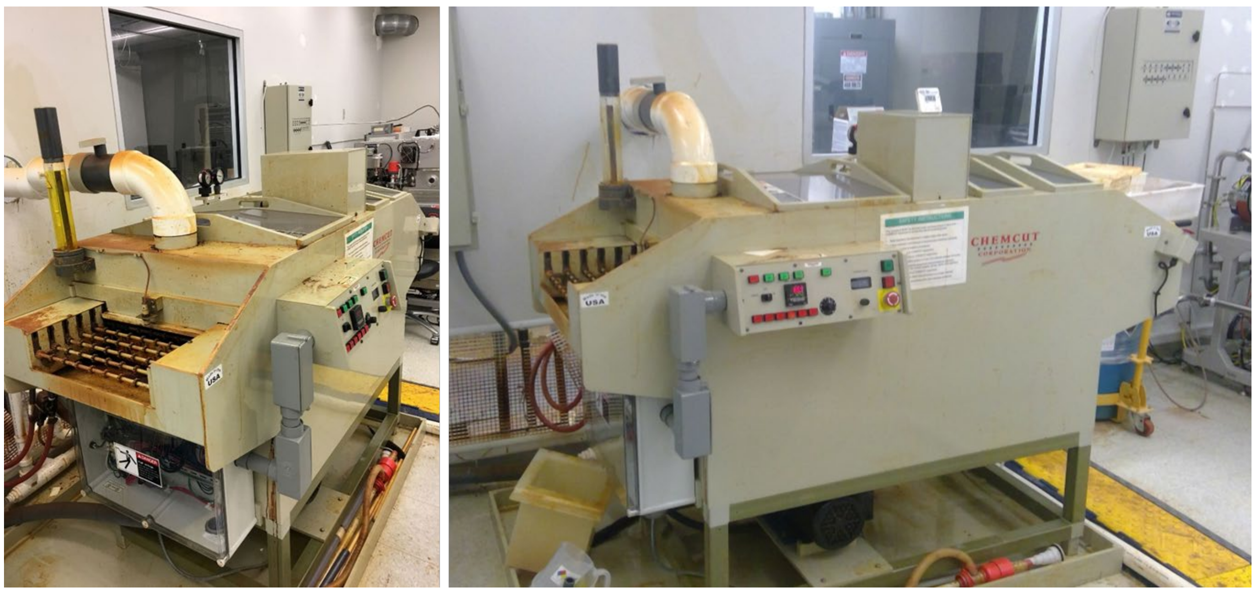


Figure 131. Chemcut Spray Etcher conveyor view (left) and control panel view (right).

Figure 132. Chemcut spray etcher control panel

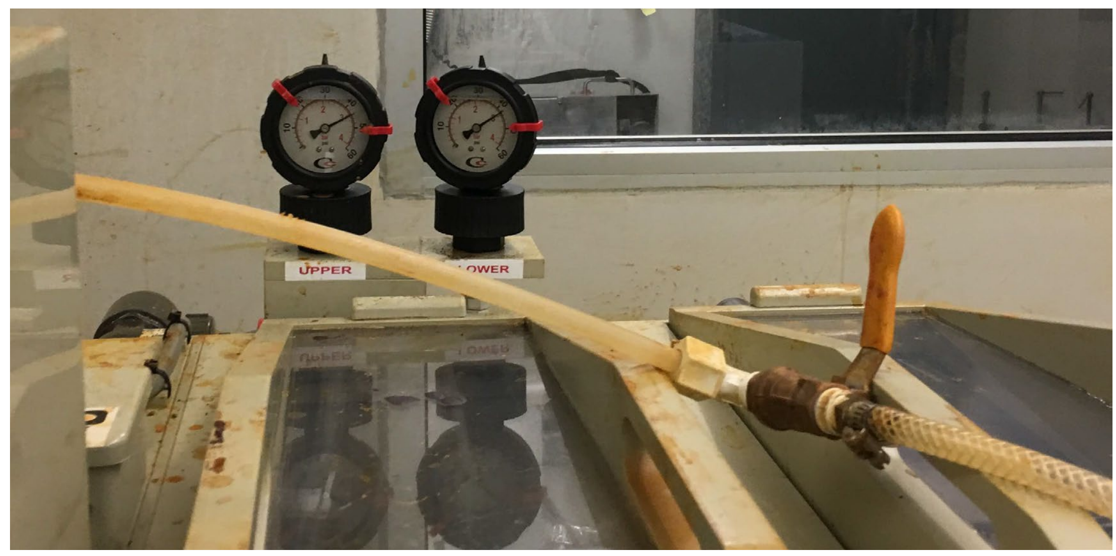


Figure 133. Pressure gauges for the chemcut.

Figure 134 shows images of the Exposure unit in the photolithography lab. The Exposure unit needs to be stabilized before it can be used. Press the POWER button. Place the whiteboard in front of the exposure unit (right-most image in Figure 134). Leave it for 20 minutes to stabilize. After 20 minutes check the light intensity in the exposure unit using the meter in the exposure bay. To do this, close the lid, disengage the timer by placing all toggle switches down, then press the EXPOSURE button. The light intensity should be 0.2 mW.

Figure 134. UV light exposure unit (left), its control panel (middle), and the top glass with lid open and whiteboard in front (right).

Figure 135 shows the dry film laminator. To prepare the laminator, remove the laminator lid and check the rollers for any obstructions like loose paper, etc. Press SWITCH ON button in the back of the laminator to power it on. Press the PREHT button to start heating the laminator. Use the temperature control UP button to set the temperature to 100 °C. It takes about three minutes to warm up. Use the speed control button to set the speed to “2” by pressing the “2” button.

Figure 135. Laminator with its cover on (left) and off (right).

Obtain chemicals and equipment needed for developing and stripping the photoresist. This includes the two-gallon container of “dry film developer,” the two-gallon container of “dry film stripper,” the development tank with agitator and the stripper tank with agitator. Don’t pour the liquid into their respective tanks yet but keep them nearby.

Step 3: Dry film photoresist lamination on DBC master card

Before laminating the DBC master cards, they must be cleaned using IPA solvent and dried using lint free towels. Leave the cards to stand for a couple of minutes before laminating.

Figure 136 shows the three-layer dry film and Figure 137 shows the laminating process.

Place the DBC board on brown paper as shown in the image on the left. Cut out dry film in a size slightly larger than the DBC with some margin on all sides, similar to the size in the image shown on the right. The dry film has a sticky side and a not-sticky side. Both sides are protected by a thin sheet of plastic. Using tweezers, remove the plastic covering from the sticky side and throw the cover away.

Figure 136. Dry film photoresist structure.

Figure 137. The laminating process.

Check roller temperature by pressing the MEAS button and ensure it is at 100 °C. If not, wait till it gets to 100 °C. Check the exit temperature of the laminator and ensure it is between

40-50 °C. If not, re-calibrate roller temperature and speed. Gently place the dry film sheet on top of the DBC that is on top of the brown paper, with the recently exposed side (the sticky side) of the dry film facing down, touching the copper. Feed the brown paper – substrate – dry film sandwich through the laminator and hold onto the dry film layer at the bottom end as shown in the figure on the right to prevent wrinkling. When the substrate sandwich comes out the other end, cut out the excess dry film – brown paper sandwich around the substrate, and remove the brown paper. Repeat the lamination process for the other side of the substrate. Normally, the dry film and the brown paper are loaded onto the rollers. But in this case, they were fed manually. Let the laminated DBC cool to room temperature over 15-20 minutes before exposing it to UV light.

Step 4: Ultraviolet (UV) exposure

Check light intensity to ensure it is at 0.2 mW. If not, do light exposure test to figure out the correct time setting. Cut the photomask to the size of the DBC with enough margin to align top and bottom sides. Align the top and bottom sides of the photo mask to the substrate using alignment marks as necessary. Ensure the printed side of the photomasks face down and touch the dry film layer. Attach the two photoplots using small pieces of tape on the edges of the photoplot. Check alignment of top and bottom patterns and the edge of the copper and ceramic layers of the substrate. Clean the glass of the exposure unit. Place the substrate face down on the glass and close the lid. Engage the timer by using the toggle switch and set a timer for 2.5 minutes. Press EXPOSURE button and cover the exposure unit with white board to avoid UV exposure. After the timer runs out, press the EXPOSURE button again and open the lid. Flip the substrate to the other side and repeat the exposure process for another 2.5 minutes (or 5.0 minutes if there is no pattern). Take the substrate out of the exposure tower and press POWER to

turn off the exposure tower. Remove the photomask and leave the substrate for 20 minutes. Finally, remove the protective cover from the dry film using tweezers as shown in the left side of Figure 138. The top and bottom patterns are now transferred to the dry film photoresist as shown on the right of Figure 138. Note that the pattern shown is different from that in the photomask made for these experiments because photos of that process were not taken, but it is the same as the process depicted here, which was taken for other test samples built previously.

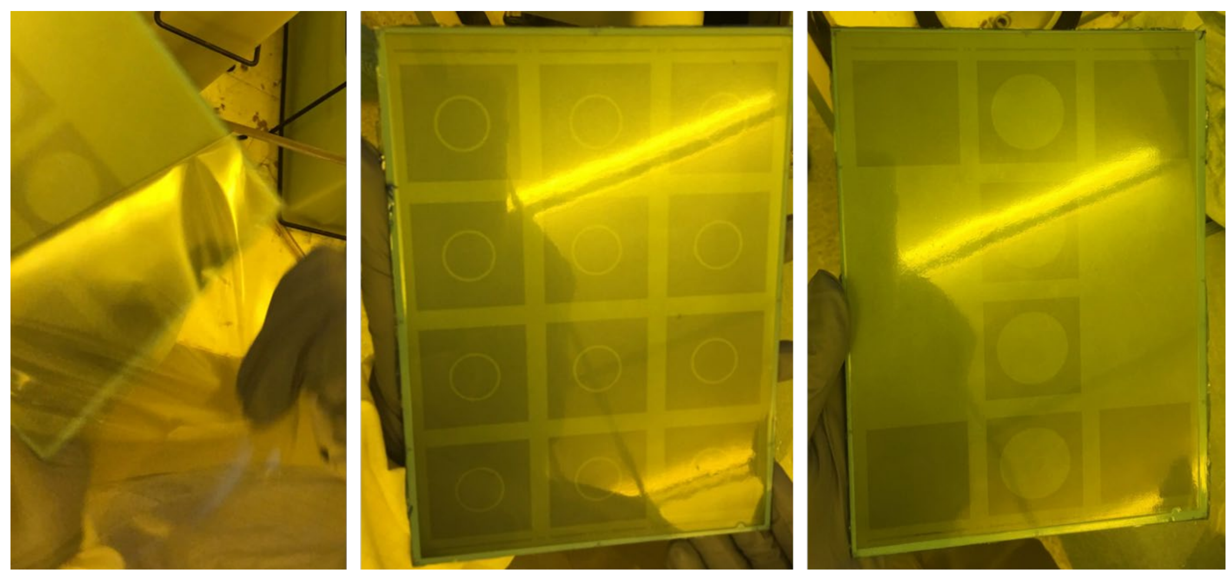


Figure 138. Dry film cover removal post exposure and before development.

Step 5: Dry film development

Since the dry film is a negative photoresist, the parts that were exposed to UV light are not soluble in the developer solution. The photolithography process for a negative photoresist is summarized in Figure 139.

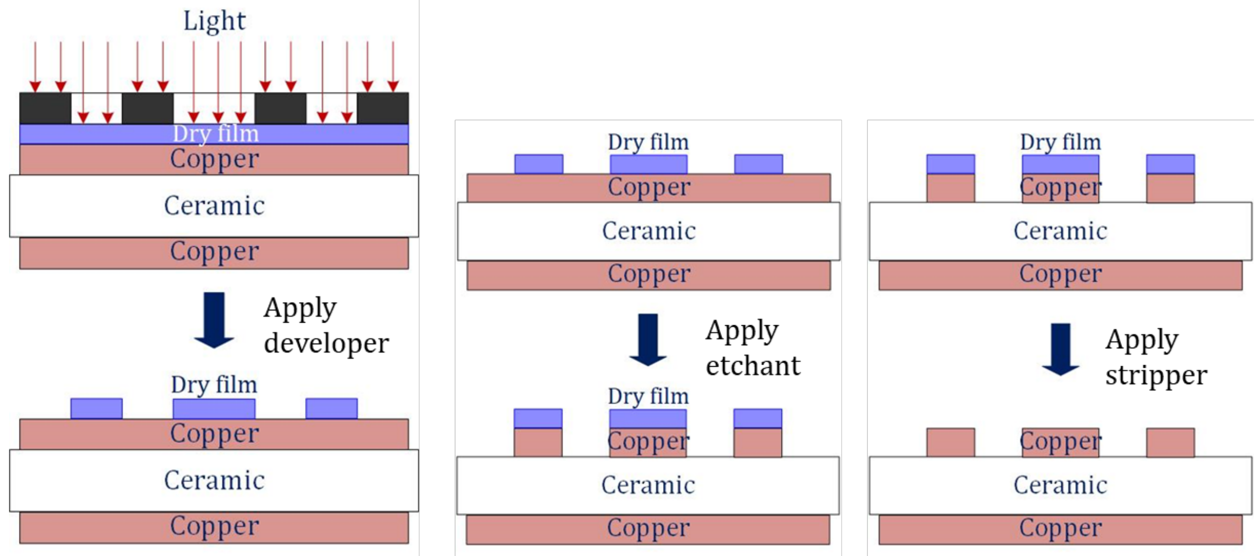


Figure 139. Dry film negative photoresist photolithography process. Image credit: Yuxiang Chen. Used with permission.

To develop the dry film, pour developer solution into the appropriate tank (labelled "D" for developer, as opposed to "S" for stripper) as shown in Figure 140. Insert the agitator tube and turn it on. This will insert bubbles to help stir the solution and expedite the development process.

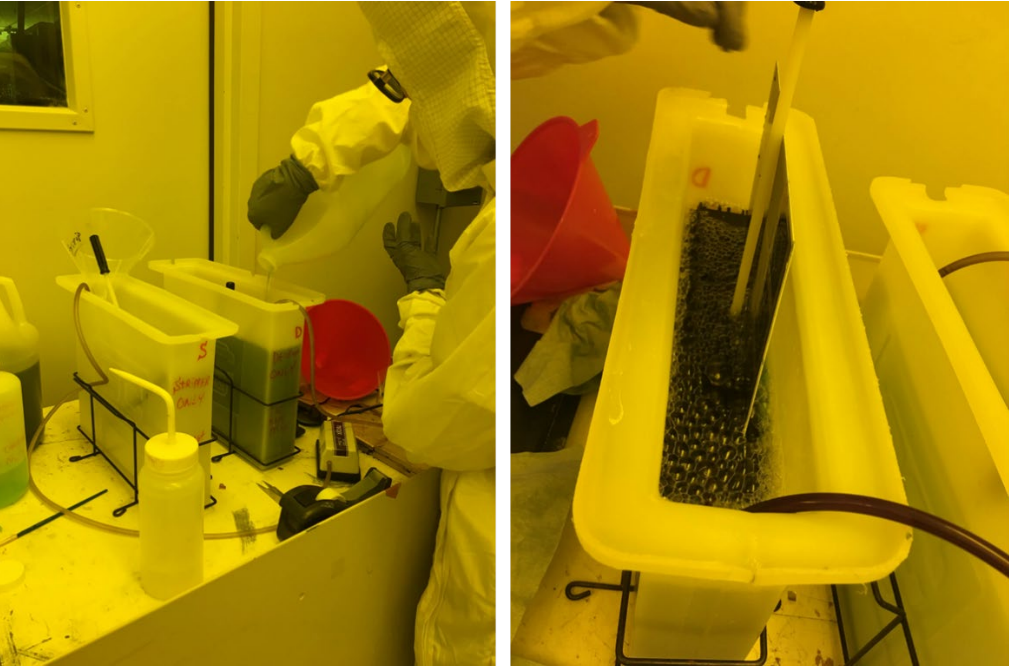


Figure 140. Development process: pouring developer solution into the tank and inserting the substrate into the tank.

After about four minutes in the tank, lift the substrate out using the plastic holder and inspect: the blue dry film should be removed from the areas to be etched. This is shown in Figure 141 where it is ready to be inserted into the Chemcut for etching the copper in regions not covered by the blue dry film photoresist. If after four minutes, the dry film is not rinsed away, keep it in the developer solution for up to a total of seven minutes. Rinse and dry the substrate before etching. Place the developer solution back in its container using the funnel and disconnect the agitator.

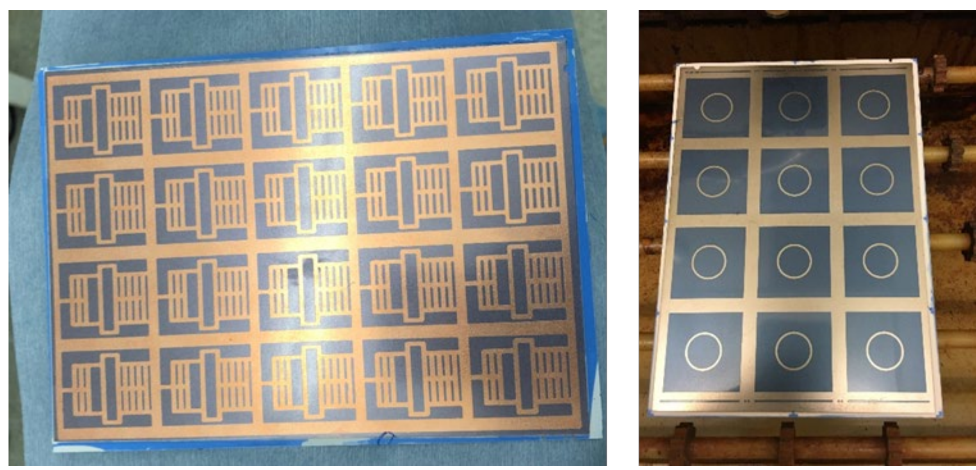


Figure 141. After development: all the blue film from the non-copper regions are rinsed away.

Step 6: Copper etching

The instructions here are to be used as guidelines. The standard operating procedure for using the Chemcut should be obtained from the HiDEC staff or on the HiDEC sharepoint site. Once the Chemcut has reached 125 °F, turn on the two valves of the rinse water in the chase way in the back (corridor behind the Chemcut room, Figure 142). Press RINSE WATER INLET ON/OFF button, OSCILLATION ON/OFF button, and set oscillation to 7 on the control panel. Turn RUNOUT switch from OFF to ON. Set conveyor speed to etch a fourth of the copper thickness per pass. The conveyor speed is measured in inches of copper etched per minute. A conveyor speed table is provided for reference (Table 23) but these should only be used as an

estimate, and the user should test out the etch rate themselves.

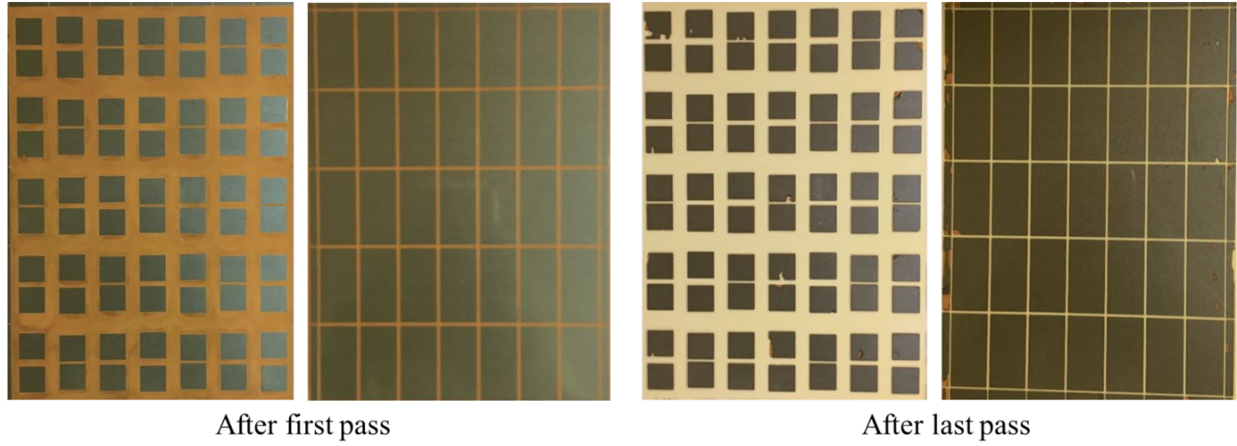
Figure 142. Valves to be opened in the chase bay behind the chemcut.

Table 23. Etch rate for Conveyor speed of the Chemcut spray etcher

Conveyor speed (in/min)	Etch rate (mils/pass)
35	0.5
20	1.0
15	1.5
12	3.5
10	3.35

Place DBC on the conveyor rollers and wait for it to go in, making sure its motion was not obstructed. Then wait for it to come out the other side. This may take 1-2 minutes. When it comes out, carry it back to the entrance end of the conveyor and place it in a way that it is flipped to the other side (flip horizontally) and rotated ninety degrees. This ensures all sides are most evenly etched. Once the substrate comes out at the other end, repeat the process until the copper is etched away and ceramic can be seen. Figure 143 shows a sample of the etching process after

the first pass and the last pass. At any point in the process (when the substrate is not inside the chemcut), the substrate can be rinsed, and its copper thickness checked and conveyor speed adjusted as needed. When completed, turn RUNOUT switch from ON to OFF. Press RINSE WATER INLET ON/OFF button, OSCILLATION ON/OFF button, ETCH PUMP ON/OFF button, ETCH HEAT ON/OFF button, and finally the STOP button. Close the valves that were opened in the chase bay. Rinse the substrate and transport it back to the photolithography lab to strip the dry film photoresist that remains.


After first pass

After last pass

Figure 143. DBC etching: after first pass through the chemcut spray etcher (left) and after the last pass through the etcher (right).

For the substrate used, the etching process was not perfect as can be seen in Figure 143. Some of the trace islands have copper etched off them resulting in little notches. This could be due to the dry film not adhering to the substrate during the development process, or the dry film peeling off on the rollers of the Chemcut. This is why is helpful to fabricate more samples than needed to compensate for fab-related losses. Since two substrates were etched and diced to get coupons, there were enough samples to do the required statistical analysis. The defected samples (especially where the trace gap was affected) were discarded.

Step 7: Dry film stripping

Pour the stripper solution into the stripper-only marked tank Figure 140. Connect the agitator and turn it on. Place the substrate on the plastic holder and insert it into the tank. Wait until all the dry film is removed. Disconnect the agitator from the hose and unplug it. Rinse and dry the substrate. Transfer the stripper solution from the tank back into its container using the funnel that is designated for the stripper solution. Since the next step (dicing) is in a different lab, cover the substrates in lint-free wipes, place them in an airtight container and transport it to the other lab and store the patterned substrates in a nitrogen box if they are not being diced right away. Figure 144 shows a summary of the photolithography process with an example test substrate's photomask, its pattern on the substrate after UV exposure and development, and finally after etching and resist-stripping is completed.

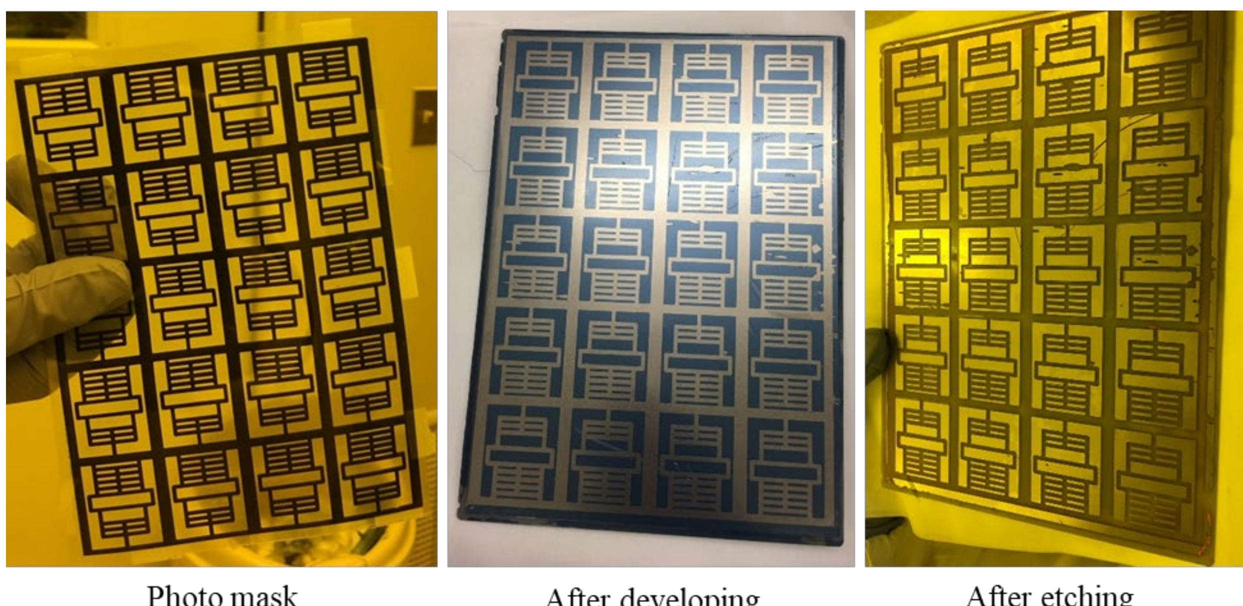


Figure 144. An example test substrate at various stages of the dry film photolithography process.

Step 8: DBC master card dicing into individual test coupons

The substrates were sent to Errol Porter, HiDEC staff, for dicing. Pictures of the substrate with dicing lines were also sent. The dicing equipment is shown in Figure 145 and some images

of dicing previous samples are shown in Figure 146 and Figure 147 and explained briefly here. The instructions here are to be used as guidelines. The standard operating procedure for using the wafer and DBC Dicing equipment should be obtained from the HiDEC staff or on the HiDEC sharepoint site.

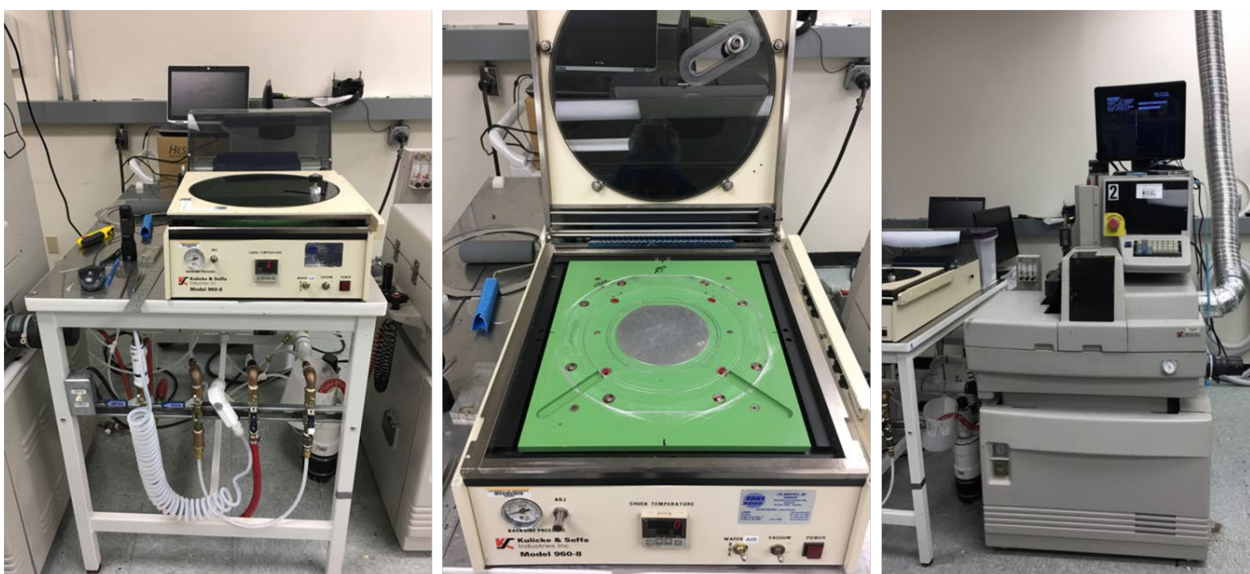


Figure 145. Kulicke & Soffa wafer mounting chuck (left and middle), and dicing machine (right).

The wafer, or in this case the DBC substrate, is mounted on the mounting chuck with the side that has the dicing marks or alignment marks facing down on the vacuum chuck. A metal frame is placed around it and a laminating sheet is applied over both the substrate and the metal frame with it adhesive side facing the substrate (Figure 146, left image). Once secured, a roller is used to roll out any bubbles between the lamination sheet and the metal frame and substrate. The excess lamination is cut away using a blade around the edge of the metal frame. To release the substrate-frame from the mounting chuck, vacuum is removed, and the frame-substrate-lamination is lifted off and mounted on to the dicing machine, aligning the notches of the metal frame to the appropriate notches on the dicing table, keeping the blue sheet side down and the

substrate on the top. The sample is “loaded” onto the dicing machine chuck by applying vacuum. Next the substrate is “aligned” by subtly adjusting the rotation and movement of the table by watching the microscope screen and aligning the crosshairs to parallel edges or alignment marks on the substrate (Figure 146, right image). The machine can run through the cut sequence without cutting but showing the cut location on the screen. This should be used to validate that the cut line is as desired. When using a ceramic-only blade, one must ensure the cut line is not going over any metal parts. If metal and ceramic need to the cut, the appropriate blade for that purpose should be used. It is typically advised to cut either metal or ceramic and not both. The left side image of Figure 147 shows the various types of blades available for dicing. Next, the blade (or crosshairs on the screen) is positioned at the location where the cut will begin. Finally, the substrate is “cut” or diced. The right side image in Figure 147 shows an example cut made by the machine on a smaller substrate.

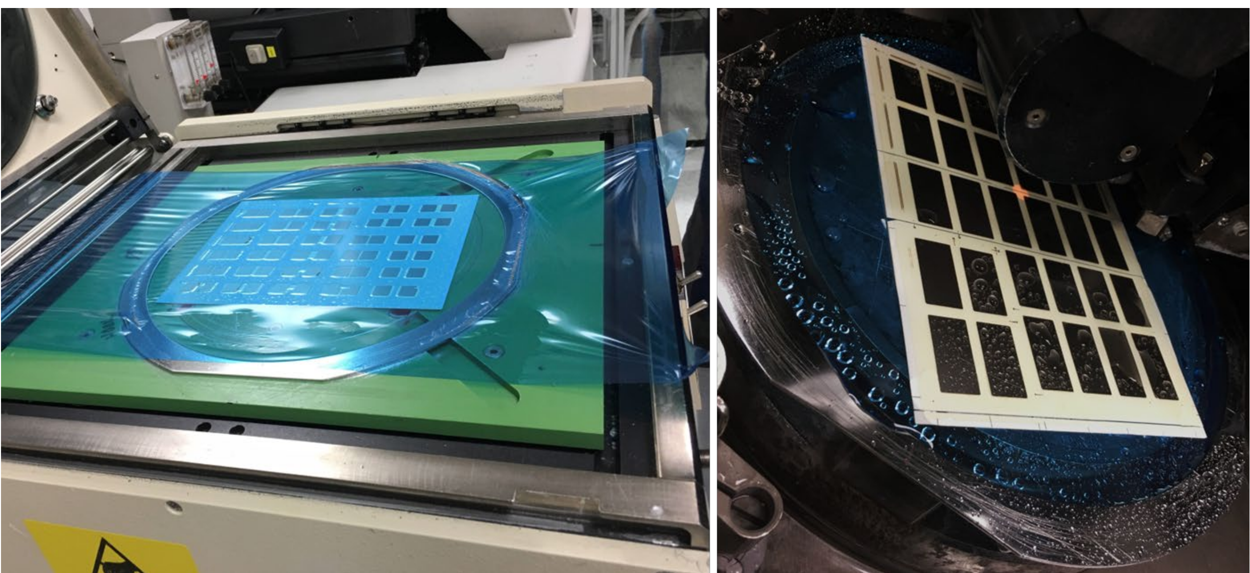


Figure 146. Substrate mounting on lamination sheet (left) and substrate alignment on dicing table (right).

For periodic patterns, equidistant offsets can be set to automate all horizontal cuts and then all vertical cuts. For more complex patterns, all lines need to be cut individually. Note that the dicing machine always cuts all the way from one side to the other. It can not stop the dicing process in the middle of the substrate. This must be kept in mind when designing the DBC dicing pattern in AutoCAD.

Once the substrate has been diced, the machine is turned off, the blade is removed and placed back in its correct location as shown in the grid inFigure 147, the metal frame with the blue laminate and substrate is released from the vacuum of the chuck. If it were not for the stickiness of the laminate, the diced samples would pop off when vacuum suction is released and fall to the ground or inside the dicing machine and likely break and litter. The frame-laminate-substrate is removed from the dicing machine and placed on another chuck where the samples are gently peeled off the sticky blue laminate. The best diced samples are shown in Figure 148.

Once removed, the test coupons or samples can be stacked and stored in a nitrogen box for the assembly process where they would be attached to the FR4 pieces cut in the previous section. The laminate can be thrown away and the metal frame returned to the wafer mounter.

Figure 147. Dicing saw blades used for cutting various types of substrate materials (left) and ceramic substrate being diced by the appropriate blade in the dicing machine (right).

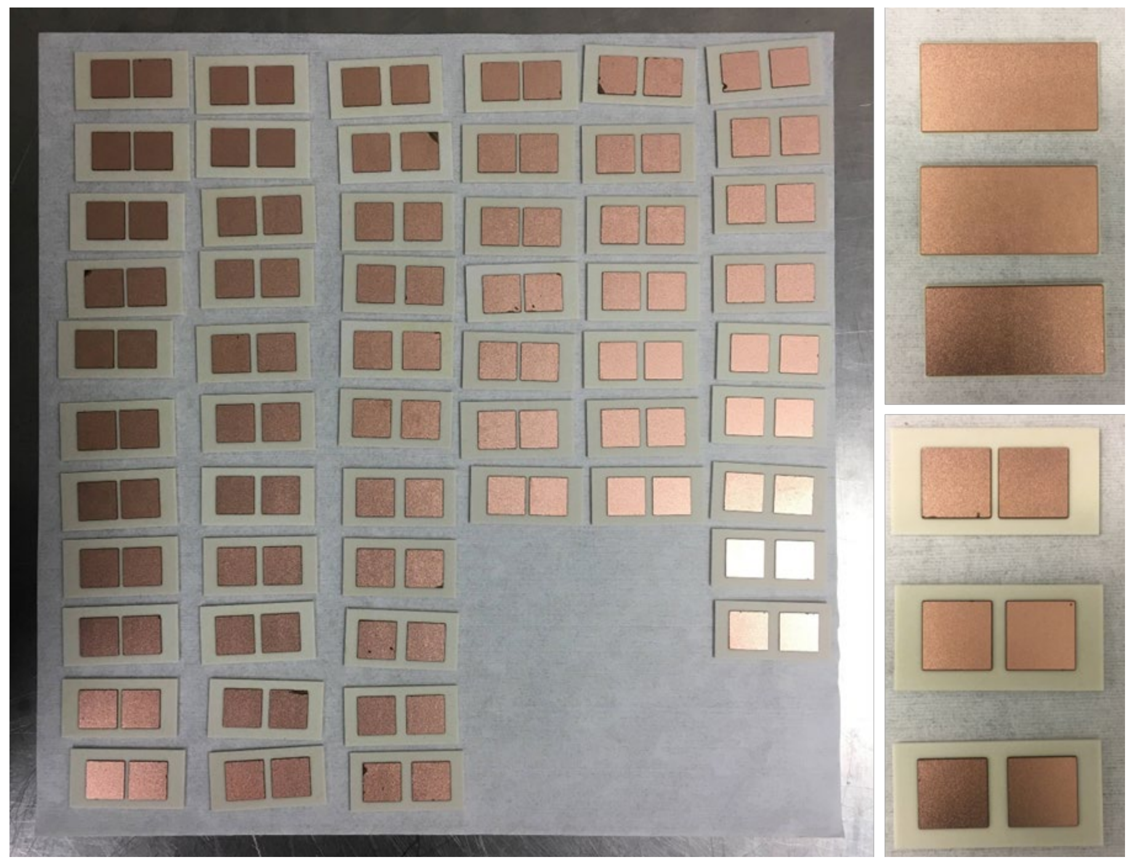


Figure 148. The best of the diced samples.

I.3 Attachment of base and terminals

Attachment was done using silver epoxy AA-DUCT AD1 by Atom Adhesives [106]. Before the FR4 baseboard pieces and the DBC pieces could be assembled, they had to be cleaned to remove any organics and oxides present on the bonding surfaces that would prevent good adhesion. First, they were cleaned using acetone and IPA and dried. Then, they were transported in an airtight container with desiccant and lint free towels to another clean room where the plasma cleaner was. The silver epoxy was also taken out of the fridge to thaw while the cleaning would take place.

The plasma cleaner used was from Diener Electronic. Figure 149 shows the equipment. The top left image is the gas flow controller box, the top right images show the oxygen and argon valves, and the image at the bottom is the pressure controlled cleaning chamber. Each type of substrate needs a full cleaning cycle, and each cleaning cycle includes cleaning with oxygen which removes any organics from the sample surface, but it creates an oxide layer in the process, and cleaning with argon which strips any oxide layers from the previous step or earlier.

Figure 149. Diener electronic plasma cleaner (bottom) and its flow controller (top) and argon and nitrogen valves (right).

The plasma cleaning chamber with various substrates in their cleaning sequence is shown in Figure 150 with each step labelled, where “A” represents oxygen cleaning and “B” represents argon cleaning. Oxygen plasma appears white in the chamber and argon plasma appears purple in the chamber. The FR4 samples were plasma cleaned first (1A and 1B), with the copper side up. It was run through ten minutes of oxygen clean (1A) and ten minutes of argon clean (1B). Next, the top side of the DBC coupons were cleaned (ten minutes under oxygen (2A), and 10 minutes under argon (2B)), followed by the back side of the DBC coupons (ten minutes for oxygen (3A) and ten minutes for argon(3B)). Finally, the terminals (or standoffs) were cleaned for ten minutes under oxygen (4A), followed by ten minutes under argon (4B). Detailed step by step instructions can be found in the instruction manual located next to the plasma cleaner in the

lab.

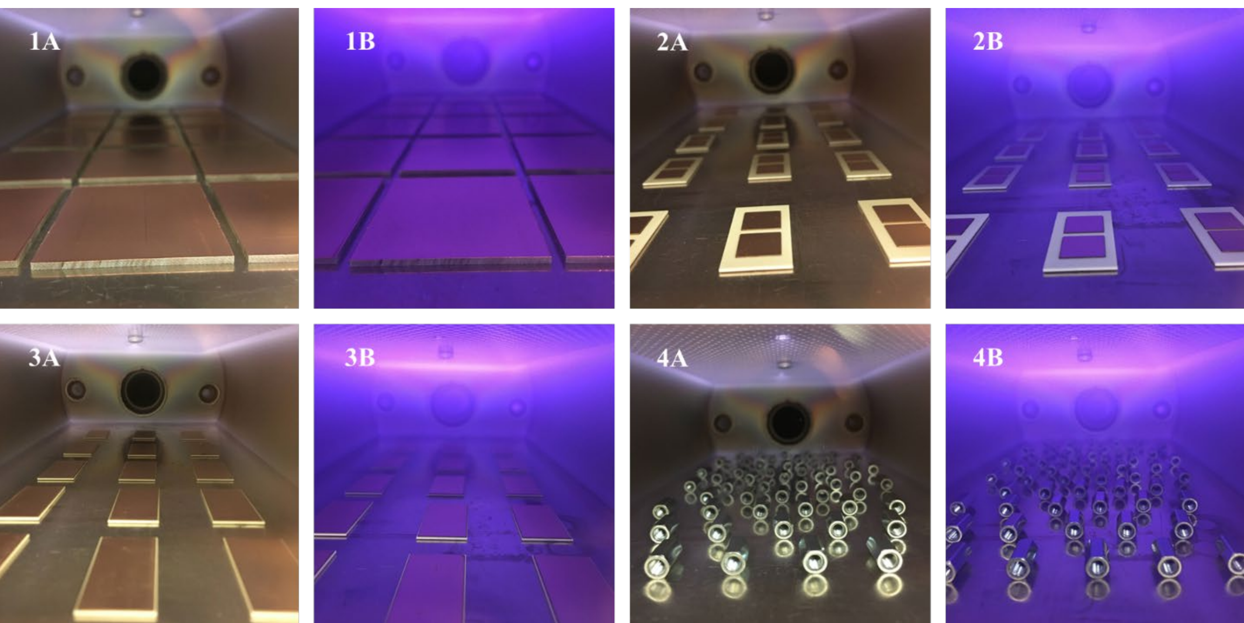


Figure 150. Plasma cleaning of subsrate surfaces and terminals.

As soon as the FR4 base board are plasma cleaned, the samples are carefully removed on to a towel where they are taped using cellophane tape according to the DBC location markings made earlier by the caliper to form a mask to protect the rest of the sample from the conductive epoxy. This is shown in Figure 151 (left). The silver epoxy syringe with attached nozzle tip is shown in Figure 152 (left). The epoxy is applied in a single line on one exposed end of the sample and then smeared using the flat head metal spreader shown in Figure 152 (right). After applying the silver epoxy, the samples look like that in Figure 151 (right). Then the tape is removed, and the samples look like that in Figure 153.

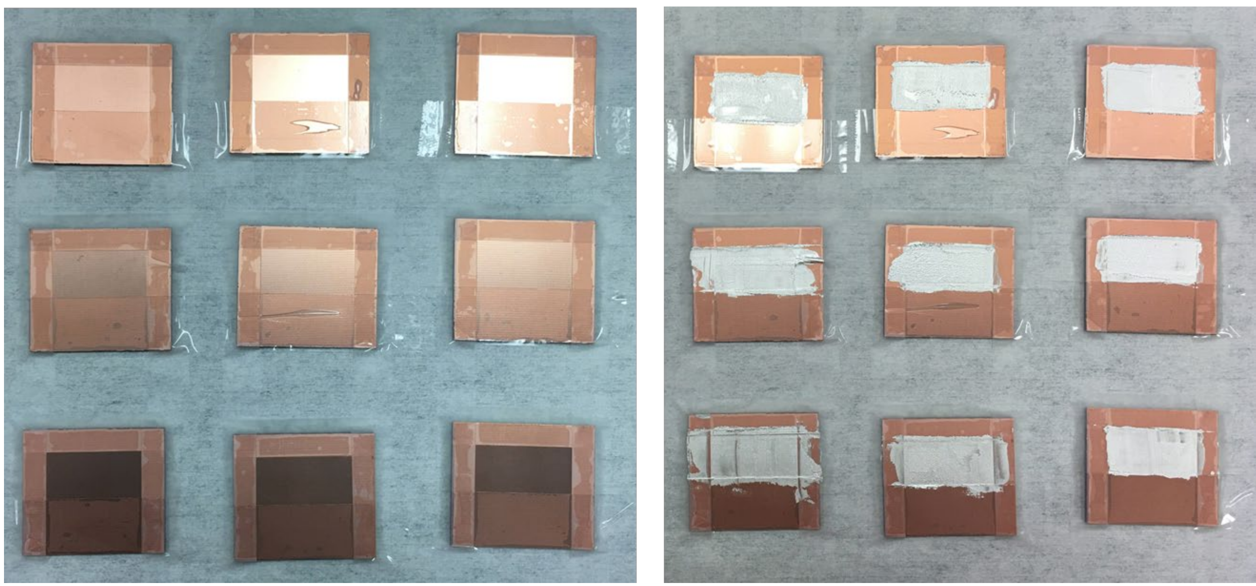


Figure 151. FR4 baseboards with tape mask (left), and with solver epoxy (right).

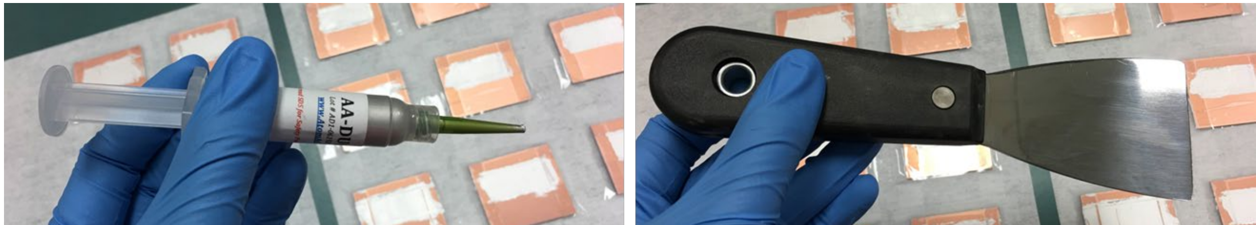


Figure 152. Silver epoxy syringe and nozzle tip (left) and flat ead spreader (right).

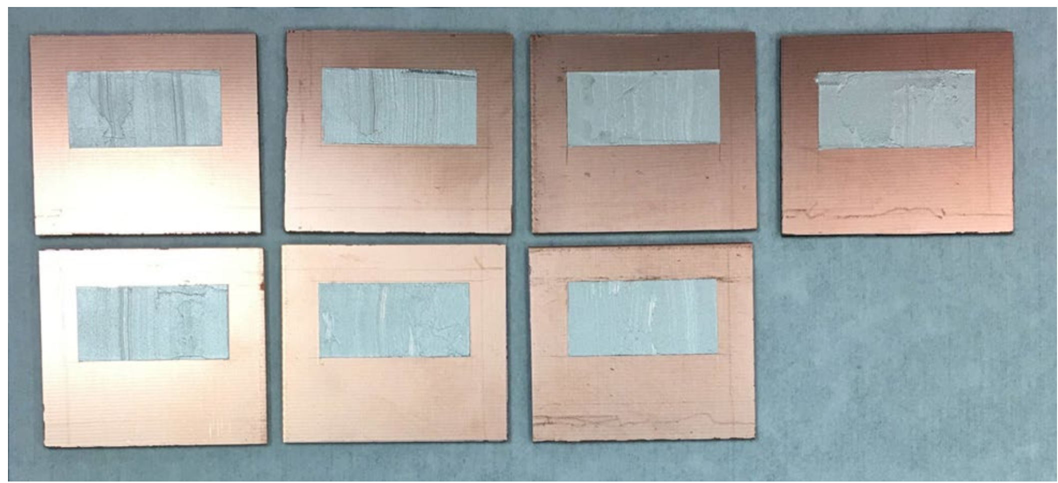


Figure 153. Masking tape removed from FR4 samples.

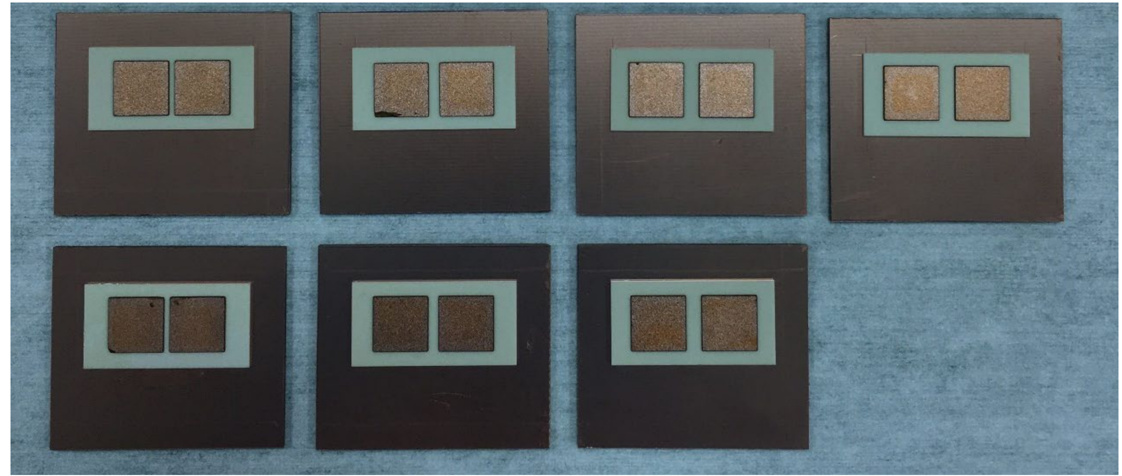


Figure 154. DBC substrates attached to FR4 substrates.

Figure 155. Terminals attached to DBC traces and FR4 base.

The DBC coupons are placed on the silver epoxy and aligned (Figure 154). Similarly, the standoffs are attached (Figure 155). Once the attachment positioning was made, the silver epoxy was cured. A Fisher Scientific Isotemp Vacuum Oven was used. The samples were baked at 200 °C for 42 minutes in a nitrogen environment. Figure 156 shows the positioning of the samples on the oven tray (left) where it was ensured that none of either 1, 2, or 3 mm samples were too close to the edge or the middle, but distributed throughout instead to even out any differences across the samples. Then the samples were mounted into the middle rack of the oven. The isotemp over

had to be preheated before the samples could be inserted. The oven is shown in Figure 157.

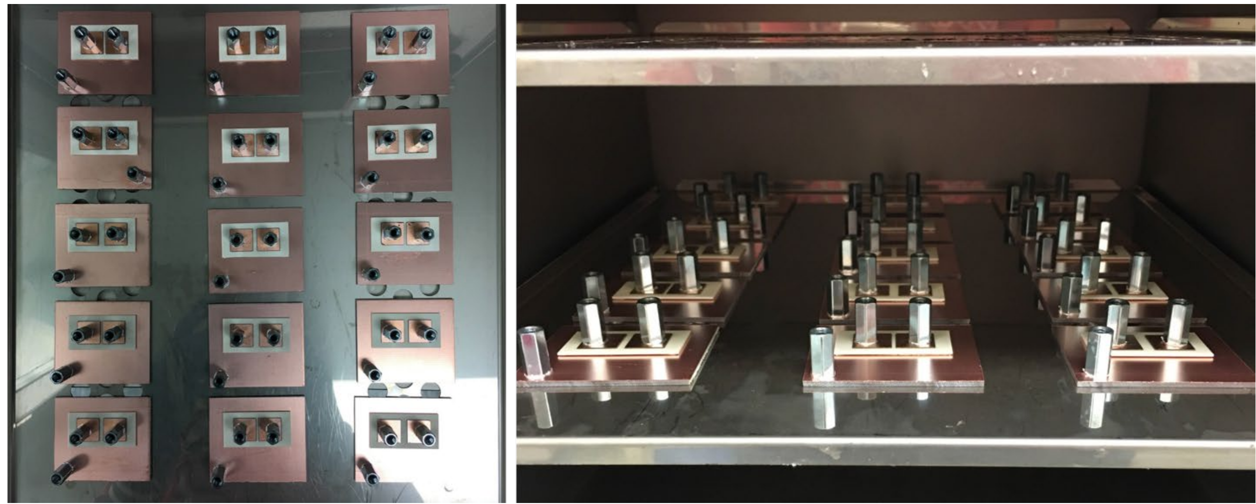


Figure 156. Samples positioned on oven tray (left) and mounted into the oven (right).

Figure 157. Fisher Scientific Isotemp Vacuum Oven.

After the cure schedule, the samples are carefully retrieved and placed on a bench, and they look as shown in Figure 158 (left). The copper color is changed but this is normal and doesn't affect functionality. Since only fifteen samples could fit in the oven at a time, they were baked in two batches of fifteen. After baking, the samples were stored in an airtight container

with desiccants and the container was placed in a nitrogen box. They were left in the container overnight. The container was specially chosen to keep the samples from colliding with each other using dividing walls. The samples' FR4 baseboard dimensions were also designed in a way that they would fit into this box. The box was obtained from Walmart's Sports and Outdoors section, and it is typically used to store fishing supplies and is airtight (Figure 158, right).

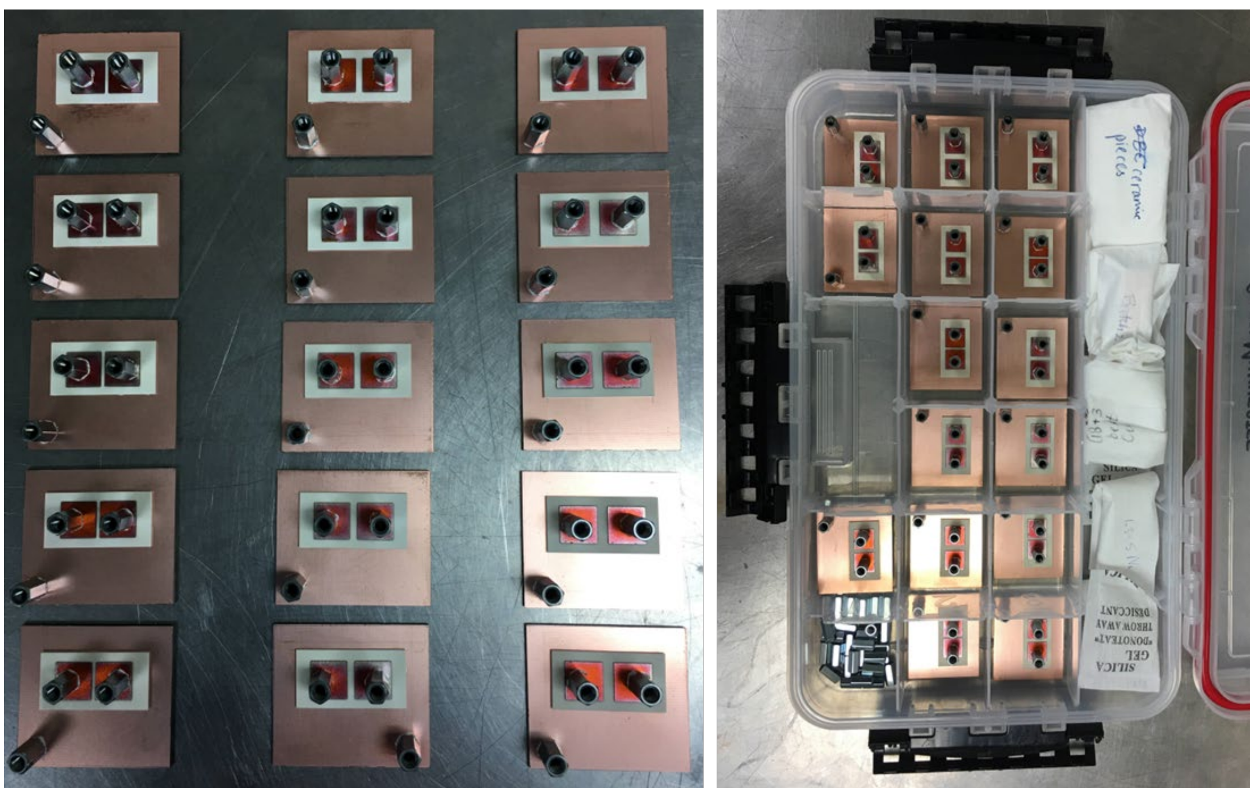


Figure 158. Sample after curing of silver epoxy (left), and after labelling (right).

I.4 Encapsulation of the trace gap and DBC with dielectric gel

Before the samples are encapsulated in gel, they need to be labelled so that they can be identified during testing (since PD is often an invisible phenomenon and a sample may look the same before and after testing, and one must use a fresh sample for best results). Labelling for the samples is shown in Figure 159. The number in the middle indicates the trace gap in mm. "DC" indicates the excitation profile. And the last two digits are the sample number for the trace gap.

Figure 159. Samples labelled.

Next, the walls of the encapsulant containment need to be 3D printed for each sample. Note that this step should be done before beginning the photolithography process for the DBCs to reduce the shelf life of all the processed substrates since the copper surfaces oxidize over time. All steps from photolithography to encapsulation need to happen in quick succession to minimize contamination on the samples, especially after the cleaning process. The plastic walls for the encapsulant were 3D printed ahead of time and were ready to be installed on the FR4 samples after the silver epoxy curing process completed. After the walls were installed, the gel was measured and poured into the samples to minimize bubble formation. Then bubbles were removed and the gel was cured at high temperature. The encapsulation process is divided into the following steps and each step is detailed next:

1. 3D print walls of the encapsulant containment
2. Attach the walls onto the sample and cure overnight
3. Measure and pour gel into the sample
4. Remove bubbles
5. Cure gel encapsulant

Step 1:

To 3D print the walls of the encapsulant, the walls were designed in SolidWorks as shown in Figure 127. This was then converted to an STL file and imported into the 3D printing software CatalystEX. This software is used for building up the layers used for 3D printing the design. The print material used was ABS, a commonly used plastic for printing. The equipment used was a Stratasys µPrint 3D printer. Instead of a hollow fill, the walls were printed "solid" to prevent leaking of the gel.

Step 2:

Loctite Go2 Glue was used to attach the 3D printed housings to the FR4. The glue needs to be stored in a refrigerator once opened because exposure to air and moisture will start curing the glue in its container. Glue was applied to the bottom edge of the printed walls and the walls were set on top of the FR4 of each sample. Gentle pressure can be applied to the sample for a minute when the attachment is first made before gently releasing and then storing the samples at room temperature for 24 hours to cure.

Figure 160 shows the housings attached to the samples. It is important to cure the glue so that it can withstand the high temperature of the oven when the encapsulant is vacuum cycled and cured. Without curing, the gel encapsulant can leak from between the plastic housing and the FR4 copper surface.

Figure 160. Housings attached on samples and glue cured over 24 hours.

Step 3:

The gel encapsulant used was Dow Corning 3-6635 Dielectric Gel [91], which is a one-part gel that does not require mixing. It cures at 100 °C over a period of two hours. To prevent bubble formation as much as possible, the bottle was not shaken but the sample was gently poured out of the bottle into small 6 oz cups. A syringe was used to measure out 3 mL of the gel fluid in a way that prevented suction of air into the syringe that would create a bubble. The syringe was kept upright (nozzle pointing up) to allow air bubbles to float to the top and exit the syringe. The gel was then slowly applied onto the sample ensuring the trace gap was covered first and the fluid would fill the rest of the regions over and under the DBC and around the

terminals. Another approach is to apply the gel along the walls of the housing, but this might cause an interface to occur when the fluid slowly merges from two directions in a region at the trace gap. Figure 161 shows the gel in the 1 oz cup (left), in the syringe (middle) and being applied to the sample (right). Figure 162 shows the samples with gel applied. The gel is so transparent, it is almost invisible. Three mL was used for each sample as this would sufficiently cover the trace gap and around the DBC on the FR4 copper. The gel is a very good insulator with a dielectric strength of 20 kV/mm.

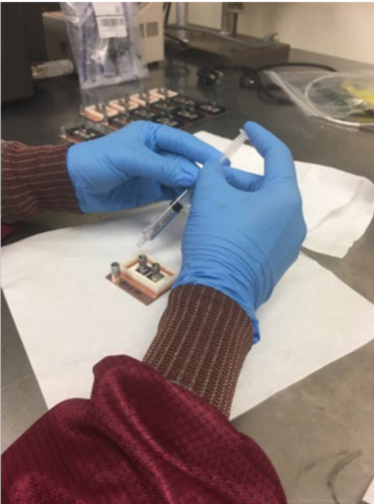


Figure 161. Encapsulant gel poured into a 1 fl. oz. cup (left), bubbles escaping from each 3mL of gel in each syringe (middle), and gel being applied onto a sample (right).

Figure 162. Samples on vacuum oven tray with gel within the 3D printed wells, ready to be vacuum cycled for bubble removal at room temeprature.

Step 4:

When the gel is poured, there are often micro-recesses in the metal-ceramic interface which may not get covered by the gel. These are air pockets that can be detrimental to PD prevention as the relative permittivity and dielectric strength of air is much lower than that of the insulation material (gel encapsulant, in this case). The gel encapsulant has a relative permittivity (relative to that of vacuum) of 2.83 and a dielectric strength of 20 kV/mm. Air has a relative permittivity of 1.0 and a dielectric strength of 3.0 kV/mm. As mentioned before, due to the reduced permittivity, there is a higher concentration of E-field in an air pocket than in an insulation material, and it is more likely to breakdown. Furthermore, the reduced dielectric strength makes it much more likely (almost inevitable) for breakdown to occur. This regional breakdown is partial discharge. It is very difficult to completely remove all bubbles perfectly. But minimizing the presence and size of the bubbles can help reduce the magnitude and likelihood of PD in the overall module.

To remove bubbles, one method is to cycle the gel encapsulated samples through vacuum multiple times. Pulling vacuum, existing bubbles in the sample enlarge, float slowly through the high viscosity fluid to the top, and then pop as they can't enlarge anymore. Filling the chamber with nitrogen presses the gel into crevices and other existing pockets where air may still be. If the region is small enough, the gel completely wets and fills the region. With multiple vacuum and nitrogen fill cycles, most bubbles are resolved, and after a while, no noticeable change is seen in the samples. For this work, six vacuum- nitrogen cycles were used at room temperature to remove the bubbles prior to curing the gel. This step needs to be performed soon after the gel has been poured as the gel does start curing slowly at room temperature. Figure 163 shows two example samples and their bubbles through their first and last vacuum cycles. Note that by the sixth vacuum cycle, there are no bubbles seen at the surface. The main region where bubbles should not exist is the trace gap. If residual bubbles remain in the 3D printed plastic walls of the encapsulant containment, that is not critical. Note that if there appear to be bubbles at the interface of the ABS plastic wall and the FR4, those bubbles may be from the superglue and are appearing magnified through the transparent gel. These bubbles do not affect safety or performance of the sample.

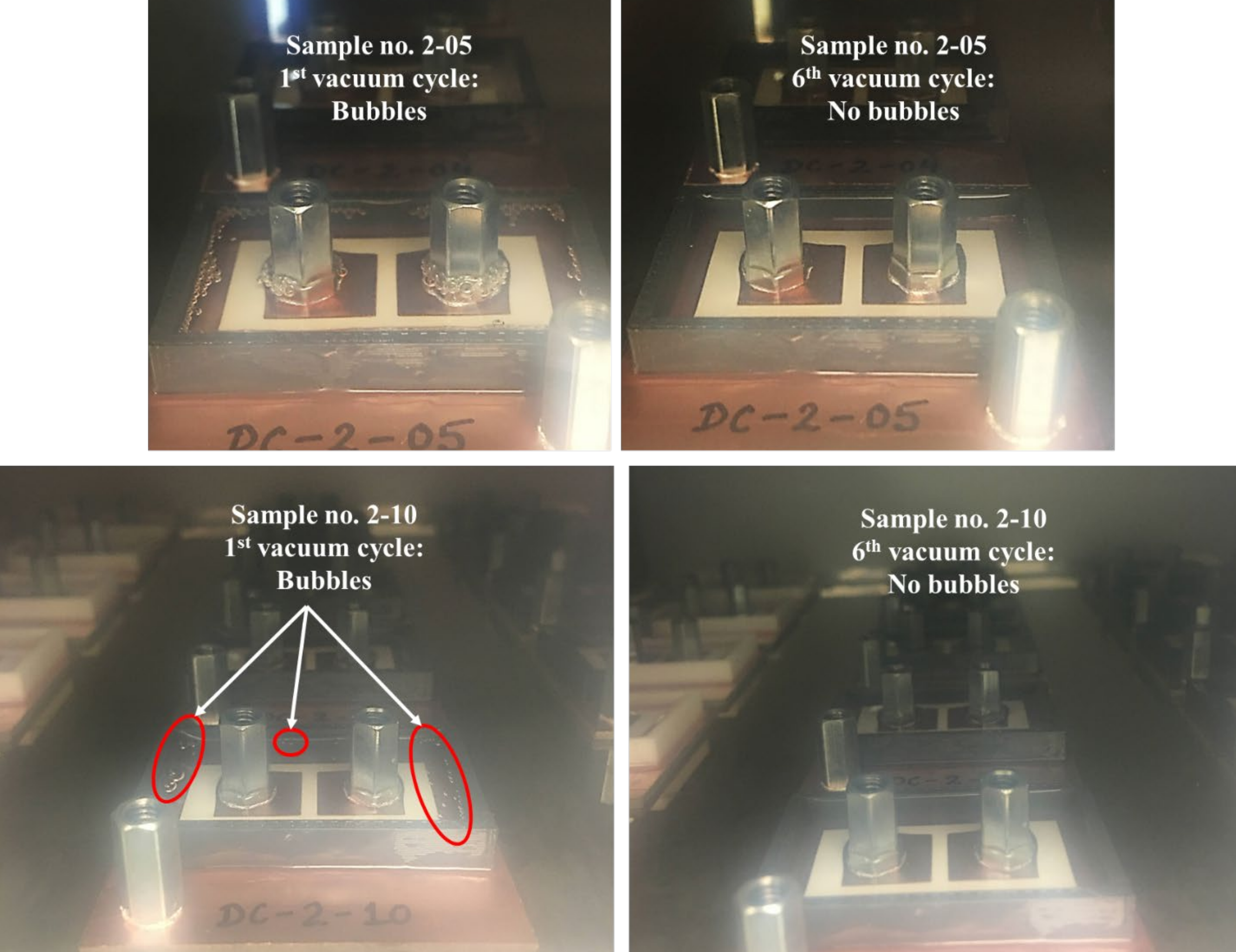


Figure 163. Sample number 5 (top) and sample number 10 (bottom) with bubbles during the first vaccum cycle (left) and no bubbles during the last vacuum cycle (right).

Step 5:

Once bubbles are removed, the dielectric gel must be cured. The oven was preheated to 100 C and the gel was cured at 100 C over a period of two hours. Since the oven could not hold all 30 samples at the same time, they were cured in two batches of 15 samples each, one after another in the same session. Figure 164 shows the samples after the encapsulation was cured. Then the samples were carefully removed from the oven, stored in the airtight container, and kept in the nitrogen box until they were ready to be tested. The gel after curing is still soft and is tacky to touch but does not flow and secures the trace gap and is ready for high voltage

application across the trace gap.

Figure 164. Samples after the dielectric gel curing process, and ready for testing.

Appendix J: PD Test Setup and Execution Related Instructions

J.1 LabView program and communication with the Spellman power supply

The LabView program used to communicate with and control the Spellman power supply was pre-programmed. The front panel interface of the program is shown inFigure 165. When run, the program communicates with the Spellman power supply and turns it on or off. This is done by the 'Enable' button. Anytime the supply is enabled, the program reads the binary switch labeled 'Man_nAuto_VCmd' which, if ON, means the program is in manual (not automatic) voltage command mode and it reads voltage input from the 'VCmd' or voltage command text box, requests the supply to apply that much voltage across its terminals, and displays the requested voltage in the 'Voltage_Cmd' field. Whatever voltage is across the terminals of the Spellman supply would be displayed on the 'Voltage_Mon(V)' voltage monitor text box in volts. The value in the voltage monitor field fluctuates a little and this is one way to know that the system is communicating. If this field shows a static value, it might mean that the program is stuck in its last state before it lost communication with the supply, and the communication needs to be re-established to ensure the power supply can be safely controlled through the software. When communication is lost, it is especially important not to touch the supply as there is no way of knowing how much voltage is across its terminals. Instead, communication should be re-established and the voltage brought down to zero, if it is not already defaulting to zero when communication is re-established.

When the 'Enable' button is clicked to turn on communication, and 'Man_nAuto_VCmd' is OFF, it means the program is not in manual voltage command mode but is in automatic voltage command mode. In this mode, the voltage that is input by the user in the back end of the program is loaded and run immediately when the 'Enable' button is clicked. This feature must be

used with care. One must ensure the automatic program is the correct one that is loaded, and then the 'Enable' button clicked. When the program starts transferring the automatic voltage profile pre-set by the user, to the power supply, the waveform in the front panel changes to show the voltage profile that is loaded into the program from the back end.

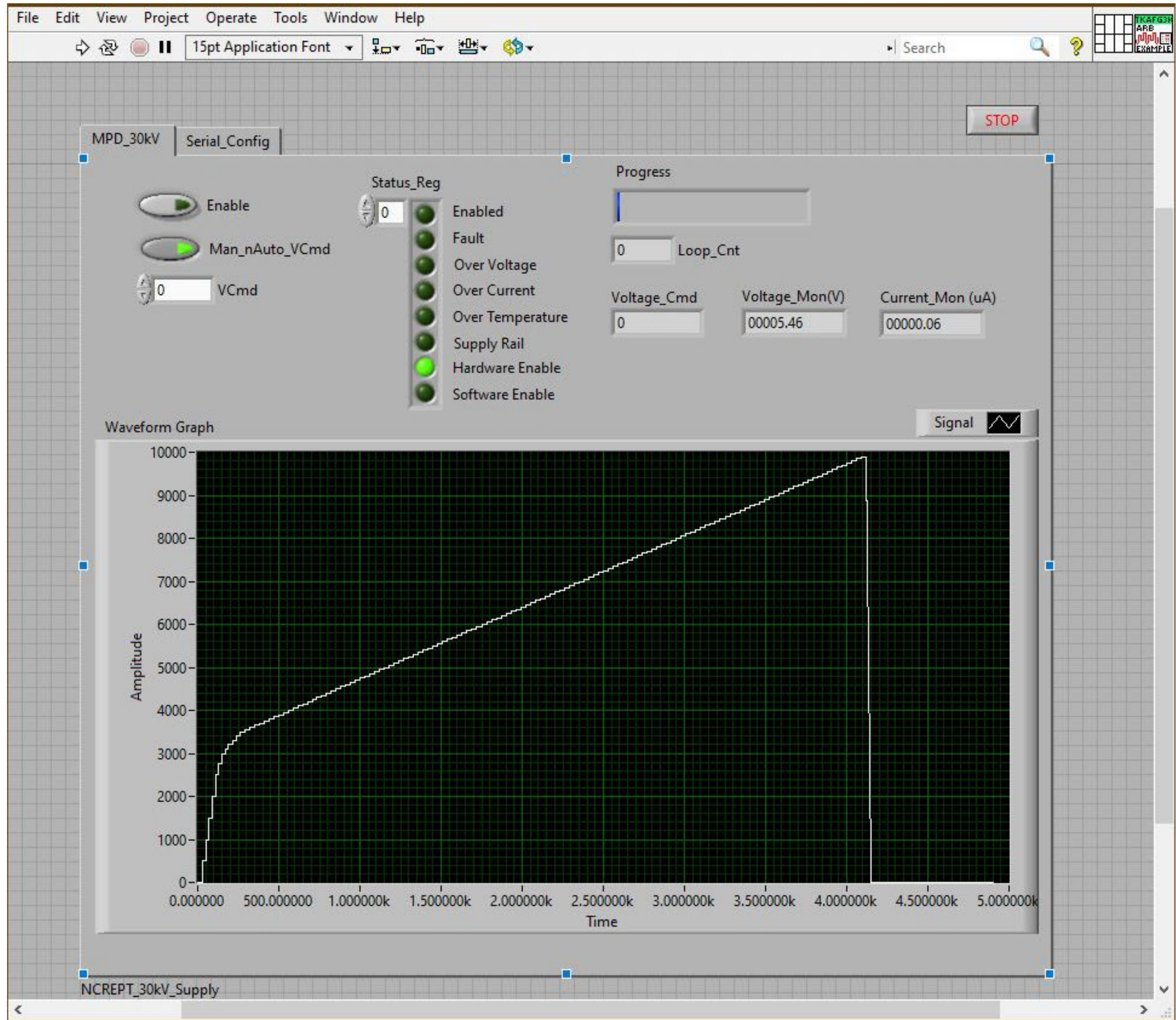


Figure 165. LabView front panel interface for controlling the 30 kV power supply.

To change the voltage profile, one must double click on the solid grey background of the front panel to access the program on the back end. An outline of the back end program is shown in Figure 166. On the top left corner of the figure is a blue box that reads "Simulate Arbitrary

Signal.” This portion of the outline is enlarged in Figure 167 and marked with a dashed outline. This should be used to access the signal configuration dialog. In the signal configuration dialog, the “Define Signal” button should be used to access the voltage vs time chart of the signal (Figure 168). The data here can be edited and saved, or a new data set can be loaded. The user must note the “Number of points” mentioned on the right and manually insert this in the appropriate box on the top left corner of the entire program schematic (Figure 167). This number indicates to the program the number of points to loop over. If this number is smaller than the actual number of points in the voltage-time chart, the program will prematurely start looping back to the beginning of the chart.

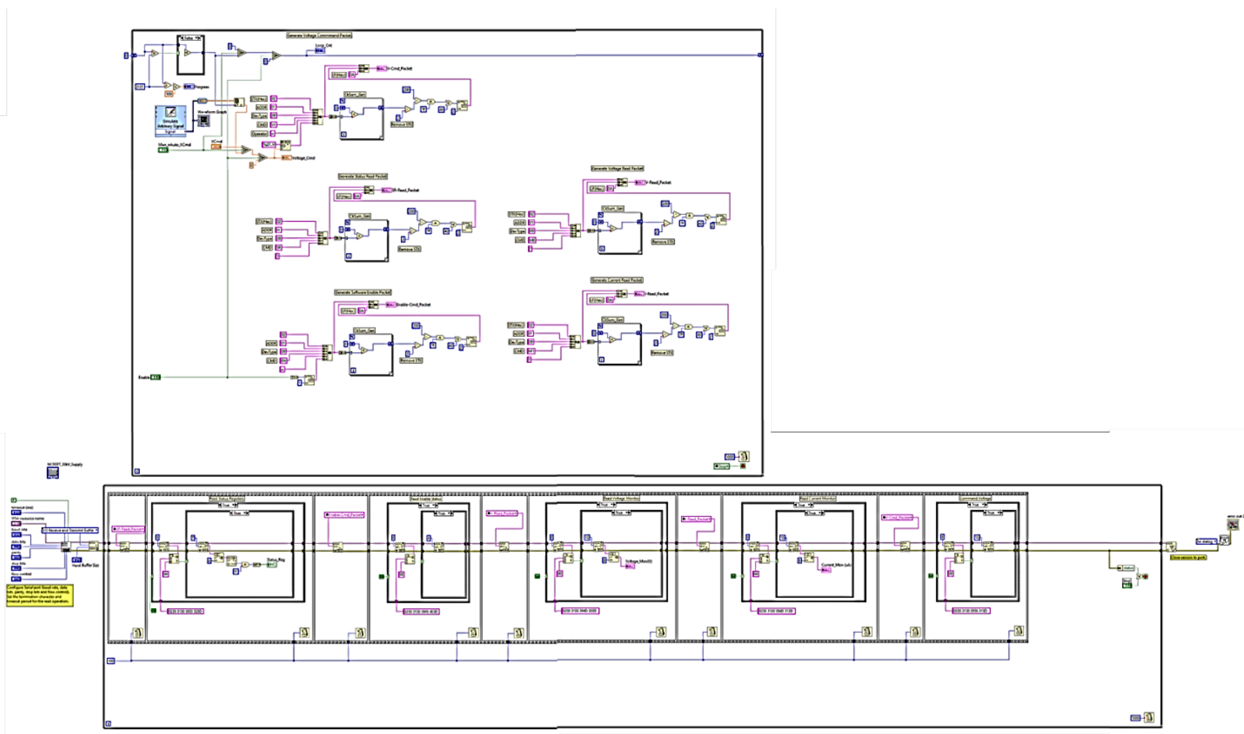
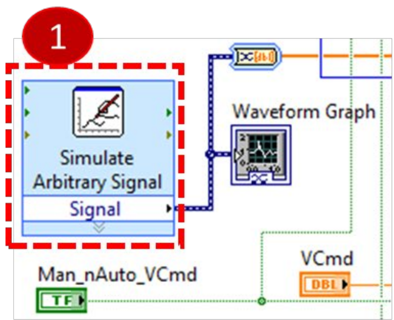


Figure 166. LabView program outline for controlling the 30 kV power supply.



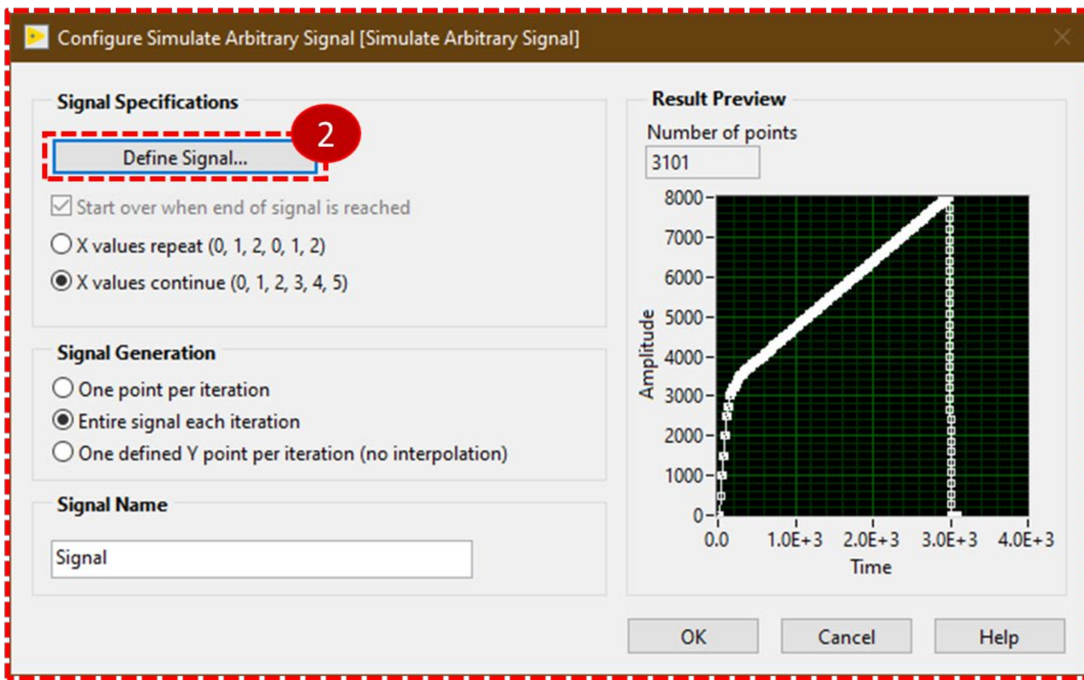


Figure 167. “Configure Simulate Arbitrary Signal” screen.

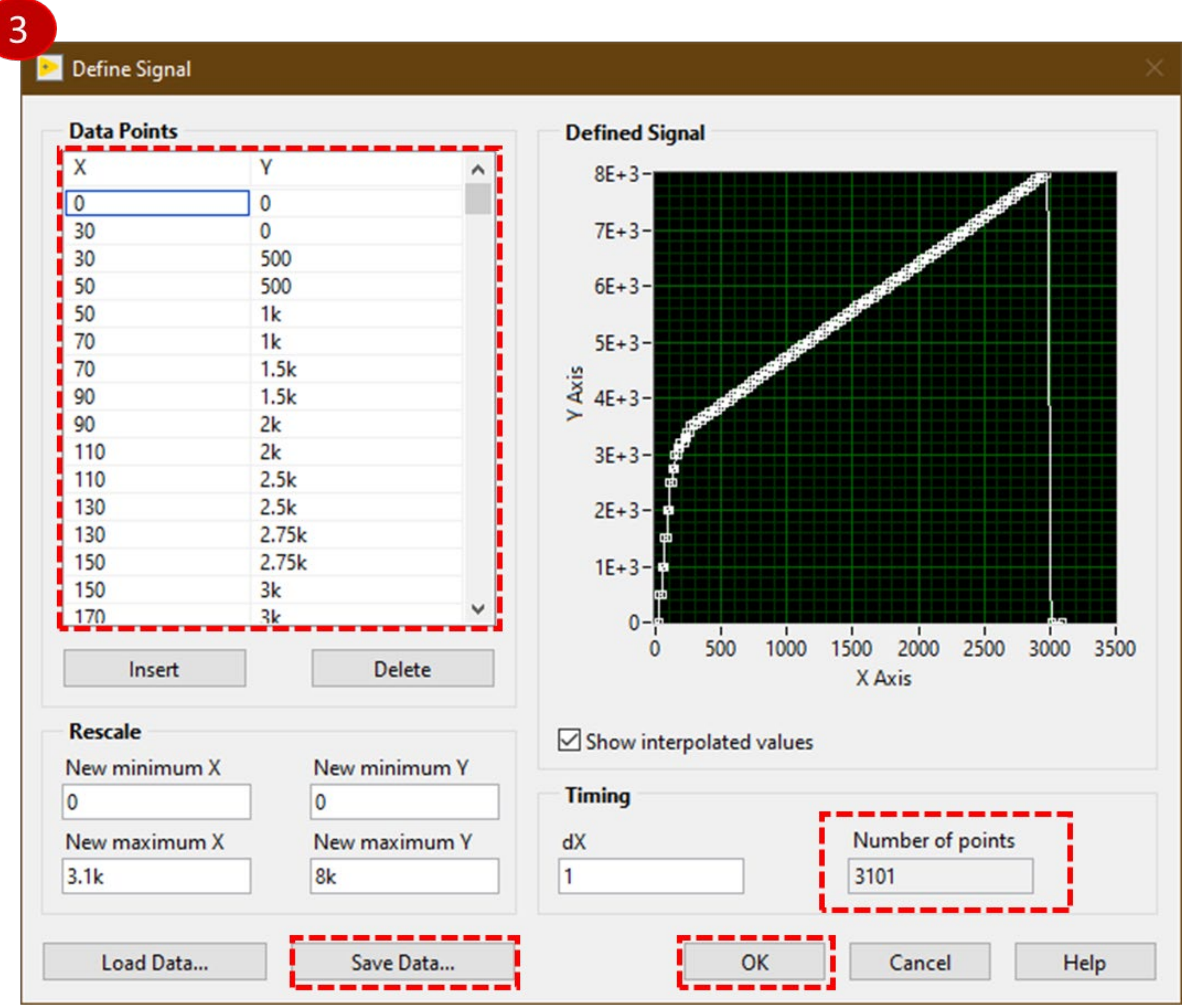


Figure 168. "Define Signal" screen.

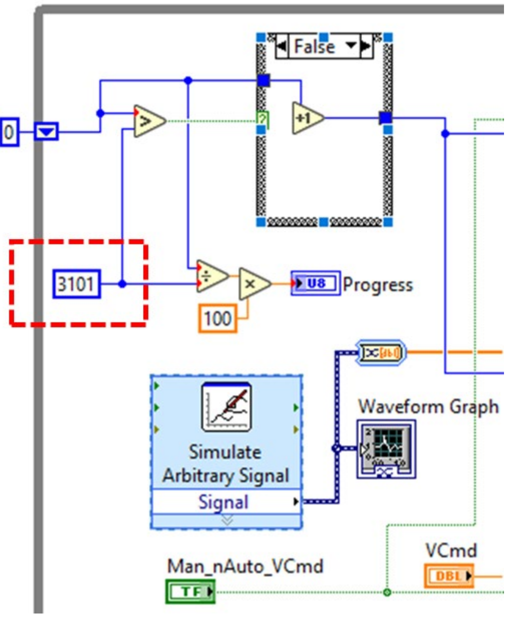


Figure 169. Number of data points in the voltage-time profile in the LabView program.

When the power supply hardware is fully ON, the program can be run using the arrow button on the task bar on the top. When the software is ready to take command from the 'VCmd' field, several indicators on the front panel will be ON (lit up as bright green): Enabled, Hardware Enable, and Software Enable. To troubleshoot communication issues, the "Serial_Config" tab should be used. To stop communication (for troubleshooting purposes only), the "STOP" button should be used. The "STOP" button should NOT be used to shutdown the power supply hardware. The "STOP" button only stops communication between the software and the hardware. In the event of an emergency, the 'Man_nAuto_VCmd' button should be clicked and "0" entered in the 'VCmd' field to bring the voltage of the power supply hardware to zero, and then the supply needs to be switched off physically using the switch it is connected to and then disconnected from the power supply of the bench. Voltage was applied with a pre-determined ramp rate. The voltage profile was programmed into the LabView interface for the power supply where the "Define Signal" feature allows the user to input the excitation profile.

J.2 Safety precautions taken for HV tests:

1. A safety partner who knows how to shut off power to the bench and call emergency services in the event of an emergency.
2. A grounding rod for discharging the HV capacitor before touching the table.
3. Ensuring all parts that need to be connected to ground are properly connected.
4. Turning ON/OFF equipment in a specific order and increase/decrease voltage appropriately.
5. Announcement to workers nearby that a high voltage test will be performed before the circuit is energized.
6. Safety goggles.
7. Not leaving the desk unattended while the circuit is energized.
8. Always letting someone know your test plans.

J.3 PD test execution steps in detail

1. Connect DUT to HV terminals, apply kapton between terminals, and pour fluorinert into the ceramic bowl to submerge the sample. Prepare a sample and test information card and note the date, time, sample ID, temperature, pressure, humidity, and test set number on it. Connect the MPD 800 to the RBP.
2. Measure the general background noise:
    a. Keep power supply disconnected.
    b. Open the MPD 800 software, connect the MCU to the computer and go to the PRPD tab. Refer to Figure 170.
    c. Go to the ADVANCED tab in the Control Panel and toggle the PD Gain by setting it first to “auto” and then setting it back to “semi.”

d. The instantaneous charge being measured at any time is given at the top of magnitude monitor panel and is called Q_{IEC}. In this figure, it is 884 fC. To capture an image of the waveform, hit F5, or go to the "PRPD & AC" tab and click "Capture PRPD", or click the sine wave icon among the snapshot icons on the top right corner. Then click the save snapshot icon. This saves an image of the main display window on the desktop or the location specified in the EXPORT tab. The general background noise is the quantity mentioned in Q_{IEC}. Clear the PRPD plot by clicking the "Clear PRPD" button.

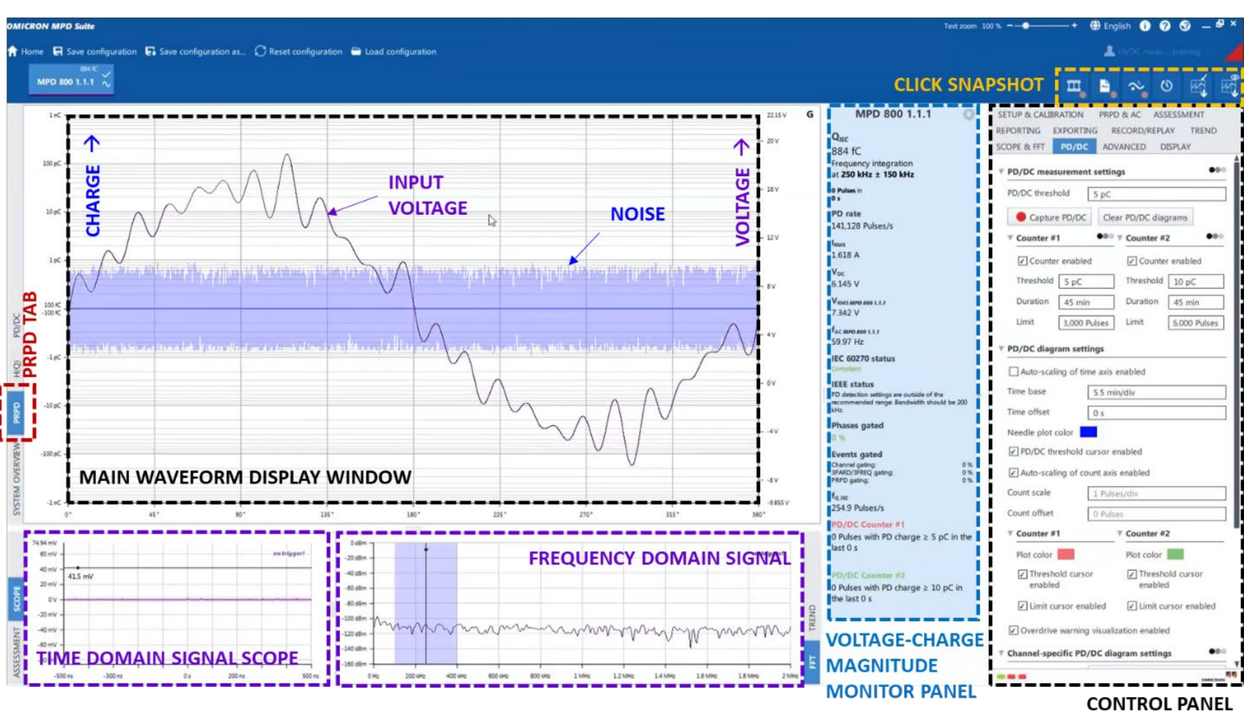


Figure 170. Main screen for PD measurement on the Omicron MPD 800 software.

3. Prep the LabView program with the correct voltage profile:

   a. Connect the power supply and ensure the LabView program can communicate with it.

   b. To check if the power supply responds, apply a small voltage (100 V) to the

"VCmd" field and see if "Voltage_Cmd" and "Voltage_Mon" change to reflect the "VCmd" that was input. Bring voltage back down to zero.

c. To check if the automatic voltage profile loads, toggle from manual mode to automatic mode and check if the correct voltage profile is loaded on the front panel waveform screen. Toggle back to manual mode and ensure voltage applied is zero.

4. Measure the noise from the power supply:
    a. With supply connected and ON, but without any voltage applied, go to the SETUP & CALIBRATION tab, and select:
        i. Sensor type = coupling capacitor
        ii. Device = Custom
        iii. Capacitance = 1 nF
        iv. Coupling Unit = CPL 542 (500 mA)
    b. In the PRPD & AC tab, set PD/AC sync to "Internal trigger." The distorted waveform should become an un-distorted sine wave in the main display screen as shown in Figure 171 (a).
    c. Take a snapshot of the image. The noise signature will now include the noise from the power supply. This is the noise floor. It should always be less than half of the PD threshold value. In this case, the PD threshold value was 10 pC and the noise was always between 2-4 pC, which is acceptable. For these tests, the noise looked like that in Figure 171 (b).
    d. Disable the power supply and disconnect its hard switch.
5. Calibrate voltage (do this only when a new test setup is used):

a. Go to the ADVANCED tab and toggle the PD gain setting to "Semi-automatic."
b. Go to PRPD & AC tab and change the PD/AC sync trigger to "AC input MPD 800.1.1.1."
c. Go to the PD/DC tab on the left of the waveform display screen.
d. Click on "Capture PD/DC" button. This will start recording the voltage vs time data that will later be exported to a csv file.
e. Under SETUP & CALIBRATION tab, go to the Test Voltage tab and put the "Dominant Voltage" to DC. Also apply the following settings:
    i. Sensor type = None
    ii. Coupling unit = None
f. Set "Calibrate to" to 100 V and apply 100 V from the power supply using LabView.
g. Click "Compute." VDC on the monitor panel in the middle should show something close to 100 V. And the calibration factor will be large because of the 1 GΩ resistor in the voltage divider.
h. Increase the voltage to 200 V and confirm if VDC seen on the MPD software responds accordingly.
i. Return voltage level to zero volts.
j. Under SETUP & CALIBRATION, revert the settings:
    i. Sensor type = coupling capacitor
    ii. Device = Custom
    iii. Capacitance = 1 nF
    iv. Coupling Unit = CPL 542 (500 mA)

k. Click "Capture PD/DC" again to deselect it.

l. Go back to the PRPD tab on the left.

m. Go to PRPD & AC tab and change the PD/AC sync trigger to "Internal trigger."

6. Calibrate charge (do this each time the test setup or DUT capacitance changes):

   a. With the supply disconnected, connect the calibrator across the DUT.

   b. Connect the power supply and turn on its hard switch. Apply zero volts to the power supply using the LabView program. The waveform for these tests looked like that in Figure 171 (b). Take a snapshot if needed.

   c. Go to the ADVANCED tab in the Control Panel and toggle the PD Gain again by setting it first to "auto" and then setting it back to "semi."

   d. On the calibrator, increase the charge level to 10 pC. The waveform on the screen should show many vertical spikes of 10 pC charge level as shown in Figure 171 (c). Take a snapshot. Q_{IEC} should read approximately 10 pC.

   e. The Scope and FFT window show the time and frequency domain of the entire waveform. To view a single signal's time and frequency signature:

      i. In the SCOPE & FFT tab, change trigger mode to PD Event trigger window and "Capture PRPD."

      ii. Next, click the "Select area of interest in PRPD," and using a mouse, draw a square around one of the 10 pC peaks as in Figure 171 (c), and observe the scope (Figure 171 (d)) and FFT (Figure 171 (e)) windows to see the time and frequency signature of the selected peak. Save a snapshot.

      iii. Deselect the event trigger window and return the trigger mode to "Edge trigger."

f. Go to SETUP & CALIBRATION tab and under "Charge," set "Calibrate to" to 10 pC. Click "Compute." This will ensure that the Q_{IEC} measured is calibrated to what is applied by the calibrator. Now, Q_{IEC} should read exactly 10 pC. This step accounts for all the parasitics in the system. Charge is now calibrated.

g. Disable the power supply using LabView, switch off the hard switch of the power supply. Reduce the charge level on the calibrator and turn it off. Disconnect the calibrator from the DUT and put it away. Reconnect the power supply and turn on its hard switch.

7. Run voltage program and measure PDIV:
   a. Re-establish communication with the power supply through LabView.
   b. Under SETUP & CALIBRATION, apply the following settings:
      i. Sensor type = None
      ii. Coupling unit = None
   c. Under the PRPD & AC tab, set PD/AC sync to "AC input."
   d. Go to the PD/DC plot tab on the left of the screen.
   e. Under the PD/DC tab on the control panel, set the "DC voltage to plot" setting to "AC input."
   f. Clear the PD/DC diagram.
   g. Set the PD/DC threshold to 10 pC. This means that only charge spikes greater than 10 pC will be shown and saved in the csv file exported. One may also choose to set the threshold to 5 pC to observe more discharges that would otherwise be censored. There are two counters. Set one of them to count every 5 pC of charge, and the other to count every 10 pC of charge. Under the diagram settings, adjust

the time axis and the charge and voltage axis as needed. An example set of these settings is shown in Figure 172.

h. Ensure the grounding rod or shorting stick is connected to earth ground and is accessible when needed.

i. Prep data collection:

    i. Under the REPORTING tab, set diagram size to “small.”
    ii. Under the EXPORTING tab, set diagram size to “small.”
    iii. Under the PD/DC tab, check the CSV export option file name and location at the bottom of the control panel under “CSV export options.”
    iv. Clear PD/DC diagrams. Capture PD/DC. Scroll down to and select the “Start exporting csv” button.
    v. In the REPORTING tab, click “start exporting.”

j. Apply voltage: On LabView, turn off the Manual mode and let the program run.

k. Observe data: On the MPD software, watch the PD/DC plot and the monitor panel to observe V_{DC} when charge level exceeds 10 pC and take a snapshot when that happens. The total test time for each sample was almost an hour.

l. Once there are numerous PD signatures beyond the threshold level of 10 pC, one may stop the test by clicking the manual mode button on the LabView program and setting the voltage to 0 V. Once the system is safely at 0 V, the system can either be turned off or be prepared for the next test, as needed. If the sample does not reach its PDIV, allow the entire voltage profile to run and it will automatically return to zero. Once the automatic program reaches 0 V, pay attention to de-select the automatic mode and enter the manual mode where voltage is set to zero.

Otherwise, the program will loop to the beginning of the voltage profile and re-start HV application.

8. Save data: Ensure that the two csv files are saved, along with all the images taken. Open the charge vs. time csv file and look for the time stamp when the charge first exceeded 10 pC. Lookup this timestamp in the voltage vs. time csv file and find the voltage at which this discharge happened. This is the PDIV to be noted for this sample.
9. Once voltage applied is zero volts, disable the supply, wait for 20 seconds, use the shorting stick to touch the HV terminal of the capacitor, then switch off the supply, disconnect it from the bench power and finally remove/replace the DUT.
10. If running another test, connect the new DUT and repeat steps 1-4, and 6-9. If not running another test, completely disengage the power supply, remove the DUT, disconnect the MPD800 unit from the RBP unit and put the RBP unit to charge. Put away the fluorinert and mark the sample as used.

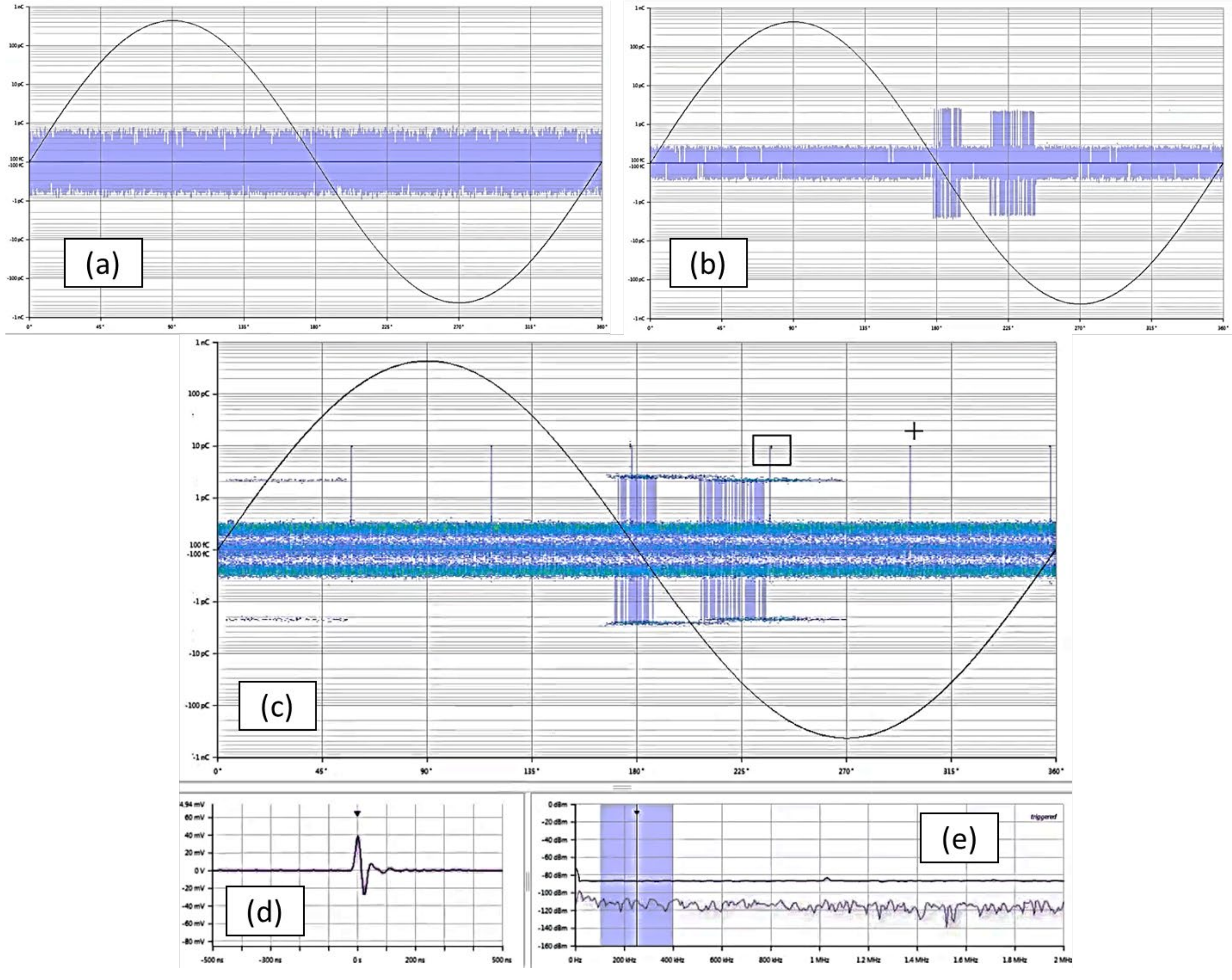


Figure 171. Signal and noise during the calibration process: (a) background noise without power supply, (b) noise including power supply, (c) 10 pC signal from calibrator unit against the noise floor.

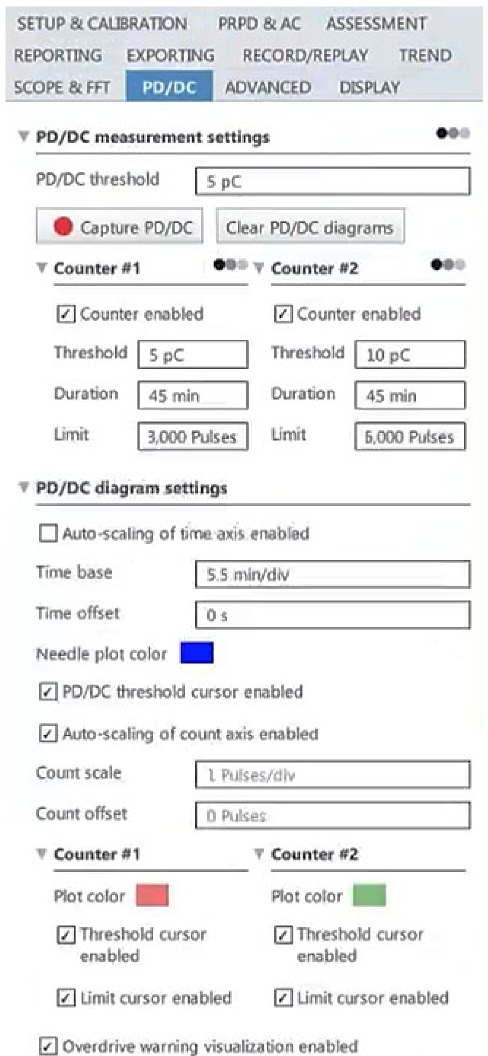


Figure 172. PD/DC settings.