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A PLL frequency synthesizer and Gilbert cell multiplier for a 916 MHz ISM band transmitter realized in 0.5 [mu]m [i.e. micrometer] CMOS technology

James C. Arnott

To the Graduate Council:

I am submitting herewith a thesis written by James C. Arnott entitled "A PLL frequency synthesizer and Gilbert cell multiplier for a 916 MHz ISM band transmitter realized in 0.5 [mu]m [i.e. micrometer] CMOS technology." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this thesis and recommend its acceptance:

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

To the Graduate Council:

I am submitting a thesis written by James Christopher Arnott entitled "A PLL Frequency Synthesizer and Gilbert Cell Multiplier for a 916 MHz ISM Band Transmitter Realized in 0.5μm CMOS Technology." I have examined the final copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major of Electrical Engineering.

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Michael L. Simpson

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Accepted for the Council:

Associate Vice Chancellor and
Dean of the Graduate School

A PLL Frequency Synthesizer and Gilbert Cell Multiplier for a 916 MHz ISM Band Transmitter Realized in 0.5μm CMOS Technology

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Dedicated to my mother and father
who have supported me through out
my college career.

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Abstract

This thesis is a study of the design of a 3rd order phase lock loop (PLL) and Gilbert cell multiplier to implement a 916MHz ISM band transmitter in 0.5μm CMOS technology. The transmitter is designed for implementing distributed biosensor systems for environmental monitoring.

The transmitter is described from a system level with the discussion of design issues concerning system topology and communication signal requirements as related to project requirements. The PLL system is described as a negative feedback system and important design considerations are discussed. Each PLL and transmitter system component is analyzed and discussed. A prototyped double balanced Gilbert cell multiplier with a power gain of 8dB, –10dBm compression point, and dissipates 7.2mW of power is analyzed and presented. The analysis and design of a prototyped current mode logic frequency divider with a fixed division factor of 256 is presented. The frequency divider dissipated 15mW of power for a –20dBm 916 MHz input signal with a maximum operating frequency of 1.8 GHz. An off-chip LC tank voltage controlled oscillator was prototyped with a tuning range of 120 MHz, dissipated 3.3mW, -15dBm single-ended output signal, and had a phase noise performance of –60dBc at a 10 kHz offset and –80dBc at 100 kHz offset is analyzed and presented. The design and simulation issues of a digital phase frequency detector (PFD), charge pump, and loop filter is presented. The charge pump was designed to source or sink a 10 μA current for an output voltage to within 0.1 V of the power supply voltages. Results show that the final transmitter can be successfully implemented with the prototyped and simulated transmitter components.

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Chapter 1

Introduction

Using integrated circuit (IC) technology to realize intelligent distributed biosensors is ideal for many applications such as environmental monitoring. IC technology is ideal for realizing the small, rugged, and inexpensive devices required for distributed sensor systems. Other environmental monitoring systems may be too large, expensive, or require too much power. However, IC technology allows for the combination of all measurement system functions on a single chip creating a microsensor. The use of wireless technology in a distributed sensor system eliminates the need for external cabling, which enhances deployment options and decreases cost. Modern wireless digital communication systems also allow multi-user interfaces; so several systems could be placed in a closely packed cluster to simultaneously collect information from each sensor network.

1.1 Bioluminescent Bioreporter Integrated Circuits (BBICs)

Biosensors are hybrid devices combining a biological component with an analytical measuring element [1-5]. The biological component acts as the measurement interface with the process of interest producing a response that can be measured by an electronic, optical, or mechanical sensor. The most common biological component uses immobilized enzymes or antibodies tailored to measurement requirements. Other less utilized systems, referred to as whole-cell biosensors, include biological components with living microorganisms or sections of organs or tissues. Originally these biosensors were

observed by detecting the activity of growing cells with electrochemical transducers. Normally, whole-cell biosensors function in controlled environments but are not applicable, because of growth on nutrients other than the target analyte causing interference in the measurement. Presently, bioluminescent bioreporters have become a popular measurement solution because a bioluminescent response is easily detected and the process under observation need not be destructive to the cells, which allows continuous real time monitoring. Bioreporters are genetically engineered for bioluminescence using both eukaryotic and prokaryotic cell lines that have been developed for the detection of water born toxins, pollutants, and soil contamination.

Bioluminescent Bioreporters Integrated Circuits (BBICs) are an integration of genetically engineered bacteria and integrated circuit technology. BBICs consist of three elements: 1) the bioluminescent bioreporters; 2) photodiodes and 3) signal processing circuitry as shown in Figure 1 *. The bioreporters are directly exposed to the analyte and produce bioluminescence. This bioluminescence produces measurable current in the integrated photodiodes. Low noise signal processing circuitry is used to measure this photocurrent. It is also desired to use a transmitter to send the data to a central node for further data collection.

This thesis focuses on the design and development of a phase lock loop and Gilbert Cell multiplier for a 916MHz BPSK transmitter for use in an environmental monitoring distributed system.

* All figures are located in Appendix 1

1.2 BBIC Transmitter System Requirements

The transmitter must be small, low power, and highly integrated to provide the most deployment options for the sensor. To avoid a cable plant, battery operation is required. Since the transmitter will dominate the power consumption of the sensor system a sleep mode is required to turn the transmitter off while the bioluminescent signal is acquired and processed. All components in the transmitter are designed for low power operation while the system is in the transmit mode and to consume no power when the system is not transmitting.

Transmission range and duty cycle are the most important design considerations concerning power consumption. Since BBIC sensor systems transmit only a short distance, a power amplifier is not required. The exclusion of a power amplifier in a short-range transmitter greatly simplifies the transmitter design, while lowering the overall power consumption. The printed circuit board, antenna type, tolerance of matching networks, and noise figure of the receiver's input limit and determine the transmission range of the transmitter.

1.3 Communication Signals and Requirements

Any communication system has a specific signal type or modulation scheme. The simplest forms of modulation and best known in communication systems are double side-band amplitude modulation (AM) [6] and frequency modulation (FM) [6]. Binary phase shift keying BPSK [7] is a very popular form of digital modulation, which can be implemented with simplicity and offers advantages over both, AM and FM modulation schemes. BPSK modulation is achieved by shifting the carrier's phase by $\pm 180^{\circ}$ for each

successive alternating symbol. A simple BPSK digital modulation also offers very low bit error rates, low system cost, and simplistic realization compared to AM and FM modulation schemes. BPSK achieves its low bit error rate performance because its power spectral density function is a sinc function with peaks at odd harmonics of the fundamental modulation frequency. Since the sinc function spreads the modulating signal across a large frequency span, spurious noise signals randomly located within the message signal will have less adverse affect the received message [7].

Spread spectrum systems are becoming widely used forms of digital communications. These systems offer superior performance when implemented with multi-user systems and when high level security is desired. The most popular forms of spread spectrum communication systems are frequency hopping [8] and direct sequence [7]. While spread spectrum communication is not necessarily a BBIC requirement, it may be useful in some distributed sensor applications.

1.4 Transmitter System Description

The fully integrated direct conversion transmitter [9] is implemented with two interconnected blocks as shown in figure 2. The two main blocks of the transmitter are a Phase Lock Loop (PLL) [10-15] and active Gilbert Cell four-quadrant mixer [15].

The PLL is implemented with five basic building blocks: 1) a precision frequency reference [16]; 2) a phase/frequency detector [17]; 3) a loop filter [18]; 4) a voltage-controlled oscillator (VCO) [18-23]; and 5) a frequency divider [18] as shown in figure 3. A PLL is a negative feedback system and operates with a highly precise reference frequency input signal, which is forced by the feedback to control a much higher

frequency signal, so that the two signals maintain phase and frequency correlation. The comparison of the reference and output phase/frequency information is filtered to produce a DC signal that adjusts the VCO operating frequency to maintain phase/frequency lock. The PLL synthesized carrier is then modulated directly with the baseband information signal with the mixer. The transmitter will transmit directly from a buffer amplifier to a standard 50Ω dipole antenna.

1.5 Scope of Thesis

This thesis presents the design, development, and characterization of the mixer, frequency divider, VCO, and charge pump PLL as part of a BBIC transmission system. Chapter 2 presents in detail the design of the individual circuits of the PLL and mixer, while Chapter 3 presents the analysis and design of the voltage-controlled oscillator. Chapter 4 details the test results of the prototype circuits used to implement the PLL, and Chapter 5 gives the conclusion and discusses future work and improvements. Appendix 2 contains process parameters and models used for the HP 0.5um process, and Appendix 3 contains all simulation circuit files used to simulate the PLL and mixer. Appendix 4 contains all simulation extraction spice files used to simulate the PLL and mixer.

Chapter 2

Phase Lock Loop and Mixer Analysis and Design

This chapter discusses the development, analysis, and design of the third order charge pump phase locked loop (PLL) and transmitter. The PLL used in the BBIC transmitter is considered a classic digital phase lock loop topology since the PLL uses a frequency divider and digital phase/frequency detector [14]. This topology is chosen for its extended tracking range, frequency acquisition, and easy implementation in CMOS technology. The phase lock loop will synthesize a 916 MHz carrier signal for the BBIC transmitter. The carrier signal is modulated by the digital signal from the signal processing circuitry to form a direct conversion BPSK signal. A CMOS double balanced Gilbert Cell multiplier along with the synthesized 916 MHz signal and the digital signal processing circuitry forms the direct conversion, 916 MHz BPSK transmitter.

2.1 PLL System Description

The charge-pump PLL is a negative feedback control system, which consists of five basic building blocks: 1) frequency reference; 2) phase/frequency detector; 3) loop filter; 4) voltage controlled oscillator (VCO); and 5) frequency divider as shown Figure 3. In the basic operation of the PLL, the phase/frequency detector compares the phase/frequency of a precision frequency reference to a fractional multiple of the VCO frequency. The loop filter then produces a near DC error signal control voltage, which

controls the operating frequency of the VCO. The VCO's output frequency is divided by a factor of 256 and then compared to the reference oscillator. Feedback ensures that the output frequency of the VCO is very stable and maintains synchronous operation with the frequency reference. The output will remain at a constant stable frequency because the frequency reference is derived from a crystal oscillator. A stable transmitting frequency is essential for maintaining a locked condition when the transmitted signal is received.

2.2 PLL System Specifications

The PLL is designed by determining several essential specifications of the PLL loop bandwidth, lock time, phase margin, and open loop gain [6]. The loop bandwidth is the adjustable bandwidth of the phase lock loop. This adjustable bandwidth is the frequency bandwidth, which the PLL can track and correct for changes in the VCO's frequency. Lock time is the time required for the PLL to acquire phase lock from a start up condition. Lock time is very important, because the BBIC transmitter does not operate continuously. The phase margin is an indicator of the stability of the PLL as a negative feedback system. Negative feedback systems with a low phase margin generally exhibit fast and ringing response to a step input with a large overshoot and long settling time. Negative feedback systems with small bandwidth, and high phase margin generally exhibit slow response to a step input with small overshoot and very small settling time. The mentioned characteristics are used to design the PLL.

Phase noise of the PLL is related to randomly occurring fluctuations in the PLL's output frequency [24]. These random fluctuations in the output frequency of the PLL appear as a wider bandwidth spectral output. Phase noise is a very important parameter in

PLL design because excessive phase noise in the synthesized output frequency greatly impairs the ability to receive and demodulate the signal. The major contributors of phase noise in a PLL are the VCO, frequency reference, and loop filter. Contributions to PLL phase noise from the frequency reference's phase noise are multiplied by the PLL gain (256) and directly add to the total phase noise of the system. The only way system phase noise from the frequency reference can be minimized is through the use of a highly precise low phase noise crystal oscillator and narrow PLL closed-loop bandwidth. This means a highly precise crystal oscillator with an operating frequency close to the synthesized frequency will produce a synthesized frequency with lower phase noise. Any noise present in the loop filter is amplified by the VCO gain at the PLL output. Phase noise generated by the loop filter is mainly due to white noise effects, while phase noise from the frequency reference is due to jitter in the crystal oscillator. Using low noise circuit design techniques and smaller VCO gain can minimize phase noise contributions from the loop filter. Phase noise contributions from the VCO are caused by the random fluctuations in operating frequency of the VCO. The VCO's phase noise is the most significant contributor to the phase noise of the PLL with a highly precise low noise reference oscillator because the phase noise of the VCO is passed to the output with a highpass transfer function [24]. Phase noise from the VCO effects is minimized in a PLL with high gain and increasing the closed loop bandwidth [24].

2.2.1 PLL System Analysis

The complete PLL system analysis was performed by determining and evaluating the transfer functions of each of the PLL components with the PLL in a locked state, then combining individual transfer functions to analyze the PLL's closed-loop response with

classical methods. Figure 3 is used as a model of the PLL for evaluating the PLL's closed-loop response. In this model the summing node and K_d represents the phase/frequency detector and charge pump transfer function. K_f represents the loop filter transfer function, and the integrator block represents the VCO's transfer function with VCO gain K_v. The output is frequency fed back through a division factor N.

2.2.2 Phase Frequency Detector with Charge Pump Analysis

A simplified diagram of the phase frequency detector (PFD) and charge pump is shown in Figure 4. The basic operation of the charge pump is to inject or absorb current pulses from the loop filter depending on one of 3 states of the PFD [18]. Since the charge pump changes the VCO's control voltage by injecting or absorbing current from the loop filter capacitor, the average value of the current is given by [14]

$$i_d = \frac{I_P \cdot \theta_e}{2 \cdot \pi}(Amps), \qquad (2.1)$$

where I_p is the pump current, θ_e is the phase difference between the phase/frequency detector inputs. The VCO's control voltage V_c is directly proportional to i_d and is given by [14]

$$V_c(s) = \frac{I_P \cdot Z_F(s) \cdot \theta_e(s)}{2 \cdot \pi}(Volts), \qquad (2.2)$$

where Z_F is the impedance of the loop filter.

2.2.3 VCO Transfer Function

The transfer function of the VCO has both frequency and phase components. The frequency component is also known as the gain of the VCO and is defined as [10]

$$K_V = \frac{\Delta\omega}{\Delta V_C}\left(\frac{rad/\sec}{volt}\right), \qquad (2.3)$$

where $\Delta\omega$ is the frequency tuning range of VCO, and ΔV_c is the range of control voltage. A small tuning range reduces the gain of the VCO and improves loop stability and reduces the VCO's phase noise contribution due to noise from the loop [24]. A tuning range of 100 MHz centered about 916 MHz-carrier frequency is chosen for the BBIC transmitter.

The phase of the VCO is obtained by the integration property of the VCO's transfer function, where the phase of the VCO is the integral of its operating frequency. The VCO's phase is used to adjust and maintain a locked condition in the PLL. This integration of the VCO's frequency results in a pole at the origin because integration in the real time domain is a multiplication by a factor of 1/s in the complex frequency domain [18]. This pole introduced by the VCO presents stability problems in the closed loop PLL.

2.2.4 Loop Filter Transfer Function

The pole at the origin introduced by the VCO must be compensated to ensure a stable closed loop system. This requires a lag filter. Adding both a pole and zero to the closed loop PLL completes the compensation by the lag filter. The zero at the orgin created by the lag filter cancels the pole created by the VCO.

A problem associated with charge-pump PLL systems is the switching action of the charge-pump, which introduces transient voltage spikes on the lag filter. Adding a capacitor in parallel with the lag filter produces a third order PLL; this can reduce these

transients as shown in Figure 5. The impedance transfer function of the lag loop filter with an additional parallel capacitor is given by [14]

$$Z_F = \left(\frac{b-1}{b}\right) \cdot \frac{s \cdot \tau + 1}{s \cdot C \cdot \left(\frac{s \cdot \tau}{b} + 1\right)} \left(\frac{volt}{amp}\right), \qquad (2.4)$$

where $b=1+C/C_p$, and $\tau=RC$. The additional capacitor C_p causes an additional pole located at $s = -b/\tau$ [14]. C_p must be chosen carefully to avoid stability problems [14]. If C is much greater than C_p, ($b >> 1$), only the high frequency effects caused the additional filtering of capacitor C_p are considered [14]. The time and frequency response of the PLL will be essentially the same as a second order PLL and can be analyzed with second order classical control system methods [14].

2.2.5 Frequency Divider Transfer Function

The transfer function of the frequency divider is given by [10]

$$N = 256 \left(\frac{\frac{rad}{\sec}}{\frac{rad}{\sec}}\right). \qquad 2.5)$$

The division factor N is the value of the PLL's closed-loop frequency gain. A division factor N of 256 is chosen so that the frequency reference can be derived from a highly precise crystal with a resonant frequency of approximately 3.578MHz [16]. The division factor of 256 is large from a PLL phase noise standpoint, but is good from stability against oscillations standpoint. Another advantage of having a large division factor is a lower operating frequency requirement of the reference frequency and phase frequency detector.

2.2.6 PLL Closed Loop Analysis

The expression for the closed loop PLL system response under locked conditions can be found using the transfer functions for the individual PLL sections. The transfer functions for the individual sections can also be used to determine which sections can be changed to improve PLL performance. The loop transmission is found by breaking the loop at the output of the frequency divider and finding the ratio of a test phase signal to the return phase signal as given by

$$|T(s)| = \frac{K_V \cdot I_P \cdot Z_F(s)}{2 \cdot \pi \cdot N \cdot s}. \qquad (2.6)$$

Using the loop transmission, the equation of the closed-loop phase transfer function can be found and is [14]

$$\frac{\theta_{in}(s)}{\theta_{reff}(s)} = H(s) = \frac{\frac{K_V}{N} \cdot I_P \cdot R \cdot \left(\frac{b-1}{b}\right) \cdot \left(s + \frac{1}{\tau}\right)}{\frac{s^3 \cdot \tau}{b} + s^2 + \frac{K_V}{N} \cdot I_P \cdot R \cdot \left(\frac{b-1}{b}\right) \cdot s + \frac{K_V}{N} \cdot I_P \cdot R \cdot \left(\frac{b-1}{b \cdot \tau}\right)}. \qquad (2.7)$$

The third pole created by the additional capacitor C_p is located at located at $s = -b/\tau$ [14]. The location of the third pole and is designed to be at a much higher frequency than the bandwidth of the PLL and approximations for the natural frequency and the damping factor can be made using second order equations. The natural frequency of the closed loop PLL is given by [14]

$$\omega_n \approx \sqrt{\frac{K_V \cdot I_P}{2 \cdot \pi \cdot N \cdot C}}. \qquad (2.8)$$

The natural frequency of the PLL is also equal to the correction bandwidth of the PLL [18]. The correction bandwidth is the frequency range over which the PLL can track and correct for any phase or frequency deviations. The correction bandwidth of the third order

PLL for the BBIC transmitter was chosen as 1% of the reference frequency, approximately 35 kHz. This 35 kHz correction bandwidth is sufficient to properly compensate for the phase noise of the VCO. The third pole created by the additional capacitor C_p is located at $15\omega_n$ and is sufficiently high to avoid stability against oscillation problems. The damping factor of a closed loop is a measure of a system's transient response to a step input in the PLL's reference frequency.

The damping factor is given by the following approximation [14]

$$\zeta \approx \frac{\tau}{2} \cdot \sqrt{\frac{K_V \cdot I_P}{2 \cdot \pi \cdot N \cdot C}}. \qquad (2.9)$$

The value of ζ for the third order PLL is $1/\sqrt{2}$ to form a critically damped system. The lock or acquisition time for the PLL is the time required for the PLL to acquire phase lock and track changes in the reference frequency is given by [10]

$$T_L \approx \frac{1}{4.5 \cdot f_n}, \qquad (2.10)$$

where f_n is the correction bandwidth of the PLL. T_L is a measure of the settling time of the step response of the closed-loop phase transfer function. Since the acquisition time of the PLL is inversely proportional to the correction bandwidth a large bandwidth requires less time to acquire phase lock. With a correction bandwidth of 35kHz, the acquisition time of the PLL is approximately 20μs and is sufficient for the BBIC transmitter [10].

2.3 Digital Phase frequency Detector

The phase frequency detector (PFD) compares the frequency dividers output to the frequency reference [18]. A simplified model of the PFD is shown in Figure 6. The

PFD detects the phase difference of the reference frequency and divider output by the measuring the time difference between pulses at inputs A and B. This time difference between the input pulses measures the phase difference between the input signals A and B. The phase frequency detector has a phase detection range of $\pm 2\pi$. The outputs Q_A and Q_B have a pulse width equal to the phase difference between the two input signals.

The PFD circuit is a synchronous tri-state machine where only Q_A or Q_B can have a high logic state as shown in Figure 7. When the phase of signal A leads signal B and ω_A equals ω_B the output signal Q_A will transition low to high with the rising edge of signal A and reset to low with the arrival of signal B. The pulse width of Q_A is the time measurement of the phase difference between A and B and will remain constant as long as ω_A equals ω_B. The output signal Q_A injects current into the loop filter for a time equal to the pulse width of Q_A and causes the VCO control voltage to increase. The complement can be said about the case when the phase of signal B leads signal A and ω_A equals ω_B. A pulse of current will be removed from the loop filter for a time equal to the pulse width of Q_B and the VCO control voltage will decrease.

When a difference between the frequencies of signals A and B exists, the operation of the PFD increases the pulse width of the output pulse providing a frequency comparison between the input signals. Large pulse widths from the PFD cause large transient voltage spikes across the loop filter. These spikes cause small changes in the operating frequency of the VCO and produce side bands in the PLL output spectrum with frequency offsets of $f_o \pm f_{reff}$, where f_{reff} is the frequency of the reference oscillator. The additional parallel capacitor C_P filters the transient spikes and stabilizes the VCO control voltage. A more effective method of filtering the switching transient spikes would be to

use a fully differential charge pump. The spikes are a common mode signal and will be greatly suppressed by a fully differential system [18].

The two inverters in series with the output of the AND gate eliminate a phenomenon call dead zone [18]. PFD's, when operating with a very small phase difference between signals A and B, produce very small output pulses on signals Q_A and Q_B. These output pulses with very small pulse widths produce very small changes in the VCO control voltage. This greatly reduces PLL lock in range when very small phase differences exist between the input signals. The addition of the inverters introduces two propagation delays in the reset path of the D flip-flops. This delay increases the minimum output pulse width when the input signals have a very small phase difference [18].

2.4 Charge Pump Complementary Current Source and Switches

The output signals Q_A and Q_B are converted to a slowly varying signal with a tri-state charge pump. Charge is removed or accumulated on the capacitor C and generates the control voltage for the VCO via output pulses from the PFD. Charge accumulates on the capacitor C and the control voltage increases when Q_A is pulsed high and charge is removed and the control voltage decreases when pulses occur on Q_B with every phase comparison.

A current source is needed to generate the pump current for the charge pump PLL. The current source must be very precise to maintain a constant complementary current over a wide range of output voltages. Changes in output current with changing output voltages would result in variations in the current and would change the bandwidth and damping factor of the PLL as predicted by Equations 2.8 and 2.9. The current source

chosen to implement the pump current for the charge pump is a complementary wide-swing current mirror [17] as shown in Figure 8. Node 60 and 50 in Figure 8 represents Ip+ and Ip- in Figure 4. The current source was design to source or sink a constant current of 10uA over an output voltage swing of 0.1 volts of the rail voltages. A problem implementing the current source with a wide-swing current mirror is the current mirror feedback networks affect PLL loop stability against oscillations by adding additional poles to the closed-loop PLL. The wide swing current mirror topology uses negative feedback to produce the output current [17]. Negative feedback in the current mirrors band limits the output current, where band limiting acts as a low pass filter. This low pass filtering of the pump current adds poles to the PLL closed loop bandwidth. The added stability problem was improved by designing the current sources with small channel lengths, which improves the current mirrors frequency response. The closed loop bandwidth of the current source is much greater than the closed loop bandwidth of the PLL, so the frequency effects of the current sources can be neglected in the PLL analysis. The complementary wide-swing current source device sizes are initially chosen with Equations from [17], and finalized with simulations (see Appendices 3-4). Results from simulations show that the complementary current source meets design requirements of constant output current to within 0.1 V of the voltage rails as shown in Figure 9. The simulation and circuit and netlist files used to simulate the current source are given in Appendices 3-4. Figure 9 shows output currents I_p+ and I_p- versus output voltage.

The switching network in the charge pump PLL is designed to apply the pump current to the load or dump the pump current into a dummy load as shown in Figure 10. Dumping the pump current into a dummy load improves the transient response of the

loop filter [18]. The switches are designed to minimize the on resistance of the switches, which reduces unwanted voltage drops in the VCO control voltage. Minimizing the on resistance of the switches requires a small channel length and large channel width. These choices of device sizes result in poor charge injection performance, but adding the additional parallel capacitor to the loop filter acts as a filter to reduce the transient effects of switch charge injection [14]. Charge injection from the switches can be modeled as the switching transients in the PFD and produce side bands in the PLL output spectrum at $f_o \pm f_{reff}$.

2.5 Frequency Divider Design and Analysis

The division function was implemented with an eight-stage divider consisting of digital dividers, standard cell DFF divide-by-2 stages, and current mode logic (CML) [18] divide-by-2 stages. The first three-divider divide-by-2 stages are implemented with current mode logic (CML) D flip-flops, which divide the input frequency, by a factor of eight. The remaining five divide-by-2 stages are implemented with standard cell D flip-flops. In the basic operation of the divider, the output of each divide-by-2 stage is connected to the clock input of the following stage. The inverted flip-flop output is fed back to its D input and divides the clock frequency by a factor of two for each stage resulting in a total division factor of 256. The clock input of the first CML stage is connected to the VCO output.

The CML D flip-flops used in the first three stages of the frequency divider are of current steering topology consisting of a differential pair and a regenerative pair as shown in Figure 11 [18]. These CML D flip-flops provide high-speed operation and, with proper

device sizes, result in a superior power-speed performance at 916 MHz compared to digital frequency divider circuits. A disadvantage of the CML DFF is the clock and "not" clock input must be precisely complementary [18].

The CML frequency divider operates by latching the clock signal, with transistors M9, M10, M17, and M18, when the "not" clock is high and holds the output constant until the next clock pulse. The major design issues concerning the CML are power consumption and minimum allowable input signal power. The minimum allowable input signal is the input, which can turn on the latch circuits. The small signal voltage gain of the CML divider is given by [28]

$$A_V = \frac{2}{\pi} \cdot g_m \cdot R_L, \qquad (2.11)$$

where g_m is the transconductance of the lower differential pairs (M5, M8 and M13, M19), R_L is the effective load resistance (M1, M2 and M11, M15), and it is assumed that the differential D input is a square wave. The circuit will operate correctly as long as the differential voltage at the latch is large enough to activate the latch circuits, gates (M9, M10 and M17, M18). The current switching characteristics of the CML DFF divider are related to the large signal voltage-current relationship of the clock input differential pairs (M5, M8 and M13, M19). Large W/L ratios in the clock input differential pair allows current switching between the differential devices at lower input voltages compared to devices with smaller W/L ratios. This is because larger W/L ratios have larger transconductance for a given bias current.

The CML DFF divide-by-2 circuits were designed for a minimum allowable input signal of –15dBm ≈ 112mVpp on the first and most important stage of the frequency

divider. The device sizes were optimized using HSPICE simulations to achieve proper operation with a clock input signal of –15dBm. HSPICE results show that the divide-by-2 circuit operates correctly with an input frequency of 1 GHz and clock input signal power of –15dBm as shown in Figure 12 (see Appendices 3-4). The successive CML divider stages are identical to the first CML divide-by-2 circuit. The bias current for the two following stages is reduced to lower the divide by 256-frequency divider's total power consumption. The second CML divider's bias current was chosen as 75% of the first CML stage and the third CML stage is 50% of the bias current of the first stage.

The following eight stages of the divide-by-256-frequency divider are standard cell DFFs without reset inputs [18]. The transition from the fully differential CML divide-by-2 circuits to the single-ended standard cell DFF is implemented with a simple differential amplifier as shown in Figure 13. The differential amplifier's inputs are connected to the differential output of the third stage of the CML frequency dividers and the single-ended rail to rail output is taken from the inverting side of the differential amplifier. The design of the differential amplifier is greatly simplified because its operating frequency is approximately 125MHz and it is only used as a rail-to-rail input to a standard cell DFF. The eight following stages of divide by two circuits are easily implemented with the standard cell DFFs because their maximum required operating frequency is approximately 125MHz which is much lower than their maximum allowable operating frequency of approximately 500 MHz for the HP 0.5μm process [16]. The complete divide-by-256 circuit was simulated with HSPICE from a layout extracted netlist file with a –15dBm 1GHz input signal. Results from HSPICE show that the circuit

correctly divides the 1GHz signal by 256 with a power consumption of 29mW as shown in Figure 14 (see Appendices 3-4).

2.6 VCO Design Overview

The voltage-controlled oscillator used in the BBIC transmitter is a negative gm LC oscillator [18]. The oscillator was implemented with an external LC tank circuit to achieve good phase noise performance [19-24]. Tuning the oscillator's operating frequency is accomplished with external varactor diodes [25-26]. The complete design and analysis is presented in Chapter 3. The VCO is designed for a tunable frequency range of 100 MHz with the operating frequency of 916 MHz close to the center of the range. The total range of the oscillator's control voltage is from 0.1V to 3.2V for a ΔV_c of 3.1V. The gain of the VCO is given by [10]

$$K_V = \frac{2 \cdot \pi \cdot 100 \cdot 10^6}{3.1} = 202.58 \cdot 10^6 \frac{rad/s}{Volt}. \qquad (2.12)$$

2.7 Complete PLL System Design

Table 2.1 gives a listing of the PLL parameters required to design the PLL. Using these values, the stability analysis of the PLL can be evaluated using Equations 2.6 and 2.7. Figure 15 is a MathCAD plot of the loop transmission of the PLL versus frequency. The loop transmission has a large gain at low frequencies. This large gain allows for fast correction of the steady state operating frequency of the VCO when small frequency deviations occur. This large loop gain forces the operating frequency of the VCO to precisely match the multiple of 256 of the reference frequency. The magnitude of the loop gain also decreases as the operating frequency approaches f_n. This decrease in the

loop gain causes slower corrections to the VCO's operating frequency as the VCO's frequency deviations from the operating frequency become large. The stability against oscillations for the PLL is indicated by the phase margin of the loop transmission. Since the third additional pole was located at a much higher frequency than f_n, the phase margin can be calculated with second order control system techniques and becomes [30]

$$\Phi_m = \tan^{-1}\left(\frac{2\cdot\zeta}{\sqrt{\sqrt{4\cdot\zeta^4+1}-2\cdot\zeta^2}}\right). \qquad (2.13)$$

Table 2.1 PLL Design Parameters

Design Parameter	**Value**
VCO Gain K_v	202.58*10^6 (rad/s/volt)
Pump Current	I_p=10uA
Loop Filter Time Constant RC	τ=4.5us
3rd pole location b/τ	5.34 kHz
Natural Frequency f_n	35385 (Hz)
Damping Factor ζ	0.707
C	22.3 pf
C_p	1.58 pf
R	203 kΩ
b	15.1
Division Factor N	256

Using $\zeta = 0.707$, the Φ_m was calculated to be 60^O. The closed loop response of the PLL is analyzed using equation 2.7. Figure 16 is a magnitude plot of the closed loop gain versus frequency. The frequency response of the PLL closed loop transfer function exhibits overshoot to an amplitude of approximately 1.5 [30], which is consistent with a damping factor of 0.707. The additional pole from parallel capacitor C_p does not cause significant deviation from the expected second order closed loop frequency response as shown in Figure 16. The magnitude of the PLL frequency response begins to drop at the value of the natural frequency of the transfer function f_n of 35kHz.

2.8 Phase Lock Loop Simulation

Transient simulation of PLL circuits is very difficult because of the required time resolution and time length to simulate tracking and acquisition (see Appendices 3-4). Most PLL designs are simulated with analog behavioral models where a specific model is used to simulate each loop component of the PLL. Great care must be taken to ensure that the analog behavioral models accurately describe each loop component. The BBIC PLL is simulated from transistor level circuits (see Appendices 3-4).

The PLL was simulated to test complete closed loop system frequency acquisition and tracking operation. The PLL was simulated with sufficient buffer bias currents for the frequency divider, VCO, and VCO buffer to ensure system operation. The VCO was biased to ensure voltage limited operation, and the divider was biased for operation with a –15dBm input signal. The VCO buffer was simulated with a 50 Ω load. The simulation was run for a sufficient time to ensure acquisition and at a time step resolution to sample the 916 MHz output signal. The PLL was simulated in HSPICE with a layout-extracted

netlist to include as accurately as possible the parasitic capacitive loading effects of the integrated circuit. The VCO control voltage approaches the voltage required for a VCO output frequency of 916 MHz as shown in Figure 17. The PLL simulation shows that the PLL is acquiring phase lock as predicted by Equation 2.11. The PLL must operate with a steady state phase error to ensure that the average value of the control voltage is the voltage required to maintain an output frequency of 916 MHz as shown in Figure 18. The steady state phase error of a PLL is analogous to the error signal in negative feedback systems. This error signal is a signal required to offset errors in the negative feedback system. The offset error in the PLL is the control voltage offset error required to generate a VCO output frequency of 916 MHz. Figure 18 shows the VCO control voltage and output signals of the reference oscillator and frequency divider. The phase difference of the reference oscillator and frequency divider is the steady state phase error of the PLL. The dead-zone elimination characteristics of the PFD can be seen in Figure 18 as the small pulses that occur at each low to high transition of the reference frequency pulses. These pulses are also caused by charge injection from the charge pump switches and produce sidebands offset by $\pm f_{reff}$ in the PLL output spectrum. The simulated output frequency is very close to 916 MHz as shown in Figure 19. Simulation results show that the PLL is operating as designed. The PLL was simulated from a startup condition to verify phase lock acquisition and VCO frequency tracking. The estimated average power consumption of the PLL is obtained from an operating point simulation. The total simulated average power consumption of the PLL is 55mW.

2.9 Mixer Analysis and Design

Because a transmission range of only a few feet is required. The BBIC system can be implemented without a power amplifier. The doubly balanced Gilbert Cell multiplier used in the transmitter functions as both a modulator and as a RF amplifier [27]. Utilizing the Gilbert Cell multiplier as an amplifying component saves system complexity and significantly reduces total system power dissipation. Several design issues must be considered when designing a Gilbert Cell multiplier as an up-conversion modulator. The main problem associated with the Gilbert Cell multiplier implemented, as an up-conversion mixer is the mixer is loaded with PMOS active loads. These PMOS load devices limit the multiplier's maximum operating frequency [27], because PMOS devices have a lower unity current gain frequency compared to NMOS devices. Replacing the PMOS active loads with resistors R1 and R2 as shown in Figure 20, adds gain without the frequency limiting effects of the PMOS devices [27]. Adding load resistors to the Gilbert Cell multiplier allows for operation as both an up-conversion and down-conversion mixer with GHZ IF frequencies.

The digital sensor data is directly up converted to 916 MHz to transmit as a BPSK message. The direct conversion operation of the Gilbert Cell multiplier requires that transistors M3-M6 (see Figure 20) act as switches to produce the 180^{O} phase shifts of the carrier. A simple model of the mixer when operated, as a BPSK modulator is the load resistors connected directly to the drains of the RF section transistors M7-M8, and the circuit is connected as a standard differential amplifier with a voltage gain of gmR_L. This model, although simple, is not correct because the abrupt switching action of transistors M3-M6 and the actual voltage gain of the mixer is given by [28]

$$A_V = g_m \cdot R_L \cdot \left(\frac{2}{\pi}\right), \qquad (2.14)$$

where A_V is the mixer voltage gain, g_m is the transconductance of the differential pair M7,M8 (see Figure 20), and R_L is the effective load resistance. Equation 2.12 is a good approximation when the square wave local oscillator voltage driving transistors M3-M6 is large compared to (Vgs-Vt) of the switching transistors M3-M6. Equation 2.12 is the value of the frequency translated first harmonic of the modulating square wave multiplied by the differential voltage gain of differential pair M7-M8 [15].

Transistors M7 and M8 form the RF input differential pair, where the RF local oscillator is connected. Large input devices also load the on-chip local oscillator, necessitating a VCO output buffer to drive the large capacitance associated with the input devices. Input devices M7, M8 also contribute to the mixer 1dB input compression point, defined as the input signal power required to decrease the gain by 1dB. Large input signals cause the input differential pair to switch abruptly, losing linearity in the output.

Another very important specification of a direct conversion transmitter is carrier feed through. Carrier power is transmitted in a BPSK transmitter when DC offsets exist in the input differential pair M7-M8 of the mixer. Carrier feed through occurs because the zero frequency DC offset signal is multiplied with the carrier frequency, resulting in a 0 Hz carrier frequency translation. This un-modulated carrier power carries no message information and is considered a spurious signal by ISM standards. The ISM standard for transmission of non-spread spectrum spurious signals is 75μW or –11dBm. These DC offsets are much worse in an active Gilbert Cell type mixer because the circuit operates with several differential pairs. Any offsets in these differential pairs cause carrier feed

through. Carrier feed through is much worse in CMOS transmitters because matching between devices is poor compared to bipolar technology. The disadvantage of any carrier feed through is less power transmission in the BPSK signal because carrier transmission contains no message information. The main design technique to combat the offsets associated with the differential pairs in the mixer is to use common-centroid layout techniques to minimize device mismatch due to process variations. Transistors M7, M8, M3, M4, and M5, M6 (see Figure 20) are laid out using a common-centroid geometry to offset any processing variations. Carrier feed through in the designed mixer was expected to meet the ISM spurious signal requirement of 75μW or –11dBm.

The mixer is simulated in HSPICE from a layout extracted netlist file, which includes parasitic capacitive loading, to verify gain and modulation characteristics (see Appendices 3-4). Applying a –20dBm differential signal to the gates of RF input with transistors M3, M6 connected to 3.3V and the gates of transistors M4, M5 grounded, simulates the mixer's gain. Simulations show that the voltage gain of the mixer and buffer into a 50 Ω load at 0.916MHz is 1.38 V/V, which is a power gain of 1.9dB as shown in Figure 21. Figure 21 shows the buffered output to be greatly attenuated compared to the buffer input due to the body effect and 50 Ω load resistors. The RF buffer circuit M1-M2 and M10-M11 is a simple differential source follower amplifier. The reason a common source amplifier configuration was chosen for its simplicity in implementation, and the circuit also provides a wide band match to the balun transformer. A major disadvantage of the circuit is the body effect. The body effect of the input transistors reduces the transistors transconductance and reduces the circuit's voltage gain to a maximum of 0.8 V/V [15].

Applying a differential digital signal to transistors M3-M6, tests mixer modulation capability. The modulated output signal has 180^{O} phase shifts during digital waveform low to high transitions as shown in Figure 22. The accuracy of the 180^{O} phase shifts is very important when the signal is received and de-modulated. Significant deviations of the 180^{O} transition phases of the BPSK signal lead to spreading of the ideal constellation locations of (±1+j0) [7]. Spreading of the constellation locations of the received BPSK signal can increase the systems bit error rate. Carrier feed through due to DC offsets in mixer differential pair M7-M8 was not simulated in HSPICE because accurate mismatch models from MOSIS were not available.

2.9.1 Mixer Bias Circuit

A 1 V bias voltage is applied to the gates to mixer RF input differential pair transistors M7, M8 with a bias circuit. The bias circuit shown in Figure 23 is simply a differential amplifier with a DC feedback loop to mirror an applied off chip voltage applied at V_{reff} to the capacitively coupled RF inputs as shown in Figure 20. The simulated bias circuit mirrors the externally applied 1.5 V DC bias level to the mixer RF inputs of the mixer to within 30mV as shown in Figure 24 (see Appendices 3-4). This small error is sufficient for proper mixer operation. This circuit allows for minimum capacitive loading of the RF inputs by off chip bias networks. The only loading of the RF input transistors is due to the large output impedance of R3, R4, and transistors M17, M19 and any parasitic capacitance associated with the active and passive devices. The additional loading effects of the bias circuit are small compared to the loading of an off-chip bias circuit. The bias circuit is biased with a 10uA current and does not significantly increase the mixer power dissipation.

2.10 PLL and Mixer Simulation Results

A complete PLL system was designed to be implemented with the HP 0.5μm CMOS process. Table 2.2 is a summary of the performance parameters of the PLL. Analysis indicates that the PLL has a correction bandwidth of 35 kHz, and an average power consumption of 55mW. The PLL was simulated to verify acquisition and tracking of the reference oscillator. Another important feature of the PLL is that the correction frequency and damping factor can be adjusted with the pump current without replacing any loop filter components. The fully balanced CMOS Gillbert Cell multiplier has been implemented in the HP 0.5μm CMOS process. The fully differential mixer provides adequate modulation and gain to provide signal transmission for the BBIC transmitter and mixer specifications are given in Table 2.3.

Table 2.2 PLL Performance Specifications

Specification	Value
VCO-tuning range	100MHz
Acquisition Time	20us
Correction Bandwidth	35kHz
Average VCO Power Consumption (with Buffer)	25mW
Average Frequency Divider Power Consumption	29mW
Average Power Consumption at VDD 3.3V (with VCO Buffer)	55mW

Table 2.3 Mixer Simulated Specifications

Specification	Value
Voltage Gain	1.38V/V
Power Gain – 50Ω system	1.9dB
Modulation at 916MHz	BPSK
Average Power Consumption at VDD 3.3V (with Buffer)	18.8mW

Chapter 3

Voltage Controlled Oscillator VCO Design

A negative g_m voltage controlled oscillator [18] design is used in the PLL with a minimum tuning range of 100 MHz. The VCO consists of a cross-coupled NMOS pair M1, M2 with current mirror M3 as shown in Figure 25. The circuit has an external parallel LC tank for tuning with a fixed inductor value and a varactor diode for self-resonance tuning. An external tank circuit was chosen for its superior quality factor (Q) compared to an integrated tank circuit or a CMOS ring oscillator [19]. Phase noise and power consumption is decreased in a negative g_m oscillator with a tank circuit with a large quality factor because smaller bias currents are required to sustain oscillations and high Q oscillators resist frequency deviations from the operating frequency.

The inductance and the varactor diode capacitance set and control the operating frequency and tuning range of the oscillator along with any stray capacitance connected in parallel with the tank circuit. The largest contributor to the stray capacitance is the chip's parasitic capacitance and is approximately 1.5pF. The next largest contributor to the tank's parasitic capacitance is that associated with the cross-coupled devices M1-M2 and is approximately 0.5pF per device. The required capacitance value with a 4.9nH inductor is 6.16pF for an operating frequency of 916MHz. These low parasitic contributions to the tank's capacitance allow for a comfortable margin of adjustability in the tuning range of the oscillator.

3.1 Modeling Real Parallel LC Tank Circuits

A critical component in this VCO configuration is the tank circuit. An LC tank circuit is characterized by its quality factor where a high quality factor is desired; this quality factor is described as the unloaded Q where the tank circuit is connected in parallel with an ideal current source. Several definitions of the quality factor of a RLC tank circuit are shown in the following Equations [12]

$$Q = \frac{2 \cdot \pi \cdot Energy\ Stored\ per\ Period}{Energy\ Dissipated\ per\ Period}, \tag{3.1}$$

$$Q = \frac{\omega_0}{BW_{\ 3dB\ Bandwidth}}, \tag{3.2}$$

$$Q = \frac{1}{2} \cdot \frac{d\theta}{d\omega}_{\omega=\omega_0}, \tag{3.3}$$

where Q is the quality factor of the tank circuit, ω_0 is the resonant frequency of the tank circuit, BW is the 3dB bandwidth of the circuit, and $d\theta/d\omega$ is the rate of change of the tank circuit's phase with respect to frequency evaluated at ω_0.

An ideal LC tank circuit with lossless components has an infinite quality factor, which simply means that no energy is lost in the tank circuit. A surface mount low loss inductor was used in the oscillator tank circuit. A surface mount varactor diode was used as the variable capacitance in the oscillator tank circuit. Real LC tank circuit components exhibit losses due to parasitic series resistances of the inductor and capacitor. These parasitic losses degrade the quality factor of an LC tank as shown by [12]

$$Q = R_P \cdot \sqrt{\frac{C}{L}}, \tag{3.4}$$

where R_P is the parallel equivalent tank resistance, and C and L are the varactor capacitance and surface mount inductance values of the RLC tank circuit. The parasitic series resistance of the tank circuit's varactor capacitance and surface mount inductor can easily be transformed into an equivalent parallel resistance as shown by [12]

$$R_{PL} = \frac{\omega_0^2 \cdot L^2}{R_{SL}}, \tag{3.5}$$

$$R_{PC} = \frac{1}{\omega_0^2 \cdot C^2 \cdot R_{SC}}, \tag{3.6}$$

where R_{SL} is the series parasitic resistance of the inductor, R_{PL} is the transformed parallel resistance of the inductor; R_{SC} is the series resistance of the capacitor and R_{PC} is the transformed parallel resistance of the capacitor. The circuit model for a transformed real parallel RLC circuit is shown in Figure 26. The total parallel resistance across the LC tank circuit is given by the parallel combination of R_{PL} and R_{PC}: [12]

$$R_P = \left(\frac{1}{R_{PL}} + \frac{1}{R_{PC}} \right)^{-1}. \tag{3.7}$$

The equivalent parallel resistance across the tank circuit in terms of the tank's circuit elements is given by

$$R_P = \frac{L^2}{C \cdot L \cdot R_{SC} + R_{SL}/\omega_0^2}. \tag{3.8}$$

Equation 3.6 shows that any series parasitic resistance of the capacitor significantly decreases the equivalent parallel resistance across the LC tank and suggests that the capacitance should be minimized when setting the resonant frequency of the RLC tank circuit.

3.2 Cross-Coupled NMOS Pair

The cross-coupled NMOS pair can be analyzed with hybrid-π technique's models a negative impedance to the parallel RLC circuit, where oscillation begins when the negative impedance of the cross-coupled devices equals the parallel parasitic resistance of the tank circuit as shown in Figure 27. Figure 27 shows that the gate to drain capacitance of each cross-coupled device is added in a parallel combination. The negative impedance developed by the cross-coupled pair replenishes the energy lost in the tank circuit. The differential negative impedance is controlled by the bias current and is ideally $-2/g_m$, but when device capacitance is considered in the analysis, the differential impedance seen looking into the cross-coupled devices is given by

$$Z_{IN} = \frac{2 \cdot r_O}{1 - g_m \cdot r_O + j \cdot \omega \cdot r_O \cdot \left(C_{gs} + 4 \cdot C_{gd}\right)}, \tag{3.9}$$

where r_o is the output impedance of a single NMOS transistor in the cross-coupled pair, C_{gs} is the gate to source capacitance, and C_{gd} is the gate to drain capacitance. Further it is assumed that r_{o1} equals r_{o2}, C_{gs1} equals C_{gs2}, and C_{gd1} equals C_{gd2} (see Figure 27). The differential impedance Z_{in} is converted to a signal ended impedance with a division by 2. Connecting the single ended $Z_{in}/2$ in parallel with the parallel RLC circuit creates the complete model of the oscillator and the impedance of the RLC tank circuit becomes

$$Z_{IN\,Tank} = \frac{j \cdot \omega \cdot L}{1 + j \cdot \omega \cdot L \cdot \left(\frac{1}{R_P} + \frac{1}{r_O} - g_m\right) - \omega^2 \cdot L \cdot \left(C + C_{gs} + 2 \cdot C_{gd}\right)}. \tag{3.10}$$

When the RLC tank is connected in parallel to the cross-coupled pair, the parasitic resistance of the tank is ideally canceled and the RLC tank circuit achieves an infinite quality factor. Adding the negative impedance in a parallel connection to the RLC circuit

is equivalent to moving the left half plane poles of Z_{inTank} into the right half plane as shown in Figure 28 [21]. Equation 3.10 shows that the conditions for oscillation at the LC tank circuit's resonant frequency is given by

$$g_m \geq \frac{1}{R_P} + \frac{1}{r_O}, \qquad (3.11)$$

where g_m cancels the first order ω term and causes the impedance of the tank to approach infinity at ω_o. The operating frequency of the oscillator is obtained from Equation 3.10 becomes

$$\omega_0 = \frac{1}{\sqrt{L \cdot \left(C + C_{gs} + 2 \cdot C_{gd}\right)}}. \qquad (3.12)$$

Equation 3.12 shows that the operating frequency of the oscillator is lowered by the parasitic gate to source and gate to drain capacitance. Figure 28 shows the pole locations of the oscillator when the transconductance of the cross-coupled devices is greater than and equal to the inverse of the parallel combination of R_p and r_o, and the regions of operation of the oscillator. Operating the cross-coupled devices with a transconductance greater than two times the inverse of the parallel combination of R_p and r_o, the poles of the system are moved to the right half plane and the oscillator is operating in the voltage limited state. Oscillator voltage limited operation occurs when the power supply voltage limits the maximum output signal amplitude. Operating the cross-coupled devices with a transconductance equal to two times the inverse of the parallel combination of R_p and $2r_o$ the oscillator is operating in the current limited state. Oscillator current limited operation occurs when the output signal amplitude is limited to the voltage drop across the parallel

resistance of the tank circuit. The quality factor (loaded Q) of the RLC tank when connected to the cross-coupled devices becomes

$$Q = \omega_0 \cdot \frac{R_P \cdot r_O}{r_O + R_P - g_m \cdot R_P \cdot r_O} \cdot \left(C + C_{gs} + 2 \cdot C_{gd}\right), \qquad (3.12)$$

where equation 3.12 is only valid for g_m less than or equal to the inverse of the parallel combination of R_P and r_o, because Equation 3.12 shows the loaded Q becomes negative for g_m greater than the inverse of the parallel combination of R_P and r_o.

A major design consideration for a LC tank circuit is the dependence of the quality factor on the parasitic resistance of the passive components. The parasitic series resistance in the inductor and varactor diode contribute to losses in the tank circuit, which lowers the tank circuit's Q. Equation 3.6 shows that the capacitor's series resistance significantly reduces the parallel equivalent resistance for a lossy LC tank circuit. Since the quality factor of an LC tank circuit is directly proportional to the parallel resistance of the RLC tank a designer should always design for a dominant or largest inductance value when designing an LC tank circuit and chose an inductance with small series parasitic resistance.

3.3 Large Signal Consideration of VCO

Adding a current source M3 to the cross-coupled pair allows larger amplitudes in the differential output voltage where the maximum peak-to-peak voltage is $V_{max}=2I_{M3}R_p$ to a maximum value of $2V_{DD}$ compared to a cross-coupled pair connected directly to ground where $V_{max}=V_{DD}$ [13]. The current mirror M3 allows for the bias current to be completely switched between the devices in the cross-coupled pair. This switching

doubles the bias current in the cross-coupled devices and produces a factor of two increases the voltage drop across R_p compared to a cross-coupled pair connected directly to ground. The maximum value of the differential output voltage is valid as long as either of the cross-coupled devices are operating in the saturation region. When the output voltage drives the either of the cross-coupled devices into the linear region, the transistor acts as a resistor connected in parallel with the tank circuit. This resistor degrades the tank's quality factor by decreasing the equivalent parallel resistance of the tank and stops the oscillation. This is referred to as voltage limiting.

3.4 Oscillator Noise Consideration

This increased voltage swings at the differential output lowers the phase noise of the oscillator. The theory of phase noise is difficult because the noise transfer functions are time varying where as present simulators like HSPICE only allow for time invariant noise analysis. A simple study of phase noise in negative g_m LC oscillators has been completed and predicts the phase noise of an ideal negative g_m LC oscillator with normalized mean-square noise voltage to the mean-square carrier voltage as given by [12]

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{2 \cdot k \cdot T}{P_{sig}} \cdot \left(\frac{\omega_0}{2 \cdot Q \cdot \Delta \cdot \omega}\right)^2\right), \qquad (3.15)$$

where P_{sig} is the output power of the oscillator, k is Boltmans constant, T is the temperature in Kelvins, Q is the loaded quality factor, ω_o is the operating frequency of the oscillator, and $\Delta\omega$ is an offset frequency relative to the operating frequency. The units of Equation 3.15 are in dBc/Hz and predict the noise power relative to the carrier power

at a specified offset frequency. Results of this equation show that the noise power is reduced by a larger signal swing at the output, and a large quality factor. This result is intuitive because one of the definitions of the quality factor states that a large value of Q resists changes in output frequency with respect to phase change and a larger output voltage swing simply increases the output signal to noise ratio. A more detailed study of phase noise was conducted by Hajimiri and is described by the Hajimiri Model [12]. This model takes an oscillator's time-varying transfer function into the analysis of the phase noise of an oscillator and will not be discussed here in great detail. A disadvantage of using the cross-coupled pair with current source M3 1/f noise directly up-converts to the operating frequency. V_{dsat} of the current source M3 limits the maximum output voltage. This reduction in output voltage amplitude is analogous to a reduction in output voltage signal to noise ratio. The disadvantage of using a current source is a tradeoff because the additional current mirror allows for a factor of two increase in oscillator output voltage, which decreases the oscillator's phase noise.

3.5 Varactor Diodes

A varactor diode was used to implement the variable capacitor in the LC tank circuit. A model of the varactor diode is shown in Figure 29 [25]. The main components in the circuit are the diode and series resistance of the diode. The model includes both stray parasitic capacitance and inductance [26]. These parasitics generally do not adversely affect the variable capacitance of the diode. The parasitic inductance is very small and will not affect the LC tank circuit until the operating frequency approaches several GHz. The most important parasitic component of the diode is the series

resistance. Varactor diodes are designed to minimize this series resistance because any resistance degrades the quality factor of the LC tank circuit.

The capacitance of the diode is controlled by the applied reverse bias voltage across the diode as given by

$$C = \frac{C_{jo}}{\left(1 + \frac{V_{br}}{V_{bi}}\right)^{M}}, \qquad (3.16)$$

where C_{jo} is the diode's depletion capacitance at zero bias, V_{br} is the applied reverse bias voltage, V_{bi} is the PN junction barrier potential, and M is set by the doping grading coefficient. The diode capacitance ranges from a maximum with zero volt reverse bias and decreases with increasing applied reverse bias. The varactor diode used in the VCO is an Alpha Industries SMV 1247 device designed for low voltage operation [27]. The modeling parameters from the manufacturer are given in Table 3.1 [25].

Table 3.1 Varactor Diode Modeling Parameters

Parameter	**Value**
C_{jo}	9.22pF
V_{bi}	100
M	100
R_s	2Ω
C_p	0.55pF
L_s	1.7nH
Breakdown Voltage	12V

The large values of V_{bi} and M are only used to fit the voltage capacitance curve and are not representative of any physical properties of the diode [25]. Using the parameter values given in Table 3.1, the voltage capacitance curve is show in Figure 30. The

voltage capacitance curve shows that the capacitance decreases up to an applied reverse voltage of five volts. Since the adjustable range of the capacitance is in the range of zero to 5 volts the varactor diode is ideally suited for the BBIC transmitter with a 3.3V power supply.

3.6 LC Tank Circuit with Varactor Diode

The actual LC tank circuit used to tune the operating frequency of the VCO was implemented with a surface mount inductor and the varactor diode. The surface mount inductors were modeled with an ideal inductor in series with a 0.2 Ω resistor. This series resistance value was obtained from the manufacture's data sheet [29]. The available tuning capacitance from Figure 30 is not adequate to achieve the desired operating frequency range of the VCO. The final design of the VCO has series capacitors CT1 and CT2 connected in series with each varactor diode and output of the cross-coupled devices to reduce the diode's capacitance as seen in Figure 31. Another advantage of adding these series capacitors is to ac couple the varactor diodes to the VCO. This ac coupling allows for the tuning voltage or control voltage to be a ground-referenced signal and the only concern is not to apply a sufficiently large reverse bias voltage to exceed the breakdown voltage of the varactor diodes.

The resistors RT1 and RT2 in Figure 31 are used to isolate the VCO control voltage from the tank circuit. The resistance is added in parallel with the LC tank circuit's parallel parasitic resistance. The isolation resistors will not significantly affect the quality factor of the tank circuit as long as the resistors are much larger than the parallel resistance of the tank circuit. A problem using the varactor diodes without the series

capacitors is the reverse bias voltage applied to the diode. This is the voltage difference between the VCO output and the VCO control voltage when using this configuration care must be taken to prevent forward biasing the diodes [18].

3.7 VCO Simulation Results

The VCO was simulated with a layout-extracted netlist in HSPICE (see Appendices 3-4). The VCO was simulated to determine the bias current required for voltage limited operation by simulating the VCO with increasing bias currents until the voltage swing across the tank circuit reaches a maximum value. The simulated required current for the VCO to operate in the voltage-limited region is 2.2mA. Operating the VCO in the voltage-limited region is essential to ensure that the output power remains constant over the tuning range of the VCO as shown in Figures 32 and 33.

The VCO was simulated at the minimum operating frequency by applying a control voltage of zero volts as shown in Figure 32. The VCO was simulated at the maximum operating frequency by applying a control voltage of 6 volts as shown in Figure 33. Applying increasing reverse bias voltage across the varactor diodes simulates the tuning range of the VCO as shown in Figure 34. The simulated tuning range of the VCO with a control voltage range of 0 to 3.3 volts is 118 MHz. The required 916 MHz operating frequency of the VCO is contained within the upper range of the tuning range of the VCO. Nominally the desired operating frequency is centered in the tuning range of the VCO, but an accurate approximation of the package parasitic capacitance was not available. The VCO was simulated with approximately 1.5pF of parasitic capacitance in the LC tank circuit. The maximum operating frequency of the VCO was simulated by

applying a control voltage of 6V, which minimizes the capacitance contribution to the tank circuit from the varactor diodes. The simulated maximum frequency of operation of the VCO is 952MHz as shown in Figure 33. The performance specifications of the VCO are given in Table 3.4. Simulation results show that the VCO and buffer average power consumption of the VCO is 7.3mW with a power supply of 3.3V and 50Ω loads. The Simulated output power into a single-ended 50Ω load is –3.9dBm. The VCO simulations show that the design will meet the system requirements of the BBIC transmitter as shown in Table 3.2.

Table 3.2 VCO Simulated Specifications

Specification	**Simulated Value**	**Calculated Value**
L f_o = 916 MHz	4.9nH	6.8nH
R_{SL}	.2 Ω	.2 Ω
C f_o = 916 MHz	6.2pF	4.44pF
R_{SC}	2 Ω	2 Ω
R_p	359 Ω	696 Ω
Q Unloaded	12.8	17.7
Maximum Frequency	952 MHz	990 MHz
Minimum Frequency	805 MHz	740 MHz
Tuning Range	147 MHz	250 MHz
Tuning Voltage Range	0 – 6 V	0 – 6 V
Pout Differential	-3.9 dBm 50Ω	N.A.
VCO Power Consumption	7.3mW	N.A.

Chapter 4

PLL Subsystem Testing

Three PLL system components and the Gillbert cell mixer have been designed, fabricated, and tested in the HP 0.5μm process. This chapter discusses the experimental results for these circuits. Three chips were fabricated for prototyping the components in the BBIC transmitter. The first prototype chip contained the mixer, while the second prototype chip contained the divide-by-256 circuit, and the third chip contains a prototype VCO. Each chip was tested for functionality and performance and compared with the simulation results.

4.1 Measurement and Testing Techniques

High frequency circuit design requires special equipment and properly designed test fixtures. All printed circuit boards (PCB) are designed to characterize the three chips and fabricated for chip-on board packaging. Care was taken to fabricate 50Ω micro-strip transmission lines for RF signals. All surface mount RF components were carefully mounted on the PCB to minimize signal cross talk between RF signals and maintain equal length traces where possible. All transmission lines were properly terminated with conjugate matching networks for maximum power transfer.

All baseband measurements were evaluated with a Tektronix TDS 360 digitizing oscilloscope for time domain analysis. A Hewlett Packard 8656A RF signal generator was used as synthesized RF carrier signals for mixer and divider testing. A Hewlett

Packard 899411A Vector Signal analyzer was used as a spectrum analyzer to measure RF spectral performance and analyze directly inserted and transmitted BPSK signal demodulation. A Hewlett Packard 8753C network analyzer was used to measure scattering parameters for component characterization. Hewlett Packard E4747-10010 Touchstone software was used to capture network analyzer scattering parameter measurements.

4.2 Individual Transmitter Component Testing

Each transmitter system component was characterized to ensure proper operation when integrated into the complete BBIC transmitter. Some circuit nodes were inaccessible due to RF loading and shielding effects. Circuit performance evaluations where inaccessible nodes presented problems were evaluated with secondary measurements if possible.

4.3 Mixer Characterization

The mixer prototype test board was designed to allow access to the bias control, differential RF input/output, and differential baseband input as shown in Figure 35. The layout of the chip and PCB is critical to proper operation. The RF input and output internal nodes are connected to large bonding pads to reduce package parasitics and each RF input and output was separated by one pad on the pad frame to reduce coupling effects. The PCB is constructed from FR4 material using a two-layer board. The board is gold plated to allow for bonding between the chip's bonding pads and the board's traces. The performance of the mixer was tested with board to chip wire bonds

approximately 1.5mm long to minimize stray series inductance. This stray inductance introduces unwanted resonance in the mixer input/output. Each input and output to the mixer requires a differential signal to operate the mixer in a double balanced configuration. A surface mount balun transformer is used to convert the single ended unbalanced input and output test signals to differential balanced signals. The RF input signal is conjugate matched to the mixers differential input by a balanced narrow-band L-type matching network connected to each balanced balun output. The unbalanced balun input is connected directly to a 50-ohm mircostrip transmission line with 3.5mm SMA connectors. The mixer's differential output signal was buffered to the output by a differential common source amplifier and coupled to the balanced balun input. The common source amplifier creates a wideband match to the balun transformer.

A 2.2 V bias voltage was applied to transistors M3-M6, the base band signal input devices, from an external power supply (see Figure 20) and the baseband signal is coupled to the input. A bias voltage of 1 V was used to bias the mixer's RF input devices M7-M8 from the voltage reference amplifier. The mixer was biased with a current of 2.2ma with a 3.3 V power supply; this gives a power dissipation of 7.2mW in the mixer core not including the buffer amplifier. The buffer is not included in the mixer power consumption, because future fabricated mixer circuits will be implemented with matched loads and will not require a buffer amplifier.

The quality of the differential input and output matching networks is measured with scattering parameter measurements using a network analyzer. Network analyzer measurements shows that the L type input differential matching network was a very high quality matching network, and the output differential matching network was wideband

and not as high quality as the input matching network as shown in Figure 36. Results show that the measured input scattering parameter S_{11} is –7dB and the output scattering parameter S_{22} is –7dB at 916 MHz. Network analyzer measurements show that the minimum value of the scattering parameter S_{11} occurs at a frequency of 990 MHz. Network analyzer measurements of the scattering parameter S_{12} indicates that the input/output isolation is less than –50dB as shown in Figure 37. S_{12} measures carrier suppression due to direct carrier feed through caused by coupling between the input and output. Carrier suppression less than –50dB is sufficient to reduce spurious carrier transmission to an acceptable ISM level. Network analyzer measurements show S_{21} is a band pass function of the input matching network and the limited frequency nature of the input RF device's f_t as shown in Figure 38. S_{21} measurements show that the available power gain of the mixer is 8dB at 916MHz.

The 1dB compression point and power gain of the mixer was tested by sweeping the power of the RF input signal until the gain of the mixer decreases 1dB. Also, the mixer's power supply rejection ratio is tested by lowering the power supply voltage to emulate the effects of a discharging battery. The power supply was lowered to 2.8 Volts to simulate a 0.5-volt decrease in power supply voltage. Results of the 1dB compression test indicate that the mixer has a 1dB compression point at an input of –10dBm as shown in Figure 39. The power gain of the mixer is tested with the gate of M3, M6 tied high, and gates M4, M5, (see Figure 20), tied low with constant input signal power less than the 1dB input compression signal. This test configuration emulates a very low frequency digital message. The results of the power gain tests of the mixer indicate a power gain of 8dB for input signals below –10dBm.

Applying a differential digital signal between the gates of transistors M3-M6 performs an operational test of BPSK modulation with a 3.3-volt power supply. The frequency of the differential digital signal is 100 kHz and results in a BPSK signal of 200 ksym/s. Results of the modulation test show that the mixer correctly modulates the 916 MHz carrier with the digital signal. The modulated signal has excellent carrier suppression, and excellent suppression of the even order carrier harmonics and only shows significant power transferred to the odd order harmonics of the digital message as shown in Figure 40. The carrier suppression and even order harmonic suppression is an indicator of the mixer's linearity and shows that the mixer operates with very good linearity. The simulated and measured results are shown in Table 4.1. Results show that the simulated results are pessimistic compared to the measured results for identical bias conditions.

Table 4.1 Gilbert Cell Design Results

Design Parameter	**Simulation**	**Measurement**
Average Power Dissipated Operating at 916 MHz	7.2mW	7.2mW
Power Gain	1.9dB	8dB
1 dB Compression Point	-5dBm	-10dBm

Power gain comparisons are the only parameters with significant differences. The model used to simulate the mixer was a standard BSIM 3V3 CMOS model obtained from MOSIS Corporation (see Appendix 2). The two most likely causes for the difference is an error modeling the output resistance or modeling the body effect of the NMOS devices. A

low NMOS output resistance model would cause a reduction in mixer gain. An error modeling the body effect of the output buffer amplifier would also cause a reduction in simulated gain. The output buffer amplifier is a simple source follower with current source loads. The buffer transistors input gates is directly connected to the mixer's load resistors, so they are biased with at a large DC level. Grounded body wells of the input buffer transistors produce a large source to body voltage. This large body effect will reduce the gain of the buffer stage and must be modeled correctly.

4.4 Frequency Divider Characterization

The frequency divider required the least and most simple characterization procedures of the three prototype circuits. The complete divide-by-256 PLL circuit was fabricated to only allow measurable access only to the differential RF inputs, frequency output, divider bias control, and reference voltage amplifier output. The divider was operated with a 3.3V power supply as shown in Figure 41. The PCB is constructed from FR4 material using a two-layer board. The board is gold plated to allow for bonding between the chip's bonding pads and the board's traces. The performance of the divider was tested with board to chip wire bonds approximately 1.5mm to minimize series stray inductance of the CML divide-by-two circuits. The main characterization measurements of the divider were dynamic range and average power consumption.

The PCB is of the chip-on-board configuration to mimic the fabrication of the complete PLL and BBIC. The differential RF inputs were resistively matched to the surface mount balun transformer for wideband matching to allow testing of the maximum operating frequency without constantly adjusting the matching network for maximum

power transfer. The resistive matching networks are not of high quality as the test setup for the mixer, but saved significant time by allowing real time input frequency adjustment. Matching the balanced balun output to resistively adds noise from the resistors directly to the circuit's input. The divider's output frequency was measured with the Tektronix oscilloscope with a differential 916 MHz RF input signal. Results show that the divider correctly divides the input frequency by a factor of 256. The divider's operating bias current was controlled with a potentiometer and was adjusted to test the minimum power consumption of the divide-by-256 divider with a RF input signal of 916 MHz and was 15mW. The divider's input dynamic range was tested by sweeping the 916 MHz input signal's power level over a range of –30dBm to 0dBm while measuring the output frequency of the divide-by-256 circuit. Results show that the frequency divider operates correctly with an input frequency of 916 MHz and at power levels from –30dBm to 0dBm. To test the divider's maximum operating frequency, the frequency of the input signal and divider's power consumption was increased incrementally while the output frequency remains a factor of 256 of the input signal's frequency. Results show that the maximum operating frequency of the divider is 1.8 GHz with a power consumption of 45mW. The measured results of the divide-by-256 circuit are shown in Table 4.2.

4.4.1 Voltage Reference Amplifier Characterization

The reference voltage amplifier's filtering capacitor C_{poly} (see Figure 20) was placed externally to allow adjustability in case of excessive RF signal coupling into the DC bias point of the CML divide-by-2 stages. The capacitor must be placed off chip because the DC bias voltages applied to the clock inputs of the CML dividers must be isolated from the fractional RF frequencies. This bias voltage is applied simultaneously to

Table 4.2 Divide-by-256 Test Results

Parameter	Measured
Input Dynamic Range	-30dBm – 0dBm
Power Consumption at 916MHz	15mW
Maximum Operating Frequency	1.8 GHz
Power Consumption at 2.1GHz	45mW

the first three CML dividers. Therefore, the reference amplifier must have a frequency bandwidth much less than approximately 125 MHz. This low bandwidth was achieved with an external 100pF filter capacitor, which would consume too much active silicon area, if placed on-chip. Placing the filtering capacitor off-chip allows possible size adjustment and allows accessible testing of the reference voltage amplifier. Applying a DC signal to the amplifier's input M17 (see Figure 20) and measuring the DC voltage across the filtering capacitor tested the reference voltage amplifier functional operation. The feedback of the differential amplifier correctly mirrored the input voltage to the dividers input differential pairs.

4.5 VCO Characterization

The VCO was packaged in a chip-on board configuration to accurately represent the actual packaging of the complete BBIC transmitter. The PCB is designed to allow access to the control voltage input and VCO buffer amplifier outputs as shown in Figure 42. The PCB was constructed from FR4 material using a two-layer board. The board was gold plated to allow for bonding between the chip's bonding pads and the board's traces. The performance of the VCO was tested with board to chip wire bonds approximately

1.5mm to minimize series stray inductance of the CML divide-by-two circuits. The PCB used to test the VCO uses separate microstrip transmission lines for the differential output. Placement of two separate microstrip lines allows testing without the band limiting balun transformer. A single-ended transformer could have limited the transmission of the VCO output if the operating frequency did not lie within the balun's pass band. The parameters of the VCO under investigation were effective LC tank parallel resistance, voltage limited operation bias, power consumption, maximum operating frequency, tuning range, and phase noise. The effective parallel resistance of the LC tank circuit was measured by applying a minimum bias current, which sets the transconductance of the cross-coupled pair to start and sustain oscillations. This current was measured at both the maximum and minimum-operating frequencies to compare with the calculated unloaded Q of the LC tank circuit. This current was used to calculate the transconductance and r_o from the model parameters. Then the effective parallel LC tank resistance can be calculated using Equation 3.11. The minimum current required to start and sustain oscillations at 931MHz was 100uA, and 300uA at 761MHz, which confirms predictions by Equation 3.11. The calculated parallel resistance using Equation 3.4 of the LC tank circuit was approximately 468Ω using L and equal to 4.9nH, 5.9pF at 931MHz and 270Ω using L and equal to 4.9nH, 8.9pF at 763MHz. The capacitance used to calculate Q of the tank circuit was calculated knowing the frequency and inductance. This resistance was used to calculate the unloaded Q of the LC tank. The unloaded Q of the tank circuit from Equation 3.4 was approximately 16 at 931MHz and 12 at 763MHz. Results show that Q unloaded was reduced by 25% over the tuning range of the VCO as predicted by Equation 3.4.

Operating the VCO in the voltage-limited region is required for optimum VCO noise and output power performance. This performance is specified as constant output power versus tuning range and low phase noise. When the output power of the VCO remained constant over the complete tuning range of the VCO, voltage limited operation was achieved. This constant output power maximizes the output signal-to-noise ratio and reduces the VCO's phase noise. Measuring the output power versus tuning range and bias current tested the voltage-limited operating region of the VCO. Results show that the VCO operated with voltage-limited operation with an output power of –15dBm over the tuning range with a 2mA bias current. The DC bias current was measured with an ampere meter in series with the VCO and power supply. A bias current of 2mA results in a VCO power consumption of 6.6mW.

The maximum operating and tuning range of the VCO are interrelated parameters and were tested simultaneously. The maximum and minimum operating frequency is tested by first applying a zero volt control voltage to the varactor diodes to maximize their capacitance. The minimum operating frequency of the VCO was measured to be 768 MHz. Secondly, the maximum operating frequency of the VCO was measured by applying a control voltage of 6 V to the varactor diodes. The maximum operating frequency of the VCO was measured to be 931 MHz. Testing the maximum operating frequency with a control voltage of 6 V practically eliminates the capacitive contributions from the varactor diodes in the LC tank, which results in an almost direct measurement of the LC tank's parasitic capacitance. The parasitic capacitance present in the LC tank circuit was found to be 5.9pF and includes all parasitic contributions from the package,

board, and active/passive components. The parasitic capacitance can easily be calculated from f_o, L and solving for C.

Applying a control voltage of 0 to 3.3V in 0.1V increments as shown in Figure 43 tested the tuning range of the VCO. The cutoff control voltage of 3.3 volts measures the tuning range of the VCO under 3.3V PLL power supply conditions. Results show that the tuning range of the VCO is 119MHz with approximate frequency sensitivity of 2MHz/V and includes the required 916MHz operating frequency.

Phase noise is a measure of the spectral power at a specified frequency offset with respect to the center frequency with a 1Hz bandwidth while operating in the voltage-limited region [24]. The phase noise of the VCO was measure at frequency offsets of 10 kHz and 100 kHz with respect to the operating frequency. The measurements were taken at minimum and maximum operating frequency as shown in Figures 44 and 45. Phase noise measured at these operating frequencies is an indication of the loaded Q of the VCO. The phase noise measured at the minimum operating frequency of approximately 763 MHz was –60dBc @ 10 kHz and –80dBc @ 100 kHz, and -45dBc @ 10 kHz and –60dBc @ 100 kHz at approximately 931 MHz. All phase noise measurements were measured relative to –15dBm single-ended oscillator output power. These results disagree with measurements of the quality factor measurements where the measured higher Q at 931 MHz would reduce the phase noise of the oscillator. This disagreement is most likely caused by jitter introduced in the VCO output frequency due to poor shielding of the test board, which produces a broader output spectrum and can be mistaken as phase noise. Results of the VCO test as given in Table 4.3.

Table 4.3 VCO Test Results

Design Parameter	**Measurement**
Maximum Frequency	931 MHz
Minimum Frequency	763 MHz
Tuning Range	168 MHz
Control Voltage Range	0-6V
Average Power Dissipated	3.3mW
Output Power S.E.	-15dBm
Phase Noise @ 763 MHz	-60dBc @ 10 kHz, -80dBc @ 100 kHz
Phase Noise @ 931 MHz	-45dBc @ 10 kHz, -60dBc @ 100 kHz
Imin @ 763 MHz / Q	300μA, Q≈ 16
Imin @ 931 MHz / Q	100uA, Q≈ 12

Chapter 5

Conclusions and Future Work

A transmitter has been designed with several critical RF sub-circuits fabricated in the HP 0.5μm CMOS process. The transmitter was designed for short-range transmission of a direct conversion BPSK signal. The transmitter contains a complete PLL synthesizer and was simulated for design verification. This chapter summarizes the simulated performance of the PLL, measured results of the sub-circuits, and gives direction for future project progress. The PLL is scheduled for fabrication in the third and final year of the BBIC project. This PLL version will contain the complete transmitter with the sub-circuits optimized for final transmitter specifications.

5.1 Conclusions

Measured results of the Gillbert Cell mixer discussed in Chapter 2 show that the circuit has convincingly demonstrated the ability to transmit the BPSK signal short-distances without a power amplifier. The circuit has a power gain greater than unity and correctly modulates the base-band digital signal. Carrier suppression in the CMOS Gilbert Cell multiplier is a strong function of DC offset due to mismatch between the source-coupled devices and the final version will be optimized to reduce these mismatch effects. The ISM band requires that transmitted power must be less than 75μW or else must use some type of spread spectrum modulation scheme. Carrier feed through would

be considered as a non-spread spectrum signal and must be suppressed below a 75μW level. The mixer as tested meets this ISM specification.

The divide-by-256 circuit discussed in Chapter 2 was also fabricated in the HP 0.5μm process as a proof-of-concept circuit. The three-cascaded current mode logic D flip-flops in the divider allowed for high-speed operation at lower power consumption compared to a single-ended standard cell CMOS DFF. These CML DFFs allowed for frequency division down to a more manageable frequency for the standard cell DFFs. Measured results show that the divide-by-256 circuit operated correctly at 916 MHz with a power dissipation of 15mW and were capable of correct operation at frequencies as high as 1.8 GHz with an average power consumption of 45mW. The only concern for a future version is phase differences between the differential inputs. These phase differences in the differential input cause errors in the first divide-by-2 CML stage. Testing the divider's operating characteristics with phase differences present in the complementary input is very difficult and requires special equipment. The divider as tested provides adequate operation of the BBIC ISM transmitter. Future optimization in the divider could focus on reducing power consumption.

The VCO discussed in Chapter 3 was fabricated in the HP 0.5μm process as a proof-of-concept circuit. The VCO was a current-steered cross-coupled configuration with an external LC tank. The operating frequency of the VCO was controlled with a varactor diode. Measured results show that the tuning-range of the VCO agrees with simulated predictions. The operating frequency of the VCO was measured to be less than the predicted operating frequency of 990 MHz. The reason for this difference was inaccurate modeling of the parasitic capacitance contributed from the test board. Parasitic

capacitance from the test board was estimated at a lower value and thus the operating frequency was lower.

The VCO was over designed with large width cross-coupled devices to ensure oscillatory startup. Results from hand analysis shows that phase noise is directly proportional to the quality factor of the LC tank circuit. The quality factor of the LC tank circuit is greater for a dominant or largest possible inductance value required for resonance. The increased cross-coupled device size added capacitance to the LC tank, thus requiring a smaller inductance to operate at 916 MHz and caused lowering of the loaded quality factor of the oscillator. A drawback of using smaller width cross-coupled devices is that a larger bias current is required to sustain voltage limited VCO operation. Future versions of the VCO could be designed with smaller W/L ratio cross-coupled devices to improve the loaded quality factor of the oscillator with a trade off of higher power consumption.

The complete PLL discussed in Chapter 2 was simulated from a layout-extracted netlist with HP 0.5um models. Simulation results show that the PLL operated correctly and approached a locked condition within the predicted time using Equation 2.10. A shunt capacitor was added to the loop filter to reduce the transit effects from the PFD and switches. This capacitor adds a pole to the PLL system and can be a concern from stability against oscillation viewpoint. The extra pole created by the shunt capacitor was at a sufficiently high frequency to avoid stability against oscillation problems. Future versions of the PLL could be designed with an active differential loop filter. An active differential charge pump and loop filter [18] would suppress the transients from the PFD and switches because these signals would be common mode.

An ISM transmitter for the BBIC has been designed and partially fabricated and convincingly demonstrates correct operation in a fully fabricated transmitter. Each fabricated critical transmitter component operated as designed and is ready for integration into the final transmitter. Several parameters with the transmitter components could be optimized in future versions of the transmitter.

5.2 Future Work

Future work in the realization of the BBIC transmitter is the development of transmitter system specifications, optimization, and digital signal processing. The transmitter system specifications required to implement the final BBIC transmitter are spread spectrum type, bit rate, bit error rate, transmitted power, and power consumption. The distributed sensor array for the BBICs requires the development of a spread spectrum communication topology, which would also require the development of the digital signal-processing scheme for correct operation. Future experiments with the analog signal processing circuits will be used to determine the BBIC system's bit rate. Experiments with the analog signal processing circuits and the biosensor will also determine the acceptable bit error rate of the transmitter. Investigation with the applications of the BBIC transmitters will determine the required transmitted output power and acceptable power dissipation of the wireless transmitter. Future versions of the transmitter will be designed to power down while not transmitting to conserve power.

Several transmitter sub-circuits can be optimized to improve performance to operate with the future system specifications. Future work also includes integrating supply independent bias circuits into the transmitter system.

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Appendices

Appendix 1
Figures

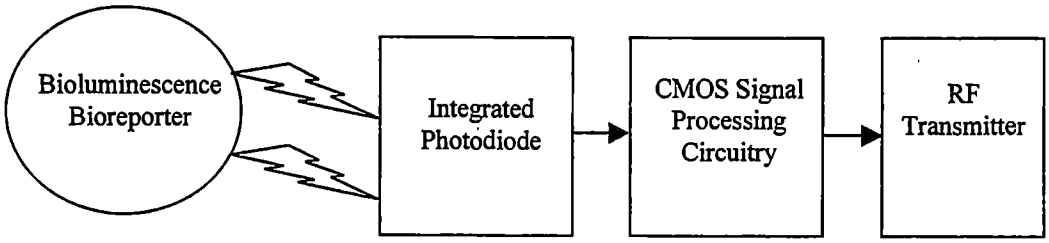


Figure 1 - Block Diagram of Bioluminescent Bioreporter Integrated Circuit

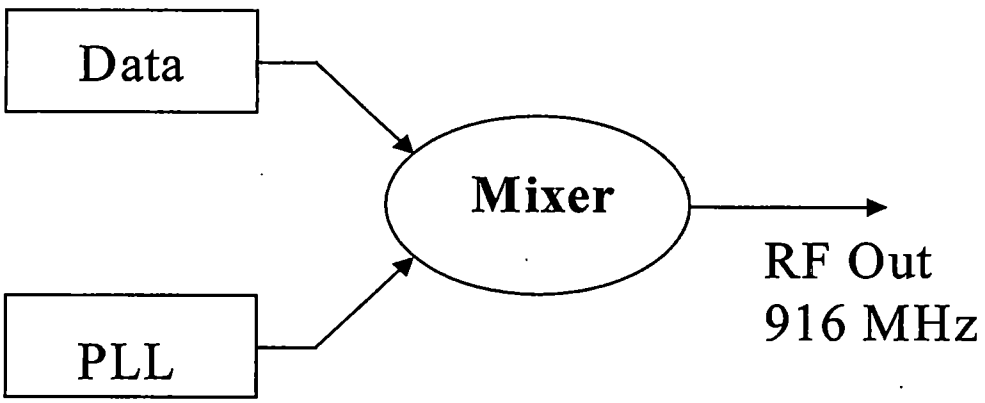


Figure 2 – Block Diagram of BBIC Transmitter

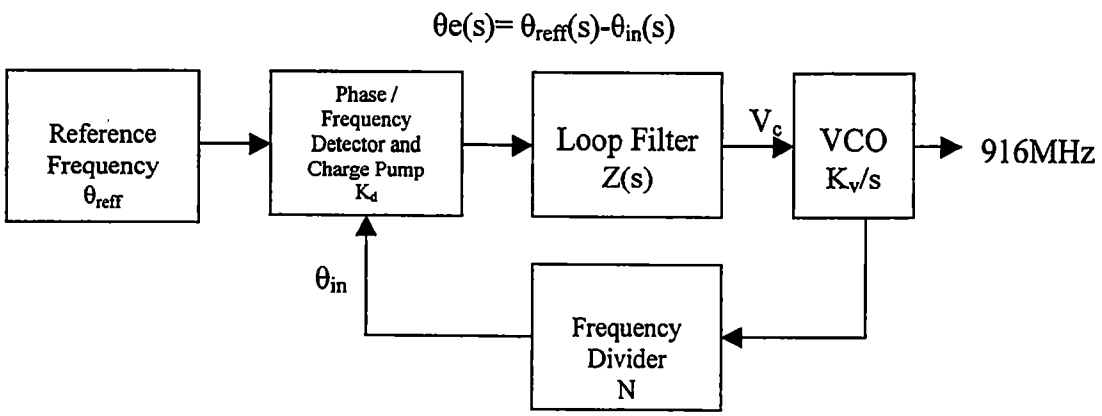


Figure 3 - Modeling Block Diagram of Phase Lock Loop

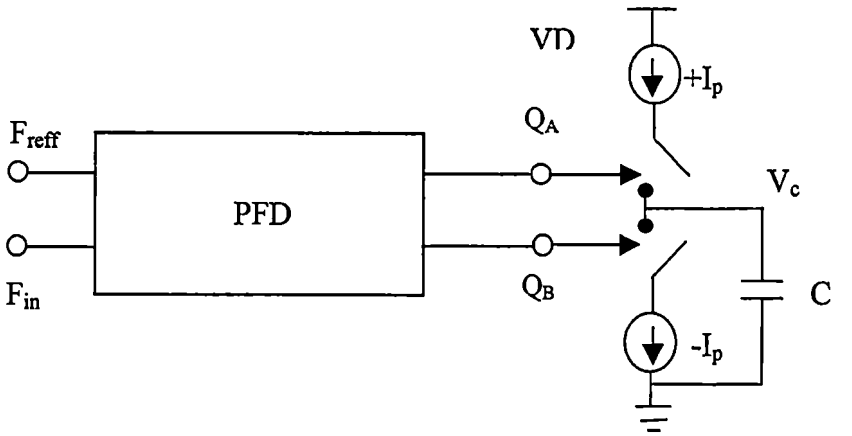


Figure 4 – Simplified Diagram of Charge Pump

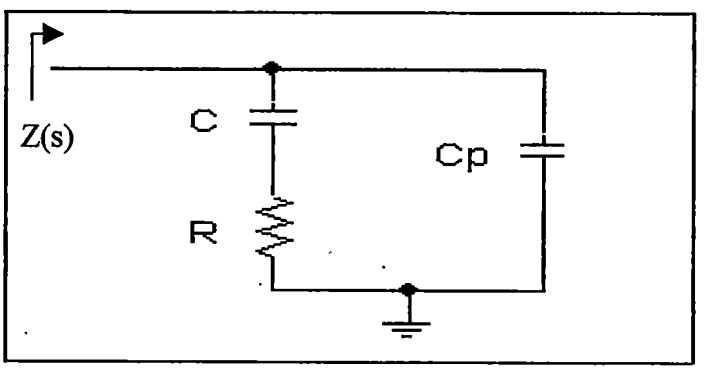


Figure 5 – Diagram of Loop Filter Circuit

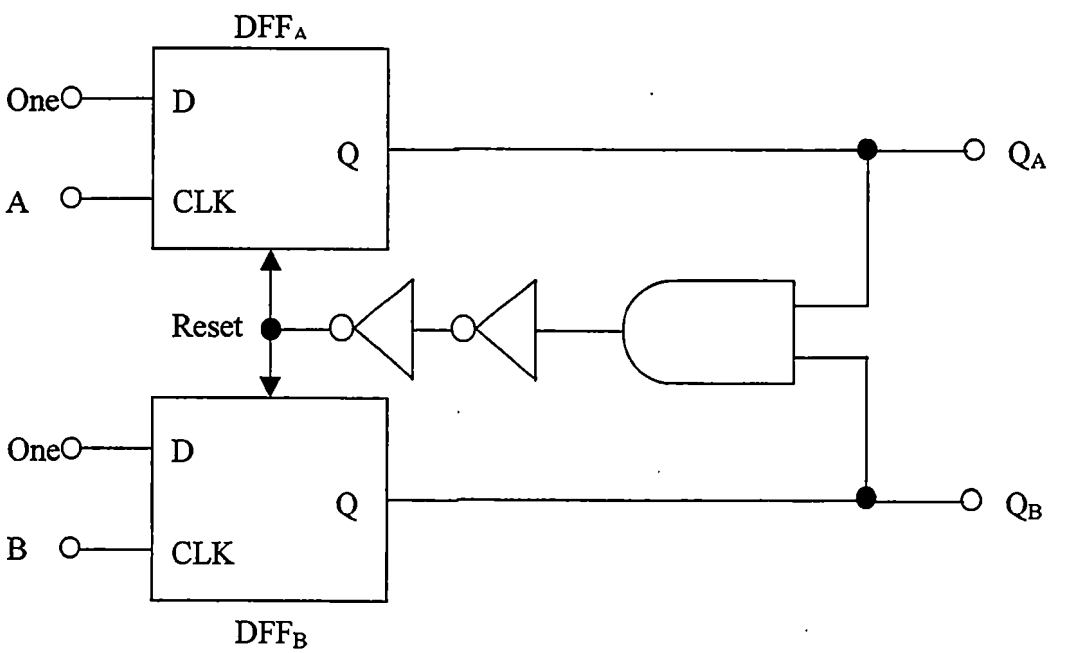


Figure 6 – Diagram of Phase Frequency Detector

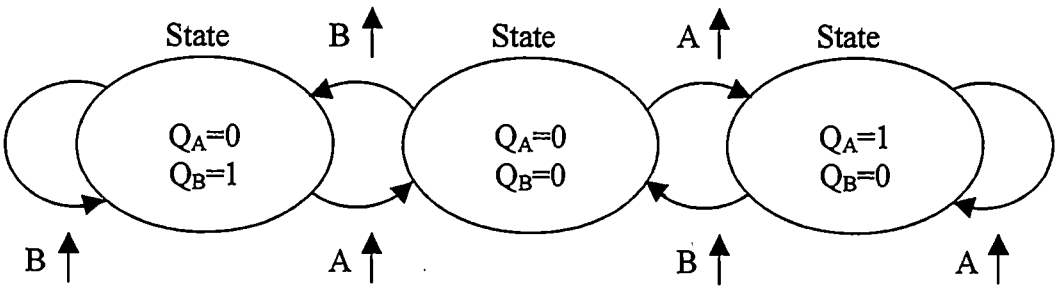


Figure 7 - State Diagram of Phase Frequency Detector

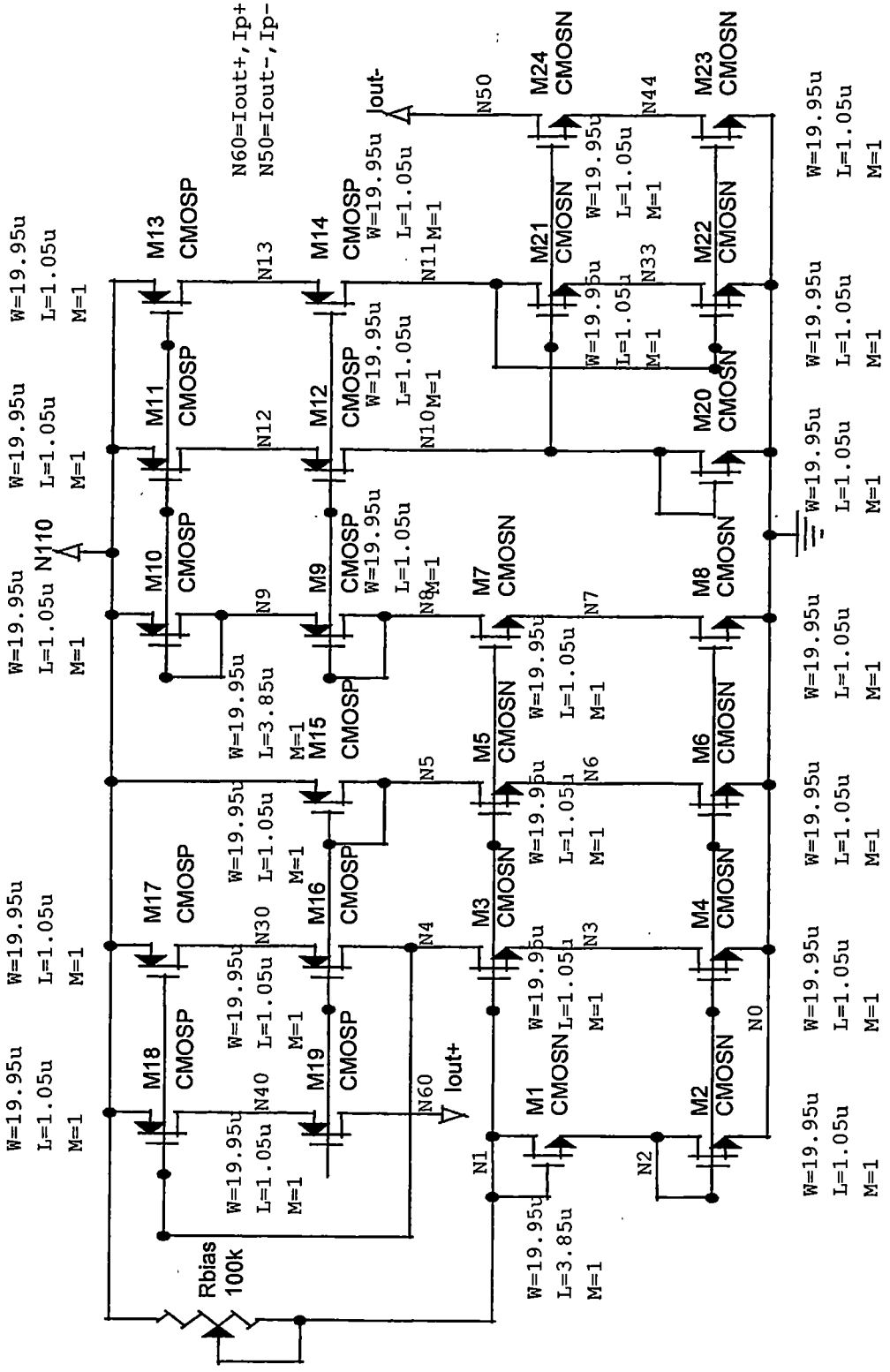


Figure 8 – Complementary Current Source Diagram

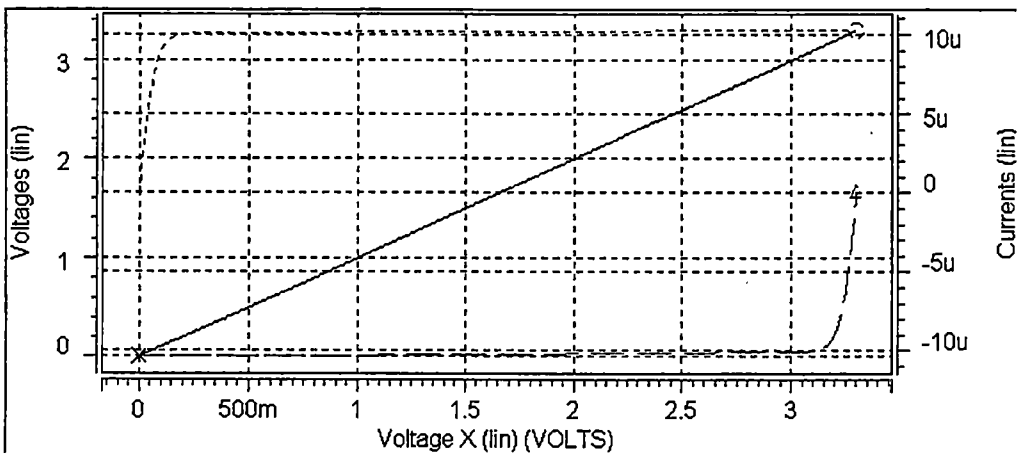


Figure 9 – Output Current versus Voltage Characteristics of Complementary Current Mirror

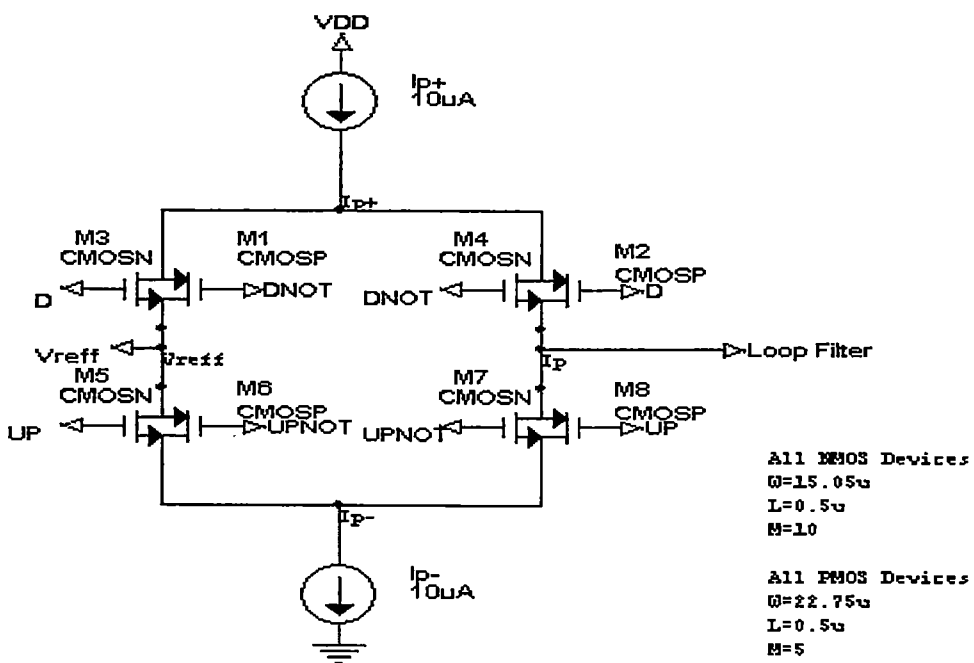


Figure 10 – Switch Network Diagram

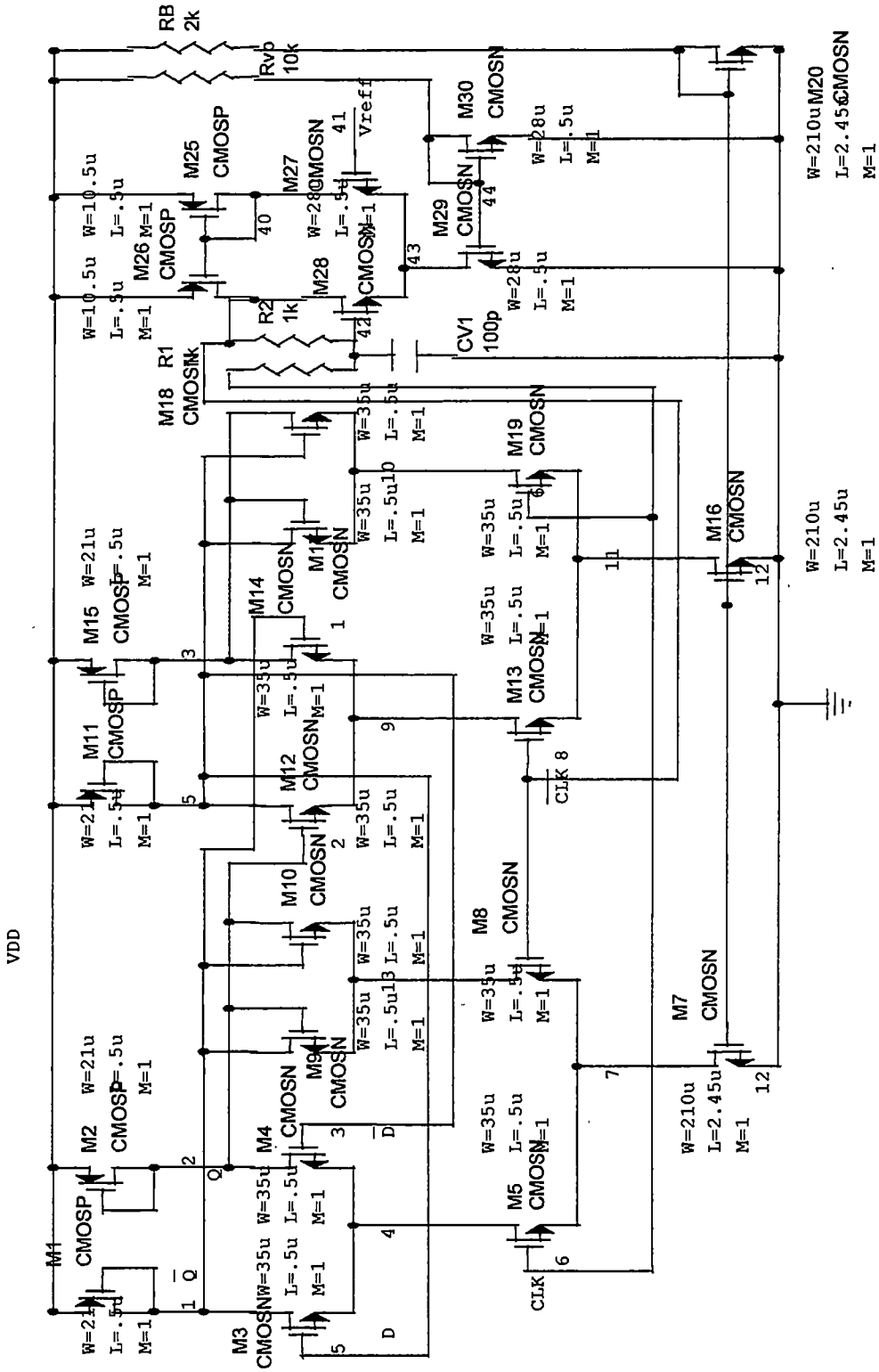


Figure 11 – CML Divide-by-2 Circuit Diagram

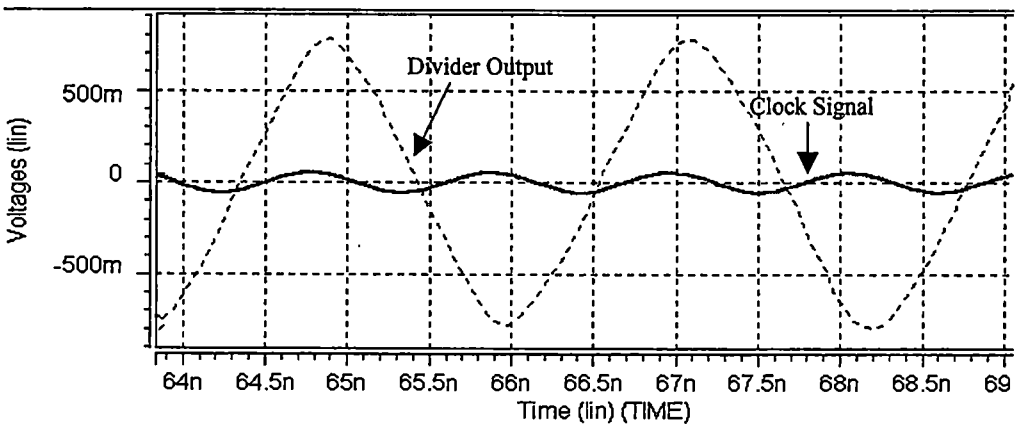


Figure 12 –Input and Output Signals for the Divide by Two Circuit

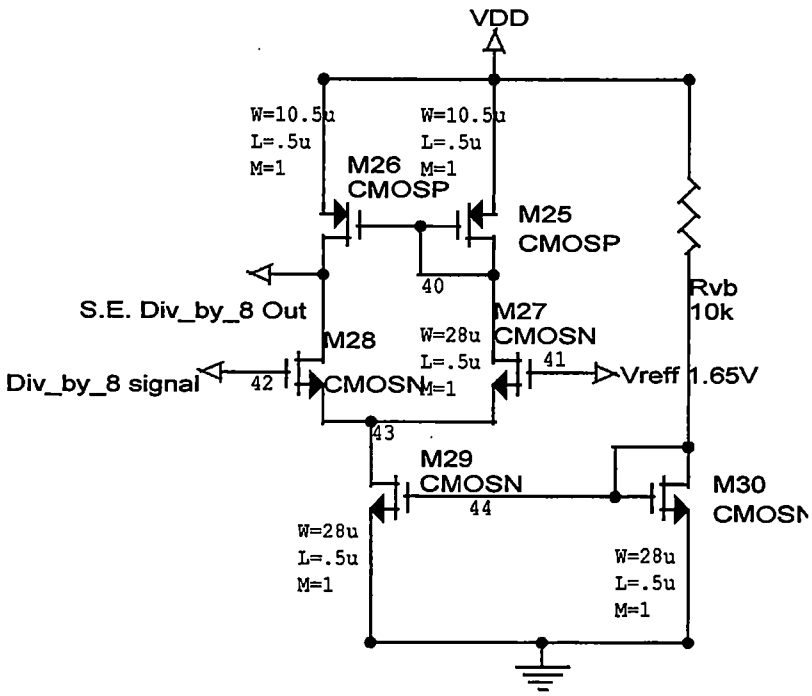


Figure 13 – Differential Amplifier Diagram

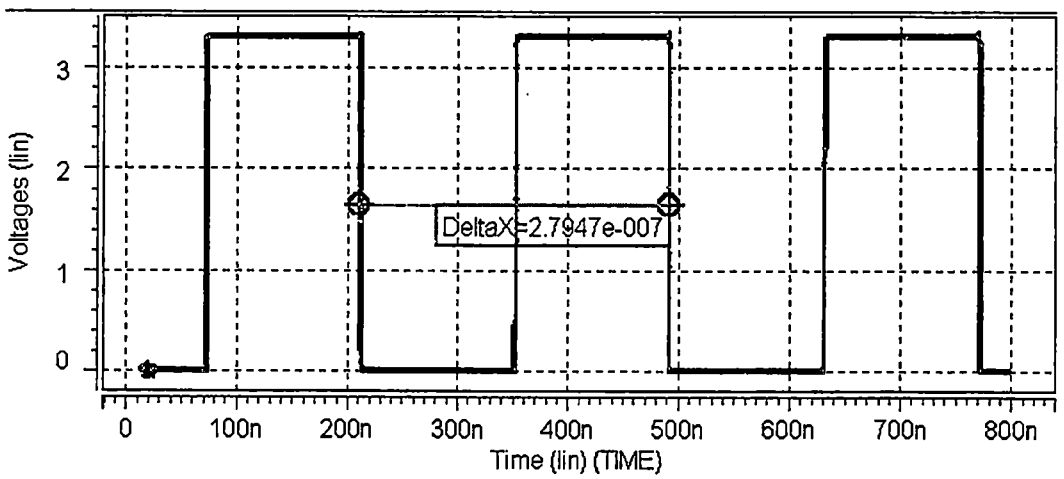


Figure 14 – 3.578 MHz Output Signal for Divide-by-256 Circuit

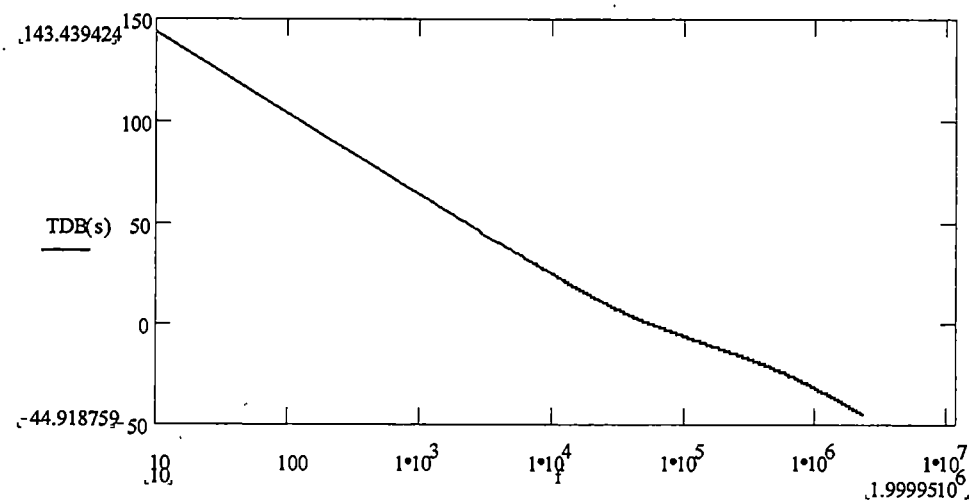


Figure 15 – Plot of PLL Loop Transmission

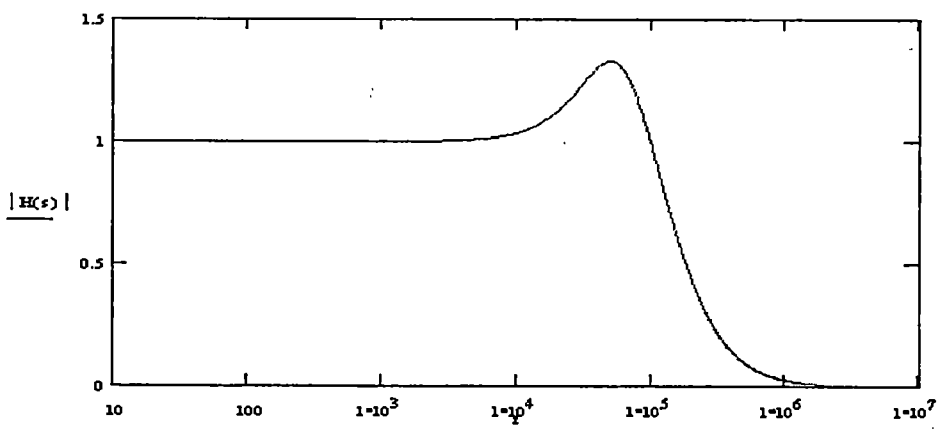


Figure 16 - Magnitude Plot of PLL Closed Loop Transfer Function

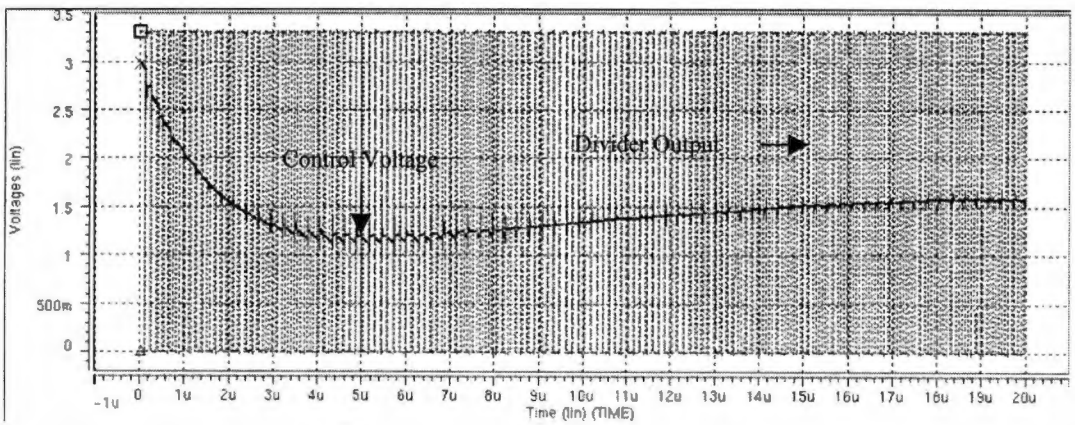


Figure 17 – PLL Divider Output Frequency and VCO Control Voltage

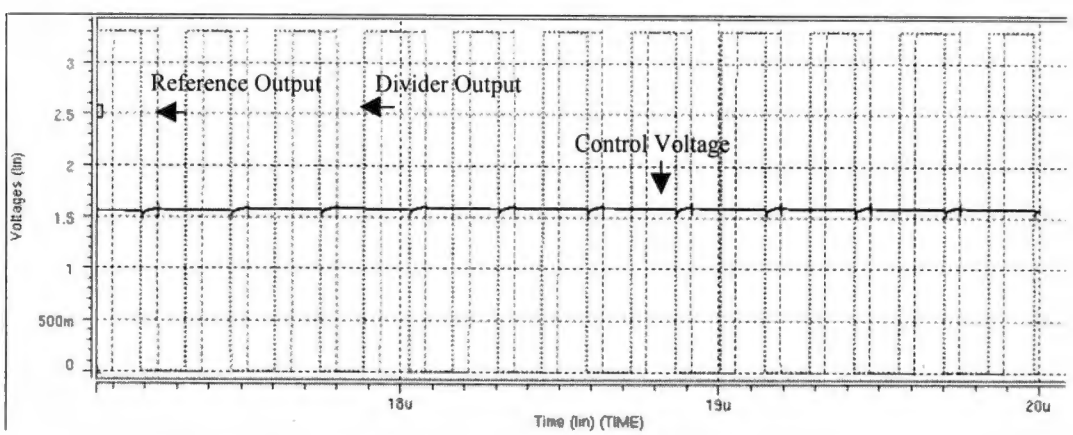


Figure 18 –Steady State Phase PLL Phase Error

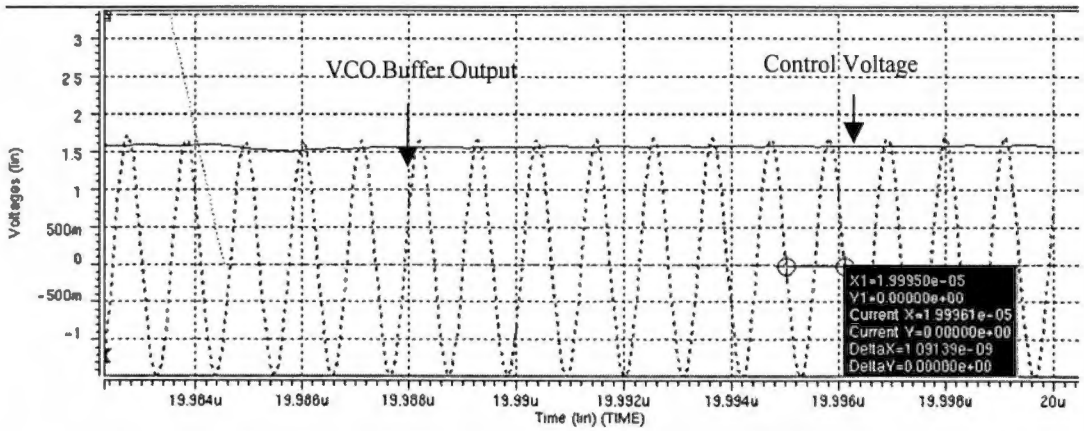
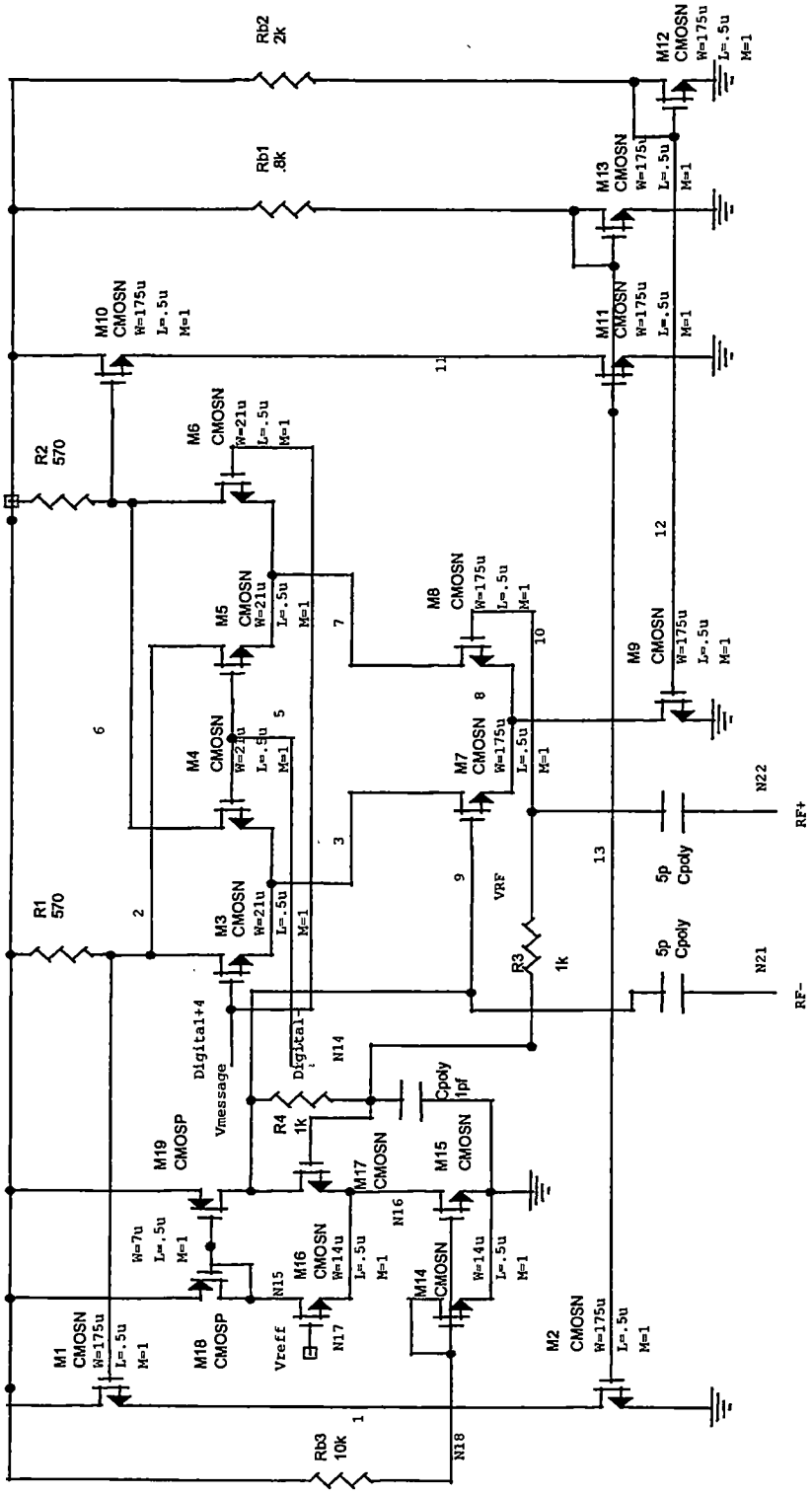


Figure 19 –PLL Output Frequency 916.2MHz



Vreff=1V

Digital Inputs biased at 2.5V

M14-M19 On chip bias network for the RF inputs

All on chip except
Rb1, Rb2, Rb3

Figure 20 – Double Balanced Gilbert Cell Multiplier

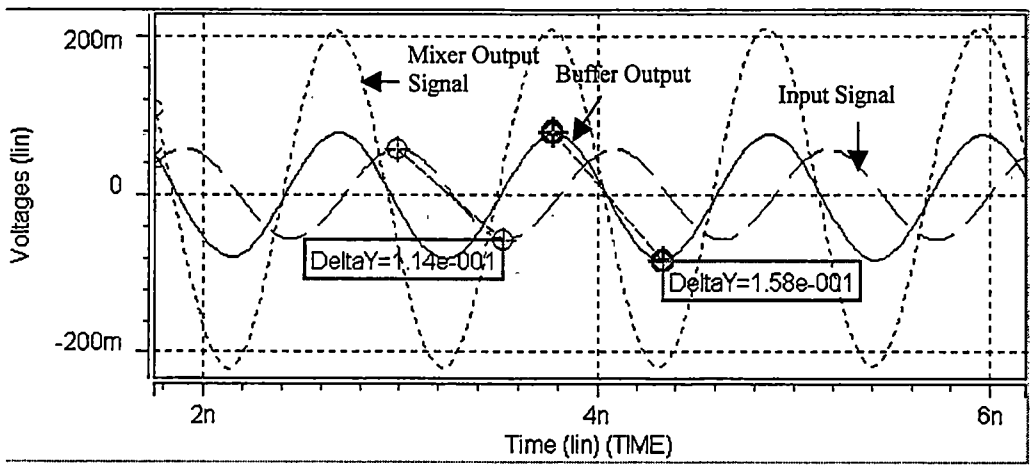


Figure 21 – Mixer and Buffer Gain with Sinusoidal Input Signal

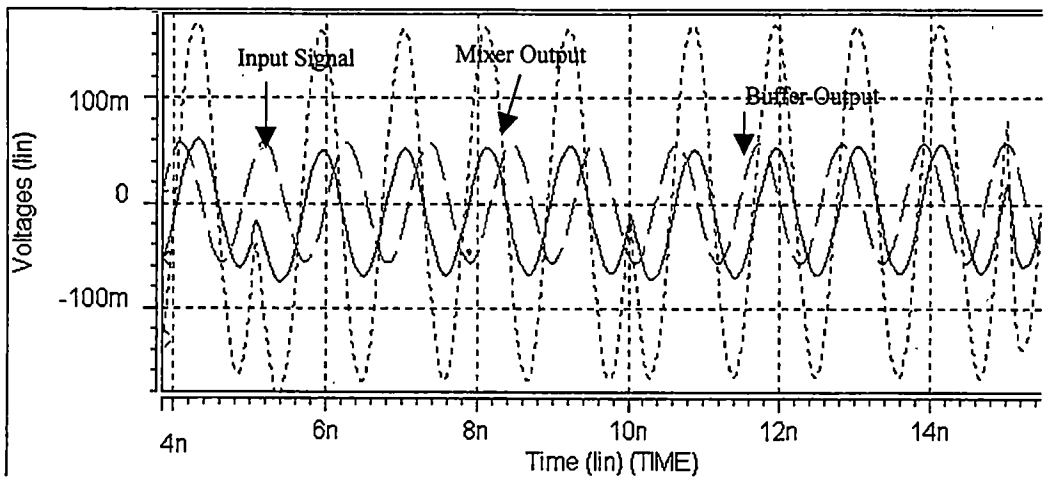


Figure 22 – BPSK Modulated Mixer and Buffer Output Signals

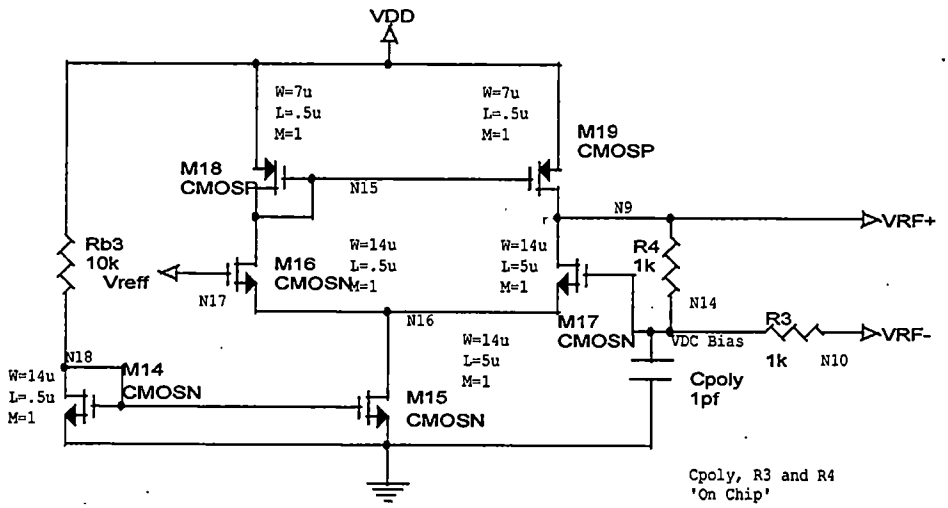


Figure 23 – RF Voltage Bias Amplifier

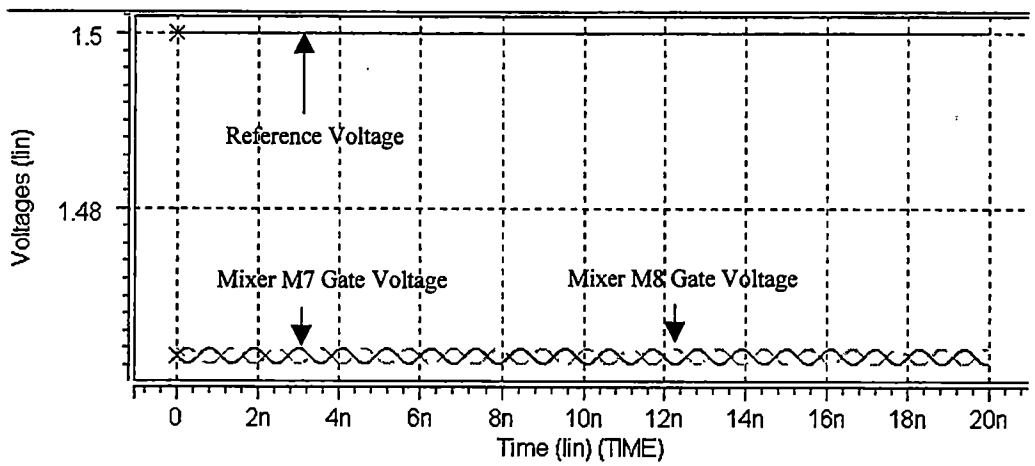


Figure 24 –Mixer Bias Points and Voltage Reference

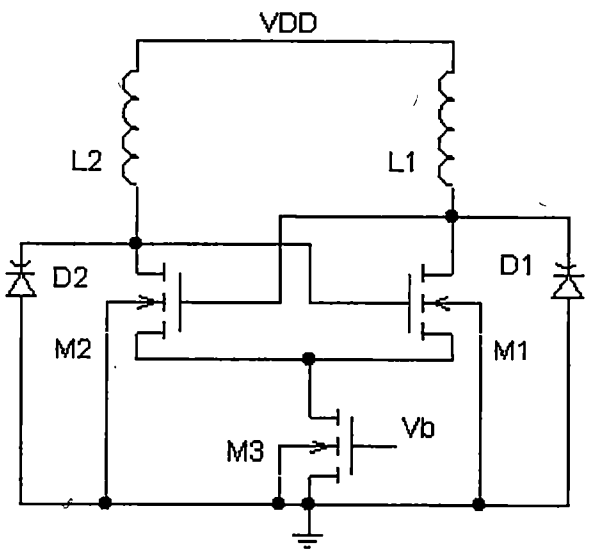


Figure 25 –Voltage Controlled Oscillator Diagram

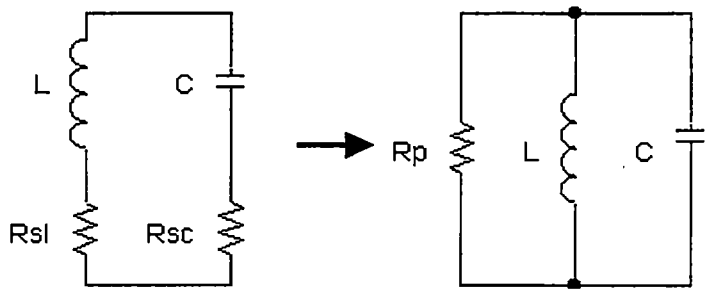


Figure 26 – Transformation of Real LC Circuit into Parallel RLC Circuit

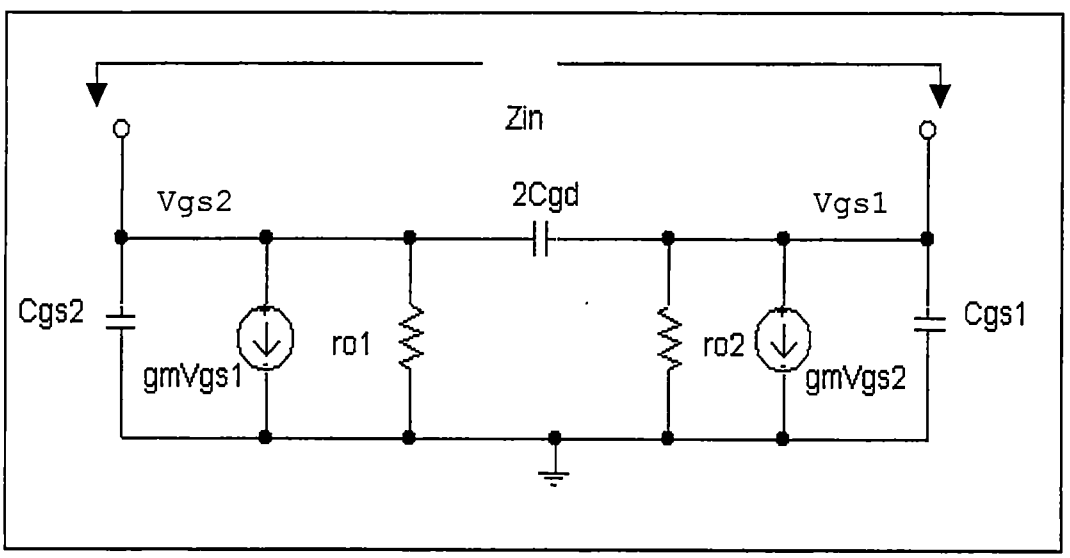


Figure 27 – Small Signal Model of Cross-Coupled NMOS Pair

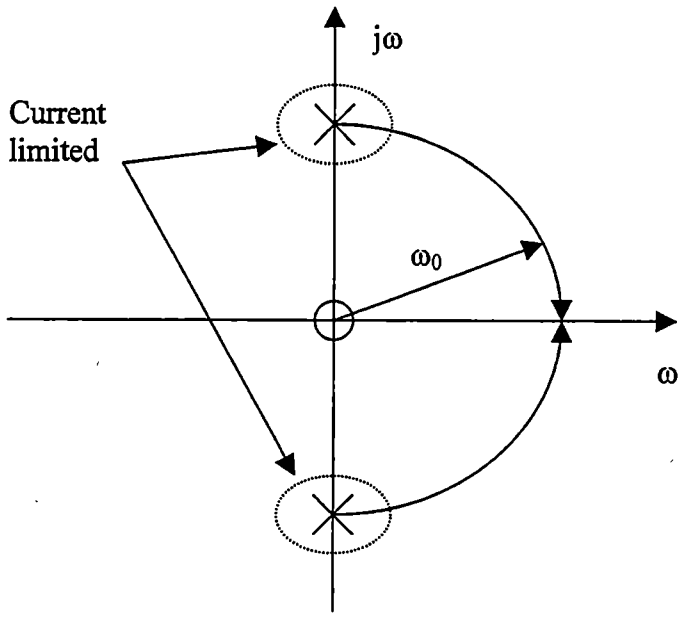


Figure 28 –Pole-Zero Locations of VCO RLC Circuit

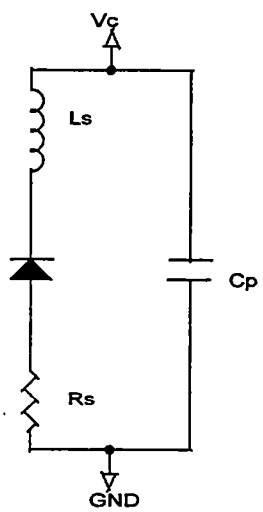


Figure 29 – Varactor Diode Model

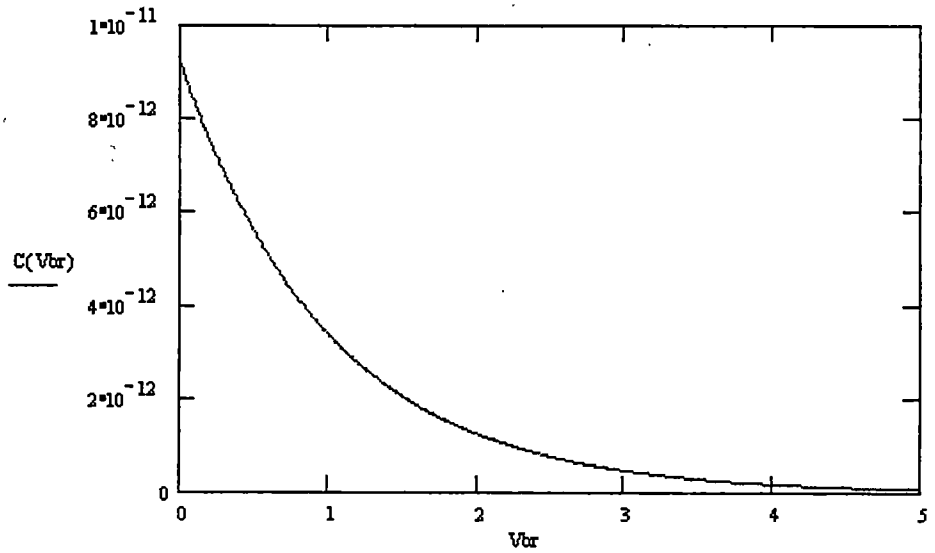


Figure 30 –Capacitance versus Reverse Bias Voltage

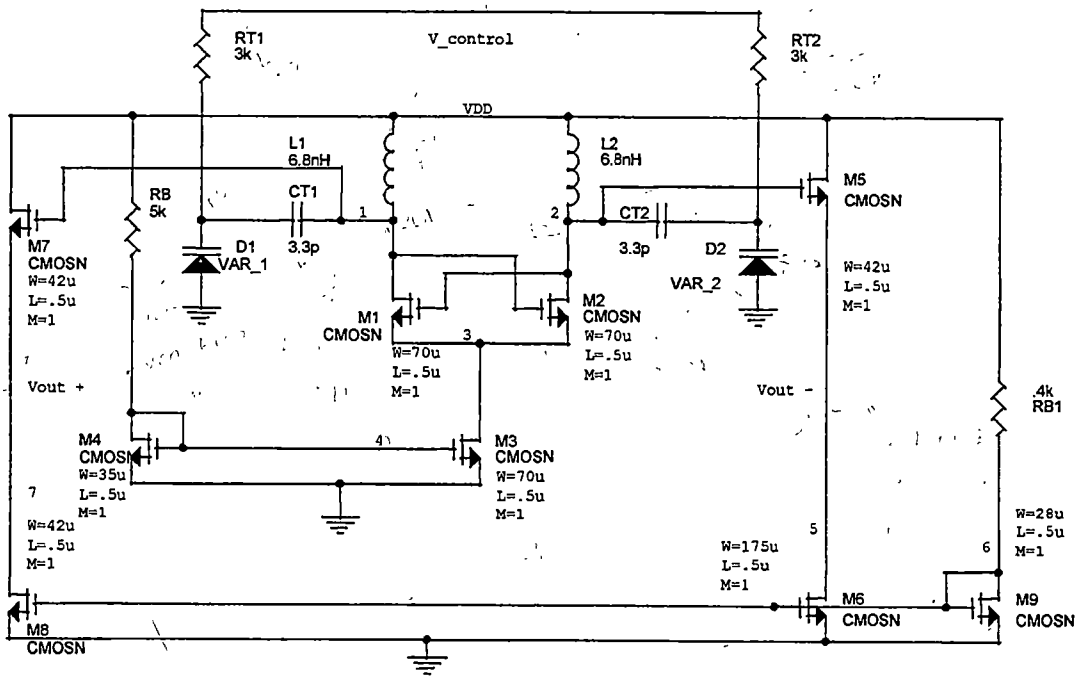


Figure 31 – Final VCO Diagram with Output Buffer

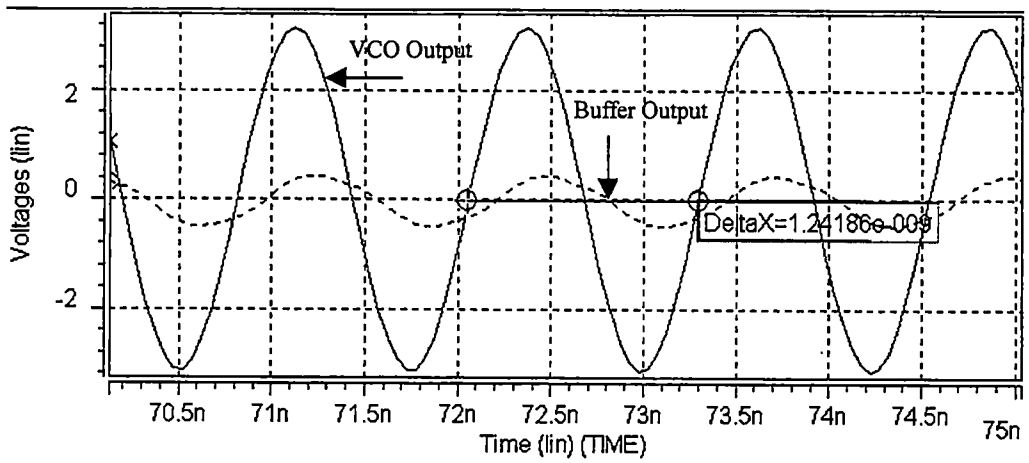


Figure 32 – VCO and Buffer Output at Minimum Operating Frequency
805 MHz with 7.5mA Bias

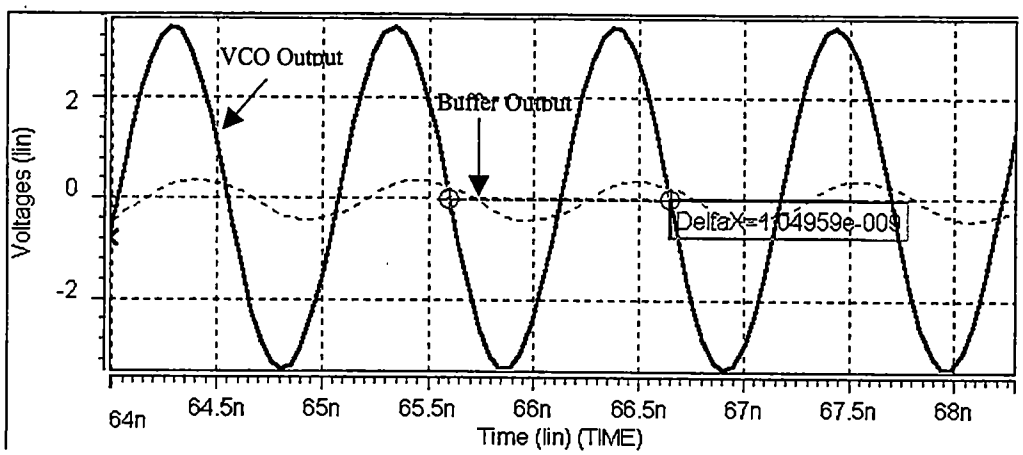


Figure 33 – VCO and Buffer Output at Maximum Operating Frequency
952 MHz with 7.5mA Bias

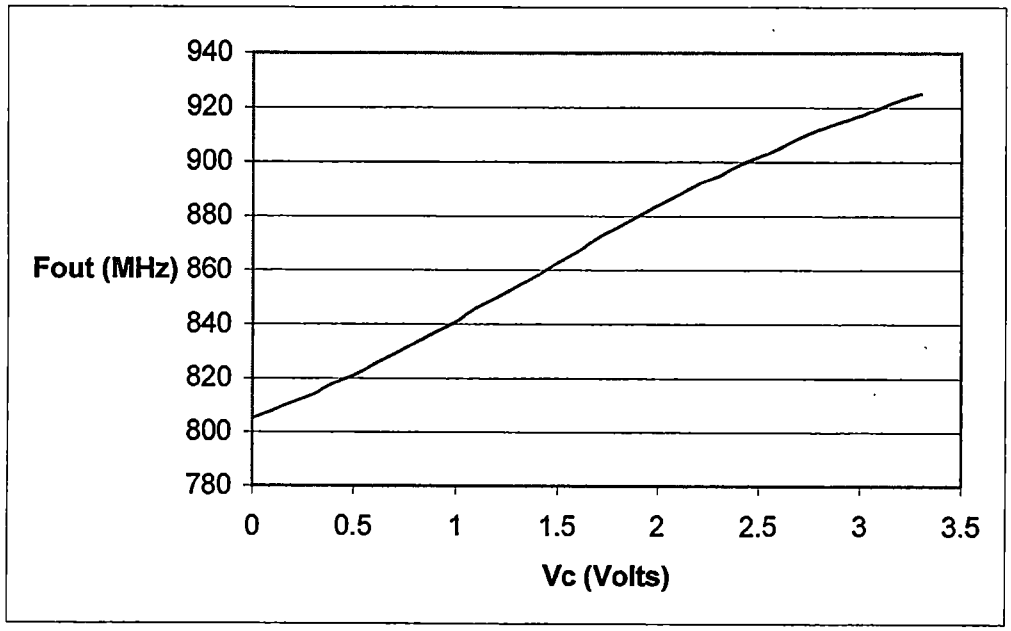


Figure 34 – VCO Frequency versus Control Voltage

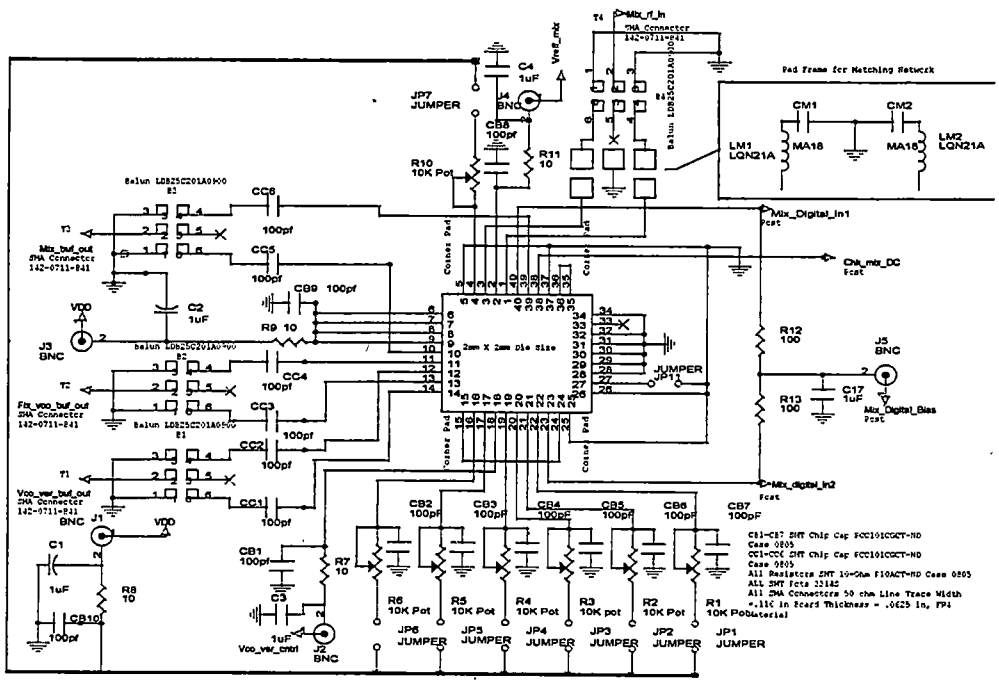


Figure 35 – Mixer Test Printed Circuit Board

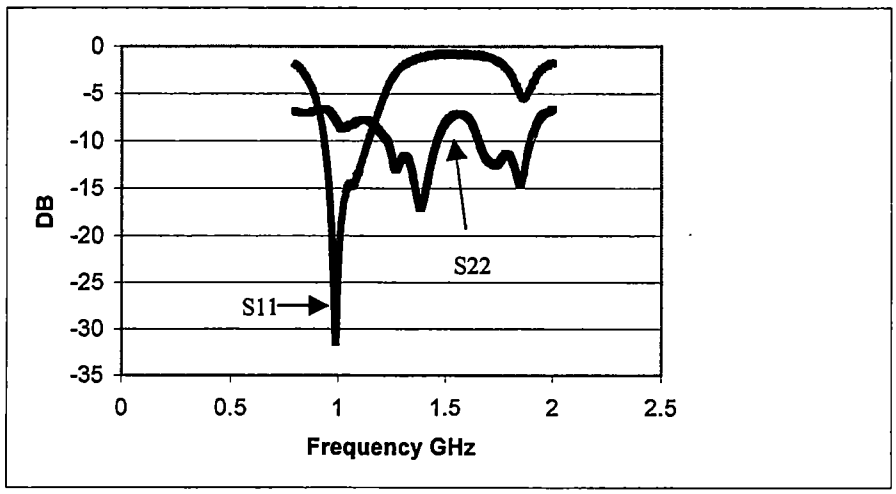


Figure 36 – Measured Mixer Input and Output Reflection

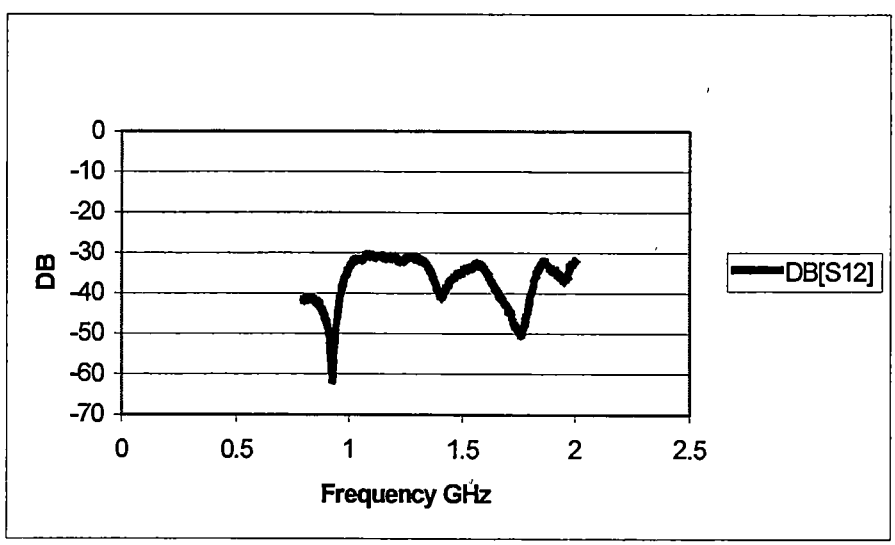


Figure 37 – Measured Mixer Reverse Power Gain S_{12}

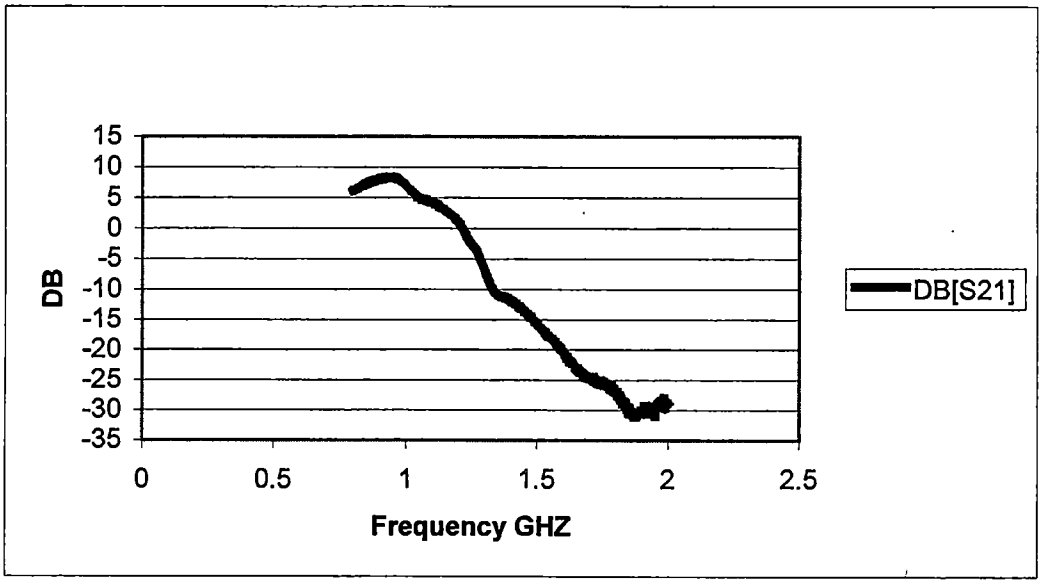


Figure 38 – Measured Mixer Forward Available Power Gain S_{21}

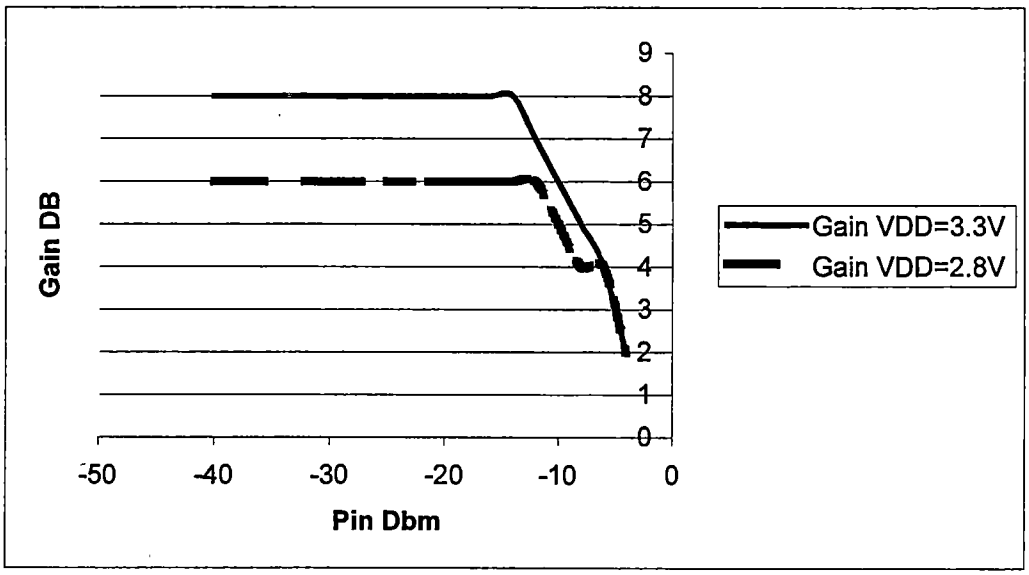


Figure 39 – Measured Mixer Power Gain and 1dB Compression Point

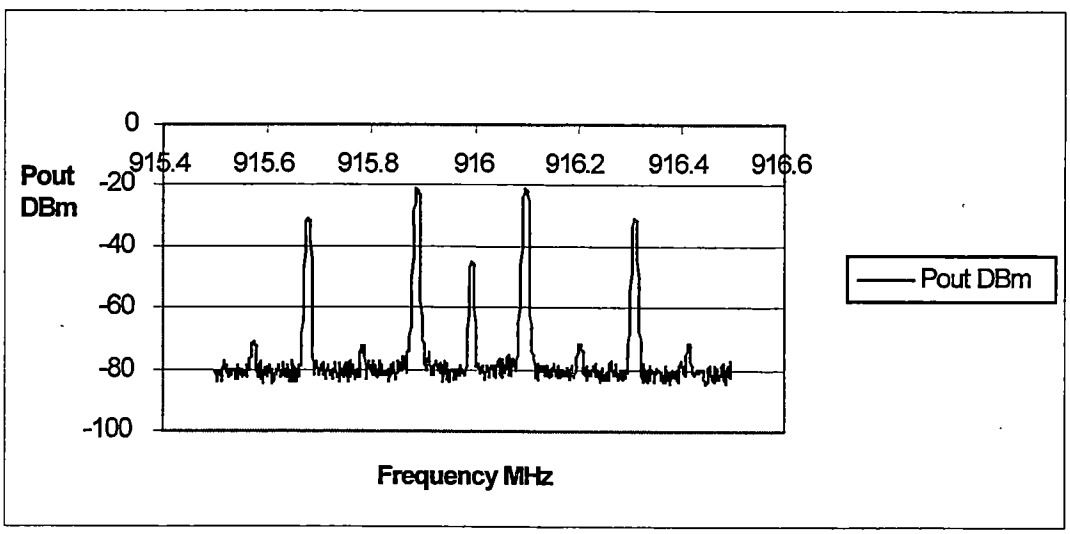


Figure 40 – Modulated BPSK Spectrum

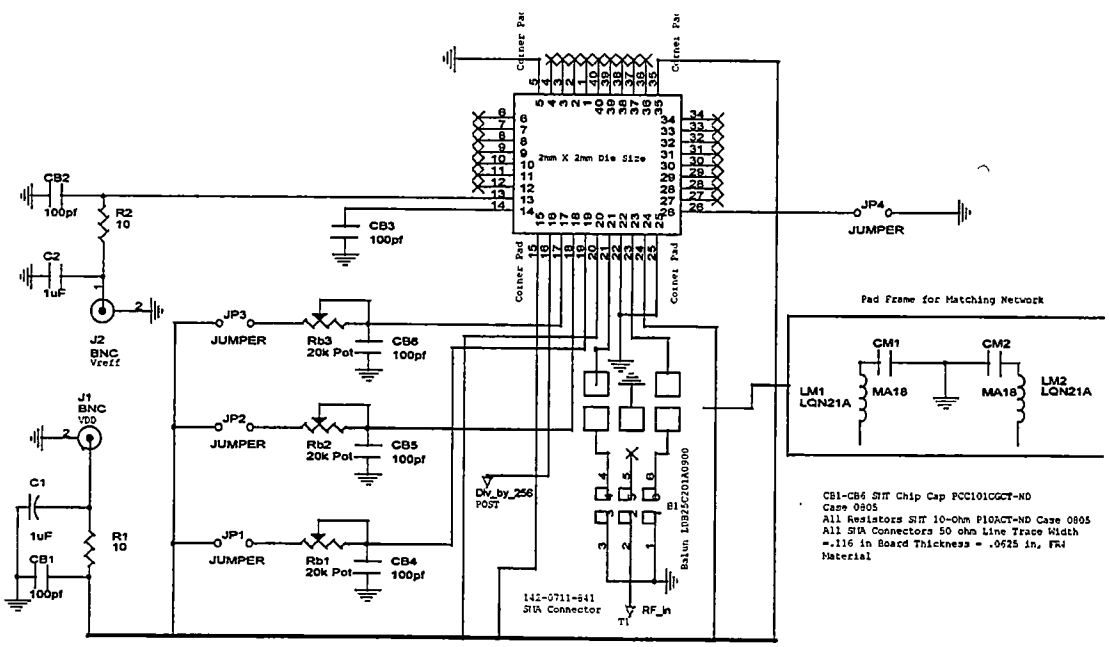


Figure 41 – Frequency Divider Test Printed Circuit Board

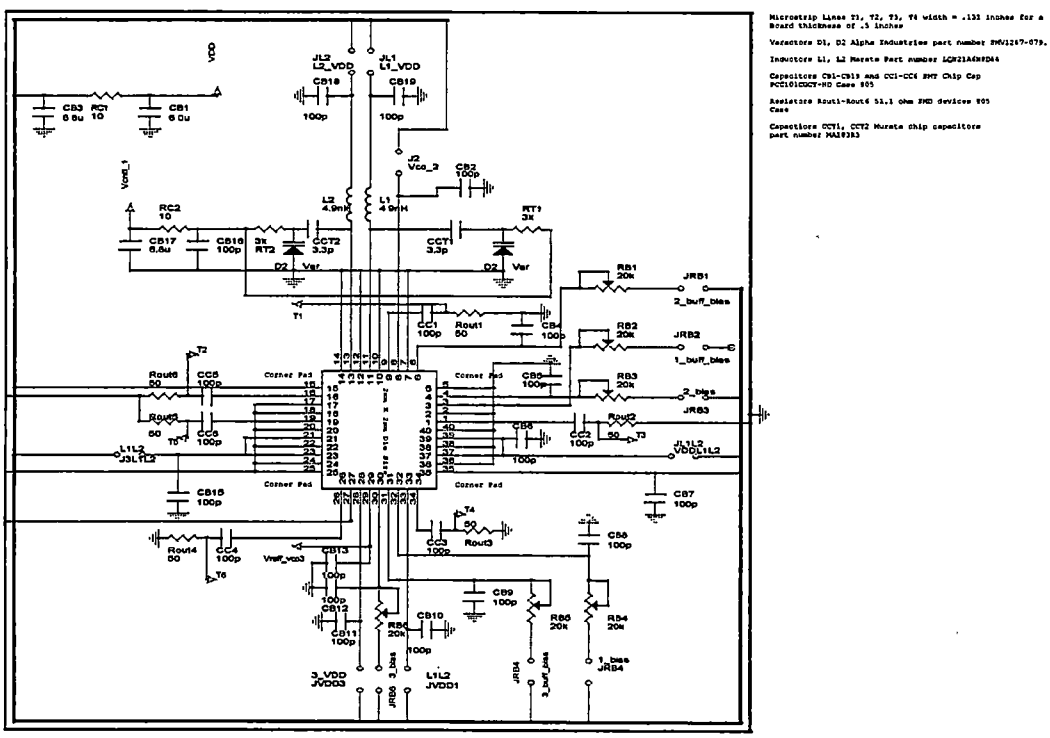


Figure 42 – VCO Test Printed Circuit Board

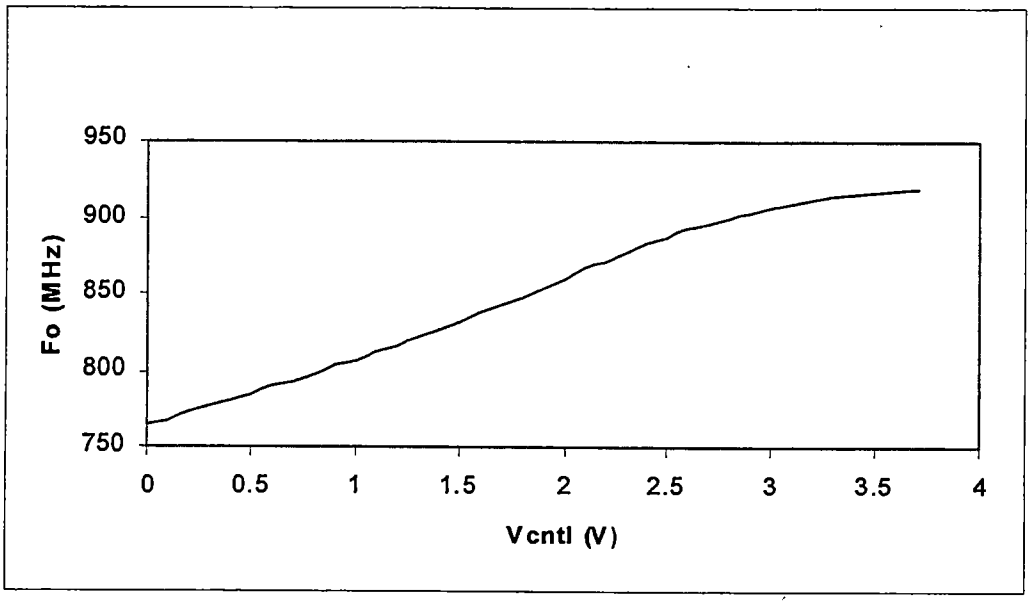


Figure 43 – Measured VCO Frequency versus Control Voltage

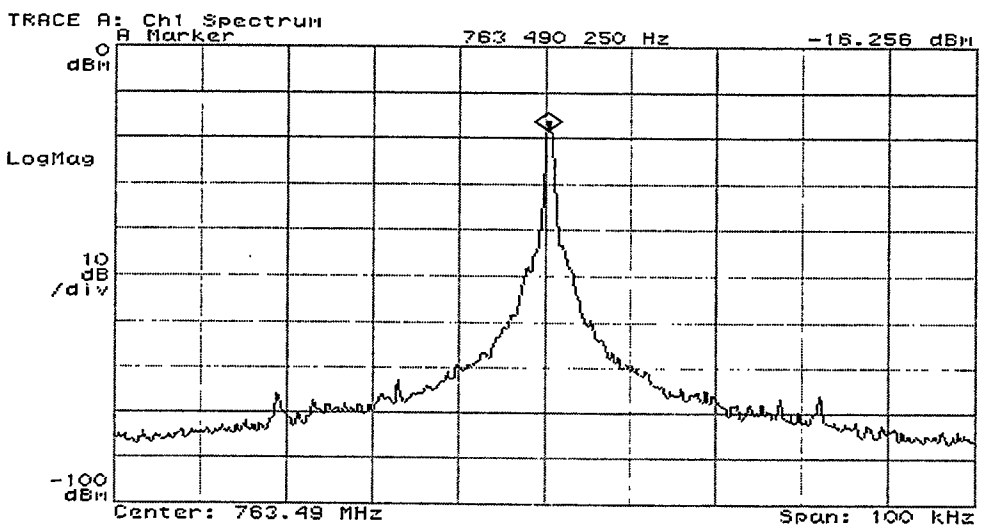


Figure 44 – Minimum 763 MHz VCO Operating Frequency Output Spectrum with 2.2mA Bias and 3.3V VDD

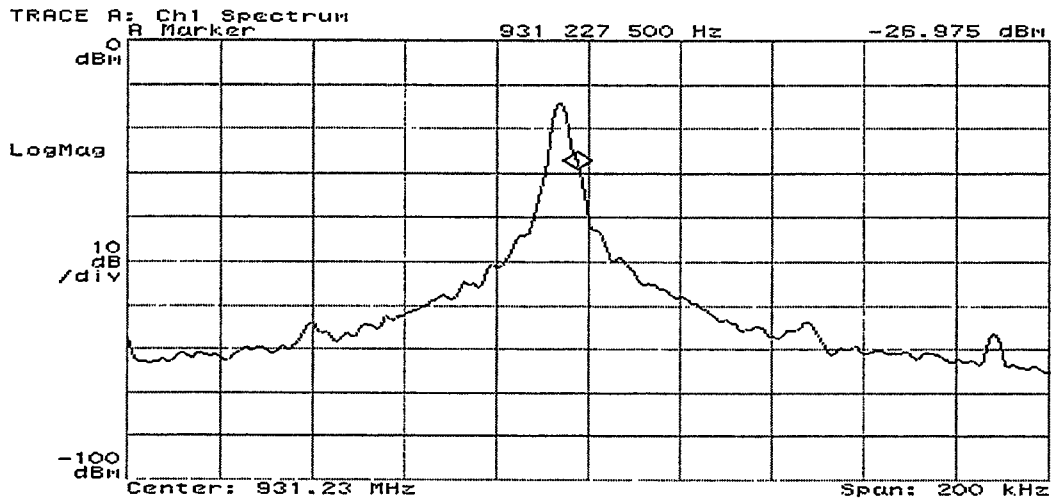


Figure 45 – Maximum 931 MHz VCO Operating Frequency Output Spectrum with 2.2mA Bias and 3.3V VDD

Appendix 2
CMOS BSIM3v3 Model Parameters

```
* N8CR SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS* DATE: Feb
17/99
* LOT: n8cr                    WAF: 56* Temperature_parameters=Default
 .MODEL CMOSN NMOS (LEVEL   = 49   acm=3 hdif=0.4u
 +VERSION = 3.1            TNOM     = 27              TOX      = 9.5E-9
 +XJ      = 1.5E-7         NCH      = 1.7E17          VTH0     = 0.6393629
 +K1      = 0.7355734      K2       = -0.0170766      K3       =
37.2752218
 +K3B     = 3.6855497      W0       = 4.580819E-6     NLX      = 1E-10
 +DVT0W   = 0              DVT1W    = 5.3E6           DVT2W    = -0.032
 +DVT0    = 9.4943826      DVT1     = 0.7193217       DVT2     = -
0.1032065
 +U0      = 447.5651181    UA       = 1.012882E-10    UB       =
2.901162E-18
 +UC      = 1.179693E-10   VSAT     = 1.558378E5      A0       = 1.0148944
 +AGS     = 0.2559616      B0       = 9.545773E-7     B1       = 5E-6
 +KETA    = -9.0726E-3     A1       = 0               A2       = 1
 +RDSW    = 1.274623E3     PRWG     = 0.057075        PRWB     = -1E-3
 +WR      = 1              WINT     = 2.300047E-7     LINT     =
3.897669E-8
 +XL      = -2E-7          XW       = 0               DWG      = -
1.99683E-8
 +DWB     = 1.348589E-8    VOFF     = -0.1312452      NFACTOR  = 0.5502693
 +CIT     = 0              CDSC     = 1.216497E-4     CDSCD    = 0
 +CDSCB   = 0              ETA0     = 5.809308E-5     ETAB     = -
0.0698897
 +DSUB    = 0.5269133      PCLM     = 0.6333193       PDIBLC1  = 0.2041976
 +PDIBLC2 = 5.498843E-3     PDIBLCB  = 0               DROUT    = 0.5795903
 +PSCBE1  = 2.249053E10     PSCBE2   = 1.073921E-8     PVAG     = 0.4337107
 +DELTA   = 0.01           MOBMOD   = 1               PRT      = 0
 +UTE     = -1.5           KT1      = -0.11           KT1L     = 0
 +KT2     = 0.022          UA1      = 4.31E-9         UB1      = -7.61E-18
 +UC1     = -5.6E-11       AT       = 3.3E4           WL       = 0
 +WLN     = 1              WW       = 0               WWN      = 1
 +WWL     = 0              LL       = 0               LLN      = 1
 +LW      = 0              LWN      = 1               LWL      = 0
 +CAPMOD  = 2              XPART    = 0.4             CGDO     = 2.4E-10
 +CGSO    = 2.4E-10        CGBO     = 0               CJ       =
5.102915E-4
 +PB      = 0.99           MJ       = 0.7923453       CJSW     =
4.085101E-10
 +PBSW    = 0.99           MJSW     = 0.1             PVTH0    = 0.0117397
 +PRDSW   = -114.1015762   PK2      = 0.0126755       WKETA    = -
2.543133E-3
 +LKETA   = 0.0109923       )
*
 .MODEL CMOSP PMOS (        LEVEL    = 49    acm=3 hdif=0.4u
 +VERSION = 3.1            TNOM     = 27              TOX      = 9.5E-9
 +XJ      = 1.5E-7         NCH      = 1.7E17          VTH0     = -
0.8358189
 +K1      = 0.3858507      K2       = 0.0139745       K3       =
37.6809886
 +K3B     = -2.5981463     W0       = 8.56663E-6      NLX      = 1E-10
 +DVT0W   = 0              DVT1W    = 5.3E6           DVT2W    = -0.032
```

```
 +DVT0     = 4.2198819      DVT1     = 0.5258824      DVT2     = -
0.0671158
 +U0       = 177.9314595    UA       = 7.1396E-10     UB       = 2.15549E-
18
 +UC       = -3.46077E-11   VSAT     = 1.856441E5     A0       = 0.8869211
 +AGS      = 0.3111564      B0       = 3.680335E-6    B1       = 5E-6
 +KETA     = -1.744397E-3   A1       = 0              A2       = 1
 +RDSW     = 2.066716E3     PRWG     = 8.766794E-3    PRWB     = -1E-3
 +WR       = 1              WINT     = 2.344067E-7    LINT     =
1.519962E-9
 +XL       = -2E-7          XW       = 0              DWG      = -
2.356086E-8
 +DWB      = 1.226092E-9    VOFF     = -0.1188256     NFACTOR  = 1.2556463
 +CIT      = 0              CDSC     = 1.413317E-4    CDSCD    = 0
 +CDSCB    = 0              ETA0     = 0.8255277      ETAB     = -
2.57421E-3
 +DSUB     = 0.6632088      PCLM     = 5.9990392      PDIBLC1  = 0.0448974
 +PDIBLC2  = 4.759132E-3    PDIBLCB  = 0              DROUT    =
9.980727E-4
 +PSCBE1   = 1.591847E10    PSCBE2   = 1.034262E-8    PVAG     =
14.9923297
 +DELTA    = 0.01           MOBMOD   = 1              PRT      = 0
 +UTE      = -1.5           KT1      = -0.11          KT1L     = 0
 +KT2      = 0.022          UA1      = 4.31E-9        UB1      = -7.61E-18
 +UC1      = -5.6E-11       AT       = 3.3E4          WL       = 0
 +WLN      = 1              WW       = 0              WWN      = 1
 +WWL      = 0              LL       = 0              LLN      = 1
 +LW       = 0              LWN      = 1              LWL      = 0
 +CAPMOD   = 2              XPART    = 0.4            CGDO     = 2.86E-10
 +CGSO     = 2.86E-10       CGBO     = 0              CJ       = 9.27314E-
4
 +PB       = 0.9276347      MJ       = 0.4718252      CJSW     =
1.470143E-10
 +PBSW     = 0.4421106      MJSW     = 0.1            PVTH0    = -
3.731288E-3
 +PRDSW    = -185.6376168   PK2      = 2.504653E-3    WKETA    =
3.621549E-3
 +LKETA    = -9.989701E-4    )
*
```

Appendix 3
Hspice Simulation Circuit Files

```
*
* File Used to Simulate Gilbert Cell Multiplier
*
* NMOS Gillbert Cell simulation
* File created on wed sep 29 98
.include 'chuck_mod.lib'
.include 'mosgil.spice'
.options POST list METHOD=GEAR
VDD 110 0 3.3
*
* "U1 n1 0 n2 0 model L=inches"
*
* used to test S22
*
*Vrf  210 0 0
*vrf1 220 0 0
*Vout 1000 0 AC=1
*
* couple caps and load resistors
*
Cout 1 100 100p
Cout1 11 110 100p
Rout 100 0 100
Rout1 110 0 100
*
* used to test trans
*
Vrf 21 22 sin(0 .0312 916Meg)
Ri1 21 0 100
Ri2 22 0 100
*Vrf 210 220 ac=1
*
* used to simulate digital input
*
*VIF 4 5 pulse(-1.65 1.65 0 0 0 5ns 10ns)
*
* RF DC voltage refference
*
Vref1 17 0 1.5
*
* Digital DC Voltage level
*
Vref2 19 0 0
Vref3 190 0 2.5
R5 5 190 100
R6 4 19 100
C100 19 0 6.8u
C200 190 0 6.8u
*
* Bias resistors
*
Rbuff1  110 13 .7k
Rbias2  110 12 1k
Rbvrff4 110 18 1k
*
```

```
.print V(2,6) V(10,9) V(1,11) V(4,5) V(21,22)

*.print AC S11(m) S11(p) S11(R) S11(I)
.op
*.net Vout RIN=100
.tran .01ns 20ns
.FFT V(2,6) NP=16384 window=kaiser alfa=3.5 Fmin=800Meg Fmax=1000Meg
Format=UNORM
*.FFT V(1,11) NP=16384 window=kaiser alfa=3.5 Fmin=800Meg Fmax=1000Meg
Format=UNORM
.FFT V(21,22) NP=1024 window=kaiser alfa=3.5 Fmin=800Meg Fmax=1100Meg
Format=UNORM
*.ac lin 1000 .5meg 5000meg
.end



*
* File Used to Simulate Divide-by-256 Circuit
*
* cmldff: Simulation
* File created on Thu Dec 31 16:02:54 1998
*
.include 'chuck_mod.lib'
*.include 'tline.lib'
.include 'div_by_256.spice'
*****************************************************
* HSPICE options
*****************************************************
*
.options POST
.options METHOD=GEAR
.op
*
Vdd 11 0 3.3
Vdd_dig 16 0 3.3
Vclk 50 0 sin(0 .05623 916MEG 0n)
*R 500 70 1k
*C 70 0 .0152p
*Eclk 500 0 50 0 scale=1 -1
Elclk 70 0 50 0 scale=1 -1
*
RM1 50 0 50
RM2 70 0 50
*L1 50 5 3n
*L2 70 7 3n
*Cp1 70 0 .25p
*Cp2 50 0 .25p
*Cp4 700 0 .25p
*Cp5 500 0 .25p
CC1 70 7 5p
CC2 50 5 5p
*
Vref 2 0 1.5
```

```
*divider bias all three stages
RB 11 1 3k
*divider voltage refference bias
Rvb 11 10 8k
CV1 3 0 100p
*divide by 8 diff amp bias
Rvb3 11 14 8k
.print V(5,7) V(6,4) V(8,9) V(12,13) I(x2.m7) I(x2.m16) I(x1.x1.m7)
V(50,70)
+ I(x1.x1.m16) I(x1.x1.m6) I(x1.x2.m7) I(x1.x2.m16)
.tran .1ns 20ns START=0ns
*.net Vin1 RIN=50
*.print AC S11(m) S11(p) S11(r) S11(i)
*.ac lin 1000 .5meg 5000meg
.END



*
* File Used to Simulate VCO
*
* rf_chip: Simulation
* File created on Fri Apr 16 14:04:30 1999

.include 'rf_chip.spice'
.include 'chuck_mod.lib'
.include 'diode.lib'
.options POST
.options METHOD=GEAR
*
* Chip simulates with 2.93pF of stray capacitance
* fo equals 1.128GHz with Ctank equal Cstray L=6.8n
* fo equals 1.014GHz with Ctank equal Cstray L=8.2n
*
VDD   VDD GND 3.3
Vgnd  GND 0 0
* chip inductor model
Rp1     VDD p1 .12
Rp2     VDD p2 .12
L1    p1   L1 6.8n
L2    p2   L2 6.8n
Clp1  VDD  L1 .103p
Clp2  VDD  L2 .103p
*
* wire bond model
Lb1   L1 L10 1.4n
Lb2   L2 L20 1.4n
Rbp1  L10 L1+ .01
Rbp2  L20 L2- .01
*
* starting Cap
Cs1    L1+ 0 .002p IC=10u
*
* Varactor Diodes and couple caps
```

```
* for fo equal to .916Ghz Cvar is approximate to 1.51p Vcntl between
1.8 and 1.7
CC1 L1 10 3.3p
Ld1 10 100 1.7n
D1  0 100 diode1
CC2 L2 20 3.3p
Ld2 20 200 1.7n
D2  0 200 diode1
*
* circuit for control voltage
*
Rv1 Vref 20 3k
Rv2 Vref 10 3k
*Vcntl Vref 0 1.65
*
* output circuit components
Cout1  buf_out+ rout1 100p
Rout1  rout1 0 1k
Cout2  buf_out- rout2 100p
Rout2  rout2 0 1k
*
*
* bias resistors
*
*
* change to vary bias current
*
*Rvcob  VDD vco_bias 8k
*
*
Rbuff1 VDD buff_bias 1.4k
*
.op
.tran .01ns 300ns start=30ns
.print V(buf_out+,buf_out-) V(L1+,L2-)
*
* change to vary bias current
*
Rvcob  VDD vco_bias 7k
*
.END



*
* Circuit used to simulate wide swing current
mirror
*
*********************************
vdd   110  0  3.3
Ibias 110 1 10u AC=1
*EboutP 50 0 POLY(1) 110 55 0 1
Vbout 50 0 1.65
* current source for both N and P wide swing current mirror
```

```
Cout 50 0 1p
.op
*.ac lin 100 10 500Meg
*.probe AC I(m24) I(m19) Idb(m24) Idb(m19)
Iout=par('db(I(m24)+I(m19))')
.dc Vbout 3.3 0 .01
.probe DC I(m24) I(m19) Iout=par('I(m24)-I(m19)')
.include 'chuck_mod.lib'
.include 'c1.spice'
.options POST METHOD=GEAR
.END
```

```
*
* Circuit File Used to Simulate Complete PLL
*
* PLL: Simulation
* File created on Mon Jul 12 15:57:31 1999

.include 'PLL.spice'
.include 'diode.lib'
.include 'chuck_mod.lib'
.options POST
.options METHOD=GEAR
*
VDD VCO_VDD 0 3.3
Vgnd VCO_GND 0 0
*
* chip inductor model
*
Rp1 VCO_VDD p1 .12
L1  p1      L10 6.8n
Clp1 p1 L100 .103p
Rp2 VCO_VDD p2 .12
L2  p2      L20 6.8n
Clp2 p2 L200 .103p
*
* wire bond model
*
Lb1 L100 L10 1.4n
Rbp1 L10 L1 .01
Lb2 L200 L20 1.4n
Rbp2 L20 L2 .01
*
* starting cap
*
CS1 L1 0 .002p IC=10u
*
* Varactor Diodes and couple caps
*
CC1 L1 10 3.3p
Ld1 10 100 1.7n
D1  0  100 diode1
```

```
CC2 L2 20 3.3p
Ld2 20 200 1.7n
D2  0 200  diode1
*
* circuit for control voltage
*
Rv1 Iout 20 3k
Rv2 Iout 10 3k
*
* Output circuit
*
*
* bias resistors
*
Rbuff1 VCO_VDD VCO_BUFF_BIAS 1.4k
Rvco   VCO_VDD VCO_BIAS  4k
*
* DIVIDER CIRCUIT COMPONENETS
*
VDIV DIV_VDD 0 3.3
VDIVGND DIV_GND 0 0
*
R1 DIV_VDD diff_amp_bias 10k
*
Vdig digital_vdd 0 3.3
*
R3 DIV_VDD div_bias 8k
*
R4 DIV_VDD DIV_VREFF_BIAS 10k
*
CDIV DIV_CAP 0 100p
*
V6 DIV_VREFF 0 1
*
*
* charge pump circuit
*
Vcp charge_pump_core_vdd 0 3.3
Vfref Freff 0 pulse(0 3.3 0 1n 1n .139737u .279476u)
CF1  Iout  0  1.58p
Rout  Iout Iout1 202.955k
CF   Iout1 0 22.3p
Icsbias charge_pump_core_vdd current_source_bias 10u
Vreff Vreff 0 1.65
*
*
*
.IC V(IOUT)=3
.op
*.tran .025n .02ms start=30ns
*.probe V(L1,L2) V(vco_buff_L1_out,vco_buff_l2_out)
.END
```

Appendix 4

Hspice Gilbert Cell Multiplier and PLL
Extracted Netlist Files

```
* Gilbert Cell Spice File
*
* mosgil.spice
*
* File Location        /msd16/arnott/magic_work/rf_chip1
* File Created         Mon Nov  2 14:56:31 1998
* Ext2spice Version    ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*           Options    -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*

** Subcircuit definition for couple_cap
** Extraction file is /msd16/arnott/magic_work/rf_chip1/couple_cap.ext
.SUBCKT couple_cap 1 2 3
C1 2 1 HPCAP50 SCALE=286.65
C1P 1 1 HPCAP50P SCALE=286.6
* C1=1020.47FF C1P=0.03FF
C2 1 0 4.0F
C3 2 0 23.0F
C4 3 0 24.0F
*** Node Listing for subckt:  couple_cap
** N0                          ==  IdealGND
** N1                [U=3]     ==  BOT_PLATE
** N2                [U=2]     ==  top_plate
** N3                [U=1]     ==  guard
.ENDS

** Subcircuit definition for gil_cap
** Extraction file is /msd16/arnott/magic_work/rf_chip1/gil_cap.ext
.SUBCKT gil_cap 1 2 3
C1 2 1 HPCAP50 SCALE=1396.50
C1P 1 1 HPCAP50P SCALE=1396.5
* C1=4971.54FF C1P=0.14FF
C2 1 0 7.0F
C3 2 0 46.0F
C4 3 0 44.0F
*** Node Listing for subckt:  gil_cap
** N0                          ==  IdealGND
** N1                [U=3]     ==  BOT_PLATE
** N2                [U=2]     ==  top_plate
** N3                [U=1]     ==  guard
.ENDS
****** top level cell is /msd16/arnott/magic_work/rf_chip1/mosgil.ext
** Instance-id:   gil_cap_1
X1 21 9 0 gil_cap
** Instance-id:   gil_cap_0
X2 0 14 0 couple_cap
** Instance-id:   gil_cap_2
X3 22 10 0 gil_cap
M1 110 2 1 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M2 1 13 0 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M3 2 4 3 0 CMOSN M=6 W=3.50U L=0.50U GEO=0
M4 6 5 3 0 CMOSN M=6 W=3.50U L=0.50U GEO=0
M5 2 5 7 0 CMOSN M=6 W=3.50U L=0.50U GEO=0
M6 6 4 7 0 CMOSN M=6 W=3.50U L=0.50U GEO=0
M7 3 9 8 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
```

```
M8 7 10 8 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M9 8 12 0 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M10 110 6 11 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M11 11 13 0 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M12 12 12 0 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M13 13 13 0 0 CMOSN M=10 W=17.50U L=0.50U GEO=0
M14 18 18 0 0 CMOSN M=4 W=3.50U L=0.50U GEO=0
M15 16 18 0 0 CMOSN M=4 W=3.50U L=0.50U GEO=0
M16 15 17 16 0 CMOSN M=4 W=3.50U L=0.50U GEO=0
M17 10 14 16 0 CMOSN M=4 W=3.50U L=0.50U GEO=0
M18 15 15 110 110 CMOSP M=2 W=3.50U L=0.50U GEO=0
M19 10 15 110 110 CMOSP M=2 W=3.50U L=0.50U GEO=0
R1 110 2 RHPPOLYSB50 SCALE=6.40
* R1=576.0 (width=1.75U)
R2 6 110 RHPPOLYSB50 SCALE=6.40
* R2=576.0 (width=1.75U)
R3 10 14 RHPPOLYSB50 SCALE=12.80
* R3=1152.0 (width=1.75U)
R4 14 9 RHPPOLYSB50 SCALE=12.80
* R4=1152.0 (width=1.75U)
C1 15 0 3.0F
C2 10 9 1.0F
C3 0 2 12.0F
C4 110 11 2.0F
C5 110 21 16.0F
C6 16 0 12.0F
C7 0 11 89.0F
C8 8 0 123.0F
C9 0 22 16.0F
C10 5 7 3.0F
C11 110 22 16.0F
C12 0 21 16.0F
C13 12 0 43.0F
C14 0 7 56.0F
C15 2 6 1.0F
C16 8 10 6.0F
C17 5 3 3.0F
C18 4 7 3.0F
C19 0 3 56.0F
C20 10 7 6.0F
C21 14 10 1.0F
C22 4 3 3.0F
C23 0 110 81.0F
C24 13 0 57.0F
C25 8 9 6.0F
C26 4 5 2.0F
C27 10 110 10.0F
C28 10 0 3.0F
C29 18 0 4.0F
C30 9 3 10.0F
C31 0 6 12.0F
C32 110 1 2.0F
C33 15 110 9.0F
C34 0 1 89.0F
C35 110 0 224.0F
```

```
C36 10 0 111.0F
C37 11 0 95.0F
C38 12 0 94.0F
C39 13 0 119.0F
C40 14 0 36.0F
C41 15 0 25.0F
C42 16 0 24.0F
C43 17 0 60.0F
C44 18 0 46.0F
C45 21 0 23.0F
C46 22 0 22.0F
C47 1 0 82.0F
C48 2 0 43.0F
C49 3 0 82.0F
C50 4 0 73.0F
C51 5 0 70.0F
C52 6 0 41.0F
C53 7 0 90.0F
C54 8 0 106.0F
C55 9 0 99.0F
*** Node Listing for subckt:  mosgil
** N0                          ==  IdealGND
** N1                [U=2]     ==  N1
** N2                [U=4]     ==  N2
** N3                [U=3]     ==  N3
** N4                [U=2]     ==  N4
** N5                [U=2]     ==  N5
** N6                [U=4]     ==  N6
** N7                [U=3]     ==  N7
** N8                [U=3]     ==  N8
** N9                [U=3]     ==  N9
** N10               [U=5]     ==  N10
** N11               [U=2]     ==  N11
** N12               [U=3]     ==  N12
** N13               [U=4]     ==  N13
** N14               [U=4]     ==  N14
** N15               [U=4]     ==  N15
** N16               [U=3]     ==  N16
** N17               [U=1]     ==  N17
** N18               [U=3]     ==  N18
** N21               [U=1]     ==  NRF+
** N22               [U=1]     ==  NRF-
** N110              [U=8]     ==  N110
************************************************************
*
* Model Definitions for HSPICE
*
************************************************************
.MODEL RHPPOLYSB50 R RES=90.0
.MODEL CHPPOLY50 C CAP=0.570FF
.MODEL HPCAP50P C CAP=0.000FF
.MODEL HPCAP50 C CAP=3.560FF
*0 errors and 0 warnings found.
```

```
*
* Extracted Circuit File for Complete Phase-Locked
* Loop Simulation
*
* PLL.spice
*
* File Location         /msd16/arnott/magic_work/PLL
* File Created          Tue Jul 13 14:17:04 1999
* Ext2spice Version     ORNL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*           Options     -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*

** Subcircuit definition for cmldff1
** Extraction file is /msd16/arnott/magic_work/PLL/cmldff1.ext
.SUBCKT cmldff1 1 2 6 8 12 41 42 44 110
M1 1 1 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M2 2 2 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M3 1 5 4 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M4 2 3 4 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M5 4 6 7 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M6 12 12 0 0 CMOSN M=6 W=3.50U L=2.45U GEO=0
M7 7 12 0 0 CMOSN M=6 W=35.00U L=2.45U GEO=0
M8 13 8 7 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M9 1 2 13 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M10 2 1 13 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M11 5 5 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M12 5 2 9 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M13 9 8 11 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M14 3 1 9 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M15 3 3 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M16 11 12 0 0 CMOSN M=6 W=35.00U L=2.45U GEO=0
M17 5 3 10 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M18 3 5 10 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M19 10 6 11 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M25 40 40 110 110 CMOSP M=3 W=3.50U L=0.70U GEO=0
M26 6 40 110 110 CMOSP M=3 W=3.50U L=0.70U GEO=0
M27 40 41 43 0 CMOSN M=4 W=7.00U L=0.70U GEO=0
M28 6 42 43 0 CMOSN M=4 W=7.00U L=0.70U GEO=0
M29 43 44 0 0 CMOSN M=4 W=7.00U L=2.45U GEO=0
M30 44 44 0 0 CMOSN M=4 W=7.00U L=2.45U GEO=0
R1 8 42 RHPPOLYSB50 SCALE=12.80
* R1=1152.0 (width=1.75U)
R2 42 6 RHPPOLYSB50 SCALE=12.80
* R2=1152.0 (width=1.75U)
C1 41 40 2.0F
C2 12 0 5.0F
C3 2 110 1.0F
C4 44 6 2.0F
C5 9 1 2.0F
C6 42 6 2.0F
C7 6 10 1.0F
C8 4 5 2.0F
C9 9 2 2.0F
C10 10 3 2.0F
C11 8 7 2.0F
```

```
C12 11 6 2.0F
C13 44 110 1.0F
C14 43 0 1.0F
C15 12 7 5.0F
C16 5 3 1.0F
C17 42 110 1.0F
C18 1 2 1.0F
C19 3 0 1.0F
C20 8 6 2.0F
C21 10 5 2.0F
C22 1 4 1.0F
C23 44 0 1.0F
C24 40 6 1.0F
C25 41 110 1.0F
C26 42 8 5.0F
C27 7 6 2.0F
C28 1 13 3.0F
C29 11 0 2.0F
C30 11 8 2.0F
C31 12 110 1.0F
C32 12 11 5.0F
C33 4 3 2.0F
C34 13 2 3.0F
C35 1 110 1.0F
C36 43 44 4.0F
C37 110 0 196.0F
C38 10 0 43.0F
C39 11 0 79.0F
C40 12 0 120.0F
C41 13 0 33.0F
C42 40 0 16.0F
C43 41 0 45.0F
C44 42 0 55.0F
C45 43 0 31.0F
C46 44 0 62.0F
C47 1 0 129.0F
C48 2 0 132.0F
C49 3 0 128.0F
C50 4 0 27.0F
C51 5 0 120.0F
C52 6 0 90.0F
C53 7 0 89.0F
C54 8 0 62.0F
C55 9 0 35.0F
*** Node Listing for subckt:  cmldff1
** N0                          ==  IdealGND
** N1                [U=7]     ==  N1
** N2                [U=7]     ==  N2
** N3                [U=6]     ==  N3
** N4                [U=3]     ==  N4
** N5                [U=6]     ==  N5
** N6                [U=6]     ==  N6
** N7                [U=3]     ==  N7
** N8                [U=4]     ==  N8
** N9                [U=3]     ==  N9
```

```
** N10                [U=3]      ==  N10
** N11                [U=3]      ==  N11
** N12                [U=5]      ==  N12
** N13                [U=3]      ==  N13
** N40                [U=4]      ==  N40
** N41                [U=2]      ==  N41
** N42                [U=4]      ==  N42
** N43                [U=3]      ==  N43
** N44                [U=4]      ==  N44
** N110               [U=13]     ==  N110
.ENDS

** Subcircuit definition for cmldff2
** Extraction file is /msd16/arnott/magic_work/PLL/cmldff2.ext
.SUBCKT cmldff2 1 2 6 8 12 14 110
M1 1 1 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M2 2 2 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M3 1 5 4 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M4 2 3 4 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M5 4 6 7 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M7 7 12 0 0 CMOSN M=6 W=26.25U L=2.45U GEO=0
M8 13 8 7 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M9 1 2 13 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M10 2 1 13 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M11 5 5 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M12 5 2 9 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M13 9 8 11 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M14 3 1 9 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M15 3 3 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M16 11 12 0 0 CMOSN M=6 W=26.25U L=2.45U GEO=0
M17 5 3 10 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M18 3 5 10 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M19 10 6 11 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
C1 2 110 1.0F
C2 9 1 2.0F
C3 6 10 1.0F
C4 4 5 2.0F
C5 9 2 2.0F
C6 10 3 2.0F
C7 2 0 1.0F
C8 8 7 2.0F
C9 11 6 2.0F
C10 5 3 1.0F
C11 12 11 5.0F
C12 1 2 1.0F
C13 3 0 1.0F
C14 8 6 1.0F
C15 10 5 2.0F
C16 12 0 6.0F
C17 1 4 1.0F
C18 7 6 2.0F
C19 1 13 3.0F
C20 11 8 2.0F
C21 12 7 5.0F
C22 5 0 1.0F
```

```
C23 4 3 2.0F
C24 13 2 3.0F
C25 1 110 1.0F
C26 110 0 168.0F
C27 10 0 43.0F
C28 11 0 69.0F
C29 12 0 79.0F
C30 13 0 33.0F
C31 14 0 1.0F
C32 1 0 129.0F
C33 2 0 132.0F
C34 3 0 128.0F
C35 4 0 27.0F
C36 5 0 120.0F
C37 6 0 71.0F
C38 7 0 83.0F
C39 8 0 77.0F
C40 9 0 35.0F
*** Node Listing for subckt:  cmldff2
** N0                          ==  IdealGND
** N1                [U=7]     ==  N1
** N2                [U=7]     ==  N2
** N3                [U=6]     ==  N3
** N4                [U=3]     ==  N4
** N5                [U=6]     ==  N5
** N6                [U=3]     ==  N6
** N7                [U=3]     ==  N7
** N8                [U=3]     ==  N8
** N9                [U=3]     ==  N9
** N10               [U=3]     ==  N10
** N11               [U=3]     ==  N11
** N12               [U=3]     ==  N12
** N13               [U=3]     ==  N13
** N14               [U=1]     ==  9_112_603#
** N110              [U=9]     ==  N110
.ENDS

** Subcircuit definition for HP50PAD
** Extraction file is /msd16/arnott/magic_work/PLL/HP50PAD.ext
.SUBCKT HP50PAD 1
C1 1 0 749.0F
*** Node Listing for subckt:  HP50PAD
** N0                          ==  IdealGND
** N1                [U=1]     ==  10_273_547#
.ENDS

** Subcircuit definition for ornlcpy270
** Extraction file is /msd16/arnott/magic_work/PLL/ornlcpy270.ext
*Null Subcircuit definition

** Subcircuit definition for invf101
** Extraction file is /msd16/arnott/magic_work/PLL/invf101.ext
.SUBCKT invf101 1 2 3 4
M1 1 2 3 3 CMOSP W=9.10U L=0.70U GEO=0
M2 1 2 4 4 CMOSN W=4.20U L=0.70U GEO=0
```

```
C1 1 0 4.0F
C2 2 0 3.0F
C3 4 0 3.0F
C4 3 0 4.0F
*** Node Listing for subckt:  invf101
** N0                          ==  IdealGND
** N1                [U=3]     ==  O
** N2                [U=3]     ==  A1
** N3                [U=3]     ==  Vdd!
** N4                [U=3]     ==  GND!
.ENDS

** Subcircuit definition for nanf401
** Extraction file is /msd16/arnott/magic_work/PLL/nanf401.ext
.SUBCKT nanf401 1 2 3 4 5 6 8
M1 1 2 3 3 CMOSP W=7.70U L=0.70U GEO=0
M2 1 4 3 3 CMOSP W=7.70U L=0.70U GEO=0
M3 1 5 3 3 CMOSP W=7.70U L=0.70U GEO=0
M4 1 6 3 3 CMOSP W=7.70U L=0.70U GEO=0
M5 1 2 7 8 CMOSN W=8.40U L=0.70U GEO=0
M6 7 4 9 8 CMOSN W=8.40U L=0.70U GEO=0
M7 9 5 10 8 CMOSN W=8.40U L=0.70U GEO=0
M8 10 6 8 8 CMOSN W=8.40U L=0.70U GEO=0
C1 8 1 1.0F
C2 3 1 1.0F
C3 2 1 1.0F
C4 1 0 7.0F
C5 6 0 3.0F
C6 4 0 3.0F
C7 5 0 3.0F
C8 2 0 3.0F
C9 8 0 6.0F
C10 3 0 7.0F
*** Node Listing for subckt:  nanf401
** N0                          ==  IdealGND
** N1                [U=6]     ==  O
** N2                [U=3]     ==  D1
** N3                [U=9]     ==  Vdd!
** N4                [U=3]     ==  C1
** N5                [U=3]     ==  B1
** N6                [U=3]     ==  A1
** N7                [U=2]     ==  150
** N8                [U=6]     ==  GND!
** N9                [U=2]     ==  151
** N10               [U=2]     ==  152
.ENDS

** Subcircuit definition for nanf301
** Extraction file is /msd16/arnott/magic_work/PLL/nanf301.ext
.SUBCKT nanf301 1 2 3 4 5 7
M1 1 2 3 3 CMOSP W=8.40U L=0.70U GEO=0
M2 1 4 3 3 CMOSP W=8.40U L=0.70U GEO=0
M3 1 5 3 3 CMOSP W=8.40U L=0.70U GEO=0
M4 6 2 7 7 CMOSN W=8.05U L=0.70U GEO=0
M5 6 4 8 7 CMOSN W=8.05U L=0.70U GEO=0
```

```
M6 8 5 1 7 CMOSN W=8.05U L=0.70U GEO=0
C1 5 1 1.0F
C2 3 1 1.0F
C3 4 1 1.0F
C4 1 0 6.0F
C5 5 0 3.0F
C6 2 0 3.0F
C7 4 0 3.0F
C8 7 0 5.0F
C9 3 0 6.0F
*** Node Listing for subckt:  nanf301
** N0                          ==  IdealGND
** N1                [U=5]     ==  O
** N2                [U=3]     ==  A1
** N3                [U=7]     ==  Vdd!
** N4                [U=3]     ==  B1
** N5                [U=3]     ==  C1
** N6                [U=2]     ==  150
** N7                [U=5]     ==  GND!
** N8                [U=2]     ==  151
.ENDS

** Subcircuit definition for nanf201
** Extraction file is /msd16/arnott/magic_work/PLL/nanf201.ext
.SUBCKT nanf201 1 2 3 4 6
M1 1 2 3 3 CMOSP W=8.75U L=0.70U GEO=0
M2 1 4 3 3 CMOSP W=8.75U L=0.70U GEO=0
M3 5 2 6 6 CMOSN W=7.35U L=0.70U GEO=0
M4 5 4 1 6 CMOSN W=7.35U L=0.70U GEO=0
C1 1 2 1.0F
C2 1 3 1.0F
C3 1 0 5.0F
C4 2 0 3.0F
C5 4 0 3.0F
C6 6 0 4.0F
C7 3 0 5.0F
*** Node Listing for subckt:  nanf201
** N0                          ==  IdealGND
** N1                [U=4]     ==  O
** N2                [U=3]     ==  A1
** N3                [U=5]     ==  Vdd!
** N4                [U=3]     ==  B1
** N5                [U=2]     ==  150
** N6                [U=4]     ==  GND!
.ENDS

** Subcircuit definition for div_by_4
** Extraction file is /msd16/arnott/magic_work/PLL/div_by_4.ext
.SUBCKT div_by_4 1 2 3 4 5 6 7 8 9 10 11 12 110
** Instance-id:   cmldff_0
X1 4 6 7 5 1 2 3 10 110 cmldff1
** Instance-id:   cmldff2_0
X2 9 8 6 4 12 11 110 cmldff2
C1 110 0 1.0F
C2 3 0 6.0F
```

```
C3 10 0 3.0F
C4 6 0 4.0F
C5 4 0 4.0F
C6 1 0 78.0F
C7 2 0 5.0F
*** Node Listing for subckt:  div_by_4
** N0                          ==  IdealGND
** N1                 [U=2]     ==  RB
** N2                 [U=2]     ==  Vreff
** N3                 [U=2]     ==  CAP
** N4                 [U=3]     ==  DIV2-
** N5                 [U=2]     ==  cmldff_0/N8
** N6                 [U=3]     ==  DIV2+
** N7                 [U=2]     ==  cmldff_0/N6
** N8                 [U=2]     ==  cmldff2_0/N2
** N9                 [U=2]     ==  cmldff2_0/N1
** N10                [U=2]     ==  RVRF
** N11                [U=2]     ==  cmldff2_0/9_112_603#
** N12                [U=2]     ==  cmldff2_0/N12
** N110               [U=3]     ==  N110
.ENDS

** Subcircuit definition for cmldff
** Extraction file is /msd16/arnott/magic_work/PLL/cmldff.ext
.SUBCKT cmldff 1 2 6 8 12 44 45 110
M1 1 1 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M2 2 2 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M3 1 5 4 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M4 2 3 4 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M5 4 6 7 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M7 7 12 0 0 CMOSN M=6 W=17.50U L=2.45U GEO=0
M8 13 8 7 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M9 1 2 13 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M10 2 1 13 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M11 5 5 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M12 5 2 9 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M13 9 8 11 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M14 3 1 9 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M15 3 3 110 110 CMOSP M=3 W=7.00U L=0.70U GEO=0
M16 11 12 0 0 CMOSN M=6 W=17.50U L=2.45U GEO=0
M17 5 3 10 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M18 3 5 10 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M19 10 6 11 0 CMOSN M=5 W=7.00U L=0.70U GEO=0
M25 40 40 110 110 CMOSP M=3 W=3.50U L=0.70U GEO=0
M26 45 40 110 110 CMOSP M=3 W=3.50U L=0.70U GEO=0
M27 40 2 43 0 CMOSN M=4 W=7.00U L=0.70U GEO=0
M28 45 1 43 0 CMOSN M=4 W=7.00U L=0.70U GEO=0
M29 43 44 0 0 CMOSN M=4 W=7.00U L=2.45U GEO=0
M30 44 44 0 0 CMOSN M=4 W=7.00U L=2.45U GEO=0
C1 1 5 1.0F
C2 9 1 2.0F
C3 2 110 1.0F
C4 5 2 1.0F
C5 7 12 5.0F
C6 8 6 1.0F
```

```
C7 9 2 2.0F
C8 10 3 2.0F
C9 40 45 1.0F
C10 44 0 1.0F
C11 4 5 2.0F
C12 11 12 5.0F
C13 43 0 1.0F
C14 2 0 1.0F
C15 5 3 1.0F
C16 7 6 2.0F
C17 10 45 1.0F
C18 8 7 2.0F
C19 11 6 2.0F
C20 44 43 4.0F
C21 1 2 1.0F
C22 45 110 1.0F
C23 3 0 1.0F
C24 10 5 2.0F
C25 1 4 1.0F
C26 11 8 2.0F
C27 1 3 1.0F
C28 1 13 3.0F
C29 40 2 2.0F
C30 12 0 6.0F
C31 5 0 1.0F
C32 2 3 1.0F
C33 45 1 2.0F
C34 4 3 2.0F
C35 13 2 3.0F
C36 1 110 1.0F
C37 110 0 196.0F
C38 10 0 43.0F
C39 11 0 56.0F
C40 12 0 81.0F
C41 13 0 33.0F
C42 40 0 16.0F
C43 43 0 31.0F
C44 44 0 50.0F
C45 45 0 67.0F
C46 1 0 175.0F
C47 2 0 174.0F
C48 3 0 129.0F
C49 4 0 27.0F
C50 5 0 120.0F
C51 6 0 86.0F
C52 7 0 75.0F
C53 8 0 81.0F
C54 9 0 35.0F
*** Node Listing for subckt:  cmldff
** N0                          ==  IdealGND
** N1              [U=8]       ==  N1
** N2              [U=8]       ==  N2
** N3              [U=6]       ==  N3
** N4              [U=3]       ==  N4
** N5              [U=6]       ==  N5
```

```
** N6                    [U=3]      ==  N6
** N7                    [U=3]      ==  N7
** N8                    [U=3]      ==  N8
** N9                    [U=3]      ==  N9
** N10                   [U=3]      ==  N10
** N11                   [U=3]      ==  N11
** N12                   [U=3]      ==  N12
** N13                   [U=3]      ==  N13
** N40                   [U=4]      ==  N40
** N43                   [U=3]      ==  N43
** N44                   [U=4]      ==  N44
** N45                   [U=3]      ==  N45
** N110                  [U=13]     ==  N110
.ENDS

** Subcircuit definition for dfnf311
** Extraction file is /msd16/arnott/magic_work/PLL/dfnf311.ext
.SUBCKT dfnf311 2 3 8 10 12 14
M1 1 2 3 3 CMOSP W=8.05U L=0.70U GEO=0
M2 4 1 3 3 CMOSP W=8.05U L=0.70U GEO=0
M3 5 6 3 3 CMOSP W=7.70U L=0.70U GEO=0
M4 7 8 3 3 CMOSP W=3.50U L=0.70U GEO=0
M5 7 1 6 3 CMOSP W=3.50U L=0.70U GEO=0
M6 6 5 9 3 CMOSP W=3.15U L=0.70U GEO=0
M7 9 4 3 3 CMOSP W=3.15U L=0.70U GEO=0
M8 1 2 10 10 CMOSN W=4.90U L=0.70U GEO=0
M9 4 1 10 10 CMOSN W=4.90U L=0.70U GEO=0
M10 11 4 3 3 CMOSP W=5.95U L=0.70U GEO=0
M11 11 5 12 3 CMOSP W=5.95U L=0.70U GEO=0
M12 12 1 13 3 CMOSP W=10.50U L=0.70U GEO=0
M13 13 14 3 3 CMOSP W=10.50U L=0.70U GEO=0
M14 14 12 3 3 CMOSP W=10.85U L=0.70U GEO=0
M15 5 6 10 10 CMOSN W=5.25U L=0.70U GEO=0
M16 15 4 10 10 CMOSN W=5.25U L=0.70U GEO=0
M17 15 8 6 10 CMOSN W=5.25U L=0.70U GEO=0
M18 6 1 16 10 CMOSN W=3.85U L=0.70U GEO=0
M19 16 5 10 10 CMOSN W=3.85U L=0.70U GEO=0
M20 17 5 10 10 CMOSN W=2.45U L=0.70U GEO=0
M21 17 1 12 10 CMOSN W=2.45U L=0.70U GEO=0
M22 12 4 18 10 CMOSN W=7.00U L=0.70U GEO=0
M23 18 14 10 10 CMOSN W=7.00U L=0.70U GEO=0
M24 14 12 10 10 CMOSN W=7.00U L=0.70U GEO=0
C1 10 5 1.0F
C2 12 10 1.0F
C3 3 5 1.0F
C4 12 3 1.0F
C5 1 4 2.0F
C6 1 10 1.0F
C7 1 3 2.0F
C8 14 10 1.0F
C9 14 3 1.0F
C10 4 10 1.0F
C11 6 0 7.0F
C12 2 0 3.0F
C13 8 0 3.0F
```

```
C14 1 0 13.0F
C15 5 0 7.0F
C16 14 0 5.0F
C17 12 0 5.0F
C18 4 0 12.0F
C19 10 0 13.0F
C20 3 0 14.0F
*** Node Listing for subckt:  dfnf311
** N0                          ==  IdealGND
** N1                [U=8]     ==  20
** N2                [U=3]     ==  CLK2
** N3                [U=21]    ==  Vdd!
** N4                [U=6]     ==  23
** N5                [U=6]     ==  25
** N6                [U=6]     ==  22
** N7                [U=2]     ==  120
** N8                [U=3]     ==  DATA1
** N9                [U=2]     ==  121
** N10               [U=21]    ==  GND!
** N11               [U=2]     ==  122
** N12               [U=7]     ==  Q_b
** N13               [U=2]     ==  123
** N14               [U=5]     ==  Q
** N15               [U=2]     ==  150
** N16               [U=2]     ==  151
** N17               [U=2]     ==  152
** N18               [U=2]     ==  153
.ENDS

** Subcircuit definition for hp50_SE
** Extraction file is /msd16/arnott/magic_work/PLL/hp50_SE.ext
.SUBCKT hp50_SE 1 2
** Instance-id:   PAD
X1 1 HP50PAD
C1 1 0 670.0F
C2 2 0 96.0F
*** Node Listing for subckt:  hp50_SE
** N0                          ==  IdealGND
** N1                [U=2]     ==  PAD
** N2                [U=1]     ==  Vss
.ENDS

** Subcircuit definition for hp50_SW
** Extraction file is /msd16/arnott/magic_work/PLL/hp50_SW.ext
.SUBCKT hp50_SW 1 2
** Instance-id:   PAD
X1 2 HP50PAD
* Unconnected Subcircuits Listing:
* Hiding> Name='ornlcpy270_0' (Type=ornlcpy270)
C1 1 2 133.0F
C2 1 0 209.0F
C3 2 0 1569.0F
*** Node Listing for subckt:  hp50_SW
** N0                          ==  IdealGND
** N1                [U=1]     ==  Vdd
```

```
** N2                [U=2]      ==  PAD
.ENDS

** Subcircuit definition for hp50_NE
** Extraction file is /msd16/arnott/magic_work/PLL/hp50_NE.ext
.SUBCKT hp50_NE 1 2
** Instance-id:   PAD
X1 2 HP50PAD
C1 2 1 325.0F
C2 1 0 53.0F
C3 2 0 1991.0F
*** Node Listing for subckt:  hp50_NE
** N0                          ==  IdealGND
** N1                [U=1]     ==  Vdd
** N2                [U=2]     ==  PAD
.ENDS

** Subcircuit definition for hp50_big
** Extraction file is /msd16/arnott/magic_work/PLL/hp50_big.ext
.SUBCKT hp50_big 1 2 3
** Instance-id:   PAD
X1 3 HP50PAD
C1 1 3 209.0F
C2 2 3 209.0F
C3 1 0 169.0F
C4 2 0 169.0F
C5 3 0 997.0F
*** Node Listing for subckt:  hp50_big
** N0                          ==  IdealGND
** N1                [U=1]     ==  Vdd
** N2                [U=1]     ==  Vss
** N3                [U=2]     ==  PAD
.ENDS

** Subcircuit definition for hp50_NW
** Extraction file is /msd16/arnott/magic_work/PLL/hp50_NW.ext
.SUBCKT hp50_NW 1 2
** Instance-id:   PAD
X1 1 HP50PAD
* Unconnected Subcircuits Listing:
* Hiding> Name='1_0' (Type=ornlcpy270)
C1 1 0 670.0F
C2 2 0 96.0F
*** Node Listing for subckt:  hp50_NW
** N0                          ==  IdealGND
** N1                [U=2]     ==  PAD
** N2                [U=1]     ==  Vss
.ENDS

** Subcircuit definition for switch_core
** Extraction file is /msd16/arnott/magic_work/PLL/switch_core.ext
.SUBCKT switch_core 1 2 3 VDD 5 6 7 GND 9 10 11 12 13 14 15 16 17
M1 1 2 3 VDD CMOSP M=5 W=22.75U L=0.70U GEO=0
M2 5 6 3 VDD CMOSP M=5 W=22.75U L=0.70U GEO=0
M3 3 7 1 GND CMOSN M=10 W=15.05U L=0.70U GEO=0
```

```
M4 3 9 5 GND CMOSN M=10 W=15.05U L=0.70U GEO=0
M5 10 11 12 GND CMOSN M=10 W=15.05U L=0.70U GEO=0
M6 12 15 10 16 CMOSP M=5 W=22.75U L=0.70U GEO=0
M7 13 14 12 GND CMOSN M=10 W=15.05U L=0.70U GEO=0
M8 12 17 13 16 CMOSP M=5 W=22.75U L=0.70U GEO=0
C1 3 1 10.0F
C2 13 12 11.0F
C3 3 5 10.0F
C4 12 10 11.0F
C5 12 0 127.0F
C6 6 0 17.0F
C7 15 0 17.0F
C8 7 0 29.0F
C9 GND 0 108.0F
C10 10 0 70.0F
C11 1 0 59.0F
C12 9 0 29.0F
C13 5 0 59.0F
C14 16 0 31.0F
C15 11 0 29.0F
C16 13 0 70.0F
C17 3 0 162.0F
C18 2 0 17.0F
C19 17 0 18.0F
C20 VDD 0 31.0F
C21 14 0 25.0F
*** Node Listing for subckt:  switch_core
** N0                          ==  IdealGND
** N1                [U=3]     ==  8_106_510#
** N2                [U=2]     ==  8_158_656#
** N3                [U=5]     ==  8_84_510#
** N5                [U=3]     ==  8_400_510#
** N6                [U=2]     ==  8_460_656#
** N7                [U=2]     ==  8_102_488#
** N9                [U=2]     ==  8_396_488#
** N10               [U=3]     ==  8_84_290#
** N11               [U=2]     ==  8_102_286#
** N12               [U=5]     ==  8_106_290#
** N13               [U=3]     ==  8_394_290#
** N14               [U=2]     ==  8_412_286#
** N15               [U=2]     ==  8_158_74#
** N16               [U=3]     ==  6_108_38#
** N17               [U=2]     ==  8_468_74#
**********************************************************
** GND               [U=5]
** VDD               [U=3]
.ENDS

** Subcircuit definition for phfdet
** Extraction file is /msd16/arnott/magic_work/PLL/phfdet.ext
.SUBCKT phfdet Fref GND D_not Down UP VDD UP_not Fdiv
** Instance-id:   invf101_3
X1 Down D_not VDD GND invf101
** Instance-id:   invf101_2
X2 UP UP_not VDD GND invf101
```

```
** Instance-id:   nanf201_2
X3 7 13 VDD 9 GND nanf201
** Instance-id:   nanf201_3
X4 13 5 VDD 7 GND nanf201
** Instance-id:   nanf201_4
X5 12 4 VDD 5 GND nanf201
** Instance-id:   nanf201_5
X6 4 1 VDD 12 GND nanf201
** Instance-id:   nanf201_1
X7 9 D_not VDD Fdiv GND nanf201
** Instance-id:   nanf301_1
X8 D_not 5 VDD 7 9 GND nanf301
** Instance-id:   invf101_1
X9 5 10 VDD GND invf101
** Instance-id:   invf101_0
X10 10 8 VDD GND invf101
** Instance-id:   nanf401_0
X11 8 9 VDD 7 4 1 GND nanf401
** Instance-id:   nanf301_0
X12 UP_not 1 VDD 4 5 GND nanf301
** Instance-id:   nanf201_0
X13 1 Fref VDD UP_not GND nanf201
C1 D_not VDD 1.0F
C2 VDD 5 1.0F
C3 VDD UP_not 1.0F
C4 VDD 9 1.0F
C5 VDD 9 1.0F
C6 5 VDD 1.0F
C7 4 VDD 1.0F
C8 GND 0 2.0F
C9 Fdiv 0 3.0F
C10 7 0 41.0F
C11 10 0 1.0F
C12 4 0 37.0F
C13 12 0 2.0F
C14 13 0 4.0F
C15 Down 0 5.0F
C16 1 0 37.0F
C17 5 0 42.0F
C18 8 0 3.0F
C19 9 0 44.0F
C20 D_not 0 38.0F
C21 UP 0 5.0F
C22 VDD 0 1.0F
C23 Fref 0 2.0F
C24 UP_not 0 55.0F
*** Node Listing for subckt:  phfdet
** N0                          ==  IdealGND
************************************************************
** 1                  [U=4]
** 10                 [U=2]
** 12                 [U=2]
** 13                 [U=2]
** 4                  [U=4]
** 5                  [U=5]
```

```
** 7                    [U=4]
** 8                    [U=2]
** 9                    [U=4]
** Down                 [U=2]
** D_not                [U=4]
** Fdiv                 [U=2]
** Fref                 [U=2]
** GND                  [U=14]
** UP                   [U=2]
** UP_not               [U=4]
** VDD                  [U=14]
.ENDS

** Subcircuit definition for current_source
** Extraction file is /msd16/arnott/magic_work/PLL/current_source.ext
.SUBCKT current_source N110 N60 N1 N0 N50
M1 N1 N1 N2 N0 CMOSN W=19.95U L=3.85U GEO=0
M2 N2 N2 N0 N0 CMOSN W=19.95U L=1.05U GEO=0
M3 N4 N1 N3 N0 CMOSN W=19.95U L=1.05U GEO=0
M4 N3 N2 N0 N0 CMOSN W=19.95U L=1.05U GEO=0
M5 N5 N1 N6 N0 CMOSN W=19.95U L=1.05U GEO=0
M6 N6 N2 N0 N0 CMOSN W=19.95U L=1.05U GEO=0
M7 N8 N1 N7 N0 CMOSN W=19.95U L=1.05U GEO=0
M8 N7 N2 N0 N0 CMOSN W=19.95U L=1.05U GEO=0
M9 N8 N8 N9 N110 CMOSP W=19.95U L=1.05U GEO=0
M10 N9 N9 N110 N110 CMOSP W=19.95U L=1.05U GEO=0
M11 N12 N9 N110 N110 CMOSP W=19.95U L=1.05U GEO=0
M12 N10 N8 N12 N110 CMOSP W=19.95U L=1.05U GEO=0
M13 N13 N9 N110 N110 CMOSP W=19.95U L=1.05U GEO=0
M14 N11 N8 N13 N110 CMOSP W=19.95U L=1.05U GEO=0
M15 N5 N5 N110 N110 CMOSP M=4 W=19.95U L=3.85U GEO=0
M16 N4 N5 N30 N110 CMOSP M=4 W=19.95U L=1.05U GEO=0
M17 N30 N4 N110 N110 CMOSP M=4 W=19.95U L=1.05U GEO=0
M18 N40 N4 N110 N110 CMOSP M=4 W=19.95U L=1.05U GEO=0
M19 N60 N5 N40 N110 CMOSP M=4 W=19.95U L=1.05U GEO=0
M20 N10 N10 N0 N0 CMOSN W=19.95U L=3.85U GEO=0
M21 N11 N10 N33 N0 CMOSN W=19.95U L=1.05U GEO=0
M22 N33 N11 N0 N0 CMOSN W=19.95U L=1.05U GEO=0
M23 N44 N11 N0 N0 CMOSN W=19.95U L=1.05U GEO=0
M24 N50 N10 N44 N0 CMOSN W=19.95U L=1.05U GEO=0
C1 N2 N40 1.0F
C2 N10 N12 1.0F
C3 N3 N5 1.0F
C4 N2 N1 1.0F
C5 N3 N4 1.0F
C6 N2 N30 1.0F
C7 N1 N40 1.0F
C8 N2 N5 3.0F
C9 N40 N5 1.0F
C10 N7 N40 1.0F
C11 N11 N10 1.0F
C12 N2 N4 2.0F
C13 N1 N30 1.0F
C14 N12 N9 1.0F
C15 N1 N5 2.0F
```

```
C16 N30 N5 1.0F
C17 N11 N12 1.0F
C18 N8 N40 1.0F
C19 N40 N110 12.0F
C20 N1 N4 2.0F
C21 N12 N8 1.0F
C22 N30 N4 7.0F
C23 N4 N5 1.0F
C24 N60 N40 6.0F
C25 N30 N110 14.0F
C26 N7 N8 1.0F
C27 N110 N5 14.0F
C28 N9 N8 2.0F
C29 N10 0 166.0F
C30 N11 0 147.0F
C31 N12 0 96.0F
C32 N13 0 94.0F
C33 N30 0 200.0F
C34 N33 0 52.0F
C35 N40 0 215.0F
C36 N44 0 57.0F
C37 N50 0 39.0F
C38 N60 0 102.0F
C39 N0 0 687.0F
C40 N1 0 218.0F
C41 N2 0 257.0F
C42 N3 0 81.0F
C43 N4 0 304.0F
C44 N5 0 395.0F
C45 N6 0 75.0F
C46 N7 0 71.0F
C47 N8 0 199.0F
C48 N9 0 157.0F
C49 N110 0 944.0F
*** Node Listing for subckt:  current_source
** N0                          ==  IdealGND
*************************************************************
** N0                [U=21]
** N1                [U=6]
** N2                [U=6]
** N3                [U=2]
** N4                [U=4]
** N5                [U=5]
** N6                [U=2]
** N7                [U=2]
** N8                [U=5]
** N9                [U=5]
** N10               [U=5]
** N11               [U=4]
** N12               [U=2]
** N13               [U=2]
** N30               [U=2]
** N33               [U=2]
** N40               [U=2]
** N44               [U=2]
```

```
** N50                [U=2]
** N60                [U=2]
** N110               [U=18]
.ENDS

** Subcircuit definition for div_by_256
** Extraction file is /msd16/arnott/magic_work/PLL/div_by_256.ext
.SUBCKT div_by_256 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
21
** Instance-id:   div_by_4_0
X1 14 3 1 4 17 5 18 8 9 19 14 14 6 div_by_4
** Instance-id:   cmldff_0
X2 7 21 8 9 14 16 2 6 cmldff
** Instance-id:   dfnf311_0
X3 2 11 22 0 22 20 dfnf311
** Instance-id:   dfnf311_1
X4 20 11 23 0 23 10 dfnf311
** Instance-id:   dfnf311_2
X5 10 11 24 0 24 12 dfnf311
** Instance-id:   dfnf311_3
X6 12 11 25 0 25 13 dfnf311
** Instance-id:   dfnf311_4
X7 13 11 26 0 26 15 dfnf311
C1 26 0 11.0F
C2 1 0 1.0F
C3 9 0 4.0F
C4 16 0 19.0F
C5 19 0 1.0F
C6 8 0 5.0F
C7 15 0 1.0F
C8 13 0 1.0F
C9 2 0 11.0F
C10 11 0 11.0F
C11 6 0 5.0F
C12 14 0 56.0F
C13 20 0 1.0F
C14 18 0 1.0F
C15 5 0 1.0F
C16 17 0 1.0F
C17 4 0 1.0F
C18 23 0 11.0F
C19 22 0 11.0F
C20 12 0 1.0F
C21 10 0 1.0F
C22 24 0 11.0F
C23 25 0 11.0F
C24 7 0 2.0F
C25 3 0 1.0F
C26 21 0 3.0F
*** Node Listing for subckt:  div_by_256
** N0                          ==  IdealGND
** N1                [U=2]     ==  CAP
** N2                [U=3]     ==  DIV8_se
** N3                [U=2]     ==  Vreff
** N4                [U=2]     ==  DIV2-
```

```
** N5                  [U=2]      ==  DIV2+
** N6                  [U=3]      ==  VDD
** N7                  [U=2]      ==  DIV8+
** N8                  [U=3]      ==  DIV4-
** N9                  [U=3]      ==  DIV4+
** N10                 [U=3]      ==  DIV32
** N11                 [U=6]      ==  V_DIG
** N12                 [U=3]      ==  DIV64
** N13                 [U=3]      ==  DIV128
** N14                 [U=5]      ==  RB
** N15                 [U=2]      ==  DIV256
** N16                 [U=2]      ==  RFRV3
** N17                 [U=2]      ==  RFIN-
** N18                 [U=2]      ==  RFIN+
** N19                 [U=2]      ==  RVRF
** N20                 [U=3]      ==  DIV16
** N21                 [U=2]      ==  DIV8-
** N22                 [U=2]      ==  dfnf311_0/Q_b
** N23                 [U=2]      ==  dfnf311_1/Q_b
** N24                 [U=2]      ==  dfnf311_2/Q_b
** N25                 [U=2]      ==  dfnf311_3/Q_b
** N26                 [U=2]      ==  dfnf311_4/Q_b
.ENDS

** Subcircuit definition for mos_vco_extank
** Extraction file is /msd16/arnott/magic_work/PLL/mos_vco_extank.ext
.SUBCKT mos_vco_extank VDD L1 VCO_L1_BUFF_OUT GND L2 VCO_L2_BUFF_OUT
VCO_BUF_BIAS
+ VCO_BIAS
M1 3 L2 L1 GND CMOSN M=8 W=8.75U L=0.70U GEO=0
M2 L2 L1 3 GND CMOSN M=8 W=8.75U L=0.70U GEO=0
M3 VCO_BIAS VCO_BIAS GND GND CMOSN M=4 W=8.75U L=0.70U GEO=0
M4 3 VCO_BIAS GND GND CMOSN M=8 W=8.75U L=0.70U GEO=0
M5 VDD L2 VCO_L2_BUFF_OUT GND CMOSN M=6 W=7.00U L=0.70U GEO=0
M6 VCO_L2_BUFF_OUT VCO_BUF_BIAS GND GND CMOSN M=6 W=7.00U L=0.70U GEO=0
M7 VDD L1 VCO_L1_BUFF_OUT GND CMOSN M=6 W=7.00U L=0.70U GEO=0
M8 VCO_L1_BUFF_OUT VCO_BUF_BIAS GND GND CMOSN M=6 W=7.00U L=0.70U GEO=0
M9 VCO_BUF_BIAS VCO_BUF_BIAS GND GND CMOSN M=4 W=7.00U L=0.70U GEO=0
C1 VCO_L2_BUFF_OUT GND 1.0F
C2 GND 3 2.0F
C3 L1 3 7.0F
C4 3 L2 7.0F
C5 L1 L2 4.0F
C6 VCO_L2_BUFF_OUT VDD 2.0F
C7 VCO_L1_BUFF_OUT GND 1.0F
C8 GND VDD 8.0F
C9 VCO_L1_BUFF_OUT VDD 2.0F
C10 GND VCO_BIAS 6.0F
C11 VCO_BUF_BIAS GND 8.0F
C12 GND 0 357.0F
C13 VCO_BUF_BIAS 0 68.0F
C14 VCO_L1_BUFF_OUT 0 55.0F
C15 L1 0 101.0F
C16 L2 0 88.0F
C17 VCO_BIAS 0 36.0F
```

```
C18 VDD 0 108.0F
C19 VCO_L2_BUFF_OUT 0 50.0F
C20 3 0 58.0F
*** Node Listing for subckt:  mos_vco_extank
** N0                          ==  IdealGND
** N3                [U=3]     ==  N3
************************************************************
** GND               [U=15]
** L1                [U=4]
** L2                [U=4]
** VCO_BIAS          [U=4]
** VCO_BUF_BIAS      [U=5]
** VCO_L1_BUFF_OUT   [U=3]
** VCO_L2_BUFF_OUT   [U=3]
** VDD               [U=3]
.ENDS

** Subcircuit definition for couple_cap
** Extraction file is /msd16/arnott/magic_work/PLL/couple_cap.ext
.SUBCKT couple_cap 1 2 3
C1 2 1 HPCAP50 SCALE=1402.50
C1P 1 1 HPCAP50P SCALE=1402.5
* C1=4992.91FF C1P=0.14FF
C2 1 0 6.0F
C3 2 0 43.0F
C4 3 0 44.0F
*** Node Listing for subckt:  couple_cap
** N0                          ==  IdealGND
** N1                [U=3]     ==  BOT_PLATE
** N2                [U=2]     ==  top_plate
** N3                [U=1]     ==  guard
.ENDS

** Subcircuit definition for rf_frame
** Extraction file is /msd16/arnott/magic_work/PLL/rf_frame.ext
.SUBCKT rf_frame 1 2 3 4 GND_r 6 7 8 9 10 11 12 13 14 16 17 18 19 20 21
+ 22 23 24 26 27 28 29 30 31 32 33 34 Vdd_r 36 37 38 39 40
XPAD1 Vdd_r GND_r 1 hp50_big
XPAD2 Vdd_r GND_r 2 hp50_big
XPAD3 Vdd_r GND_r 3 hp50_big
XPAD4 Vdd_r GND_r 4 hp50_big
XPAD5 Vdd_r GND_r hp50_NE
XPAD6 Vdd_r GND_r 6 hp50_big
XPAD7 Vdd_r GND_r 7 hp50_big
XPAD8 Vdd_r GND_r 8 hp50_big
XPAD9 Vdd_r GND_r 9 hp50_big
XPAD10 Vdd_r GND_r 10 hp50_big
XPAD11 Vdd_r GND_r 11 hp50_big
XPAD12 Vdd_r GND_r 12 hp50_big
XPAD13 Vdd_r GND_r 13 hp50_big
XPAD14 Vdd_r GND_r 14 hp50_big
XPAD15 Vdd_r GND_r hp50_NW
XPAD16 Vdd_r GND_r 16 hp50_big
XPAD17 Vdd_r GND_r 17 hp50_big
XPAD18 Vdd_r GND_r 18 hp50_big
```

```
XPAD19 Vdd_r GND_r 19 hp50_big
XPAD20 Vdd_r GND_r 20 hp50_big
XPAD21 Vdd_r GND_r 21 hp50_big
XPAD22 Vdd_r GND_r 22 hp50_big
XPAD23 Vdd_r GND_r 23 hp50_big
XPAD24 Vdd_r GND_r 24 hp50_big
XPAD25 Vdd_r GND_r hp50_SW
XPAD26 Vdd_r GND_r 26 hp50_big
XPAD27 Vdd_r GND_r 27 hp50_big
XPAD28 Vdd_r GND_r 28 hp50_big
XPAD29 Vdd_r GND_r 29 hp50_big
XPAD30 Vdd_r GND_r 30 hp50_big
XPAD31 Vdd_r GND_r 31 hp50_big
XPAD32 Vdd_r GND_r 32 hp50_big
XPAD33 Vdd_r GND_r 33 hp50_big
XPAD34 Vdd_r GND_r 34 hp50_big
XPAD35 Vdd_r GND_r hp50_SE
XPAD36 Vdd_r GND_r 36 hp50_big
XPAD37 Vdd_r GND_r 37 hp50_big
XPAD38 Vdd_r GND_r 38 hp50_big
XPAD39 Vdd_r GND_r 39 hp50_big
XPAD40 Vdd_r GND_r 40 hp50_big
C1 19 0 1.0F
C2 24 0 1.0F
C3 1 0 1.0F
C4 27 0 1.0F
C5 32 0 1.0F
C6 4 0 1.0F
C7 12 0 1.0F
C8 Vdd_r 0 2.0F
C9 40 0 1.0F
C10 GND_r 0 2.0F
C11 7 0 1.0F
C12 20 0 1.0F
C13 38 0 1.0F
C14 18 0 1.0F
C15 23 0 1.0F
C16 26 0 1.0F
C17 31 0 1.0F
C18 3 0 1.0F
C19 11 0 1.0F
C20 29 0 1.0F
C21 34 0 1.0F
C22 6 0 1.0F
C23 14 0 1.0F
C24 37 0 1.0F
C25 9 0 1.0F
C26 17 0 1.0F
C27 22 0 1.0F
C28 30 0 1.0F
C29 2 0 1.0F
C30 10 0 1.0F
C31 28 0 1.0F
C32 33 0 1.0F
C33 13 0 1.0F
```

```
C34 36 0 1.0F
C35 8 0 1.0F
C36 16 0 1.0F
C37 21 0 1.0F
C38 39 0 1.0F
*** Node Listing for subckt:  rf_frame
** N0                          ==  IdealGND
** N1                [U=2]     ==  C21
** N2                [U=2]     ==  C20
** N3                [U=2]     ==  C19
** N4                [U=2]     ==  C18
** N6                [U=2]     ==  C17
** N7                [U=2]     ==  C16
** N8                [U=2]     ==  C15
** N9                [U=2]     ==  C14
** N10               [U=2]     ==  C13
** N11               [U=2]     ==  C12
** N12               [U=2]     ==  C11
** N13               [U=2]     ==  C10
** N14               [U=2]     ==  C9
** N16               [U=2]     ==  C8
** N17               [U=2]     ==  C7
** N18               [U=2]     ==  C6
** N19               [U=2]     ==  C5
** N20               [U=2]     ==  C4
** N21               [U=2]     ==  C3
** N22               [U=2]     ==  C2
** N23               [U=2]     ==  C1
** N24               [U=2]     ==  C0
** N26               [U=2]     ==  C35
** N27               [U=2]     ==  C34
** N28               [U=2]     ==  C33
** N29               [U=2]     ==  C32
** N30               [U=2]     ==  C31
** N31               [U=2]     ==  C30
** N32               [U=2]     ==  C29
** N33               [U=2]     ==  C28
** N34               [U=2]     ==  C27
** N36               [U=2]     ==  C26
** N37               [U=2]     ==  C25
** N38               [U=2]     ==  C24
** N39               [U=2]     ==  C23
** N40               [U=2]     ==  C22
************************************************************
** GND_r             [U=41]
** Vdd_r             [U=41]
.ENDS

** Subcircuit definition for charge_pump_core
** Extraction file is /msd16/arnott/magic_work/PLL/charge_pump_core.ext
.SUBCKT charge_pump_core UP DOWN_NOT DOWN current_source_bias Fdiv
Freff
+ Iout UP_NOT Ip+ Ip- VSS Vreff VDD
** Instance-id:   switch_core_0
X1 Vreff DOWN_NOT Ip+ VDD Iout DOWN DOWN VSS DOWN_NOT Vreff UP Ip- Iout
```

```
+ UP_NOT UP_NOT VDD UP switch_core
** Instance-id:   phfdet_0
X2 Freff VSS DOWN_NOT DOWN UP VDD UP_NOT Fdiv phfdet
** Instance-id:   current_source_0
X3 VDD Ip+ current_source_bias VSS Ip- current_source
C1 Fdiv VDD 1.0F
C2 VDD DOWN_NOT 1.0F
C3 DOWN_NOT VDD 1.0F
C4 Ip+ Iout 1.0F
C5 Ip+ Vreff 1.0F
C6 VSS Iout 1.0F
C7 VSS Vreff 1.0F
C8 UP_NOT UP 3.0F
C9 VDD Freff 4.0F
C10 VDD UP 3.0F
C11 UP Ip+ 1.0F
C12 VSS UP 2.0F
C13 Ip- Vreff 1.0F
C14 UP_NOT VSS 2.0F
C15 Vreff Ip+ 1.0F
C16 VSS Vreff 1.0F
C17 VDD VSS 25.0F
C18 VSS Ip- 2.0F
C19 VDD Fdiv 1.0F
C20 VSS Ip+ 1.0F
C21 VDD DOWN_NOT 1.0F
C22 UP 0 122.0F
C23 current_source_bias 0 36.0F
C24 Freff 0 13.0F
C25 Fdiv 0 14.0F
C26 VDD 0 1152.0F
C27 Ip- 0 57.0F
C28 DOWN 0 54.0F
C29 Ip+ 0 92.0F
C30 Iout 0 29.0F
C31 Vreff 0 28.0F
C32 VSS 0 860.0F
C33 DOWN_NOT 0 72.0F
C34 UP_NOT 0 115.0F
*** Node Listing for subckt:  charge_pump_core
** N0                          ==  IdealGND
************************************************************
** current_source_bias  [U=2]
** DOWN                [U=4]
** DOWN_NOT            [U=4]
** Fdiv                [U=2]
** Freff               [U=2]
** Iout                [U=3]
** Ip+                 [U=3]
** Ip-                 [U=3]
** UP                  [U=4]
** UP_NOT              [U=4]
** VDD                 [U=5]
** Vreff               [U=3]
** VSS                 [U=4]
```

```
.ENDS

** Subcircuit definition for rf_core
** Extraction file is /msd16/arnott/magic_work/PLL/rf_core.ext
.SUBCKT rf_core DIV_BIAS VCO_BUFF_L1_OUT DIV_BY_32 DIV_IN_L2 DIV_BY_64
+ VCO_BUFF_BIAS GND L1 DIV_IN_L1 DIV_BY_256 DIFF_AMP_BIAS VCO_BIAS 13
DIV_VDD
+ DIV_BY_2- DIV_BY_16 DIV_BY_2+ VCO_GND L2 DIV_BY_8+ DIV_VREFF
DIV_BY_8_se
+ DIV_VREFF_BIAS DIV_BY_4- VCO_BUFF_L2_OUT DIV_BY_128 DIV_CAP DIV_BY_4+
DIV_BY_8-
+ VCO_VDD
** Instance-id:   div_by_256_0
X1 DIV_CAP DIV_BY_8_se DIV_VREFF DIV_BY_2+ DIV_BY_2- DIV_VDD DIV_BY_8+
+ DIV_BY_4- DIV_BY_4+ DIV_BY_32 13 DIV_BY_64 DIV_BY_128 DIV_BIAS
DIV_BY_256
+ DIFF_AMP_BIAS DIV_IN_L2 DIV_IN_L1 DIV_VREFF_BIAS DIV_BY_16 DIV_BY_8-
+ div_by_256
** Instance-id:   mos_vco_extank_0
X2 VCO_VDD L1 VCO_BUFF_L1_OUT VCO_GND L2 VCO_BUFF_L2_OUT VCO_BUFF_BIAS
+ VCO_BIAS mos_vco_extank
** Instance-id:   couple_cap_1
X3 VCO_BUFF_L2_OUT DIV_IN_L2 GND couple_cap
** Instance-id:   couple_cap_0
X4 VCO_BUFF_L1_OUT DIV_IN_L1 GND couple_cap
C1 VCO_BUFF_L2_OUT 0 46.0F
C2 DIV_VDD 0 1.0F
C3 VCO_VDD 0 42.0F
C4 VCO_BUFF_L1_OUT 0 45.0F
C5 DIV_BY_2+ 0 1.0F
C6 DIV_BY_2- 0 1.0F
C7 VCO_BUFF_BIAS 0 3.0F
C8 L1 0 23.0F
C9 L2 0 30.0F
C10 VCO_GND 0 248.0F
C11 GND 0 273.0F
C12 DIFF_AMP_BIAS 0 2.0F
C13 VCO_BIAS 0 3.0F
C14 13 0 1.0F
C15 DIV_BY_16 0 1.0F
C16 DIV_BY_4+ 0 1.0F
C17 DIV_BY_4- 0 1.0F
C18 DIV_BY_32 0 1.0F
C19 DIV_BY_64 0 1.0F
C20 DIV_BY_8+ 0 1.0F
C21 DIV_BY_8- 0 1.0F
C22 DIV_IN_L1 0 8.0F
C23 DIV_IN_L2 0 7.0F
C24 DIV_BY_128 0 1.0F
C25 DIV_BIAS 0 1.0F
C26 DIV_BY_256 0 1.0F
C27 DIV_BY_8_se 0 1.0F
*** Node Listing for subckt:  rf_core
** N0                          ==  IdealGND
** N13              [U=2]      ==  DIGITAL_VDD
```

```
**************************************************************
** DIFF_AMP_BIAS      [U=2]
** DIV_BIAS           [U=2]
** DIV_BY_128         [U=2]
** DIV_BY_256         [U=2]
** DIV_BY_4+          [U=2]
** DIV_BY_4-          [U=2]
** DIV_BY_8+          [U=2]
** DIV_BY_8-          [U=2]
** DIV_BY_8_se        [U=2]
** DIV_BY_16          [U=2]
** DIV_BY_2+          [U=2]
** DIV_BY_2-          [U=2]
** DIV_BY_32          [U=2]
** DIV_BY_64          [U=2]
** DIV_CAP            [U=2]
** DIV_IN_L1          [U=3]
** DIV_IN_L2          [U=3]
** DIV_VDD            [U=2]
** DIV_VREFF          [U=2]
** DIV_VREFF_BIAS     [U=2]
** GND                [U=3]
** L1                 [U=2]
** L2                 [U=2]
** VCO_BIAS           [U=2]
** VCO_BUFF_BIAS      [U=2]
** VCO_BUFF_L1_OUT    [U=3]
** VCO_BUFF_L2_OUT    [U=3]
** VCO_GND            [U=2]
** VCO_VDD            [U=2]
.ENDS
****** top level cell is /msd16/arnott/magic_work/PLL/PLL.ext
** Instance-id:   rf_frame_0
X1 DIV_GND DIV_GND L1 DIV_GND DIV_GND DIV_GND L2 DIV_GND DIV_GND
DIV_GND
+ DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND
DIV_GND
+ DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND
DIV_GND
+ DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND DIV_GND
DIV_GND
+ DIV_GND rf_frame
** Instance-id:   charge_pump_core_0
X2 UP DOWN_NOT DOWN current_source_bias DIV_BY_256 Freff Iout UP_NOT
IP+
+ IP- DIV_GND Vreff charge_pump_core_vdd charge_pump_core
** Instance-id:   rf_core_0
X3 DIV_BIAS VCO_BUFF_L1_OUT DIV_BY_32 DIV_IN_L2 DIV_BY_64 VCO_BUFF_BIAS
+ DIV_GND L1 DIV_IN_L1 DIV_BY_256 DIFF_AMP_BIAS VCO_BIAS DIGITAL_VDD
DIV_VDD
+ DIV_BY_2- DIV_BY_16 DIV_BY_2+ VCO_GND L2 DIV_BY_8+ DIV_VREFF
DIV_BY_8_se
+ DIV_VREFF_BIAS DIV_BY_4- VCO_BUFF_L2_OUT DIV_BY_128 DIV_CAP DIV_BY_4+
DIV_BY_8-
+ VCO_VDD rf_core
```

```
C1 charge_pump_core_vdd DIV_GND 30.0F
C2 UP_NOT 0 1.0F
C3 VCO_BUFF_L2_OUT 0 2.0F
C4 DIV_VDD 0 1.0F
C5 current_source_bias 0 2.0F
C6 Freff 0 1.0F
C7 DIV_CAP 0 1.0F
C8 IP+ 0 1.0F
C9 IP- 0 2.0F
C10 VCO_VDD 0 9.0F
C11 VCO_BUFF_L1_OUT 0 1.0F
C12 DOWN 0 1.0F
C13 DIV_VREFF 0 1.0F
C14 DIV_VREFF_BIAS 0 1.0F
C15 VCO_BUFF_BIAS 0 1.0F
C16 Iout 0 1.0F
C17 L1 0 70.0F
C18 L2 0 10.0F
C19 VCO_GND 0 13.0F
C20 DIFF_AMP_BIAS 0 1.0F
C21 Vreff 0 1.0F
C22 VCO_BIAS 0 1.0F
C23 DIGITAL_VDD 0 1.0F
C24 UP 0 1.0F
C25 DIV_BY_2+ 0 1.0F
C26 DIV_BY_2- 0 1.0F
C27 DIV_BY_16 0 1.0F
C28 DIV_BY_4+ 0 1.0F
C29 DIV_BY_32 0 1.0F
C30 DIV_BY_4- 0 1.0F
C31 DIV_BY_64 0 1.0F
C32 DIV_BY_8+ 0 1.0F
C33 DIV_BY_8- 0 1.0F
C34 DOWN_NOT 0 1.0F
C35 DIV_GND 0 18091.0F
C36 DIV_IN_L1 0 1.0F
C37 DIV_BY_8_se 0 1.0F
C38 DIV_IN_L2 0 1.0F
C39 DIV_BY_128 0 1.0F
C40 DIV_BIAS 0 1.0F
C41 DIV_BY_256 0 94.0F
C42 charge_pump_core_vdd 0 67.0F
*** Node Listing for subckt:  PLL
** N0                          ==  IdealGND
*************************************************************
** charge_pump_core_vdd  [U=1]
** current_source_bias  [U=1]
** DIFF_AMP_BIAS     [U=1]
** DIGITAL_VDD       [U=1]
** DIV_BIAS          [U=1]
** DIV_BY_128        [U=1]
** DIV_BY_2+         [U=1]
** DIV_BY_2-         [U=1]
** DIV_BY_256        [U=2]
** DIV_BY_4+         [U=1]
```

```
** DIV_BY_4-          [U=1]
** DIV_BY_8+          [U=1]
** DIV_BY_8-          [U=1]
** DIV_BY_8_se        [U=1]
** DIV_BY_16          [U=1]
** DIV_BY_32          [U=1]
** DIV_BY_64          [U=1]
** DIV_CAP            [U=1]
** DIV_GND            [U=38]
** DIV_IN_L1          [U=1]
** DIV_IN_L2          [U=1]
** DIV_VDD            [U=1]
** DIV_VREFF          [U=1]
** DIV_VREFF_BIAS     [U=1]
** DOWN               [U=1]
** DOWN_NOT           [U=1]
** Freff              [U=1]
** Iout               [U=1]
** IP+                [U=1]
** IP-                [U=1]
** L1                 [U=2]
** L2                 [U=2]
** UP                 [U=1]
** UP_NOT             [U=1]
** VCO_BIAS           [U=1]
** VCO_BUFF_BIAS      [U=1]
** VCO_BUFF_L1_OUT    [U=1]
** VCO_BUFF_L2_OUT    [U=1]
** VCO_GND            [U=1]
** VCO_VDD            [U=1]
** Vreff              [U=1]
************************************************************
*
* Model Definitions for HSPICE
*
************************************************************
.MODEL RHPPOLYSB50 R RES=90.0
.MODEL CHPPOLY50 C CAP=0.570FF
.MODEL HPCAP50P C CAP=0.000FF
.MODEL HPCAP50 C CAP=3.560FF
*0 errors and 0 warnings found.
```

Vita

James C. Arnott was born July 21, 1971, in Kingsport, Tennessee. He lived with his family in Surgoinsville, Tennessee. After receiving his high school diploma from Volunteer High School in Church Hill, Tennessee, in 1990, he began a career as an Automotive Service Technician. James began his academic career by enrolling at East Tennessee State University in Johnson City, Tennessee, in 1993, majoring in pre-engineering. James transferred to the University of Tennessee, Knoxville, in 1994, during the summer semester with a major of Electrical Engineering. James completed his undergraduate studies and graduated with his Bachelor of Science in Electrical Engineering in the spring semester in 1998. He immediately began his career as a graduate student at the University of Tennessee, Knoxville, majoring in Electrical Engineering. James' graduate work was conducted in the UT/ORNL Joint Program in Mixed Signal VLSI and Integrated Sensor program. James' hobbies and interests include flying, movies, and various outdoor activities.