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A PLL frequency synthesizer for a 300 MHz high temperature transceiver realized in 0.5um SOS technology

Andrew Philip Moor

To the Graduate Council:

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James M. Rochelle, Major Professor

We have read this thesis and recommend its acceptance:

Britton, Bouldin

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A PLL Frequency Synthesizer for a 300 MHz High Temperature Transceiver Realized In 0.5um SOS Technology

A Thesis
Presented for the
Master of Science
Degree

The University of Tennessee, Knoxville

Andrew Philip Moor
May 2001

Dedicated to my family and friends who
have motivated and supported me
throughout my college career.

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Abstract

This thesis presents a study of the design of a phase-lock loop (PLL) system, including specific designs for a voltage-controlled oscillator and programmable frequency divider, implemented in a 0.5um silicon-on-sapphire CMOS technology. The system is designed for use as a frequency synthesizer in a high-temperature transceiver. Several issues relating to high-temperature applications as well as the overall system architecture are presented. Principles of the PLL system are described, and critical design considerations are discussed. The designs of the VCO and programmable divider are described and analyzed in detail. A brief discussion of the design and analysis of other PLL components is presented. Prototyping and testing procedures are discussed and the results of the prototyped circuits are evaluated. Finally, a summary of the work is presented along with insights gained toward future research.

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Chapter 1

Overview

1.1 Introduction

In many commercial and industrial environments, system engineers can easily obtain process measurements and information by connecting a test instrument directly to a sensor. In some cases, information from many different sensors can be combined and routed to a different location for centralized monitoring. However, difficulties can arise in situations where the sensor itself is too large to monitor the target process, or the process environment itself is considered 'hostile' to measurements, due to extremes in atmospheric conditions, chemical reactivity, or temperature. In these cases, specialized systems must be designed to meet the challenges of the hostile environment while providing accurate measurement capability of the target process.

The implementation of remote measurement and monitoring systems for hostile environments poses a significant challenge to system engineers. In many cases, the constraints make traditional measurement techniques impractical or even impossible. Integrated circuit (IC) technology offers several distinct advantages which can be leveraged to meet the demands of hostile environments requiring sensors that must be relatively small, and be capable of operating over a wide range of temperature.

First of all, IC technology provides the capability to produce small, durable, and relatively inexpensive devices. Thousands of transistors and many types of passive devices can

be easily manufactured on a very small chip. Secondly, these devices have the potential to operate more predictably at higher temperatures than an equivalent discrete-component implementation. Devices on an integrated circuit can be matched to a much higher precision, and the effects of temperature gradients can be minimized by using appropriate layout techniques. Finally, recent innovations in IC fabrication have spurred new developments in sensor technology, yielding the ability to incorporate many unique, specialized, and highly accurate sensors on a single silicon substrate. On-chip sensors are considerably smaller and more accurate than many of their discrete counterparts. These benefits make IC technology an obvious solution for remote measurement applications where a high degree of measurement precision is required, but size constraints or unusual operating temperature requirements cannot be avoided.

Many variations of IC processing technology exist, such as bulk CMOS, Silicon-Germanium, and Gallium-Arsenide. However, the use of Silicon-on-Sapphire (SOS) processing provides several distinct advantages compared to traditional processes. First of all, devices fabricated in SOS are effectively isolated, because the sapphire substrate is a very good insulator. This prevents substrate leakage current flow between devices, translating into reduced noise and reduced power consumption, and the ability to increase the packing density of devices on a single chip [1]. In fact, analog and digital circuits can be easily implemented on the same chip, compared to the cumbersome design techniques required to achieve mixed signal circuits in traditional processes. SOS circuits are also more resistant to radiation effects, making them ideal for use in radio transmitters for applications such as cellular phones and communications satellites [1]. Thermal effects of SOS circuits differ significantly from other processes, because the

sapphire substrate has a lower thermal conductivity than bulk silicon [2]. Another advanced application of SOS technology is optical networking, where signals from fiber-optic cables can be processed and routed on a single chip [3]. Of these advantages, the noise-reducing properties of the insulating substrate are the primary reason for the selection of SOS technology for the PLL.

This thesis describes the design and testing of a phase-locked loop (PLL) to be used as a frequency synthesizer in a high-temperature remote sensor system. An overview of the PLL is presented, along with a discussion of critical performance criteria. Subsequent chapters present the design and analysis of two major sub-components of the PLL: a voltage-controlled oscillator (VCO) and a frequency divider. Simulation results and prototype test results are compared, and the feasibility of the design is evaluated.

1.2 Overview of Phase-Locked Loop Functionality

The primary function of a PLL is to synchronize a controllable oscillator with a precision reference oscillator. The controllable oscillator can operate at a much higher frequency than the reference if a frequency divider is also included in the loop. This makes PLLs useful in applications such as local oscillators for radios, clock generation for digital circuitry, and data synchronization for communication systems [4]. In general, the PLL can be interpreted as a negative-feedback system, where the error between the phase (or frequency) of the reference signal and output (feedback) signal is converted into a voltage that drives the oscillator. The PLL architecture for this application is composed of several modules, including a voltage-controlled oscillator (VCO), programmable

frequency divider, phase detector, charge pump, and a loop filter. More details regarding the functions of each block are presented in Chapters 2-4.

1.3 High Temperature System Considerations

Because the PLL is required to operate in a high temperature environment, special consideration must be given to temperature effects on the devices used. Adverse effects of temperature include physical breakdown of solder joints, potentially uncorrelated drift of device parameters such as resistance and capacitance, and deviations in operating frequency, stability, and output power. The voltage-controlled oscillator topology used in the PLL offers a limited amount of flexibility in dealing with temperature effects. In addition, the architecture of the PLL itself provides some compensation of temperature effects through the negative feedback loop. Specific details of temperature effects and related design issues for each block are presented in the following chapters.

1.4 Scope of Thesis

This thesis presents the design, development, simulation, and characterization of the VCO and programmable frequency divider as components of the PLL. Chapter 2 contains a brief overview of the other components of the PLL, including the phase detector, charge pump, and loop filter. Chapter 3 presents a detailed analysis of the VCO, including high-temperature considerations. Chapter 4 describes the design of the programmable divider. Chapter 5 presents a discussion of prototype fabrication issues, as well as the testing and characterization of the prototyped components. Chapter 6 contains the conclusion and a brief discussion of ideas for future improvements. Appendix A contains all source files used in the simulation of the VCO and programmable

divider. Appendix B contains post-layout extracted parameter source files used to simulate the VCO and programmable divider.

Chapter 2

Phase Locked Loop Design and Analysis

This chapter discusses the design and analysis of the phase-locked loop (PLL). The specific architecture used in the PLL design is based on a digital phase-locked loop topology, making use of a digital frequency divider and a digital phase detector. Advantages of this approach include a wide lock range, fast acquisition time, and straightforward implementation in CMOS technology. The loop is capable of generating frequencies from 250 to 350 MHz using a precision reference oscillator.

2.1 PLL System Architecture

A phase-locked loop is composed of five major components: a precision frequency reference, a phase detector and charge pump, a loop filter, a voltage-controlled oscillator (VCO), and a frequency divider (see Figure 2.1). The loop can be analyzed as a negative feedback control system [5, 6]. The signal from the precision frequency reference has very low phase noise and jitter. This signal is compared with the feedback signal, and the phase difference is converted into a current pulse using a circuit commonly known as a charge pump. These current pulses have a width proportional to the difference in phase (a longer pulse is generated by a larger phase difference). The current pulses are passed to the loop filter to generate a voltage, which in turn drives the voltage-controlled oscillator.

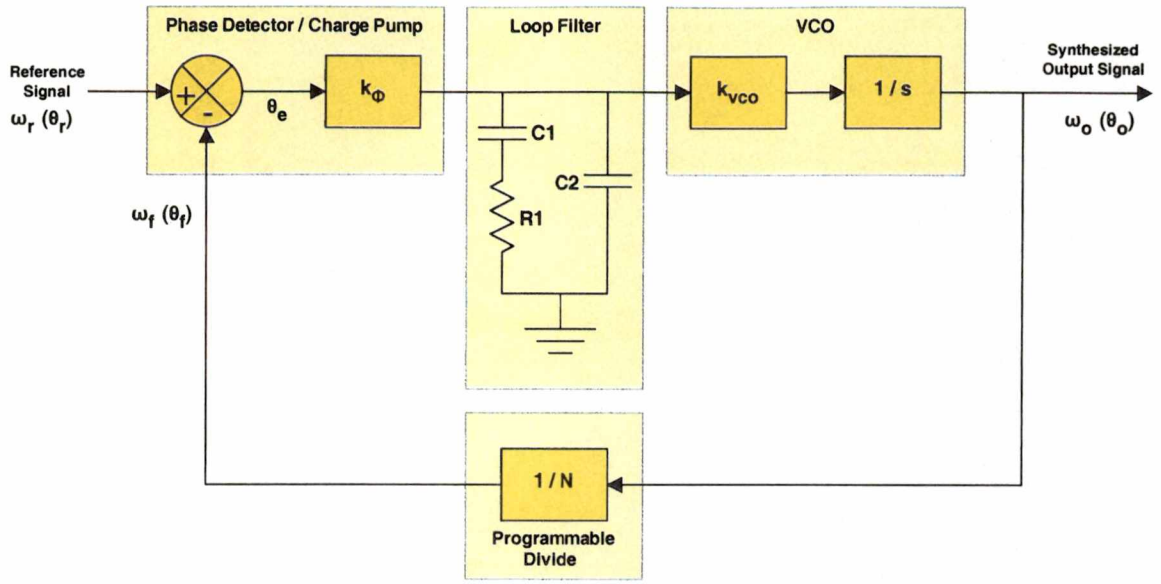


Figure 2.1: PLL block diagram

The VCO output frequency changes proportionally to its control voltage. This output signal drives the output of the PLL, and is also connected to the input of the programmable divider to complete the negative feedback loop. The divider reduces the frequency of the signal so that it is approximately equal to the precision reference frequency. The difference between the reference signal and the feedback signal then adjusts the VCO control voltage, until the error between the two is minimized. In this manner, the negative feedback loop allows the PLL to precisely generate arbitrary output frequencies that are multiples of the precision reference frequency.

2.2 Phase Detector and Charge Pump

One of the fundamental requirements of any phase locked loop is the capability to detect and quantify a difference in phase or frequency between the precision reference signal and the feedback signal. This can be accomplished using several different circuit

topologies [7]. However, one of the most common and easily implemented approaches is a digital phase comparator. This method uses two flip-flops, with one clocked by the reference signal and the other clocked by the feedback signal, as seen in Figure 2.2. [4]

The output of each flip-flop is connected through an AND gate and a delay element, ΔT, back to the reset lines of the flip-flops, and also to a current switch that controls the flow of current into or out of the loop filter. If the feedback signal is perfectly in phase with the reference signal, then the flip-flops will be clocked at the same time, causing the output of the AND gate to be asserted. Once this signal passes the delay element, both flip-flops will be reset simultaneously. The net effect of this perfect synchronization is to close both current switches simultaneously, and a short time later, open them simultaneously. Thus, if the switching currents are matched, the total current delivered to the loop filter through I_{OUT} is 0, thus the output of the loop filter remains unchanged and the VCO continues to run at the same frequency.

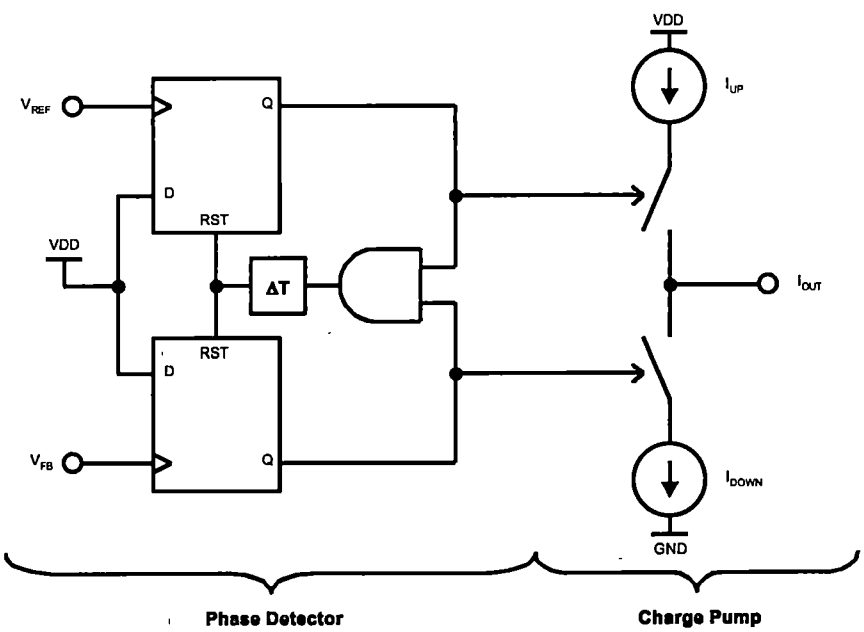


Figure 2.2: Phase detector / charge pump diagram
Adapted from: John Wetherell, "Phase Locked Loop Design and Analysis", 1997.

If, however, the feedback signal is out of phase with the reference signal, one of the two current switches will be closed before the other, depending on whether the feedback signal leads or lags the reference. The phase error between the two signals is translated into a current pulse delivered to (or pulled from) I_{OUT}. This process effectively adds or removes charge from the loop filter, thus changing the loop filter output voltage and the VCO operating frequency. A comparison of the charge pump output for these cases is given in Figure 2.3. When the loop filter is properly adjusted, the closed-loop system can be stabilized to automatically synchronize the feedback signal to the reference signal. Using a divider in the feedback path allows the closed-loop PLL output frequency to be a precise multiple of the signals in the phase detector.

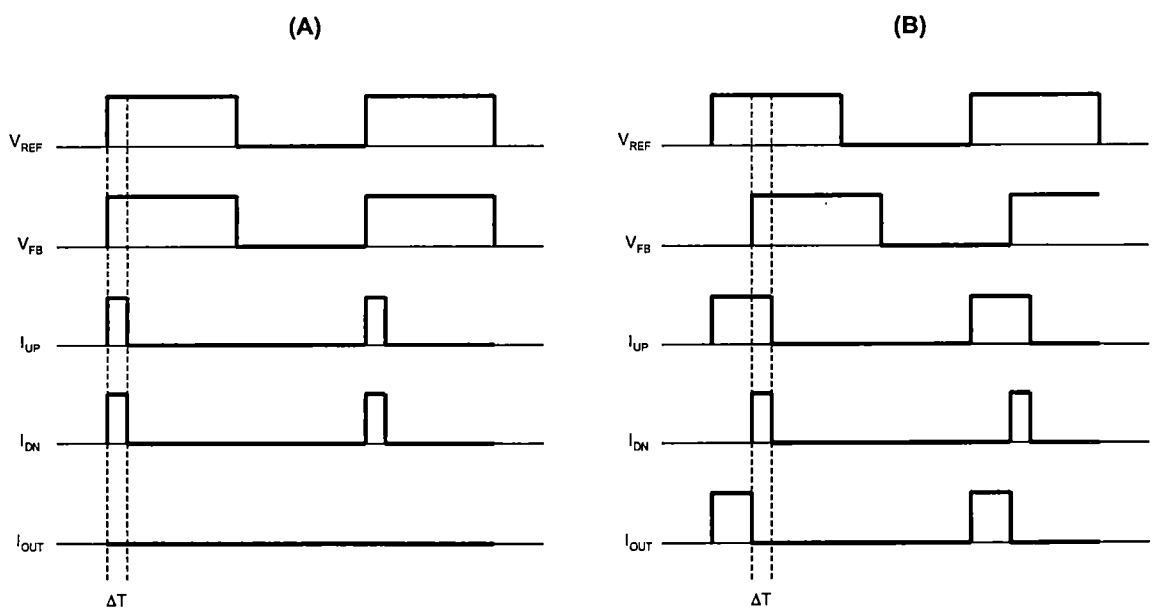


Figure 2.3: Charge pump output comparison
Synchronized (A) and unsynchronized (B)

2.3 Loop Filter

The purpose of the loop filter is to integrate the output of the charge pump, providing a voltage level to control the input of the VCO. Several types of loop filters are commonly used, including second and third-order filters. The selection of filter component values also controls what is commonly known as the loop bandwidth. This is the effective bandwidth of the signal present at the output of the charge pump. By reducing the loop bandwidth, the rejection of high-frequency transients is improved. However, the capture range becomes narrower, the lock time increases, and the overall loop phase margin is reduced [6]. The performance and stability of the entire PLL is therefore critically dependent on the loop filter.

Selection of appropriate loop filter component values is a somewhat open-ended process. One approach is to utilize the Laplace transform to derive an equivalent expression for the loop filter transfer function. Using the designations from Figure 2.1, the transfer function for the loop filter can be obtained [4].

$$F(s) = \frac{1 + RC_1 s}{s(C_1 + C_2)(1 + RC_1 \parallel C_2 s)} \qquad 2.1$$

The open-loop transfer function for the PLL can be found by incorporating the gain of the phase detector (K_ϕ) and VCO (K_v), and the division ratio (N).

$$A_{OL} = \frac{K_\phi K_v (1 + RC_1 s)}{N(C_1 + C_2)s(1 + RC_1 \parallel C_2 s)} \qquad 2.2$$

Setting the open-loop transfer function equal to unity allows the unity-gain bandwidth to be determined [4].

$$1 = \frac{K_\phi K_v \sqrt{1 + (RC_1\omega_u)^2}}{N(C_1 + C_2)\omega_u^2 \sqrt{1 + (RC_1 \| C_2\omega_u)^2}} \quad 2.3$$

The loop filter component values can be expressed in terms of their relationship to the pole and zero in the transfer function. First, an appropriate value of the unity-gain bandwidth, ω_u, should be determined. Various rules-of-thumb exist for choosing this value, with the goal of allowing a fast settling time while still filtering out spurs from the reference frequency. Finally, the locations of the pole and zero must be chosen to provide adequate phase margin for the system. A typical practice is to use a common factor to scale the unity-gain bandwidth, as in the following examples: [4]

$$\omega_Z = \frac{\omega_u}{4} \qquad \omega_P = 4 \cdot \omega_u \quad 2.4$$

Once these frequencies have been selected, the component values can be calculated using Equation 2.3, and are dependent only on the gain of the charge pump and VCO, the feedback division ratio, and the unity-gain bandwidth.

$$C_1 = \frac{4K_\phi K_v}{N\omega_u^2} - C_2 \quad 2.5$$

$$C_2 = \frac{K_\phi K_v}{4N\omega_u^2} \quad 2.6$$

$$R = \frac{4}{\omega_u C_1} \quad 2.7$$

2.4 Voltage Controlled Oscillator

With respect to the operation of the PLL, the voltage-controlled oscillator functions as a gain block, with units of Hertz per volt. The VCO uses an L-C tank circuit as a resonator, and includes varactor diodes to tune the resonant frequency. Output buffers are included to provide the capability to drive a 50-Ω load. The VCO gain and the maximum tuning range are determined by the selection of devices within the tank circuit, and are constraints which affect the design of other components in the PLL. Further details of the VCO design are given in Chapter 3.

2.5 Frequency Divider

The primary purpose of the frequency divider is to allow the VCO to run at a higher frequency than the reference frequency. In principle, this allows the accurate synthesis of much higher frequency signals which are phase locked to a lower-frequency reference signal. When a precision reference signal is used, the negative feedback loop will force the VCO to track the reference signal with almost the same level of precision. In this application, the frequency divider is a digital module consisting of standard-cell blocks. Programmability is also included, which allows the division ratio to be altered. While certain divider architectures can allow division by non-integer ratios, this capability was not required for the PLL design, thus an integer-only architecture was used to reduce the overall system complexity. Using the programmable divider, the PLL can be configured to generate one of many possible signals, all of which are integer multiples of the reference signal frequency and phase-locked to the reference signal. Additional details of the programmable divider design are presented in Chapter 4.

2.6 PLL Performance Issues

The performance of phase-locked loops is dependent on several design parameters. PLL systems are generally characterized according to their loop bandwidth, phase margin, and lock time. Loop bandwidth is the effective bandwidth of the signal at the output of the charge pump, and corresponds to the rate at which the VCO control voltage can vary (for example, due to FM modulation of the reference source) while maintaining the locked condition of the PLL. Phase margin relates to the stability of the PLL as a negative feedback system. Circuits with a low phase margin are subject to large overshoot and long settling time, and may exhibit a ringing response to a step input. Circuits with high phase margins are more stable, with little or no overshoot and a much shorter settling time. The lock time for a PLL is the time required for the loop to achieve phase lock after starting up. These system characteristics are somewhat mutually related, and are affected primarily by the design of the VCO, charge pump, and loop filter.

One of the most important goals in the design of a PLL is the minimization of phase noise. This type of noise is directly related to randomly occurring variations in the frequency of the PLL output signal. As an unavoidable condition in physical circuits, phase noise can best be understood using a phasor representation, as in Figure 2.4 [6, 7]. In this diagram, a small rotating phasor, with randomly-varying amplitude and frequency (V_n and ω_n) is superimposed on the phasor of an ideal oscillator, having a fixed amplitude and frequency (V_{ref} and ω_{ref}). The resultant vector (V_{out}) has a randomly-fluctuating phase difference from the reference signal, represented by ϕ_n. In relation to the frequency spectrum of the output signal, phase noise appears as a widening of the bandwidth of the

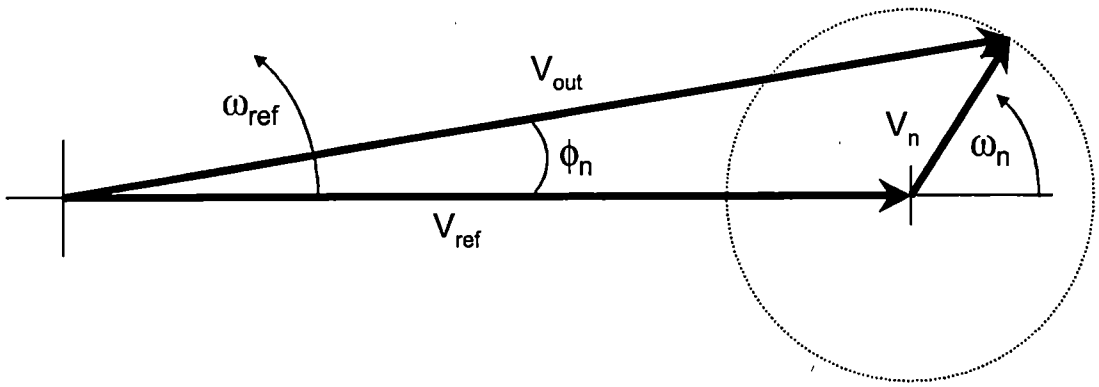


Figure 2.4: Phasor representation of phase noise

output signal. While an ideal sine wave would appear as an impulse in frequency space, a sine wave with phase noise would appear to have noise sidebands shaped like a concave-sided triangle, the width of which is proportional to the amount of phase noise present in the signal, as depicted in Figure 2.5 [7].

Phase noise can have a significant impact on the performance of systems which incorporate a PLL, such as RF transceivers. The sideband noise from the PLL can adversely affect both modulation and demodulation of signals using the PLL output as a carrier reference, resulting in a frequency-domain 'smearing' of the modulated signal. Depending on the amount of phase noise and the type of signal being modulated, the resulting output could be significantly degraded or even irrecoverable [8, 9]. In addition, government licenses for radio systems frequently specify spectral limitations that cannot be exceeded. Thus it is critical to minimize phase noise effects in the design of phase-locked loop systems [10, 11]

The majority of phase noise in a PLL can be attributed to one or more of the precision reference frequency source, the loop filter, and the VCO. The precision reference

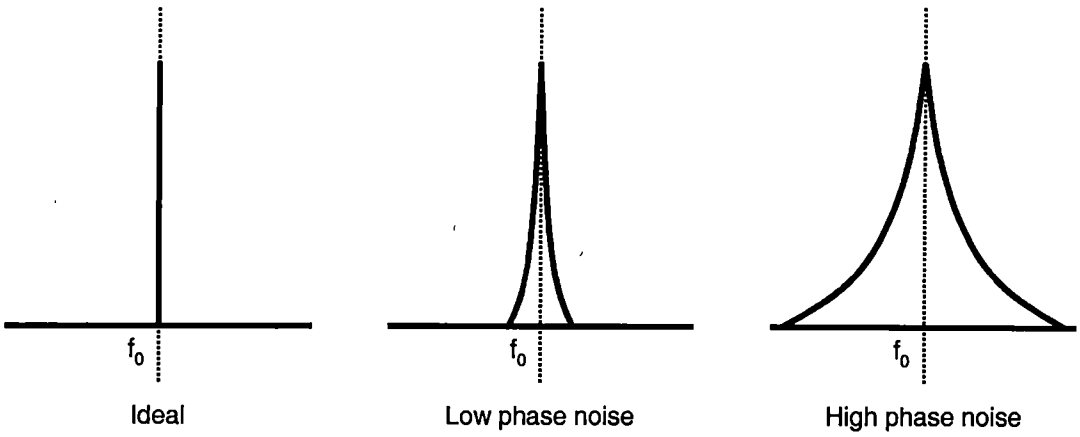


Figure 2.5: Examples of phase noise in output signal spectrum

frequency source, by itself, has a certain amount of phase noise. When placed inside the PLL, this reference phase noise is multiplied by the loop gain (set by the division ratio). The PLL loop appears as a low-pass filter to the reference frequency, thus a significant amount of the close-in phase noise (that which is very close to the output frequency) of the PLL output can be attributed to the reference frequency. This implies that to reduce the phase noise contributions from the reference source, an extremely high precision, low noise frequency reference must be used, such as a temperature-compensated crystal oscillator.

Noise effects present in the loop filter also contribute to the phase noise of the PLL. Components in the loop filter generate some amount of noise, which is passed to the control voltage of the VCO. Intuitively, this noise on the control voltage will create random fluctuations in the frequency of the VCO output. The final effect is that the noise of the loop filter is multiplied by the gain of the VCO, and the resulting phase noise adds directly to the output phase noise of the entire PLL. The effects of loop filter noise can be minimized by using low-noise circuit designs and a lower VCO gain.

The voltage-controlled oscillator also contributes to the phase noise of the PLL. Noise effects in the VCO introduce random deviations in the output frequency, resulting in phase noise. The amount of phase noise generated is dependent on several aspects of the VCO design, including the selection of passive components for the L-C resonator, the size of the active devices used, and the topology of the circuit. In PLLs using a very high precision reference frequency, the VCO is often a dominant source of phase noise. Minimizing phase noise from the VCO requires optimizing the closed-loop PLL bandwidth, because the loop appears as a high-pass filter relative to the VCO [6, 12]. While a small loop bandwidth would minimize the overall output phase noise, the lock time of the PLL and the phase noise contributed by the VCO within the loop bandwidth would be increased. As a consequence, the design must balance these trade-offs to arrive at an optimum solution, in which the loop bandwidth is set to minimize the effect of VCO phase noise relative to the overall PLL phase noise [7].

The primary difference between the noise generated by the reference frequency, loop filter, and VCO is the physical origin of the noise itself. Reference frequency noise is due mainly to jitter in the crystal oscillator, while noise in the charge pump can be attributed to the nonlinearities in the active devices. Loop filter noise is primarily due to white noise in the passive components of the filter. Phase noise generated by the VCO stems from noise in both the active and passive devices, as well as the topology of the oscillator circuit. Figure 2.6 [7] shows the relative contributions of phase noise by the major components in the PLL.

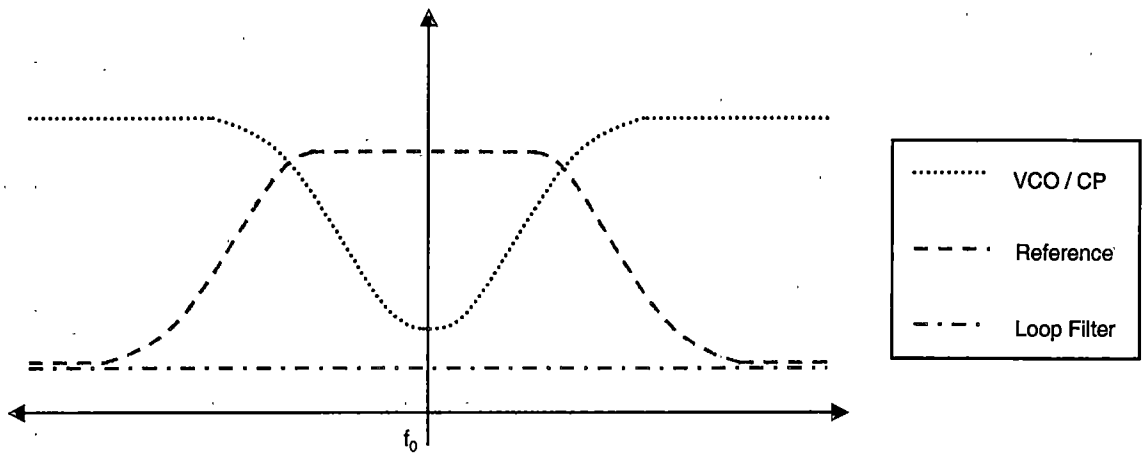


Figure 2.6: Contributions to overall phase noise in a PLL
Adapted from: R. K. Feeney and D. R. Hertling, "Fundamentals of Frequency Synthesis and Phase-Locked Loops", 1997.

An analysis of the overall phase noise of the PLL reveals that most of the close-in phase noise is due to the reference source and the charge pump, while the higher-frequency phase noise can be traced to the VCO. The loop filter noise, while still present, is not usually a dominant contributor to the output phase noise.

Chapter 3

Voltage-controlled Oscillator Design and Analysis

3.1 Specifications

The voltage-controlled oscillator (VCO) accepts a DC control voltage between 0 and 3.3 V and is capable of generating a sinusoidal output signal with a frequency between 250 and 350 MHz. The frequency of the output signal is regulated by the control voltage. Any changes in the control voltage produce a proportional change in the output frequency.

3.2 Architecture Considerations

Two common VCO topologies were considered, including ring oscillators and negative-g_m L-C oscillators (see Figure 3.1). A typical ring oscillator consists of several inverting

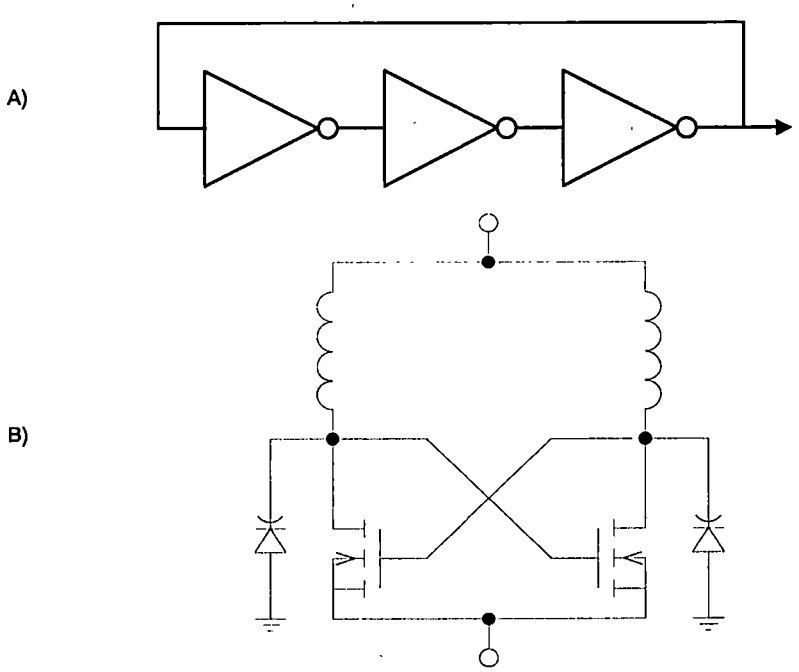


Figure 3.1: Schematic diagrams of typical oscillators
Simple ring oscillator (A) and simple negative-g_m L-C oscillator (B)

amplifiers, connected in series such that the total phase difference between the first stage and the last stage is 180 degrees. Ring oscillators are easily implemented using digital logic cells, and do not require passive components such as inductors and capacitors. They are commonly used in digital clock-recovery and clock-distribution circuits [13]. Unfortunately, this type of oscillator is plagued by poor phase noise performance, primarily because the transfer of energy within the circuit takes place during a transition between voltages, rather than at a minimum or maximum voltage [14]. In digital logic circuitry, this phase noise degradation may be of secondary concern, since other steps can be taken to assure synchronization of the clock throughout the chip. However, this limitation has prevented ring oscillators from being used in most RF applications, where good phase noise performance is required to meet spectral power limitation requirements.

A typical negative-g_m L-C oscillator consists of a resonant tank circuit connected to a cross-coupled differential pair of transistors. The transistors act to restore energy that is lost to resistive elements in the tank circuit, where the oscillation takes place. By the nature of the circuit, more energy is restored to the resonator during peaks in the oscillation. This reduces the effects of amplitude noise being translated into phase shifts in the resonant signal, and results in far superior phase noise performance when compared to a ring oscillator [10]. For this reason, the negative-g_m L-C oscillator is frequently used in RF applications. Many modern IC fabrication processes are capable of creating the necessary passive components on-chip, resulting in even better phase noise performance. Because of its good phase noise performance and stability, the negative-g_m L-C oscillator topology was selected as the basis for the VCO design.

3.3 Topology Analysis and Design Considerations

The complete VCO design incorporates several features to improve performance and output drive capability. A schematic diagram of the VCO is presented in Figure 3.2. Detailed analyses of the topology, design considerations, and relevant performance issues are presented in the following sections.

3.3.1 Tank Circuit

The core of any negative-g_m VCO is the tank circuit. This circuit is composed of the inductors, capacitors, and varactors, as well as the cross-coupled differential pair of NMOS transistors. The operating frequency and tuning range of the VCO are determined by these components. As a whole, the tank has a certain amount of inductance,

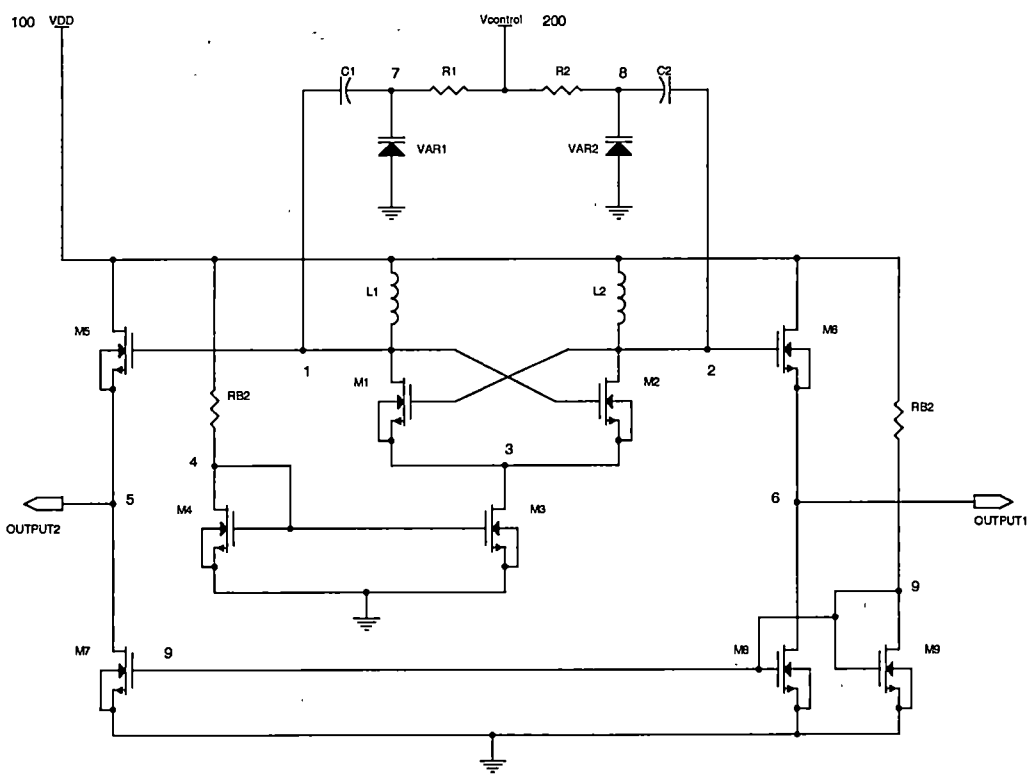


Figure 3.2: VCO Schematic

dominated by the off-chip discrete inductors (L1 and L2). A small amount of parasitic inductance is also introduced by the bond wires and board traces, although for the purposes of this design, the effects of parasitic inductance are negligible. The net tank capacitance is set by a combination of the varactor capacitances (VAR1 and VAR2) and the discrete chip capacitors (C1 and C2). In addition, there are several sources of stray capacitance which are accounted for. The chip, bond wires, and board traces all have a certain amount of parasitic capacitance. As a design parameter, the total capacitance due to these parasitic effects was estimated at 2 pF. The cross-coupled differential pair (M1 and M2) also have inherent capacitances, which were estimated at 0.5 pF per device. The total stray capacitance in the design was estimated at 3 pF.

The tank circuit also has a small amount of parasitic resistance, due to non-ideal effects of physical devices. For instance, the inductors have a small, but finite, series resistance in the wire, and the varactors and capacitors have similar resistances in the contacts and internal structure. Board traces and bond wires also contribute parasitic resistance. These parasitic resistances are precisely what the cross-coupled differential transistors are designed to offset. Energy lost in the parasitic resistance must be restored to maintain oscillation, and these transistors provide the means to do so.

3.3.2 Varactor Diodes

To achieve the VCO design goal of having an output frequency controlled by an input voltage, a means must be provided to adjust or 'tune' the resonant frequency of the oscillator tank circuit. This implies changing either the inductance or capacitance, or both. A simple approach to this task uses a varactor as the tuning element. This type of device

has a capacitance which varies as a function of its applied bias voltage. Depending on the specific type of varactor, the capacitance may or may not be linearly related to the bias voltage. Varactors are typically implemented as reverse-biased P-N junction diodes. In all P-N junction diodes, the depletion width of the junction is dependent on the bias voltage. Reverse-biasing a varactor diode causes the depletion width, w_d, to increase beyond the zero-bias value. Inherently, this also increases the charge in the depletion region. This fact means that the charge in the diode changes as a function of the reverse bias voltage, as shown in Equation 3.1 [15] where A is the cross-sectional area of the diode and N_A and N_D are the doping concentrations.

$$Q_n = q\left(\frac{N_A N_D}{N_A + N_D}\right) w_d A \qquad 3.1$$

The resulting capacitance can be expressed in terms of the zero-bias junction capacitance C_{j0}, the junction potential ϕ_j, and the reverse bias voltage, v_R.

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{v_R}{\phi_j}}} \qquad 3.2$$

The equation shows that the diode capacitance will be at a maximum when there is no reverse-bias voltage applied. The capacitance will decrease as the reverse-bias voltage increases. This provides a means of controlling the capacitance, and therefore the resonant frequency of the tank circuit, simply by altering the reverse-bias voltage on the varactors.

Modeling the non-ideal parasitic effects of varactors provides a more accurate estimation of actual performance. Most manufacturers provide a model which includes parasitic resistance, capacitance, and inductance. The particular varactors used in the VCO are the Alpha Industries SMV1236. The manufacturer's model, shown in Figure 3.3 [16], accounts for the parasitics mentioned above. In addition, the manufacturer provides a capacitance modeling equation [16], similar to Equation 3.2, which utilizes a set of process-extracted parameters.

$$C_V = \frac{C_{J0}}{\left(1 + \frac{V_R}{V_J}\right)^M} + C_P \qquad 3.3$$

The values V_J, C_P, and M are not representative of any physical quantities. They are merely curve-fitting parameters that allow the equation to more closely track the actual voltage-capacitance curve. The manufacturer's modeling parameters are presented in Table 3.1.

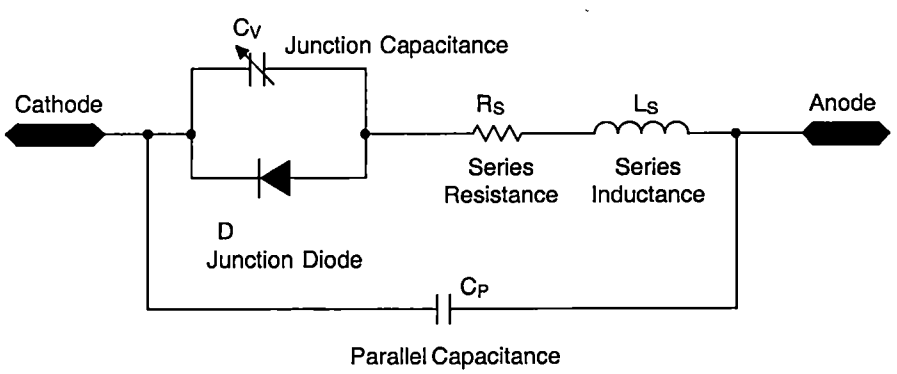


Figure 3.3: Varactor diode model
Source: Varactor SPICE Models for RF VCO Applications, Alpha Industries application note APN1004.

Table 3.1: Varactor diode modeling parameters for SMV1236

C_{J0}	21.63 pF
V_J	8 V
M	4.2
C_P	3.2 pF
R_S	0.5
L_S	1.7 nH

Some of the varactor parasitic values are quite important to the design, while others are negligible. For instance, the parasitic inductance is very small, and will not have a significant effect on the resonant frequency of the tank circuit unless the resonant frequency approaches the gigahertz range. The parasitic capacitance is also a very small percentage of the total tank capacitance, and can therefore be neglected. However, the parasitic resistance of the varactor cannot be easily overlooked. In fact, this resistance can have a significant effect on the quality factor of the tank circuit.

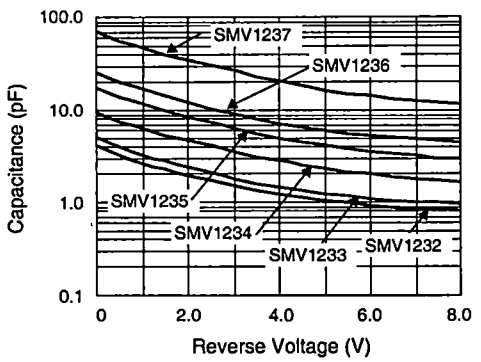
Additional information about the varactors can be obtained by inspecting the manufacturer's performance curves [17], shown in Figure 3.4. Using the capacitance vs. reverse voltage chart for the SMV1236 device, the measured characteristics of the varactor can be evaluated. These characteristics will be reflected in the tuning range of the tank circuit, as well as the gain of the VCO (Hz/volt). In addition, the series resistance vs. reverse voltage chart is useful in determining the anticipated parasitic resistance of the varactors, and in turn the effect on the quality factor of the tank. An important goal is to ensure that the series resistance remains fairly constant over the entire operating voltage, as this will maintain a relatively constant quality factor of the tank regardless of

the operating frequency. Lower parasitic resistances will also result in an increased quality factor.

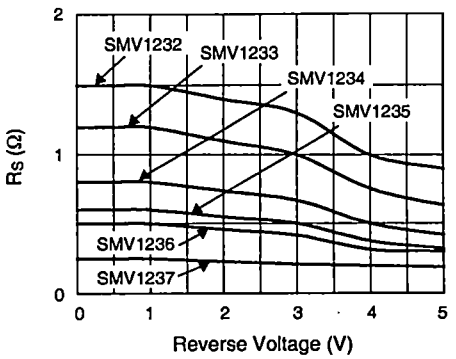
3.3.3 Integration of Varactor Diodes in the Tank Circuit

Varactor diodes are included in the tank circuit to provide voltage-controlled adjustment of the resonant frequency of the tank. However, the varactors alone may not be sufficient to establish the desired resonant frequency, or the available tuning range of the tank may result in an unnecessarily large VCO gain. To compensate for these effects, additional fixed capacitors can be inserted in the tank, in series with the varactors. Placing capacitors in series with the varactors will lower the effective capacitance of the tank, thus raising the center frequency of the VCO, and will also significantly increase the percentage change of tank capacitance contributed by the varactors, thus expanding the tuning range.

An added benefit of the additional capacitors is the isolation of the tank circuit from the cross-coupled transistors. The capacitors provide AC coupling between the varactor



Capacitance vs. Reverse Voltage



Series Resistance vs. Reverse Voltage @ 500 MHz

Figure 3.4: Varactor diode performance data
Source: Hyperabrupt Tuning Varactors, Alpha Industries product data sheet SMV1232-SMV1237.

diodes and the rest of the VCO. This allows the varactor tuning voltage to be referenced to ground instead of the bias voltage of the transistors, and facilitates the ability of other components in the PLL to drive the varactors. Additional problems are also avoided, such as inadvertent forward-biasing of the varactors. Without the series capacitors, the varactor bias voltage would be the difference between the tank circuit output and the control voltage, presenting the possibility of a forward-bias situation. Isolation resistors are included between the control voltage source and the varactors. Unlike the parasitic resistances in the tank, these resistors have no effect on the quality factor of the tank, provided that they are much larger than the equivalent parallel resistance of the tank.

3.3.4 Quality Factor of Tank Circuit

The performance of resonant circuits can be characterized using a quantity known as quality factor. This dimensionless value has no direct correspondence with a physical property. Instead, it is a measure of the energy stored in a circuit relative to the energy lost in the circuit. The most common definition of quality factor, Q, is shown in the following equation [18]:

$$Q = \frac{\omega_0}{BW} \tag{3.4}$$

In this case, ω_0 is the center frequency, and BW is the -3 dB bandwidth of the circuit. A perfect tank circuit, composed of lossless inductors and capacitors, would have an infinitely large quality factor. In reality, all tank circuits contain parasitic resistances which degrade the quality factor. The amount of degradation is directly proportional to the

equivalent parallel tank resistance, as shown in Equation 3.5 [18].

$$Q = R_P\sqrt{\frac{L}{C}} \tag{3.5}$$

Both the inductors and capacitors contribute to the tank resistance. The parasitic resistances of these components, usually expressed as a series resistance by the manufacturer, can be represented with equivalent parallel resistances, R_{PL} and R_{PC} [18].

$$R_{PL} = \frac{\omega_0^2 \cdot L^2}{R_{SL}} \tag{3.6}$$

$$R_{PC} = \frac{1}{\omega_0^2 \cdot C^2 \cdot R_{SC}} \tag{3.7}$$

Since all the tank components are connected in parallel, these resistances can be combined to derive the net parallel tank resistance [18].

$$R_P = \left(\frac{1}{R_{PL}} + \frac{1}{R_{PC}}\right)^{-1} \tag{3.8}$$

$$R_P = \frac{L^2}{C \cdot L \cdot R_{SC} + \frac{R_{SL}}{\omega_0^2}} \tag{3.9}$$

The results of this analysis provide a degree of insight into the design principles for tank circuits. Equation 3.9 demonstrates that the parasitic resistance of the capacitor contributes significantly to the reduction of the quality factor of the tank. Noting that the

the equivalent parallel resistance of an ideal tank circuit is infinite (which yields the ideal infinite Q), the design of physical tank circuits must seek to maximize the equivalent parallel resistance. This can be achieved by reducing the parasitic resistance of the inductor and capacitor. The parasitic resistance of the inductor is dependent on several factors, including the particular physical structure and configuration used. Because most inductors are metallic, parasitic resistance is usually quite small, and further minimization may not be possible. In contrast, the parasitic resistance of a capacitor is related to its capacitance as well as its physical structure, and these observations imply that the net capacitance should be minimized when designing a tank circuit [19]. Unfortunately, the other requirements of the tank, such as tuning range, may impose a lower bound on the capacitance that can be used.

3.3.5 Cross-coupled Differential Transistor Pair

The cross-coupled differential transistor pair (M1 and M2 in Figure 3.2) provide a means of restoring energy lost to parasitic resistances in the tank circuit. The transistors are biased from the positive rail voltage through the tank inductors (which have very small DC resistance) and a current mirror (M3 and M4 in Figure 3.2). The current mirror helps to establish the proper DC operating points to drive the output buffers.

A detailed analysis of the AC characteristics of the differential pair can be derived through the use of the Hybrid-Pi model [20, 21]. This model accounts for the parasitic effects of the transistors, as well as the small signal gain. Because the goal of the differential pair is to present a negative impedance to the tank circuit, thereby restoring energy, it is useful to evaluate the Hybrid-Pi model in such a way that the input impedance can be obtained.

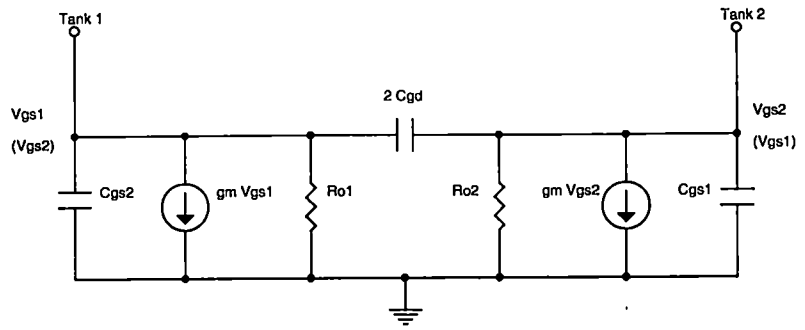


Figure 3.5: Hybrid-Pi model for cross-coupled differential transistor pair

The schematic in Figure 3.5 shows the circuit used for this evaluation. The Tank 1 and Tank 2 terminals represent the connections to the rest of the tank circuit. Each transistor is represented by an equivalent transconductance source, parasitic output resistance, and parasitic gate-source and gate-drain capacitances. Because the transistors are cross-coupled, the gate-drain capacitances appear in parallel with each other, thus doubling the capacitance between the transistors.

To analyze the input impedance seen by the tank circuit, the effects of each transistor can be represented as a single impedance block, Z1 and Z2, respectively, as seen in Figure 3.6. Assuming the transistors are well-matched, these impedances are equal, and can be obtained through the parallel combination of the transistor gate-source capacitance, transconductance, and output resistance.

$$Z_1 = Z_2 = \frac{1}{j\omega C_{gs}} \| \frac{1}{-g_m} \| r_o \qquad 3.10$$

$$= \left(j\omega C_{gs} - g_m + \frac{1}{r_o} \right)^{-1} \qquad 3.11$$

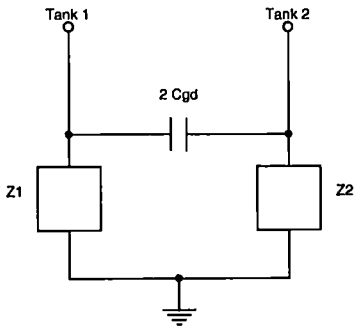


Figure 3.6: Equivalent impedance Hybrid-Pi model

$$Z_1 = Z_2 = \frac{r_o}{1 - g_m r_o + j\omega C_{gs} r_o} \tag{3.12}$$

The resulting impedance can then be combined with the parasitic gate-drain capacitances by employing the half-circuit technique. This additional capacitance is then in parallel with the gate-source capacitance. After combining all the parasitic effects of the differential transistor pair, the total input impedance seen by the tank circuit, Z_{in} is:

$$Z_{in} = \frac{2r_o}{1 - g_m r_o + j\omega r_o (C_{gs} + 4C_{gd})} \tag{3.13}$$

3.3.6 VCO Resonant Frequency and Quality Factor

The remaining components of the tank circuit can be included in the Hybrid-Pi model to determine the complete characteristics of the VCO, as seen in Figure 3.7. At resonance, the energy contributed by the differential pair will exactly balance the energy lost in the tank due to the equivalent parallel resistance. The equivalent tank impedance can be found using the half-circuit technique, and includes the effects of all devices and parasitic

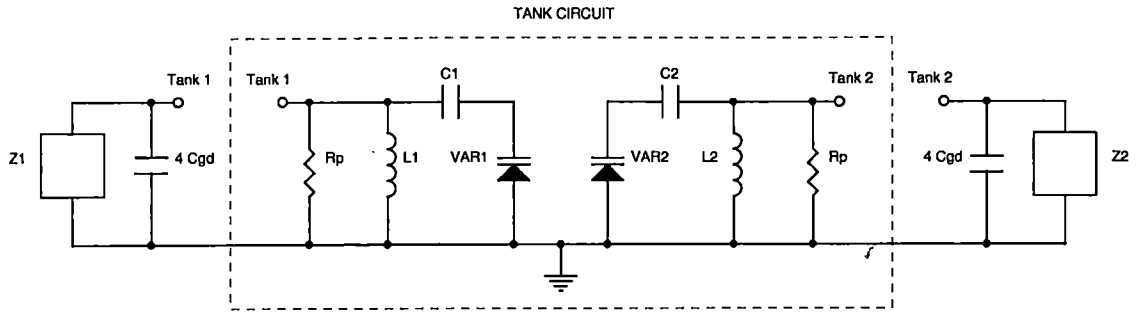


Figure 3.7: Hybrid-Pi model for complete tank circuit

effects in the tank circuit.

$$Z_{TANK} = \frac{j\omega L}{1 + j\omega L\left(\frac{1}{R_p} + \frac{1}{2r_o} - \frac{g_m}{2}\right) - \omega^2 L\left(C_{gs} + 2C_{gd} + \frac{C \cdot C_{var}}{C + C_{var}}\right)} \qquad 3.14$$

Equation 3.14 reveals that if the negative impedance of the differential transistors is sufficiently large, it will cancel the loss due to the parasitic output resistance of the transistors and the equivalent parallel resistance of the tank. In fact, because the transconductance of the differential transistors directly controls their negative impedance, the condition for oscillation can be described in terms of a minimum g_m value:

$$g_m \geq \frac{1}{r_o} + \frac{2}{R_P} \qquad 3.15$$

This is an important result, demonstrating that the proper transconductance of the differential transistors will allow the impedance of the tank to become purely reactive, achieving a theoretically infinite quality factor.

The resonant frequency of the VCO can be obtained from Equation 3.14. The negative impedance of the transistors will cancel the first-order ω term in the denominator. At the

resonant frequency, the second-order ω term in the denominator is ideally equal to 1, which will result in an infinite parallel tank impedance. Using this information, the resonant frequency is therefore:

$$\omega_0 = \frac{1}{\sqrt{L \cdot \left(C_{gs} + 2C_{gd} + \left(\frac{C \cdot C_{var}}{C + C_{var}}\right)\right)}} \quad 3.16$$

The quality factor of the circuit can also be obtained by evaluating Equation 3.14 if the transconductance is assumed to be less than the value required to completely cancel the parasitic resistances in the tank circuit.

$$g_m \leq \frac{1}{r_o} + \frac{2}{R_P} \quad 3.17$$

$$Q = \omega_0 \cdot \frac{C_{gs} + 2C_{gd} + \left(\frac{C \cdot C_{var}}{C + C_{var}}\right)}{\frac{1}{R_P} + \frac{1}{2r_o} - \frac{g_m}{2}} \quad 3.18$$

Recalling from Equation 3.9 that the equivalent parallel tank resistance, R_P, is significantly affected by the choice of capacitors for the tank circuit, it becomes apparent that these capacitors also affect the quality factor of the circuit. By maximizing the equivalent parallel tank resistance, the quality factor of the oscillator will also be maximized. This underscores the importance of selecting appropriate components for the tank circuit, balancing the requirements for operating frequency and tuning range against the need to minimize parasitic resistances.

3.3.7 Biasing and Output Buffering

The tank circuit and differential transistors are biased through a current mirror (M3 and M4 in Figure 3.2). The use of a current mirror allows the differential output voltage to be current-limited with peak-to-peak voltages, V_{max}, in the range of

$$2I_{M3}R_P \leq V_{mzx} \leq 2V_{DD} \qquad 3.19$$

This range of peak-to-peak voltages is significantly higher than what would be achievable if the differential transistors were connected directly to ground, where $V_{max} = V_{DD}$. Current limiting occurs as long as the differential transistors are operating in the saturation region [22, 23]. If the output voltage drives these transistors into the linear region, the oscillation will stop because the transistors appear as resistors in parallel with the tank circuit. This condition is referred to as voltage limiting [22, 23].

To provide the capability to drive a 50-Ω load, the VCO incorporates source-followers to implement output buffering, allowing the output signals to be isolated from the tank circuit. This approach has two advantages. First of all, external adjustments can be made to the bias points of the differential transistor current mirror, as well as the output buffer current mirror, allowing the operation of the VCO to be optimized with respect to its current-limited and voltage-limited states. Secondly, the quality factor of the tank circuit is independent of the load on the output. Because the input impedance of the gate of a MOS device is quite large, there is no substantial reduction in the tank's equivalent parallel resistance. In fact, low-impedance loads connected directly to the tank output will greatly reduce the equivalent parallel resistance (and thus the Q of the tank circuit,

resulting in increased phase noise), and could potentially prevent the circuit from oscillating altogether [24].

3.3.8 Noise Effects and Design Tradeoffs

Several noise sources contribute to the overall output noise of the VCO, which is generally quantified in terms of phase noise. These include components in the tank circuit, the differential transistors, the output buffers, and the current mirrors. An ideal negative-g_m oscillator, with noise effects due only to resistance in the tank, has an output noise spectrum described by the following equation, where k is Boltzmann's constant and T is the temperature in Kelvin [18]:

$$\frac{v^2}{\Delta f} = 4kTR_P\left(\frac{\omega_0}{2Q\Delta\omega}\right) \qquad 3.20$$

Inspection of this equation shows that the noise spectral density is not independent of frequency, due to the filtering of the tank circuit. This equation accounts for variations in both amplitude and phase of the output signal. Because all realizable circuits have some means of amplitude limiting, the amplitude variations are attenuated, leaving the phase variations as the dominant result of the tank noise. The equipartition theory of thermodynamics allows the assumption that without amplitude limiting, the tank noise energy splits equally between amplitude variations and phase variations [18]. Thus when amplitude limiting is applied, the total output noise is half of that expressed by Equation 3.20 [18]. By normalizing the output noise spectrum to the carrier power, a more

convenient expression for phase noise is obtained, where P_{sig} is the output carrier power

$$P(\Delta\omega) = 10 \cdot \log\left[\frac{2kT}{P_{sig}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \quad 3.21$$

The units of Equation 3.21 are dBc/Hz, specified at a given frequency offset from the carrier. Inspection of this equation shows that the phase noise will improve if the carrier power is increased, or if the quality factor is increased. The equation also demonstrates that the noise falls off in proportion to the inverse square of the frequency offset, yielding noise spectrums such as those presented in Figure 2.5.

While Equation 3.21 adequately describes the noise characteristics for an ideal oscillator, additional consideration must be given to the noise contributed by the active devices in the design, such as the differential transistors and output buffering. These additional effects are accounted for in Leeson's equation for phase noise, shown in Figure 3.8. The figure compares Leeson's model to the idealized model of Equation 3.21. Regions of specific interest are labeled A, B, and C in Figure 3.8. Leeson's model includes a scale factor F to account for additional noise in the $1/(\Delta\omega)^2$ region (region B), a unity addition factor to account for the 'noise floor' (region C), and an additional scale factor to account for additional noise at frequency offsets very close to the carrier (region A) [18]. Leeson's equation for phase noise is:

$$P(\Delta\omega) = 10 \cdot \log\left\{\frac{2FkT}{P_{sig}} \cdot \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \quad 3.22$$

The various scale factors associated with Leeson's model are not always related to a physical device characteristic, and thus are generally treated as curve-fitting parameters.

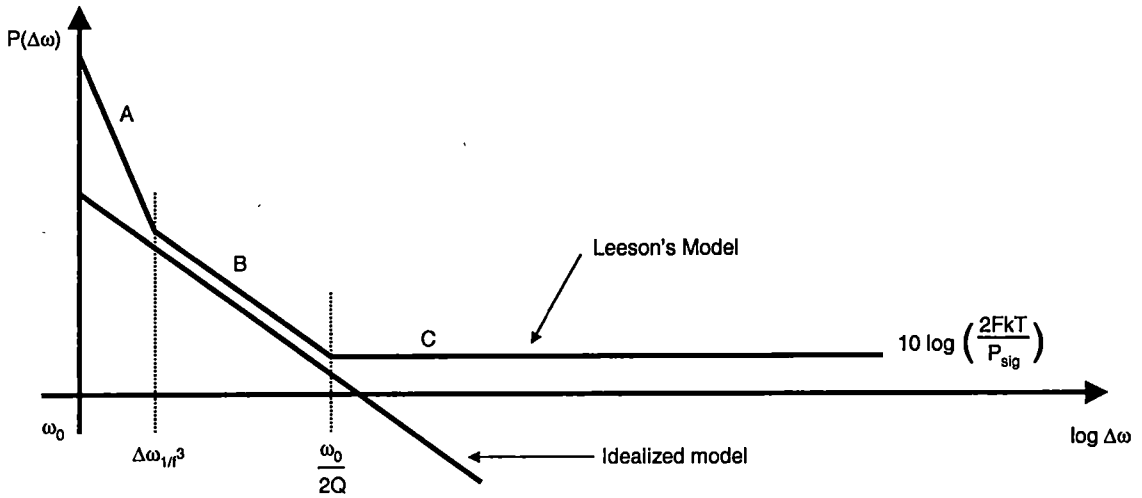


Figure 3.8: Comparison of phase noise models
Adapted from: Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.

Other, more advanced models of phase noise, such as the Hajimiri model, take into account additional factors such as non-linearity and time-variance, both of which affect the phase noise of a real oscillator [10].

Leeson's model shows that noise generated by active devices in the circuit will cause phase noise in the output signal. For instance, noise associated with the differential transistor current mirror will be modulated to the resonant frequency of the oscillator. Effects such as this are observed in region A of Figure 3.8. Noise associated with the output buffers will add to the overall noise floor of the oscillator, as seen in region C. The additional phase noise resulting from these components presents an interesting design tradeoff. The current mirror allows an increase in the resonant tank peak-to-peak voltage, which helps to reduce phase noise. Likewise, the output buffers are required to prevent the tank circuit Q from being severely degraded. Therefore, the design must balance the

benefits of these additional devices against their potential effect on the output phase noise.

3.4 High Temperature Considerations

The VCO is required to operate over a temperature range from room temperature (25 ºC) up to 200 ºC. This wide temperature range raises several important issues which must be addressed in the design of the VCO. First of all, the gain (Hz/volt) of the VCO should stay constant or nearly constant over the entire temperature range. This will ensure that the stability of the PLL will not be affected by a change in the VCO. Secondly, the passive components of the VCO should have minimal deviation over temperature [25]. This will maintain the Q of the tank, as well as keep the operating frequency constant for a fixed control voltage. Finally, the transistors used must continue to operate at high temperature, without compromising the output voltage swing requirements necessary to drive the rest of the PLL.

The majority of the design of the VCO was done using room-temperature parameters, allowing the design to be optimized with respect to its operating characteristics. After a suitable set of component values and transistor sizes was determined, the design was simulated over temperature using HSPICE [26] as discussed in Section 3.6. Because the simulator uses complex thermal models in its calculations, a relatively good prediction can be made about the operation of the circuit at a given temperature. In fact, the results of initial temperature simulations prompted a few adjustments, such as the sizing of the output buffer transistors, to optimize the performance of the VCO over the entire range of operating temperatures.

3.5 Preliminary Design

The resonant tank components of the VCO were initially determined using hand calculations based on the formulas presented in Section 3.3.6. Because the varactor diodes control the tuning range of the VCO, the selection of an appropriate device was critical to achieving the 100 MHz tuning range. Secondary considerations involved the inductors and coupling capacitors, which predominantly control the center frequency of the VCO. Using a spreadsheet analysis, suitable component values were determined, and are listed in Table 3.2.

Approximate bias points for the circuit were obtained by first determining the g_m value necessary to achieve oscillation in the resonant tank. This value was calculated using Equation 3.15 with a calculated equivalent parallel tank resistance of 546 ohms at 300 MHz. The minimum g_m required for oscillation was calculated to be 3.68 mS. To establish this bias condition in the differential transistor pair, the bias current for each device was calculated to be approximately 500 uA. The transistors of the tank and the associated current mirror were sized to achieve the appropriate bias. To isolate the VCO output load from the resonant tank and provide increased output drive capability, the output buffer transistors were biased at a quiescent current of approximately 15 mA. The g_m of the source-following transistors was approximately 35 mS. Current mirrors

Table 3.2: VCO tank circuit component values

Component	Value
Inductor	18 nH
Coupling Capacitor	22 pF
Varactor	9 - 28 pF

associated with the output buffers were sized to handle the current requirements of the output load. Pre-layout simulations were used to refine the initial design.

3.6 Simulation and Layout Techniques

After the initial design of the VCO was completed, the circuit was simulated using HSPICE to evaluate its performance over the entire range of operating temperatures. The simulation accounted for anticipated parasitic effects to more accurately model the real-world circuit behavior. A subcircuit model was generated for the varactor diodes, according to the manufacturer's suggested parameters, as discussed in Section 3.3.2. The complete HSPICE file used for pre-layout simulations is included in Appendix A, and includes all device sizes. Low-threshold devices, available in the fabrication process, were used to improve the voltage range of the output. Results of the pre-layout simulation showed that the VCO would perform acceptably over the required operating parameters, including frequency range, output drive, and temperature. In addition, several preliminary design calculations were validated, including the g_m value required to achieve oscillation (3.8 mS simulated as compared to 3.68 mS calculated).

Figure 3.9 shows the results of a pre-layout simulation of the VCO over temperature. The blue trace reflects operation at 25 ºC, while the red trace represents 200 ºC. The control voltage in this simulation is 3.0 V, resulting in an oscillation frequency of approximately 357 MHz at 25 ºC. Several effects of temperature are immediately obvious from the simulation, including a drop in output drive capability, as well as an increase in operating frequency by 25% to approximately 450 MHz. Both of these effects were anticipated, but do not pose a significant problem to the operation of the PLL. The VCO output is still

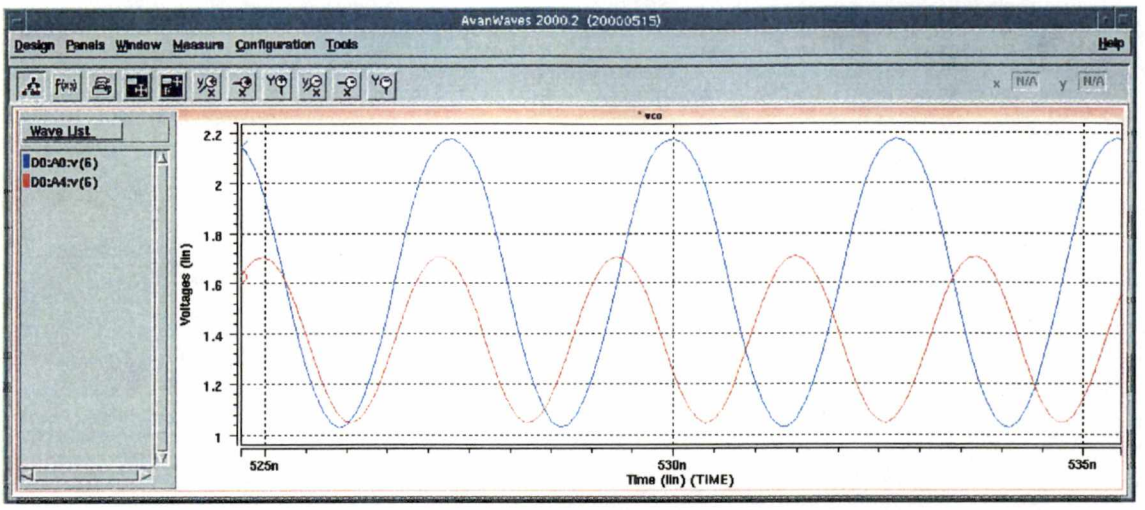


Figure 3.9: VCO pre-layout simulation
Blue: 25 ºC output, Red: 200 ºC output
Source file: Appendix A.1. Vdd = 3.3V, Vcontrol = 3.0V

capable of driving the 50-ohm load, and the tuning range of the VCO is sufficient to allow the PLL to correct for the shift in frequency. In addition, the simulation shows virtually no distortion of the output waveform at either of the two temperature extremes. This is a very valuable result, since distortion of the waveform would introduce additional phase noise in the PLL output. Further simulations revealed the tuning range of the VCO, shown in Table 3.3.

Layout of the VCO was done by hand using the MAGIC software package [27]. A 'foundry rules' technology file for the Peregrine technology was used. In this technology file, the minimum incremental size was 0.1 um, commonly referred to as 'lambda' (λ). However, the minimum gate length in the process was 0.5 um, or 5λ. This contrasts to

Table 3.3: VCO pre-layout simulation results

Parameter	25 ºC	200 ºC
Min frequency	240 MHz	290 MHz
Max frequency	357 MHz	440 MHz

typical scalable-CMOS design rules, where the minimum gate length is 2λ. Foundry rules provide the designer with a higher degree of precision, while SCMOS designs have the advantage of being easily translated and scaled between various processes.

In the layout of the VCO, several techniques were used to minimize parasitics and the potential effects of thermal gradients and processing variations. First of all, each of the transistors in the VCO was divided into several smaller transistors which could be placed in parallel. These smaller transistors were laid out in an interdigitated format, allowing the source and drain terminals between adjacent devices to be shared. This approach helped to minimize parasitic capacitance within each transistor. Also, the total width of each transistor was realized in a much more compact physical area, helping to minimize the effects of thermal gradients and processing variations. Another layout technique involved the arrangement of the transistors relative to each other on the chip. This approach is commonly referred to as 'common-centroid' layout. Most important in this respect was the positioning of the tank transistors, M1 and M2. To achieve the lowest possible phase noise, these devices must be precisely matched and symmetrically connected to the remaining devices in the VCO, as well as to the pad frame. To facilitate these connections, the transistors were laid out as mirror images, and positioned between the corresponding buffer devices M5 and M6, as seen in Figure 3.10, where M6 is in the upper left corner and M1 is in the top center of the layout. This approach allowed the shortest possible connections between the critical signal path transistors, thus minimizing parasitics which could contribute to the phase noise of the VCO. An added benefit was the simplification of connections to the bias transistors and current mirrors. Because of the symmetrical approach to the VCO layout, parasitic effects were minimized

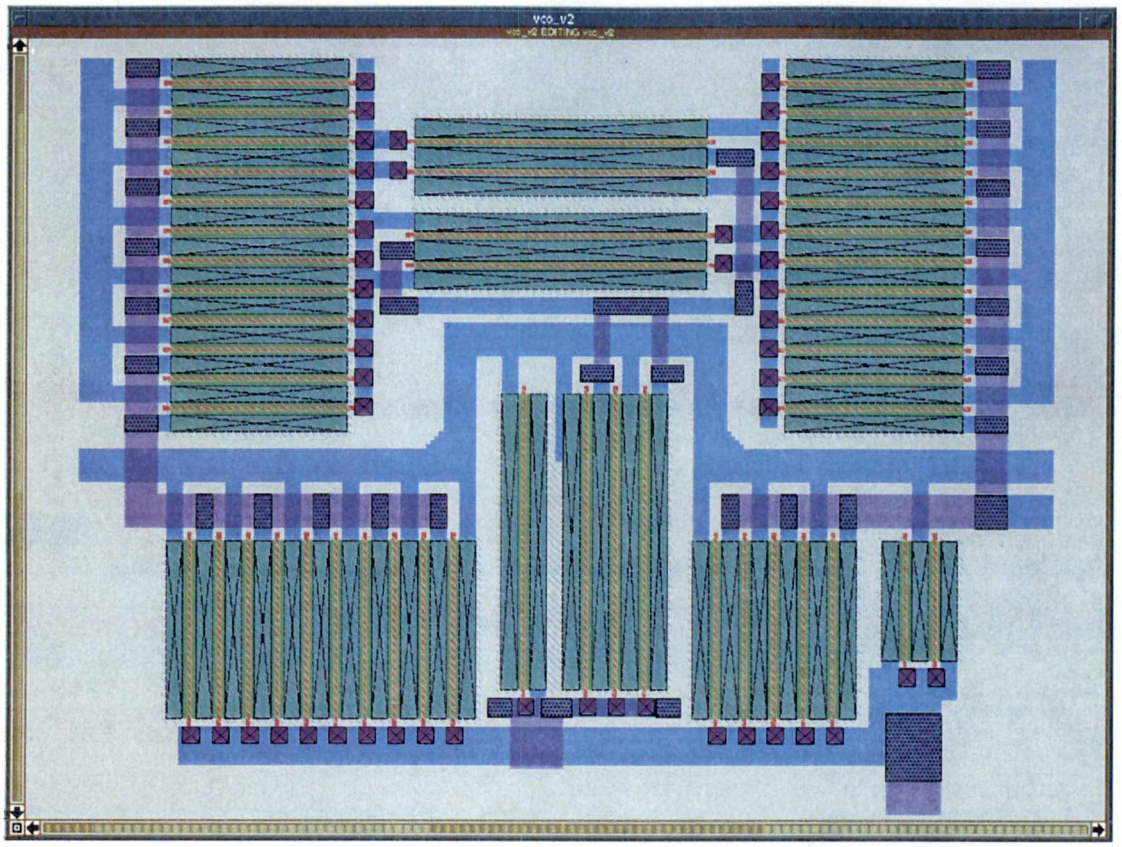


Figure 3.10: Screen shot of VCO layout

and the sensitivity to thermal gradients and processing variations was significantly reduced.

After completing the layout, the design was exported from MAGIC and run through the *ext2spice* extraction program. This software analyzes the MAGIC layout and derives the appropriate parameters for device geometry and relevant parasitics. A new HSPICE input file is generated which more accurately represents the physical structure of the circuit. This file was used to simulate the VCO over the complete range of operating parameters, including frequency range, output drive, and temperature. A sample of this file is included in Appendix B.

Figure 3.11 shows the results of a post-layout simulation of the VCO over temperature. The blue trace reflects operation at 25 ºC, while the red trace represents 200 ºC. The control voltage in the simulation is 3.0 V, resulting in an oscillation frequency of approximately 370 MHz at 25 ºC. As with the pre-layout simulation, the effects of temperature are fairly obvious, including a drop in output drive capability, as well as an increase in operating frequency by 23% approximately to 455 MHz. The post-layout simulation does show a slightly different amount of degradation due to temperature. This is expected, because the layout parameter extraction process produces a more accurate simulation than an idealized netlist simulation. As before, the effects of temperature can be compensated by the remaining components in the PLL. In addition, the output signal is distortion-free, preventing the introduction of additional phase noise into the PLL.

Overall, both the pre-layout and post-layout simulations showed that the VCO design performed acceptably over the complete range of operating parameters, including output

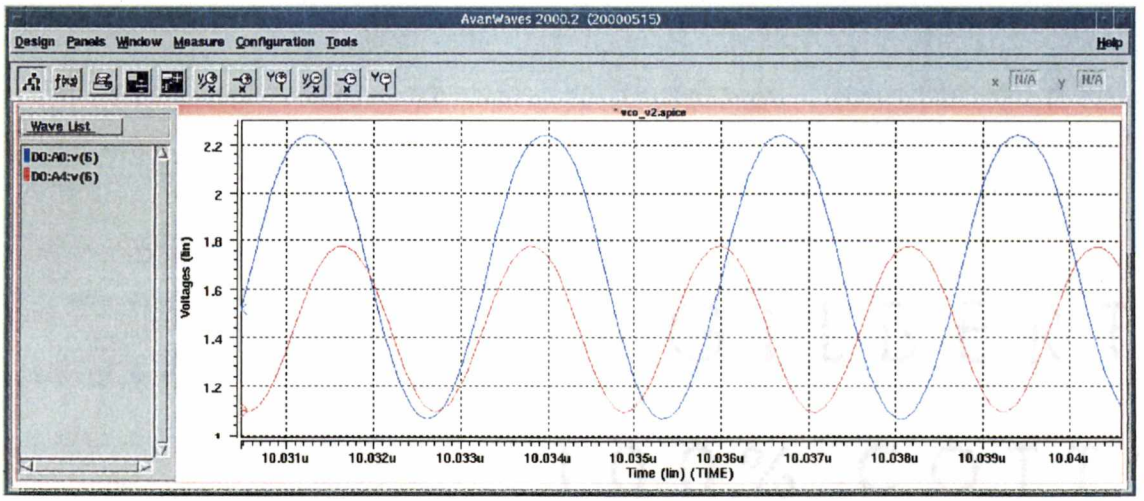


Figure 3.11: VCO post-layout simulation
Blue: 25 ºC output, Red: 200 ºC output
Source file: Appendix B.1. Vdd = 3.3V, Vcontrol = 3.0V

drive capability, frequency range, and temperature. A summary of the simulated results is presented in Table 3.4.

The design also incorporated a degree of flexibility by allowing the VCO bias points to be externally adjusted. This capability becomes increasingly important at higher temperatures, when bias points can shift due to physical changes in other circuit components. Additional simulations of the VCO were performed at various temperatures to optimize the bias settings. These optimizations helped to reduce the deviations of operating frequency and output drive over temperature, and underscored the necessity of optimizing the bias settings again during laboratory tests on the prototype oscillator.

Table 3.4: VCO post-layout simulation results

Parameter	**25 ºC**	**200 ºC**
Min frequency	230 MHz	295 MHz
Max frequency	370 MHz	455 MHz
Peak-to-peak output voltage	1.2 V	0.9 V

Chapter 4

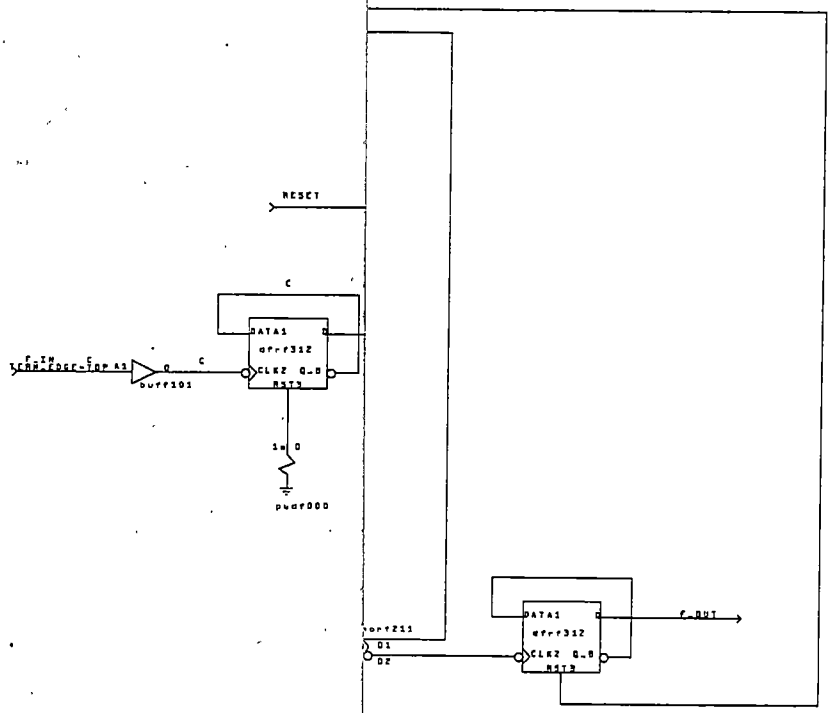
Programmable Frequency Divider Design and Analysis

4.1 Specifications

The frequency divider accepts a sinusoidal input with a frequency of 260, 280, 300, 320, or 340 MHz and generates a logic-level output with a frequency of 1 MHz. The division ratio is selectable, and the duty cycle of the output must be 50% to prevent the introduction of additional phase noise into the PLL.

4.2 Architecture

For this divider, a three-stage digital architecture is used. The input frequency drives a single flip-flop connected as a divide-by-2 circuit. The output of this circuit is then half the frequency of the original input, and is a logic-level digital signal instead of a sinusoid. This signal becomes the clock for a 7-bit synchronous counter, with the output of each bit compared to a corresponding programmed bit for a given divide ratio. When the counter reaches the desired value, a final divide-by-2 flip-flop is clocked, and the counter is reset. The output of the divider is the output of the final flip-flop. A logic-level schematic of the divider circuit is presented in Figure 4.1.


RESET
C
DATA1
dffrf312
CLK2 Q_B
RST1
f_IN
TCAR_FDEF-TOP A1
C
buff101
1
0
pwdf000
orrf211
D1
D2
DATA1
dffrf312
CLK2 Q_B
RST1
f_OUT

-FLATTEN -R4

4.2.1 Front End Design

The sinusoidal input is converted to a logic-level signal using the front-end divide-by-2 flip-flop to increase the stability of the entire block and reduce any additional phase noise contributions. This reduces the need for flip-flops in the counter to be precisely matched, since the transition times between low and high states are significantly faster and more predictable for logic level 'step' inputs than for sinusoidal inputs.

The clock signal for the synchronous counter is also half as fast; therefore, the propagation delay between sequential bits in the counter becomes less significant. The phase noise of the divider block is also comparatively reduced, because the duty cycle of the synchronous counter clock becomes independent of the duty cycle of the sinusoidal input.

4.2.2 Programmability Considerations

The specification for supporting multiple input frequencies while producing a common output frequency requires the divider circuit to be programmable. The necessary programming information could be passed to the divider in several ways, such as a serial input, parallel input, or an encoder. In this case, a parallel programming architecture is used, primarily because of its simplicity and ease of implementation. Other methods such as serial programming introduce additional logic components and add to the overall complexity of the system.

To support the required input frequency range of 250 to 350 MHz and generate a 1 MHz output frequency, a 9-bit divisor is required, yielding a maximum division ratio d_{max} of:

$$d_{max} = 2^9 = 512 \qquad 4.1$$

Due to the design of the divider block, two of the nine bits are essentially 'hard-wired', in that there is a forced divide-by-2 at the input, and a forced divide-by-2 at the output. Consequentially, the divider has a minimum division increment d_{min} of:

$$d_{min} = 2^2 = 4 \qquad 4.2$$

For this application, the minimum increment limitation is transparent to the user, since all five channel frequencies mentioned in Section 4.1 are evenly divisible by a multiple of four to obtain a 1 MHz output signal. The allowable division ratios are described by the following formula:

$$d = (n+1) \cdot d_{min} \qquad 0 \leq n \leq 127 \qquad 4.3$$

This approach leaves 7 bits available for user programming, which is accomplished using exclusive nor (XNOR) gates to compare each bit in the synchronous counter to a value set by the user. If each bit of the counter output matches the programmed value, the output flip-flop is clocked and the counter is reset. The output flip-flop is therefore clocked at 2 MHz, yielding an output of 1 MHz with a 50% duty cycle. As the frequency of the divider input changes, the frequency of the divider output will be proportionally changed. At the input to the phase-frequency detector block in the PLL, this shift in frequencies appears as a phase shift between the 1 MHz reference signal and the divider output.

4.3 High Temperature Considerations

As with the other components in the PLL, the programmable frequency divider must maintain consistent operation over a wide range of ambient temperature. Because the divider block is composed entirely of digital standard cells, no special temperature criteria were used in the initial design of the divider. This is because the performance of digital blocks is, in general, not as critically dependent on temperature as are many analog circuits. Almost all analog circuits require precision biasing to achieve the desired operation. Digital circuits, on the other hand, are relatively independent of biasing, since most transistors are biased at either the positive or negative rail voltage, both of which are ideally independent of temperature. Bias points for analog transistors are set by other components in the circuit, and are therefore much more sensitive to temperature variations, potentially impacting the performance of the entire circuit.

To validate this initial assumption, several simulations of the divider were performed using HSPICE on a Magic circuit extraction, which was generated after making the manual routing adjustments discussed in Section 4.4. This allowed the circuit to be simulated at the transistor level, using actual extracted process parameters, instead of the logic-level simulation provided in PowerView. To verify the divider operation, the HSPICE simulations used a transient analysis with a sinusoidal input, with amplitude characteristics equivalent to the output signal of the VCO. A temperature sweep was included which forced simulation over the required operating range of 25 to 200 ºC. The results of the simulation showed that the divider continued to perform acceptably over the entire temperature range, using any of the five input frequencies. This supported the

design assumption that deviations in operating temperature do not significantly affect the operation of the divider.

4.4 Simulation, Synthesis and Optimization

The programmable frequency divider was synthesized using the ViewDraw and ViewSim applications in the PowerView [28] tool set. A schematic was created in ViewDraw using components from the ITD/AuE standard cell library [29]. This approach significantly reduced the design time, since logic-level simulations could be immediately performed to analyze the functional accuracy of various implementations. In addition, the automatic placement and routing capabilities of the PowerView tool set allowed an optimized, compact Magic layout to be generated with minimal user intervention.

After entering the schematic for the divider circuit, several simulations were performed using ViewSim to verify each of the five required division ratios. Based on these simulations, a few areas of the circuit were redesigned to reduce latency and ensure an accurate division ratio. Figure 4.2 shows the results of a pre-layout ViewSim simulation using several division ratios. The timing information in the simulation output was used to calculate the precise division ratio for the circuit. Overall, the circuit simulation produced the expected output, and showed that the desired functions could be performed.

The counter programming ratios can be determined mathematically by converting the desired ratio to binary, subtracting 1, and then dropping the two least-significant bits. The remaining seven bits are used to program the divider. Table 4.1 presents a list of division ratios and their corresponding programming codes.

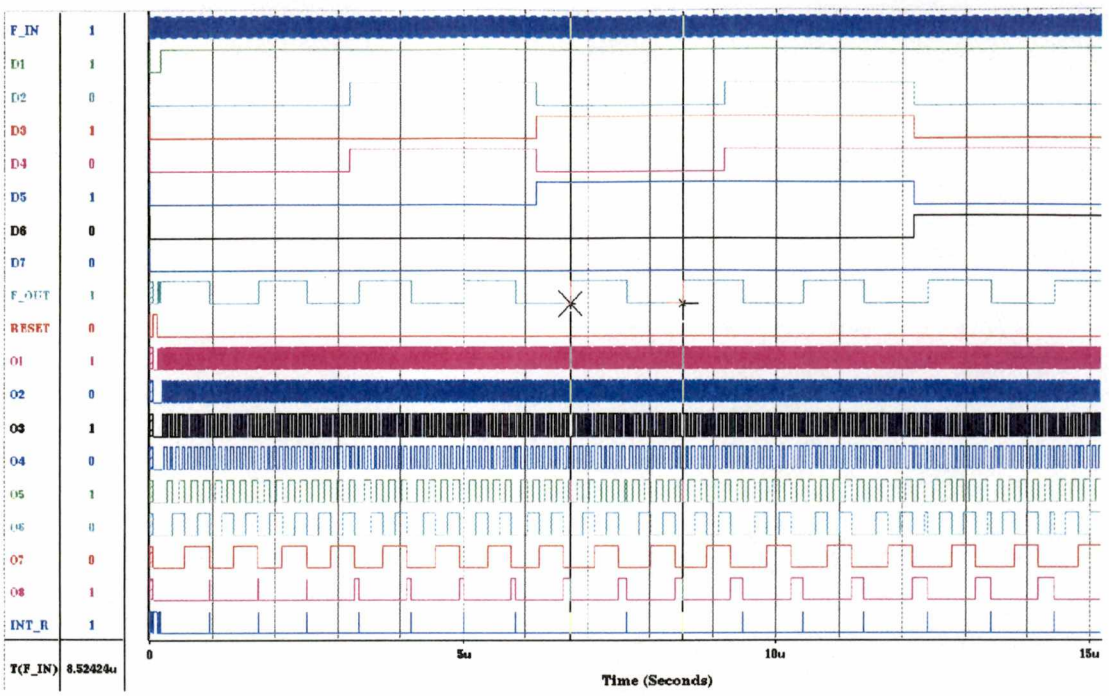


Figure 4.2: Pre-layout simulation of programmable divider
Source files: Appendix A.2, A.3

Table 4.1: Divider programming codes

Ratio	D6	D5	D4	D6	D2	D1	D0
260	1	0	0	0	0	0	1
280	1	0	0	0	1	1	0
300	1	0	0	1	0	1	0
320	1	0	1	0	0	0	0
340	1	0	1	0	1	0	1
32	0	0	0	0	1	1	1
16	0	0	0	0	0	1	1

The Lager toolset was used to create a Magic layout from the PowerView schematic. Using the ITD/AuE standard-cell library, the circuit was first extracted into a scalable CMOS (SCMOS) technology Magic cell. To scale and translate the SCMOS cell into a Peregrine 0.5um technology cell, the design was exported to a circuit interchange format (CIF) file, which completely specifies the dimensions of every layer in the layout. MAGIC provides the capability to read CIF files, which become formatted to the current technology file when they are read in. Thus, by exporting using the SCMOS tech file, then importing using the Peregrine tech file, the design was translated and scaled automatically. Items such as gate lengths were converted automatically from 2λ in the SCMOS technology to 5λ in the Peregrine technology. Although somewhat tedious, this process was necessary because there were no pre-existing standard-cell libraries in the Peregrine technology database.

Once the divider was converted to the Peregrine technology, a few manual routing optimizations were performed on the layout. Due to the constraints of the placement and routing software, a few sections of the circuit had areas where the routing between cells could obviously be improved. The most notable of these was the input to the entire divider. Manual editing allowed a shorter and more efficient connection to the input. A few other minor adjustments were made to provide shorter signal paths and fewer metal-level transitions. Overall, the automatic placement and routing software provided a very compact layout, which required very few manual adjustments to achieve an acceptable result. Figure 4.3 shows a screen shot of the divider circuit layout.

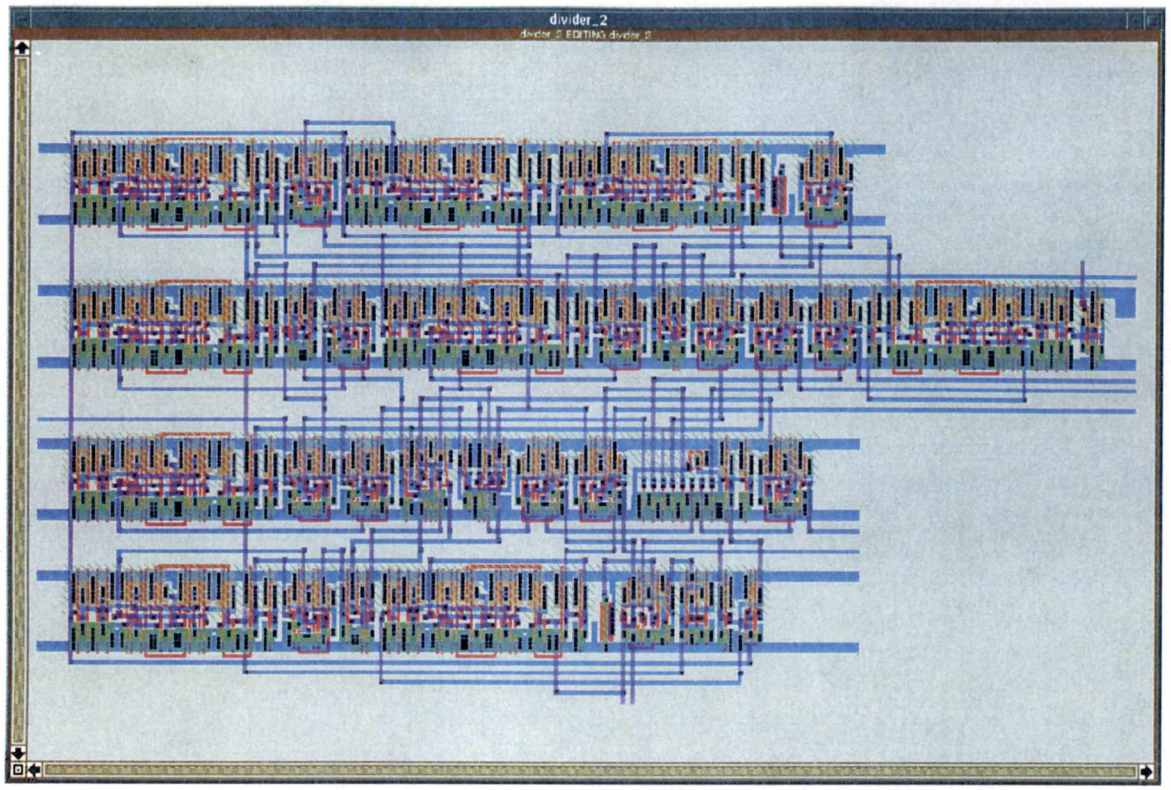


Figure 4.3: Screen shot of programmable divider layout

After completing the optimizations mentioned above, the layout was exported from MAGIC and run through the *ext2spice* program to extract relevant device geometry and parasitic information. The complete divider circuit was then simulated using HSPICE with a sinusoidal input corresponding to the output drive of the VCO. Several division ratios were analyzed, and the simulation was also configured to run at 25 ºC and 200 ºC to evaluate the performance over temperature. A sample HSPICE simulation file is included in Appendix B.

Results of the post-layout simulation show that the divider performs acceptably over the complete temperature range and all required division ratios. The output waveforms from a post-layout simulation using a 300 MHz input and 1/300 ratio, at temperatures of 25 ºC

and 200 ºC are shown in Figure 4.4. There is no appreciable difference in the performance of the divider between the two temperatures. A closer inspection of the results, using Figures 4.5 and 4.6, shows that the propagation delay through the divider from input to output at 200 ºC increases by just over 2 ns. However, because this shift affects both the rising and falling edges, it does not affect the frequency of the output signal, which is the most critical output requirement. The amount of increase in propagation delay remains steady across the entire division range. Figures 4.7 and 4.8 show operation at 260 MHz and 340 MHz, and demonstrate the consistent increase in propagation delay over the full division range.

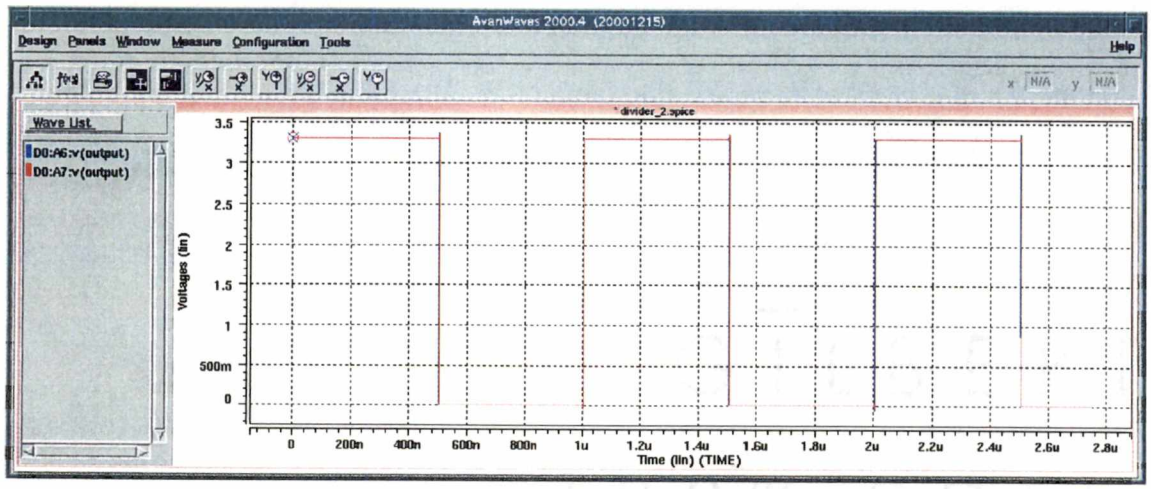


Figure 4.4: Post-layout simulation of divider at 300 MHz
Blue: 25 ºC output, Red: 200 ºC output
Source file: Appendix B.2

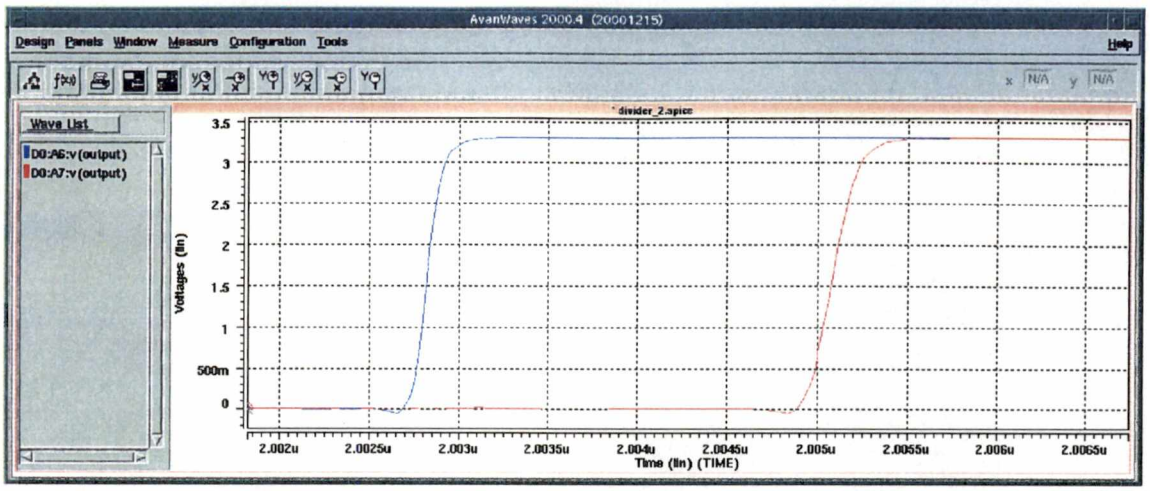


Figure 4.5: Post-layout simulation of divider at 300 MHz - rising edge
Blue: 25 ºC output signal, Red: 200 ºC output
Source file: Appendix B.2

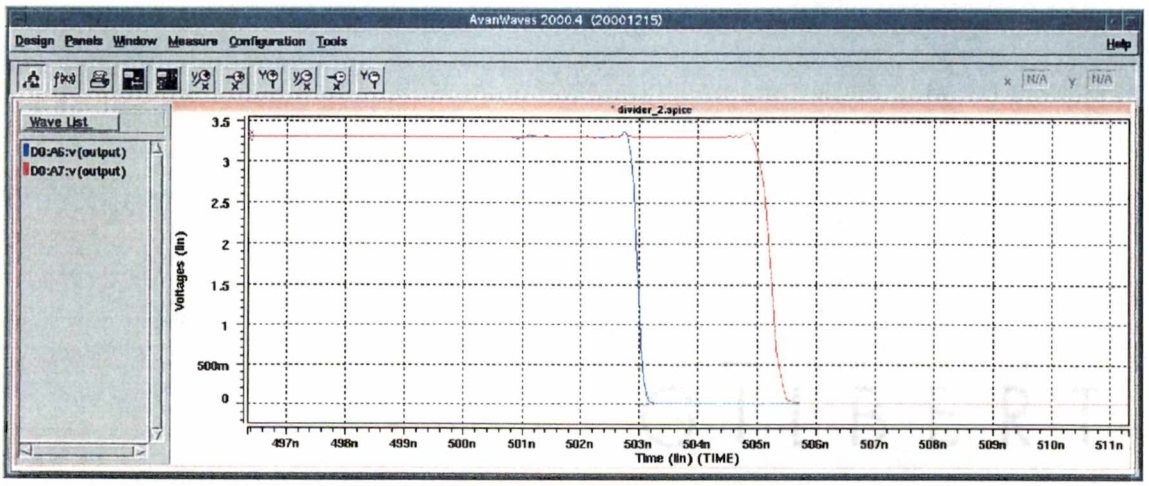


Figure 4.6: Post-layout simulation of divider at 300 MHz - falling edge
Blue: 25 ºC output, Red: 200 ºC output
Source file: Appendix B.2

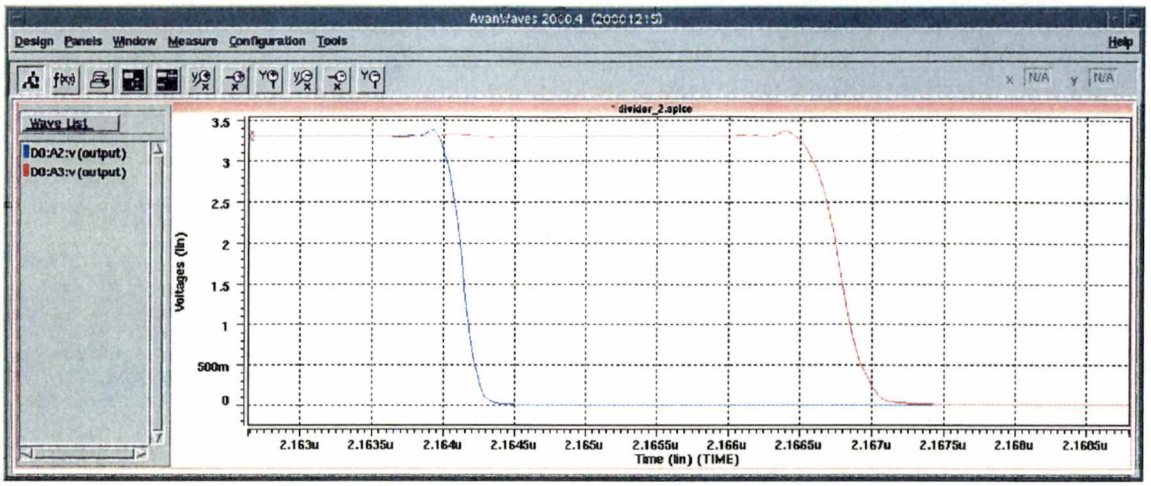


Figure 4.7: Post-layout simulation of divider at 260 MHz - falling edge
Blue: 25 ºC output, Red: 200 ºC output
Source file: Appendix B.2

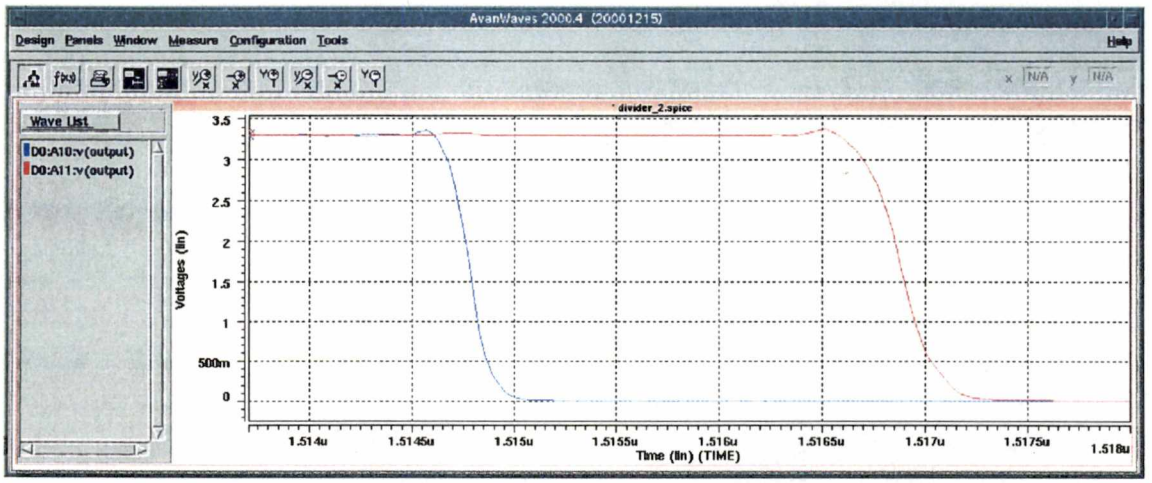


Figure 4.8: Post-layout simulation of divider at 340 MHz - falling edge
Blue: 25 ºC output, Red: 200 ºC output
Source file: Appendix B.2

Overall, both the pre-layout and post-layout simulations showed that the programmable frequency divider performed acceptably over the full range of operating parameters, including all division ratios, output frequency accuracy, and temperature. The circuit remained stable and exhibited a small but consistent increase in propagation delay at higher temperatures. The division accuracy was verified and remained stable over temperature regardless of division ratio. In addition, the duty cycle of the output remained steady at 50%. This fact is critical to prevent additional phase noise from being introduced in the closed-loop PLL output signal. A summary of the divider simulation results is presented in Table 4.2.

Table 4.2: Divider simulation results

Parameter	**25 ºC**	**200 ºC**
Output drive	rail-to-rail	rail-to-rail
Average rising edge slew rate	15 V/ns	11.25 V/ns
Average falling edge slew rate	12.5 V/ns	6.25 V/ns
Increased propagation delay	-	2.1 ns

Chapter 5

Prototype Testing and Evaluation

5.1 Chip Layout Techniques

The MAGIC software package was used to arrange the VCO, divider, and PFD / charge pump circuits on a common chip for fabrication using MOSIS. Each module was imported as a sub-block into an empty pad frame, allowing manual placement and routing of I/O connections to the pads. Separate power and ground busses were provided to modules such as the VCO, frequency divider, and charge pump, to allow independent operation and isolation from other devices on the chip. The pad frame included protection diodes for overvoltage and ESD protection. A screen shot of the complete chip layout is presented in Figure 5.1.

The various blocks of the PLL were arranged on the chip according to the external connections required by each block. By evaluating the anticipated board-level connections between certain components to optimize placement of the blocks on the chip, this approach allowed I/O connections within the chip to remain at a minimum length, while reducing the trace lengths required on the test circuit board. External noise and parasitic effects are also minimized through this technique.

The completed chip layout was compiled to generate an extracted circuit file containing additional information about the parasitics of the chip. This circuit file was re-simulated using HSPICE to verify the operation of each block. In all cases, the pad frame did not

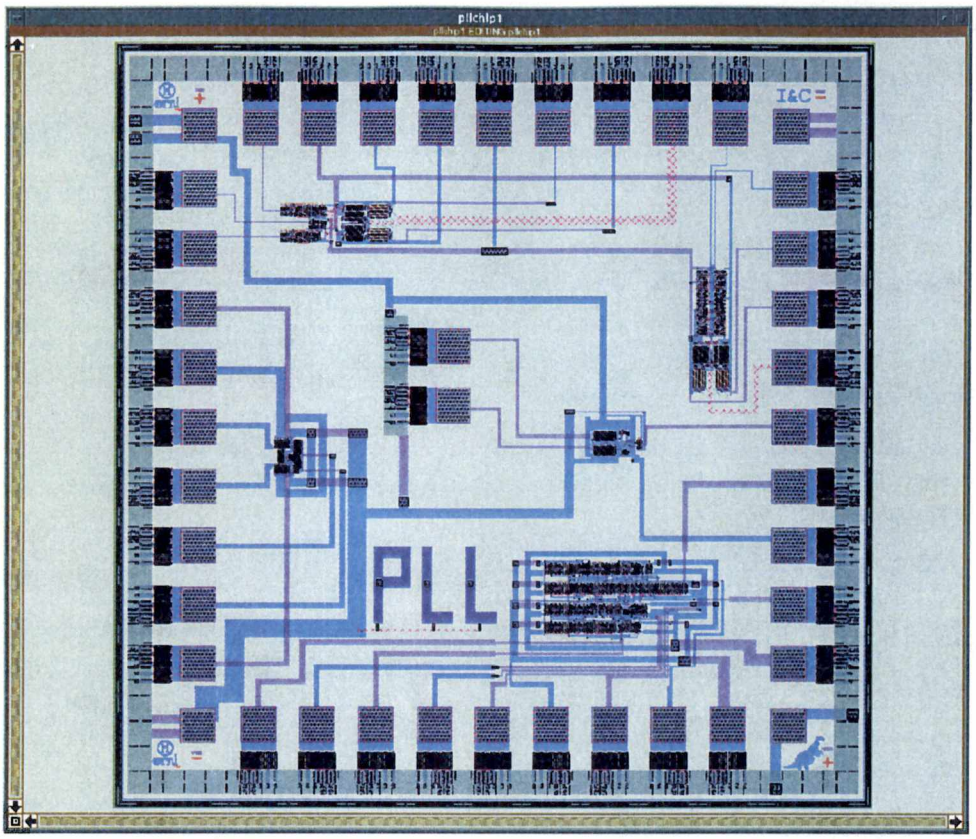


Figure 5.1: Screen shot of complete chip layout

have a significant effect on the performance of any component of the PLL. As a final precaution, a complete design-rule check was performed by exporting the layout to a CIF file, then re-importing it and evaluating the results. This approach allowed MAGIC design macros to be converted to their foundry equivalent implementations. A few minor design rule violations were discovered and easily corrected, and the design was then submitted to MOSIS for fabrication under the design name 'PLLCHIP1'.

5.2 Chip Fabrication

The PLLCHIP1 design was fabricated through MOSIS using the Peregrine Semiconductor 0.5um silicon-on-sapphire process. This is one of several cutting-edge

processes that take advantage of the unique electrical properties of silicon deposited on an insulating substrate, also referred to as silicon-on-insulator (SOI).

One distinct advantage of SOI processes is the ability to electrically isolate various sections of a chip. In traditional silicon processes, the substrate is shared by all the devices on the chip (see Figure 5.2). This can impose significant limitations on the arrangement of blocks on a chip, especially in mixed-signal applications. Digital blocks can inject noise into the substrate, which can then adversely affect analog blocks on the same chip. Although some techniques such as substrate 'plugging' and metal ground rings can reduce the noise effects of digital blocks in traditional processes, the substrates of the analog blocks and digital blocks cannot be physically separated and thus some noise effects will always be present.

SOI processes do not suffer from these limitations, because they allow separate silicon substrates to be implanted into a larger insulating substrate. The placement of usable silicon can be controlled by the circuit designer. This allows analog and digital blocks to

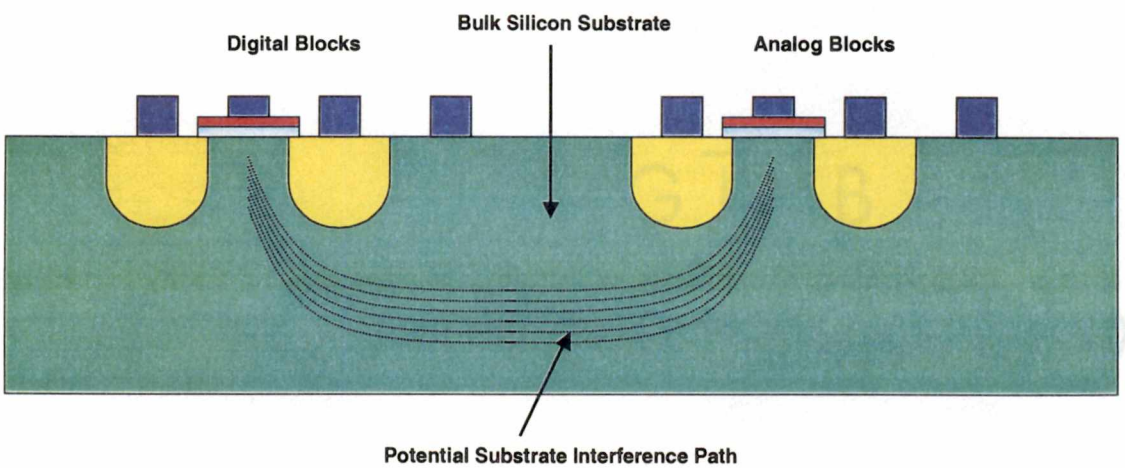


Figure 5.2: Traditional bulk silicon process cross-section

be arranged in close proximity to each other, and eliminates the need for additional precautions such as ground rings and plugging (see Figure 5.3). Because the silicon substrates are electrically isolated, noise effects due to the digital blocks are significantly reduced. In mixed-signal designs, it is possible to achieve a tighter layout using an SOI process instead of a traditional process, since separation of the analog and digital portions becomes less of an issue.

SOS technology also has some distinct high-temperature advantages over traditional bulk CMOS processes. Leakage currents in SOS are substantially smaller, and do not flow into the substrate as in bulk CMOS. This fact also implies that the output transconductance of SOS devices is not degraded by the leakage currents. At high temperatures, the effects of leakage currents in bulk CMOS are more pronounced, and can contribute to latch-up and instability. SOS circuits are capable of running at much higher temperatures before encountering these problems.

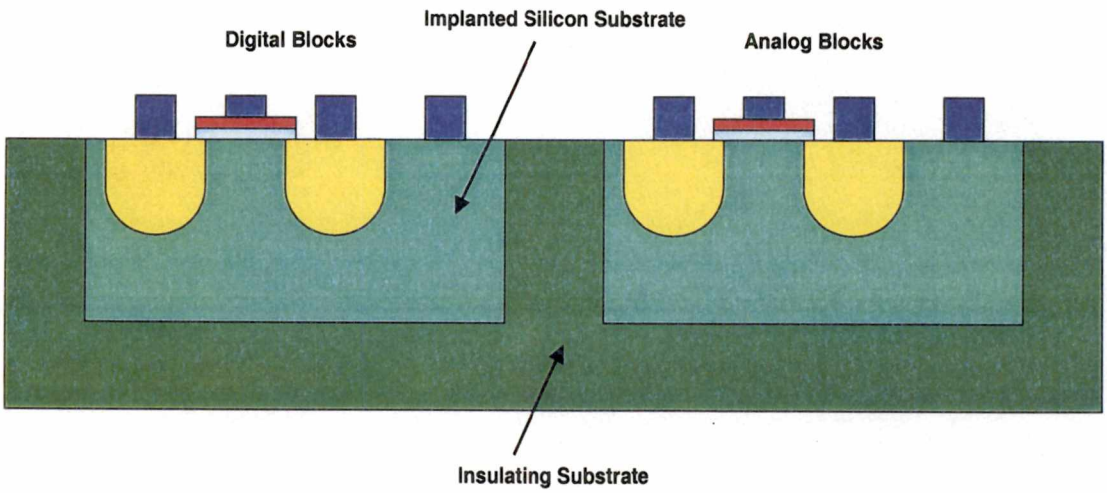


Figure 5.3: Typical silicon-on-insulator (SOI) cross-section

Fabrication of the PLLCHIP1 design took approximately 5 months. After the run was completed and the chips were received, a visual inspection was performed to verify the layout. A high-power optical microscope was used to photograph the chip and several of the major blocks. Figure 5.4 shows the entire die, corresponding to the complete chip layout in Figure 5.1. The voltage-controlled oscillator is shown in Figure 5.5, and the programmable frequency divider is presented in Figure 5.6. These photographs correspond with the layouts presented in Chapter 3 and Chapter 4.

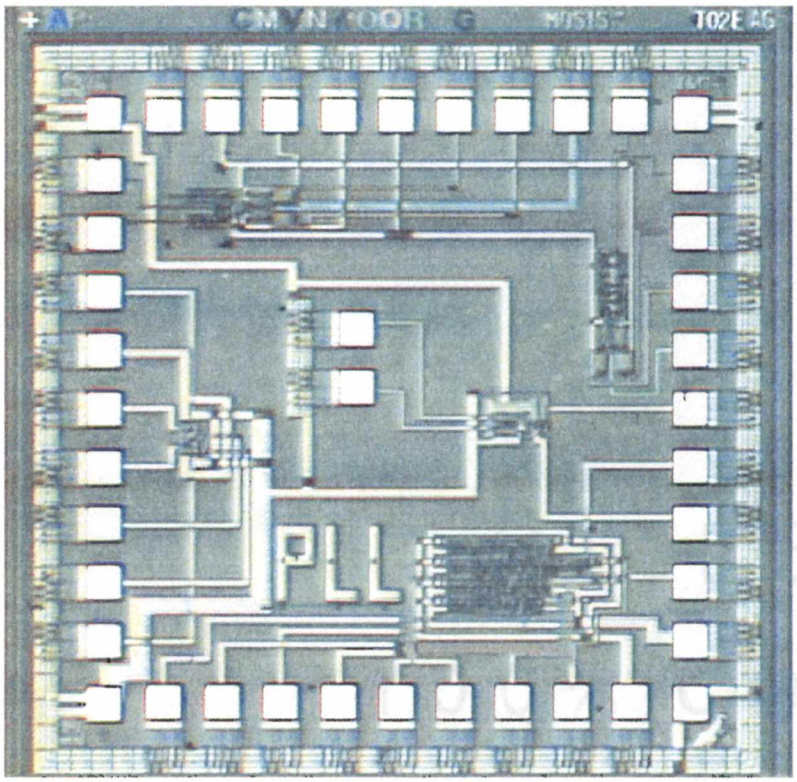


Figure 5.4: Microscope photo of PLLCHIP1 die

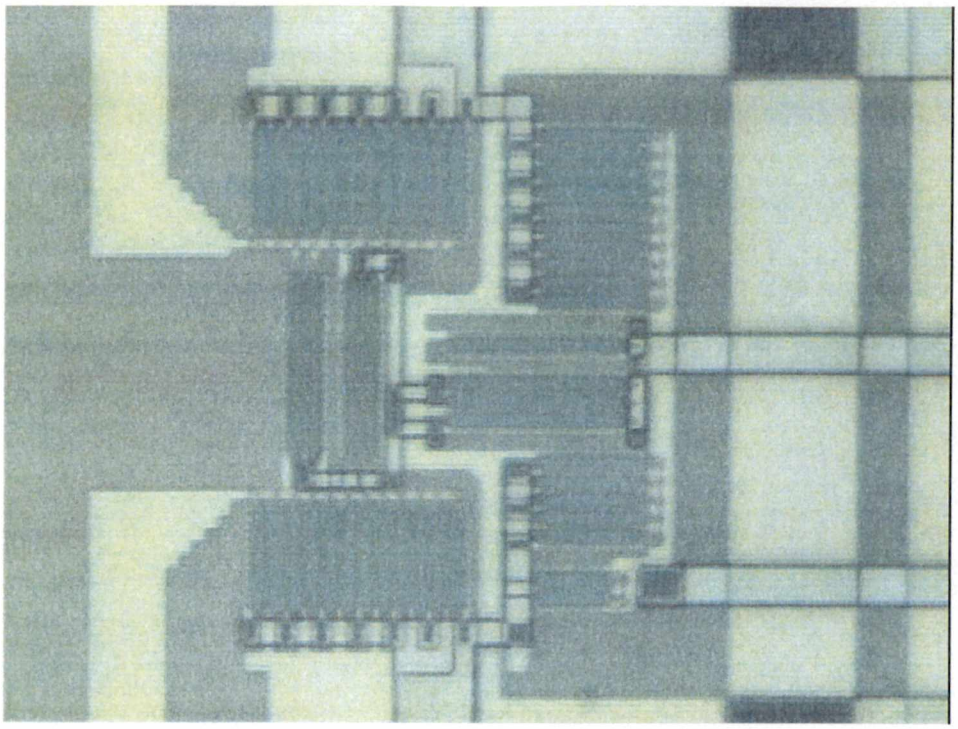


Figure 5.5: Microscope photo of PLLCHIP1 VCO

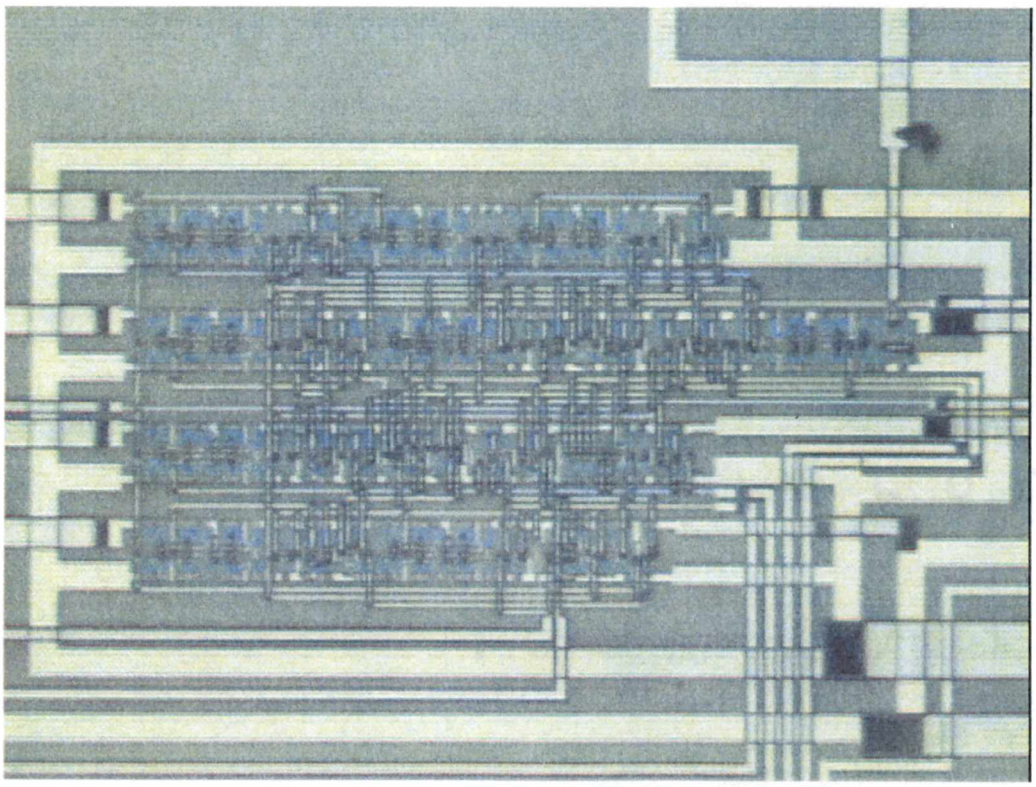


Figure 5.6: Microscope photo of PLLCHIP1 divider

5.3 Test Board Design

To adequately characterize the performance of the chip, a custom test fixture was designed. This system consists of two interconnected printed circuit boards and the off-chip components necessary to complete the PLL circuits. The main board, referred to as the motherboard, contains DC and low-frequency signal paths, including configuration jumpers and bias adjustment resistors. The other board, referred to as the daughterboard, contains the chip, resonant tank components, and all high-frequency signal paths. Table 5.1 lists the specific functions of each test board.

Table 5.1: Test board functions

Motherboard	Daughterboard
• DC power interface. • Biasing • Configuration jumpers • Control interfaces	• Surface-mounted IC chip • Resonant tank circuit components • RF input and output connectors

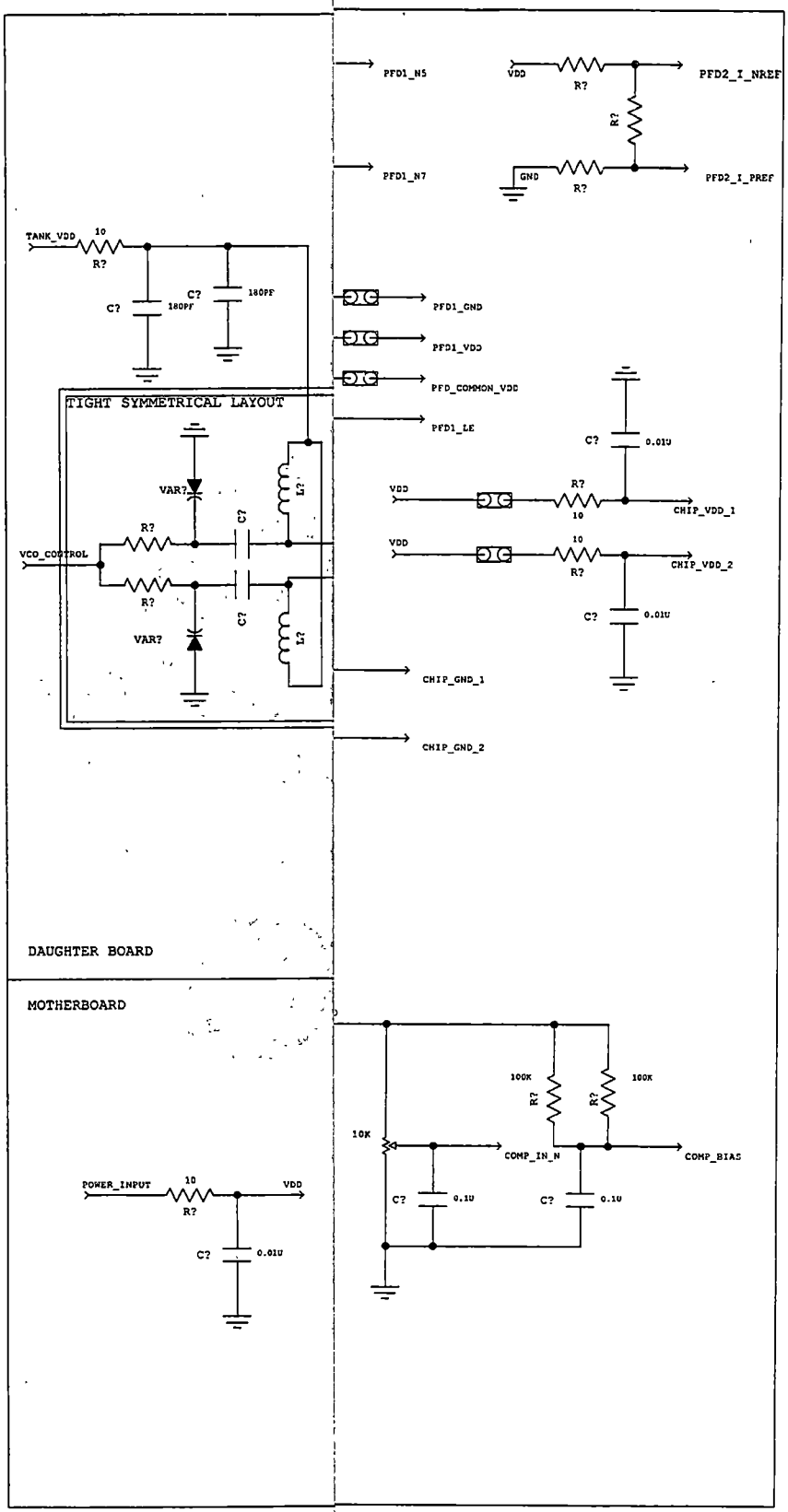
The chip is mounted on the circuit board using a technique known as "chip-on-board". In this approach, the cut die is not packaged, but is instead mounted directly onto the circuit board using epoxy. Wirebonds run directly from the pads on the chip to microstrips on the circuit board, thus minimizing parasitic effects due to the resistance and inductance in the wirebonds, and capacitance associated with a packaged-die implementation.

The test fixture is segmented into two boards because of the frequency-sensitive nature of many of the inputs and outputs on the chip. For instance, the resonant tank circuit for the VCO must be symmetrically laid out, in very close proximity to the chip, to achieve the

lowest possible noise. All high-frequency inputs and outputs are specified as 50-ohm transmission lines. These lines are located only on the daughterboard to simplify the design and minimize trace length. Connections to the transmission lines and other test points on the daughterboard are provided using SMA connectors.

The PLL loop filter was originally designed to be located on the motherboard. However, test results in the lab showed noise affecting the performance of the loop. The loop filter components were then attached to the bottom of the daughterboard, allowing shorter length connections. More details of this and other modifications are given in Section 5.4.

The daughterboard connects to the motherboard using a set of 1/10" pin headers. All biasing and DC control signals such as the programmable divider ratio are routed through the motherboard. A schematic diagram of the test boards is presented in Figure 5.7. Layout design for the test boards was done in cooperation with technical support staff at Oak Ridge National Laboratory. Based on trace routing requirements, a 1/16" thick two-layer board was used for the motherboard, while a 1/32" thick four-layer board was used for the daughterboard. Both boards used the industry-standard FR4 printed circuit board technology.


PFD1_N5
PFD1_N7
VDD
R?
PFD2_I_NREF
R?
GND
R?
PFD2_I_PREF
TANK_VDD
10
R?
C?
180PF
C?
180PF
PFD1_GND
PFD1_VDD
PFD_COMMON_VDD
PFD1_LE
TIGHT SYMMETRICAL LAYOUT
VAR?
L?
C?
R?
VCO_CONTROL
R?
C?
VAR?
L?
C?
0.01U
VDD
R?
10
CHIP_VDD_1
VDD
10
R?
CHIP_VDD_2
C?
0.01U
CHIP_GND_1
CHIP_GND_2
DAUGHTER BOARD
MOTHERBOARD
100K
R?
100K
R?
10K
COMP_IN_N
COMP_BIAS
C?
0.1U
C?
0.1U
POWER_INPUT
10
R?
VDD
C?
0.01U

Several layout revisions were made prior to fabrication to tweak the transmission line properties, interface points, and tank circuit symmetry. The daughterboard layout proved to be the most challenging. One interesting technique used in the daughterboard layout involves the design of the high-frequency transmission lines. These were fabricated using the top layer metal and the third-layer ground plane. This approach allowed a significantly narrower trace width than would have been possible using the second-layer ground plane. Consequentially, the traces on the board could be arranged closer together, providing a more compact board layout. Figure 5.8 illustrates the design tradeoffs, comparing a cross-section of the board for the two possible transmission line designs. Computer layout drawings for each layer of the daughterboard are presented in Figures 5.9 through 5.12. Drawings for the motherboard are presented in Figure 5.13 and Figure 5.14.

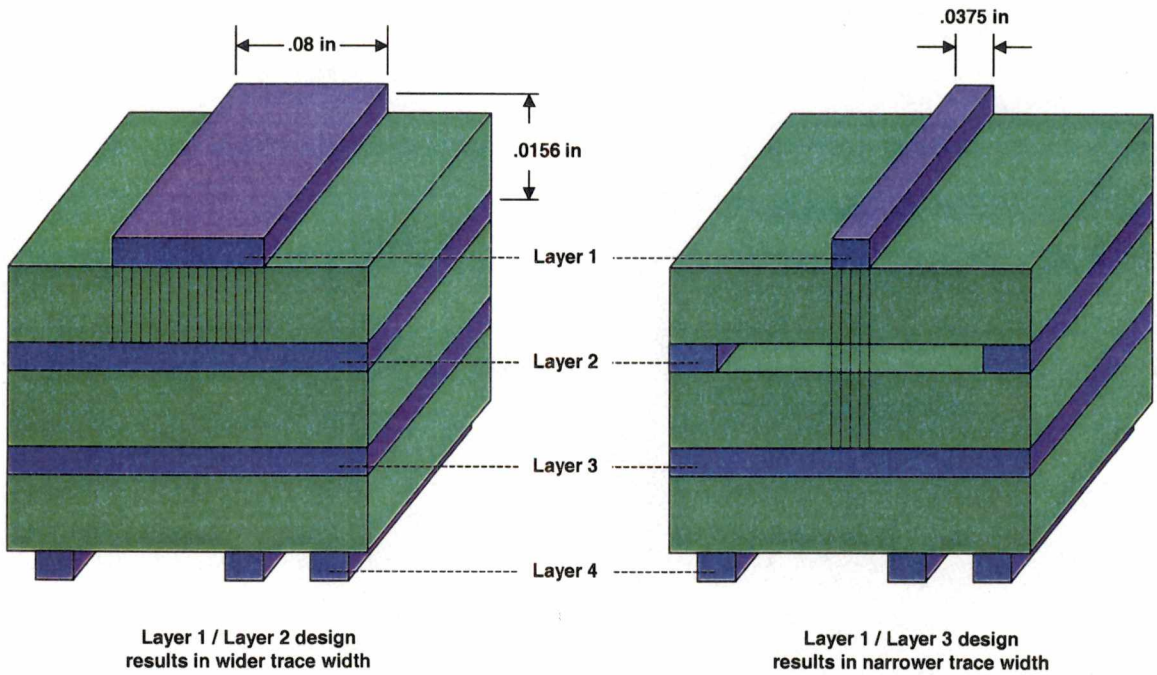


Figure 5.8: Comparison of transmission line designs

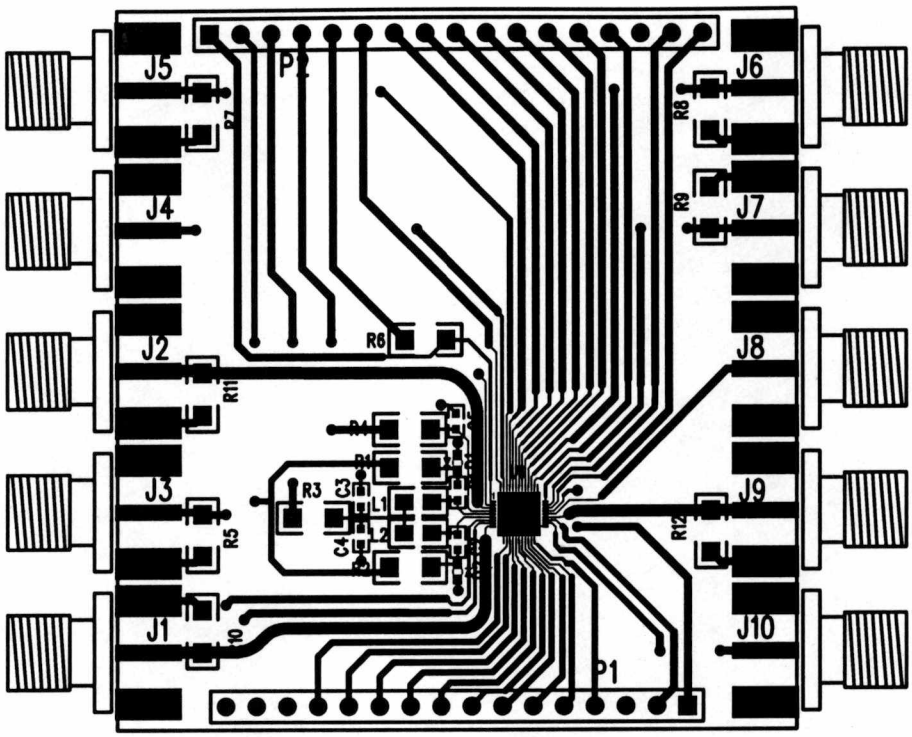


Figure 5.9: PLLCHIP1A test board layout: layer 1 (top)

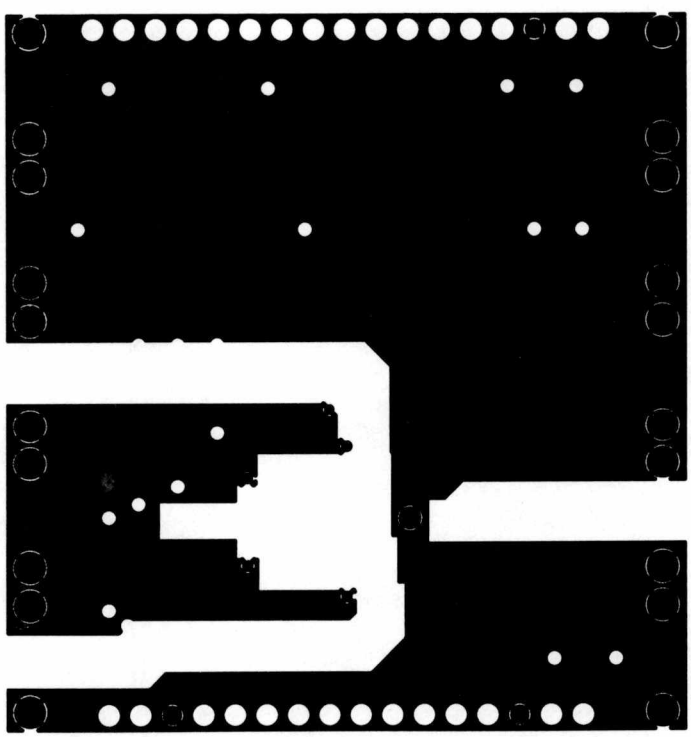


Figure 5.10: PLLCHIP1A test board layout: layer 2

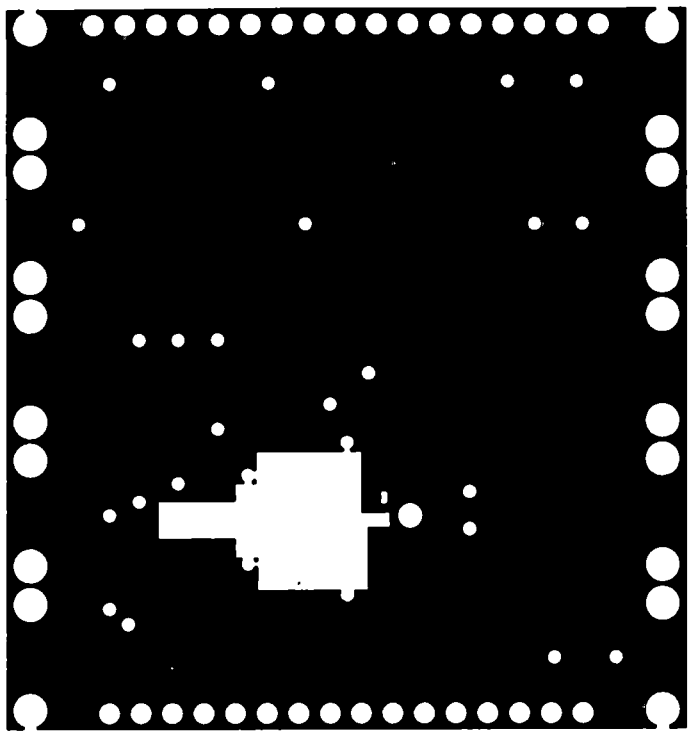


Figure 5.11: PLLCHIP1A test board layout: layer 3

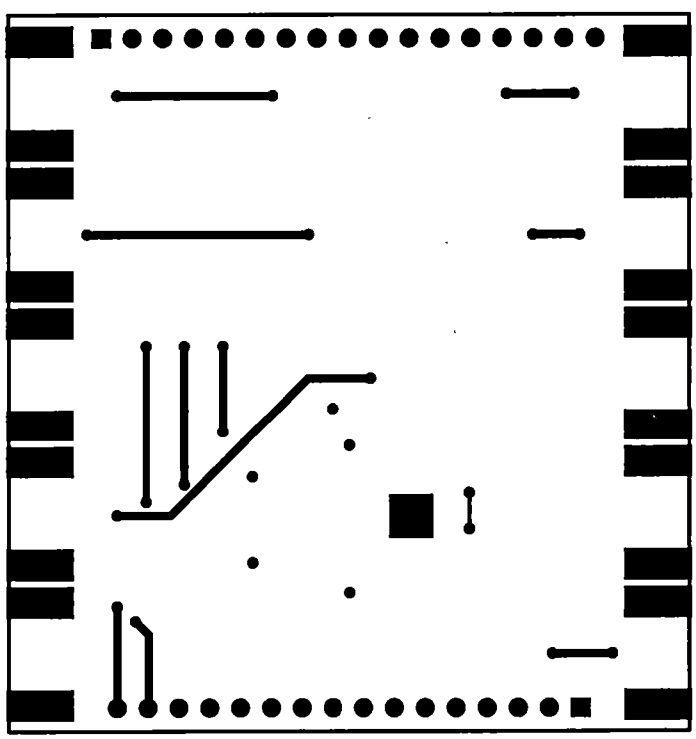


Figure 5.12: PLLCHIP1A test board layout: layer 4 (bottom)

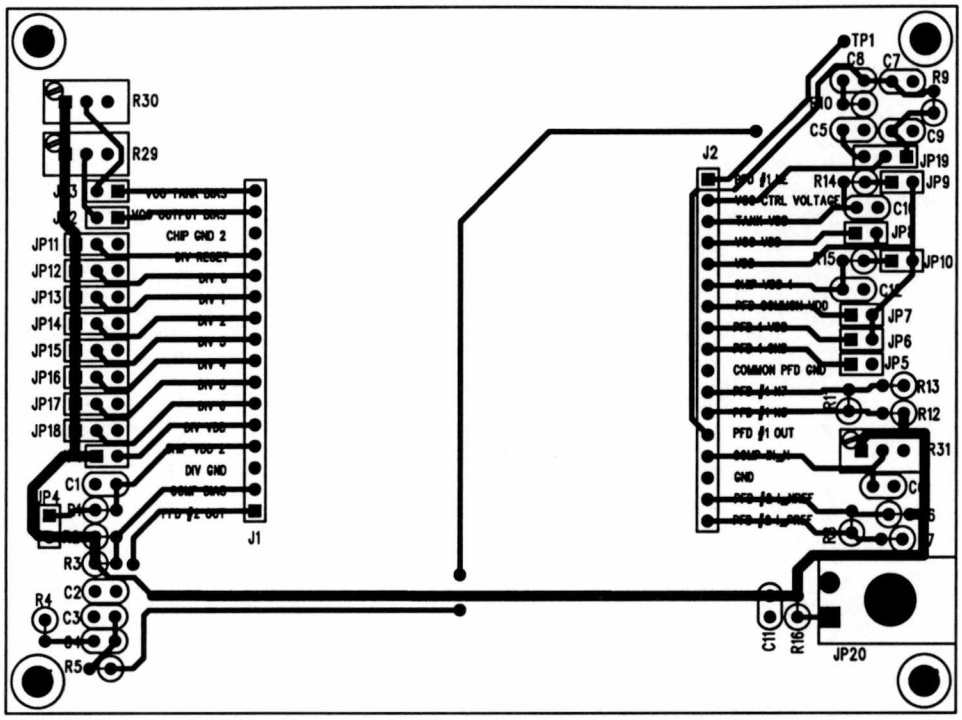


Figure 5.13: PLLCHIP1B test board layout: top

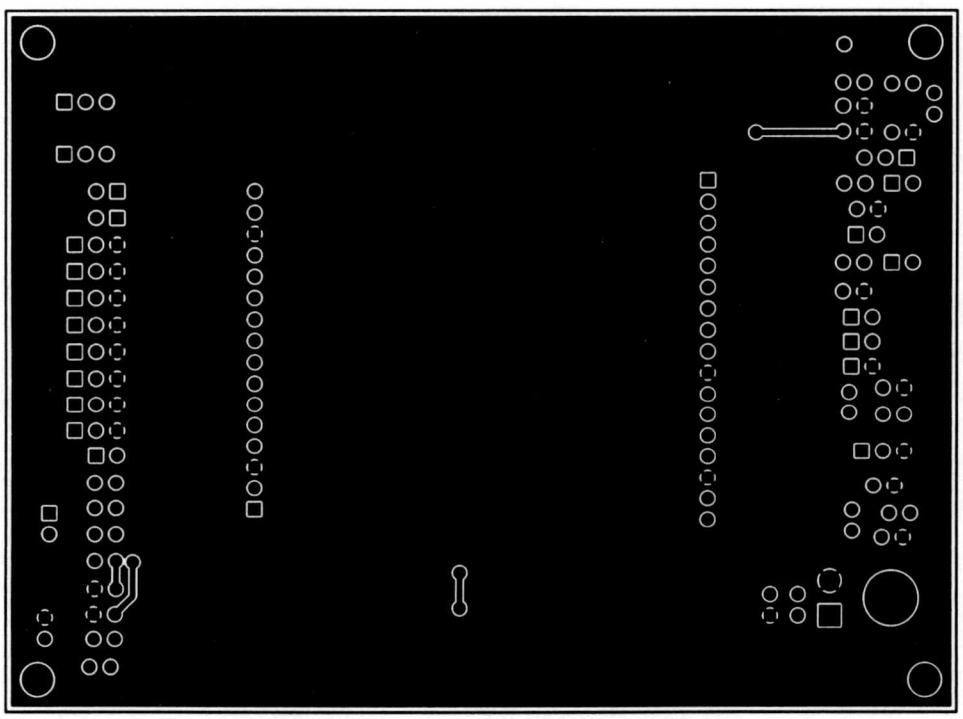


Figure 5.14: PLLCHIP1B test board layout: bottom

5.4 Test Board Modifications

After the test boards were fabricated, the PLLCHIP1 die was mounted and wirebonded by technical support staff at ORNL. Surface-mount devices and the remaining board-level components were soldered into place in the lab prior to testing. After evaluating some initial test results involving the closed-loop PLL, several modifications were made to improve the performance of the system. Specific details of the circumstances which prompted some of the modifications are described in Section 5.7.2. Photographs of the final test board configurations are presented in Figure 5.15 and Figure 5.16.

First of all, the PLL loop filter was moved from the motherboard to the bottom of the daughterboard. This was accomplished by rerouting some of the signals on the daughterboard and eliminating unnecessary signal paths. The improvement realized by this modification was substantial, as it resulted in a dramatic reduction in phase noise of the closed-loop system.

A second modification was the installation of additional power supply bypass capacitors on the interface points to the daughterboard. This helped to eliminate another source of noise, which improved both the phase noise of the VCO (open-loop) and of the PLL (closed-loop). Third, the output of the divider was rerouted so that it was hard-wired to the input of the phase detector. This provided the shortest and cleanest signal path possible, making the best use of the divider's limited drive capability.

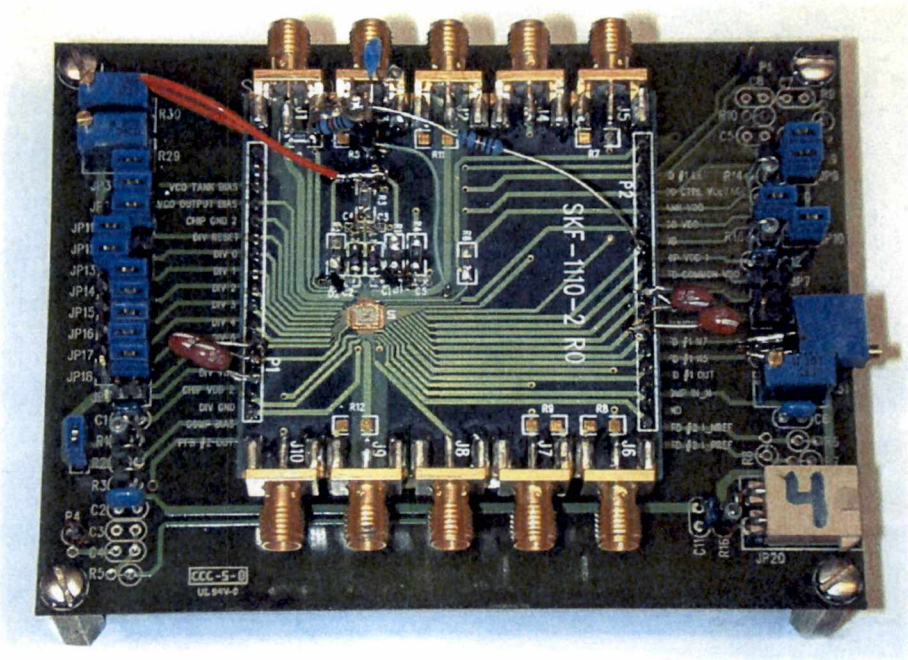


Figure 5.15: Test boards with modifications, top view

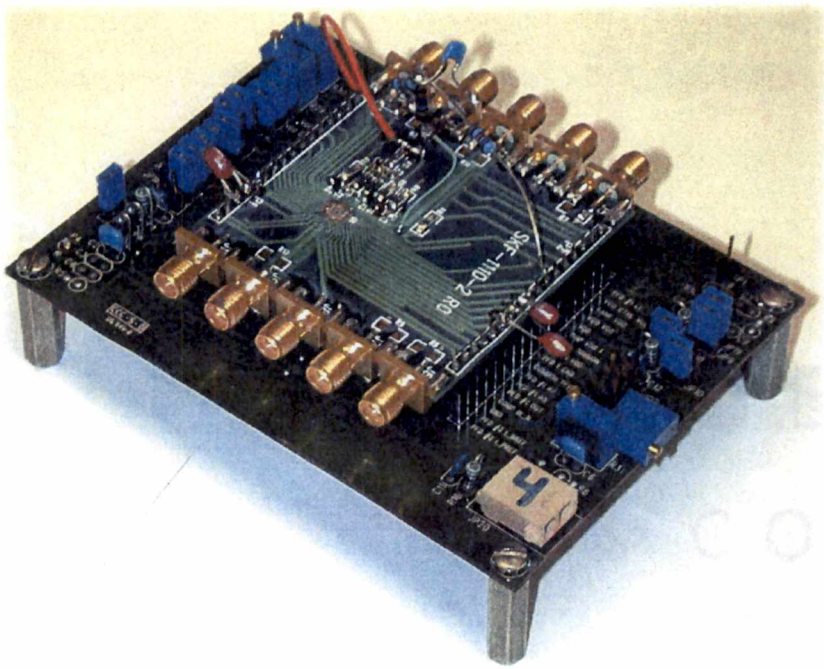


Figure 5.16: Test boards with modifications, isometric view

Fourth, a simple level-shifting circuit was built at the reference frequency input, which moved the DC offset voltage to the middle of the divider's rail voltage. This allowed an external signal generator having a 0-V offset to be used as the reference source. Finally, separate power connections were established on the motherboard to control the divider rail voltage as well as the phase detector and charge pump rail voltages. This allowed the signal swings from each component to be optimized when the loop was closed, and resulted in improved loop stability and phase noise.

5.5 VCO Test Procedures and Results

Testing of the prototype voltage-controlled oscillator was conducted to evaluate several key operating parameters, including tuning range, output drive, and phase noise, and stability of these over temperature. During the tests, the VCO was not connected to the other components of the PLL. This allowed the control voltage to be manually set, and the outputs to be monitored using appropriate test equipment.

5.5.1 Tuning Range

The tuning range of the VCO was characterized by incrementally sweeping the control voltage from rail to rail (0 V to 3.5 V) in steps of 0.25 V. The output frequency at each step was measured using a spectrum analyzer. In addition, the tuning range tests were conducted over the complete range of operating temperatures, from 25 ºC to 200 ºC, in increments of 25 ºC. The set of curves derived from these tests provided some insight into the gain of the VCO as well as its stability over temperature. Figures 5.17 and 5.18 show results of the tuning range tests from two different test boards.

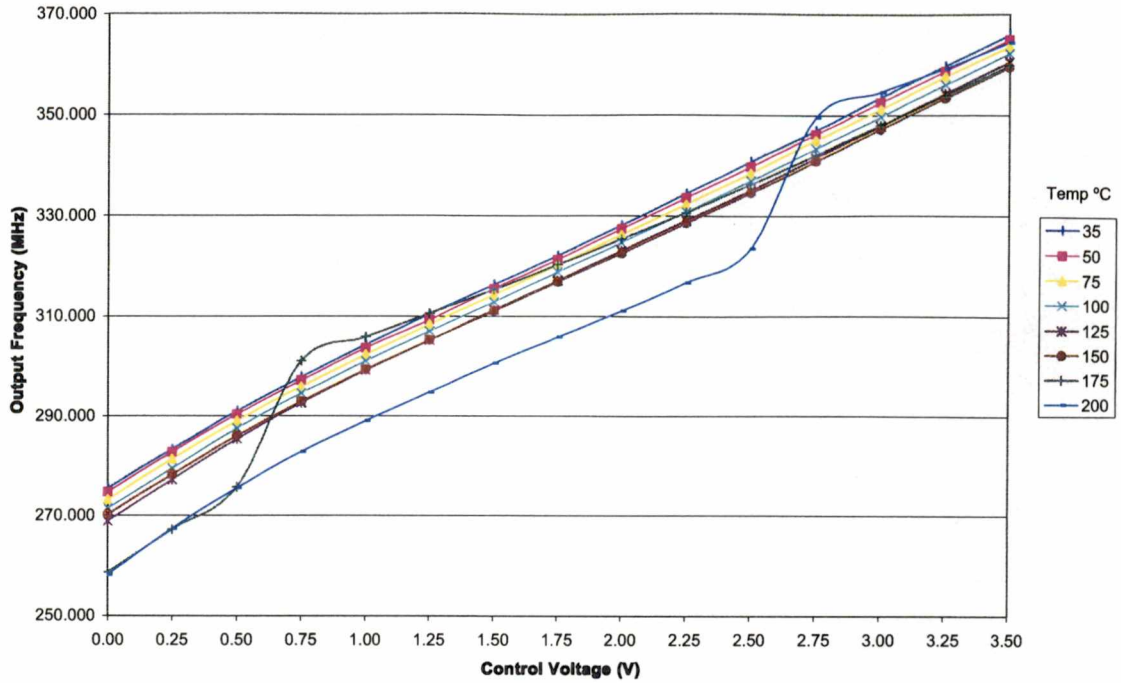


Figure 5.17: VCO control voltage vs. frequency - Test board #1

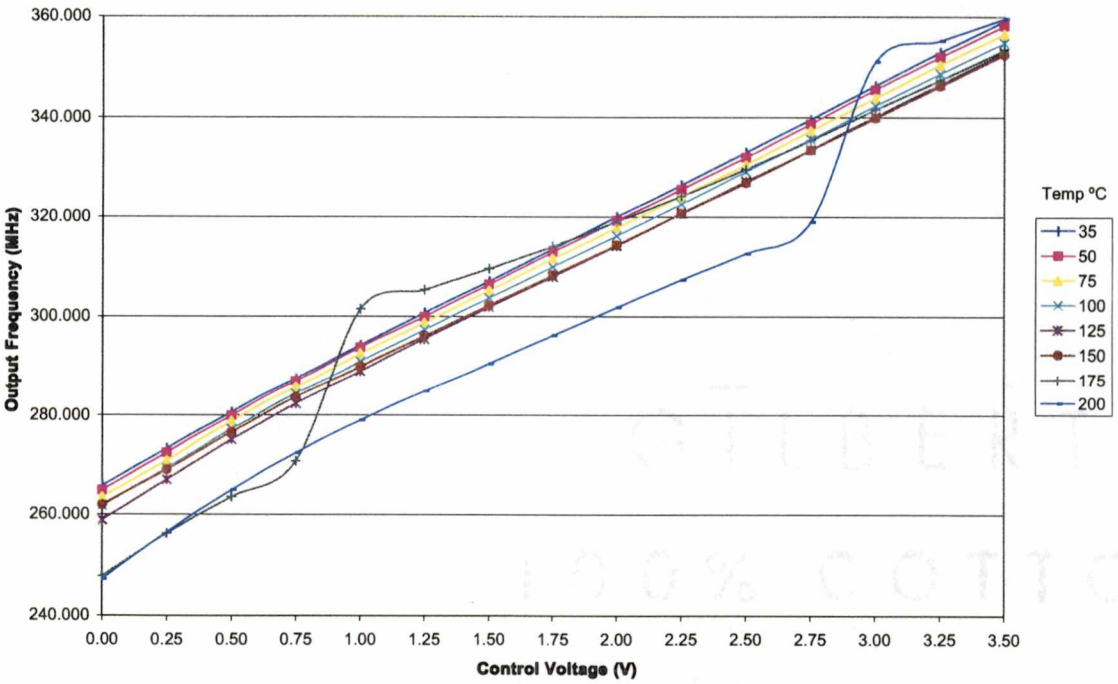


Figure 5.18: VCO control voltage vs. frequency - Test board #2

Multiple boards were used in this test to demonstrate consistency of the results. The VCO gain is reflected in the slope of the lines in Figures 5.17 and 5.18. A numerical evaluation of the measured test data was performed to obtain information about the gain of the VCO at each temperature, as well as the drift in VCO gain over temperature. A summary of the results is presented in Tables 5.2 through 5.4.

These results reveal several important characteristics of the VCO performance. First of all, the gain remains relatively constant over temperature. The slopes of the control voltage vs. frequency curves do not change significantly over most of the temperature

Table 5.2: VCO measured gain - Test board #1

Temp (ºC)	Gain (MHz/V)
25	25.25
50	25.17
75	25.17
100	25.22
125	25.41
150	24.80
175	27.05
200	30.19

Table 5.3: VCO measured gain - Test board #2

Temp (ºC)	Gain (MHz/V)
25	26.38
50	26.35
75	26.22
100	26.20
125	26.31
150	25.48
175	29.51
200	30.75

Table 5.4: Comparison of VCO gain and drift

Test Board	Average Gain	Gain Drift
#1	26.0 MHz/V	0.021569 MHz/ºC
#2	27.2 MHz/V	0.022226 MHz/ºC

range. However, an interesting anomaly occurred in both test boards at 175 and 200 ºC, where an abrupt shift in frequency was observed. This was not predicted by simulations. Because this effect was observed in both test boards at approximately the same temperature and control voltage settings, the anomaly is likely not a function of differences between the test board components or assembly. Instead, it is most likely attributable to a non-linear characteristic of the tank circuit, and most probably, the varactor diodes [30]. Since the manufacturer's measured specifications did not extend above 90 ºC, the only means of modeling the diode performance at high temperatures was a continued extrapolation of lower-temperature measurements using the manufacturer's model, which has no means of accounting for discontinuities in the performance of the diode. Therefore, because the varactors control the resonant frequency of the VCO, a reasonable explanation of the discontinuity in the VCO tuning range is a discontinuity in the varactor's reverse-bias capacitance.

Despite these discontinuities, the average gain for both test boards agreed within 5% over all temperatures. The gain drift, or amount of change in gain relative to temperature, agreed within 3% between the test boards. These two results are quite important, as they demonstrate that the VCO has a consistent level of performance between different boards, temperatures, and operating frequencies. Especially notable is the very low gain drift, which averaged approximately 22 kHz/V per ºC. If the anomalies at 175 and 200 ºC are excluded, the average gain drift is approximately -3.5 kHz/V per ºC. In either case, the measured gain drift of the VCO demonstrates remarkable stability over temperature, especially considering that many of the components used in the tank circuit had no manufacturer's characterization above 100 ºC.

5.5.2 Output Drive

The output drive capability of the VCO was documented using both a spectrum analyzer and an oscilloscope. During the tuning range tests, the output power level was recorded, in addition to the frequency. This allowed a plot to be generated showing the output power of the VCO over the entire range of control voltages and temperatures. Plots for both test boards are presented in Figures 5.19 and 5.20. In addition, several plots of the output waveforms at different control voltages and temperatures were obtained using an oscilloscope. These plots allow visual inspection of the output peak-to-peak voltage range and offset, as well as any distortion or noise that may be present on the output waveform. The oscilloscope plots are included as Figures 5.21 through 5.25.

An inspection of the spectrum analyzer plots shows that the output power remains fairly constant over the entire tuning range at a given temperature, with the exception of the anomalies previously discussed at 175 and 200 ºC. In those cases, the output power drops abruptly at the point of anomaly, reflecting a drop in the resonant signal voltage in the tank circuit. Like the shift in frequencies, this effect can also be attributed to a discontinuity in the varactors. Overall, the output power levels of the VCO are relatively constant, and are consistent with simulations showing that the output drive of the VCO drops slightly as the ambient temperature increases. Likewise, the oscilloscope waveforms correspond well with the simulation results presented in Figures 3.9 and 3.11. The VCO maintained correct operation over a range of supply voltages from 2.55 to 3.3 V, although the output drive was proportionally lower at reduced supply voltages.

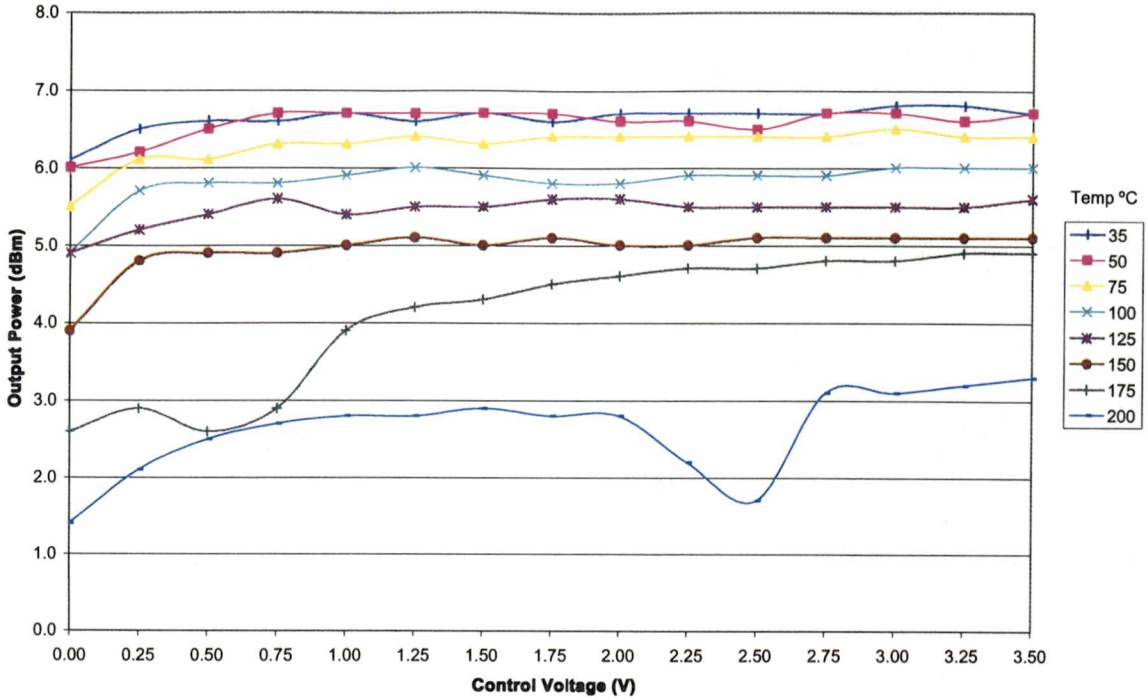


Figure 5.19: VCO output power vs. control voltage - Test board #1

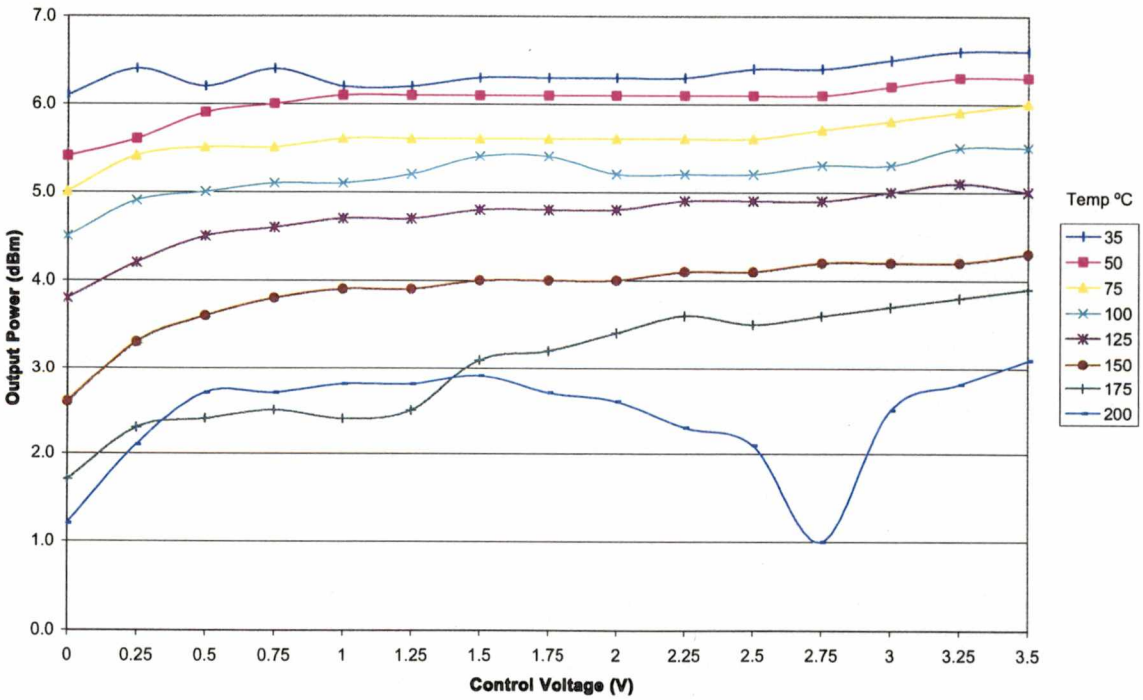


Figure 5.20: VCO output power vs. control voltage - Test board #2

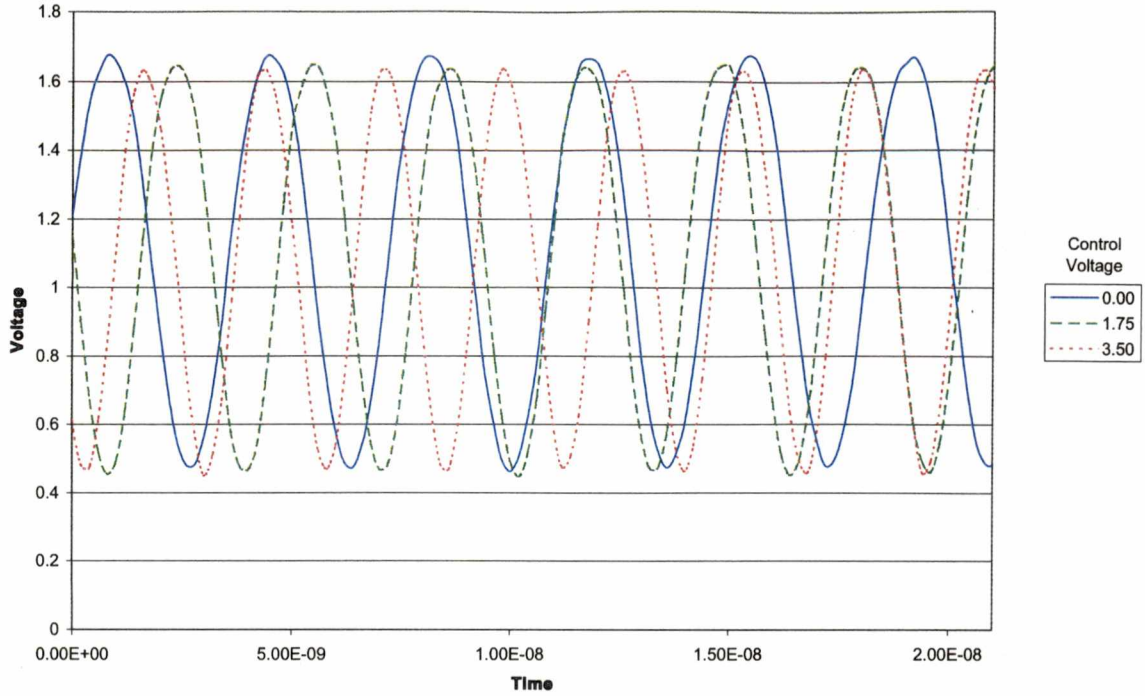


Figure 5.21: VCO output waveforms at 25 ºC

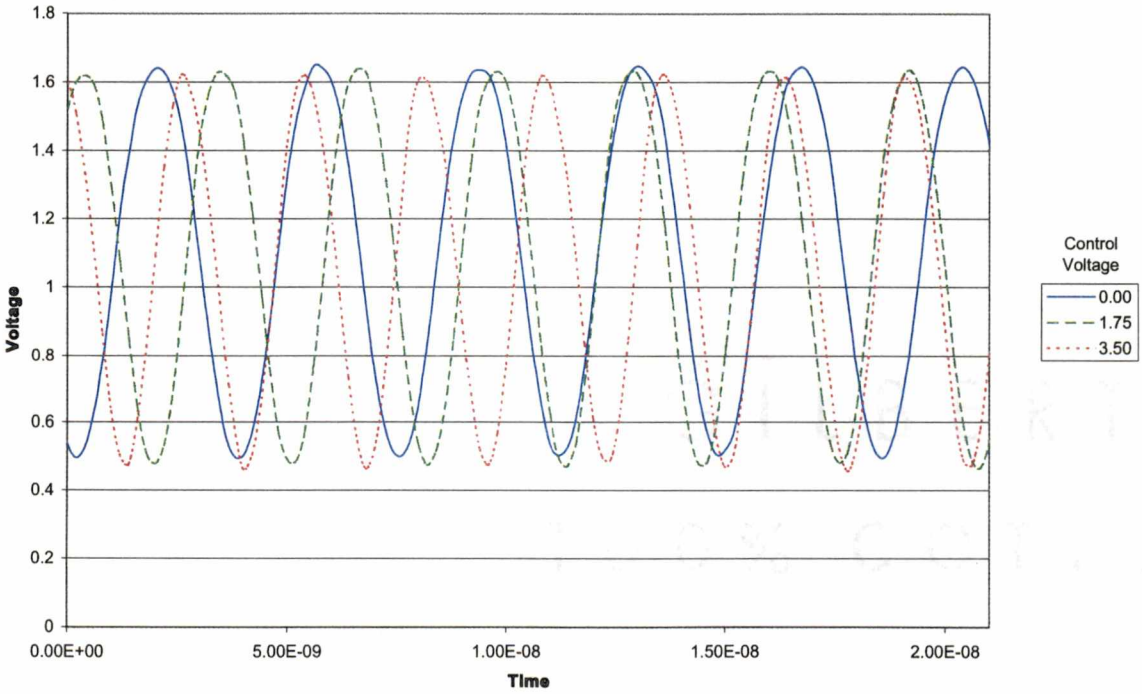


Figure 5.22: VCO output waveforms at 50 ºC

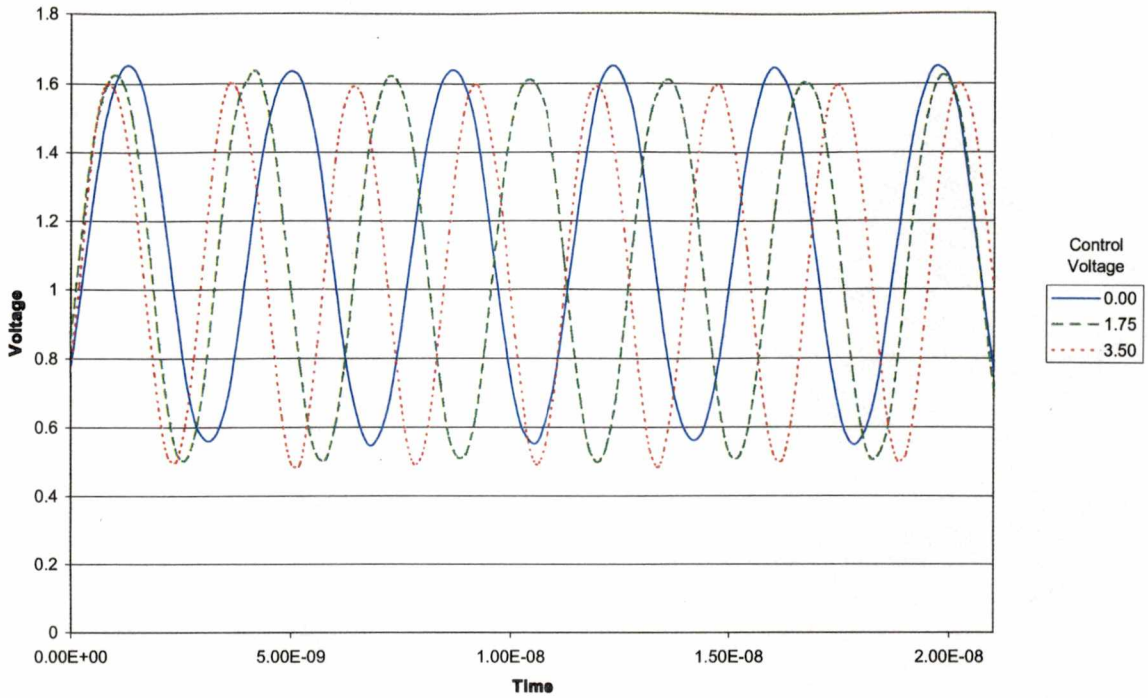


Figure 5.23: VCO output waveforms at 100 ºC

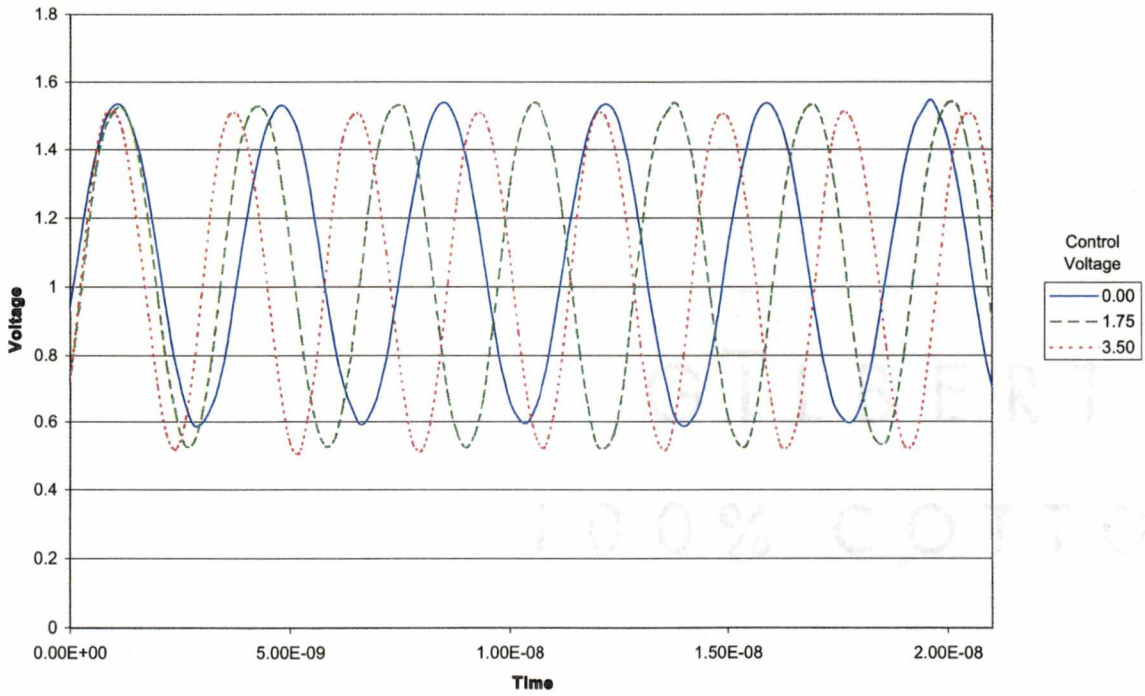


Figure 5.24: VCO output waveforms at 150 ºC

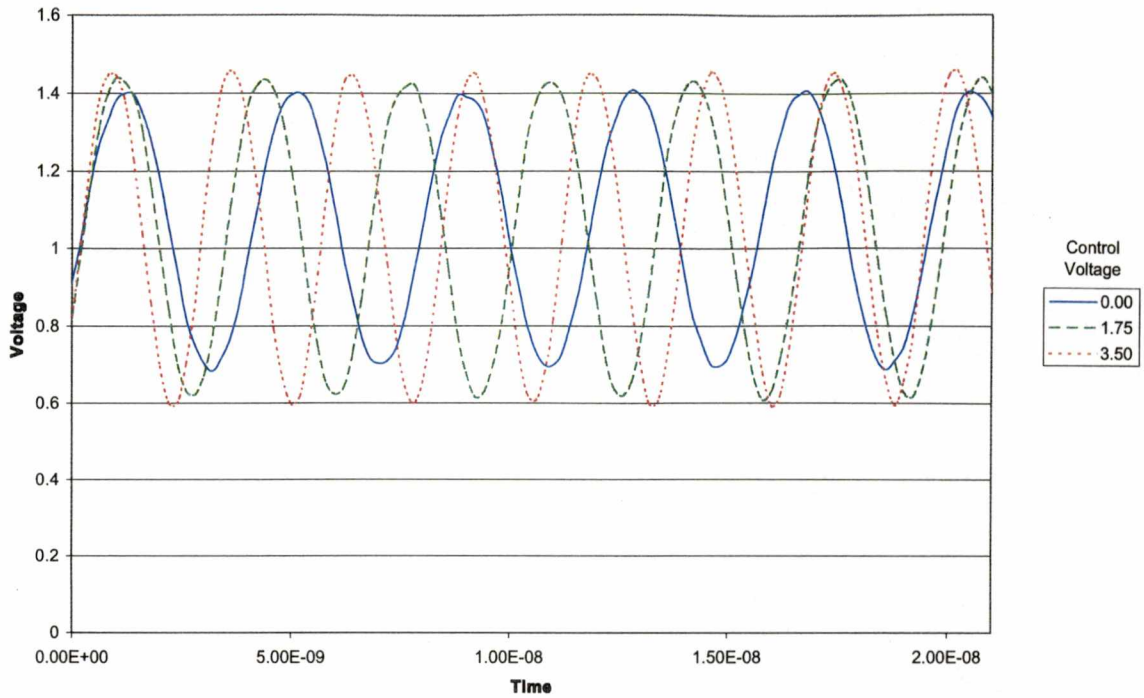


Figure 5.25: VCO output waveforms at 200 ºC

In fact, the measured results show that the peak-to-peak voltage drop from 25 ºC to 200 ºC is slightly less than the simulations predicted. This is an excellent and very beneficial result in terms of the overall performance of the VCO, although it underscores the fact that the simulation models do not fully account for the effects present in the physical circuit.

5.5.3 Phase Noise

The open-loop phase noise of the VCO was measured using a spectrum analyzer. The control voltage was fixed at the midpoint of the tuning range, and data was recorded over the entire range of operating temperatures. Table 5.5 details the measured data, which was compiled to generate a spectral plot over temperature, shown in Figure 5.26.

Table 5.5: VCO open-loop phase noise measurements

Temp ºC	dBc at Offset Frequency (kHz)								
	0.5	1	2	4	10	20	50	100	200
25	-18	-28	-32	-37	-48	-61	-68	-71	-73
50	-24	-35	-41	-49	-55	-59	-65	-70	-73
75	-21	-32	-38	-42	-51	-61	-69	-71	-74
100	-20	-29	-35	-38	-49	-60	-68	-71	-74
125	-19	-26	-36	-45	-55	-58	-67	-70	-73
150	-18	-25	-35	-44	-53	-63	-69	-71	-74
175	-21	-28	-40	-49	-58	-62	-70	-72	-74
200	-20	-27	-39	-45	-57	-59	-68	-71	-74

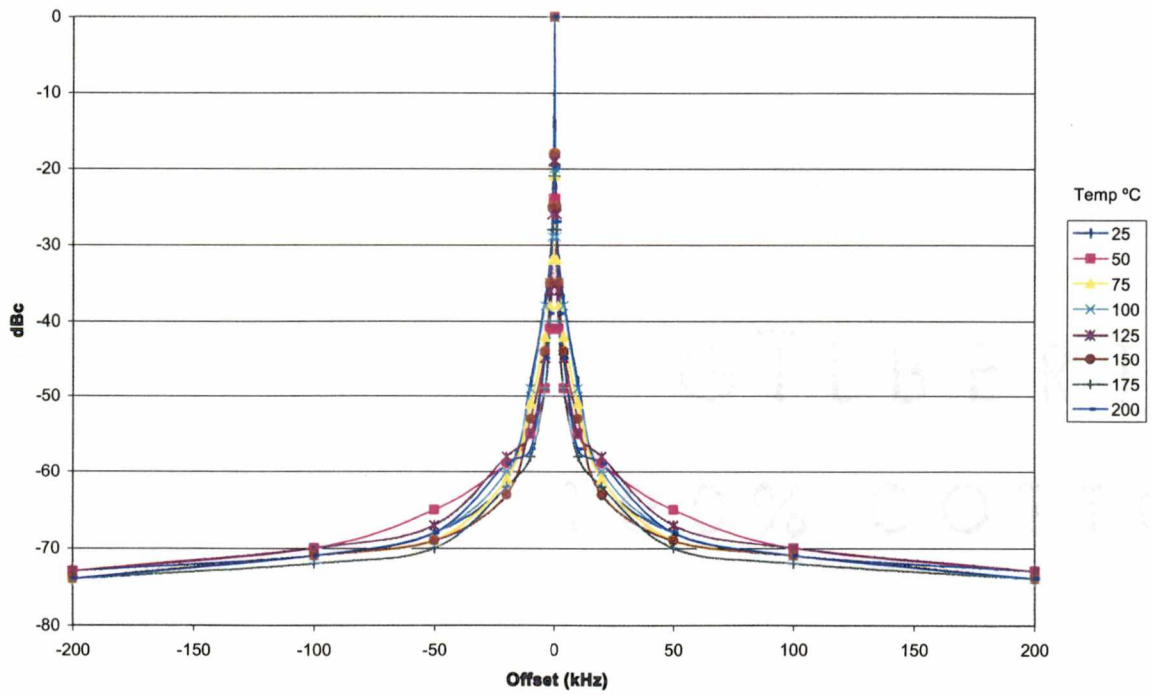


Figure 5.26: VCO output spectrum over temperature

The open-loop phase noise performance of the VCO is relatively good, with results over temperature yielding at least -48 dBc at a 10 kHz offset. Of equal importance is the fact that the output power spectrum does not exhibit significant deviations over temperature, demonstrating that the resonant tank components are capable of maintaining a relatively constant quality factor regardless of temperature. These two characteristics are very important in the overall performance of the PLL. As discussed in Section 2.6, the phase noise of the VCO contributes to the overall phase noise of the PLL. Therefore, good VCO phase noise performance will be reflected in the closed-loop PLL output as well.

5.6 Frequency Divider Test Procedures and Results

The programmable frequency divider was tested open-loop in several different configurations to ensure accuracy over different division ratios. This was accomplished by connecting a reference signal generator to the input of the divider, using a sinusoidal signal with appropriate voltage levels to emulate the output of the VCO. The divider output was monitored using a digital oscilloscope and FET-input probe, allowing the output frequency to be obtained without severely loading the output of the circuit. During this test, the divider was not connected to any other components of the PLL.

The five major division ratios (260, 280, 300, 320, and 340) were all tested successfully using a corresponding input frequency in the MHz rage. For instance, the divider was configured to divide by 300, and a 300 MHz input signal was applied. The output signal was then evaluated to determine the accuracy of the division ratio. In all cases, the division ratio was accurate up to the limit of measurement resolution of the test equipment.

Measurement of the divider output over temperature proved to be significantly challenging. This was due in part to the output drive capability of the divider. During the initial design phase, output buffering on the divider was not designed to drive low impedance loads, due to the fact that the divider was to interface with the phase/ frequency detector, which has a high impedance input. The limited output drive capability of the divider caused the output waveform to be slewed when connected to a load other than the PFD input, including normal oscilloscope probes and other cables.

To circumvent these loading issues, a FET-input oscilloscope probe was used to monitor the output of the divider. Thus, measurements at high temperatures could not easily be performed without risking damage to the test equipment. The only means of obtaining high-temperature measurements was to heat the circuit in the oven with no measurement equipment attached. Then, once the desired temperature was reached, the oven was quickly opened and the FET probe applied to the divider output. A digital oscilloscope was used to capture the output waveform before significant cooling could occur. Although this measurement technique was not optimum in the sense of precise temperature control, it did allow a reasonable sampling of high-temperature performance of the divider.

Several oscilloscope plots of the divider output were recorded to compare performance at various temperatures and division ratios. To characterize the minimum and maximum division ratios and verify that the divider was operating correctly, plots were obtained using a divide-by-4 configuration and a divide-by-512 configuration at room temperature. Additional plots were recorded at a fixed division ratio over the full temperature range.

The room-temperature plots are presented in Figures 5.27 and 5.28. A noticeable feature of the divide-by-4 plot is the slew rate limiting of the divider output. This effect is primarily due to the sizing of the output buffers, which were not intended to drive a signal off-chip. The slew rate could potentially be improved by increasing the buffer sizes to allow a larger current capacity. The divide-by-512 plot shows a typical square-wave digital output, and highlights the 50% duty cycle of the divider output signal. To characterize the performance of the divider output over temperature, the plots in Figures 5.29 through 5.33 were obtained using a divide-by-16 configuration at several temperatures between 25 and 200 ºC. These plots enabled the output slew rate to be determined, along with any deviations in duty cycle or peak-to-peak amplitude. The divider also maintained acceptable operation over supply voltages ranging from 2.25 V to 3.3 V.

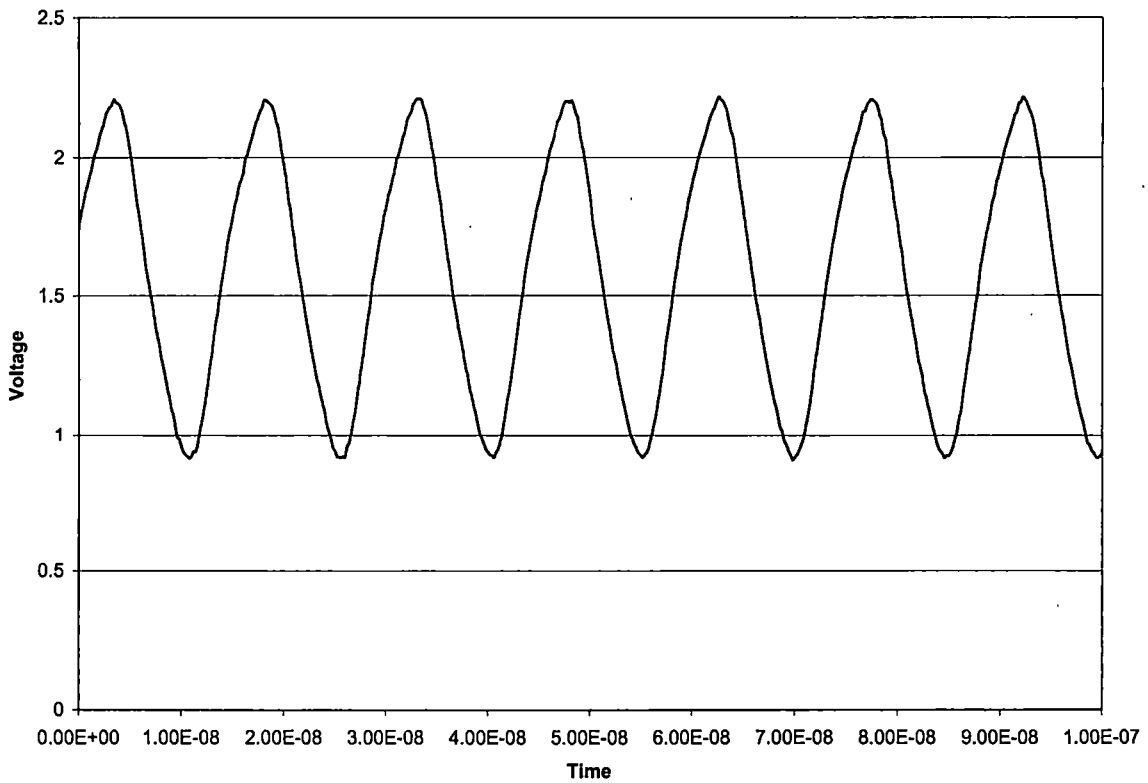


Figure 5.27: Divide-by-4 output at 25 ºC

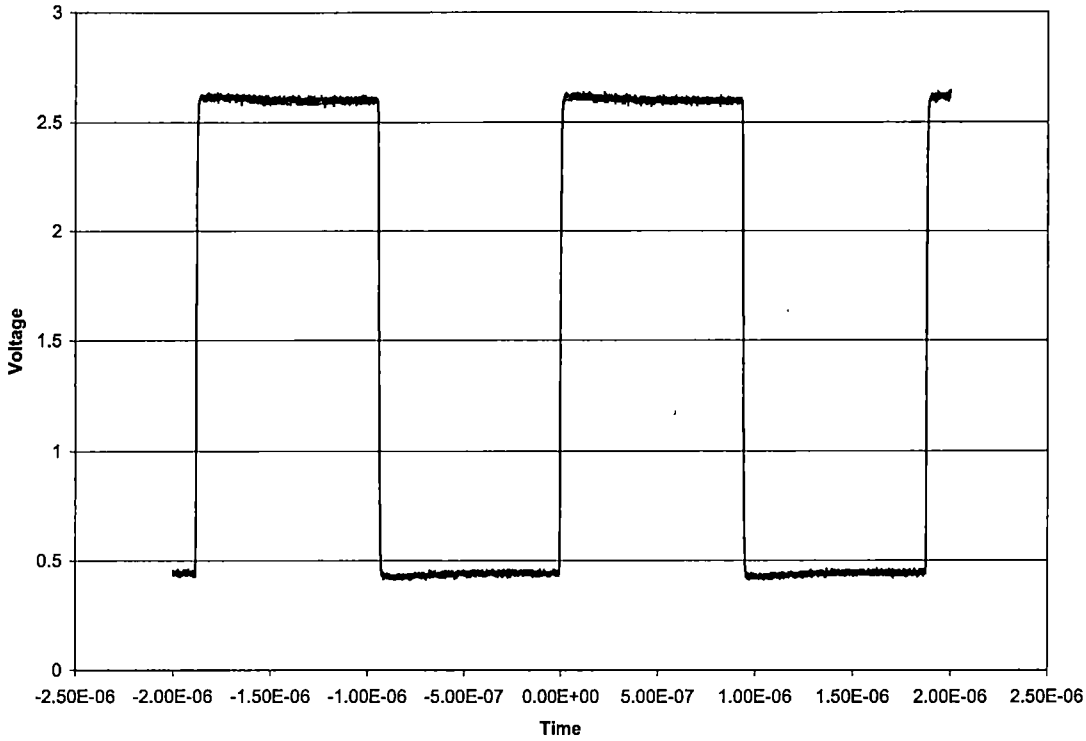


Figure 5.28: Divide-by-512 output at 25 ºC

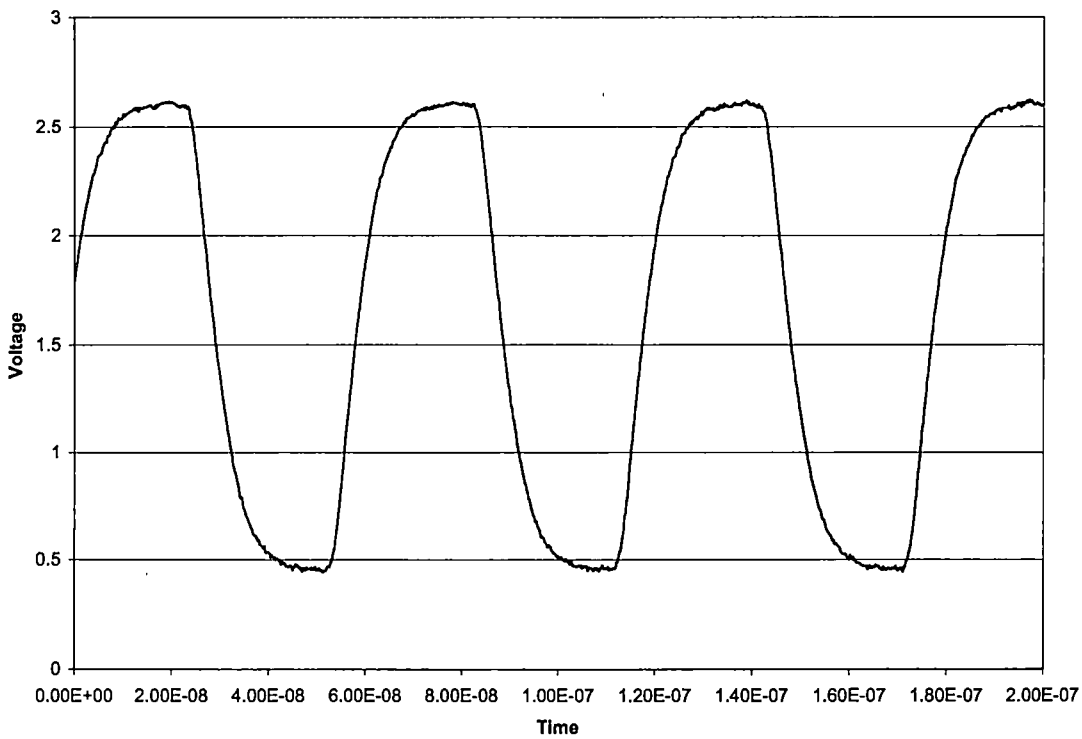


Figure 5.29: Divide-by-16 output at 25 ºC

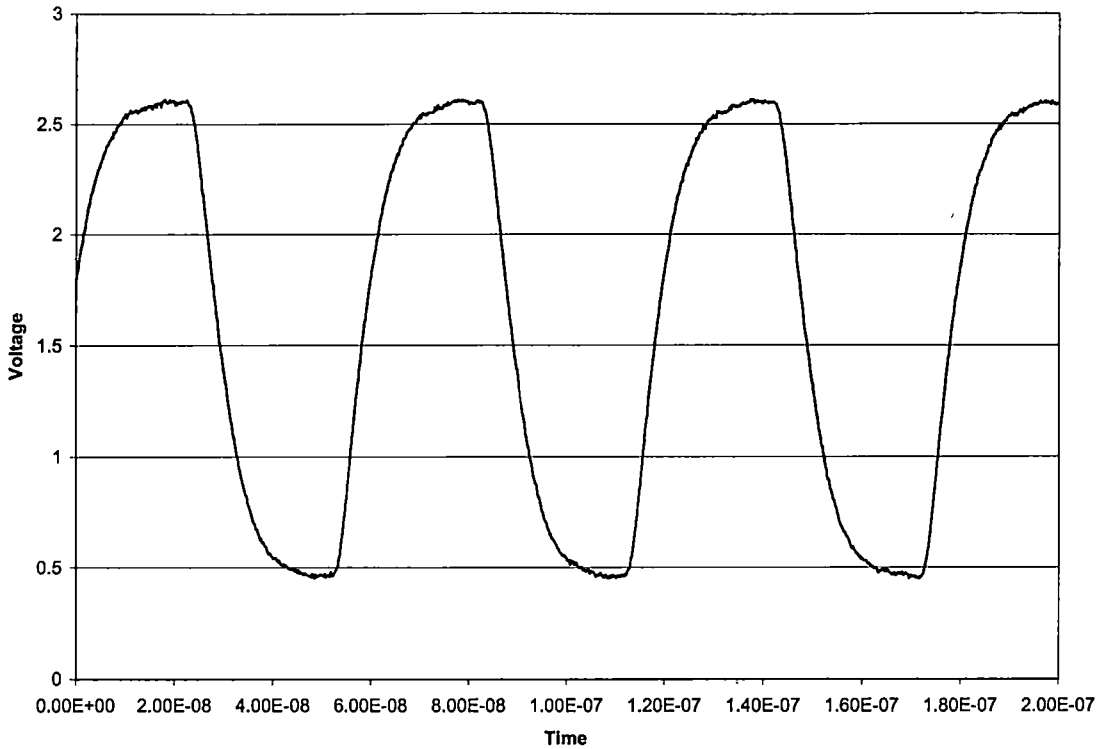


Figure 5.30: Divide-by-16 output at 75 ºC

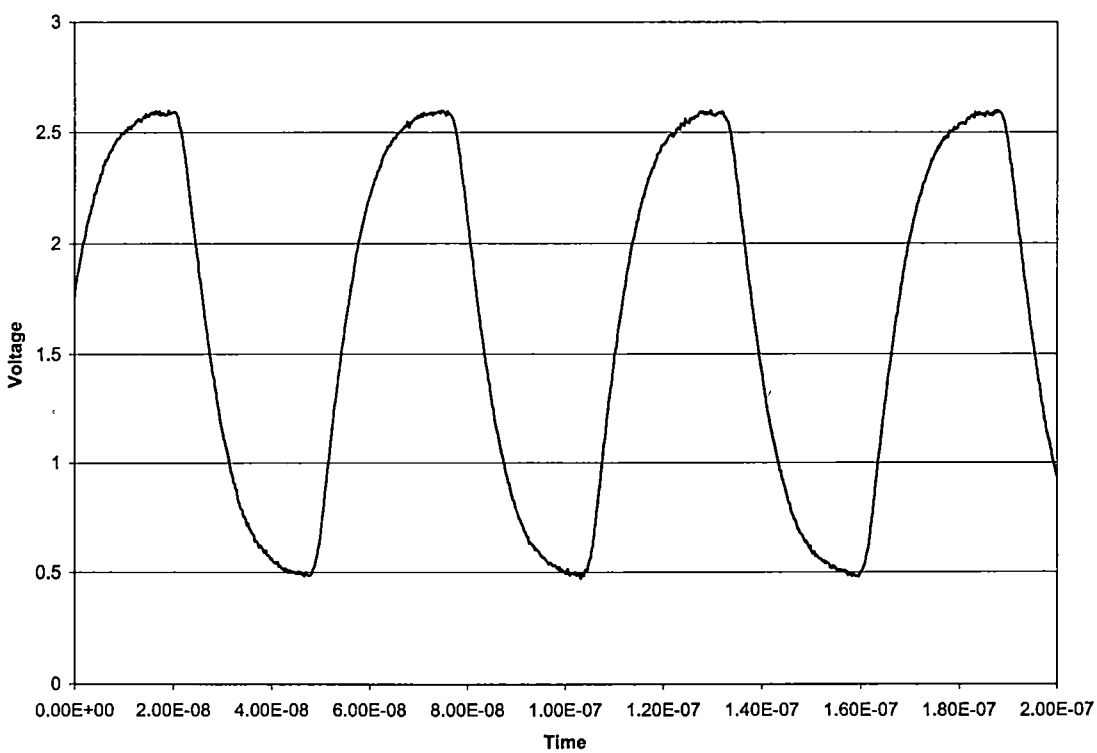


Figure 5.31: Divide-by-16 output at 125 ºC

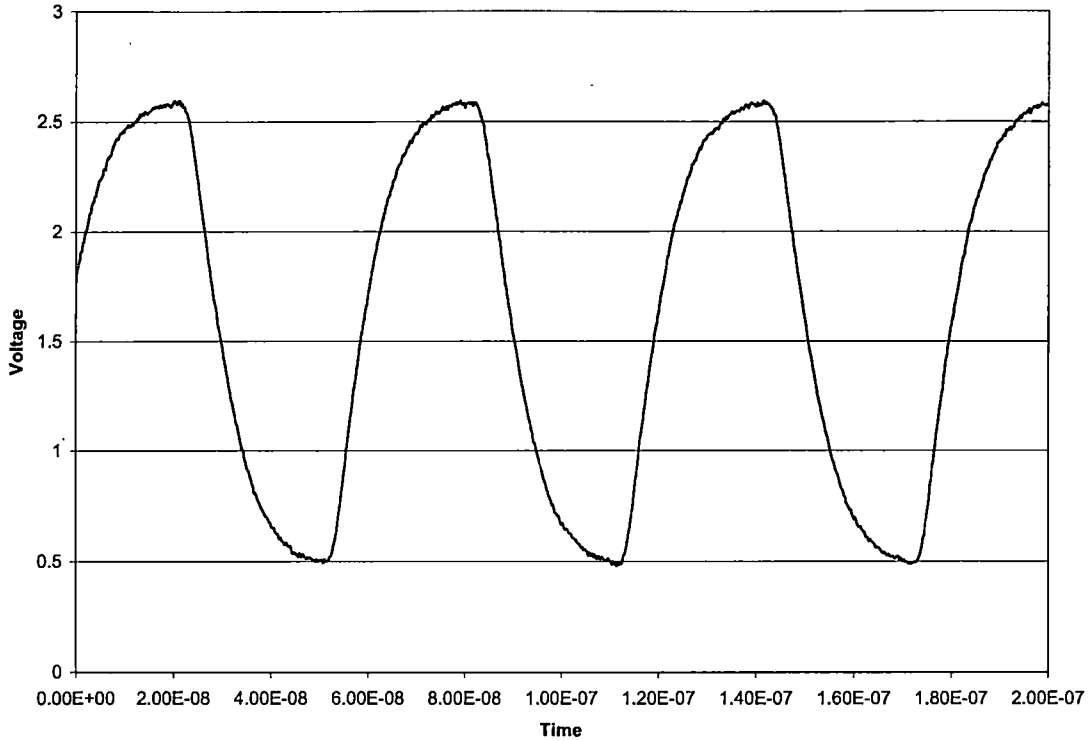


Figure 5.32: Divide-by-16 output at 175 ºC

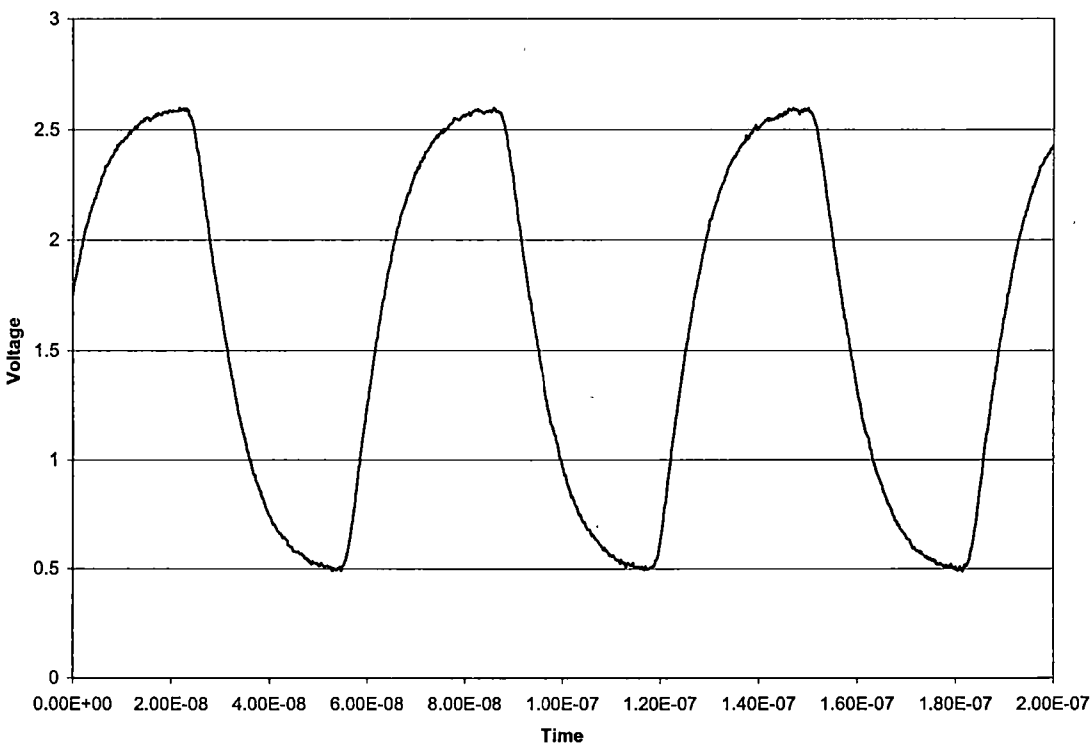


Figure 5.33: Divide-by-16 output at 200 ºC

Overall, the divider performed quite well over temperature, especially considering that the primary design elements in the circuit were standard digital logic cells. All the primary design goals for the divider circuit were met. The duty cycle of the output signal remains stable at 50%, and the division ratio is accurate regardless of the ratio used or temperature. While the slew rate of the physical circuit was considerably less than that predicted by the simulation (Table 4.2), the results demonstrated that the divider is capable of performing acceptably over the complete range of temperature and division ratios. Table 5.6 summarizes the measured slew rate of the divider output.

Table 5.6: Divider measured results

Parameter	25 ºC	200 ºC
Average rising edge slew rate	141.5 V/us	99.8 V/us
Average falling edge slew rate	142.2 V/us	95.7 V/us

5.7 Closed-loop PLL Test Procedures and Results

The complete phase-locked loop prototype was tested to evaluate its performance. To account for differences in measured performance of fabricated components relative to their respective simulation results, appropriate loop filter components were selected based on measured data instead of initial simulations. For instance, the measured gains of the VCO and charge pump were used, instead of their simulated gains, allowing the loop filter to be optimized to the prototyped components. After overcoming some initial difficulties with stability, a series of measurements were performed to document the PLL performance over its full temperature and tuning range.

5.7.1 Initial Testing

Prior to testing the PLL, the loop filter components were determined using measurements from the VCO and charge pump. The measured gain of the VCO was approximately 26.5 MHz/V, and the measured gain of the charge pump was approximately 5.5 uA/V. Using these values, an average division ratio (N) of 300, and desired loop bandwidth of 1.5 kHz, the formulas presented in Section 2.3 were used to determine appropriate component values for the loop filter. These values guided the selection of physical components for the filter, since exact values could not be easily obtained. The initial physical configuration of the loop filter is presented in Table 5.7.

Table 5.7: Initial loop filter component values

Component	Value
C1	0.347 uF
C2	2.20 nF
R	1.5 kΩ

Initial testing was performed using a 1 MHz precision reference signal and the output of the divider as the inputs to the phase detector. The output of the charge pump was connected across the loop filter to the control voltage input on the VCO. The secondary output of the VCO was connected to drive the input of the divider. The divider was configured to use a ratio of 1/300. During these first tests, the loop did not achieve phase lock. Several attempts were made to adjust the biasing of various components, but nothing that was done had any noticeable benefit. Further experimentation revealed several reasons for the inability to achieve phase lock.

5.7.2 Troubleshooting and Optimization

The first major investigation into the loop involved the output of the charge pump. By testing this component outside the loop, it became evident that the reference signal was not triggering the input of the phase detector. The reference signal had a 0-V DC offset, while the phase detector required a signal having an offset voltage centered between the rail voltages of the cell, approximately 1.6 V DC. To remedy this situation, a simple voltage level-shifting circuit was constructed at the board input from the reference source. This allowed a DC offset to be applied to an AC-coupled signal from the reference source, thus bringing the DC level of the reference signal up to a level where it could trigger the phase detector input. After this modification was completed, the charge pump output was again monitored and was deemed to be working correctly. The loop was closed, but the PLL still did not achieve phase lock.

With the free-running VCO still connected to the divider, the output of the divider was observed, and no output signal was present. This led to an inspection of the VCO output voltage drive, relative to the level required to drive the divider input. A mismatch in voltage levels was preventing the VCO from toggling the input flip-flop on the divider. This effect was not observed in simulations, even though the divider was successfully simulated using an input signal with characteristics equivalent to the simulated output of the VCO. To rectify this situation, a separate supply voltage was used for the divider circuit, slightly lower than the supply voltage of the VCO (2.4 V DC compared to 3.3 V DC for the VCO). This allowed the divider to function with smaller peak-to-peak input signals as well as a lower DC offset voltage. After this adjustment was made, the VCO was able to drive the divider, and an appropriate signal was observed at the divider output. The

loop was closed, and the PLL achieved phase lock at 300 MHz. However, a substantial amount of phase noise and jitter was observed in the output signal spectrum.

A series of steps towards alleviating these problems involved modifications to the test board. First, the divider output signal was hard-wired to the appropriate input on the phase detector, using a minimum-length wire on the bottom of the daughterboard instead of an SMA cable between connectors on the test board. Traces leading to the previously-used connectors were cut, thus minimizing the capacitance of the signal path. Secondly, the reference source signal path was re-routed in a similar fashion to the divider output, using a minimum-length wire across the top of the daughterboard. Again, unused traces were cut to minimize the capacitance of the signal path.

Third, the path between the loop filter and the VCO control voltage input was shortened by connecting a wire directly from the control voltage trace, around the side of the daughterboard, to the loop filter on the bottom of the daughterboard. Finally, additional bypass capacitors were added at critical bias points to reduce the noise coming into the system from the power supply lines. A metal ground plane was also soldered to the bottom of the daughterboard, between the loop filter components and the rest of the board, to further reduce noise from the loop filter. These modifications had a positive impact on the phase noise of the PLL. A cleaner output spectrum was observed, and jitter was reduced. A further improvement in phase noise was observed by changing the reference frequency to 18.75 MHz, and reducing the division ratio to 16. The loop filter was also adjusted to reflect the new division ratio by changing the C2 capacitor, as presented in Table 5.8. This maintained a 300 MHz output, but with substantially less

Table 5.8: Final loop filter component values

Component	Value
C1	0.347 uF
C2	0.039 uF
R	1.5 kΩ

phase noise. A simulation of the loop transfer function was also performed to verify the gain and phase margin characteristics of the loop configuration (see Figure 5.34).

5.7.3 Closed-loop Measurements

The phase noise and output power of the closed-loop PLL were measured at several different offset frequencies. In addition, these measurements were repeated at high temperatures using a programmable oven. The primary goal of the temperature tests was to determine the maximum operating temperature of the PLL. Data was collected using several output frequencies, and the results compiled to generate spectral plots.

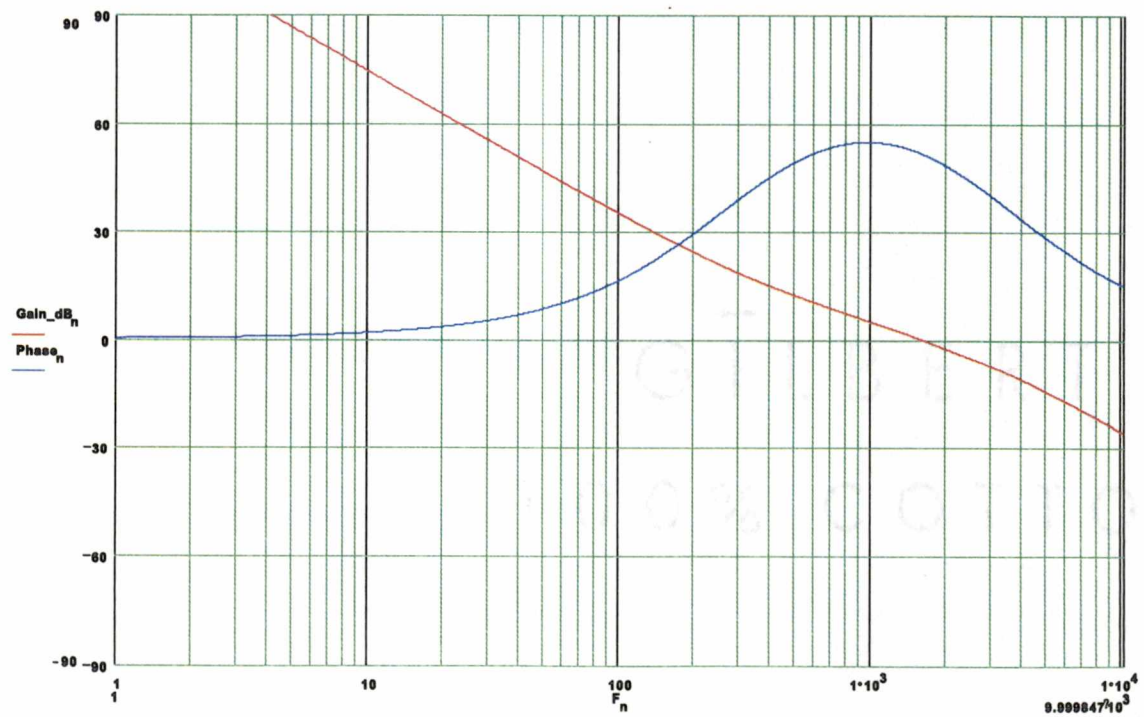


Figure 5.34: Simulated PLL transfer function characteristics

Overall, the measured output spectrum was consistent with expectations based on the VCO open-loop phase noise measurements (see Section 5.5.3). Figures 5.35 through 5.37 present the results of the PLL closed-loop phase noise measurements over temperature. Figure 5.38 shows the PLL output power as a function of temperature.

At approximately 160 ºC, the PLL lost phase lock and the output signal immediately jumped to one of the extremes of the VCO tuning range. Based on the open-loop testing done on the VCO and divider, the reasons for this condition cannot be proven conclusively. However, a possible contributor to the loss of phase lock may be the output signal of the divider. Due to the small device sizes on the divider output, the divider may lack the ability to fully drive the input of the phase detector at higher temperatures.

This theory is supported by the divider test plots in Figures 5.29 through 5.33, which show a noticeable reduction in the slew rate of the divider output as temperature increases. If the load on the divider was increased, the additional capacitance could further reduce the slew rate, until the peak-to-peak output voltage swing from the divider would be insufficient to toggle the input of the phase detector. Another possible cause of the loss of phase lock is the anomaly in the VCO control voltage response curves, shown in Figures 5.17 and 5.18. The substantial deviation in the VCO gain at the points of discontinuity may cause the PLL to become unstable, resulting in the loss of phase lock. However, of these two possibilities, the divider output remains the most probable cause of the loss of phase lock.

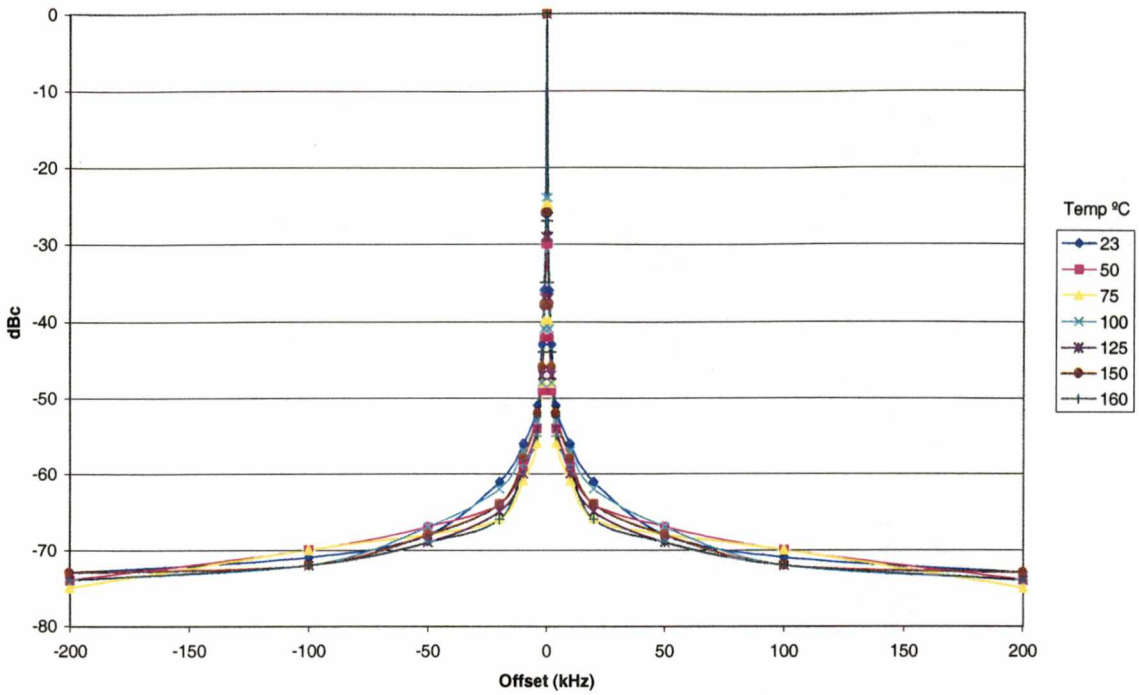


Figure 5.35: PLL 280 MHz output spectrum over temperature

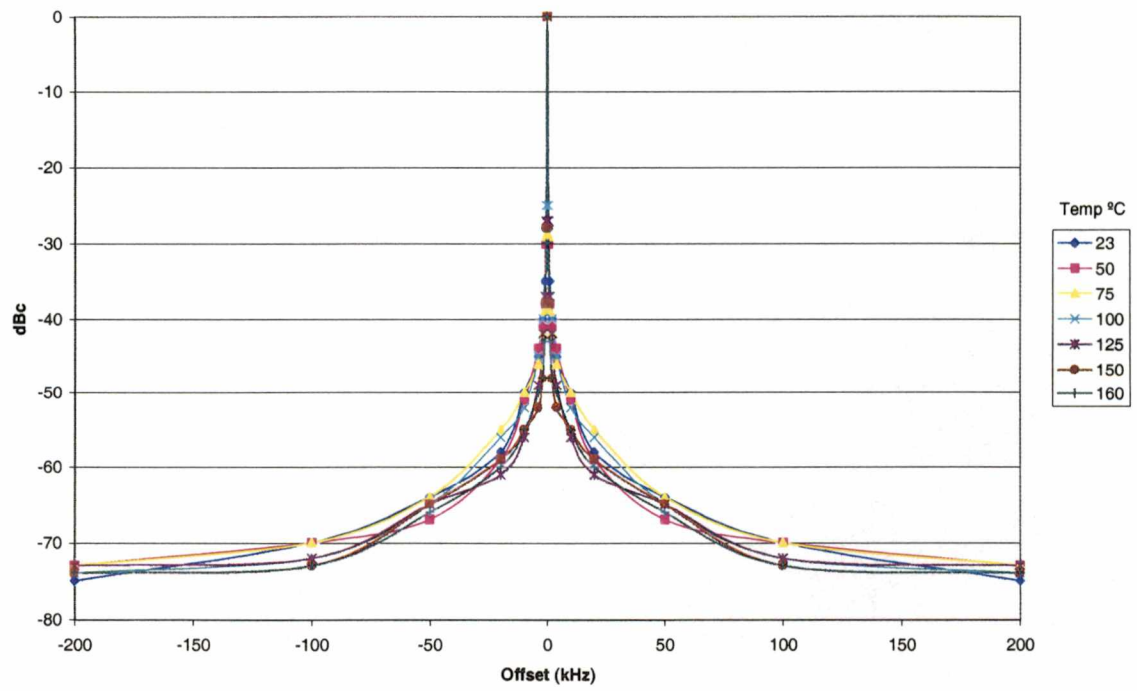


Figure 5.36: PLL 300 MHz output spectrum over temperature

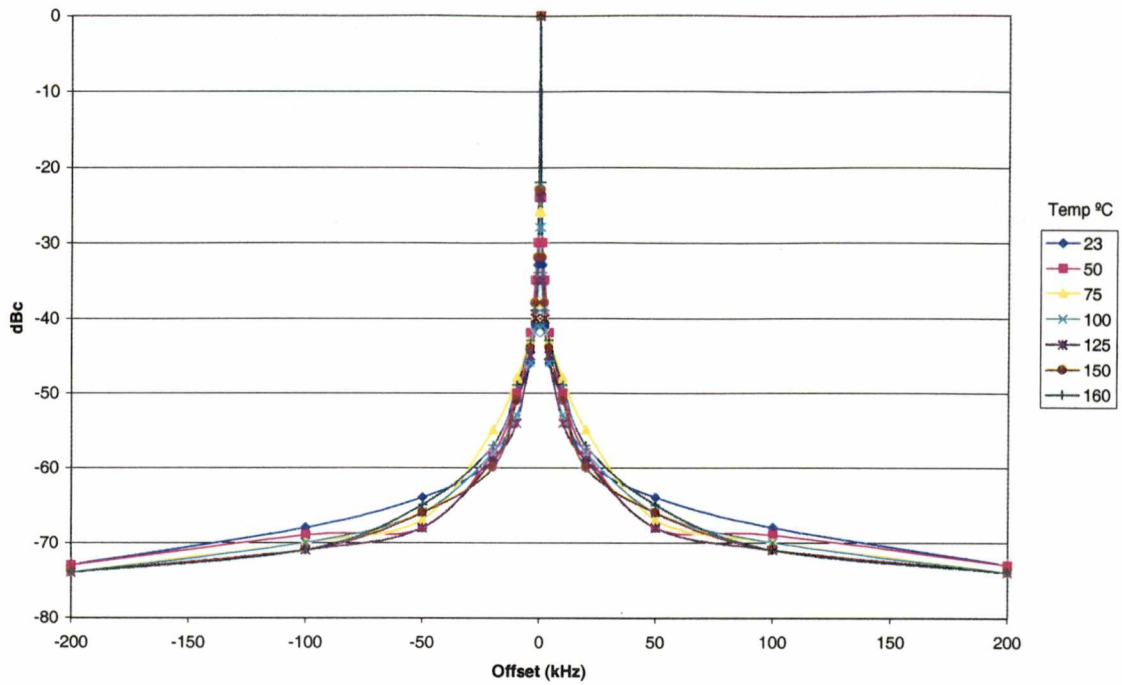


Figure 5.37: PLL 320 MHz output spectrum over temperature

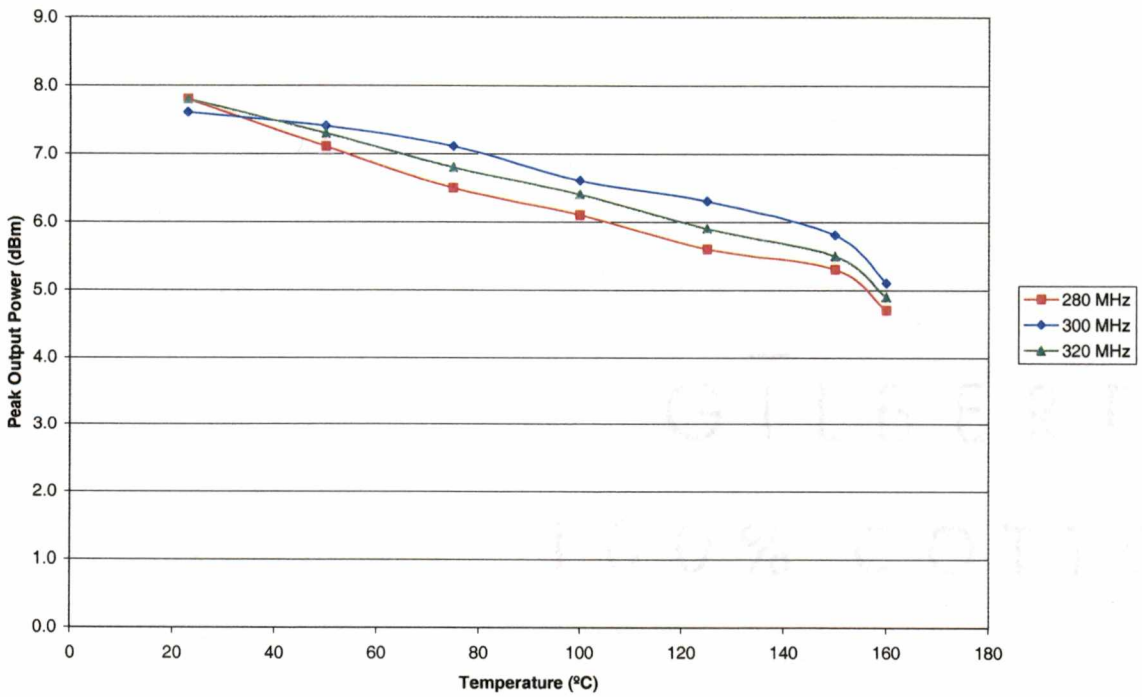


Figure 5.38: PLL output power over temperature

5.7.4 Small-signal Response

The small-signal response of the loop was measured to determine its sensitivity to frequency deviations in the reference source. This test was conducted by monitoring the VCO control voltage while FM modulating the reference source using a 50 kHz deviation with both a 50 Hz square wave and a 500 Hz square wave. A simulation of the small-signal response, based on equations presented in Section 2.3, is presented in Figure 5.39 and shows a slightly underdamped response to a square-wave stimulus. The measured results confirm the simulation, showing a similar response characteristic. Figure 5.40 shows the small-signal response using a 50 Hz square wave, while Figure 5.41 shows the response to a 500 Hz square wave. As expected, the 500 Hz measurements clearly show the effects of the 1.5 kHz loop bandwidth of the PLL, and the effect on the lock time of the system during transitions between frequencies.

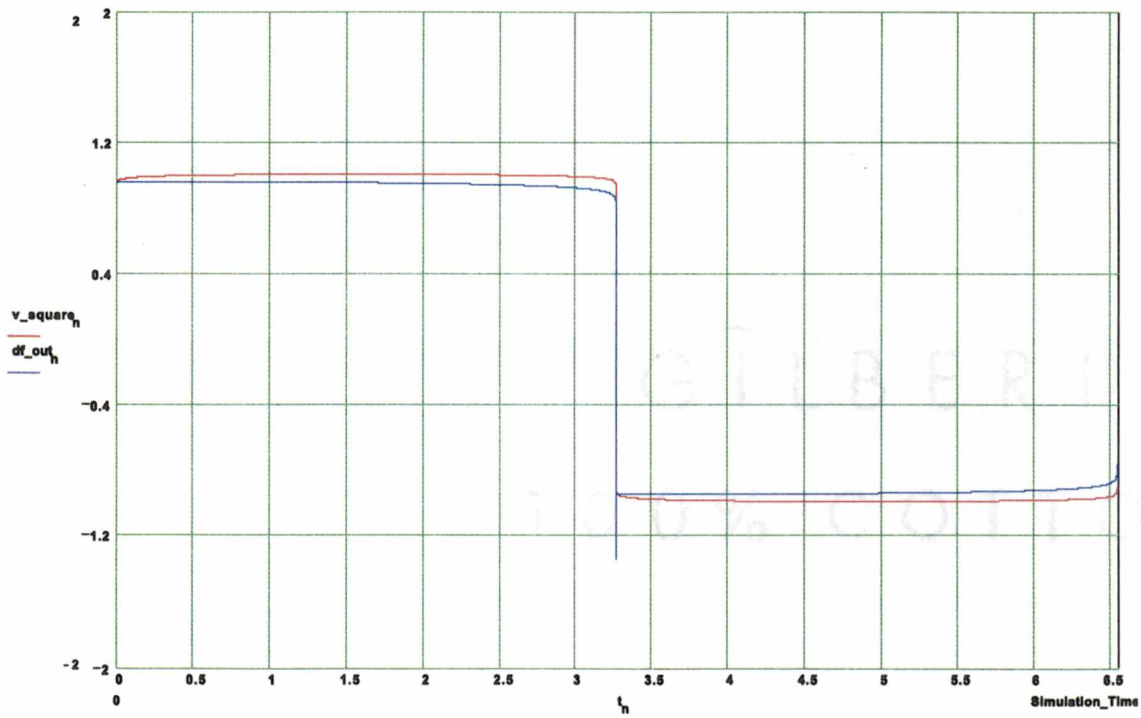


Figure 5.39: Simulated PLL small-signal response

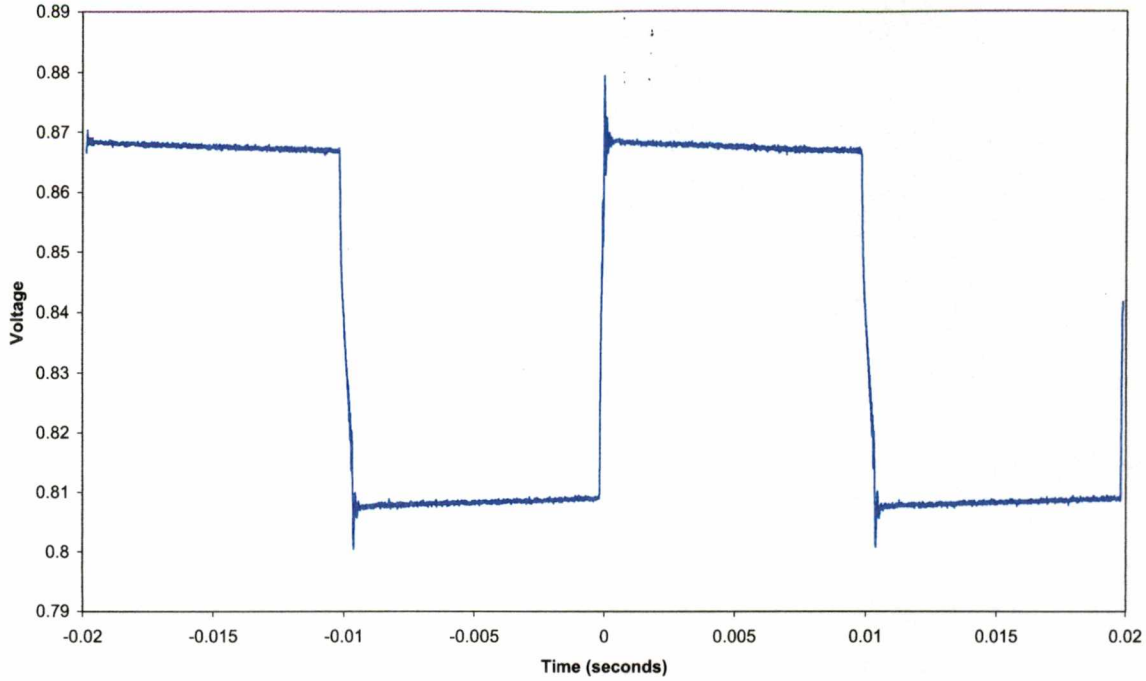


Figure 5.40: Measured PLL small signal response - 50 Hz square wave
VCO Control voltage monitored during FM modulation of reference frequency, 50 kHz deviation

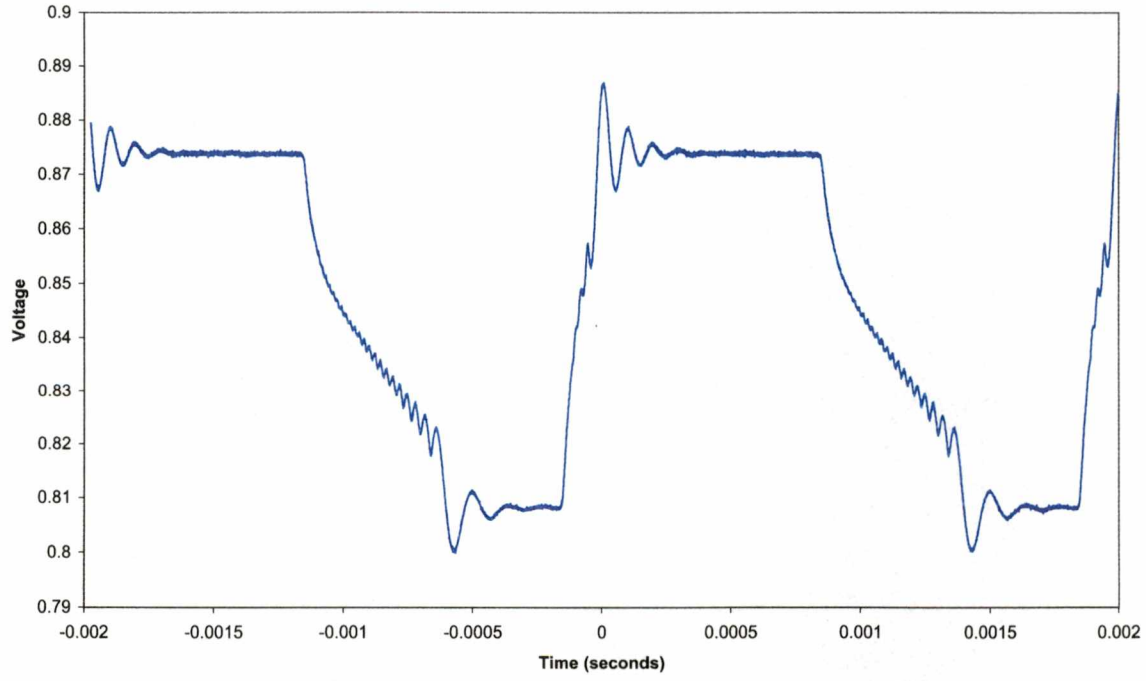


Figure 5.41: Measured PLL small signal response - 50 Hz square wave
VCO Control voltage monitored during FM modulation of reference frequency, 50 kHz deviation

Chapter 6

Conclusions and Future Improvements

A programmable phase-locked loop was designed to operate over a temperature range from 25 to 200 ºC. Specific design issues related to the VCO and programmable frequency divider were analyzed and discussed in detail. Simulation and layout techniques were reviewed, and test results of prototype circuits were presented. This chapter summarizes and compares the results of simulations and prototype measurements, and discusses ideas for future improvements in various aspects of the PLL design.

6.1 Conclusions

Several components of the phase-locked loop were fabricated using the Peregrine Semiconductor 0.5um process. The voltage-controlled oscillator detailed in Chapter 3 used a cross-coupled differential pair architecture with an off-chip resonant tank circuit incorporating varactor diodes as tuning elements. Measurements of the prototyped voltage-controlled oscillator are in agreement with the expected results. The tuning range, output voltage drive and phase noise of the oscillator are all very similar to the results anticipated as a result of hand calculations and computer simulation. In addition, the VCO demonstrated excellent stability over temperature, exhibiting only minimal deviations in operating frequency and phase noise. Results from two independent test boards agreed extremely well, showing consistency across different physical

implementations. A non-linear effect was observed above 175 ºC, which can be traced to a discontinuity in the varactor diode capacitance characteristics.

Measurements of the VCO output drive were slightly higher over temperature than predicted by simulations. This discrepancy is not surprising, and can be attributed to simulation models which do not fully characterize the performance of the physical circuit. Given that many of the manufacturer's measured characteristics for the discrete devices in the tank do not extend above 100 ºC, the performance of the VCO at high temperatures could not be simulated with a high degree of precision. However, the performance of the prototyped circuit demonstrates that the extrapolation of low-temperature model data can yield acceptable results over a wider range of temperatures.

The programmable frequency divider discussed in Chapter 4 used a parallel programming interface, having a minimum division increment of 4, and an allowable division range of 4 up to 512. The architecture of the divider ensured a 50% duty cycle output signal, critical to minimizing the introduction of phase noise into the PLL output. Measured results from the prototyped divider agreed extremely well with simulations, showing a high degree of accuracy in the division ratio, and the ability to function over a very wide temperature range.

The closed-loop PLL system performed very well over temperature, and was capable of accurately tracking the reference frequency. Phase noise and output jitter were minimized by optimizing the loop filter and bias points of the PLL components. Overall, the PLL output phase noise was in line with expectations based on the VCO phase noise

measurements. The PLL successfully achieved high-temperature operation up to 160 ºC, at which point phase lock was lost. However, this can potentially be attributed to the buffer sizes of the divider output, which may have been slew-rate limited due to capacitive loading effects, and thus failed to adequately drive the input to the frequency detector.

As a whole, the PLL performance was fairly consistent with expectations. Both the VCO and frequency divider performed very well and were consistent with predictions from hand calculations and computer simulations, and the closed-loop PLL exhibited good phase noise performance and stability over temperature. However, unforeseen effects such as the VCO discontinuity at high temperatures and the divider output buffering limitation underscored the potential for future improvements to the design.

6.2 Future Improvements

The first area of potential improvement to the design involves the buffering of the programmable frequency divider. Additional devices could be added on-chip to boost the output drive capability of the divider, helping to counteract the slew rate limiting effects that may have contributed to the loss of closed-loop phase lock at higher temperatures. Also, the core logic of the divider could be reevaluated to optimize the latency in the design, potentially increasing the accuracy of the divider across the required division ratios.

A second area of improvement involves the VCO design. Larger buffer transistors could be used, allowing a more substantial output drive capability. This would potentially improve the VCO's ability to drive the divider input, and in turn, the phase noise of the

PLL could be reduced. In conjunction with the VCO design, a detailed thermal characterization of the varactor diode performance would be valuable in predicting anomalies such as the high-temperature discontinuity observed in the current design. Another interesting approach would be to implement all the passive tank components on-chip, including the inductors, capacitors, and varactors. This could offer dramatic improvements in phase noise, as well as improved consistency between separate physical implementations [31, 32].

Finally, optimizations of other PLL components such as the charge pump and loop filter could yield further performance gains. The use of several different phase detector and charge pump architectures could be evaluated. Experimentation with higher-order loop filters could improve the stability of the loop while reducing noise transferred to the VCO input. Overall, the initial designs of the PLL architecture and components presented in this thesis have established a solid, working foundation for the development and implementation of future enhancements.

References

1. Rupert Howes and WIlliam Redman-White, "A Small-Signal Model for the Frequency-Dependent Drain Admittance in Floating-Substrate MOSFET's", IEEE Journal of Solid-State Circuits, Vol. 27, No. 8, August 1992.

2. Bernard Tenbroek, Michael Lee, William Redman-White, R. John Bunyan, and Michael Uren, "Impact of Self-Heating and Thermal Coupling on Analog Circuits in SOI CMOS", IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, July 1998.

3. John Spooner, "New Optical Chips Sparkle for Peregrine", CNET News.com, March 12, 2001 (http://news.cnet.com/news/0-1004-200-5112299.html).

4. John Wetherell, "Phase Locked Loop Design and Analysis", 1997.

5. Phase-Locked Loop Design Fundamentals, Motorola application note AN535, July 1993.

6. Mark Curtin and Paul O'Brien, "Phase-Locked Loops for High-Frequency Receivers and Transmitters", Analog Dialogue Vol. 33, 1999.

7. R. K. Feeney and D. R. Hertling, "Fundamentals of Frequency Synthesis and Phase-Locked Loops", 1997.

8. Behzad Rezavi, RF Microelectronics, Prentice Hall, 1998.

9. Bernard Sklar, Digital Communications: Fundamentals and Applications, Prentice Hall, 1988.

10. Ali Hajimiri and Thomas H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", IEEE Journal of Solid-State Circuits, Vol. 33, No. 2, February 1998.

11. A. Bruce Carlson, Communication Systems: An Introduction to Signals and Noise in Electrical Communication, McGraw Hill, 1986.

12. William B. Wilson, "A CMOS Self-Calibrating Frequency Synthesizer", IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000.

13. Ali Hajimiri, Sotirios Limotyrakis, and Thomas H. Lee, "Jitter and Phase Noise In Ring Oscillators", IEEE Journal of Solid-State Circuits, Vol. 34, No. 6, June 1999.

14. Thomas H. Lee and Ali Hajimiri, "Oscillator Phase Noise: A Tutorial", IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000.

15. Richard C. Jaeger, Microelectronic Circuit Design, McGraw-Hill, 1997.

16. Varactor SPICE Models for RF VCO Applications, Alpha Industries application note APN1004.

17. Hyperabrupt Tuning Varactors, Alpha Industries product data sheet SMV1232-SMV1237.

18. Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.

19. James Arnott, A Voltage Controlled Oscillator Realized in 0.5um CMOS Technology for a Wireless Bioluminescent Bioreporter Integrated Circuit, Master's Thesis, University of Tennessee, 1999.

20. Paul R. Gray and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, 1993.

21. David A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997.

22. Ali Hajimiri, Thomas H. Lee, "Phase Noise in CMOS Differential L-C Oscillators", Stanford University Center for Integrated Systems publication, undated.

23. Ali Hajimiri and Thomas H. Lee, "Design Issues in CMOS Differential LC Oscillators", IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999.

24. John W. Rogers, Jose A. Macedo, and Calvin Plett, "The Effect of Varactor Nonlinearity on the Phase Noise of Completely Integrated VCOs", IEEE Journal of Solid-State Circuits, Vol. 35, No. 9, September 2000.

25. Temperature Effects On Silicon Semiconductor Devices, Zetex Design Note 4, Issue 2, June 1995.

26. Software Application: HSPICE, Version 98.2 (980711), Avant! Corporation, 1985-1997

27. Software Application: MAGIC Version 6.5.1 ORNL 1.1, University of California, Berkeley.

28. Software Application: PowerView Version 6.1, Innoveda Software, Inc., 1997.

29. Software Library: ITD/AuE Standard-cell Library, Microsystems Processing Laboratory, Mississippi State University, 1995-1998.

30. Charles L. Britton, Personal communication, 1999-2001.

31. Hirad Samavati, Ali Hajimiri, Arvin Shahani, Gitty Nasserbakht, and Thomas H. Lee, "Fractal Capacitors", IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998.

32. Thomas H. Lee, "CMOS RF: No Longer an Oxymoron", Stanford University Center for Integrated Systems publication, undated.

Appendices

Appendix A: Pre-layout HSPICE Simulation Files

A.1: VCO Pre-layout HSPICE Simulation File

```
* vco_pre.cir
*
* Peregrine model files
.include cdh_ttt.lp0


************************
* Varactor diode model *
************************
.model SMV1236 D
+IS=1E-14
+RS=0
+N=1
+CJO=21.63E-12
+VJ=8
+M=4.2
+EG=1.11
+XTI=3
+KF=0
+AF=1
+FC=0.50
+BV=0
+IBV=1E-3

*****************************
* Varactor subcircuit model *
*****************************
.subckt VAR 1 2
Dv3 1 SMV1236
Rsv3 4 0.5
Lsv4 2 1.7n
Cpv1 2 3.2p
.ends VAR




*****************
* MAIN CIRCUIT *
*****************


****
* Voltage sources

vdd100 0 3.3
vcont200 0 3



****
* Off-chip components

L1100 1 18n
L2100 2 18n
C11 7 22p
C22 8 22p
R1200 7 2.2k
R2200 8 2.2k
X17 0 VAR
X28 0 VAR
* Tank bias current
RB1100 9 1.5k
* Output bias current (osc gain)
RB2100 4 20k
* Output loads
RL16 0 50
RL2     5 0 51


****
```

```
* Parasitics
Cp11 0 3.0p
Cp22 0 3.0p


****
* On-chip components

*   Tank
M11 2 3 0 nl w=35u l=0.5u m=2
M22 1 3 0 nl w=35u l=0.5u m=2
*   Tank bias (uses RB2)
M33 4 0 0 nl w=35u l=0.5u m=3
M44 4 0 0 nl w=35u l=0.5u
*   Active load for tank output
M5100 1 5 5 nl w=21u l=0.5u m=12
M6100 2 6 6 nl w=21u l=0.5u m=12
*   Active load bias (uses RB1)
M75 9 0 0 nl w=21u l=0.5u m=10
M86 9 0 0 nl w=21u l=0.5u m=5
M99 9 0 0 nl w=14u l=0.5u m=2


* PRIMARY OUTPUT IS NODE 6

.temp 25 75 125 175 200
.tran .1n 600n 500n .1n
.options POST
.options METHOD=GEAR
.end
```

A.2: Divider Pre-layout ViewSim Simulation Source File

```
V 6.0
|
| Wirelist created using VIEWSIM WIRELISTER 6.0
| Using initialization file '/usr/local/view/standard/vsm.ini'
|    Using 24 attribute filter(s)
| Long format VIEWSIM file for project DIVIDER_2
|
DW DIVIDER_2 35 195238070000
I #! $TRIG0
I ## $TRIG1
I #$ VDD
I #% GND
I #& $XXX
I #' $ZZZ
I #* $1N539
NA #* ( C )
I #+ $1N543
NA #+ ( C )
I #- $1N558
NA #- ( C )
I #. F_IN
NA #. ( C )
M $1I281 SMV ( LAYOUT_GENERATOR="\STDCELL -F -FLATTEN -R4" SIVMASTER=DIVIDER_2 +
 STRUCTURE_PROCESSOR )
I #/ $1N325
I #0 $1N540
I #1 $1N108
M $1I317 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #/ #* #0 #1 #/
I #2 $1N549
I #3 $1N342
I #4 RESET
I #5 $1N502
M $1I353 MUXF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:MUXF201 ) #2 #3 #4 #5
M $1I356 PUDF000 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:PUDF000 ) #2
I #6 $1N92
I #7 $1N321
M $1I37 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #1 #6 #7
I #8 $1N94
I #9 $1N106
I #? $1N72
M $1I38 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #8 #9 #?
I #@ $1N96
I #A $1N115
I #B $1N74
M $1I39 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #@ #A #B
I #C $1N98
I #D $1N334
I #E $1N77
M $1I40 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #C #D #E
I #F $1N100
I #G $1N124
I #H $1N82
M $1I41 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #F #G #H
I #I $1N102
I #J $1N537
I #K $1N85
M $1I42 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #I #J #K
M $1I45 NANF211 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NANF211 ) #6 #1 ? #9
I #L $1N201
I #M $1N199
I #N $1N195
I #O $1N184
I #P $1N186
I #Q $1N188
```

```
I #R $1N190
I #S $1N464
M $1I460 NANF811 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NANF811 ) #L #M #N #N #O #P #Q #R #S ?
I #T D7
M $1I471 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #T #I #N
I #U D6
M $1I472 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #U #F #M
I #V D5
M $1I473 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #V #C #L
I #W D4
M $1I474 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #W #@ #R
I #X D3
M $1I475 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #X #8 #Q
I #Y D2
M $1I476 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #Y #6 #P
I #Z D1
M $1I477 XORF201 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:XORF201 ) #Z #1 #O
M $1I478 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #7 #* #0 #6 ?
M $1I48 NANF211 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NANF211 ) #C #D ? #G
M $1I49 NANF211 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NANF211 ) #F #G ? #J
M $1I490 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #? #* #0 #8 ?
M $1I491 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #B #* #0 #@ ?
M $1I492 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #E #* #0 #C ?
M $1I493 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #H #* #0 #F ?
M $1I494 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #K #* #0 #I ?
I #\ $1N498
I #^ $1N447
I #_ F_OUT
M $1I497 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #\ #^ #4 #_ #\
M $1I501 INVF103 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:INVF103 ) #5 #0
M $1I505 NANF311 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NANF311 ) #8 #6 #1 ? #A
M $1I506 NANF411 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NANF411 ) #@ #8 #6 #1 ? #D
M $1I533 NORF211 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:NORF211 ) #S #* #3 #^
I #` $1N371
M $1I542 DFRF312 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:DFRF312 ) #+ #- #` #* #+
M $1I550 PUDF000 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:PUDF000 ) #`
M $1I555 BUFF101 ( CELLIBTYPE=\STDCELL NEW_SYMBOL SIMMODEL=VHDL +
 VHDL=STDCELL:BUFF101 ) #. #-
WD
```

A.3: Divider Pre-layout ViewSim Simulation Command File

```
wave divider_2.wfm F_IN D1 D2 D3 D4 D5 D6 D7 F_OUT
clock F_IN 0 1
stepsize 3ns
l D1 D2 D3 D4 D5 D6 D7
l RESET
c 10
h RESET
c 10
l RESET
c 10
h D1
l D7 D6 D5 D4 D3 D2
c 500
h D4 D2 D1
l D7 D6 D5 D3
c 500
h D5 D3 D1
l D7 D6 D4 D2
c 500
h D5 D4 D3 D2 D1
l D7 D6
c 500
h D6 D4 D1
l D7 D5 D3 D2
c 500
```

Appendix B: Post-layout HSPICE Simulation Files

B.1: VCO Post-layout HSPICE Simulation File

```
* vco_post.cir
*
* Peregrine model files
.include cdh_ttt.1p0
.param MM=0
*
****** top level cell is /users2/students/moorap/iclayout/prgr/vco/vco_v2.ext
M1 1 2 3 Vsan! NL M=2 W=35.00U L=0.50U AD=87.50P PD=75.00U AS=57.50P PS=43.29U
M2 2 1 3 Vsan! NL M=2 W=35.00U L=0.50U AD=87.50P PD=75.00U AS=57.50P PS=43.29U
M3 3 4 999 Vsan! NL M=3 W=35.00U L=0.50U AD=57.50P PD=43.29U AS=62.14P PS=49.93U
M4 4 4 999 Vsan! NL W=35.00U L=0.50U AD=87.50P PD=75.00U AS=62.14P PS=49.93U
M5 100 2 5 Vsan! NL M=12 W=21.00U L=0.50U AD=31.50P PD=24.00U AS=33.41P PS=26.09U
M6 6 1 101 Vsan! NL M=12 W=21.00U L=0.50U AD=35.21P PD=28.06U AS=31.50P PS=24.00U
M7 5 9 999 Vsan! NL M=10 W=21.00U L=0.50U AD=33.41P PD=26.09U AS=37.28P PS=29.96U
M8 6 9 999 Vsan! NL M=5 W=21.00U L=0.50U AD=35.21P PD=28.06U AS=37.28P PS=29.96U
M9 9 9 999 Vsan! NL M=2 W=14.00U L=0.50U AD=35.00P PD=33.00U AS=24.86P PS=19.97U
*** Node Listing for subckt:  vco_v2
** N0                          ==  IdealGND
**                    [HIDE]    ==  ox_n185_110#
**                    [HIDE]    ==  ox_265_n60#
**                    [HIDE]    ==  ox_n185_220#
**                    [HIDE]    ==  ox_n75_n365#
**                    [HIDE]    ==  ox_n475_n400#
**                    [HIDE]    ==  ox_380_n330#
**                    [HIDE]    ==  ox_155_n400#
**                    [HIDE]    ==  ox_n470_n60#
** N1                 [U=3]     ==  N1
** N2                 [U=3]     ==  N2
** N3                 [U=3]     ==  N3
** N4                 [U=3]     ==  N4
** N5                 [U=2]     ==  N5
** N6                 [U=2]     ==  OUTPUT
** N9                 [U=4]     ==  N9
** N100               [U=1]     ==  VDD1
** N101               [U=1]     ==  VDD2
** N999               [U=5]     ==  GND1
****************************************************************
** Vsan!              [U=9]
****************************************************************
*
* Model Definitions for PSPICE
*
****************************************************************



************************
* Varactor diode model *
************************
.model SMV1236 D
+IS=1E-14
+RS=0
+N=1
+CJO=21.63E-12
+VJ=8
+M=4.2
+EG=1.11
+XTI=3
+KF=0
+AF=1
+FC=0.50
+BV=0
+IBV=1E-3

*****************************
* Varactor subcircuit model *
*****************************
.subckt VAR 1 2
Dv3 1 SMV1236
Rsv3 4 0.5
Lsv4 2 1.7n
Cpv1 2 3.2p
.ends VAR
```

```
*****************
* MAIN CIRCUIT *
*****************


****
* Voltage sources

vdd100 0 3.3
vcont200 0 3
rdd100 101 0
rgnd999 0 0



****
* Off-chip components

L1100 1 18n
L2100 2 18n
C11 7 22p
C22 8 22p
R1200 7 2.2k
R2200 8 2.2k
X17 0 VAR
X28 0 VAR
* Tank bias current
RB1100 9 1.5k
* Output bias current (osc gain)
RB2100 4 20k
* Output load
RL16 0 55
RL25 0 50
* Parasitics
Cp11 0 3p
Cp22 0 3p



* PRIMARY OUTPUT IS NODE 6


*.op
.temp 25 75 125 175 200
.tran .1n 10100n 10000n .1n
.options POST
.options METHOD=GEAR

.END
```

B.2: Divider Post-layout HSPICE Simulation File

```
* divider_2.spice
*
* File Location         /users2/students/moorap/iclayout/prgr/divider/prgr-conv
* File Created          Fri Jan 28 16:25:16 2000
* Ext2spice Version     OrnL 2.6.4 <=> Tue Jan 27 17:32:51 EST 1998
*           Options     -m -n -M -N -mm
*

** Subcircuit definition for norf211
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
norf211.ext
.SUBCKT norf211 1 2 5 6 7 8 10
M1 1 2 3 Vsap! rp W=15.00U L=0.50U AD=11.09P PD=11.74U AS=0.00P PS=0.00U
M2 3 5 6 Vsap! rp W=15.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M3 6 1 7 Vsap! rp W=15.50U L=0.50U AD=0.00P PD=0.00U AS=13.76P PS=14.60U
M4 8 2 1 Vsan! rn W=4.00U L=0.50U AD=14.29P PD=15.37U AS=2.96P PS=3.13U
M5 1 5 8 Vsan! rn W=4.00U L=0.50U AD=2.96P PD=3.13U AS=14.29P PS=15.37U
M6 8 1 7 Vsan! rn W=8.50U L=0.50U AD=30.37P PD=32.66U AS=7.54P PS=8.00U
*** Node Listing for subckt:  norf211
** N0                          ==  IdealGND
** N1                [U=6]     ==  O2
** N2                [U=3]     ==  A1
** N3                [U=2]     ==  120
** N5                [U=3]     ==  B1
** N6                [U=3]     ==  VddX
** N7                [U=3]     ==  O1
** N8                [U=4]     ==  GNDX
** N10               [U=1]     ==  w_n15_165#
************************************************************
** Vsan!             [U=3]
** Vsap!             [U=3]
.ENDS

** Subcircuit definition for invf103
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
invf103.ext
.SUBCKT invf103 1 2 3 5 7
M1 1 2 3 Vsap! rp M=3 W=12.50U L=0.50U AD=8.38P PD=8.20U AS=0.00P PS=0.00U
M2 1 2 5 Vsan! rn M=3 W=6.00U L=0.50U AD=4.02P PD=3.94U AS=14.93P PS=14.53U
*** Node Listing for subckt:  invf103
** N0                          ==  IdealGND
** N1                [U=3]     ==  O
** N2                [U=3]     ==  A1
** N3                [U=2]     ==  VddX
** N5                [U=2]     ==  GNDX
** N7                [U=1]     ==  w_n15_165#
************************************************************
** Vsan!             [U=1]
** Vsap!             [U=1]
.ENDS

** Subcircuit definition for muxf201
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
muxf201.ext
.SUBCKT muxf201 1 3 5 8 10 11 15
M1 1 2 3 Vsap! rp W=11.50U L=0.50U AD=11.75P PD=12.06U AS=0.00P PS=0.00U
M2 3 5 6 Vsap! rp W=13.50U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M3 6 7 2 Vsap! rp W=13.50U L=0.50U AD=0.00P PD=0.00U AS=6.84P PS=6.39U
M4 2 8 9 Vsap! rp W=13.50U L=0.50U AD=6.84P PD=6.39U AS=0.00P PS=0.00U
M5 9 10 3 Vsap! rp W=13.50U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M6 3 10 7 Vsap! rp W=9.50U L=0.50U AD=0.00P PD=0.00U AS=9.75P PS=10.51U
M7 1 2 11 Vsan! rn W=7.00U L=0.50U AD=7.15P PD=7.34U AS=13.91P PS=12.81U
M8 11 5 13 Vsan! rn W=5.50U L=0.50U AD=10.93P PD=10.06U AS=4.12P PS=7.00U
M9 13 10 2 Vsan! rn W=5.50U L=0.50U AD=4.12P PD=7.00U AS=2.79P PS=2.61U
M10 2 8 14 Vsan! rn W=5.50U L=0.50U AD=2.79P PD=2.61U AS=4.12P PS=7.00U
M11 14 7 11 Vsan! rn W=5.50U L=0.50U AD=4.12P PD=7.00U AS=10.93P PS=10.06U
M12 11 10 7 Vsan! rn W=5.50U L=0.50U AD=10.93P PD=10.06U AS=5.65P PS=6.09U
*** Node Listing for subckt:  muxf201
** N0                          ==  IdealGND
** N1                [U=3]     ==  O
** N2                [U=6]     ==  20
** N3                [U=5]     ==  VddX
** N5                [U=3]     ==  A1
** N6                [U=2]     ==  120
```

```
** N7                [U=4]     ==  22
** N8                [U=3]     ==  B2
** N9                [U=2]     ==  121
** N10               [U=5]     ==  SEL3
** N11               [U=5]     ==  GNDX
** N13               [U=2]     ==  150
** N14               [U=2]     ==  151
** N15               [U=1]     ==  w_n15_165#
*************************************************************
** Vsan!             [U=6]
** Vsap!             [U=6]
.ENDS

** Subcircuit definition for nanf811
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
nanf811.ext
.SUBCKT nanf811 2 3 5 7 9 10 11 12 13 14 15 16
M1 1 2 3 Vsap! rp W=5.00U L=0.50U AD=8.30P PD=6.19U AS=0.00P PS=0.00U
M2 3 1 5 Vsap! rp W=15.00U L=0.50U AD=0.00P PD=0.00U AS=15.11P PS=16.19U
M3 3 5 6 Vsap! rp W=15.00U L=0.50U AD=0.00P PD=0.00U AS=15.11P PS=16.19U
M4 2 7 1 Vsan! rn W=11.50U L=0.50U AD=24.61P PD=18.08U AS=19.09P PS=14.23U
M5 1 9 2 Vsan! rn W=11.50U L=0.50U AD=19.09P PD=14.23U AS=24.61P PS=18.08U
M6 2 10 1 Vsan! rn W=11.50U L=0.50U AD=24.61P PD=18.08U AS=19.09P PS=14.23U
M7 1 11 2 Vsan! rn W=11.50U L=0.50U AD=19.09P PD=14.23U AS=24.61P PS=18.08U
M8 2 12 1 Vsan! rn W=11.50U L=0.50U AD=24.61P PD=18.08U AS=19.09P PS=14.23U
M9 1 13 2 Vsan! rn W=11.50U L=0.50U AD=19.09P PD=14.23U AS=24.61P PS=18.08U
M10 2 14 1 Vsan! rn W=11.50U L=0.50U AD=24.61P PD=18.08U AS=19.09P PS=14.23U
M11 1 15 2 Vsan! rn W=11.50U L=0.50U AD=19.09P PD=14.23U AS=24.61P PS=18.08U
M12 2 1 5 Vsan! rn W=11.50U L=0.50U AD=24.61P PD=18.08U AS=11.59P PS=12.41U
M13 2 5 6 Vsan! rn W=11.50U L=0.50U AD=24.61P PD=18.08U AS=11.59P PS=12.41U
*** Node Listing for subckt:  nanf811
** N0                          ==  IdealGND
** N1                [U=11]    ==  N1
** N2                [U=12]    ==  GNDX
** N3                [U=4]     ==  VddX
** N5                [U=5]     ==  O1
** N6                [U=2]     ==  O2
** N7                [U=2]     ==  A1
** N9                [U=2]     ==  B1
** N10               [U=2]     ==  C1
** N11               [U=2]     ==  D1
** N12               [U=2]     ==  E1
** N13               [U=2]     ==  F1
** N14               [U=2]     ==  G1
** N15               [U=2]     ==  H1
** N16               [U=1]     ==  w_n15_165#
*************************************************************
** Vsan!             [U=10]
** Vsap!             [U=3]
.ENDS

** Subcircuit definition for nanf311
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
nanf311.ext
.SUBCKT nanf311 2 3 5 6 7 11 12
M1 1 2 3 Vsap! rp W=12.00U L=0.50U AD=7.84P PD=7.17U AS=0.00P PS=0.00U
M2 3 5 1 Vsap! rp W=12.00U L=0.50U AD=0.00P PD=0.00U AS=7.84P PS=7.17U
M3 1 6 3 Vsap! rp W=12.00U L=0.50U AD=7.84P PD=7.17U AS=0.00P PS=0.00U
M4 3 1 7 Vsap! rp W=12.50U L=0.50U AD=0.00P PD=0.00U AS=13.12P PS=12.88U
M5 1 2 8 Vsan! rn W=11.50U L=0.50U AD=7.52P PD=6.88U AS=8.62P PS=13.00U
M6 8 5 10 Vsan! rn W=11.50U L=0.50U AD=8.62P PD=13.00U AS=8.62P PS=13.00U
M7 10 6 11 Vsan! rn W=11.50U L=0.50U AD=8.62P PD=13.00U AS=22.67P PS=18.16U
M8 11 1 7 Vsan! rn W=7.50U L=0.50U AD=14.78P PD=11.84U AS=7.88P PS=7.72U
*** Node Listing for subckt:  nanf311
** N0                          ==  IdealGND
** N1                [U=6]     ==  O1
** N2                [U=3]     ==  C1
** N3                [U=5]     ==  VddX
** N5                [U=3]     ==  B1
** N6                [U=3]     ==  A1
** N7                [U=3]     ==  O2
** N8                [U=2]     ==  150
** N10               [U=2]     ==  151
** N11               [U=3]     ==  GNDX
** N12               [U=1]     ==  w_n15_165#
*************************************************************
** Vsan!             [U=4]
```

```
** Vsap!              [U=4]
.ENDS

** Subcircuit definition for nanf411
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
nanf411.ext
.SUBCKT nanf411 1 2 5 6 7 8 13 14
M1 1 2 3 Vsap! rp W=8.50U L=0.50U AD=0.00P PD=0.00U AS=4.62P PS=5.56U
M2 3 5 1 Vsap! rp W=8.50U L=0.50U AD=4.62P PD=5.56U AS=0.00P PS=0.00U
M3 1 6 3 Vsap! rp W=8.50U L=0.50U AD=0.00P PD=0.00U AS=4.62P PS=5.56U
M4 3 7 1 Vsap! rp W=8.50U L=0.50U AD=4.62P PD=5.56U AS=0.00P PS=0.00U
M5 1 3 8 Vsap! rp W=11.50U L=0.50U AD=0.00P PD=0.00U AS=11.67P PS=14.15U
M6 3 2 9 Vsan! rn W=12.50U L=0.50U AD=6.79P PD=8.17U AS=9.38P PS=14.00U
M7 9 5 11 Vsan! rn W=12.50U L=0.50U AD=9.38P PD=14.00U AS=9.38P PS=14.00U
M8 11 6 12 Vsan! rn W=12.50U L=0.50U AD=9.38P PD=14.00U AS=9.38P PS=14.00U
M9 12 7 13 Vsan! rn W=12.50U L=0.50U AD=9.38P PD=14.00U AS=32.11P PS=31.55U
M10 13 3 8 Vsan! rn W=8.50U L=0.50U AD=21.84P PD=21.45U AS=8.63P PS=10.46U
*** Node Listing for subckt:  nanf411
** N0                          ==  IdealGND
** N1                [U=6]     ==  VddX
** N2                [U=3]     ==  D1
** N3                [U=7]     ==  O1
** N5                [U=3]     ==  C1
** N6                [U=3]     ==  B1
** N7                [U=3]     ==  A1
** N8                [U=3]     ==  O2
** N9                [U=2]     ==  150
** N11               [U=2]     ==  151
** N12               [U=2]     ==  152
** N13               [U=3]     ==  GNDX
** N14               [U=1]     ==  w_n15_165#
************************************************************
** Vsan!             [U=5]
** Vsap!             [U=5]
.ENDS

** Subcircuit definition for buff101
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
buff101.ext
.SUBCKT buff101 2 3 5 6 8
M1 1 2 3 Vsap! rp W=5.50U L=0.50U AD=6.70P PD=9.21U AS=0.00P PS=0.00U
M2 3 1 5 Vsap! rp W=15.50U L=0.50U AD=0.00P PD=0.00U AS=13.46P PS=14.25U
M3 1 2 6 Vsan! rn W=2.50U L=0.50U AD=3.05P PD=4.19U AS=7.29P PS=7.14U
M4 6 1 5 Vsan! rn W=8.00U L=0.50U AD=23.31P PD=22.86U AS=6.94P PS=7.35U
*** Node Listing for subckt:  buff101
** N0                          ==  IdealGND
** N1                [U=4]     ==  21
** N2                [U=3]     ==  A1
** N3                [U=3]     ==  VddX
** N5                [U=3]     ==  O
** N6                [U=3]     ==  GNDX
** N8                [U=1]     ==  w_n15_165#
************************************************************
** Vsan!             [U=2]
** Vsap!             [U=2]
.ENDS

** Subcircuit definition for nanf211
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
nanf211.ext
.SUBCKT nanf211 1 2 5 6 9 10
M1 1 2 3 Vsap! rp W=11.50U L=0.50U AD=0.00P PD=0.00U AS=8.36P PS=9.06U
M2 3 5 1 Vsap! rp W=11.50U L=0.50U AD=8.36P PD=9.06U AS=0.00P PS=0.00U
M3 1 3 6 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=13.39P PS=13.39U
M4 3 2 7 Vsan! rn W=10.50U L=0.50U AD=7.63P PD=8.27U AS=7.88P PS=12.00U
M5 7 5 9 Vsan! rn W=10.50U L=0.50U AD=7.88P PD=12.00U AS=30.48P PS=22.80U
M6 9 3 6 Vsan! rn W=7.00U L=0.50U AD=20.32P PD=15.20U AS=7.21P PS=7.21U
*** Node Listing for subckt:  nanf211
** N0                          ==  IdealGND
** N1                [U=4]     ==  VddX
** N2                [U=3]     ==  A1
** N3                [U=5]     ==  O1
** N5                [U=3]     ==  B1
** N6                [U=3]     ==  O2
** N7                [U=2]     ==  150
** N9                [U=3]     ==  GNDX
** N10               [U=1]     ==  w_n15_165#
```

```
**************************************************************
** Vsan!              [U=3]
** Vsap!              [U=3]
.ENDS

** Subcircuit definition for pudf000
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
pudf000.ext
.SUBCKT pudf000 1 2 3 5
M1 1 2 3 Vsan! rn W=2.00U L=15.00U AD=9.40P PD=13.40U AS=5.60P PS=9.60U
*** Node Listing for subckt:  pudf000
** N0                          ==  IdealGND
** N1                [U=2]     ==  GNDX
** N2                [U=2]     ==  VddX
** N3                [U=2]     ==  O
** N5                [U=1]     ==  w_n15_310#
**************************************************************
** Vsan!              [U=1]
.ENDS

** Subcircuit definition for dfrf312
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
dfrf312.ext
.SUBCKT dfrf312 1 2 6 12 17 20 21 26
M1 1 2 3 Vsap! rp M=2 W=14.50U L=0.50U AD=0.00P PD=0.00U AS=11.49P PS=8.48U
M2 1 3 5 Vsap! rp M=2 W=14.50U L=0.50U AD=0.00P PD=0.00U AS=11.49P PS=8.48U
M3 1 6 7 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M4 7 3 8 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=9.61P PS=7.60U
M5 8 9 10 Vsap! rp W=13.00U L=0.50U AD=9.61P PD=7.60U AS=0.00P PS=0.00U
M6 10 5 1 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M7 1 8 11 Vsap! rp W=14.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M8 11 12 9 Vsap! rp W=14.00U L=0.50U AD=0.00P PD=0.00U AS=13.89P PS=11.29U
M9 1 5 13 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M10 13 9 14 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=9.61P PS=7.51U
M11 14 3 15 Vsap! rp W=13.00U L=0.50U AD=9.61P PD=7.51U AS=0.00P PS=0.00U
M12 15 16 1 Vsap! rp W=13.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M13 17 2 3 Vsan! rn M=2 W=12.00U L=0.50U AD=32.12P PD=24.33U AS=9.51P PS=7.02U
M14 17 3 5 Vsan! rn M=2 W=12.00U L=0.50U AD=32.12P PD=24.33U AS=9.51P PS=7.02U
M15 1 14 19 Vsap! rp W=16.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M16 19 12 16 Vsap! rp W=16.00U L=0.50U AD=0.00P PD=0.00U AS=15.03P PS=12.06U
M17 1 14 20 Vsap! rp W=16.50U L=0.50U AD=0.00P PD=0.00U AS=13.39P PS=15.61U
M18 1 20 21 Vsap! rp W=15.50U L=0.50U AD=0.00P PD=0.00U AS=12.47P PS=14.91U
M19 17 5 22 Vsan! rn W=9.50U L=0.50U AD=25.43P PD=19.26U AS=7.12P PS=11.00U
M20 22 6 8 Vsan! rn W=9.50U L=0.50U AD=7.12P PD=11.00U AS=7.02P PS=5.55U
M21 8 3 23 Vsan! rn W=9.00U L=0.50U AD=6.65P PD=5.26U AS=6.75P PS=10.50U
M22 23 9 17 Vsan! rn W=9.00U L=0.50U AD=6.75P PD=10.50U AS=24.09P PS=18.25U
M23 17 8 9 Vsan! rn W=8.50U L=0.50U AD=22.75P PD=17.23U AS=8.43P PS=6.85U
M24 9 12 17 Vsan! rn W=8.50U L=0.50U AD=8.43P PD=6.85U AS=22.75P PS=17.23U
M25 17 9 24 Vsan! rn W=9.50U L=0.50U AD=25.43P PD=19.26U AS=7.12P PS=11.00U
M26 24 3 14 Vsan! rn W=9.50U L=0.50U AD=7.12P PD=11.00U AS=7.02P PS=5.49U
M27 14 16 25 Vsan! rn W=9.50U L=0.50U AD=7.02P PD=5.49U AS=7.12P PS=11.00U
M28 25 5 17 Vsan! rn W=9.50U L=0.50U AD=7.12P PD=11.00U AS=25.43P PS=19.26U
M29 17 14 16 Vsan! rn W=9.50U L=0.50U AD=25.43P PD=19.26U AS=8.92P PS=7.16U
M30 16 12 17 Vsan! rn W=9.00U L=0.50U AD=8.45P PD=6.78U AS=24.09P PS=18.25U
M31 17 14 20 Vsan! rn W=9.50U L=0.50U AD=25.43P PD=19.26U AS=7.71P PS=8.99U
M32 17 20 21 Vsan! rn W=8.00U L=0.50U AD=21.41P PD=16.22U AS=6.43P PS=7.69U
*** Node Listing for subckt:  dfrf312
** N0                          ==  IdealGND
** N1                [U=11]    ==  VddX
** N2                [U=3]     ==  CLK2
** N3                [U=8]     ==  clkb
** N5                [U=6]     ==  clkbb
** N6                [U=3]     ==  DATA1
** N7                [U=2]     ==  a_252_215#
** N8                [U=6]     ==  Q1b
** N9                [U=7]     ==  Q1
** N10               [U=2]     ==  a_312_215#
** N11               [U=2]     ==  a_372_215#
** N12               [U=5]     ==  RST3
** N13               [U=2]     ==  a_492_210#
** N14               [U=8]     ==  Q2b
** N15               [U=2]     ==  a_552_210#
** N16               [U=5]     ==  Q2
** N17               [U=13]    ==  GNDX
** N19               [U=2]     ==  a_652_180#
** N20               [U=5]     ==  Q
** N21               [U=3]     ==  Q_b
```

```
** N22                [U=2]      ==  a_252_15#
** N23                [U=2]      ==  a_312_15#
** N24                [U=2]      ==  a_492_15#
** N25                [U=2]      ==  a_552_15#
** N26                [U=1]      ==  w_n15_165#
********************************************************************
** Vsan!              [U=16]
** Vsap!              [U=16]
.ENDS

** Subcircuit definition for xorf201
**   Extraction   file   is   /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
xorf201.ext
.SUBCKT xorf201 2 3 7 9 10 14
M1 1 2 3 Vsap! rp W=8.00U L=0.50U AD=6.11P PD=8.44U AS=0.00P PS=0.00U
M2 3 2 5 Vsap! rp W=15.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M3 5 6 7 Vsap! rp W=15.00U L=0.50U AD=0.00P PD=0.00U AS=11.07P PS=8.05U
M4 7 1 8 Vsap! rp W=15.00U L=0.50U AD=11.07P PD=8.05U AS=0.00P PS=0.00U
M5 8 9 3 Vsap! rp W=15.00U L=0.50U AD=0.00P PD=0.00U AS=0.00P PS=0.00U
M6 3 9 6 Vsap! rp W=8.00U L=0.50U AD=0.00P PD=0.00U AS=7.56P PS=9.89U
M7 10 2 1 Vsan! rn W=3.00U L=0.50U AD=8.55P PD=8.79U AS=2.29P PS=3.16U
M8 10 2 12 Vsan! rn W=5.50U L=0.50U AD=15.68P PD=16.11U AS=4.12P PS=7.00U
M9 12 9 7 Vsan! rn W=5.50U L=0.50U AD=4.12P PD=7.00U AS=4.06P PS=2.95U
M10 7 6 13 Vsan! rn W=5.50U L=0.50U AD=4.06P PD=2.95U AS=4.12P PS=7.00U
M11 13 1 10 Vsan! rn W=5.50U L=0.50U AD=4.12P PD=7.00U AS=15.68P PS=16.11U
M12 10 9 6 Vsan! rn W=3.00U L=0.50U AD=8.55P PD=8.79U AS=2.84P PS=3.71U
*** Node Listing for subckt:  xorf201
** N0                             ==  IdealGND
** N1                 [U=4]       ==  24
** N2                 [U=5]       ==  A1
** N3                 [U=5]       ==  VddX
** N5                 [U=2]       ==  121
** N6                 [U=4]       ==  25
** N7                 [U=5]       ==  O
** N8                 [U=2]       ==  120
** N9                 [U=5]       ==  B1
** N10                [U=5]       ==  GNDX
** N12                [U=2]       ==  151
** N13                [U=2]       ==  150
** N14                [U=1]       ==  w_n15_165#
********************************************************************
** Vsan!              [U=6]
** Vsap!              [U=6]
.ENDS
******  top  level  cell  is  /users2/students/moorap/iclayout/prgr/divider/prgr-conv/
divider_2.ext
** Instance-id:dfrf312_8
X1 1 2 3 4 5 6 3 7 dfrf312
** Instance-id:dfrf312_7
X2 1 8 9 10 5 11 12 7 dfrf312
** Instance-id:norf211_0
X3 2 13 8 1 14 5 7 norf211
** Instance-id:invf103_0
X4 10 15 1 5 7 invf103
** Instance-id:muxf201_0
X5 15 1 16 14 4 5 7 muxf201
** Instance-id:pudf000_1
X6 5 1 16 7 pudf000
** Instance-id:nanf211_2
X7 1 17 18 19 5 7 nanf211
** Instance-id:xorf201_12
X8 11 1 9 19 5 7 xorf201
** Instance-id:dfrf312_6
X9 20 8 21 10 22 23 24 25 dfrf312
** Instance-id:xorf201_11
X10 26 20 27 11 22 25 xorf201
** Instance-id:nanf811_0
X11 22 20 13 28 29 30 30 31 32 27 33 25 nanf811
** Instance-id:xorf201_10
X12 34 20 31 18 22 25 xorf201
** Instance-id:xorf201_9
X13 35 20 32 17 22 25 xorf201
** Instance-id:nanf311_0
X14 18 20 17 11 36 22 25 nanf311
** Instance-id:nanf411_0
X15 20 18 17 11 23 37 22 25 nanf411
** Instance-id:xorf201_8
```

```
X16 23 20 21 36 22 25 xorf201
** Instance-id:xorf201_7
X17 38 20 28 39 22 25 xorf201
** Instance-id:dfrf312_5
X18 40 41 42 43 44 8 42 45 dfrf312
** Instance-id:dfrf312_4
X19 40 8 46 10 44 47 48 45 dfrf312
** Instance-id:dfrf312_3
X20 40 8 49 10 44 39 50 45 dfrf312
** Instance-id:buff101_0
X21 51 40 41 44 45 buff101
** Instance-id:xorf201_6
X22 52 40 29 53 44 45 xorf201
** Instance-id:xorf201_5
X23 54 40 33 23 44 45 xorf201
** Instance-id:xorf201_4
X24 55 40 30 47 44 45 xorf201
** Instance-id:nanf211_1
X25 40 53 56 57 44 45 nanf211
** Instance-id:xorf201_3
X26 47 40 46 57 44 45 xorf201
** Instance-id:xorf201_2
X27 39 40 49 37 44 45 xorf201
** Instance-id:nanf211_0
X28 40 39 37 56 44 45 nanf211
** Instance-id:xorf201_1
X29 53 58 59 56 60 61 xorf201
** Instance-id:dfrf312_2
X30 58 8 59 10 60 53 62 61 dfrf312
** Instance-id:pudf000_0
X31 60 58 43 61 pudf000
** Instance-id:dfrf312_1
X32 58 8 63 10 60 17 64 61 dfrf312
** Instance-id:dfrf312_0
X33 58 8 65 10 60 18 65 61 dfrf312
** Instance-id:xorf201_0
X34 18 58 63 17 60 61 xorf201
*** Node Listing for subckt:  divider_2
** N0                              ==  IdealGND
** N1                  [U=8]       ==  Vdd
** N2                  [U=2]       ==  dfrf312_8/CLK2
** N3                  [U=2]       ==  dfrf312_8/Q_b
** N4                  [U=2]       ==  RESET
** N5                  [U=8]       ==  GND
** N6                  [U=1]       ==  F_OUT
** N7                  [U=8]       ==  dfrf312_7/w_n15_165#
** N8                  [U=9]       ==  dfrf312_5/Q
** N9                  [U=2]       ==  xorf201_12/O
** N10                 [U=8]       ==  invf103_0/O
** N11                 [U=5]       ==  dfrf312_7/Q
** N12                 [U=1]       ==  dfrf312_7/Q_b
** N13                 [U=2]       ==  nanf811_0/O1
** N14                 [U=2]       ==  muxf201_0/B2
** N15                 [U=2]       ==  muxf201_0/O
** N16                 [U=2]       ==  pudf000_1/O
** N17                 [U=6]       ==  dfrf312_1/Q
** N18                 [U=6]       ==  dfrf312_0/Q
** N19                 [U=2]       ==  nanf211_2/O2
** N20                 [U=9]       ==  Vdd_3_
** N21                 [U=2]       ==  xorf201_8/O
** N22                 [U=9]       ==  GND_3_
** N23                 [U=4]       ==  dfrf312_6/Q
** N24                 [U=1]       ==  dfrf312_6/Q_b
** N25                 [U=9]       ==  dfrf312_6/w_n15_165#
** N26                 [U=1]       ==  D3
** N27                 [U=2]       ==  xorf201_11/O
** N28                 [U=2]       ==  xorf201_7/O
** N29                 [U=2]       ==  xorf201_6/O
** N30                 [U=3]       ==  xorf201_4/O
** N31                 [U=2]       ==  xorf201_10/O
** N32                 [U=2]       ==  xorf201_9/O
** N33                 [U=2]       ==  xorf201_5/O
** N34                 [U=1]       ==  D1
** N35                 [U=1]       ==  D2
** N36                 [U=2]       ==  nanf311_0/O2
** N37                 [U=3]       ==  nanf211_0/B1
** N38                 [U=1]       ==  D5
```

```
** N39                [U=4]     ==  dfrf312_3/Q
** N40                [U=11]    ==  Vdd_5_
** N41                [U=2]     ==  buff101_0/O
** N42                [U=2]     ==  dfrf312_5/Q_b
** N43                [U=2]     ==  pudf000_0/O
** N44                [U=11]    ==  GND_5_
** N45                [U=11]    ==  buff101_0/w_n15_165#
** N46                [U=2]     ==  xorf201_3/O
** N47                [U=3]     ==  dfrf312_4/Q
** N48                [U=1]     ==  dfrf312_4/Q_b
** N49                [U=2]     ==  xorf201_2/O
** N50                [U=1]     ==  dfrf312_3/Q_b
** N51                [U=1]     ==  F_IN
** N52                [U=1]     ==  D6
** N53                [U=4]     ==  dfrf312_2/Q
** N54                [U=1]     ==  D4
** N55                [U=1]     ==  D7
** N56                [U=3]     ==  nanf211_0/O2
** N57                [U=2]     ==  nanf211_1/O2
** N58                [U=6]     ==  Vdd_7_
** N59                [U=2]     ==  xorf201_1/O
** N60                [U=6]     ==  GND_7_
** N61                [U=6]     ==  dfrf312_0/w_n15_165#
** N62                [U=1]     ==  dfrf312_2/Q_b
** N63                [U=2]     ==  xorf201_0/O
** N64                [U=1]     ==  dfrf312_1/Q_b
** N65                [U=2]     ==  dfrf312_0/Q_b
**********************************************************
*
* Model Definitions for PSPICE
*
**********************************************************

.include cdh_ttt.1p0
.param BIT1g=0
.param BIT2g=0
.param BIT3g=0
.param BIT4g=0
.param BIT5g=0
.param BIT6g=0
.param BIT7g=0

.param BIT1d=999meg
.param BIT2d=999meg
.param BIT3d=999meg
.param BIT4d=999meg
.param BIT5d=999meg
.param BIT6d=999meg
.param BIT7d=999meg

.param FREQIN=300MEG
.param RESETg=999MEG
.param RESETd=0

****
* Circuit interconnections


*** VDD ***
Vdd999 0 3.3
Rdd11 999 0
Rdd220 999 0
Rdd340 999 0
Rdd458 999 0

*** GND ***
Rgnd15 0 0
Rgnd222 0 0
Rgnd344 0 0
Rgnd460 0 0

*** Frequency selection bits
RD134 999 BIT1d
RD235 999 BIT2d
RD326 999 BIT3d
RD454 999 BIT4d
RD538 999 BIT5d
```

```
RD652 999 BIT6d
RD755 999 BIT7d

RG134 0 BIT1g
RG235 0 BIT2g
RG326 0 BIT3g
RG454 0 BIT4g
RG538 0 BIT5g
RG652 0 BIT6g
RG755 0 BIT7g



*** Master Reset ***
Rrst4 0 RESETg
Rrst24 999 RESETd

*** Frequency Input ***
Vfin51 0 SIN(1.5 1.5 FREQIN)

*** Frequency Input is node 51
*** Frequency Output is node 6
Rload 6 999 2
Cload 999 0 2p

*.op
*
.temp 25 200
.tran 1n 1000n 0 1n
* First run is in reset mode with all frequency selection
* pins grounded

.option POST
.option METHOD=GEAR
.option PROBE
.probe TRAN 51 6


* Test at 260MHz
.alter
.param BIT1g=999meg
.param BIT1d=0
.param BIT2g=0
.param BIT2d=999meg
.param BIT3g=0
.param BIT3d=999meg
.param BIT4g=0
.param BIT4d=999meg
.param BIT5g=0
.param BIT5d=999meg
.param BIT6g=0
.param BIT6d=999meg
.param BIT7g=999meg
.param BIT7d=0
.param RESETd=999meg
.param RESETg=0
.param FREQIN=260MEG


* Test at 280MHz
.alter
.param BIT1g=0
.param BIT1d=999meg
.param BIT2g=999meg
.param BIT2d=0
.param BIT3g=999meg
.param BIT3d=0
.param BIT4g=0
.param BIT4d=999meg
.param BIT5g=0
.param BIT5d=999meg
.param BIT6g=0
.param BIT6d=999meg
.param BIT7g=999meg
.param BIT7d=0
.param RESETd=999meg
```

```
.param RESETg=0
.param FREQIN=280MEG


* Test at 300MHz
.alter
.param BIT1g=999meg
.param BIT1d=0
.param BIT2g=999meg
.param BIT2d=0
.param BIT3g=0
.param BIT3d=999meg
.param BIT4g=999meg
.param BIT4d=0
.param BIT5g=0
.param BIT5d=999meg
.param BIT6g=0
.param BIT6d=999meg
.param BIT7g=999meg
.param BIT7d=0
.param RESETd=999meg
.param RESETg=0
.param FREQIN=300MEG


* Test at 320MHz
.alter
.param BIT1g=0
.param BIT1d=999meg
.param BIT2g=0
.param BIT2d=999meg
.param BIT3g=0
.param BIT3d=999meg
.param BIT4g=0
.param BIT4d=999meg
.param BIT5g=999meg
.param BIT5d=0
.param BIT6g=0
.param BIT6d=999meg
.param BIT7g=999meg
.param BIT7d=0
.param RESETd=999meg
.param RESETg=0
.param FREQIN=320MEG


* Test at 340MHz
.alter
.param BIT1g=999meg
.param BIT1d=0
.param BIT2g=0
.param BIT2d=999meg
.param BIT3g=999meg
.param BIT3d=0
.param BIT4g=0
.param BIT4d=999meg
.param BIT5g=999meg
.param BIT5d=0
.param BIT6g=0
.param BIT6d=999meg
.param BIT7g=999meg
.param BIT7d=0
.param RESETd=999meg
.param RESETg=0
.param FREQIN=340MEG


.END
*0 errors and 0 warnings found.
```

Vita

Andrew Moor was born in Knoxville, Tennessee in 1976. He attended elementary and high school at Christian Academy of Knoxville. After graduating Summa Cum Laude from Christian Academy in June 1994, he began studies at the University of Tennessee, Knoxville, majoring in Electrical Engineering. During his undergraduate education, he participated in the Cooperative Engineering Program, working four semesters as an RF Engineering Co-op Student with U.S. Cellular in Knoxville. He was also initiated into Tau Beta Pi, Phi Kappa Phi, and Eta Kappa Nu, where he served as the Beta Phi chapter President during his senior year. Andrew completed his undergraduate courses in the spring of 1999, and received the B.S. degree in Electrical Engineering, Magna Cum Laude. In June 1999 he passed the Fundamentals of Engineering Exam and received certification as an Engineer Intern from the State of Tennessee.

For his graduate education, Andrew accepted the Lucent Fellowship in the UT/ORNL Joint Program. During an internship in the summer of 1999, he worked as a Senior Technical Associate in the Microelectronics Group at Lucent Technologies in Reading, Pennsylvania. In August 1999 he returned to the University of Tennessee for graduate studies in Electrical Engineering. As a part of the Joint Program, Andrew was awarded a Graduate Research Assistant position within the Department of Electrical Engineering. His research was conducted primarily at the Oak Ridge National Laboratory. After receiving the M.S. degree in Electrical Engineering from UT in May 2001, Andrew began work as a design engineer at ASIC International. His hobbies and interests include computers, professional audio, internet development, hiking, and snow skiing.