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Development of a 6-bit 15.625 MHz CMOS two-step flash analog-to-digital converter for a low dead time sub-nanosecond time measurement system

Brian Keith Swann

To the Graduate Council:

I am submitting herewith a thesis written by Brian Keith Swann entitled "Development of a 6-bit 15.625 MHz CMOS two-step flash analog-to-digital converter for a low dead time sub-nanosecond time measurement system." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this thesis and recommend its acceptance:

T. Vaughn Black, Danny F. Newport, David M. Binkley

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Accepted for the Council:

Associate Vice Chancellor and
Dean of The Graduate School

Development of a 6-bit 15.625 MHz CMOS Two-Step Flash Analog-to-Digital Converter for a Low Dead Time Sub-Nanosecond Time Measurement System

A Thesis
Presented for the
Master of Science
Degree
The University of Tennessee, Knoxville

Brian Keith Swann
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Dedication

This thesis is dedicated to my parents Robert L. and Bertie L. Swann who have sacrificed much to give me unlimited opportunities in life which they never had and to my brother Rodger M. Swann who has always been there for me no matter what the circumstances.

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Abstract

The development of a 6-bit 15.625 MHz CMOS two-step analog-to-digital converter (ADC) is presented. The ADC was developed for use in a low dead time, high-performance, sub-nanosecond time-to-digital converter (TDC). The TDC is part of a new custom CMOS application specific integrated circuit (ASIC) that will be incorporated in the next generation of front-end electronics for high-performance positron emission tomography imaging.

The ADC is based upon a two-step flash architecture that reduces the comparator count by a factor-of-two when compared to a traditional flash ADC architecture and thus a significant reduction in area, power dissipation, and input capacitance of the converter is achieved. The converter contains time-interleaved auto-zeroed CMOS comparators These comparators utilize offset correction in both the preamplifier and the subsequent regenerative latch stage to guarantee good integral and differential non-linearity performance of the converter over extreme process conditions. Also, digital error correction was employed to overcome most of the major metastability problems inherent in flash converters and to guarantee a completely monotonic transfer function.

Corrected comparator offset measurements reveal that the CMOS comparator design maintains a worse case input-referred offset of less than 1 mV at conversion rates up to 8 MHz and less than a 2 mV offset at conversion rates as high as 16 MHz while dissipating less than 2.6 mW. Extensive laboratory measurements indicate that the ADC achieves differential and integral non-linearity performance of less than ±½ LSB with a 20 mV/LSB resolution. The ADC dissipates 90 mW from a single 5 V supply and occupies a die area of 1.97 mm x 1.13 mm in 0.8 μm CMOS technology.

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Chapter 1

Introduction

1.1 Time Measurement Application for Positron Emission Tomography

The precise electronic measurement of time between two physical events is very important and fundamental in many experimental and applied systems. A time-to-digital converter (TDC) is one type of an electronic instrumentation system that is capable of measuring the time difference between two random events. Time-to-digital converters have a variety of industrial and research applications. They are used in laser range finding where distance measurements are required, instrumentation and electronic test equipment such as digital storage oscilloscopes, positron emission tomographs and various high-energy physics experiments. The TDC described in this work is for use in commercial positron emission tomography (PET) medical imaging systems.

In a PET system, a positron emitting radionuclide is injected into the patient. When a positron comes into contact with an electron within the body, the two particles annihilate and produce two time coincident 511 keV gamma rays that are emitted 180 degrees apart. If two gamma ray detectors are placed on opposite sides of the body, the detection and coincidence measurement of two annihilation photons can be performed (Figure 1-1). Many gamma ray detectors are arranged in paralleled rings that encircle the patient to be imaged to generate a full tomographic data set [1]. A time measurement is required to detect the coincidence of two opposing gamma rays that hit two detector pairs. Coincidence refers to the arrival and detection of two events in a particular timing

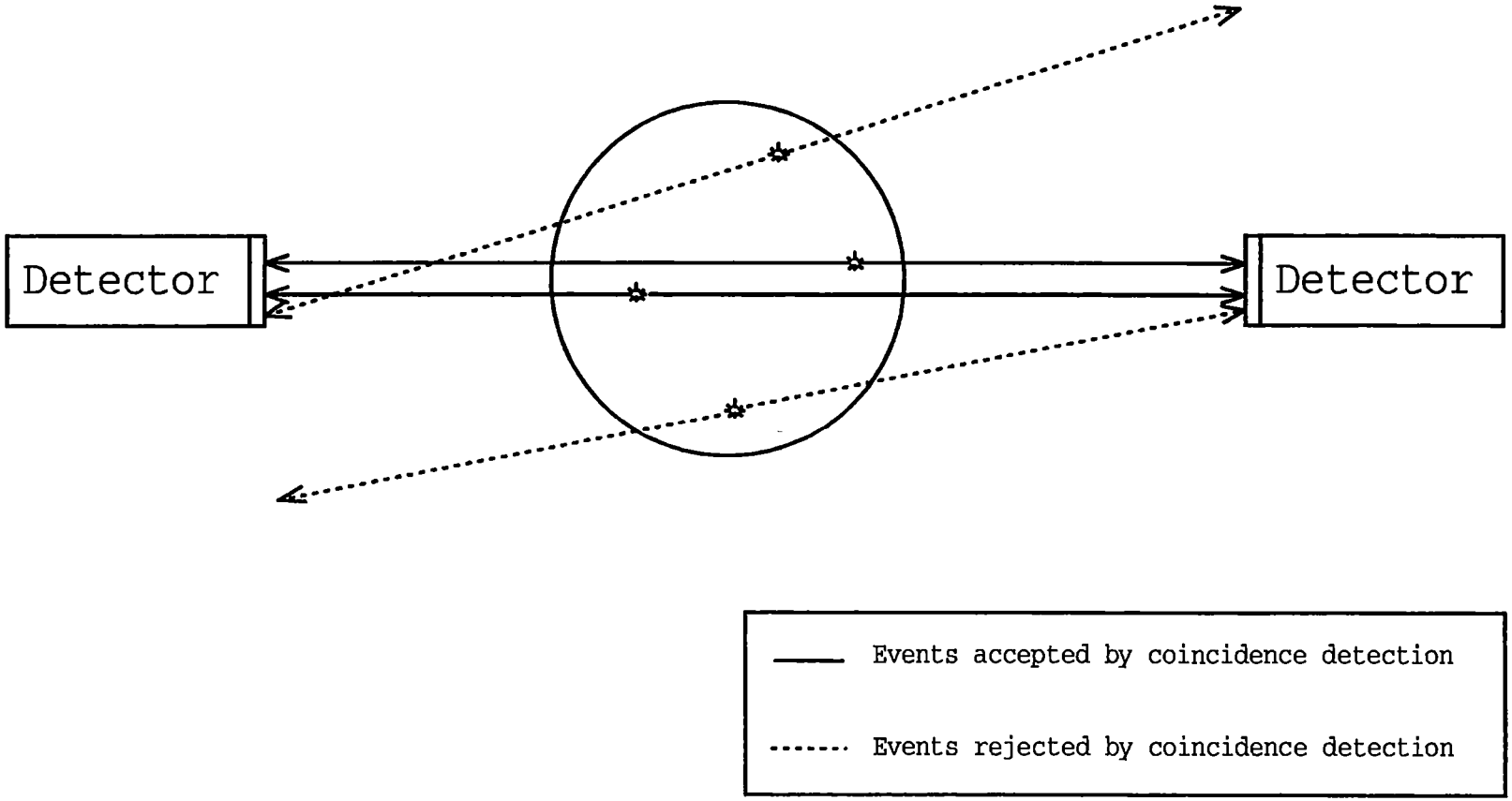


Figure 1-1. Basic principles of PET event coincidence detection.

window. Only the events that are in coincidence are accepted and all others are rejected. The line between the two detector pairs is known as the line of response. From the timing measurements, a histogram array of coincident events is then generated that contains all possible lines of response. The histogram array of all possible lines of response is called a sinogram. This sinogram is converted into a medical image through various reconstruction techniques.

Since in a PET system a large number of measuring channels is required, a key goal is to realize the TDC in standard low cost technologies, such as CMOS, while meeting the design challenges of high-performance sub-nanosecond time resolution. The TDC discussed here will be part of a new custom, front-end CMOS integrated circuit for high-performance Lutetium Oxyorthosilicate (LSO) PET imaging applications. The motivation for the development of a custom, front-end CMOS integrated circuit is the reduction in cost, size, and power while simultaneously increasing performance, reliability, and testability of the system

1.2 Time Measurement System Description and Requirements

1.2.1 Time Measurement Overview

An architectural description of this proposed front-end CMOS application specific integrated circuit (ASIC) is shown in Figure 1-2. The timing output of the constant-fraction discriminator (CFD) is connected to the TDC where the event time is digitized with respect to the rising edge of the system clock. The CFD provides logic timing signal that is independent of the input signal amplitude. Figure 1-3 shows the system level

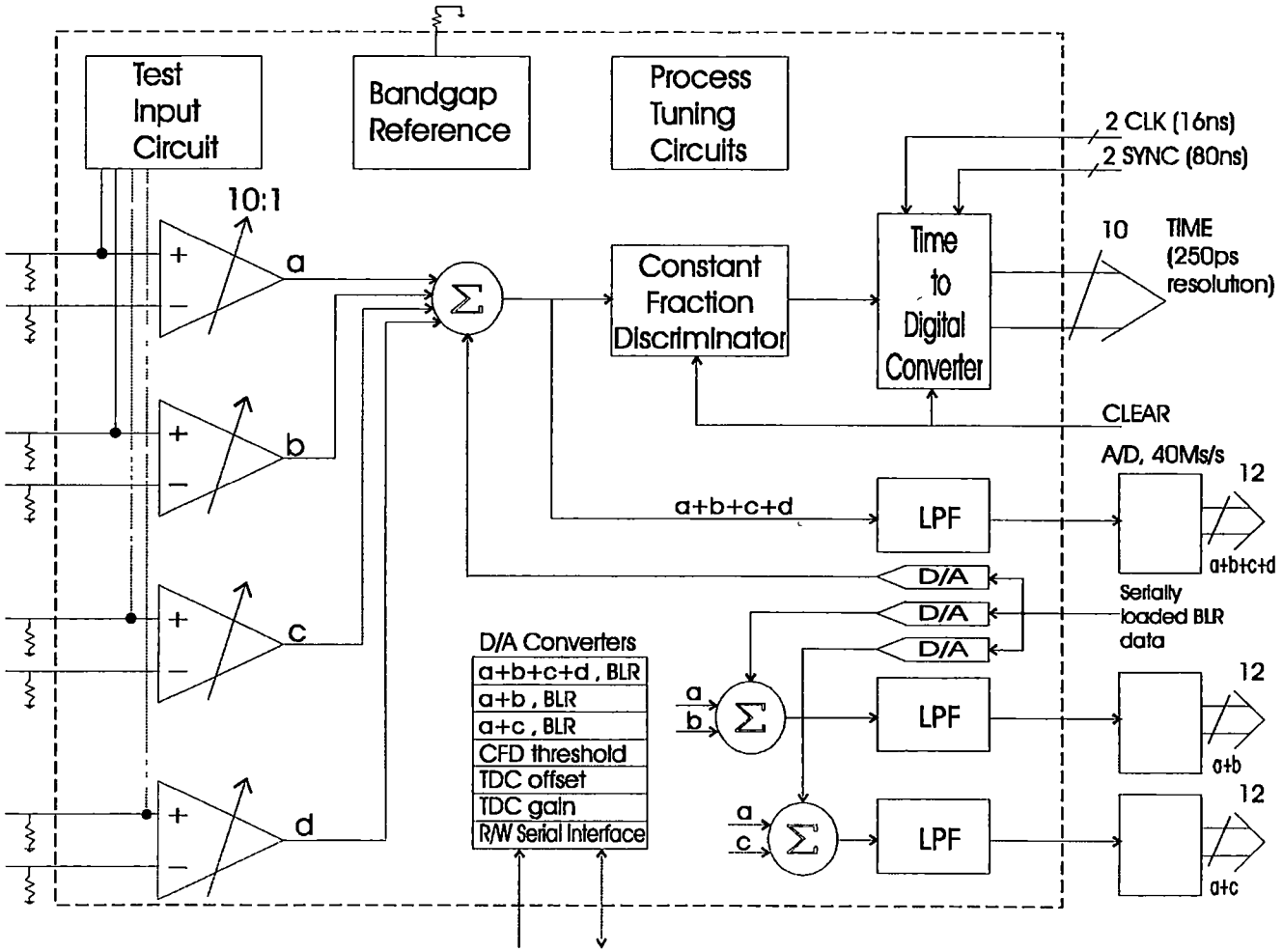


Figure 1-2. Block diagram of the high-performance LSO PET front-end ASIC.

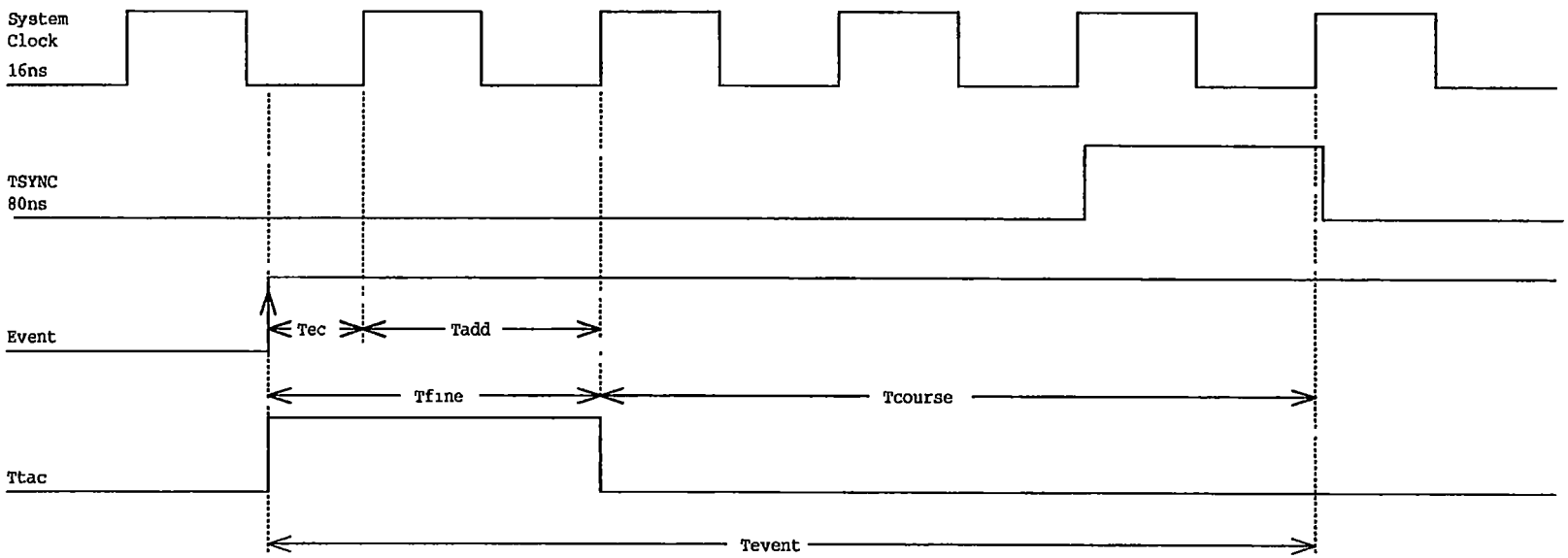


Figure 1-3. TDC system level timing signals.

timing waveforms that are relevant to the TDC. The event signal from the CFD is completely random with respect to the 16 ns system clock and serves as an asynchronous start command to the TDC. The 80 ns *SYNC* signal provides a synchronous stop command to the TDC. Thus, the objective is to digitize the time interval labeled T_{event} in Figure 1-3. This time period can be divided into two major parts: a T_{fine} time period and a T_{coarse} time period. The T_{coarse} time interval requires a coarse timing resolution of 16 ns and can be provided by just counting the system clock once the event signal has been detected. The duration of the T_{coarse} time interval can ideally vary from 0 ns to 80 ns depending upon the occurrence of the event signal relative to the rising edge of the system clock. A fine timing resolution system is needed to resolve and determine the time interval T_{fine}. The T_{fine} time interval is composed of the two time periods, which are T_{ec} and T_{add}. The interval T_{ec} is the total time from the event to the next rising edge of the clock. T_{add} is a fixed time period and is simply the duration of one clock cycle. The time period T_{add} is added to the interval T_{ec} to help improve the linearity of the time interval measurement and perhaps relax the propagation delay requirements of the signal processing circuits. Note that the duration of T_{fine} time interval can ideally vary from 16 ns to 32 ns depending upon the arrival of the event signal relative to the rising edge of the system clock.

1.2.2 TDC Specifications and Design Requirements

For this sub-nanosecond time measurement application, the critical specifications and requirements of the TDC are:

- 250 ps time resolution
- Dead time < 80 ns
- Integral and Differential Non-linearity < ±½ LSB
- CFD circuitry will provide asynchronous START command
- 16 ns (62.5 MHz) system clock and 80 ns *SYNC* signal used for synchronous STOP command
- Multi-hit and multi-channel TDC implementations are not required for this application since there is only one timing channel per ASIC
- Single 5 V supply compatibility in CMOS technology
- Final design for either stand-alone or integrated function in larger chip
- Cost equal to or less than $2.00 for discrete electronic circuit which has a 2 ns time resolution

The principle methods of time interval measurements were reviewed by Porat [2]. Many solutions to achieve nanosecond and sub-nanosecond TDCs in standard CMOS technologies have been recently reported [3-11]. So there are various TDC architectures one might consider using to satisfy these performance requirements. TDCs have traditionally been divided into two types: the current integration TDC being a high-resolution analog converter and the digital counter TDC being a low resolution converter.

Recently, other alternative TDC architectures have emerged mainly of the delay-locked loop (DLL) approach or some variation which have achieved resolutions somewhere in between these two extremes.

The digital counter based TDC is relatively easy to design, but only very limited resolution can be obtained with reasonable clock frequencies. For the counter based approach, sub-nanosecond timing requires a clock frequency of over 1 GHz which would consume a great deal of power and be very difficult to implement in standard CMOS processes. With a fundamental system clock frequency of 62.5 MHz, the digital counter based architecture gives a resolution of 16 ns with a ±16 ns uncertainty and is therefore clearly unacceptable for this application However, this counter based method can be used to determine the T_{coarse} timing information labeled in Figure 1-3.

DLL architectures rely on tuned delay elements to determine the resolution of the TDC. Basic CMOS gates are inverting and therefore two gates (inverters) are normally used as the fundamental delay element. As a result, most straight forward DLL architectures are limited to a time resolution that is basically the combined delay of two inverters in a given CMOS process For our application, the delay of two inverters must be tuned to an overall delay of 250 ps. There is substantial technical risk and uncertainty whether tuned digital delays of 250 ps can be controlled over extreme process and temperature variations in 0.8 μm CMOS technology. Another major concern is the total number of tuned delay elements required for sub-nanosecond timing resolution. For our reference clock frequency of 62.5 MHz, 64 delay elements are required to achieve the desired 250 ps resolution. The 64 element delay line can be relatively long and therefore

these elements have a non-negligible amount of non-linearity due to process gradients. The linearity of the delay lines is limited by the matching of minimum sized logic delay elements. Therefore, to achieve good linearity performance, good matching between relatively small unit delay elements must be achieved and also systematic layout errors must be minimized. For these reasons, the fundamental DLL based TDC architecture was not selected for this application

Many variations of the DLL based TDC architecture have been developed to improve the time resolution beyond the basic delay of two inverters in a given CMOS technology [4, 5, 8]. These architectures contain some form of a timing generator that achieves sub-gate delays and can be implemented in standard digital CMOS processes However, these architectures become more complex to design and are still susceptible to the fundamental non-linearity problems associated with the delay lines.

Because of the issues associated with the digital counter based and the DLL based TDC architectures, the analog current integration approach was chosen to achieve a high-performance sub-nanosecond TDC. There are many ways to implement an analog current integration based TDC. The classical analog current integration TDC that utilizes a time-to-amplitude converter (TAC) followed by an analog-to-digital converter (ADC) was selected for this application. This architecture is appropriate for this application since high-resolution, good linearity, and fast conversion times are preferred while multi-hit capability and multi-channel integration is not necessary. In fact, a discrete TDC design that was based upon this approach, but with different specifications, was previously developed and successfully incorporated in an earlier time-of-flight PET tomograph over

ten years ago [12].

A block diagram of the chosen TDC architecture is shown in Figure 1-4. The major components of this TDC architecture consist of event capture circuitry, a TAC, an ADC, a coarse clock counter, digital control logic, and output register. The event capture circuitry generates a pulse whose width is proportional to the time difference between the event and the rising edge of the 16 ns system clock. This pulse width is labeled T_{fine} in Figure 1-3 and will ideally vary in duration from 16 ns to 32 ns, depending upon the arrival of the event signal relative to the system clock. The TAC receives this pulse as its input signal and generates a corresponding output voltage that is directly proportional to the pulse width. The TAC output voltage ideally varies from 2.475 V to 3.75 V, depending upon the input pulse width. The ADC then digitizes this voltage. Meanwhile, the coarse clock counter starts counting the number of clock cycles that occurs before the rising edge of clock and the 80 ns *SYNC* signal. The ADC output code is then combined with the output of the coarse clock counter to generate a final timing code for that particular event. This timing information is then stored in the digital output register that can be accessed by the system at a later time. The control logic generates all the necessary timing information and signals required to operate and interface to the TDC.

1.2.3 ADC Specifications and Design Requirements

A key component in the TDC architecture described above is the ADC To achieve the desired 250 ps time resolution, the system clock period of 16 ns needs to be resolved into 64 intervals or time bins. Therefore, a 6-bit ADC with 64 channels is

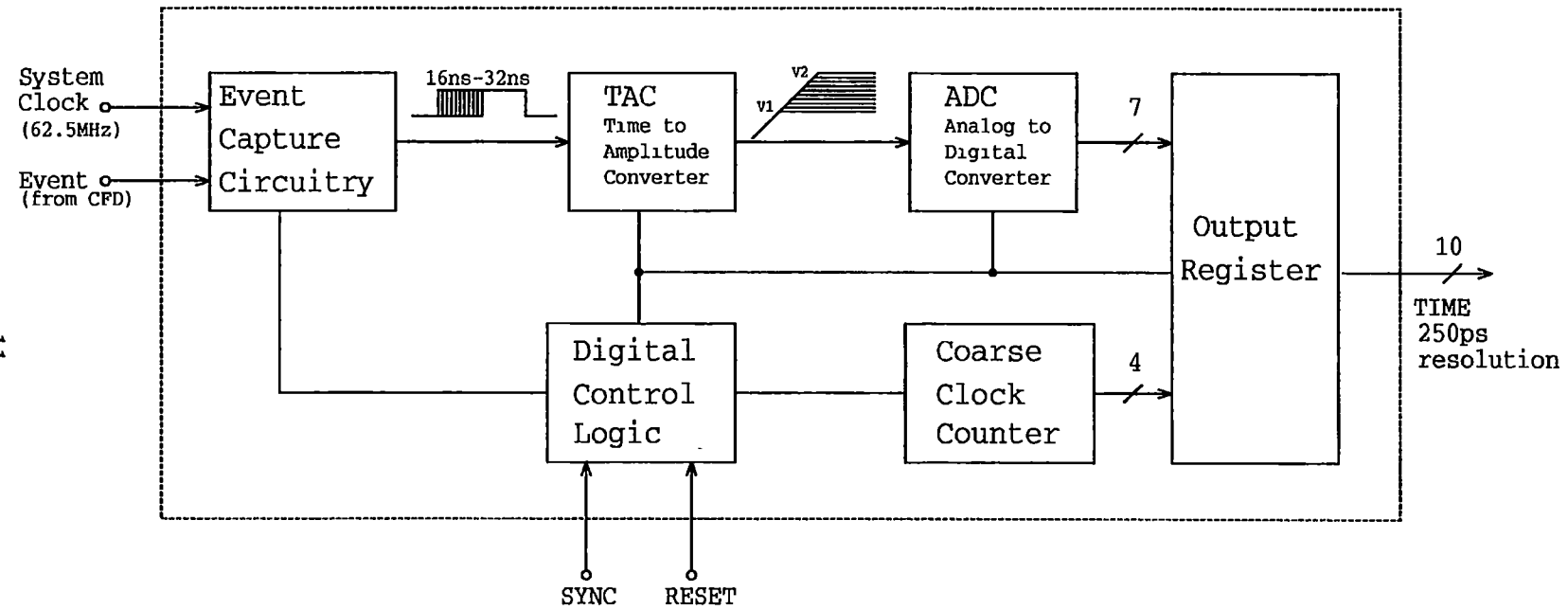


Figure 1-4. Block diagram of TDC architecture.

required to achieve the desired time resolution. Also, to satisfy the TDC's integral and differential non-linearity specification of ±½ LSB, the ADC will need equal or better performance. The TDC dead time specification of 80 ns will determine the required conversion speed of the ADC. The dead time specification for a TDC is typically defined as the time from when an event is detected until the TDC is ready to accept another event. This time period must include the conversion times of the TAC and ADC plus any additional time allocation for reset or re-initialization of circuitry. A timing diagram with time allocation on each functional block to achieve the 80 ns dead time requirement is shown in Figure 1-5. This particular timing configuration places very stringent demands on the speed performance of the ADC. The ADC will need to run at a 62.5 MHz conversion rate to satisfy the dead time specification. In general, ADCs in this speed category can be very complex and demanding to implement in CMOS technologies and also consume a good amount of power. Therefore, a sample-and-hold circuit was implemented at the system level to relax the performance requirements of the ADC.

The new proposed TDC timing diagram that includes the use of sample-and-hold circuit is shown in Figure 1-6. Through the utilization of a sample-and-hold circuit, a paralleled architecture is achieved which reduces the speed requirements of the ADC by a factor-of-five. The ADC must now digitize an input voltage within the allotted time of 80 ns instead of 16 ns. One subtle issue is that the input voltage presented by the sample-and-hold circuitry to the ADC is only available for 64 ns. However, an extra 16 ns is available to the ADC before the next conversion is required. Therefore, an ADC with a conversion speed of 15.625 MHz with a one clock cycle latency of 16 ns is acceptable.

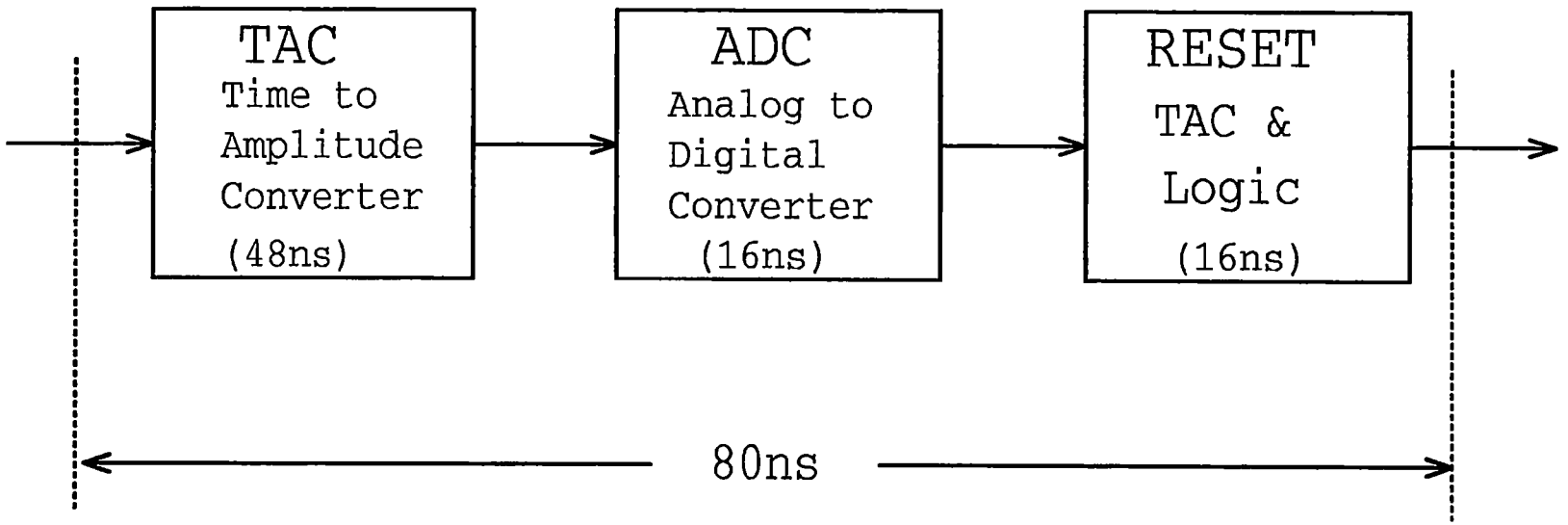


Figure 1-5. TDC conversion timing diagram.

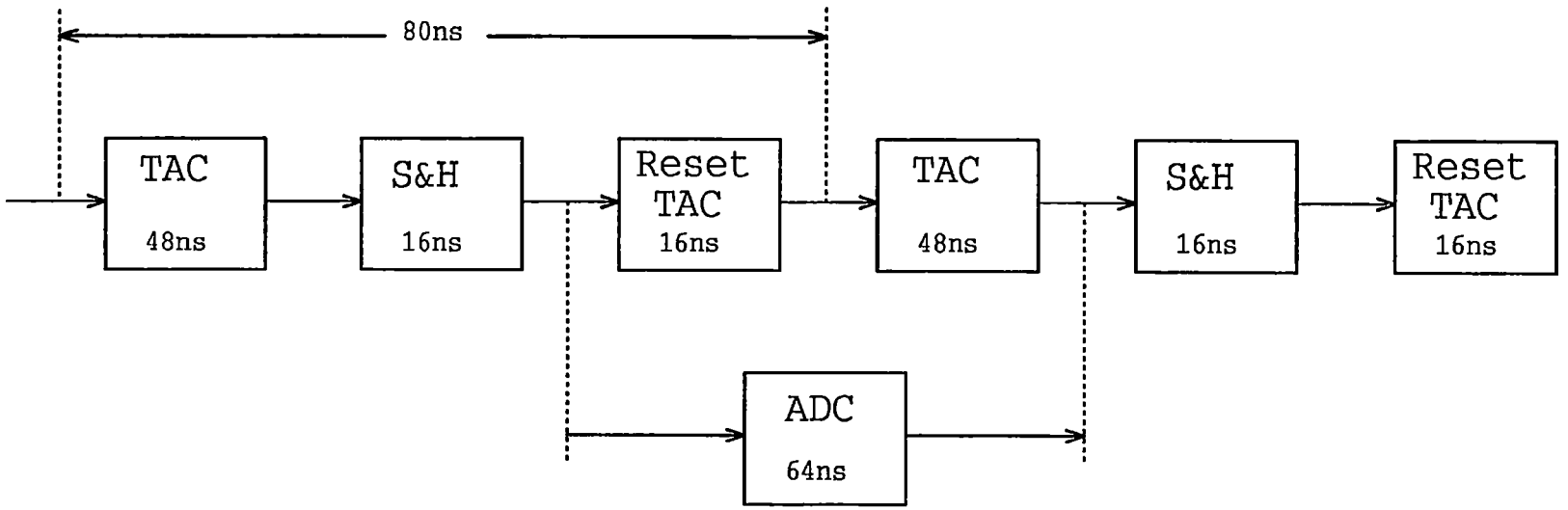


Figure 1-6. TDC conversion timing diagram with sample-and-hold implementation.

The focus of this work is the development of an ADC for use in a low dead time high-performance sub-nanosecond time-to-digital converter. The performance of the ADC should meet the following specifications:

- 6-bits of resolution
- Differential non-linearity < ±½ LSB
- Integral non-linearity < ±½ LSB
- Conversion rate of 15.625 MHz (64 ns) with a latency of one clock cycle (16 ns)
- 62.5 MHz (16 ns) system clock used for timing and control logic
- Typical reference voltage of 1.275 V resulting in a 20 mV/LSB resolution
- Accommodation of a 2 V input range to the ADC with a typical input range from the TAC of 2.475 V to 3.75 V
- Significant offset error is tolerable since variations in the TAC output voltage will be corrected by system calibration of the ADC reference voltage
- Low metastability error rate performance is not required since the total error rate of the time measurement system will be dominated by system level issues
- Single 5 V supply compatibility in 0.8 μm CMOS technology

1.3 Thesis Organization

The selection of an appropriate ADC architecture for the time measurement system application is found in Chapter 2. Also, a detailed description of the proposed two step flash ADC architecture is presented.

The design and analysis of the major functional blocks of the ADC are given in Chapter 3 with special emphasis placed on the development of an auto-zeroed CMOS comparator. After a brief introduction to comparators, the motivation and requirement for an offset corrected comparator is presented. The concept of charge injection is presented and the fundamental limitations of offset correction techniques due to charge injection is discussed. Next, the most common comparator offset cancellation techniques are explained. Extensive analysis of the selected comparator architecture is then presented. A complete non-linearity analysis of the ADC is presented which relates reference generation errors and comparator offsets to integral and differential linearity performance of the converter. Digital error correction and encoder design requirements are then shown. Finally, a brief description of the ADC control logic design is given.

Chapter 4 contains all key simulations and critical layout issues of the ADC design. Preamplifier and regenerative latch simulations are shown. Also, simulated performance of an ADC comparator channel is presented. Next, the simulation technique used to evaluate the complete ADC design is discussed. Integrated circuit layout plots of critical sections of the ADC are illustrated throughout Chapter 4.

Experimental results achieved by two different ADC test methodologies are presented in Chapter 5. The complex test circuitry required to fully characterize the ADC

is discussed. A summary of the experimental measurements obtained on the ADC is given. Also, corrected CMOS comparator offset measurements are reported.

Chapter 6 contains a summary of the work and potential design improvements are suggested.

Chapter 2

ADC Architecture Selection and Description

2.1 ADC Overview and Architecture Requirements

An ADC is a device that takes an analog input signal and generates a digital output code. Most ADCs are required to interface analog signals to digital signal processing systems. A wide variety of ADC architectures and applications have been reported [13-23]. A literature review of current ADCs reveals that most recent research and implementations can be classified into four types of architecture: pipeline, flash or flash-type, successive approximation, and oversampled ADCs [24]. All of these ADC architectures have been customized and optimized for their particular application and span the spectrum of speed and resolution.

For mixed-signal system applications, the latency and speed of the ADC are important design parameters. The latency of an ADC is defined as the delay between the sampling of the analog signal and the moment that the corresponding digital output code is available. However, the latency specification of an ADC is generally referenced to the end of a conversion and usually specified in an integer multiple of clock cycles. It is important to differentiate this specification from the conversion speed of the ADC. The time required for the analog signal to be presented to the ADC for a successful conversion is typically defined as the conversion speed or throughput of the converter. For our application, an ADC conversion speed of 15.625 MHz is required. Therefore, the analog input signal is only available to the converter for a total time period of 64 ns

However, from the start of the conversion process, a total time period of 80 ns is available until the digital output code is required Therefore, the ADC requirements are a conversion speed of 15.625 MHz with one 16 ns clock cycle latency while achieving 6-bits of resolution.

Architectural choices directly influence the speed and latency of a converter. For the ADC application described in Chapter 1, there is a requirement for a high-speed (15.625 MHz) and low latency (16 ns) converter architecture because the 6-bit ADC output code must be combined with output of the course clock counter at the end of the 80 ns *SYNC* period (Figures 1-3 and 1-4). There are a number of ADC architectures suitable for sampling rates of 15.625 MHz. However, the system requirement for a low latency converter eliminates most of the possible architectures from consideration. The ever popular pipeline ADC and other architectures have an inherently larger latency than a flash ADC architecture. Therefore, for high-speed and low latency ADC applications, the implementation of a flash or flash-type ADC architecture is almost mandatory. As a result, the investigation and implementation of an appropriate flash or flash-type ADC architecture for this application was performed.

2.2 Traditional Flash ADC Architecture

The fastest ADC architecture reported to date is the flash ADC [20]. Therefore, it has become one of the standard approaches for realizing high-speed converters Figure 2-1 shows a block diagram of a classical three-bit flash ADC. This architecture utilizes (2^N-1) comparators to achieve one comparator per quantization level and requires 2^N resistors,

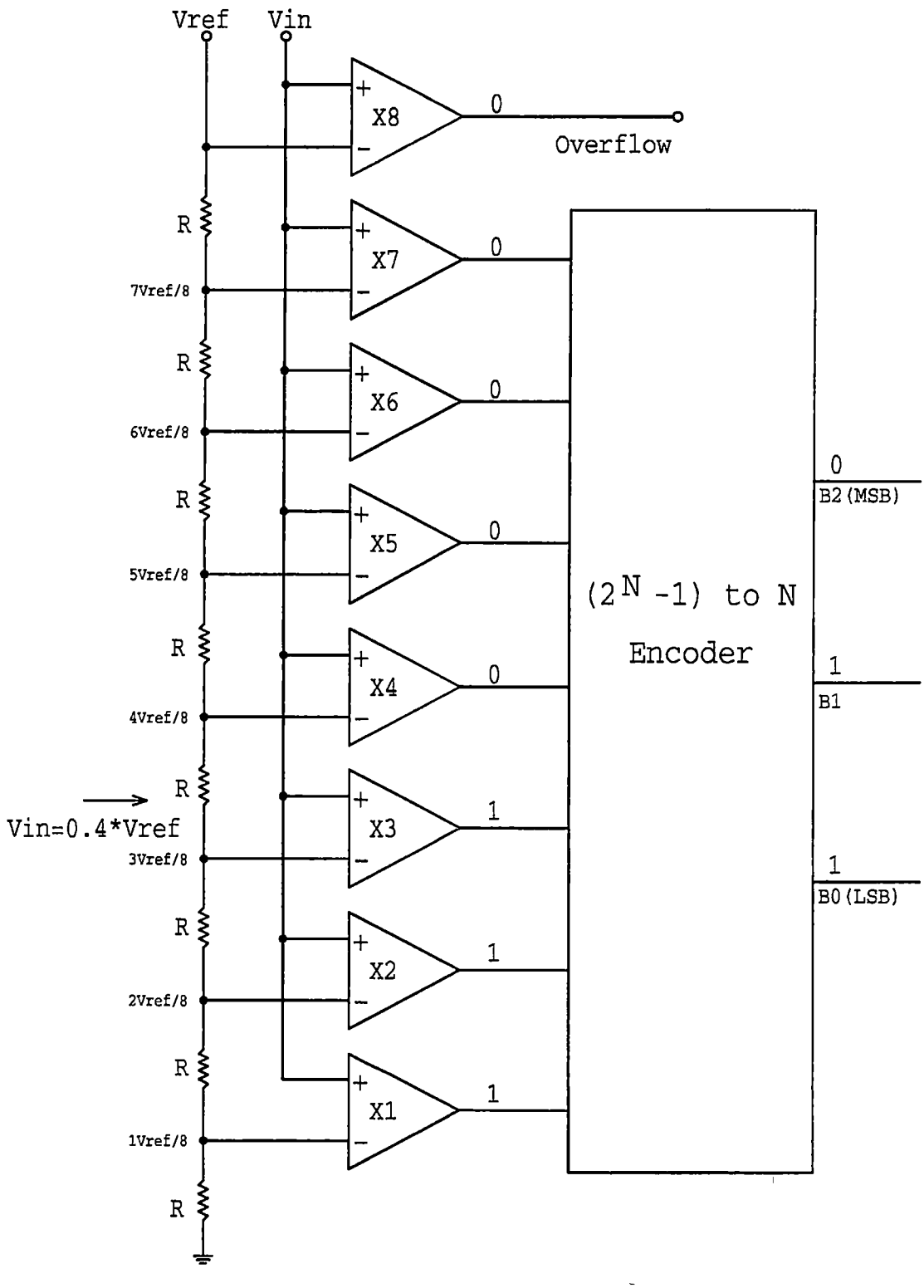


Figure 2-1. Block diagram of a classical 3-bit flash ADC architecture.

where N is the number of desired bits. The input signal, V_{in}, is connected to the positive input of all the comparators that are in parallel The reference voltage, V_{ref}, is divided into 2^N, or eight, reference values as indicated in the figure. Each of these references is applied to the negative input of a comparator. The input voltage is compared with each individual reference value or quantization level. The outputs of the comparators are passed into a digital encoder which generates a digital output code based upon the comparator outputs.

As an example, if V_{in} is equal to $0.4*V_{ref}$, then the outputs of the comparators, *X4-X7*, are a logical 0, and the bottom comparators outputs, *X1-X3*, are all a logical 1. The digital encoder logic would calculate 011 as the binary output code. Thus, any comparator connected to a resistor string node whose voltage is larger than V_{in} will have a logical 0 output while those who have voltages smaller than V_{in} will have a logical 1 output. This output code arrangement is typically called a thermometer code since it looks similar to the mercury bar in a thermometer. Table 2-1 shows the entire range of analog input voltages with the corresponding comparator outputs and the correct digitally encoded output code.

Although the classical flash converters are the fastest, they require (2^N-1) comparators, where N is the number of desired bits. Therefore, the layout area, power dissipation, and input capacitance of the ADC are all directly proportional to the number of comparators (2^N-1) for a given resolution. The required silicon area of an ADC is very important since it directly affects the cost and yield of the design. Also, power efficient CMOS integrated circuit design is always a goal and the power dissipation of ADCs is

Table 2-1. Truth table for classical 3-bit flash ADC.

Analog Input Voltage	Comparator Outputs							Digital Code		
Vin	X7	X6	X5	X4	X3	X2	X1	B2	B1	B0
Vin < Vref/8	0	0	0	0	0	0	0	0	0	0
Vref/8 < Vin < 2Vref/8	0	0	0	0	0	0	1	0	0	1
2Vref/8 < Vin < 3Vref/8	0	0	0	0	0	1	1	0	1	0
3Vref/8 < Vin < 4Vref/8	0	0	0	0	1	1	1	0	1	1
4Vref/8 < Vin < 5Vref/8	0	0	0	1	1	1	1	1	0	0
5Vref/8 < Vin < 6Vref/8	0	0	1	1	1	1	1	1	0	1
6Vref/8 < Vin < 7Vref/8	0	1	1	1	1	1	1	1	1	0
7Vref/8 < Vin < Vref	1	1	1	1	1	1	1	1	1	1

consistently a key specification. In some applications, the input capacitance of the ADC can ultimately limit the speed of the converter and may require an input buffer to drive the capacitive load presented by the ADC. Therefore, the main disadvantages of this architecture are that the layout area, power dissipation, and input capacitance nearly double for each additional bit of resolution needed. Consequently, most traditional flash converters implemented in CMOS technologies are typically limited to 6 to 8 bits of resolution [17-19, 25].

2.3 Two-Step Flash ADC Architecture

The traditional flash ADC architecture can be modified, at the expense of increased latency, to reduce the comparator count, and thus require less silicon area, dissipate less power, and achieve a smaller input capacitance. These groups of converters are commonly called a two-step flash ADC and are currently the most popular for achieving high-speed and medium resolution conversion. These converter architectures use a two-step conversion process and trade a factor-of-two in speed reduction for a large area and power savings.

There have been many types of two-step flash ADC architectures reported in the literature. Most two-step flash architectures require a DAC, amplifier, subtractor, digital error correction, and other additional circuitry [24, 26]. As a result, the design complexity of these converters drastically increases when compared to the traditional flash ADC implementation The main drawbacks of most two-step ADC converters have been the requirement for a high-speed, high-gain operational amplifier and a digital-to-analog

converter (DAC). However, one particular two-step flash ADC architecture reported by Ahmed [27] does not require any of these additional complex circuits. The design methodology of this two-step architecture can be explained by careful examination of the traditional flash ADC operation (Figure 2-1 and Table 2-1). In the classical flash ADC, the comparator, which compares the analog input voltage with $\frac{1}{2}V_{ref}$, generates the most significant bit (MSB) of the final output code. This aforementioned comparator is labeled *X4* in Figure 2-1. Throughout this work, this comparator is referred to as the MSB comparator since it is the comparator that generates the MSB decision of the ADC output code. After analyzing Figure 2-1 and Table 2-1, it can be concluded that it is only necessary to observe either the comparator outputs of *X1*, *X2*, and *X3*, or *X5*, *X6*, and *X7* depending upon the decision of the MSB comparator. If the output of the MSB comparator is a logical 0, then it is only necessary to look at the outputs of *X1*, *X2*, and *X3* to determine the final output code. Similarly, if the output of the MSB comparator is a logical 1, then only the outputs of *X5*, *X6*, and *X7* are required to calculate the output code. Therefore, after the output of the MSB comparator is known, it is only necessary to look at the results of half the comparators in a traditional flash architecture to determine the output code. This information can be used to simplify the ADC design because the output of the MSB comparator can be used as a control signal to reduce the required number of comparators

A simplified block diagram of the proposed two-step flash ADC architecture for a 3-bit converter is shown in Figure 2-2 Just as in the traditional flash ADC, a resistive ladder can be used to generate all the necessary reference voltages, but this ladder

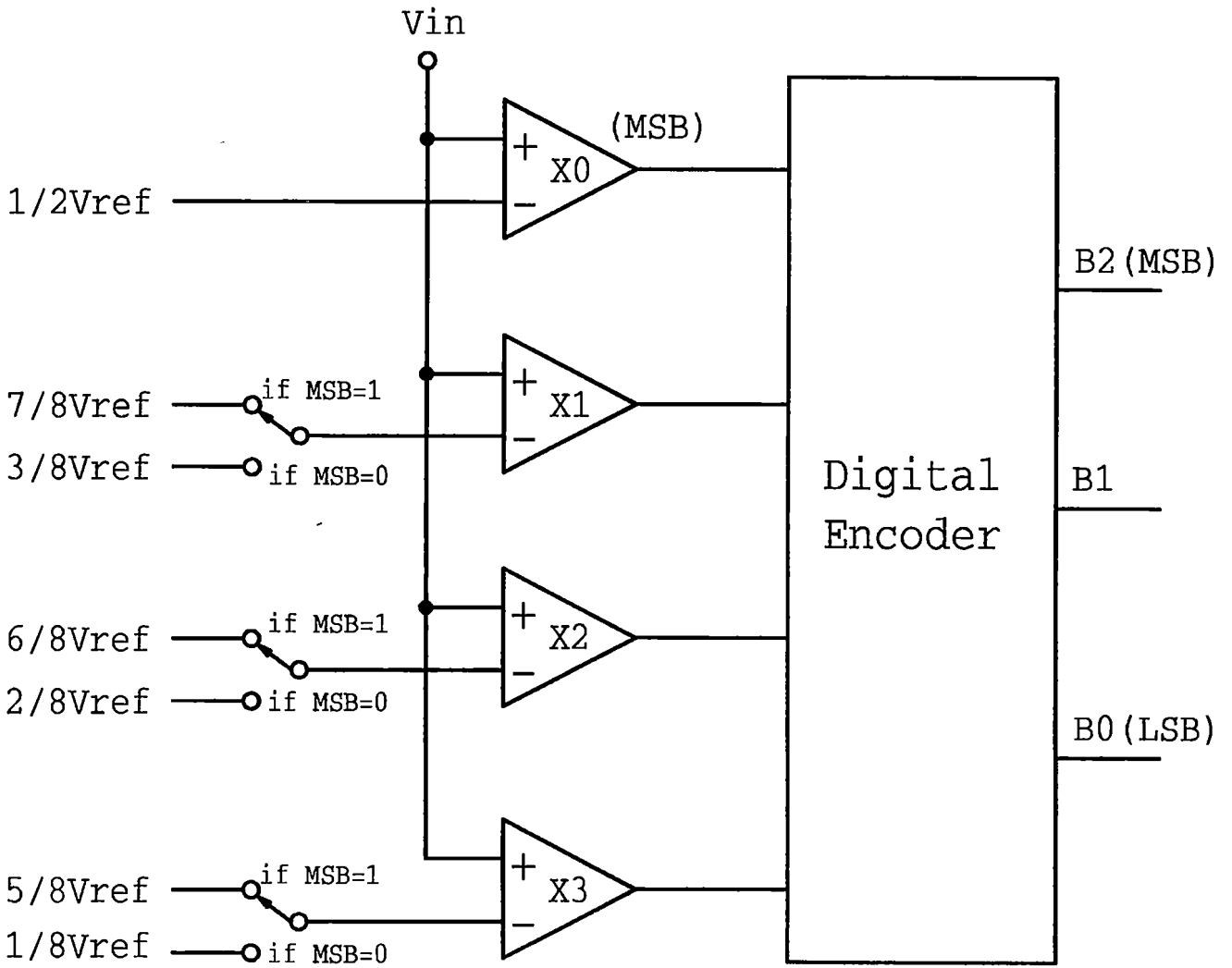


Figure 2-2. Block diagram of a 3-bit two-step flash ADC architecture.

network is omitted from the figure for clarity. The operation of this proposed converter architecture can be described as a two-phase conversion process. The output of the MSB comparator is generated in the first step of the conversion. Next, the MSB decision is used to select the appropriate references for the rest of the comparators (*X1*, *X2*, and *X3*) and the second conversion is made. The comparators *X1*, *X2*, and *X3* will be referred to as other significant bits (OSB) comparators throughout the rest of this work To encode the outputs of the comparators into a final binary output code, the basic truth table of Table 2-2 can be used. Note from the figure that the encoder design is also simplified because of the reduced number of inputs.

This simple two-step flash ADC architecture only requires $2^{(N-1)}$ comparators for an N bit conversion. Therefore, the comparator count is reduced by factor-of-two when compared to the traditional flash ADC architecture. Another advantage of this architecture is that it does not require additional complex circuitry like most other two-step flash ADC architectures. For example, this architecture eliminates the need for a DAC and high-speed amplifier which are typically required in other two-step ADC architectures. Also, the required silicon area for the encoder design is reduced because of the lower number of inputs to the encoder relaxes the design requirements. The main disadvantage of this and all two-step flash ADC architectures is that the latency of the converter is now increased since two sequential conversions are required.

In this work, the two-step flash ADC architecture presented was chosen and customized to meet the requirements of the ADC for the high-performance sub-nanosecond TDC application. This topology can be expanded to 6-bits to meet the

Table 2-2. Truth table for 3-bit two-step flash ADC.

Analog Input Voltage	Comparator Outputs				Digital Code		
Vin	X0	X1	X2	X3	B2	B1	B0
Vin < Vref/8	0	0	0	0	0	0	0
Vref/8 < Vin < 2Vref/8	0	0	0	1	0	0	1
2Vref/8 < Vin < 3Vref/8	0	0	1	1	0	1	0
3Vref/8 < Vin < 4Vref/8	0	1	1	1	0	1	1
4Vref/8 < Vin < 5Vref/8	1	0	0	0	1	0	0
5Vref/8 < Vin < 6Vref/8	1	0	0	1	1	0	1
6Vref/8 < Vin < 7Vref/8	1	0	1	1	1	1	0
7Vref/8 < Vin < Vref	1	1	1	1	1	1	1

required resolution of the ADC. Since this two-step flash ADC architecture requires $2^{(N-1)}$ comparators, a 6-bit converter implementation will require thirty-two comparators which will consist of one MSB comparator and thirty-one OSB comparators. Figure 2-3 shows a preliminary timing diagram to meet the 15.625 MHz conversion rate with a latency of one 16 ns clock cycle. The MSB comparator has 24 ns to compare the analog input voltage with $½V_{ref}$. A total time period of 16 ns is allowed for the interpretation of the MSB output and the selection of reference voltages for the OSB comparators. The OSB comparators are allowed 24 ns of conversion time. These time periods consume the entire allotted time of 64 ns that the analog input voltage will be available to the ADC As a result, the encoding of the comparator outputs is performed during the allowed latency period of one clock cycle.

A block diagram of the 6-bit 15.625 MHz CMOS two-step flash ADC architecture is shown in Figure 2-4. The architectural requirements of the ADC can be divided into four major sections of development: MSB and OSB comparator design, reference generation and selection network, encoder design with digital error correction, and control logic. The development and performance requirements of these sections will be presented with special emphasis placed on the design and analysis of an auto-zeroed CMOS comparator.

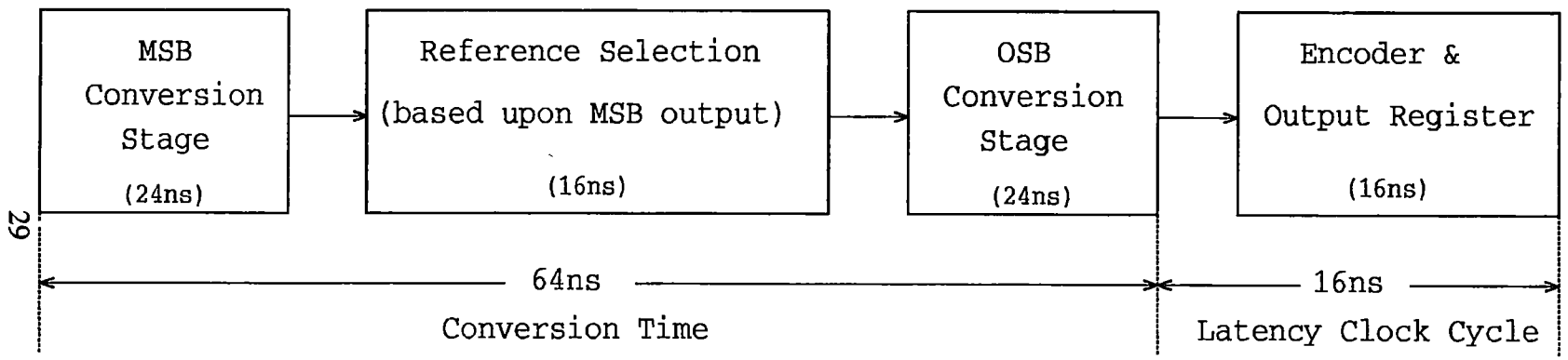


Figure 2-3. Preliminary timing diagram of proposed 6-bit two-step flash ADC.

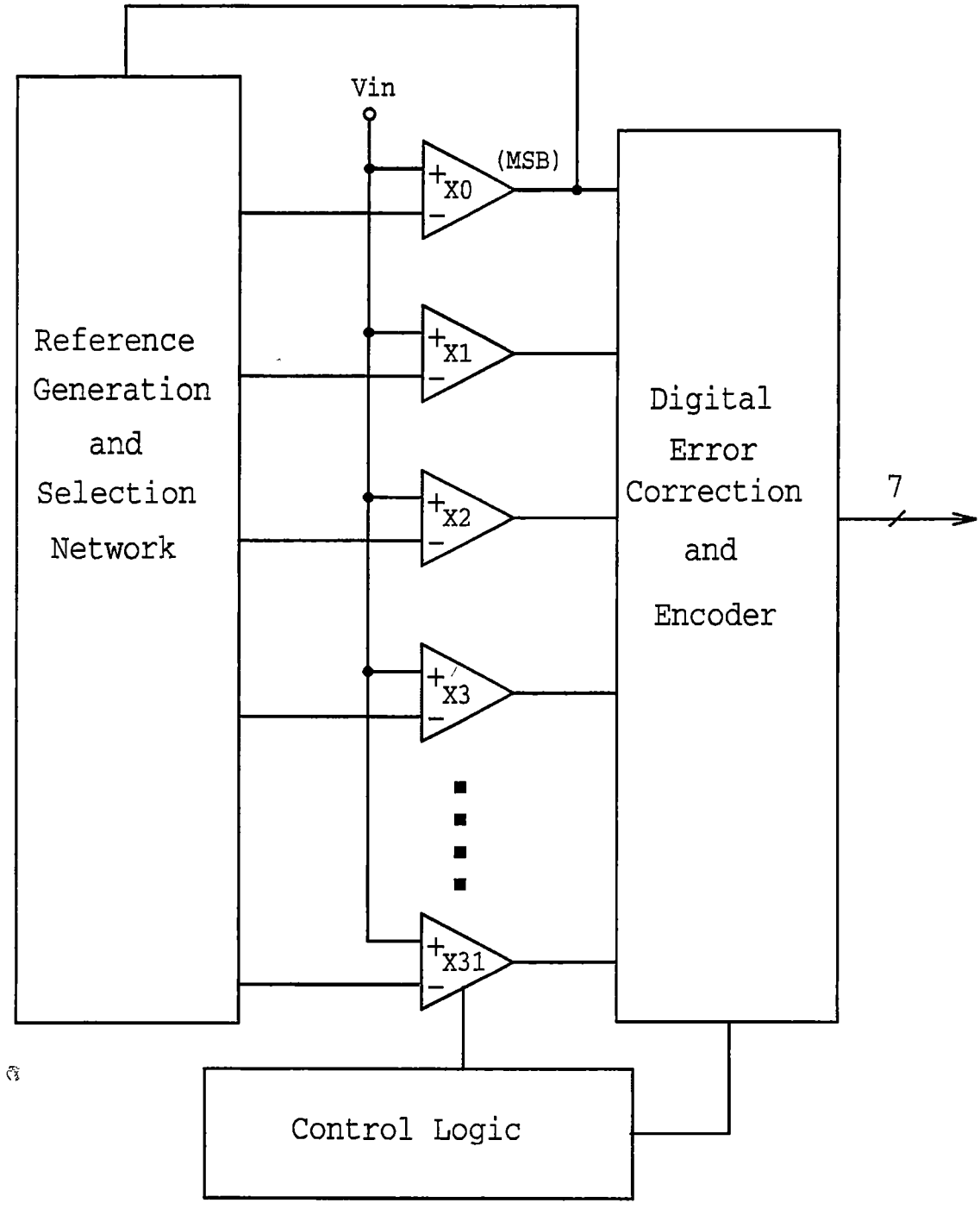


Figure 2-4. Block diagram of the 6-bit two-step flash ADC architecture.

Chapter 3

ADC Design and Analysis

3.1 Comparator Design and Analysis

3.1.1 Comparator Overview and Fundamentals

A comparator is a circuit that compares two analog signals and outputs a binary signal based upon the comparison. Thus, a comparator can be thought of as a decision making circuit. Most comparators are considered nonlinear circuits since the inputs are not linearly related to the outputs. A comparator is not purely analog or digital and is considered a mixed-signal circuit since it interfaces analog signals to digital circuitry.

The schematic symbol and basic operation of a voltage comparator is shown in Figure 3-1. If the positive input signal, V_{in}, of the comparator is at a greater potential than the negative input, V_{ref}, then the output of the comparator is a logical 1 Conversely, if the positive input of the comparator is at a potential less than the negative input, then the output of the comparator is a logical 0 Thus, a comparator is used to determine whether a given signal is larger or smaller than another signal. Fundamentally, a comparator can be thought of as a one bit ADC since it takes an analog signal and generates a digital output.

The basic function of the comparator is that of providing sufficient amplification to generate digital output levels in response to small analog input differences Depending upon the application, the amplification process of the comparator does not need to be linear and not necessarily continuous in time. Also, in applications where latency can be tolerated, the amplification process can be achieved by several cascaded amplifier stages.

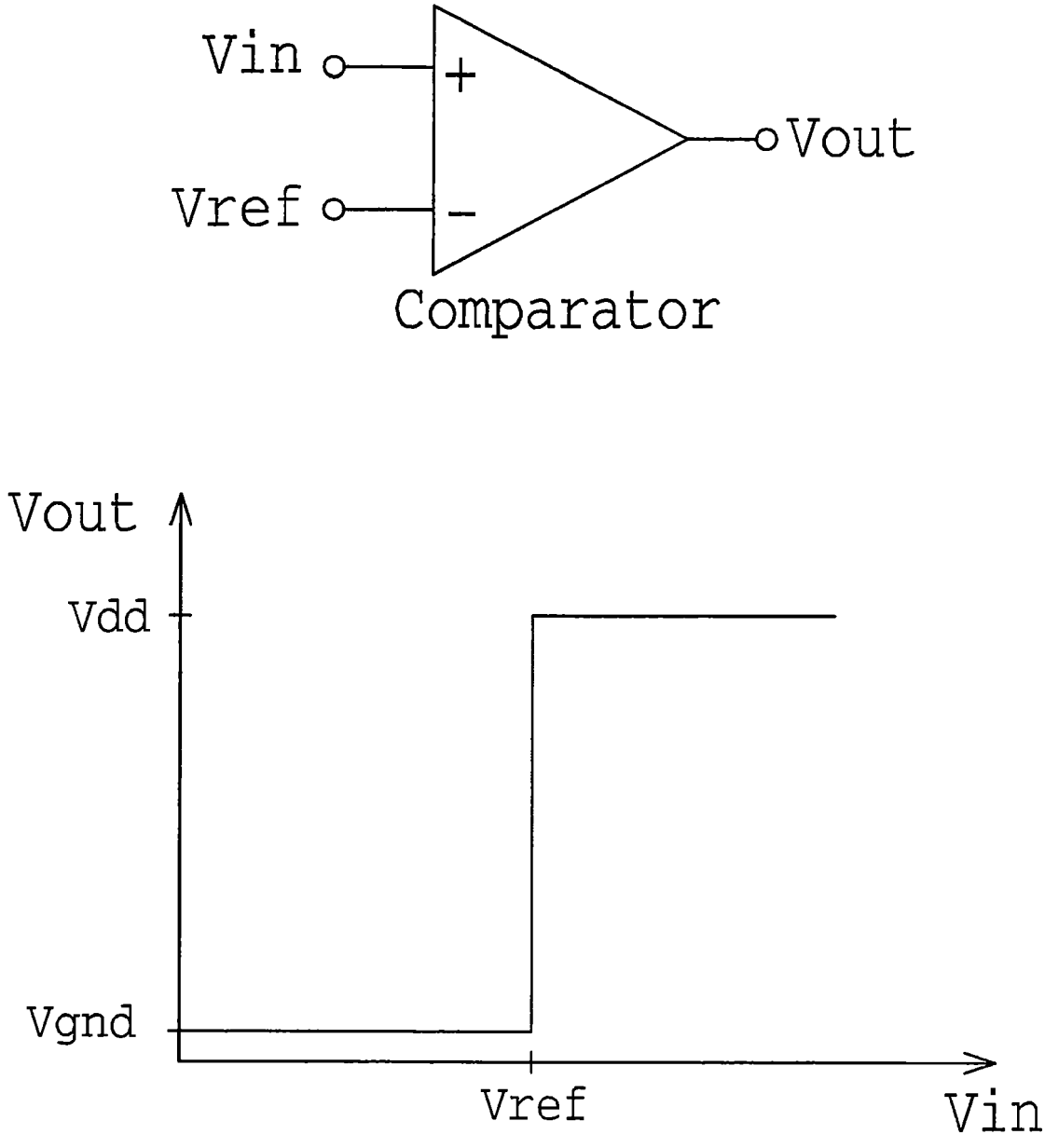


Figure 3-1. Circuit symbol and transfer function of an ideal voltage comparator.

In most data conversion systems, the comparator decision time is not arbitrary and must be made within a specified time interval. Therefore, most data converter comparators employ regeneration through positive feedback to make a decision in a timely manner. In fact, Lim and Wooley have reported that in order to achieve a minimum power-delay product, the amplification process in a comparator is best obtained by means of regeneration [28]. The comparator development presented here will focus on the application in a high-performance parallel ADC architecture and realizations that can be readily implemented in CMOS technology.

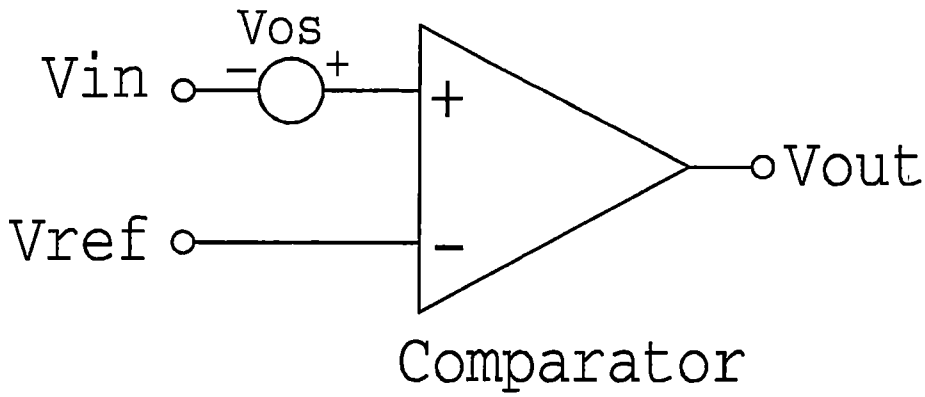
The performance of ADCs is generally limited by the speed and precision with which the function of comparison can be made. Therefore, the design and performance of a comparator is a critical and often limiting component in the design of high-speed data conversion systems. Converter architectures that incorporate a large number of comparators in parallel, such as a flash ADC architecture, to obtain high throughput impose very stringent conditions and constraints on the comparator performance. Key specifications and design parameters of a comparator commonly include: propagation delay, resolution, input offset voltage, power dissipation, area, input common-mode range, and input impedance. As typical in the design process, several tradeoffs between these parameters must be made when designing a comparator for a particular application.

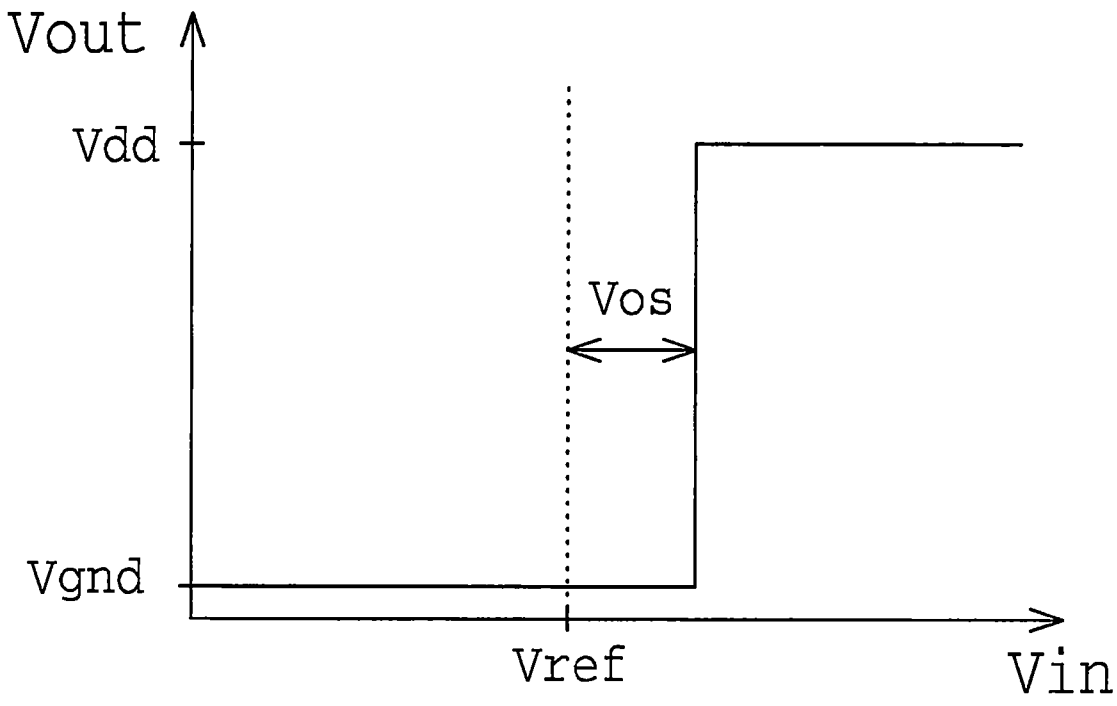
3.1.2 Motivation for an Auto-zeroed Comparator

A particular difficulty encountered in the design and performance of a CMOS comparator is that of the input offset voltage. The comparator transfer function including

the input offset voltage effects is shown in Figure 3-2. The output does not change until the input difference of the comparator has reached a value of V_{OS}. The input offset voltage of a comparator is caused by two components: random offset and systematic offset effects. Random offsets are caused by device mismatch, such as transistor threshold voltage mismatch due to process gradients. Systematic offsets are present even when all devices are assumed ideal and no process variations exist These offsets can be a result of charge injection, clock coupling, substrate noise, or could be inherent in the design of the comparator. Both of these offset effects can be minimized through careful circuit design, but typically can not be completely eliminated. For precision applications, such as a high-resolution ADCs, the comparator's offset voltage can severely limit the performance and operation of the converter. If the input offset voltage of a comparator could be predicted and well controlled, it could be managed much more easily through simple calibration techniques. However, most of the time the offset of the comparator varies randomly from circuit to circuit for a given design. Due to the fact that the chosen ADC architecture requires many comparators in parallel, the random distribution of the comparators offset voltages can completely distort the linearity of the output data.

One of the most fundamental issues in the selection of a CMOS comparator topology is the decision whether to employ offset cancellation techniques to the comparator. This decision should be based upon the desired resolution of the converter relative to the anticipated offset voltage of the comparator and the required linearity performance of the converter. A well-informed, intelligent decision cannot be made based solely upon the number of bits of a given converter. For example, due to the





If Vin>(Vref+Vos) then Vout=Vdd

If Vin<(Vref+Vos) then Vout=Vgnd

Figure 3-2. Ideal comparator transfer function including offset voltage effects.

difference in required resolution, an 8-bit converter may not require offset corrected comparators in one particular application, while a 4-bit converter may require offset correction techniques in another application.

The relationship between the non-linearity errors of a flash or flash-type converter, the required resolution, and the comparator offset voltages can be developed. Consider two consecutive comparators in a flash or flash-type architecture shown in Figure 3-3. The output of comparator *X1* changes from 0 to 1 when $V_{in} > V_{r1} - V_{OS1}$. For comparator *X2*, the output change occurs when $V_{in} > V_{r2} - V_{OS2}$. The transition of one comparator ideally takes place when the input voltage, V_{in}, reaches its reference voltage. However, the actual transition occurs when V_{in} reaches $V_r - V_{OS}$. This deviation between the ideal transition and the actual transition is called integral non-linearity (INL) The INL error associated with one comparator is, its input offset voltage, V_{OS}, plus any error in the reference voltage, V_r, and is usually expressed as a fraction of a least significant bit (LSB).

The LSB of an ADC is defined as

$$LSB = \frac{V_{ref}}{2^N}, \tag{3-1}$$

where V_{ref} is the reference voltage, equal to the ADC input voltage range, and N is the number of bits of the converter [25]. Considering comparator offset voltages and reference generation errors, the INL of a flash or flash-type ADC expressed as a fraction of a LSB can be written as

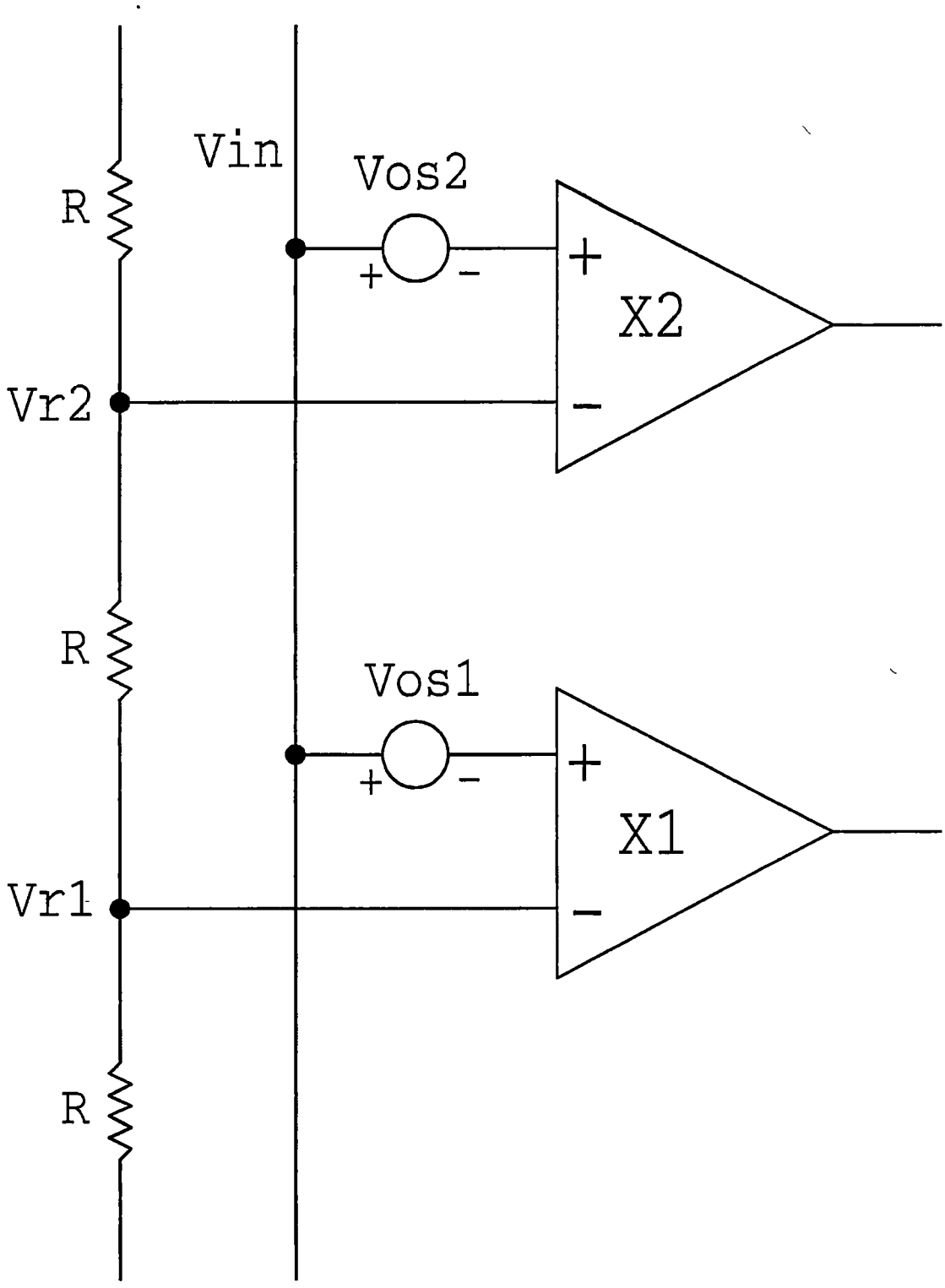


Figure 3-3. Two adjacent comparators in a flash or flash-type ADC architecture.

$$INL = \frac{|V_{OS}| + |Vr_{actual} - Vr_{ideal}|}{1\,LSB} = \frac{|V_{OS}| + |\Delta Vr|}{\frac{V_{ref}}{2^N}} \quad . \tag{3-2}$$

Assuming the reference voltage, V_r, is ideal, the INL expressed as a fraction of a LSB simplifies to the expression

$$INL = \frac{|V_{OS}|}{1\,LSB} = \frac{|V_{OS}|}{\frac{V_{ref}}{2^N}} \quad . \tag{3-3}$$

The differential non-linearity (DNL) can be defined by considering the input values for which two consecutive comparators, *X1* and *X2*, change their output state. These values are $V_{r1} - V_{OS1}$ and $V_{r2} - V_{OS2}$ and the deviation of their difference with respect to their ideal value, $\frac{V_{ref}}{2^N}$, is the DNL. The DNL expressed as fraction of a LSB can be written as

$$DNL = \frac{1}{1\,LSB}\left| (V_{r2} - V_{OS2}) - (V_{r1} - V_{OS1}) - \frac{V_{ref}}{2^N} \right| . \tag{3-4}$$

If the references, V_{r1} and V_{r2}, are assumed to be ideal, then

$$(V_{r2} - V_{r1}) = \frac{V_{ref}}{2^N} \quad , \tag{3-5}$$

and the DNL expression can be simplified to

$$DNL = \frac{|V_{OS1} - V_{OS2}|}{1\,LSB} = \frac{|V_{OS1} - V_{OS2}|}{\frac{V_{ref}}{2^N}} \quad . \tag{3-6}$$

The derivation of Equations 3-3 and 3-6 illustrates the relationship between the comparator offset voltages, the resolution of the ADC, and the non-linearity

specifications of the ADC. Note that in general the DNL specification imposes a more stringent requirement on the offset voltage of the comparator, V_{OS}, than an INL specification of equal value.

Another important specification of an ADC is that of no missing codes The condition of no missing codes refers to the fact that every ADC output code is present and represented. Figure 3-4 illustrates an ADC transfer function with a missing code. From the figure, it is evident that to satisfy the condition of no missing codes, the condition

$$|V_{OS1} \pm V_{OS2}| < V_{r2} - V_{r1} \tag{3-7}$$

must be satisfied. Again if the references, V_{r1} and V_{r2}, are assumed ideal, then the equation for the condition of no missing codes can be simplified to

$$|V_{OS1} \pm V_{OS2}| < \frac{V_{ref}}{2^N} \ . \tag{3-8}$$

Most of the time a missing code is caused by excessively large differential non-linearity errors. If the DNL of an ADC is less than ±1 LSB, then the condition of no missing codes is guaranteed. This application requires a DNL specification of ±½ LSB. Therefore, the condition of no missing codes is already represented by the DNL specification.

Based upon the linearity analysis presented, the calculation of the maximum allowable comparator offset voltage to meet the desired INL and DNL specifications of the converter can be performed by utilizing Equations 3-3 and 3-6. These foregoing equations can be used to derive conclusions concerning the implementation and architectural selection of a comparator in the design of ADCs employing parallel

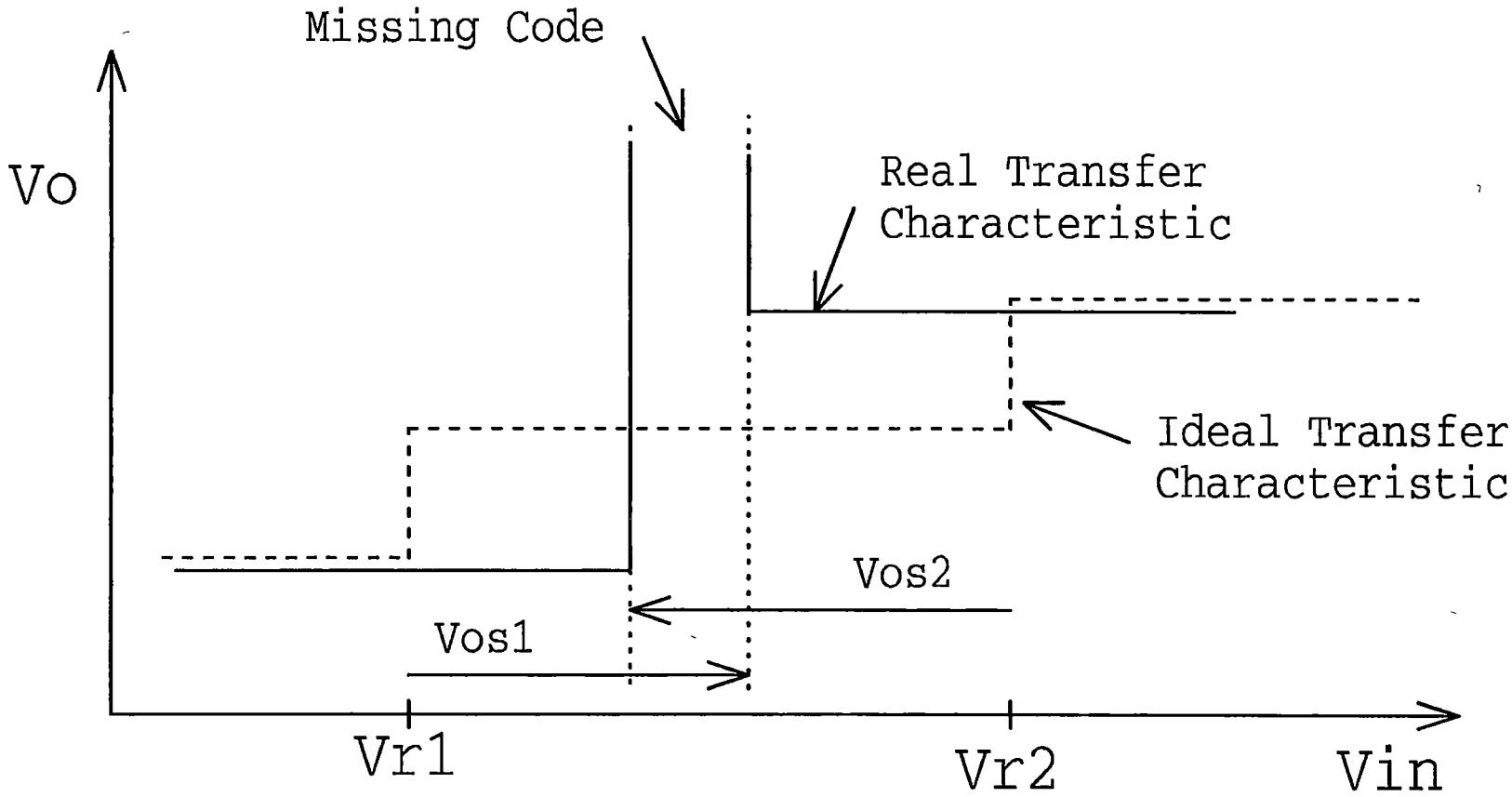


Figure 3-4. ADC transfer function with a missing code due to excessively large comparator offsets.

conversion stages

For this particular application, the nominal reference voltage, V_{ref}, is 1.275 V and the number of desired bits, N, is 6. Therefore, the LSB of the ADC can be calculated as

$$1\,LSB = \frac{1.275\,V}{2^6} \approx 20\,mV\ , \tag{3-9}$$

which results in a 20 mV/LSB resolution. To achieve the desired INL specification of ±½ LSB (±10 mV), the maximum allowable comparator offset can be calculated as

$$\left|V_{OS}\right| < 10\,mV\ . \tag{3-10}$$

Similarly, the maximum allowable offset voltage of two consecutive comparators to achieve the required DNL specification of ±½ LSB (±10 mV) can be calculated as

$$\left|V_{OS1} - V_{OS2}\right| < 10\,mV\ . \tag{3-11}$$

If we assume that V_{OS1} and V_{OS2} are statistically independent random variables with zero average and equal standard deviation $\sigma(V_{OS1}) = \sigma(V_{OS2}) = \sigma(V_{OS})$, then

$$\sigma(V_{OS1} - V_{OS2}) = \sqrt{2}\sigma(V_{OS})\ , \tag{3-12}$$

and Equation 3-11 can be expressed as

$$\sigma(V_{OS1} - V_{OS2}) = \sqrt{2}\sigma(V_{OS}) < \frac{1}{2}\,LSB\ . \tag{3-13}$$

Solving Equation 3-13 for the necessary standard deviation of the offset voltage to ensure a DNL specification of ±½ LSB (±10 mV) yields

$$\sigma(V_{OS}) < 7\,mV\ . \tag{3-14}$$

For good yield performance over extreme process conditions, we should impose a three sigma value of

$$3\sigma(V_{OS}) < 7\,mV \tag{3-15}$$

to satisfy the given INL and DNL specifications. Therefore, the required standard deviation of the offset voltage now becomes

$$\sigma(V_{OS}) < 2.33\,mV\ . \tag{3-16}$$

As Equations 3-10 and 3-16 illustrate, the standard deviation for each comparator's offset voltage is a very critical and crucial parameter to know in order to achieve good accuracy and linearity performance of a flash or flash-type ADC architecture.

A rough estimate of the offset voltage presented by a comparator can be performed if some basic assumptions about the offset phenomenon are made. The first simplification is that the random offset component of the comparator's offset voltage is the dominant source of error and therefore the systematic offset component is completely negligible. Also, if the input-referred offset voltage of a comparator is assumed to be dominated by the differential input transistor pair, then MOSFET transistor threshold voltage mismatch is the dominant source of offset voltage error. (As will be explained later in this chapter, these are not necessarily always good assumptions and will result in a very optimistic calculation. However, using these assumptions will provide an approximate offset voltage anticipated for a given comparator.) If these assumptions are granted, then the standard deviation of the random component of a comparator's offset voltage can be calculated using matching theory [29, 30]. The equation that predicts threshold voltage mismatch of adjacent devices with equal layout area is

$$\sigma(\Delta V_T) = \frac{A_{VTO}}{\sqrt{Weff \cdot Leff}}\ , \tag{3-17}$$

where A_{VTO} is a constant and *Weff* and *Leff* are the effective channel width and length of the device, respectively. For submicron processes, reported values of A_{VTO} have been around the value of 25 mV μ [22]. Using this expression, one can calculate the required transistor area to achieve the necessary threshold voltage matching for a low offset comparator. Assuming that $\sigma(\Delta V_T) \approx \sigma(V_{OS})$ and the application requirement of $\sigma(V_{OS}) < 2.33\,mV$, the required input transistor dimensions can be expressed as

$$Weff \cdot Leff = \left[\frac{A_{VTO}}{\sigma(V_{OS})}\right], \tag{3-18}$$

and substitution of parameters yields

$$Weff \cdot Leff = \left[\frac{25\,mV \cdot \mu}{2.33\,mV}\right]^2 \approx 115\,\mu^2 . \tag{3-19}$$

This optimistic calculation illustrates the requirement for very large input devices of the comparator needed to achieve sufficient matching accuracy to guarantee an offset voltage, $\sigma(V_{OS})$, of less than 2.33 mV. Consequently, these devices will occupy a fair amount of silicon area and present a large input capacitance. Also, depending upon the actual selection of transistors sizes for the input pair, these transistors could also consume a large current for strong inversion operation. It is important to note that this calculation also assumes ideal reference voltage generation for the comparators. In reality, the voltage references provided for the comparators will be non-ideal and therefore the maximum allowable comparator offset voltage will be reduced. Also, unless sufficient statistical data is available for the A_{VTO} parameter of a given process, it is questionable whether low offset voltages can be achieved over extreme process conditions Although

others have reported successful ADC implementations at the 6 to 8 bit level without the use of auto-zeroed or offset corrected comparators, it was decided to employ offset correction techniques instead of intensive transistor dimension optimization to achieve acceptable comparator offset performance for this application [18, 22].

3.1.3 Limitations of Offset Cancellation Due to Charge Injection

CMOS technology provides the advantages of simple zero-offset, low leakage analog switches, high-impedance charge storage nodes, and complementary devices This analog sampling capability inherent in CMOS technology provides a means whereby offsets can be periodically sensed, stored, and then subtracted from the input signal These CMOS characteristics allow for the extensive use of circuit techniques for comparator offset cancellation. Comparator offset correction techniques are intended to achieve improved resolution and speed, while maintaining low power dissipation, small area and input capacitance, and low complexity.

Perhaps the major limitation on the offset cancellation process of a comparator is due to charge injection. This error is a result of unwanted charges that are injected into a circuit when transistor switches turn off. In CMOS technology, switches are usually implemented by either using a single NMOS or PMOS transistor or by a CMOS transmission gate that is composed of both a NMOS and PMOS device connected in parallel. Examples of these possible switch configurations are shown in Figure 3-5. All of these switches have their particular application which usually depends upon the desired pass signal voltage levels.

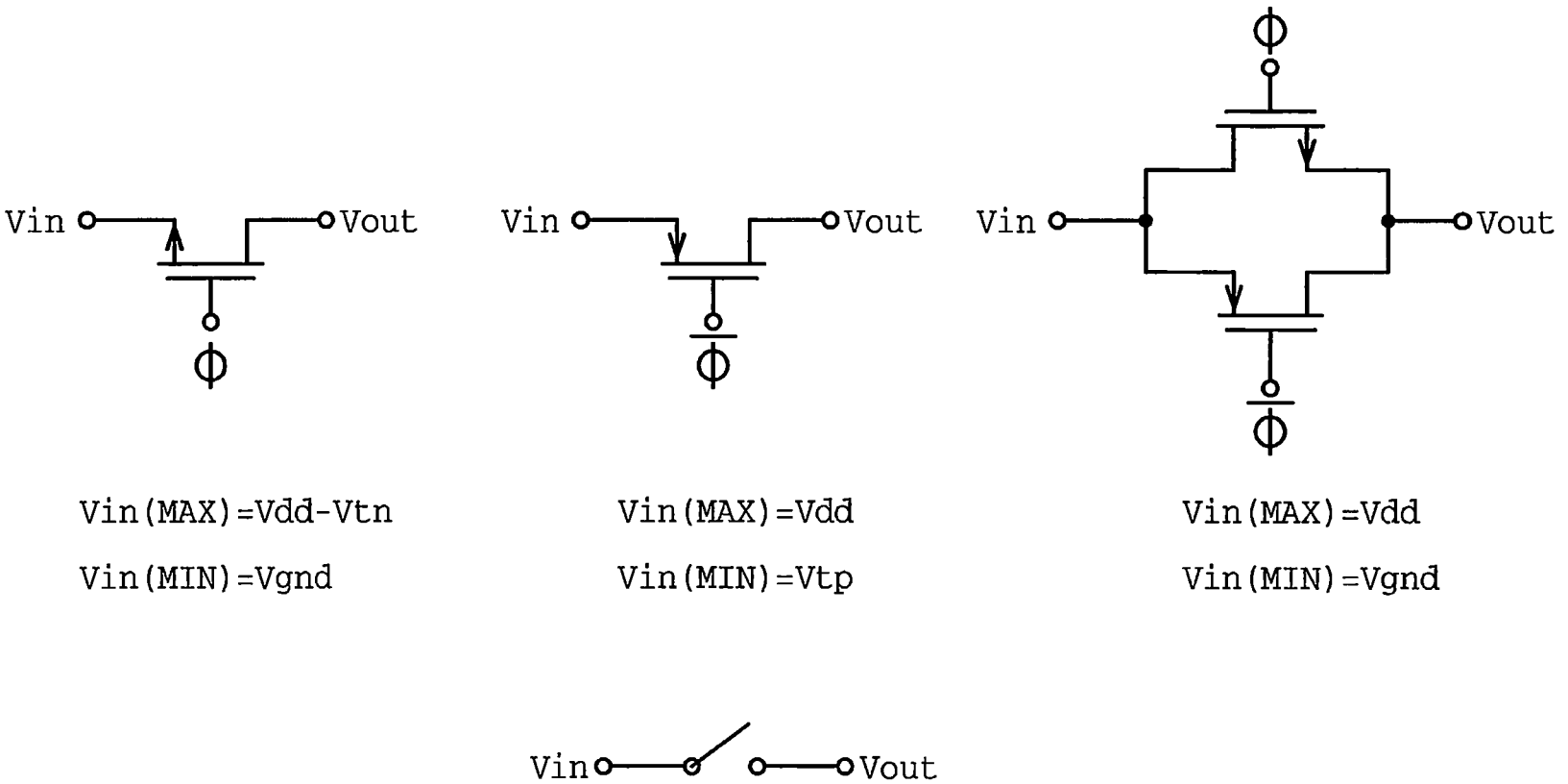


Figure 3-5. Typical analog switch configurations available in CMOS technology.

Unfortunately, the non-ideal effects typically associated with these CMOS switches can be significant and may ultimately limit the performance of some high precision circuits. The charge injection errors associated with CMOS switches are caused by two mechanisms known as channel charge injection and clock feedthrough

3.1.3.1 Channel Charge Injection Effects

The channel charge injection effect usually dominates the overall charge injection error and can be understood with the help of Figure 3-6. When the control signal $V_{CONTROL}$ is high or a logical 1, the NMOS device is in the ohmic region resulting in a very small V_{DS} of the device. Under this condition, the switch or transistor is considered to be on and charge is accumulated under the gate oxide of the device. The channel charge of a transistor that has zero V_{DS} is given by

$$Qch = W\ L\ C_{OX} \cdot (V_{GS} - V_T)\ , \tag{3-20}$$

where W and L are the device dimensions, C_{OX} is the gate oxide capacitance, and $(V_{GS} - V_T)$ is the gate overdrive of the device [24]. When the control signal is taken low or a logical 0, the NMOS transistor turns off and this channel charge must flow out of the channel region through the source and drain junctions of the transistor As a result, a portion of this charge is injected onto the hold capacitor, C_h, and the input signal, V_{in} If the control signal waveform is fast, this channel charge distributes equally between the two connecting nodes [31, 32]. Therefore, half of the channel charge is injected on C_h and the other half to the input signal generator. Since V_{in} is typically a low impedance node, the injected charge has little or no effect on this node. However, the *Qch/2* charge

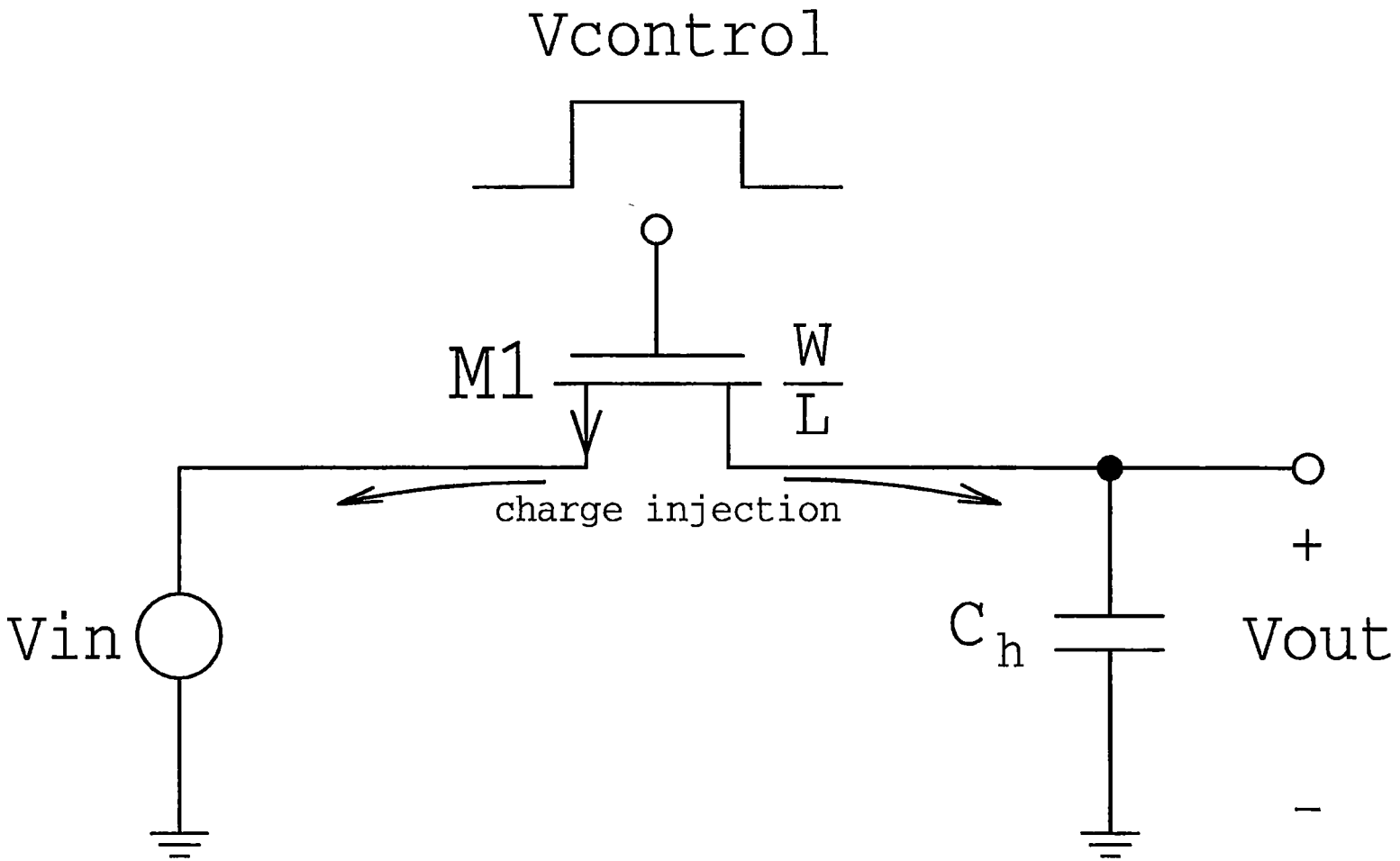


Figure 3-6. Simple circuit configuration using a NMOS switch to illustrate channel charge injection effects.

injected onto the hold capacitor results in a corresponding voltage change that introduces an error. Since in this example, a NMOS transistor is used as the switch, this injected charge is negative and will cause a decrease in voltage across the hold capacitor. The voltage change due to channel charge injection is given by the expression

$$\Delta V_{CCI} = \frac{\frac{Qch}{2}}{C_h} = \frac{-W\ L \cdot C_{OX}\ (V_{GS} - V_T)}{2\ C_h}\ , \tag{3-21}$$

and can be calculated for a given transistor switch size, hold capacitor, and input signal voltage [24]. If CMOS logic levels are used for the transistor control signal, then Equation 3-21 can be simplified to

$$\Delta V_{CCI} = \frac{-W\ L \cdot C_{OX}\ [Vdd - V_{in} - V_T]}{2 \cdot C_h}\ . \tag{3-22}$$

The current form of Equation 3-22 can sometimes mask a subtle problem associated with charge injection. At first glance it might appear as if the charge injection is linearly related to the input signal. However, the threshold voltage of the NMOS device is dependent upon the input signal voltage level due to the body effect of the device. Modifying Equation 3-22 to include the transistor threshold voltage dependence upon the input signal results in

$$\Delta V_{CCI} = \frac{-W\ L \cdot C_{OX}\ \left[Vdd - V_{in} - \left(V_{TO} + \gamma\left(\sqrt{2\phi_F + V_{in}} + \sqrt{2\phi_F}\right)\right)\right]}{2 \cdot C_h} \tag{3-23}$$

Thus, the voltage change across C_h caused by channel charge injection is dependent upon the input signal in a nonlinear relationship. Since channel charge injection is input signal dependent, complete cancellation of channel charge injection is very difficult to achieve for varying ranges of input signal conditions.

3.1.3.2 Clock Feedthrough Effects

The other component of charge injection is clock or capacitive feedthrough. This effect can be explained through the use of Figure 3-7. Illustrated in the figure are the gate-to-diffusion overlap capacitances associated with a MOS transistor. Clock feedthrough occurs on each transition of the clock or control signal edge. When the gate control signal switches, the clock signal feeds through the C_{ov1} and C_{ov2} overlap capacitances onto the source and drain nodes. However, this effect is usually only of concern when the control signal transition is in a direction to turn the switch off. This is because when the transistor is turned on, the capacitor C_h will charge to the correct final value regardless of the injected charge from the clock signal. Thus, the result is that capacitive feedthrough has no effect on the circuit when the switch is turned on. However, when the transistor turns off, the capacitive divider that exists between the C_{ov2} capacitance and the hold capacitance will couple the clock signal from the gate to the storage node and introduces an error which in some cases can be significant.

One can use capacitive voltage division to calculate the change in voltage across the C_h capacitor due to the clock feedthrough phenomenon [24]. Applying this to the circuit of Figure 3-7 results in

$$\Delta V_{CFT} = \frac{\Delta V_{in} \cdot C_{ov2}}{C_{ov2} + C_h} = \frac{(Vgnd - Vdd)\ C_{ov2}}{C_{ov2} + C_h}\ , \qquad (3\text{-}24)$$

which is just capacitive voltage division between the gate-to-diffusion overlap capacitance and the hold capacitor. This voltage excursion is typically less than the channel charge injection component of charge injection because C_{ov2} can be kept relatively small when compared to the capacitor C_h. However, for high-precision signal

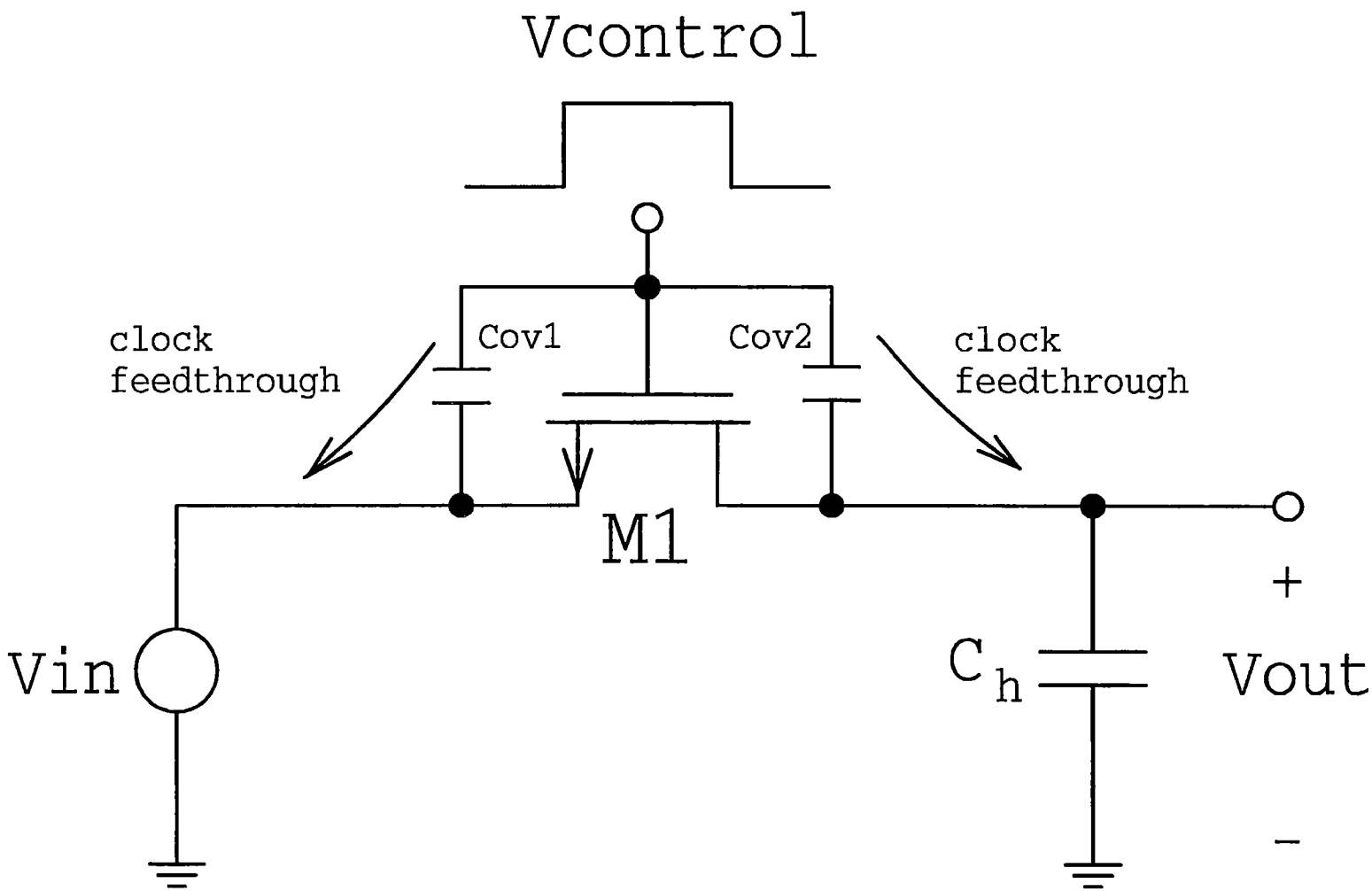


Figure 3-7. Simple circuit configuration using a NMOS switch to illustrate capacitive feedthrough effects.

processing circuits both components of charge injection must be considered and minimized.

3.1.3.3 Techniques to Minimize Charge Injection in CMOS Circuits

To illustrate the significance of charge injection errors in CMOS circuits, an example calculation will be performed. Assume in Figure 3-6 or Figure 3-7 the following conditions: C_h=0.5 pF, C_{OX}=2.11 fF/μm^2, W_1=2.5 μm, L_1=0.8 μm, $C_{ov1} = C_{ov2}$=0.525 fF, V_T=0.8 V, Vdd=5 V, and V_{in}=2.5 V. These are typical parameters in a 0.8 μm CMOS process. Based upon these conditions, the channel charge injection component can be calculated using Equation 3-22 and is given by

$$\Delta V_{CCI} = \frac{-(2.5\,um)\cdot(.8\,um)\ \ (2.1\,fF/um^2)\cdot[5\,V-2.5\,V-0.8\,V]}{2\ \ 500\,fF} = -7\,1\,mV \ . \quad (3\text{-}25)$$

The clock feedthrough error component of charge injection can be calculated using Equation 3-24 and is given by

$$\Delta V_{CFT} = \frac{(-5\,V)(0.525\,fF)}{500\,fF + 0.525\,fF} = -5.2\,mV \ . \quad (3\text{-}26)$$

Thus the total charge injection error due to the non-ideal effects of the NMOS switch can be found by adding the results of Equations 3-25 and 3-26, which sums to

$$\Delta V_{ERROR} = \Delta V_{CCI} + \Delta V_{CFT} = (-7.1\,mV) + (-5.2\,mV) = -12.3\,mV \ . \quad (3\text{-}27)$$

The result of Equation 3-27 shows a charge injection error that is about factor-of-five larger than the allowed corrected comparator offset voltage. Obviously, additional measures must be taken in order to minimize the effects of charge injection errors in offset correction circuits.

Based upon Equations 3-22 and 3-24, both components of charge injection can be reduced by the use of largest possible capacitors values, the use of minimum geometry switches, and keeping control signal levels as small as possible. However, these obvious solutions to minimize charge injection are sometimes very difficult to satisfy and still meet high-performance design requirements. Therefore, certain design compromises must always be made. For example, linear capacitors on an integrated circuit require a large amount of silicon area and these capacitors typically have large (10-15%) parasitic capacitances associated with them. These parasitic capacitances can be significant and can reduce the bandwidth performance of circuits. As a result, capacitors cannot just be made arbitrarily large to reduce charge injection effects. In addition, the reduction in control signal voltages to minimize charge injection drastically reduces the dynamic range of single device switches and thus the signal processing circuits. Also, minimum size switches cannot always be used either. These small switches usually have a high switch on resistance that can create non-negligible time constants on critical nodes in a circuit. Therefore, other solutions to minimize charge injection errors must be utilized. Since charge injection limits the performance of offset cancellation techniques in comparators and other circuits, many methods have been reported to reduce its effects

One of the most common charge injection cancellation techniques is the use of a compensation transistor or dummy switch. This circuit configuration is illustrated in Figure 3-8. Note that two complementary control signals are now required for operation of the switch. Although transistor *M2* has its drain and source connected to the capacitor node, a channel charge is still formed under the gate oxide when a voltage is applied to

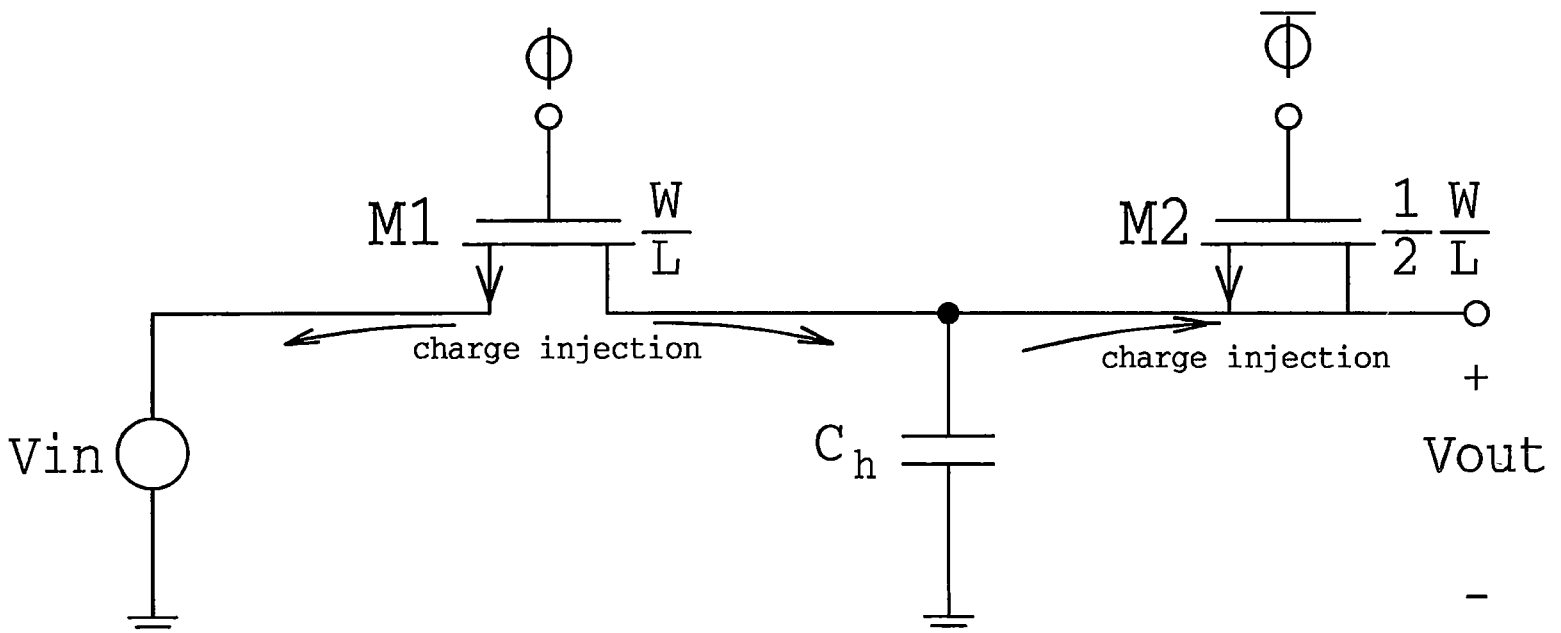


Figure 3-8. Simple circuit illustrating the use of a compensation transistor to minimize charge injection.

the gate of the device. The size of transistor *M2* is designed to provide charge cancellation and is usually selected as half the size of transistor *M1*. As discussed earlier, when transistor *M1* turns off, half of the channel charge is injected onto the hold capacitor. However, with transistor *M2* in the circuit, the charge injected by transistor *M1* is absorbed or matched by the charge induced by the transistor *M2* and the overall channel charge injection is cancelled. Also, this configuration provides partial clock feedthrough cancellation because transistors *M1* and *M2* have complementary clock control signals.

Another common method to counteract charge injection is the use of a CMOS transmission gate as a switch. A CMOS switch contains a NMOS and PMOS transistor in parallel and requires complementary control signals. The use of a CMOS switch offers several advantages over the single device NMOS or PMOS switch. One important advantage is that the dynamic range of the switch is greatly increased The idea of the CMOS switch implementation is that the complementary signals and devices will act to cancel each other's effects and the overall charge injection will be cancelled or at least reduced. Because of this self-compensating feature, the use of a CMOS switch does provide a reduction in charge injection errors when compared to a single device switch. However, complete cancellation is seldom achieved since this requires precise control of the complementary control signals and depends upon the input signal voltage levels which determines whether the NMOS or PMOS transistor is dominant in the CMOS switch.

The best approach for minimizing charge injection errors in circuit design is to

employ fully differential design techniques. When differential design techniques are used, charge injection will only affect the common-mode voltage levels and the differential input signal is unaffected. Since charge injection appears as a common-mode signal, it will be reduced by the common-mode rejection ratio (CMRR) of the amplifier or comparator. Therefore, the only error now present are those due to mismatches in charge injection which are typically a factor-of-ten smaller than the single ended case [26]. As a result, almost all modern high-performance CMOS comparators utilize fully differential architectures. Accordingly, fully differential design techniques will be employed in the comparator development and offset correction process to minimize charge injection errors.

3.1.4 Comparator Offset Cancellation Techniques

A literature review of the conventional approaches to comparator offset correction reveals that most implementations can be classified into three architectures input offset storage (IOS), output offset storage (OOS), and multistage offset storage (MSOS) [33]. All of these topologies comprise of at least one or multiple elements of a preamplifier, offset storage capacitors, and a latch. Each of these methods to achieve offset correction in a fully differential comparator architecture will be discussed and their fundamental tradeoffs and limitations will be presented.

3.1.4.1 Input Offset Storage

An illustration of the IOS architecture applied to a fully differential comparator is

shown in Figure 3-9. Offset cancellation is performed by closing a unity gain loop around the preamplifier *X1* and storing the offsets on the input coupling capacitors *C1* and *C2*. In auto-zero mode, switches *S1* and *S2* are open while switches *S3-S6* are closed. Therefore, the preamplifier must be unity gain stable and may require common-mode feedback (CMFB) to stabilize bias levels. In comparison mode, switches *S1* and *S2* are closed and switches *S3-S6* are open. The offset voltage that is differentially stored on capacitors *C1* and *C2* is combined with the input signal and thus the offset of the comparator is cancelled. The input signal is amplified by the preamplifier and then converted to CMOS logic levels by the latch. During offset cancellation, the input capacitance of the IOS circuit is equal to the offset storage capacitors while in comparison mode it is approximately equal to the sum of the input capacitance of the preamplifier and the parasitic capacitance of the storage capacitor. This parasitic capacitance can be as large as 10-15% of the offset storage capacitor, and therefore is non-negligible when considering the capacitance presented by the preamplifier.

With the IOS architecture, the residual input-referred comparator offset voltage after calibration is given by

$$V_{OS} = \frac{V_{OS1}}{1+A_1} + \frac{\Delta Q}{C} + \frac{V_{OSL}}{A_1}, \tag{3-28}$$

where V_{OS1} is the offset voltage of the preamplifier *X1*, A_1 is the gain of the preamplifier *X1*, ΔQ is the mismatch in charge injection onto capacitors *C1* and *C2* when switches *S5* and *S6* are opened, C is the value of the offset storage capacitors, and V_{OSL} is the offset voltage of the latch. The first term in Equation 3-28 is a result of the limited offset correction available due to the finite gain of the preamplifier. This is analogous with the

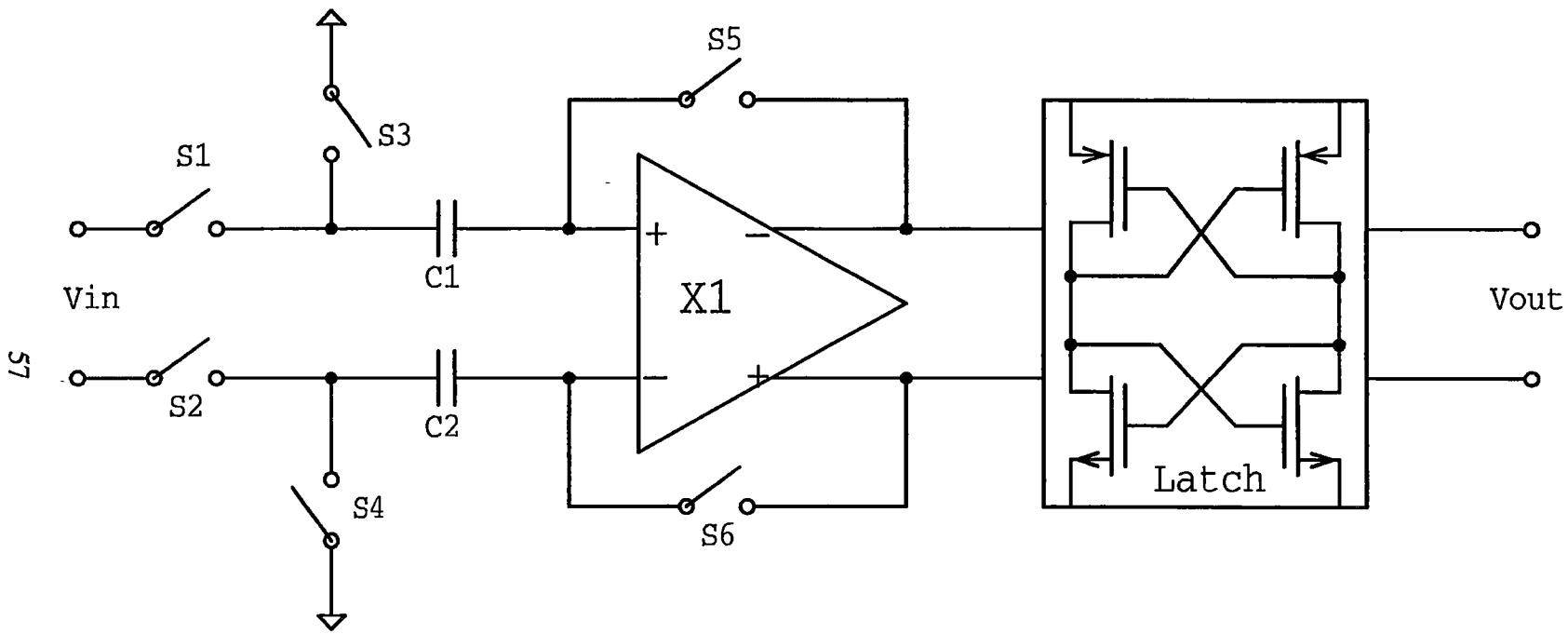


Figure 3-9. Input offset storage calibration technique applied to a fully differential comparator.

fractional error concept associated with operational amplifier theory. Since this architecture employs a fully differential topology, the circuit is only sensitive to the mismatch in charge injection on the storage capacitors and this effect is represented by the second term in Equation 3-28. The second term of Equation 3-28 could also represent any additional errors such as an imbalance in capacitive division or charge injection due to the mismatch in capacitors values of *C1* and *C2*. The last term in the equation is just simply the offset voltage of the latch referred to the input of the preamplifier. Equation 3-28 illustrates that quite large values for A_1 and C are needed to guarantee a low corrected offset voltage.

3.1.4.2 Output Offset Storage

Another common offset cancellation technique is OOS. The OOS architecture applied to a fully differential comparator is shown in Figure 3-10. With OOS, offset cancellation is achieved by connecting the preamplifier inputs and storing the amplified offset voltage onto the output coupling capacitors *C1* and *C2*. In auto-zero mode, switches *S1* and *S2* are open while switches *S3-S6* are closed. Since OOS is an open-loop operation, tight control of the preamplifier gain is required due to finite dynamic range issues in the output stage of the preamplifier. Therefore, the preamplifier of the OOS topology must be designed for a low gain to avoid output saturation and is typically implemented with a gain of less than 10 to ensure operation in the active region over extreme process variations In the comparison mode, switches *S1* and *S2* are closed and switches *S3-S6* are open. The dc coupling at the input of an OOS comparator limits the

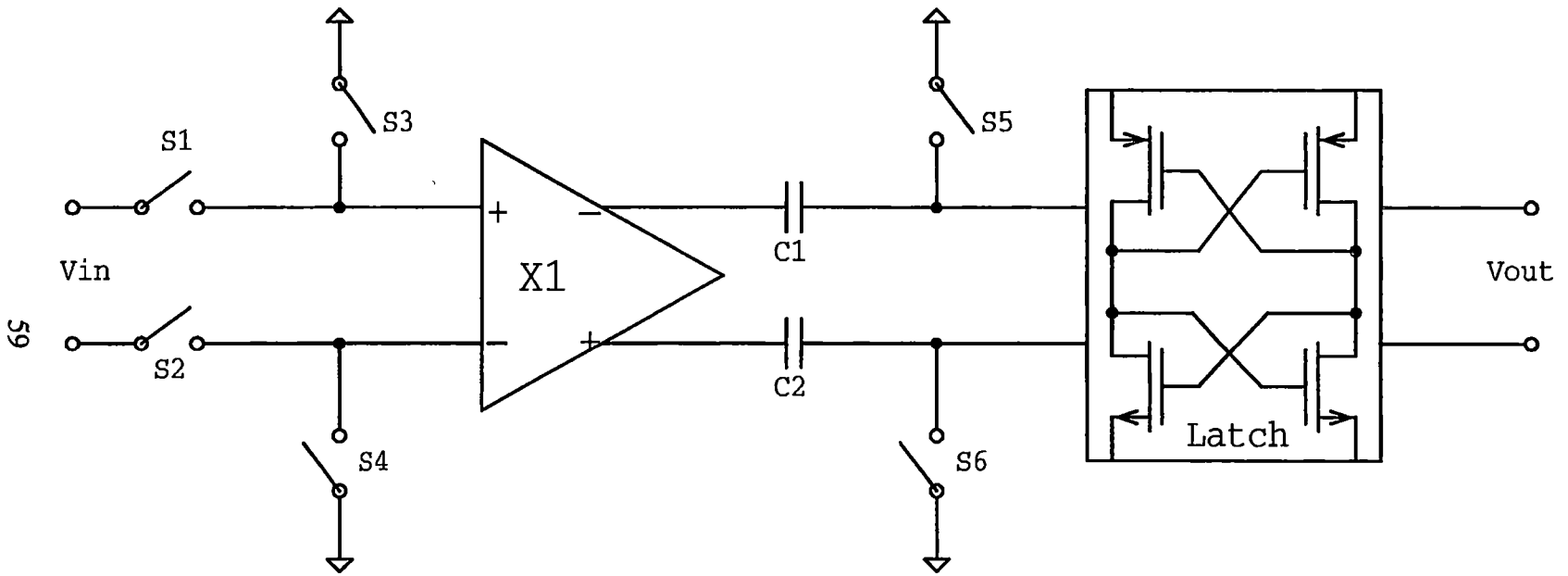


Figure 3-10. Output offset storage calibration technique applied to a fully differential comparator.

common-mode input range (CMIR), but in most cases this limitation is manageable. The input capacitance of the OOS configuration can be very small and is essentially equal to the input capacitance of the preamplifier.

With the OOS architecture, the residual input-referred comparator offset voltage after calibration is given by

$$V_{OS} = \frac{\Delta Q}{A_1 C} + \frac{V_{OSL}}{A_1}, \tag{3-29}$$

where A_1 is the gain of the preamplifier *X1*, ΔQ is the mismatch in charge injection onto capacitors *C1* and *C2* when switches *S5* and *S6* are opened, C is the value of the offset storage capacitors, and V_{OSL} is the offset voltage of the latch. Note that with the OOS circuit configuration, complete cancellation of the preamplifier's offset voltage is achieved. The differential mismatch in charge injection onto the storage capacitors is represented by the second term in Equation 3-29. The second term of Equation 3-29 could also represent any additional errors such as an imbalance in capacitive division or charge injection due to the mismatch in capacitors values of *C1* and *C2*. Note that the sensitivity to mismatches in charge injection and capacitive division is greatly reduced since there effects are decreased by the gain of the preamplifier when referred to the input. The last term in Equation 3-29 is the offset voltage of the latch referred to the input of the preamplifier.

Equations 3-28 and 3-29 illustrate that for similar preamplifiers, the residual comparator offset obtainable with OOS can be smaller than that achievable with IOS Also, the OOS topology does not require a unity gain stable preamplifier to perform the offset correction process. Since the value of input coupling capacitors in a IOS

configuration is dictated by charge injection issues and attenuation considerations, the input capacitance of this topology is usually higher than a OOS circuit configuration. Therefore, the OOS architecture is generally preferable in flash stages where many comparators are connected in parallel.

3.1.4.3 Multi-Stage Offset Storage

In conventional CMOS comparator designs, the preamplifier is typically followed by a standard CMOS latch. The offset voltage of the latch is a potential offset error term for both IOS and OOS comparator architectures. As shown earlier in both of these architectures, the residual comparator offset voltage after calibration is very much dependent upon the offset voltage of the latch stage referred to the input of the comparator. A CMOS latch can have a potentially large offset voltage in the several tens of millivolts (60 mV) and therefore has a non-negligible amount of comparator offset contribution unless a high-gain preamplifier is used [33]. However, neither the IOS or OOS topology will permit the use of a high-gain preamplifier. A high-gain preamplifier cannot be used in a single stage of OOS because of dynamic range issues in the output stage while a single stage of IOS would suffer from degradation in bandwidth performance because of the necessary closed loop compensation required for a high-gain preamplifier. These disadvantages and limitations of the IOS and OOS topologies have led to the development and use of multi-stage offset storage techniques for high-resolution applications

Most typical MSOS comparator topologies just utilize multiple stages of IOS and

OOS that are clocked sequentially to achieve low offset performance. The number of stages is usually selected to provide the smallest propagation delay of the comparator. An illustration of a three stage MSOS architecture applied to a fully differential circuit is shown in Figure 3-11. In this topology, a large latch offset is tolerated through the use of multiple preamplifier stages each with offset cancellation. Preamplifier *X1* utilizes an OOS offset cancellation topology while preamplifiers *X2* and *X3* employ the IOS calibration technique. For dynamic range issues, additional preamplifier stages beyond *X3* would be configured in IOS architectures. Also, these stages would be clocked sequentially following the first two preamplifiers. Figure 3-12 shows a timing diagram for the three stage MSOS architecture. When in auto-zero mode, switches *S1* and *S2* are open and switches *S3-S8* are closed. In compare mode, switches *S5* and *S6* are first opened and their corresponding charge injection is stored on capacitors *C1* and *C2*. This error voltage is then amplified by *X2* and stored on capacitors *C3* and *C4* before switches *S7* and *S8* are opened. Thus, the charge injection of the second stage is completely eliminated. Next, switches *S3*, *S4*, *S7*, and *S8* are all opened and then switches *S1* and *S2* are closed to initiate the actual comparison process.

With the three stage MSOS architecture presented, the residual input-referred comparator offset voltage after calibration is given by

$$V_{OS} = \frac{\Delta Q}{A_1 A_2 C} + \frac{V_{OS2}}{A_1(1+A_2)} + \frac{V_{OS3}}{A_1 A_2 (1+A_3)} + \frac{V_{OSL}}{A_1 A_2 A_3}, \qquad (3\text{-}30)$$

where A_1, A_2, A_3 and V_{OS2}, V_{OS3} are the gains and offsets of the preamplifiers, respectively, ΔQ is the mismatch in charge injection onto capacitors *C3* and *C4* when switches *S7* and *S8* are opened, *C* is the value of the offset storage capacitors, and V_{OSL} is

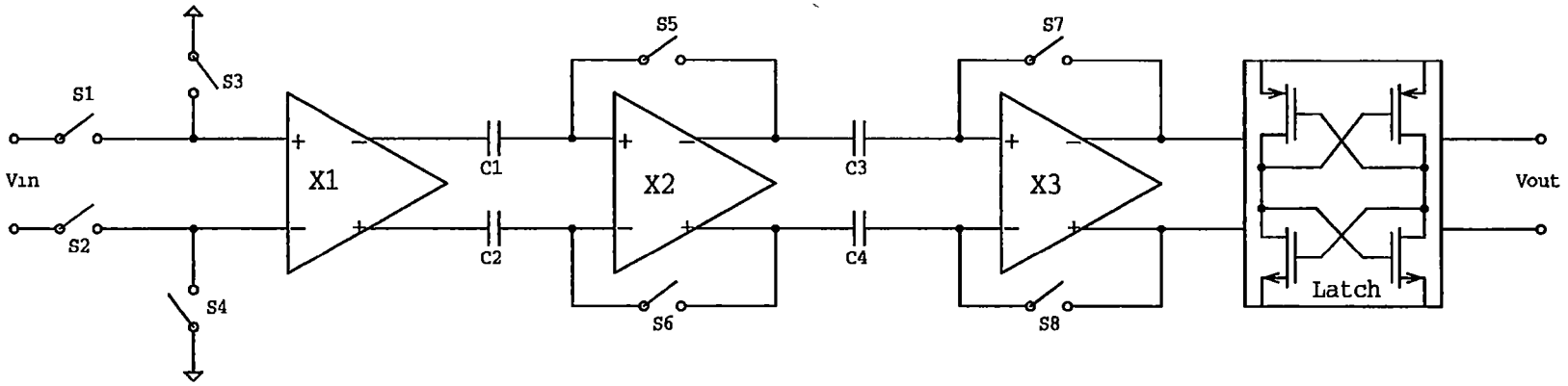


Figure 3-11. Multi-stage offset storage calibration technique applied to a fully differential comparator.

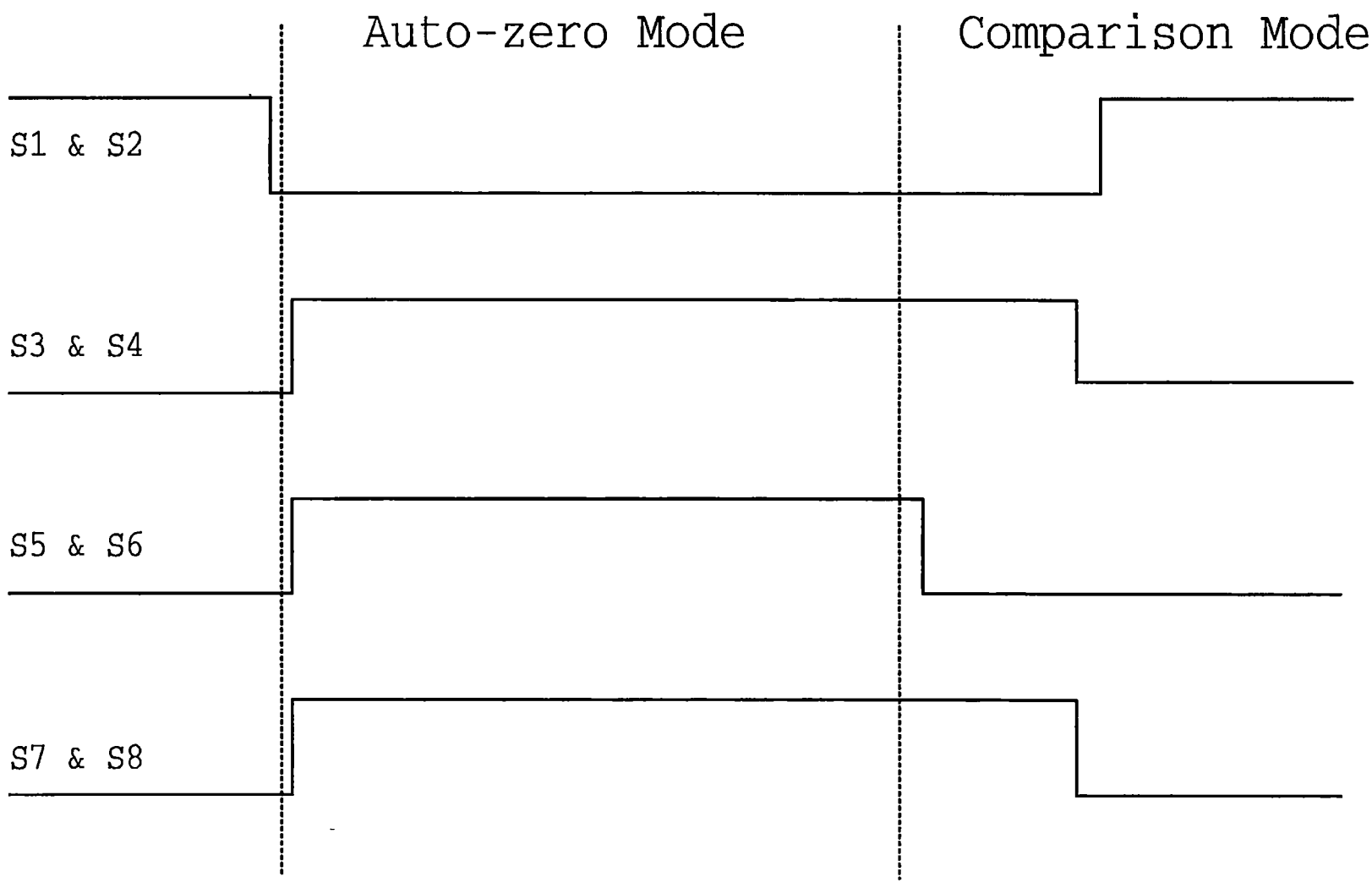


Figure 3-12. Timing diagram for a three-stage MSOS comparator architecture.

the offset voltage of the latch. Equation 3-30 predicts that the MSOS architecture can achieve a very low corrected comparator offset voltage. However, the main disadvantage of the MSOS topology when compared to the IOS and OOS implementations is the additional circuitry, area, power dissipation, and complexity required to implement the design.

3.1.5 Comparator Architecture Selection and Channel Implementation

3.1.5.1 Comparator Offset Correction Topology

After reviewing the tradeoffs and limitations of these common offset correction architectures, it is evident that in most of these topologies, the resolution performance of the CMOS comparator is limited by the large offset of the latch. For this application, there is substantial risk and uncertainty whether the corrected offset voltage of the comparator can be maintained less than 2.33 mV in a IOS or OOS offset correction architectures due to the potentially large offset of the latch. Also, a MSOS architecture implementation with three stages or more is undesirable in parallel flash ADC applications because of the large area, power dissipation, and complexity required to realize the design. However, a two stage MSOS architecture may be practical and appropriate in some high-resolution ADC applications.

Instead of utilizing multiple preamplifier stages, each with offset correction to accommodate a large latch offset, offset correction techniques were applied to the latch circuitry to relax the gain and performance requirements of the preamplifier. In essence, this selected topology is an OOS offset correction architecture with offset cancellation

techniques applied to the latch circuitry.

Unfortunately, most traditional CMOS latch circuits do not easily facilitate the use of offset correction techniques due to their non-linear behavior. In most ADCs, clocked comparators employing regeneration are commonly used to sample the input in one phase of the clock cycle and make a decision in the next part of the clock cycle. Consequently, offset correction techniques are very difficult to integrate in most of these popular two state comparators. After reviewing extensive literature of different circuit topologies for the preamplifier and latch, a slightly modified two-stage MSOS comparator architecture was chosen. This circuit configuration which is shown in Figure 3-13 is a variation of the MSOS architecture where the second stage preamplifier and latch are combined in the same circuitry. Essentially, the second stage is a latched comparator with IOS offset cancellation calibration. The fully differential comparator offset correction topology shown in Figure 3-13 is unique and not believed to have been previously reported in the literature

Preamplifier *X1* utilizes OOS offset cancellation while the second stage which consists of a combined preamplifier and latch employ the IOS calibration technique When in auto-zero mode, switches *S1* and *S2* are open and switches *S3-S6* are closed. The offset voltage of preamplifier *X1* is stored on the output capacitors *C1* and *C2* Simultaneously, the combined offset of the preamplifier and latch are also stored on capacitors *C1* and *C2*. In comparison mode, switches *S3-S6* are opened and *S1* and *S2* are closed to sample the input signal and initiate the comparison process

With this selected offset cancellation architecture, the residual input-referred

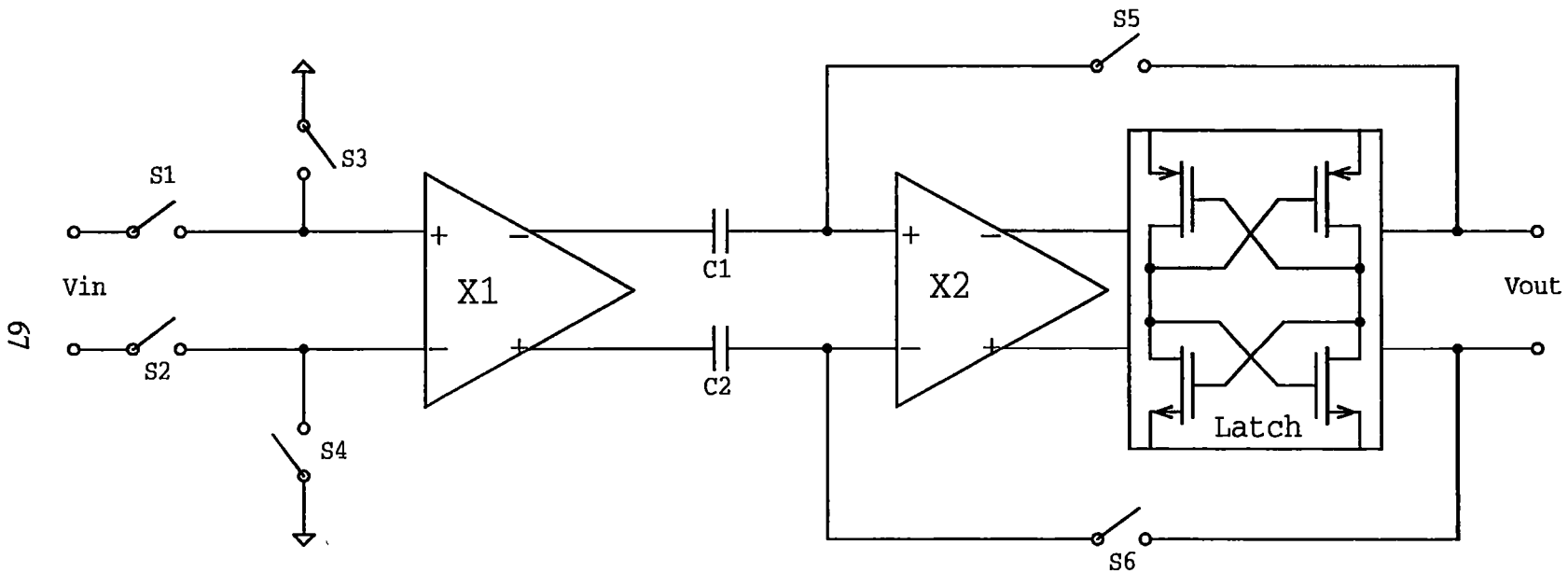


Figure 3-13. Fully differential comparator offset correction topology implemented in the 6-bit ADC.

comparator offset voltage after calibration is given by

$$V_{OS} = \frac{\Delta Q}{A_1 C} + \frac{V_{OS2}}{A_1(1+A_2)}, \tag{3-31}$$

where A_1 and A_2 are the gains of the preamplifiers *X1* and *X2*, respectively, ΔQ is the mismatch in charge injection onto capacitors *C1* and *C2* when switches *S5* and *S6* are opened, C is the value of the offset storage capacitors, and V_{OS2} is the combined total offset of the preamplifier *X2* and the latch.

The mismatch in charge injection onto the offset storage capacitors is represented by the first term in Equation 3-31. The first term of Equation 3-31 could also represent any additional errors such as an imbalance in capacitive division or charge injection due to the mismatch in capacitors *C1* and *C2*. Note that the sensitivity to mismatches in charge injection and capacitive division is greatly reduced since there effects are decreased by the gain of the preamplifier *X1* when referred to the input. The second term in Equation 3-31 is a result of the limited offset correction available due to the finite gain of the second stage *X2*, simply referred to the input of preamplifier *X1*.

This offset correction topology achieves superior residual input-referred offset performance when compared to the IOS and OOS offset cancellation architectures with the same amount of circuitry, power dissipation, and complexity. These advantages make this comparator architecture suitable for integration in high-performance parallel flash ADCs.

3.1.5.2 Preamplifier Design and Analysis

A schematic of the preamplifier used in this CMOS comparator offset correction

architecture is shown in Figure 3-14. The preamplifier design employs diode-connected transistors to keep all nodes at relatively low impedance levels while providing a limited but reasonable amount of gain with very high bandwidth. Note that this circuit can easily achieve zero systematic offset error performance if complete symmetry is preserved in the design of the circuit. Also, this circuit topology utilizes limited positive feedback from the cross gate connection of transistors *M9* and *M11* to increase the gain of the preamplifier. The positive feedback loop gain provided by *M9* and *M11* is designed to be less than unity, and therefore the circuit is stable. The applied positive feedback increases the impedance levels at the differential outputs and thus increases the gain of the preamplifier. The selection of the transistor sizes for *M8* and *M10* relative to the transistors sizes of *M9* and *M11* is central in this design since this provides a gain stage and determines the amount of positive feedback present in the circuit.

The differential gain of the preamplifier can be derived by using small signal analysis assuming the sizes of all transistors are selected to achieve complete circuit symmetry which establishes zero systematic offset performance. Therefore, this symmetry condition of the circuit requires the relative sizes of the transistors to be: $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$, $\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5$, $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7$, $\left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_{10}$, and $\left(\frac{W}{L}\right)_9 = \left(\frac{W}{L}\right)_{11}$.

The overall differential gain of the preamplifier can be written as

$$\frac{V_5 - V_6}{V_4 - V_3} = \left(\frac{V_9 - V_{10}}{V_4 - V_3}\right)\left(\frac{V_5 - V_6}{V_9 - V_{10}}\right) \tag{3-32}$$

The complete gain analysis of the preamplifier can be divided into calculating the two gain stages in Equation 3-32.

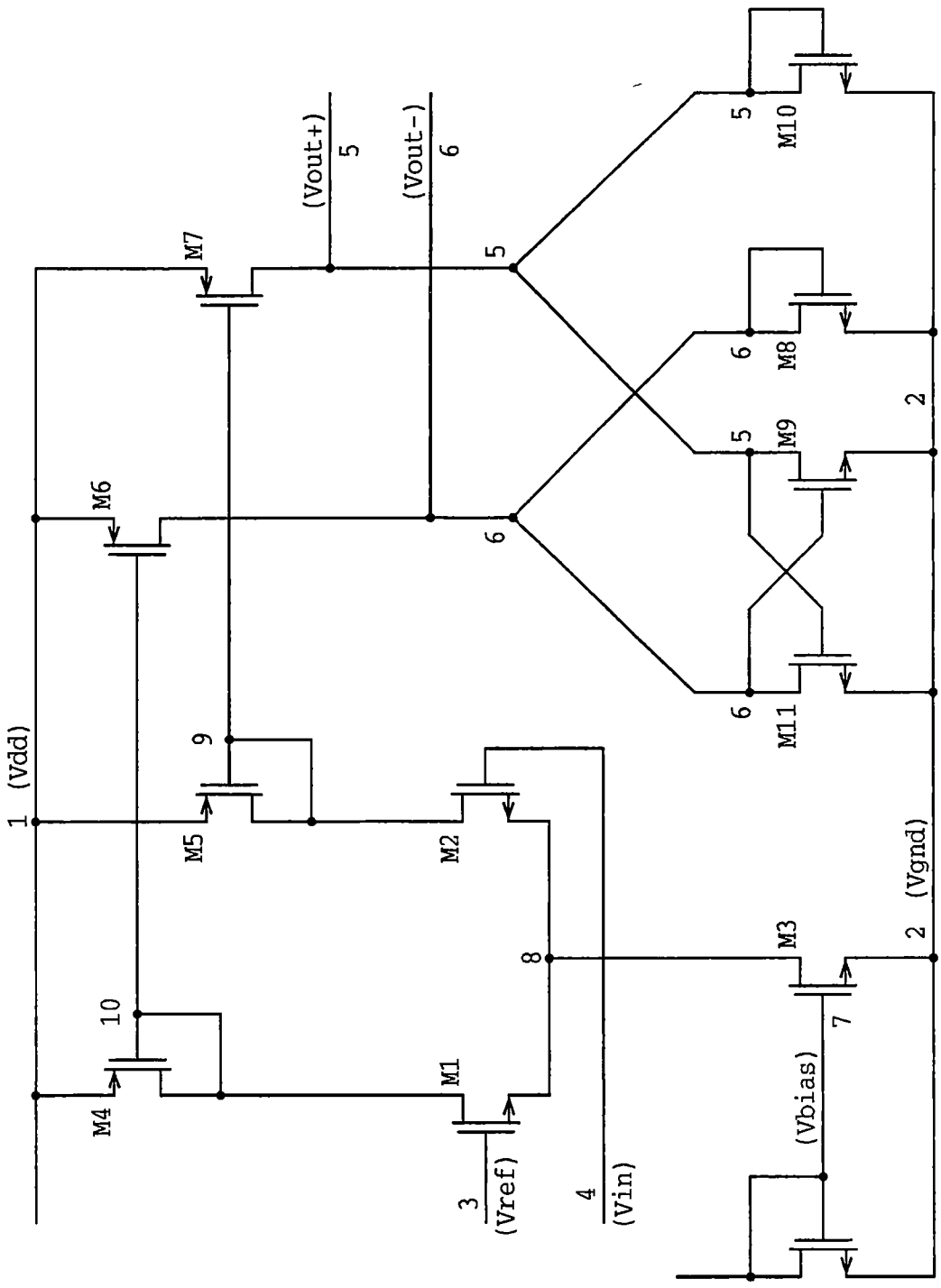


Figure 3-14. Schematic diagram of the preamplifier used in the offset corrected comparator architecture.

The first term in Equation 3-32 is the differential gain from the input transistors *M1* and *M2* to the gates of diode connected transistors *M4* and *M5*. By neglecting the body effect of the differential input transistor pair, the gain calculation of the first stage is simplified and can be approximated as

$$\frac{V_9 - V_{10}}{V_4 - V_3} \approx \frac{-gm_1}{gm_4}, \tag{3-33}$$

where gm_1 and gm_4 are the transconductance of transistors *M1* and *M4*, respectively.

The second term in Equation 3-32 represents the differential gain from the gates of transistors *M6* and *M7* to the gates of the output transistors *M8* and *M10*. The calculation of this gain is complicated by the differential positive feedback provided by transistors *M9* and *M11*. This gain can be derived with the help of Figure 3-15 which shows the small signal equivalent circuit of the output gain stage that is composed of transistors *M6* through *M11*. Applying nodal analysis to the output nodes and writing current summation equations results in two equations

$$V_6 gm_8 = -\left[gm_6 V_{10} + gm_{11} V_5\right], \tag{3-34}$$

and

$$V_5 gm_{10} = -\left[gm_7 V_9 + gm_9 V_6\right]. \tag{3-35}$$

Rearranging Equations 3-34 and 3-35 in matrix solution, applying Cramer's rule, and solving for the output nodes V_5 and V_6 in terms of V_{10} and V_9 yields

$$V_6 = \frac{-V_{10}\left[\frac{gm_6}{gm_8}\right] + V_9\left[\frac{gm_7 gm_{11}}{gm_{10} gm_8}\right]}{1 - \left[\frac{gm_9 gm_{11}}{gm_{10} gm_8}\right]}, \tag{3-36}$$

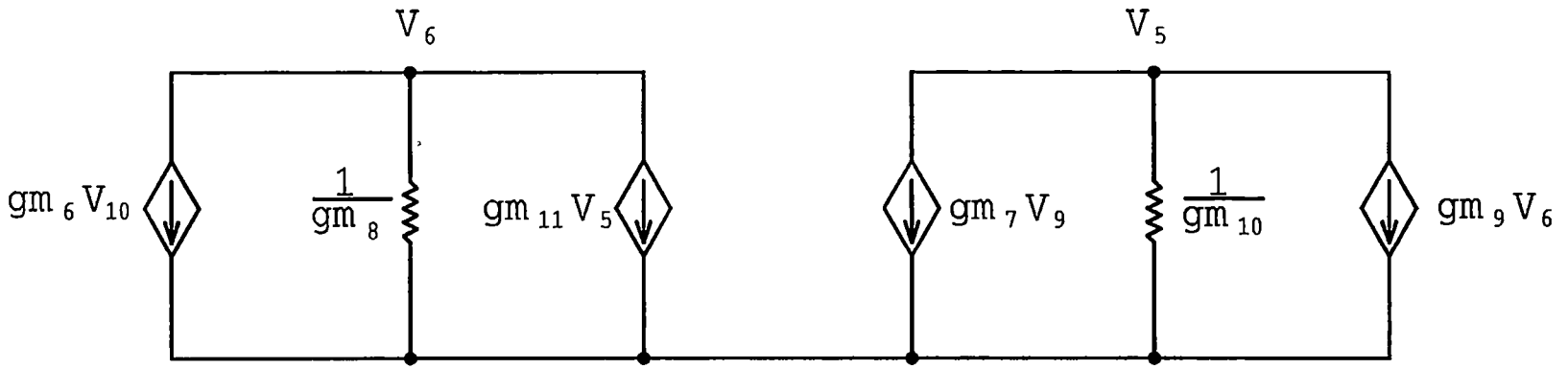


Figure 3-15. Small signal equivalent circuit of the output gain stage in the preamplifier.

and

$$V_5 = \frac{-V_9\left[\frac{gm_7}{gm_{10}}\right] + V_{10}\left[\frac{gm_9 gm_6}{gm_{10} gm_8}\right]}{1-\left[\frac{gm_9 gm_{11}}{gm_{10} gm_8}\right]}. \qquad (3\text{-}37)$$

Taking Equations 3-36 and 3-37 and solving for the differential output expression yields

$$(V_5 - V_6) = \frac{V_{10}\left[\left(\frac{gm_6}{gm_8}\right) + \left(\frac{gm_9 gm_6}{gm_{10} gm_8}\right)\right] - V_9\left[\left(\frac{gm_7}{gm_{10}}\right) + \left(\frac{gm_7 gm_{11}}{gm_{10} gm_8}\right)\right]}{1-\left[\frac{gm_9 gm_{11}}{gm_{10} gm_8}\right]}. \qquad (3\text{-}38)$$

If complete symmetry is preserved in the circuit design, then $gm_8=gm_{10}$, $gm_9=gm_{11}$, and $gm_6=gm_7$. Thus, Equation 3-38 can be re-written as

$$(V_5 - V_6) = \frac{(V_{10} - V_9)\left[\left(\frac{gm_6}{gm_8}\right)\left(1+\frac{gm_9}{gm_8}\right)\right]}{1-\left[\frac{gm_9^{\,2}}{gm_8^{\,2}}\right]}, \qquad (3\text{-}39)$$

and then factored and simplified to

$$(V_5 - V_6) = \frac{-1(V_9 - V_{10})\left(\frac{gm_6}{gm_8}\right)}{1-\left(\frac{gm_9}{gm_8}\right)}. \qquad (3\text{-}40)$$

Finally, solving for the differential gain gives the result

$$\frac{(V_5 - V_6)}{(V_9 - V_{10})} = \frac{-gm_6}{gm_8 - gm_9}. \qquad (3\text{-}41)$$

After substituting Equations 3-33 and 3-41 into Equation 3-32, the overall differential

gain of the preamplifier can be expressed as

$$\frac{(V_5 - V_6)}{(V_4 - V_3)} = \left(\frac{gm1}{gm4}\right)\left(\frac{gm_6}{gm_8 - gm_9}\right). \tag{3-42}$$

This is a very interesting result in that the small signal differential gain of the preamplifier is very much dependent upon the subtraction of two NMOS transistor transconductances. Further investigation of Equation 3-42 can be performed. Suppose that all transistors in the preamplifier are operating in strong inversion. The transconductance of a MOS transistor operating in strong inversion is given by [25] and is

$$gm = \sqrt{2I_D \mu_o C_{OX}\left(\frac{W}{L}\right)}. \tag{3-43}$$

Substituting this expression for the transconductance of a transistor into Equation 3-42, results in

$$\frac{(V_5 - V_6)}{(V_4 - V_3)} = \left(\frac{\sqrt{2I_{D1}\mu_n C_{OX}\left(\frac{W}{L}\right)_1}}{\sqrt{2I_{D4}\mu_p C_{OX}\left(\frac{W}{L}\right)_4}}\right)\left(\frac{\sqrt{2I_{D6}\mu_p C_{OX}\left(\frac{W}{L}\right)_6}}{\sqrt{2I_{D8}\mu_n C_{OX}\left(\frac{W}{L}\right)_8} - \sqrt{2I_{D9}\mu_n C_{OX}\left(\frac{W}{L}\right)_9}}\right). \tag{3-44}$$

Note that transistors *M4* and *M6* of Figure 3-14 comprise a simple transistor current mirror circuit configuration and therefore the drain currents of the transistors are related by the relationship

$$I_{D6} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} I_{D4}. \tag{3-45}$$

Also, from Figure 3-14, the drain current of transistor *M6* splits between transistors *M8* and *M11*. Therefore, the sum of the drain currents in transistors *M8* and *M11* equals the total drain current in *M6*, or simply

$$I_{D6} = I_{D8} + I_{D11} \,. \tag{3-46}$$

The current split of I_{D6} is based upon the relative transistor sizes of *M8* and *M11*, which can be calculated as

$$I_{D8} = \frac{\left(\frac{W}{L}\right)_8 I_{D6}}{\left(\frac{W}{L}\right)_{11} + \left(\frac{W}{L}\right)_8} \,, \tag{3-47}$$

and

$$I_{D11} = \frac{\left(\frac{W}{L}\right)_{11} I_{D6}}{\left(\frac{W}{L}\right)_{11} + \left(\frac{W}{L}\right)_8} \,. \tag{3-48}$$

Substituting Equations 3-46, 3-47, and 3-48 into Equation 3-44 and factoring out common terms in the numerator and denominator results in the expression

$$\frac{(V_5 - V_6)}{(V_4 - V_3)} = \left(\frac{\sqrt{\left(\frac{W}{L}\right)_1}}{\sqrt{\left(\frac{W}{L}\right)_4}} \right) \left(\frac{\sqrt{\left(\frac{W}{L}\right)_6}}{\sqrt{\frac{\left[\left(\frac{W}{L}\right)_8\right]^2}{\left(\frac{W}{L}\right)_8 + \left(\frac{W}{L}\right)_{11}}} - \sqrt{\frac{\left[\left(\frac{W}{L}\right)_{11}\right]^2}{\left(\frac{W}{L}\right)_8 + \left(\frac{W}{L}\right)_{11}}}} \right) . \tag{3-49}$$

Thus, for strong inversion operation, the differential gain of the preamplifier is

independent of the bias current in the devices and depends only upon the relative size ratios of the transistors. This feature is advantageous since variations in the bias currents of the circuit due to transistor mismatch or other process variations will have little effect on the gain performance of the circuit. Another important issue in the design of the preamplifier is that the transconductances of transistors *M8* and *M10* relative to the transconductances of transistors *M9* and *M11* must be separated by enough margin so that small mismatches between these transistors do not result in large gain variations. Therefore, good matching between these devices is desired for tight open loop gain control. This requirement is addressed by selection of transistor device sizes and layout techniques to improve matching of these transistors.

The frequency response of the preamplifier consists of two poles in the signal path and can be expressed as

$$A_v(f) = \frac{Amid}{\left(1 + j \cdot \frac{f}{f_1}\right)\left(1 + j\ \frac{f}{f_2}\right)}, \tag{3-50}$$

where *Amid* is the low frequency gain of the preamplifier given by Equation 3-42. The terms f_1 and f_2 in Equation 3-50 are the representative frequencies of the two poles (nodes *5* and *9*) that are present in the signal path of the circuit. The term f_1 can be found by the expression

$$f_1 = \frac{1}{2\pi\left(\frac{1}{gm_4}\right)C_9}, \tag{3-51}$$

where gm_4 is transconductance of transistor *M4* and *C9* is the total capacitance on node *9* of the circuit. Similarly, the term f_2 is given by

$$f_2 = \frac{1}{2\pi\left(\frac{1}{gm_8 - gm_9}\right)C_5}, \tag{3-52}$$

where gm_8 and gm_9 are the transconductance of transistors *M8* and *M9*, respectively, and *C5* is the total capacitance on the output node of the circuit. From the equations presented above, an intuitive feel and fundamental understanding can be developed to determine what design parameters influence the gain and bandwidth performance of the circuit. Neglecting the preamplifier's load capacitance, the transistor device sizes and the parasitic capacitances present in the integrated circuit layout will dictate the total capacitance on nodes *9* and *5* and thus ultimately determine the overall bandwidth of the circuit. As previously mentioned and given in Equation 3-49, the relative transistor device sizes will also determine the gain of the preamplifier because the gain, to first order, is independent of bias currents in the transistors for strong inversion operation. To achieve optimal performance, small geometry devices with small capacitances and good tight layout interconnect techniques should be implemented in the design and layout of the preamplifier.

The dc coupling at the input of the preamplifier in this offset correction architecture limits the CMIR of the comparator. For this ADC application, a CMIR of 2-volts is desired. Thus, it is necessary to find the maximum positive and negative common-mode input ranges of the preamplifier. The maximum positive CMIR is given by

$$Vin_{\max} = Vdd - Vgs_{M4} - Vds_{M1} + Vgs_{M1}, \tag{3-53}$$

and can be simplified to

$$Vin_{\max} = Vdd - \sqrt{\frac{2I_{D4}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_4}} - Vt_{M4} + Vt_{M1} \,. \tag{3-54}$$

From Equation 3-53, it can be seen that the body effect on the differential input pair, which increases the threshold voltages of *M1* and *M2*, actually helps improve the positive CMIR. The maximum negative CMIR of the preamplifier is given by

$$Vin_{\min} = Vgs_{M1} - \Delta V_{M3} \,, \tag{3-55}$$

and can be simplified to

$$Vin_{\min} = Vt_{M1} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + \sqrt{\frac{2I_{D3}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} \,. \tag{3-56}$$

Equation 3-56 shows that the body effect on the differential input pair actually degrades the negative CMIR of the preamplifier.

Equations 3-54 and 3-56 indicate that for given transistor device sizes an increase in bias current of the differential input stage results in the reduction of the preamplifier's CMIR. Also, note that the overall value of the CMIR for the preamplifier is independent of the transistor threshold voltage of the differential input pair.

3.1.5.3 Regenerative Latch Design and Analysis

The regenerative latch selected and designed for this application is shown in Figure 3-16. The latch design is a derivative of the design reported by Song [23]. The circuit is an amplifier and latch integrated into the same functional block. The diode connected loads of the input stage with current mirrors provide a limited amount of gain

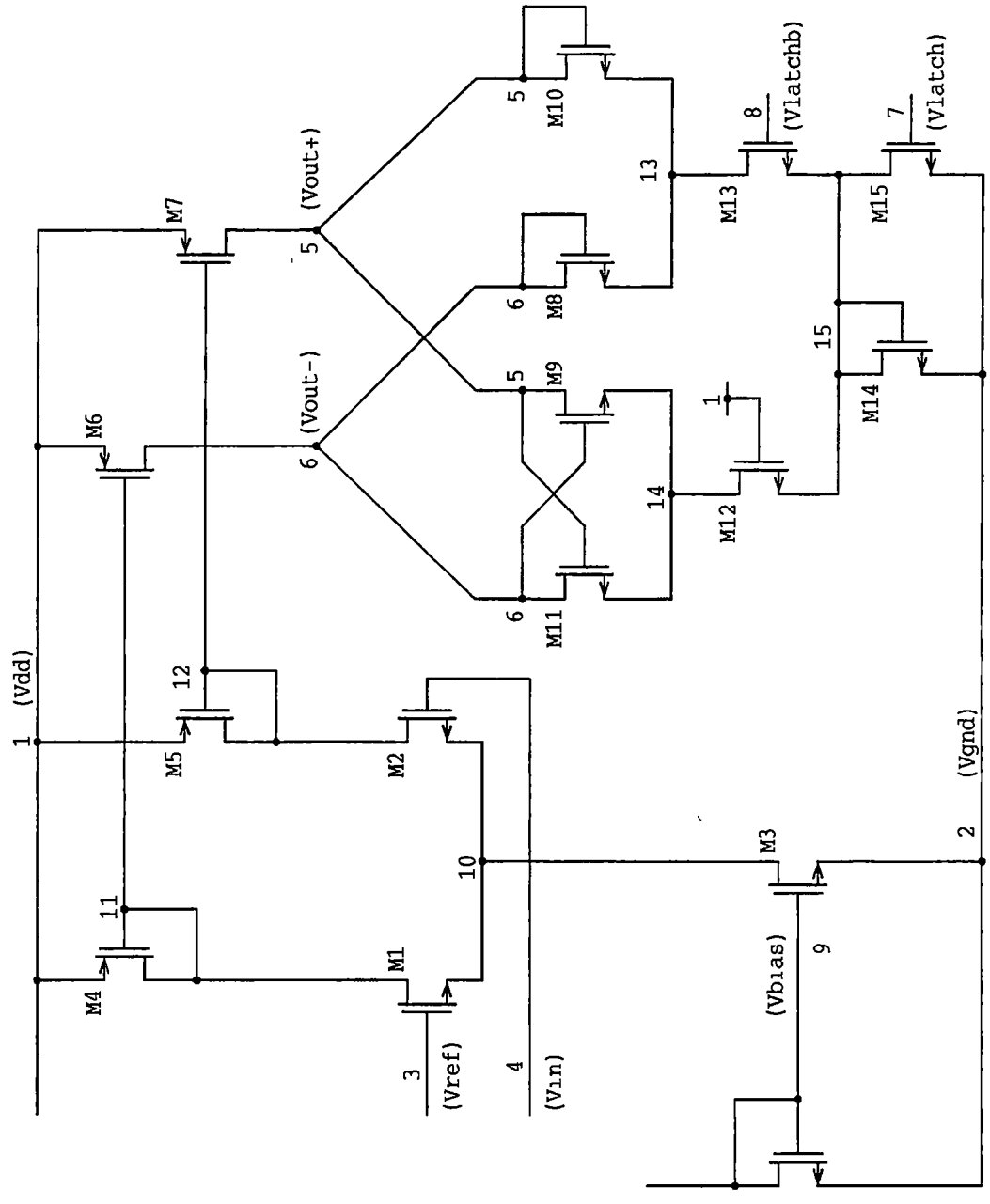


Figure 3-16. Schematic diagram of the regenerative latch used in the offset corrected comparator channel.

while isolating the kickback effects of the latch from the input stage. Kickback denotes any charge transfer or disturbance on the input nodes when the circuit transitions to latch mode. If the V_{latch} control signal is a logical 0 or low (V_{latchb} is a logical 1 or high), the circuit is in compare mode and performs as an amplifier. The operation of the circuit in this condition is essentially identical to the preamplifier previously discussed in the last section. Once the V_{latch} control signal goes high or is a logical 1 (V_{latchb} is a logic 0 or low), the diode connected transistors *M8* and *M10* are effectively disconnected from the circuit, and the amplifier becomes a positive feedback regenerative latch because of the cross coupled gate connection of transistors *M9* and *M11*. The amplified differential voltage at the output just before the V_{latch} signal goes high determines the decision of the latch. Since in latch mode transistor *M15* effectively shorts node *15* to ground, full CMOS logic levels are obtained from the output of the circuit.

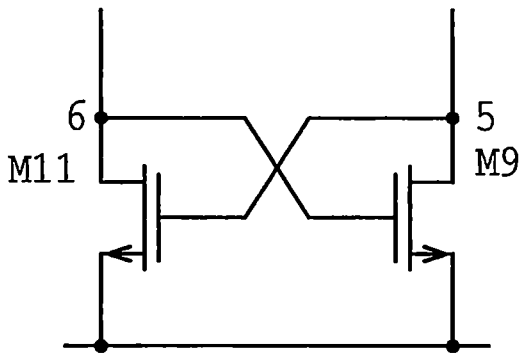
For the selected comparator offset correction architecture, the regenerative latch circuit will employ the IOS calibration technique. Therefore, the latch circuit must be unity gain stable and the common-mode output voltage levels must be well controlled The common-mode output levels must be controlled because they must lie within the CMIR of the differential input stage of the latch circuit when placed into a unity gain configuration. Common-mode voltage levels in differential circuits are usually achieved with CMFB. A key element in this design was the elimination of the requirement for CMFB. CMFB is usually required with fully differential circuits and has several drawbacks, which usually include a reduction in speed, and an increase in power consumption and complexity. Transistor *M14* is added in series with the output stage to

level shift the common-mode output voltage level to accommodate the CMIR requirements of the latch circuit when placed in a unity gain configuration during IOS auto-zero mode. Transistor *M12* is only used to match the on resistance of *M13* when in compare mode. Since the output is diode clamped and level shifted to accommodate the CMIR requirements of the input stage, the latch circuit will achieve stable dc bias levels when placed in a unity gain feedback configuration and thus no CMFB is required.

Since the operation of the latch circuit in compare mode is essentially identical to the preamplifier with the output level shifted, the analysis of the circuit is this condition will not be repeated. Instead, emphasis will be placed on the analysis of the circuit when in a regenerative latch configuration. The decision time required for the regenerative latch to discriminate very small input signal differences is a fundamental issue in the design of the circuit since it will impact the overall performance of the comparator

The decision time of the latch to achieve CMOS logic levels is related to the latch time constant when placed in a positive feedback state. The latch time constant is found by analyzing the regenerative part of the circuit consisting of two transistors that form the positive feedback loop. A simplified schematic of the regenerative portion of the latch circuit is shown in Figure 3-17. The output voltages (nodes *5* and *6*) are assumed close together at the beginning of the latch mode so that both transistors are in the linear amplification range of operation and are driving some impedance as a load. In addition, the on resistance of transistor *M12* and the common-mode voltage level shift provided by *M14* are neglected in this latch mode analysis.

Writing current summation equations for the two output nodes of Figure 3-17



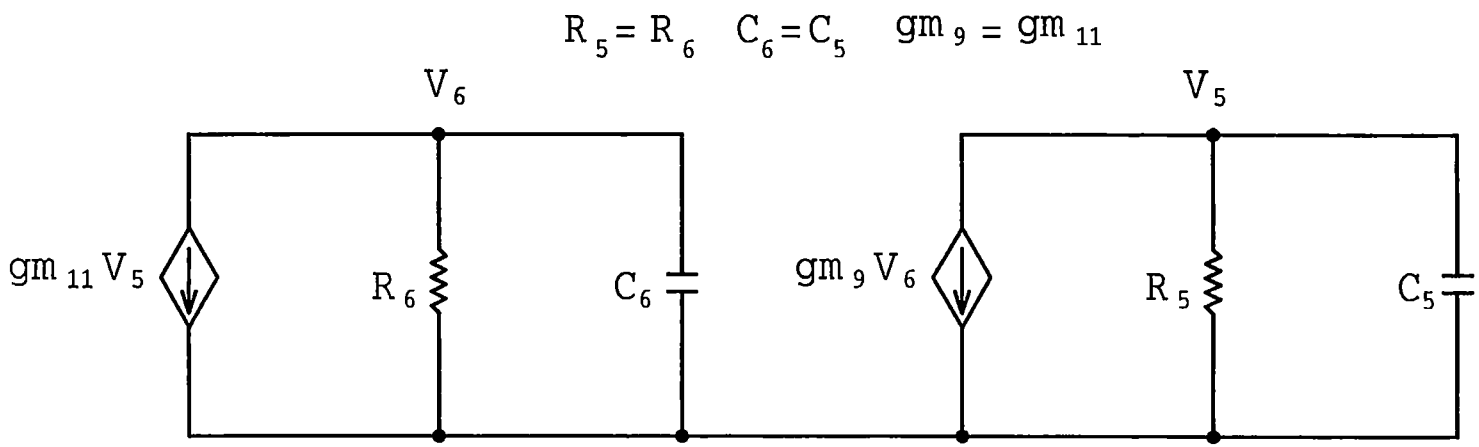


Figure 3-17. Small signal equivalent circuit of the regenerative output stage in the latch circuit.

yields

$$gmV_5 + \frac{V_6}{R_L} + C_L \frac{dV_6}{dt} = 0 \ , \tag{3-57}$$

and

$$gmV_6 + \frac{V_5}{R_L} + C_L \frac{dV_5}{dt} = 0 \ , \tag{3-58}$$

where gm is the transconductance of transistors *M5* and *M6*, and R_L and C_L are the loads of each device. Assuming that $gm=gm_5=gm_6$, and that both transistors have identical loads. These two equations can be simplified to

$$R_L C_L \frac{dV_6}{dt} + V_6 = -gmR_L V_5 \ , \tag{3-59}$$

and

$$R_L C_L \frac{dV_5}{dt} + V_5 = -gmR_L V_6 \ . \tag{3-60}$$

Subtracting Equations 3-59 and 3-60 from each other results in

$$R_L C_L \left(\frac{dV_5}{dt} - \frac{dV_6}{dt} \right) + (V_5 - V_6) = gmR_L (V_5 - V_6) \ . \tag{3-61}$$

By defining $\Delta V = V_5 - V_6$, Equation 3-61 can be reduced to

$$R_L C_L \left(\frac{d\Delta V}{dt} \right) + \Delta V = gmR_L \Delta V \ , \tag{3-62}$$

and rearranging results in the expression

$$\left(\frac{R_L C_L}{gmR_L - 1} \right) \frac{d\Delta V}{dt} = \Delta V \ , \tag{3-63}$$

which is a first order ordinary differential equation. Equation 3-63 can be solved by

several techniques and the solution gives

$$\Delta V = \Delta V_0 e^{\left(\frac{t}{\tau_{latch}}\right)} . \tag{3-64}$$

Thus, the differential output voltage of the latch increases exponentially in time with a latch time constant given by

$$\tau_{latch} = \frac{R_L C_L}{gmR_L - 1} \approx \frac{C_L}{gm} . \tag{3-65}$$

Note that if the gain of each transistor is large when compared to unity, then the latch time constant is approximately equal to the inverse of the unity gain frequency of each transistor.

This circuit configuration and analysis assumes that the load capacitance C_L is directly proportional to the size of the output transistors, which will determine the amount of capacitance on the output nodes. If the gate oxide capacitance of the output transistors is assumed to dominate the total overall load capacitance, then the load capacitance can be approximated by

$$C_L = K_1 \ W \ L \cdot C_{OX} , \tag{3-66}$$

where K_1 is a proportionality constant which is determined by specific bias conditions and parameters of the circuit. Substituting the expression for C_L and the transconductance of a NMOS transistor operating in strong inversion into Equation 3-65 results in

$$\tau_{latch} \approx \frac{K_1 \cdot W \cdot L \ C_{OX}}{\mu_n C_{OX}\left(\frac{W}{L}\right)(Vgs - Vt)} = \frac{K_2 L^2}{(Vgs - Vt)} . \tag{3-67}$$

Equation 3-67 states that the latch time constant depends upon the technology and the transistor sizes and bias conditions. Also, a good latch design is one which minimizes the

C_L load capacitance and maximizes the gate overdrive $(Vgs - Vt)$ of transistors *M9* and *M11*.

Timing considerations often necessitate estimating the minimum differential input voltage of the latch required to obtain successful CMOS logic levels within a given time period. This can be achieved by solving for the time variable in Equation 3-64 and is given by

$$t = \tau_{latch} \cdot \ln\left[\frac{\Delta V \log ic}{\Delta V_o}\right] = \left(\frac{C_L}{gm}\right) \cdot \ln\left[\frac{\Delta V \log ic}{\Delta V_o}\right], \tag{3-68}$$

where τ_{latch} is the time constant of the latch, ΔV_o is the initial differential input voltage of the latch, and $\Delta V_{\log ic}$ is the differential output voltage of the latch required to achieve valid CMOS logic levels. Equation 3-68 can be used to determine the time difference to achieve successful logic levels for two initial differential input voltages applied to the latch and this results in

$$\Delta t = t_2 - t_1 = \left(\frac{C_L}{gm}\right)\left(\ln\left[\frac{\Delta V \log ic}{\Delta V_2}\right] - \ln\left[\frac{\Delta V \log ic}{\Delta V_1}\right]\right), \tag{3-69}$$

and simplifies to

$$\Delta t \approx \tau_{latch} \cdot \ln\left[\frac{\Delta V_2}{\Delta V_1}\right]. \tag{3-70}$$

Equations 3-64 and 3-68 imply that the response of the regenerative latch for various levels of differential input overdrive will be the same shape or waveform, but just delayed in time which can be calculated by using Equation 3-70. Figure 3-18 shows the response of the regenerative latch circuit for various levels of differential input overdrive.

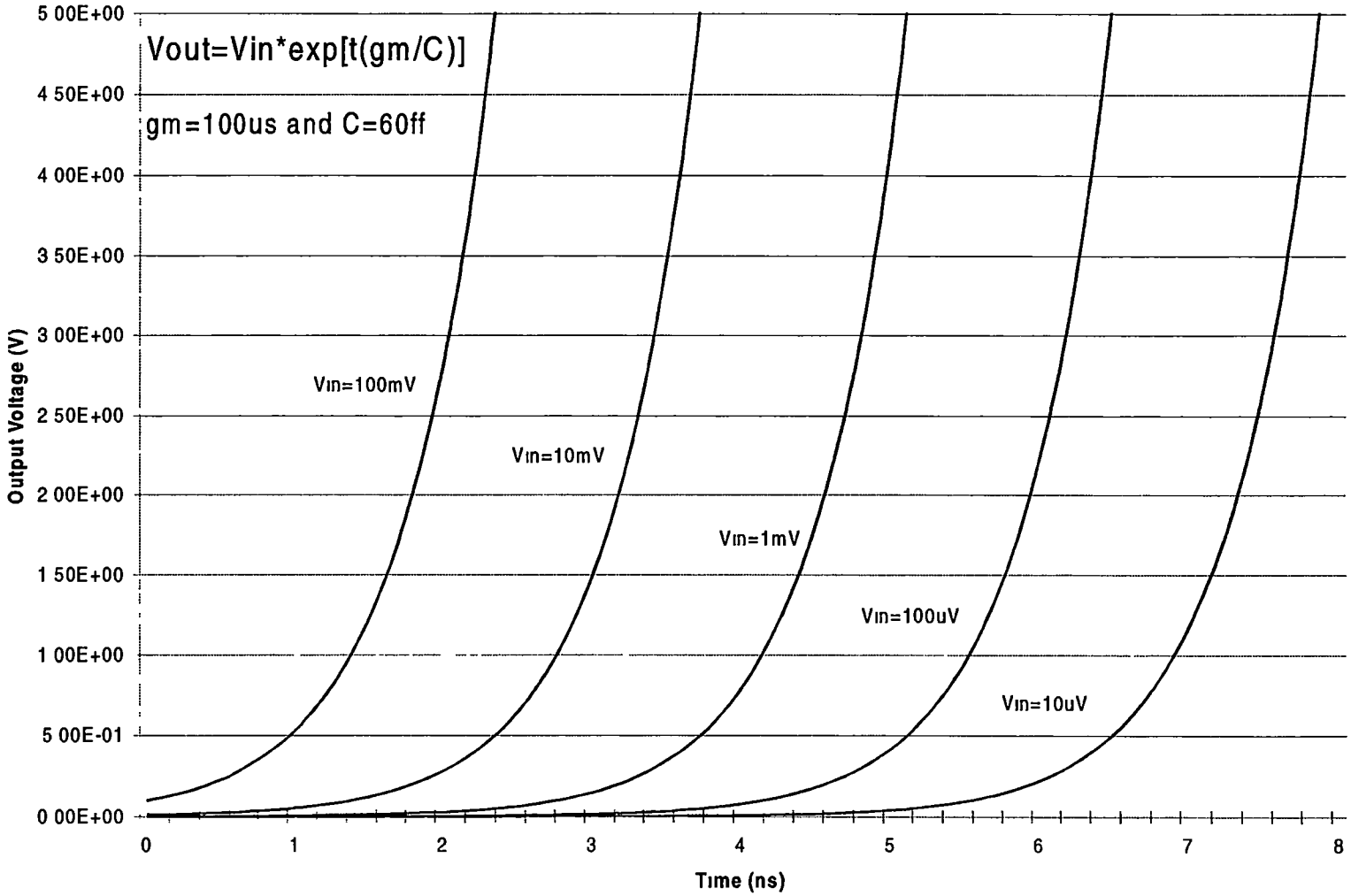


Figure 3-18. Regenerative latch response for different levels of input voltage overdrive.

As can be seen from the figure, the responses of the latch for different input conditions have the same shape or waveform, but they are just delayed in time.

3.1.5.4 MSB and OSB Comparator Channel Integration

Detailed schematics of the MSB and OSB comparator channels are shown in Figures 3-19 and 3-20, respectively. The two comparator channels are essentially identical except for the *X11* analog multiplexer that is present in the OSB comparator design. The analog multiplexer of the OSB channel is basically two CMOS transmission gate structures that are connected in parallel and is used to select the appropriate reference level of the OSB comparator. This reference selection function is integrated in the OSB comparator channel instead of the reference generation network due to replication issues in the integrated circuit layout.

The subcircuit *X1* consists of the differential preamplifier and *X8* represents the regenerative latch circuit All analog switches (*X2-X7*) in the comparator channel are implemented with CMOS transmission gates to minimize charge injection and to accommodate a large dynamic range. The NOR gate represented by *X9* is needed because the output of the latch is an undefined CMOS logic level when placed in auto-zero mode (switches *S1* and *S2* are open and switches *X4-X7* are all closed). Since node *18*, the V_{latchb} signal, is high during this condition, one input of the NOR gate is a logical 1 and thus the output of *X9* is defined as a logical 0 regardless of the other input. This prevents an undefined CMOS logic level to be passed to the D flip-flop of *X10*, possibly causing excessive and unnecessary power dissipation in CMOS logic circuits. Thus, the *X9* NOR

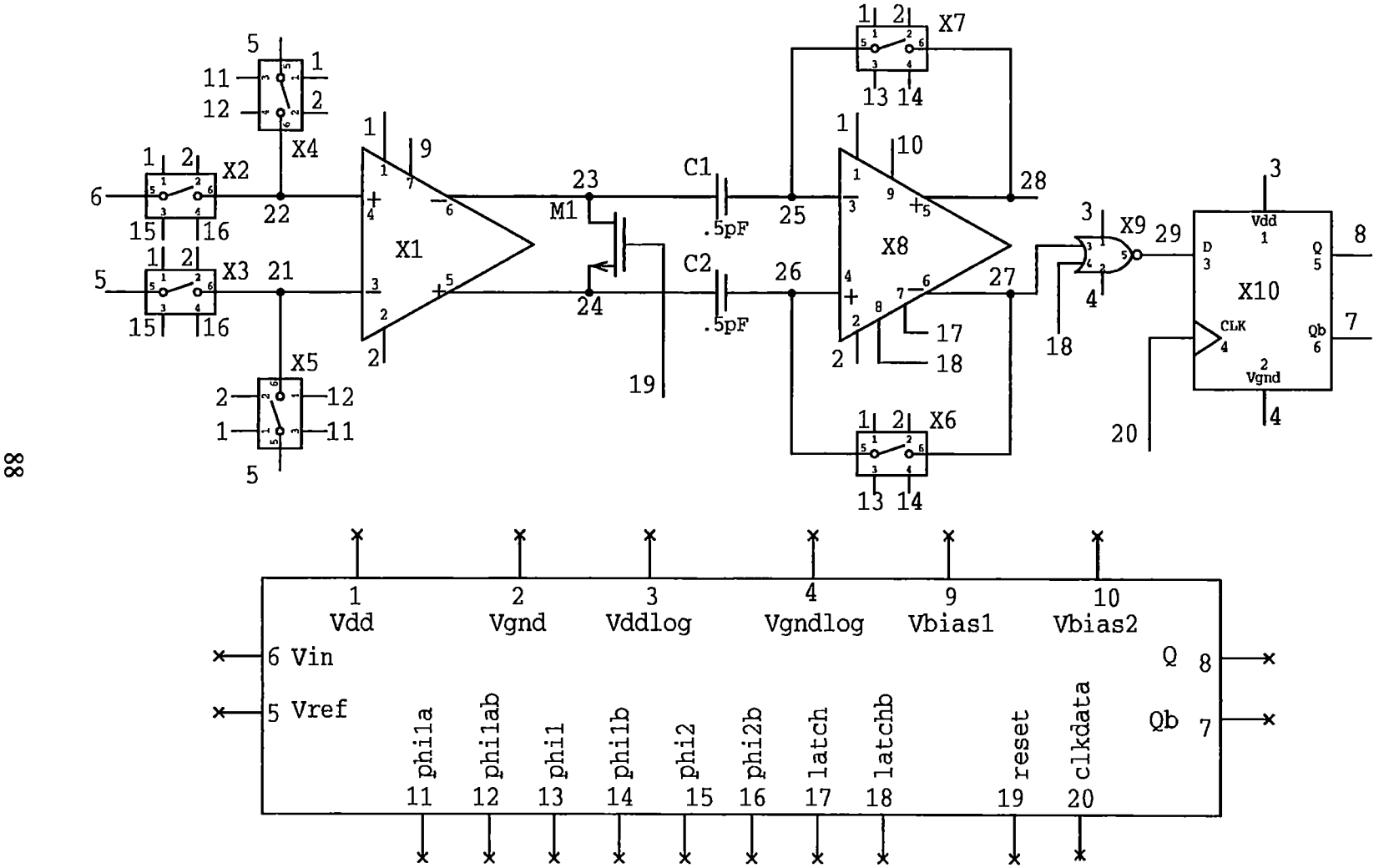


Figure 3-19. Most significant bit (MSB) offset corrected comparator channel.

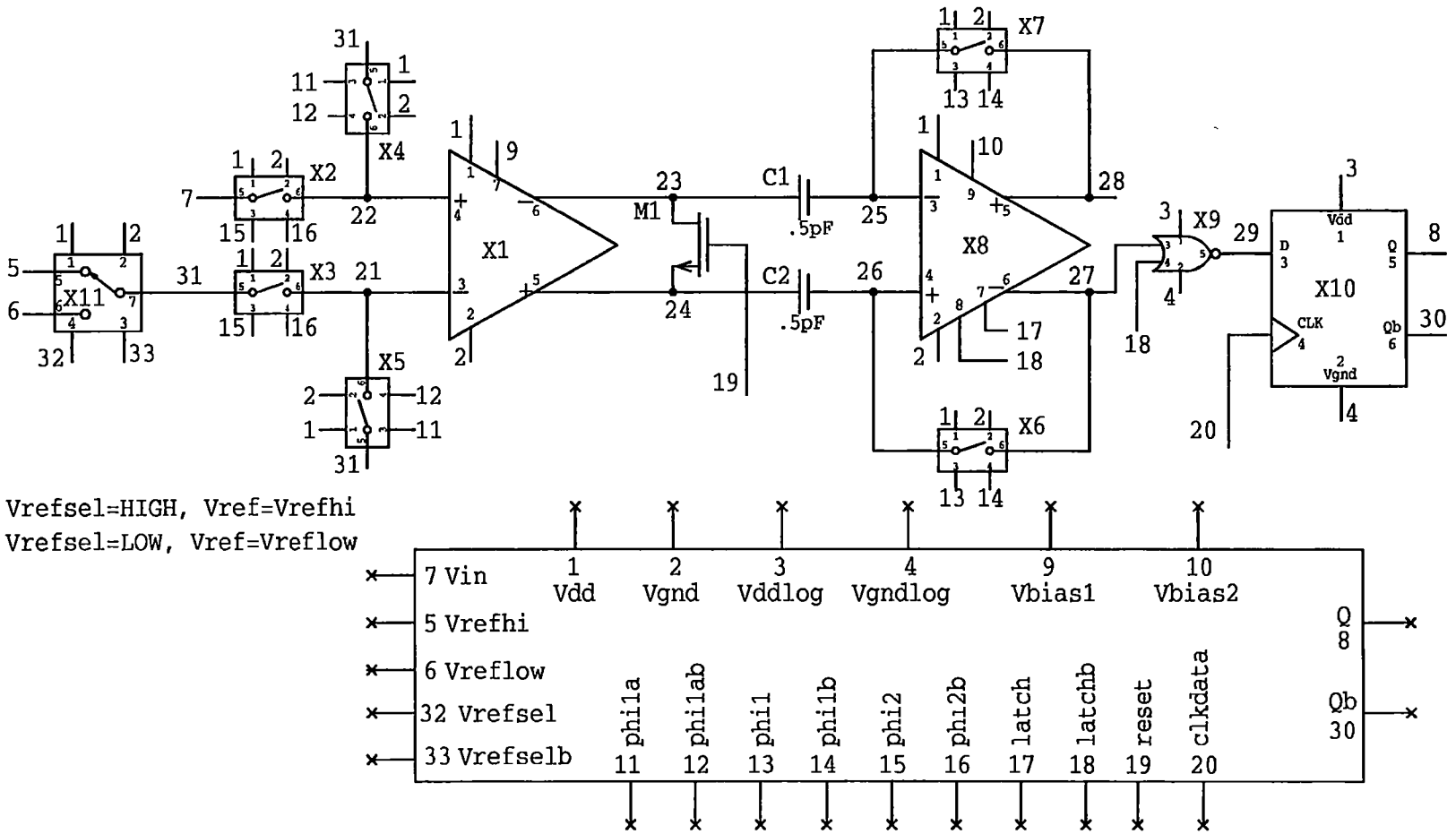


Figure 3-20. Other significant bits (OSB) offset corrected comparator channel.

gate is used to sample the output of the latch circuit and present this signal to the D flip-flop which records the comparator decision that will be accessed by the system at a later time.

The D flip-flop in the comparator channel is not the traditional implementation of an edge-triggered D flip-flop in CMOS technology. Usually a master-slave dynamic topology is invoked which consists of two transmission gates and two inverters to lower the device count and reduce area. A schematic of the edge-triggered D flip-flop is shown in Figure 3-21. The NAND gate implementation of the D flip-flop results in a larger circuit than the standard digital D flip flop, but has several important advantages for this application. The NAND circuit has a symmetrical sampling window in which the setup time is equal to the hold time. Also, this D flip-flop topology has excellent resolution. Its sampling window (setup time + hold time) has been reported to be below 50 ps in 2 μm CMOS technology [34]. Thus, the flip-flop achieves low metastability performance due to its high-resolution characteristics. These features are advantageous for this application because this allows a longer acceptable latch response time and results in reduced comparator metastability performance.

The NMOS transistor *M1* shown in Figures 3-19 and 3-20 is used to provide overdrive recovery when the circuit transitions from compare mode back into auto-zero mode. The overdrive recovery feature was implemented because of the following scenario. When in compare mode, a large differential input signal of the comparator can saturate the output stage of the preamplifier. This condition can be a problem when the circuit transitions back into auto-zero mode. In auto-zero mode, the comparator will

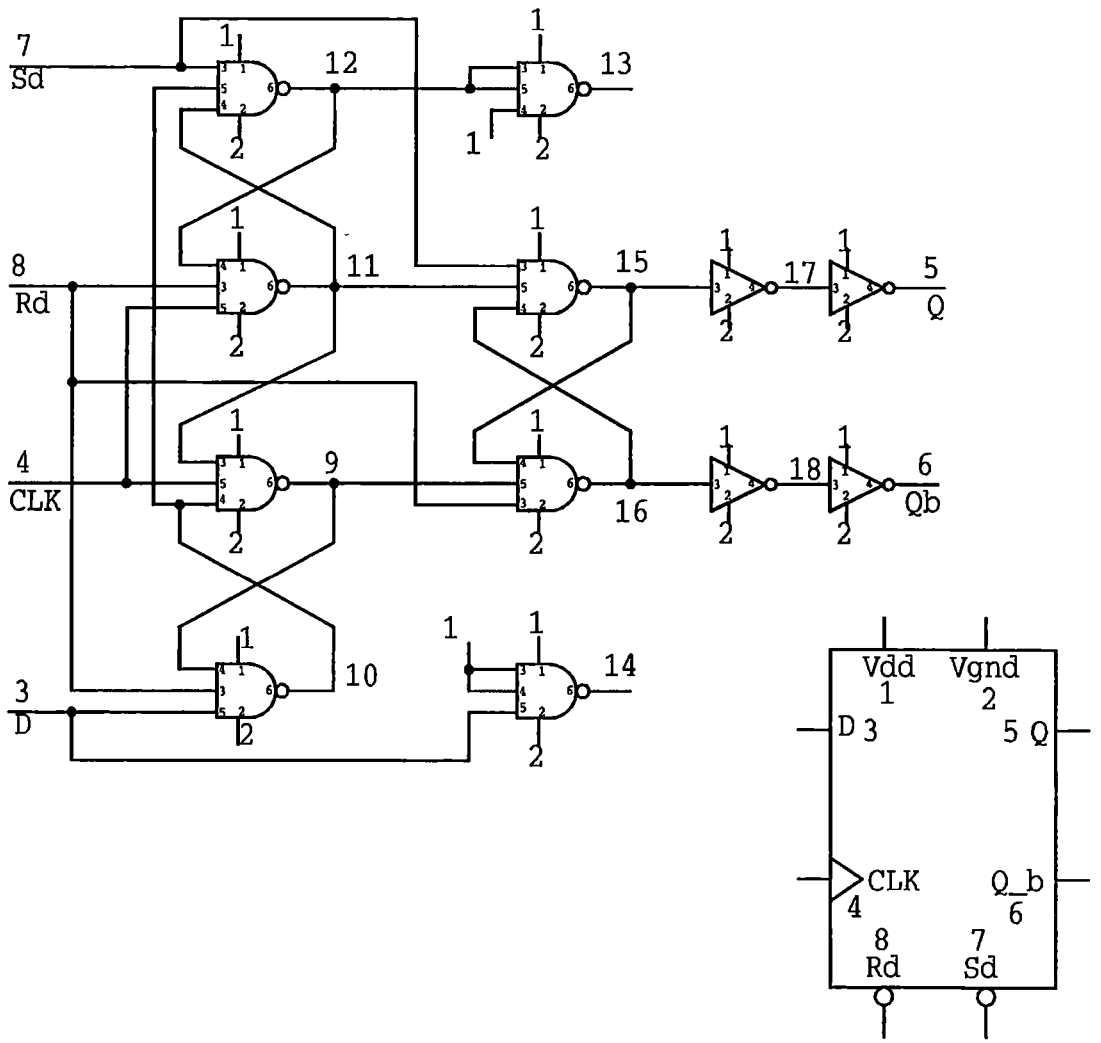


Figure 3-21. Schematic diagram of the high-performance D flip-flop used in the comparator channel.

normally have a small differential input overdrive condition, which will be the input offset voltage of the preamplifier. Because of this small input overdrive condition in auto-zero mode, combined with the preamplifier's output stage being saturated in compare mode, the preamplifier's response can be much slower than normal when the circuit transitions from comparison mode to auto-zero mode. The implementation of transistor *M1* effectively resets the preamplifier and improves the recovery process, which lowers the overall time period required for the comparator offset correction process.

3.2 Reference Generation Circuitry and Analysis

A resistor string was chosen as the reference generation circuit for this ADC application. This simple architecture generally results in good accuracy provided that no output current is required and the resistors can be realized within the required accuracy. The main advantages of the resistor string implementation are low complexity, guaranteed monotonic transfer characteristics, and the excellent differential non-linearity obtained with the reference voltages.

Since the comparators of the ADC rely on the applied reference voltages in the decision making process, the reference generation circuitry plays an important role in determining the overall linearity performance of the ADC. The accuracy of the reference generation circuitry is obviously related to the matching of the resistor string. To determine the required resistor matching for this application, the relationship between resistor mismatches and reference generation errors must be formed. Since the reference generation errors directly affect the linearity performance of the ADC, determining the

INL and DNL of the reference generation network for a given resistor mismatch is very beneficial.

The INL and DNL associated with the reference generation circuitry can be derived based upon resistor matching [24, 35, 36]. Suppose the *i-th* resistor, R_i, has a mismatch error associated with it so that

$$R_i = R + \Delta R_i \ , \tag{3-71}$$

where R is the ideal value of the resistor and ΔR_i is the mismatch error. Now assume that all mismatches are symmetrical about the resistive ladder so that the sum of all the mismatch terms are equal to zero. Therefore, this assumption means the relationship

$$\sum_{i=1}^{2^N} \Delta R_i = 0 \tag{3-72}$$

exists, where 2^N is the total number of resistors in the string required for a N-bit converter. The ideal voltage value at each node of the resistor string can be found by using simple voltage division and can be expressed as

$$V(i)_{ideal} = \frac{(i)V_{ref}}{2^N} \quad \text{for } i=0, 1, 2, 3....., (2^N\text{-}1) \ . \tag{3-73}$$

Including resistor mismatch errors, the actual value of the voltage at each node of the resistor string can be found by summing all of the resistors up to the node and then dividing by the sum of all the resistors in the string. This results in the expression

$$V(i)_{actual} = \frac{V_{ref}\sum_{k=1}^{i} R_k}{\sum_{k=1}^{2^N} R_k} = \frac{V_{ref}\sum_{k=1}^{i} (R + \Delta R_k)}{\sum_{k=1}^{2^N} (R + \Delta R_k)} \ , \tag{3-74}$$

and can be re-written as

$$V(i)_{actual} = \frac{V_{ref}\left[(i)R + \sum_{k=1}^{i} \Delta R_k\right]}{2^N R + \sum_{k=1}^{2^N} \Delta R_k} . \tag{3-75}$$

Since the sum of all mismatch errors along the resistor string are assumed zero (Equation 3-72), the second term in the denominator of Equation 3-75 sums to zero, and thus

$$V(i)_{actual} = \frac{V_{ref}\left[(i)R + \sum_{k=1}^{i} \Delta R_k\right]}{2^N R} = \frac{V_{ref}(i)R}{2^N R} + \frac{V_{ref}}{2^N}\left(\frac{\sum_{k=1}^{i} \Delta R_k}{R}\right) . \tag{3-76}$$

Equation 3-76 can be re-written in the form of

$$V(i)_{actual} = V(i)_{ideal} + \frac{V_{ref}}{2^N}\left(\sum_{k=1}^{i} \frac{\Delta R_k}{R}\right) . \tag{3-77}$$

The form of Equation 3-77 is very useful and can be used to help determine the INL and DNL of the resistor string.

The INL of the resistor string is defined as the difference between the actual and ideal reference voltage taps, or

$$INL(i) = V(i)_{actual} - V(i)_{ideal} . \tag{3-78}$$

Substituting Equation 3-77 into Equation 3-78, yields

$$INL(i) = \left[V(i)_{ideal} + \frac{V_{ref}}{2^N}\left(\sum_{k=1}^{i} \frac{\Delta R_k}{R}\right)\right] - V(i)_{ideal} , \tag{3-79}$$

and simplifies to

$$INL(i) = \frac{V_{ref}}{2^N}\left(\sum_{k=1}^{i} \frac{\Delta R_k}{R}\right) . \tag{3-80}$$

Equation 3-80 is a general expression of the INL for a given *i-th* tap of the resistor string expressed in terms of volts This equation can easily be expressed as a fraction of an LSB. A worst-case condition of INL can be imposed by assuming that the lower half of resistors have a maximum positive mismatch and the upper half of resistors have a maximum negative mismatch, or vice versa [24, 35]. Thus, using this worst-case analysis the maximum INL occurs at the middle tap of the resistor string [$i=2^{(N-1)}$], and results in the expression of

$$|INL|_{\max} = \frac{V_{ref}}{2^N}\left(\sum_{k=1}^{2^{N-1}} \frac{\Delta R_k}{R}\right) = \frac{V_{ref}}{2}\left|\frac{\Delta R_k}{R}\right|_{\max} . \tag{3-81}$$

The DNL of the resistor string can be defined as the actual step value between two adjacent reference voltage taps minus the ideal voltage step value Using Equations 3-73 and 3-77, this is expressed as

$$|V_{i+1} - V_i| = \left[\frac{(i+1)V_{ref}}{2^N} + \frac{V_{ref}}{2^N}\sum_{k=1}^{i+1}\frac{\Delta R_k}{R}\right] - \left[\frac{(i)V_{ref}}{2^N} + \frac{V_{ref}}{2^N}\sum_{k=1}^{i}\frac{\Delta R_k}{R}\right] , \tag{3-82}$$

and can be simplified to

$$|V_{i+1} - V_i| = \left|\frac{V_{ref}}{2^N} + \frac{V_{ref}}{2^N}\left(\frac{\Delta R_i}{R}\right)\right| = \left|\frac{V_{ref}}{2^N}\left(1+\frac{\Delta R_i}{R}\right)\right| . \tag{3-83}$$

The DNL of each voltage tap can be calculated by the expression

$$DNL(i) = \left|\frac{V_{ref}}{2^N}\left(1+\frac{\Delta R_i}{R}\right) - \frac{V_{ref}}{2^N}\right| = \frac{V_{ref}}{2^N}\left|\frac{\Delta R_i}{R}\right|_{\max} . \tag{3-84}$$

Thus, the maximum DNL of the resistor string will occur at the voltage tap for which ΔR is at its maximum value and is given by

$$|DNL|_{max} = \frac{V_{ref}}{2^N}\left|\frac{\Delta R_i}{R}\right|_{max} . \qquad (3\text{-}85)$$

Now that the INL and DNL expressions of the reference generation circuitry have been derived, the linearity errors of the reference generation circuitry can be calculated based upon a given resistor mismatch. For this application, 6-bits of resolution with a nominal reference voltage of 1.275 V is desired. Therefore, the reference generation circuitry must contain 2^N or 64 resistors. Suppose resistor matching of 1% is achieved in the reference generation circuitry. The maximum INL error contribution of the resistor string expressed as a fraction of an ADC LSB is given by

$$|INL|_{max} = \frac{\frac{V_{ref}}{2}\left|\frac{\Delta R}{R}\right|_{max}}{1\ LSB} = \frac{\frac{1.275}{2}\left|\frac{0.01R}{R}\right|_{max}}{\frac{V_{ref}}{2^N}} = \frac{6.37\ mV}{20\ mV} = 0.32\ LSB\ . \qquad (3\text{-}86)$$

The maximum DNL error contribution of the resistor string expressed as a fraction of an ADC LSB is given by

$$|DNL|_{max} = \frac{\frac{V_{ref}}{2^N}\left|\frac{\Delta R}{R}\right|_{max}}{1\ LSB} = \frac{\frac{1.275}{2^6}\left|\frac{0.01\ R}{R}\right|_{max}}{\frac{V_{ref}}{2^6}} = \frac{0.02\ mV}{20\ mV} = 0.01\ LSB\ . \qquad (3\text{-}87)$$

Note that resistor matching in the reference generation circuitry is not as critical when determining the DNL compared to an INL specification of equal value The INL specification is the limiting factor in the determining the required matching accuracy of the resistor string since its maximum error value can be $2^{(N-1)}$ times larger than the maximum DNL error that can occur. It is important to note that both resistor string INL and DNL expressions are independent of the reference voltage applied to the resistive

ladder and the absolute value of the resistors, but are dependent only upon resistor matching, and the total number of resistors in the string.

3.3 ADC Non-linearity Analysis

The linearity performance of the ADC is dependent upon the controlled offset voltages of the comparators and the accuracy of the reference generation circuitry. The non-linearity analyses of each of these two critical sections of the ADC have already been derived and presented. However, these results can be combined to describe the total non-linearity errors present in a flash or flash-type ADC based upon the offset voltage of the comparators and resistor matching in the reference generation circuitry.

The maximum INL error present in the ADC can be found by combining Equations 3-3 and 3-81. The worst-case INL error associated with the ADC expressed as a fraction of an LSB is given by

$$INL_{ADC} = \frac{|V_{OS}|_{\max} + \frac{V_{ref}}{2}\left|\frac{\Delta R}{R}\right|_{\max}}{1\,LSB} = \frac{|V_{OS}|_{\max} + \frac{V_{ref}}{2}\left|\frac{\Delta R}{R}\right|_{\max}}{\frac{V_{ref}}{2^N}} \tag{3-87}$$

Similarly, Equations 3-6 and 3-85 can be combined to establish the maximum DNL error that can occur in the ADC. The worst-case DNL error associated with the ADC expressed as a fraction of an LSB is given by

$$DNL_{ADC} = \frac{|V_{OS_i} - V_{OS_{i+1}}|_{\max} + \frac{V_{ref}}{2^N}\left|\frac{\Delta R}{R}\right|_{\max}}{1\,LSB} = \frac{2|V_{OS}|_{\max} + \frac{V_{ref}}{2^N}\left|\frac{\Delta R}{R}\right|_{\max}}{\frac{V_{ref}}{2^N}}, \tag{3-88}$$

which assumes two adjacent comparators have maximum comparator offset voltages in

the positive and negative directions.

Some observations can be made regarding Equations 3-87 and 3-88. First of all, the DNL errors of the ADC will be totally dominated by the offset voltage of the comparators and the resistor mismatch in the reference generation circuitry is negligible. Interesting to note, however, that both resistor mismatch and comparator offset can be significant contributors to INL errors in a flash or flash-type ADC. Therefore, both the offset voltages of the comparators and resistor mismatches must be well controlled over process variations to guarantee good ADC linearity performance.

Suppose resistor matching of 1% is achieved in the reference generation circuitry and the maximum corrected comparator offset voltage is maintained below 2.5 mV. Based upon these assumptions, the INL and DNL errors of the ADC can be calculated. The worst-case INL of the ADC can be calculated by using Equation 3-87 and is given by

$$INL = \frac{2.5\,mV + \frac{1.275}{2}\left(\frac{0.01R}{R}\right)}{1\,LSB} = \frac{8.9\,mV}{20\,mV} = 0.44\,LSB\ . \qquad (3\text{-}89)$$

The DNL of the ADC can also be calculated by using Equation 3-88 and is given by

$$DNL = \frac{2(2.5\,mV) + \frac{1.275}{2^6}\left(\frac{0.01R}{R}\right)}{1\,LSB} = \frac{5.2\,mV}{20\,mV} = 0.26\,LSB\ . \qquad (3\text{-}90)$$

The calculated INL and DNL values based upon the assumptions above will meet the linearity requirements of the converter. Therefore, resistor matching of 1% or less in the reference generation circuitry and corrected comparator offset voltages of less than 2.5 mV are good design goals that should meet the linearity performance required for this 6-bit ADC application.

3.4 Digital Error Correction and Encoder Description

The outputs of the comparators in flash or flash-type ADC architectures should form a thermometer code with a single transition point. A well-behaved comparator output bank in a flash converter produces a sequence of ones up to a certain point and then contains a sequence of zeroes beyond that point. Figure 3-22 shows an example of a thermometer code in a classical 3-bit flash ADC. However, due to comparator metastability, noise, delay mismatches between comparators, limited bandwidth, and other effects, the comparator outputs may produce out-of-sequence ones and zeroes in the thermometer code. This effect is called thermometer code bubbles. These bubbles can easily be recognized by a one found among zeroes or a zero found among ones. However, these bubbles usually occur near the transition point of the thermometer code.

These bubbles can be removed by using three-input NAND gates to provide limited digital error correction. This correction technique is shown in Figure 3-23. With this decoding modification, there must now be at least two consecutive zeros above a one in determining the correct transition point in the thermometer code. Thus, the digital error correction detects a 1-0-0 transition in the thermometer code. Note that this method of digital error correction does not eliminate all possible bubble errors, but analysis of the most common types of bubbles shows that this techniques greatly reduces the probability of a bubble propagating through the transition detection circuitry [17].

The data is encoded by three-input NAND gates that generate a single logic 0 in the output data. Thus, the encoder design required is a 0-out-of-1 detection scheme. Also, the use of three-input gates instead of two guarantees a monotonic transfer function. This

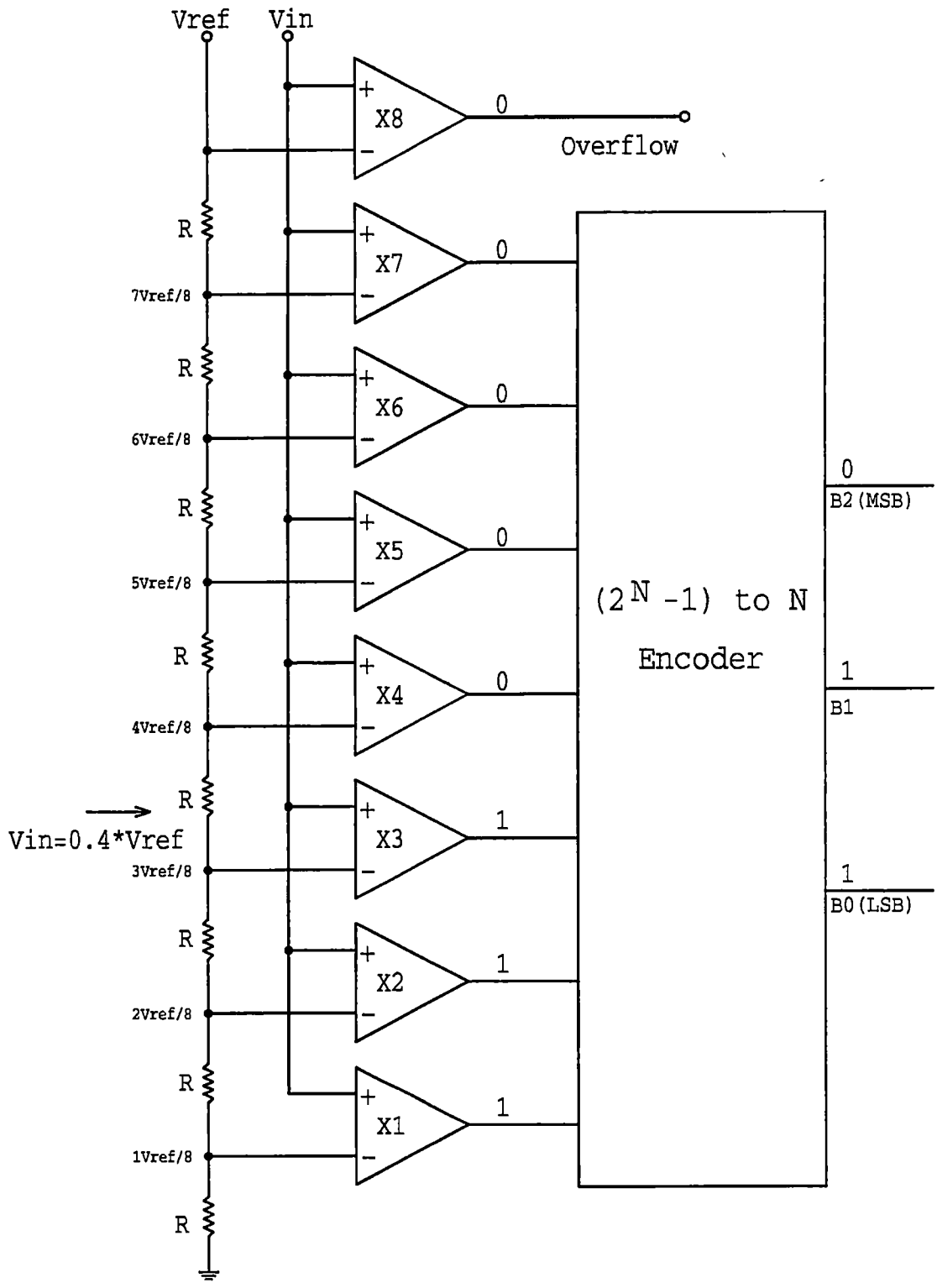


Figure 3-22. An example of a thermometer code in a classical 3-bit flash ADC.

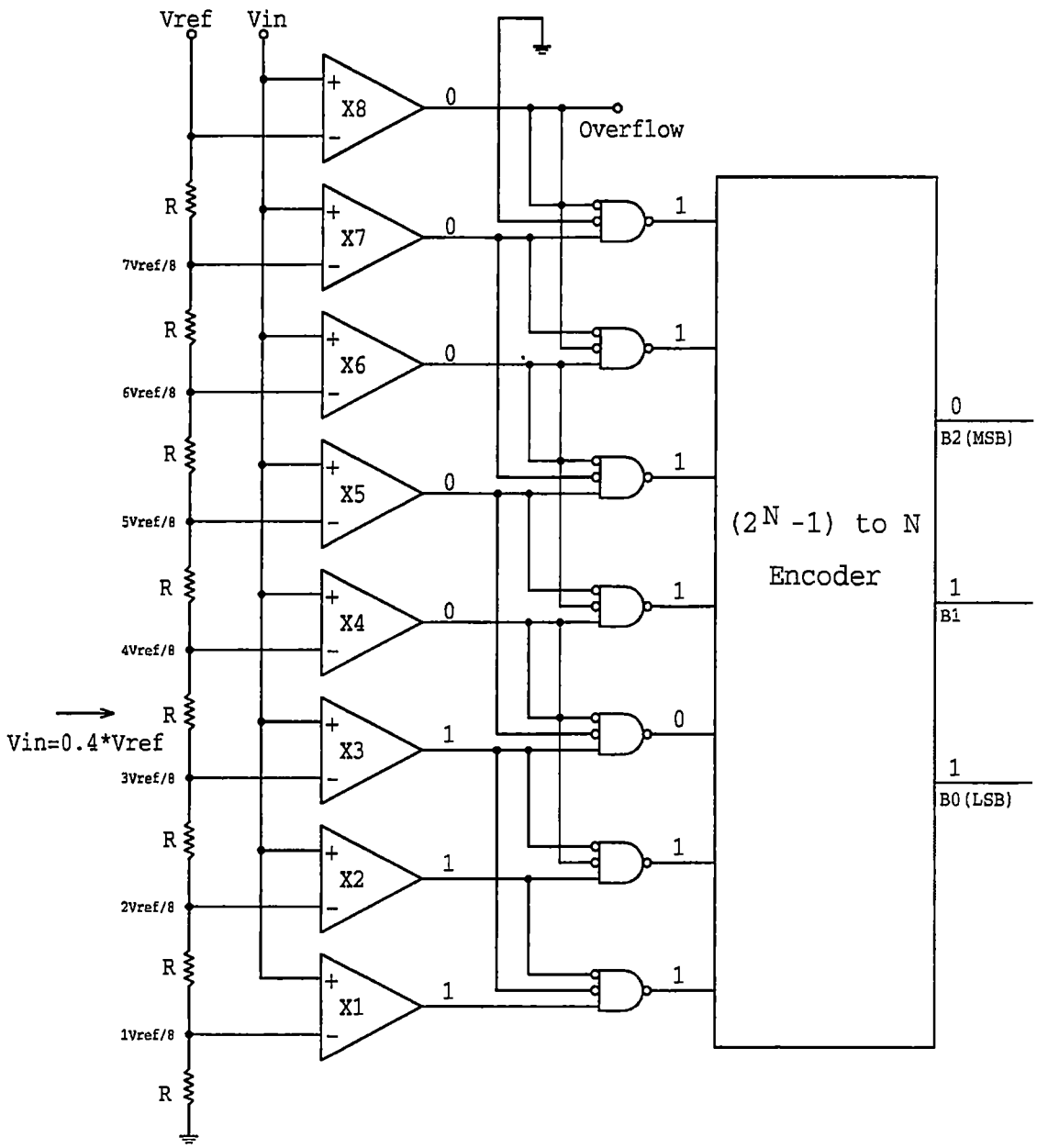


Figure 3-23. Limited digital error correction provided from 3-input NAND gates.

is because the code sequence that will identify the 0-1 transition in the comparator outputs is a one and two zeroes from three consecutive comparators instead of a one followed by a zero from only two comparators. The encoder is designed to select the highest 1-0-0 transition and may result in a larger output code, but this will not result in a monotonicity error.

Metastability errors in ADCs occurs when undefined comparator outputs are passed to the digital encoder which can result in an incorrect output code. Under normal operating conditions in a flash or flash-type converter, the comparator outputs generate a thermometer code. The comparators with reference levels below the input signal will output a logical 1 and the rest of the comparators will have a logical 0 as their outputs. However, if the input signal is close or equal to a reference voltage for a particular comparator, then that comparator's output may be undefined at the end of the allotted evaluation time. There always exist a finite probability that the voltage difference at the input of a given comparator cannot be sufficiently amplified to achieve valid CMOS logic levels within the allotted comparison time. Thus, when this condition occurs, the output of the comparator is undefined and this indeterminate digital logic level is passed to the digital encoder possibly causing errors. This phenomenon is referred to as comparator metastability and is illustrated in Figure 3-24.

Since comparator metastability in high-speed ADCs can cause performance limiting glitches in the converter's output code, minimizing errors due to metastability is important . While it is possible to reduce error rates by improving the comparator or latch design, this typically conflicts with other requirements such as low area and power

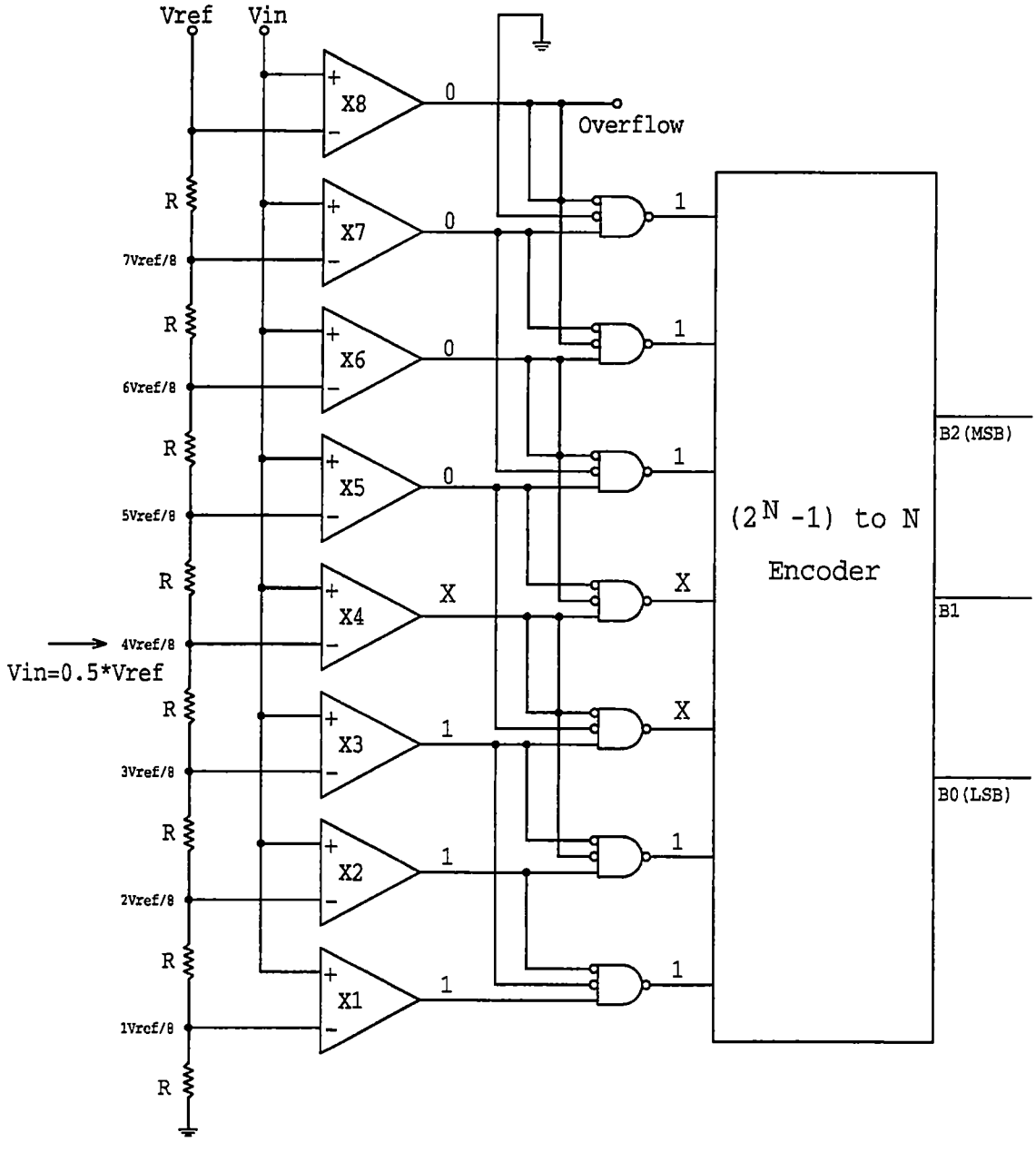


Figure 3-24. An example of comparator metastability in a 3-bit flash ADC.

dissipation. Metastability error probability can be related to the regenerative time constant of the latch used in the comparator channel. The smaller the regenerative time constant of the latch, the lower the metastability error rate. Normally, most of the parameters of the metastability probability expression are not known with sufficient accuracy to determine the metastability error rate to more than an order of magnitude [17, 37].

Metastability errors in flash or flash-type ADCs are fundamental and can be reduced but never completely eliminated. For this application, a very low metastability error rate is not required. This is because other issues such as finite time resolution in the event capture circuitry and scanner efficiency performance will dominate the overall error rate of the time measurement system. The addition of a second latch in the comparator channel has been reported to reduce metastability errors in flash ADCs by two orders of magnitude [17, 37]. Since metastability error rate is not critical for this application, this simple metastability reduction technique was implemented in this design.

3.5 ADC Timing Information and Digital Controller Requirements

Although the digital control logic design of the ADC is not the focus of this work, certain relevant ADC timing information is presented in this section. The ADC control logic, which utilizes the 16 ns system clock, is responsible for all the necessary timing information to generate MSB and OSB comparator control signals and interfaces the ADC with the rest of the system. Figure 3-25 presents the two-step flash ADC timing diagram which shows most of the relevant ADC control signals and documents the ADC

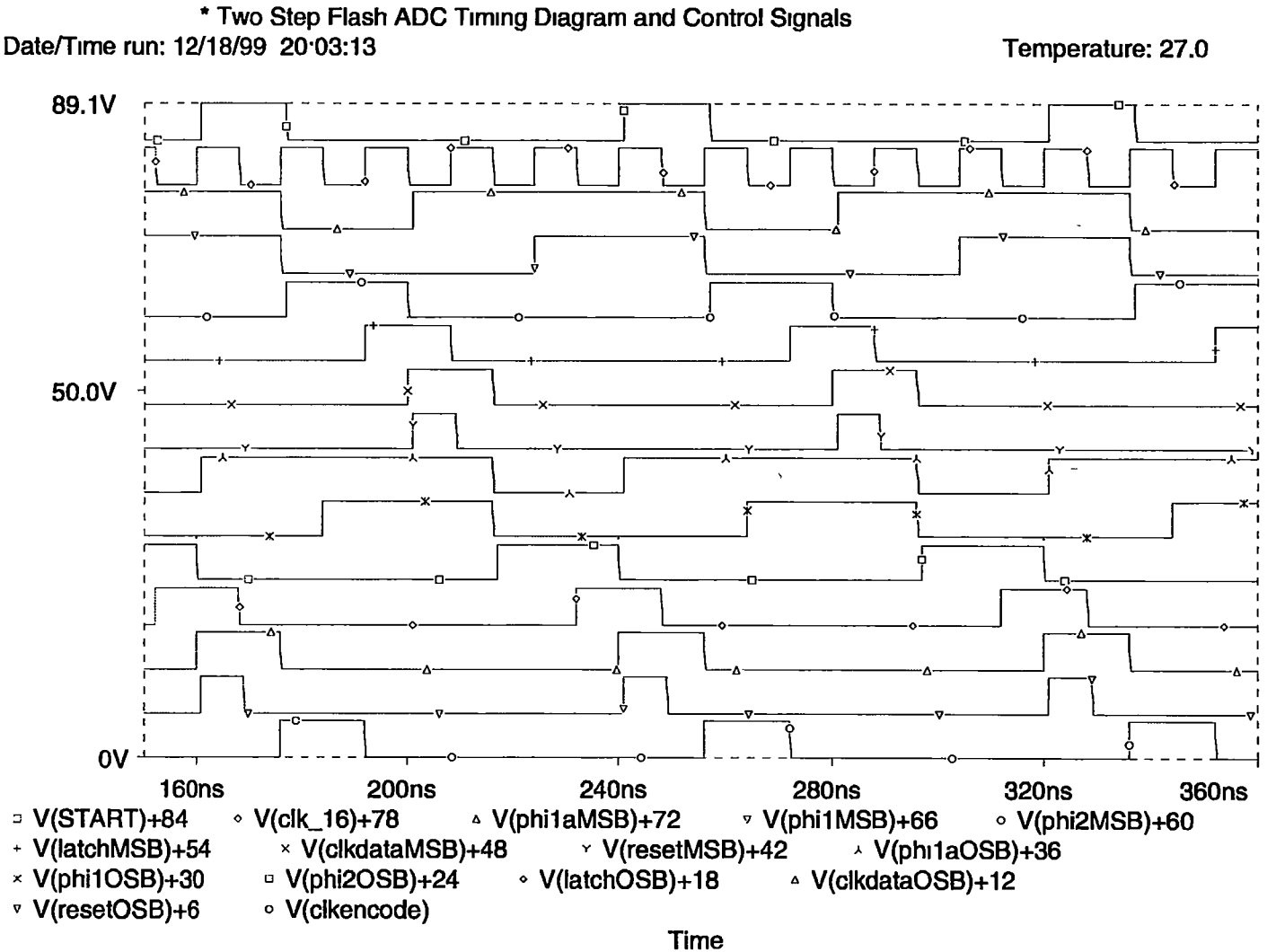


Figure 3-25. Two-step flash ADC timing diagram and control signals.

timing information and controller requirements. The specification of the ADC controller requirements assumes that a synchronous *START* command will be provided to the ADC from the system to initiate a conversion Once the *START* command is received, the MSB comparison process begins while the OSB comparators remain in the auto-zero mode The MSB comparator has 24 ns to compare the analog input signal with $½V_{ref}$. At the end of this evaluation time period, the output of the MSB comparator is clocked into a register. A total time period of 16 ns is allowed for the interpretation of the MSB output and selection of the appropriate reference levels for the OSB comparators. Meanwhile, after the output of the MSB channel is registered, the MSB comparator immediately enters auto-zero mode to get ready for the next conversion. After the reference voltages are selected, the OSB comparators begin their comparison process, which consumes 24 ns of conversion time. Finally, the output of the OSB comparators are clocked into their output registers and encoding with error correction is performed during the allowed latency period of one 16 ns clock cycle.

Chapter 4

ADC Transistor Level Design, Layout, and Simulation

4.1 Preamplifier Design, Layout, and Simulation

The preamplifier was developed based upon the analysis presented in Chapter 3. A detailed schematic of the preamplifier, which shows all device sizes and bias currents, is given in Figure 4-1. Since the preamplifier is being used in an OOS correction technique, the circuit was designed for a nominal gain of 20 dB with a bandwidth that allowed the comparator outputs to reach their final values within a comparison time of 16 ns. Gain allocation of the two gain stages in the preamplifier was performed to achieve a small input capacitance while maintaining good bandwidth performance. This design methodology resulted in the use of small device sizes for the input differential pair and a 4X PMOS current mirror gain configuration for transistors *M4-M7*. Also, non-minimum gate lengths were used in most devices to improve transistor matching resulting in tighter open loop gain control and lower random offset voltage effects. In addition, device sizes and bias currents were selected to achieve a common-mode input range of at least 2 volts.

The simulated frequency response of the preamplifier with all parasitic layout and load capacitances is shown in Figure 4-2. The preamplifier achieves a bandwidth of f_{-3dB} = 57 MHz and a gain-bandwidth-product of 570 MHz while consuming 300 μA of current. The parasitic layout capacitances decreased the preamplifier's bandwidth performance by 15 MHz. Also, the load capacitance of 75 fF degraded the frequency response by an additional 30 MHz. The load capacitance of 75 fF is a conservative (15%)

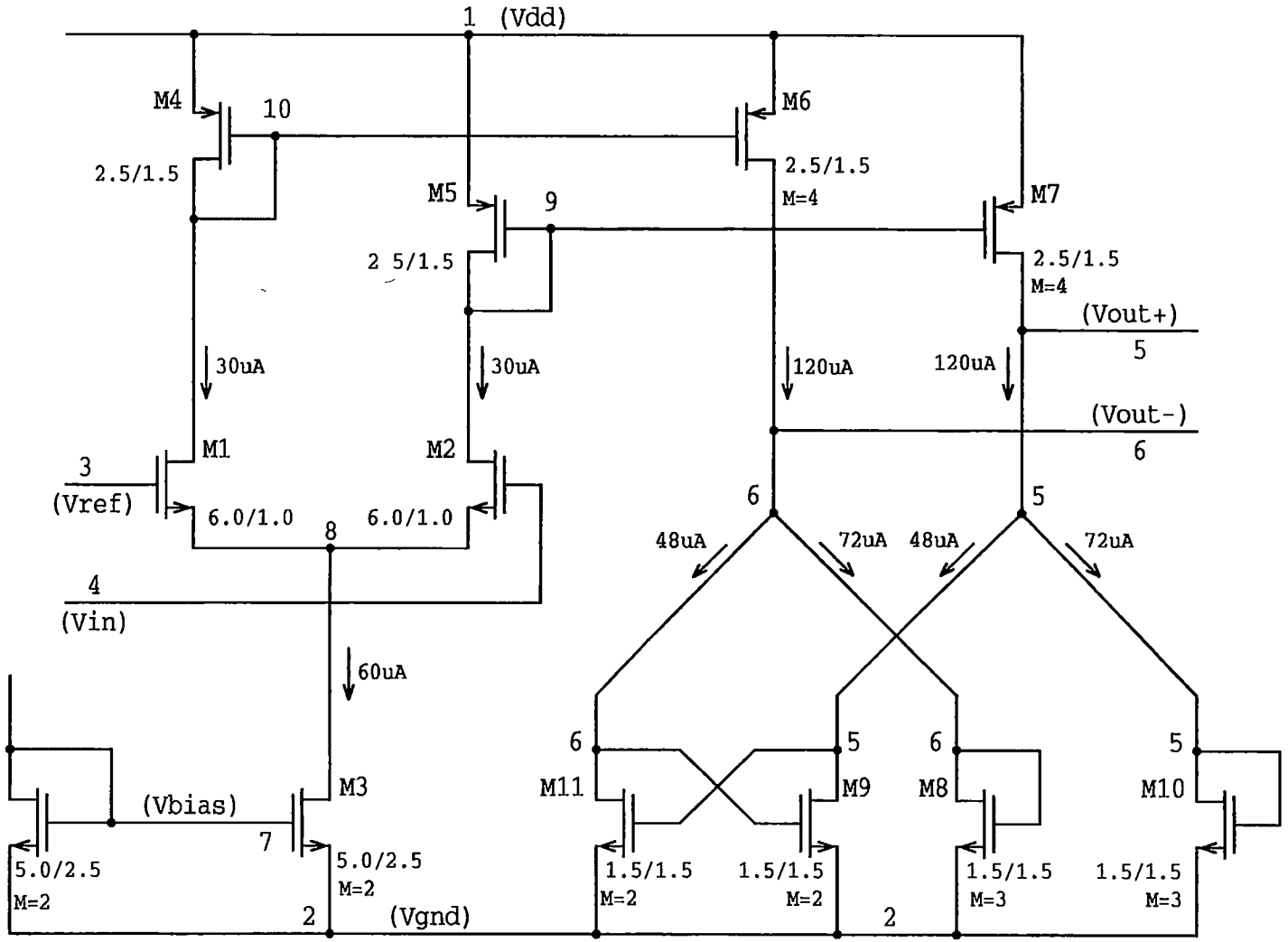


Figure 4-1. Schematic diagram of preamplifier including transistor sizes (in μm) and bias currents.

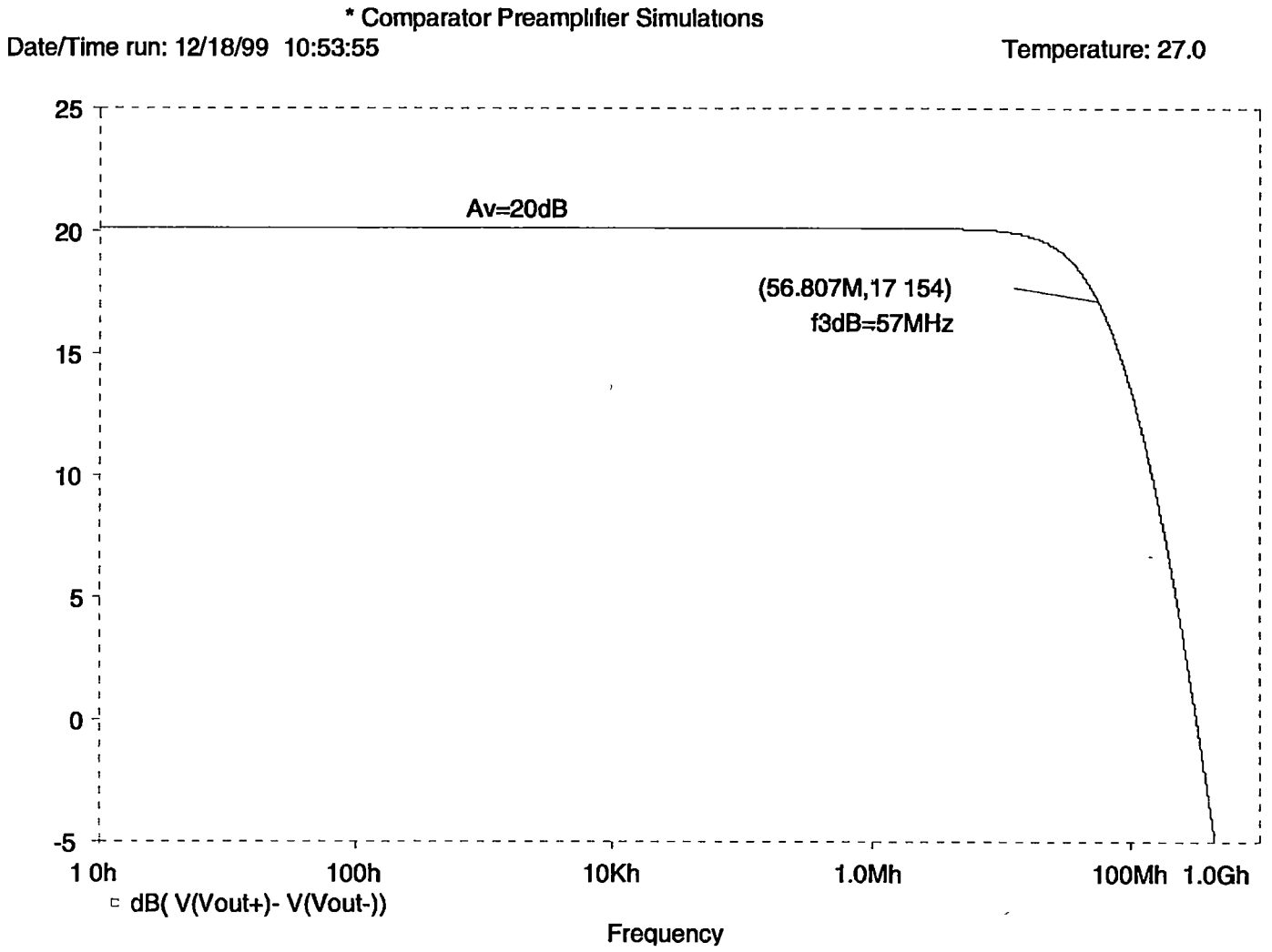


Figure 4-2. Frequency response of the preamplifier with a 75 fF load capacitance.

approximation of the parasitic capacitance that is associated with the output offset storage capacitors, which are nominally 0.5 pF. The transient response of the preamplifier is shown in Figure 4-3. This simulation verifies that the preamplifier has a gain of approximately 20 dB and the differential outputs reach their final value within the allotted evaluation time period of 16 ns with a ±10 mV input signal overdrive condition.

The preamplifier's dc output transfer function was found by sweeping V_{in} from 2 V to 3 V with V_{ref} held at 2.5 V. The result of this simulation is shown in Figure 4-4. The preamplifier achieves zero systematic offset error performance with no hysteresis. Figure 4-4 also shows that the output transfer characteristics of the preamplifier is very much a nonlinear response. However, the preamplifier does exhibit a fairly linear region of operation when the input lies within ±50 mV from the reference voltage. This characteristic of the preamplifier, which is illustrated in Figure 4-5, is important since the circuit will employ an OOS calibration technique. Since the preamplifier's output is linearly related to its input, in this region of operation, the preamplifier can accommodate and correct offsets of at least 50 mV in magnitude. The nonlinear response of the preamplifier can be explained with the help of Figure 4-6, which shows the bias currents in the output transistors in addition to the preamplifier outputs. Note that switching of the preamplifier outputs occurs when the currents in *M8* and *M10* are equal and the currents in *M9* and *M11* are equal. The addition of transistors *M9* and *M11*, combined with *M8* and *M10*, provides limited positive feedback that increases the gain and performance of the preamplifier. However, this feedback loop is effectively disabled when any of output transistors (*M8-M11*) turn off. Thus, the nonlinear behavior of the preamplifier's transfer

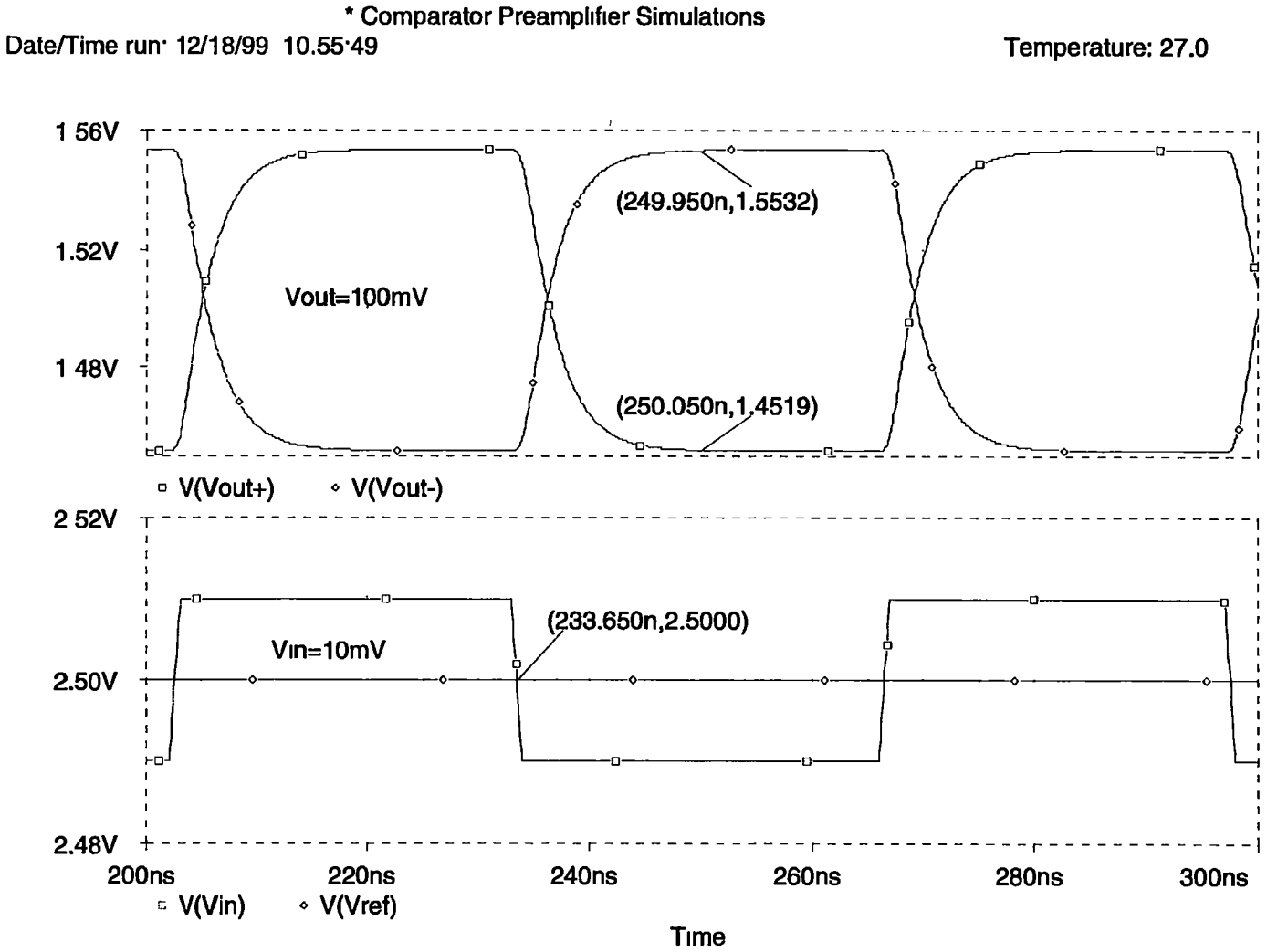


Figure 4-3. Transient response of the preamplifier with a 10 mV input overdrive signal.

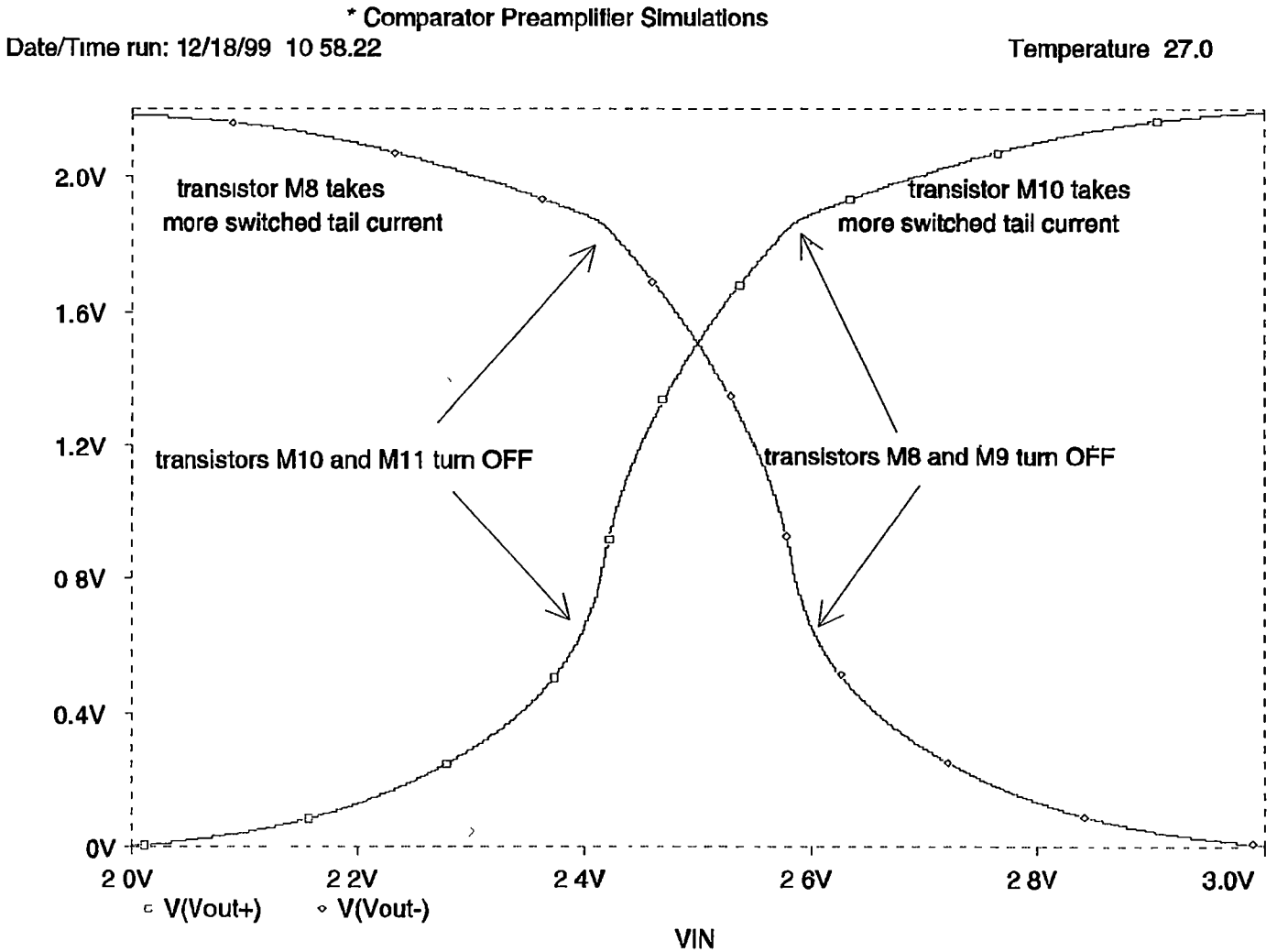


Figure 4-4. DC sweep response giving the Vout vs. Vin transfer function of the preamplifier.

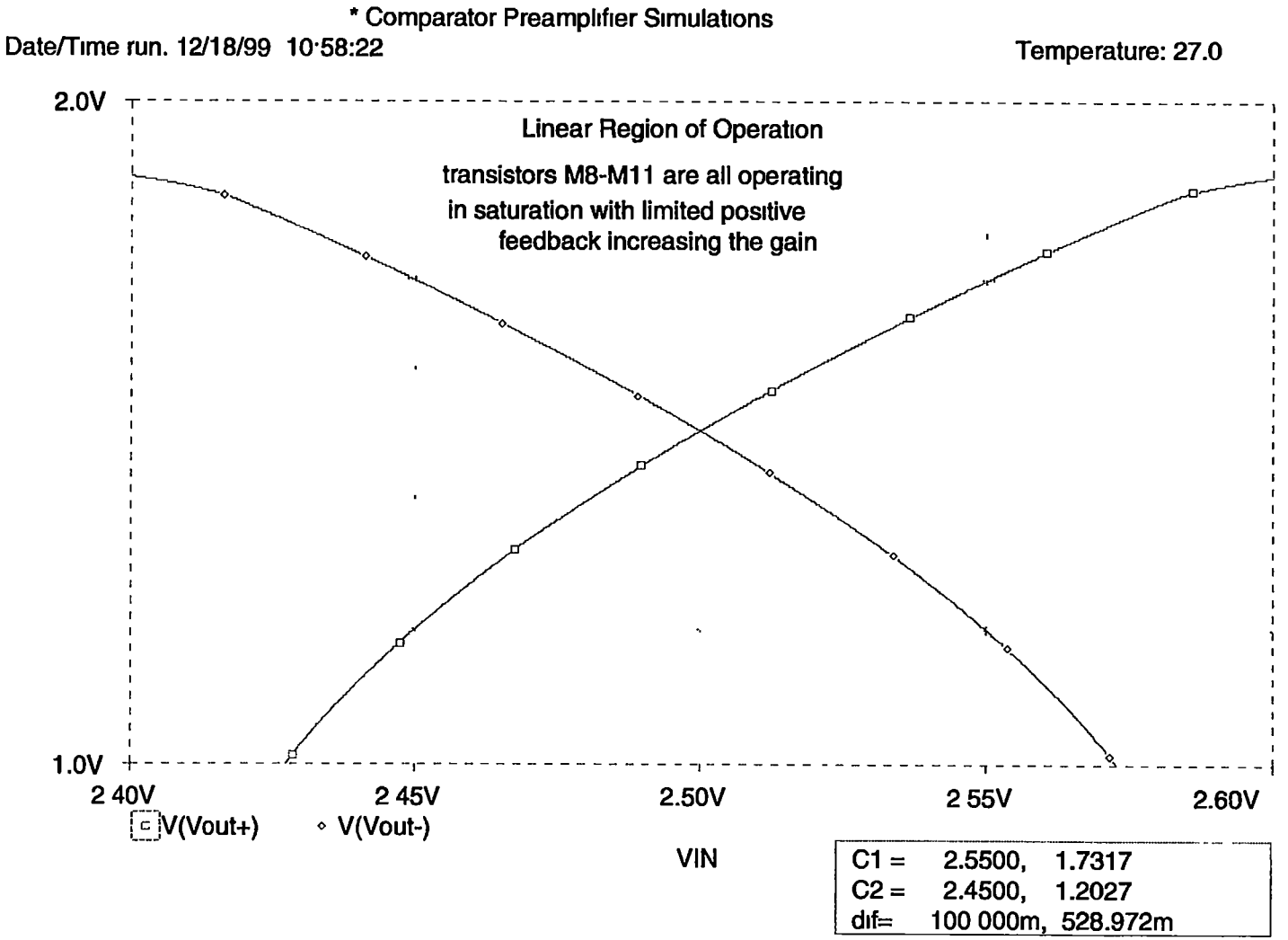


Figure 4-5. DC sweep response showing the preamplifier's linear region of operation.

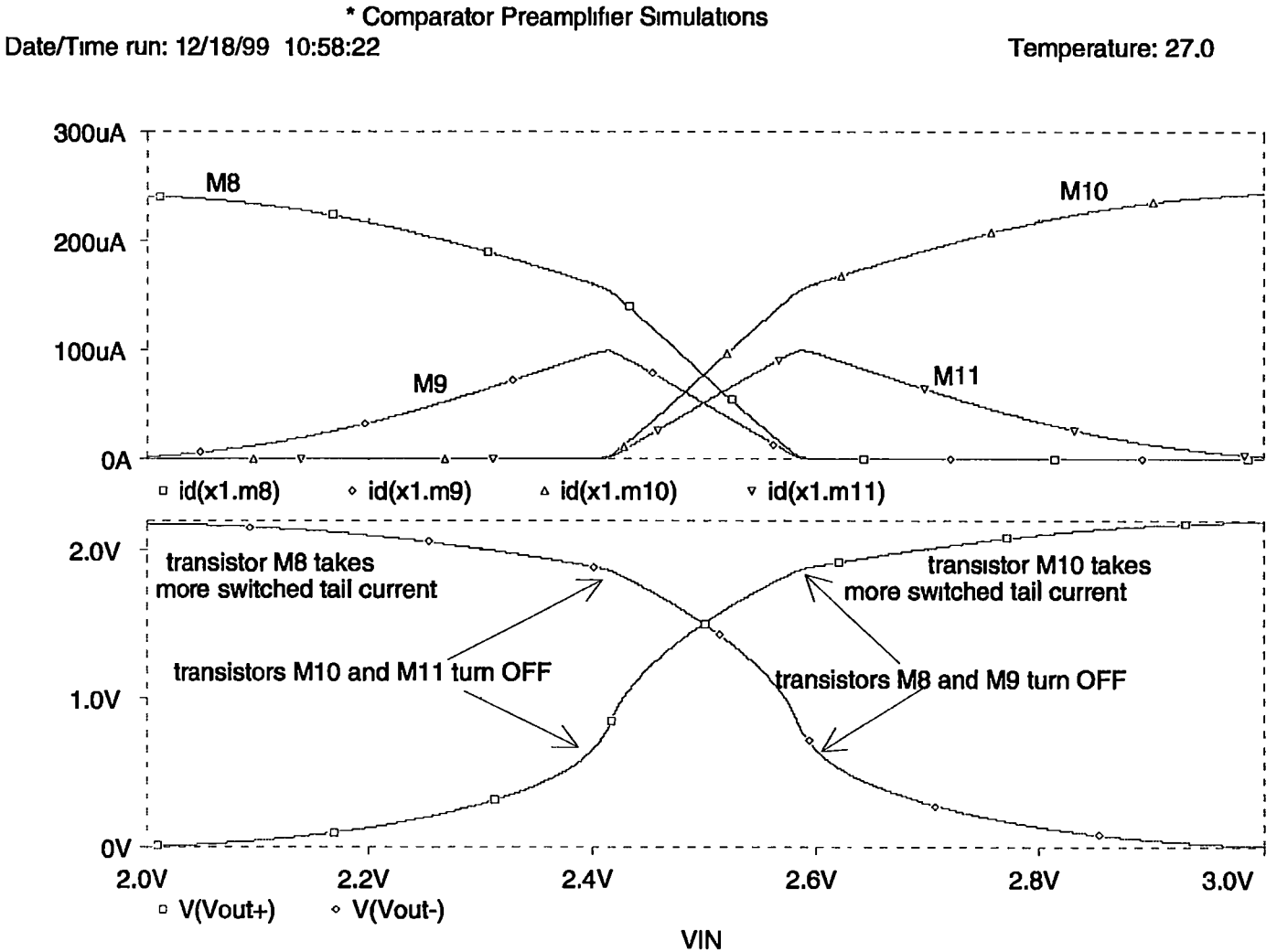


Figure 4-6. DC sweep response of the preamplifier showing device currents and bias conditions.

function is due to the fact that the positive feedback used in the preamplifier is only active for a limited range of input signal.

Figure 4-7 shows the gain and frequency response of the preamplifier over a 2 volt (2 V-4 V) common-mode input range. There is a slight decrease (7%) in the preamplifier's gain as the common-mode input voltage is increased. This gain variation is due to the body effect on the differential input transistor pair. As the common-mode voltage increases, the threshold voltages of the input transistor pair increases due to body effect and this lowers the effective transconductance of the input stage transistors which decreases the gain of the input stage and results in an overall lower gain of the preamplifier. This slight open loop gain variation is only a concern if the preamplifier's gain changes or is different when the circuit is in an OOS correction mode versus comparison mode. The gain variation of the preamplifier has no consequences for the MSB comparator channel since the MSB comparator uses the same reference voltage value all the time. However, since reference voltages for the OSB comparators are switched based upon the MSB comparator decision, the gain variation of the preamplifier deserves some consideration for the OSB comparator channels. Special attention was dedicated in the ADC design to ensure that the OSB comparator channel always used the same reference voltage in both the auto-zero and comparison modes. If this condition is not satisfied, then a residual input-referred offset error is created due to the preamplifier's gain variation as a function of common-mode input range. The requirement of using the same reference voltage for both auto-zero and comparison mode was achieved in the OSB comparator channels by starting the preamplifier's OOS calibration process based

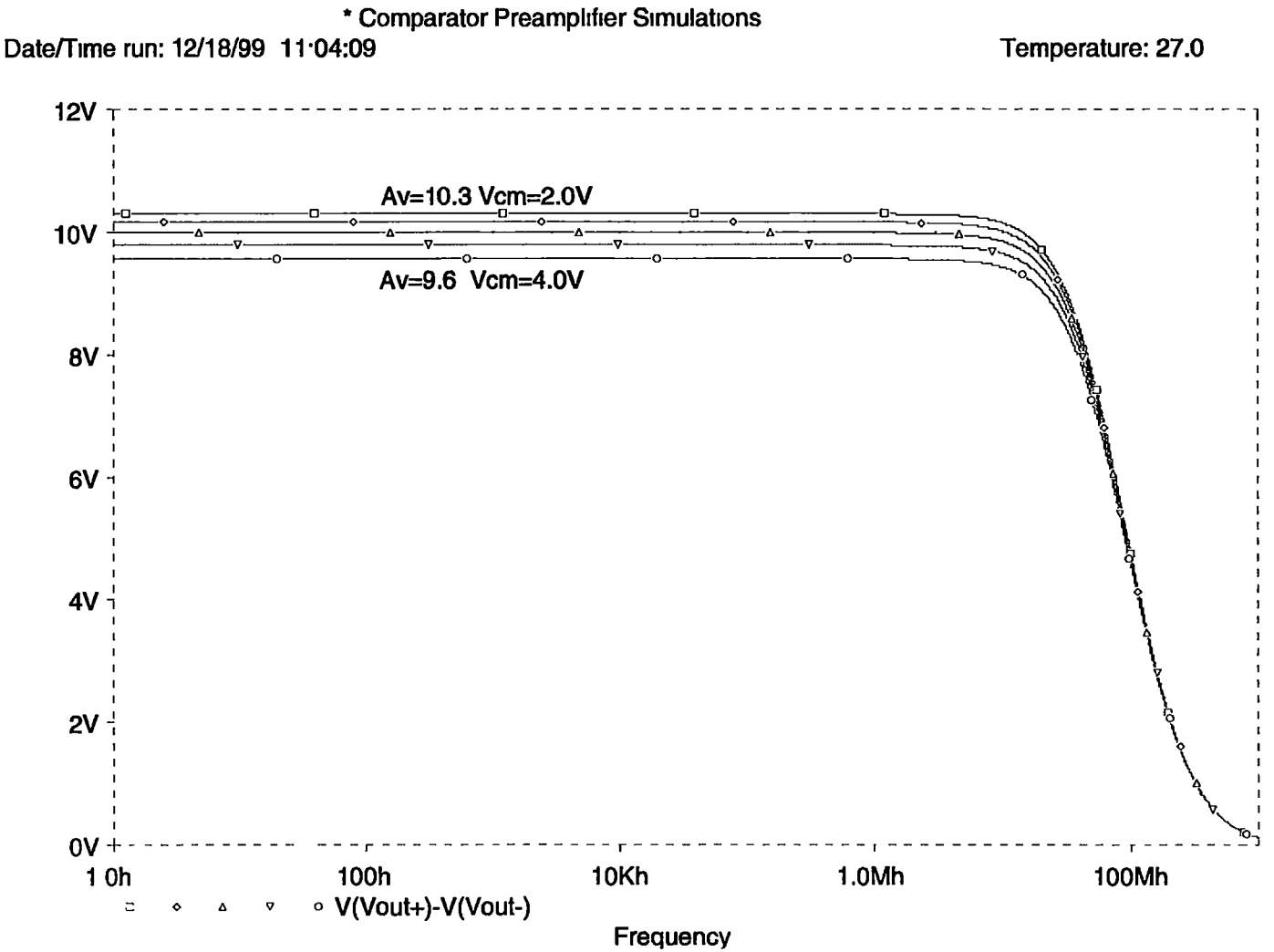


Figure 4-7. Preamplifier gain variation as a function of a 2-volt common-mode input range.

upon the last reference selected from the previous conversion and then switching the OSB references as soon as the MSB comparator decision was available.

The integrated circuit layout plot of the preamplifier is shown in Figure 4-8. Special attention was given to the layout to keep all interconnects as short as possible to reduce parasitic layout capacitances. Also, guard rings were placed extensively around the design to minimize substrate noise and clock coupling into the input. Transistor replication techniques were used in the layout to improve transistor matching resulting in tighter open loop gain control and lower random offset voltage effects. The preamplifier occupies a silicon area of 51 μm x 66 μm and dissipates 1.5 mW from a single 5 V supply.

4.2 Regenerative Latch Design, Layout, and Simulation

The regenerative latch was developed based upon the analysis presented in Chapter 3. A detailed schematic of the regenerative latch circuit, which shows all device sizes and bias currents, is given in Figure 4-9. Since the functionality of the latch circuit is essentially identical to the preamplifier when placed into the comparison mode, a similar design methodology was implemented. The regenerative latch was designed for a gain of around 20 dB in comparison mode with a bandwidth that allowed good transient response in the allotted 16 ns comparison time.

As expected, the simulation results of the latch circuit when in compare mode are very similar to that achieved with the preamplifier. The simulated frequency response of the regenerative latch with all parasitic layout and load capacitances is illustrated in

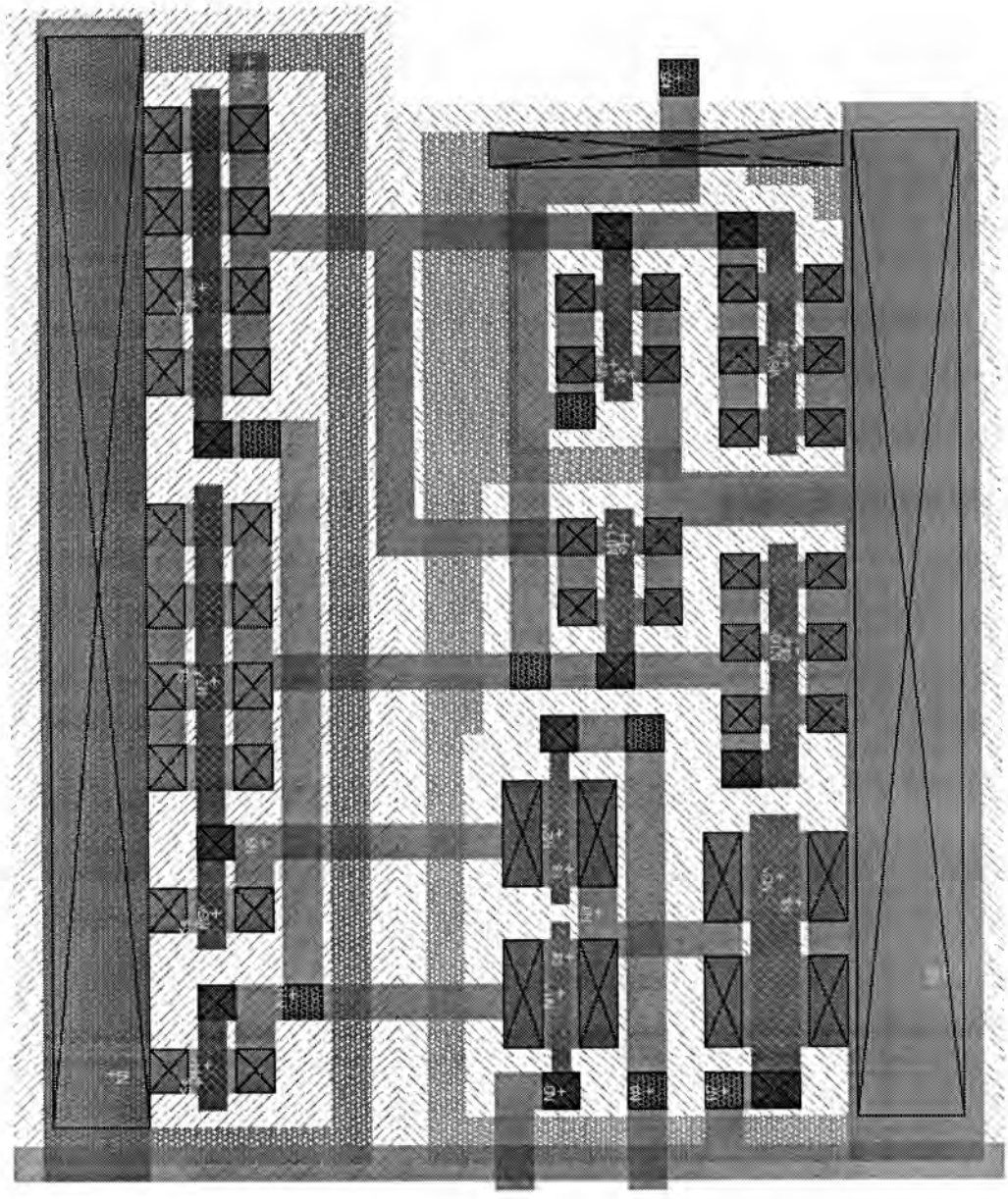


Figure 4-8. Integrated circuit layout plot of the preamplifier.

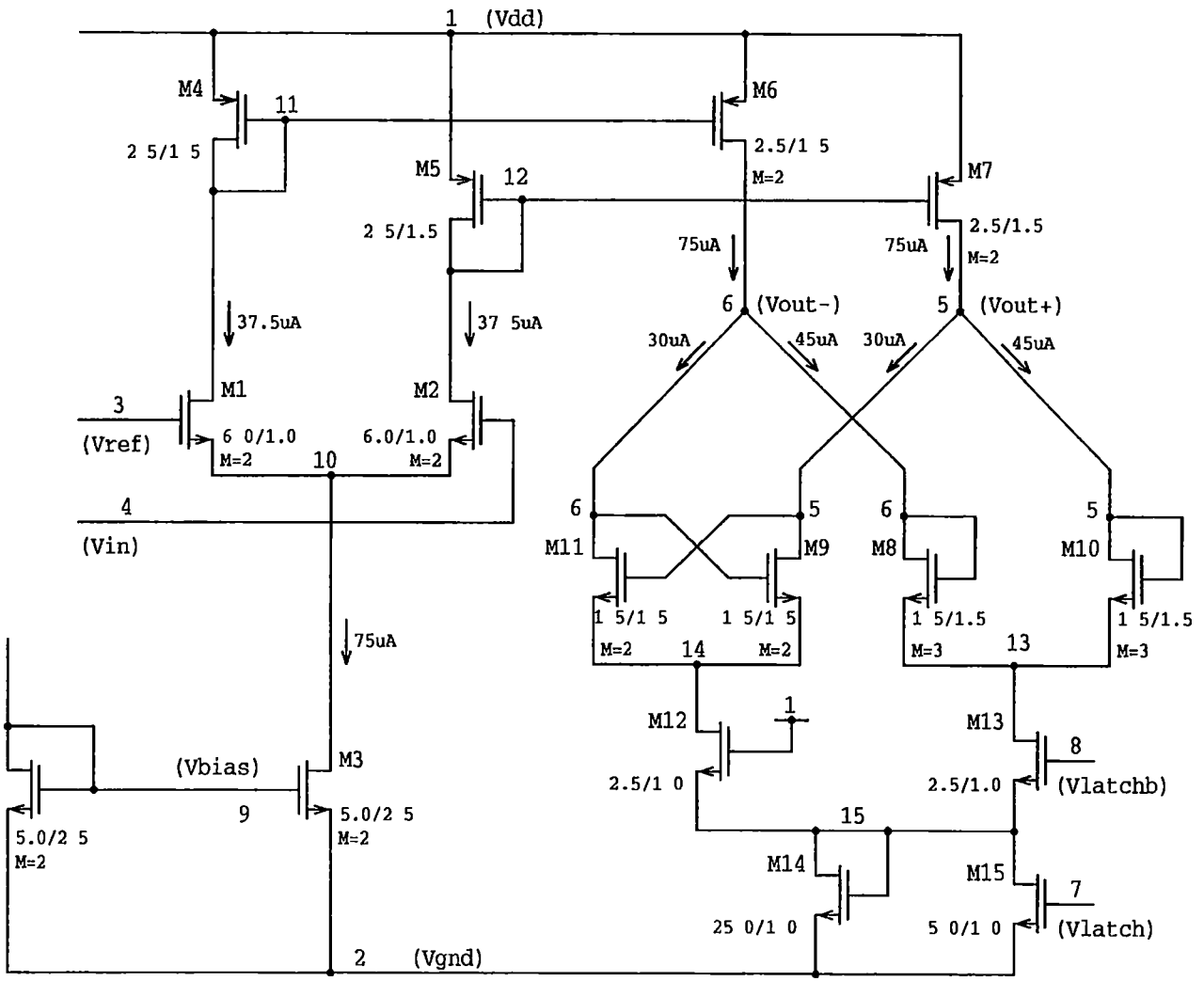


Figure 4-9. Schematic diagram of regenerative latch including transistor sizes (in μm) and bias currents.

Figure 4-10. The latch circuit design achieves a gain of approximately 21 dB with a bandwidth of f_{-3dB} = 55 MHz. The transient response of the latch circuit when in compare mode is shown in Figure 4-11 for a ±10 mV input signal overdrive condition. This simulation verifies that the latch has a gain of approximately 21 dB and the differential outputs reach their final value within the allotted evaluation time period of 16 ns. Special consideration was given to the design and simulation of the regenerative latch when the circuit transitioned into latch mode. The performance of the latch circuit in this regenerative mode is critical since the circuit needs to supply enough amplification to convert potentially very small analog signals to full CMOS logic levels. The regenerative latch was designed to make this transition to logic levels within an 8 ns time period. Figure 4-12 shows the transient response of the latch circuit in regenerative mode for different levels of input overdrive. The simulated transient response of the latch is based upon a 16 ns comparison interval and an 8 ns regenerative latch period. The performance of the latch is very impressive since the circuit is able to compare very small input signals and convert them to CMOS logic levels within a total time period of 24 ns. Also, note that the latch response for all input signal conditions displays basically the same shape but is just delayed in time as predicted by the latch analysis presented in Chapter 3.

The integrated circuit layout plot of the regenerative latch is shown in Figure 4-13. Special attention was given to the layout to keep all interconnects as short as possible to reduce parasitic layout capacitances. Also, guard rings were placed extensively around the design. Transistor replication techniques were used in the layout to improve transistor matching resulting in tighter open loop gain control and lower random offset voltage

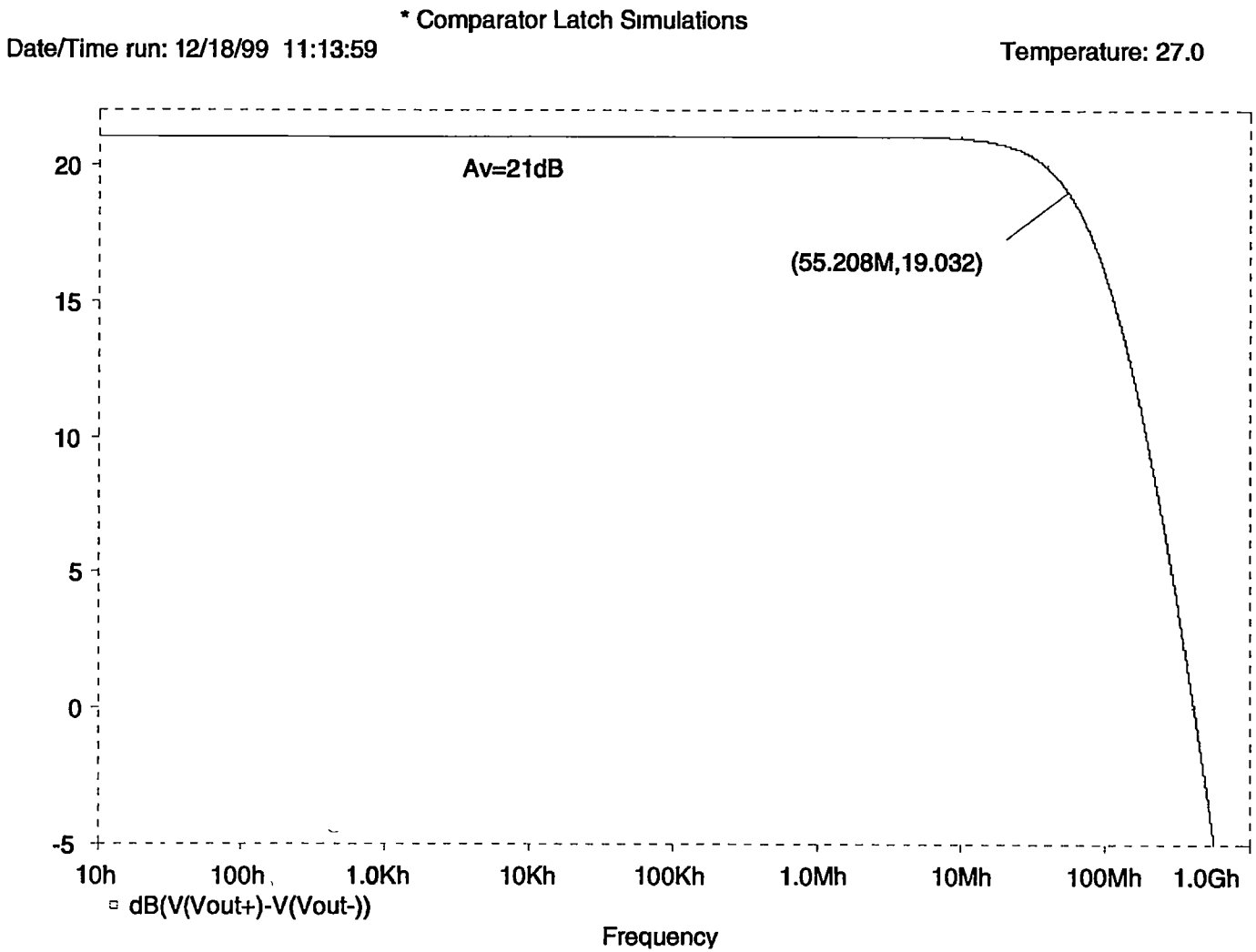


Figure 4-10. Frequency response of the regenerative latch in compare mode with a 25 fF load capacitance.

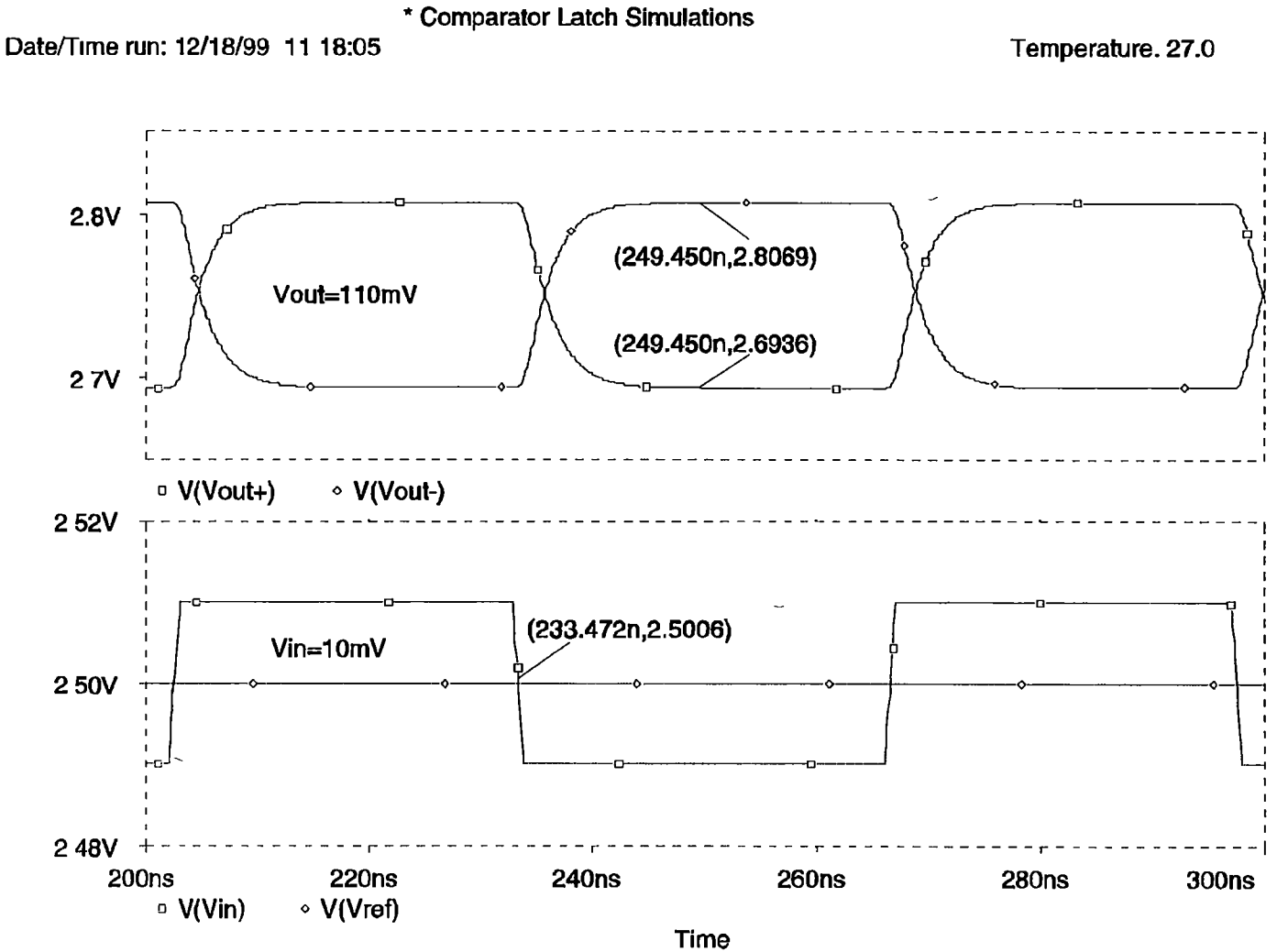


Figure 4-11. Transient response of the regenerative latch in compare mode with a 10 mV input overdrive.

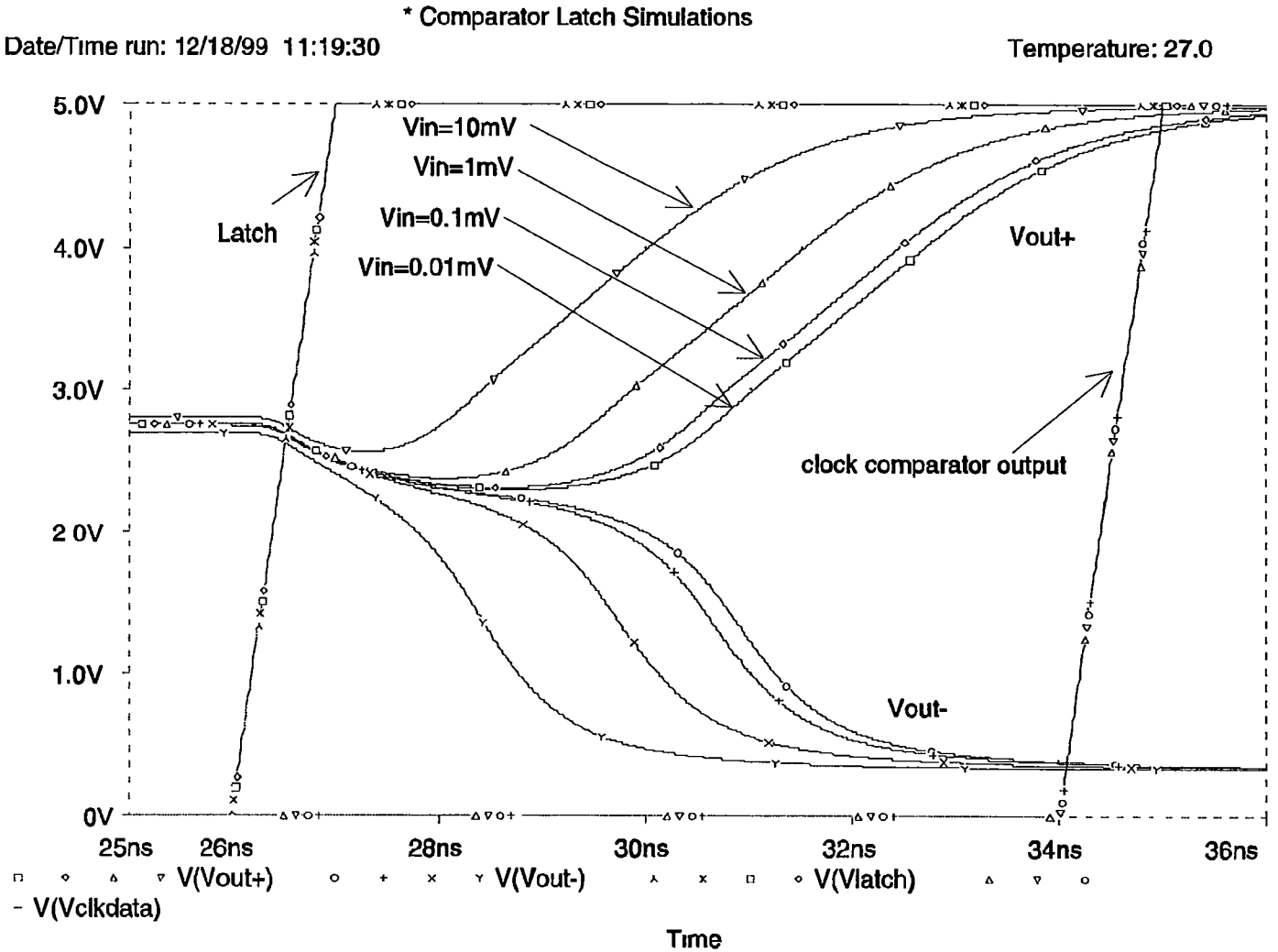


Figure 4-12. Transient response of the regenerative latch in latch mode for different levels of input overdrive.

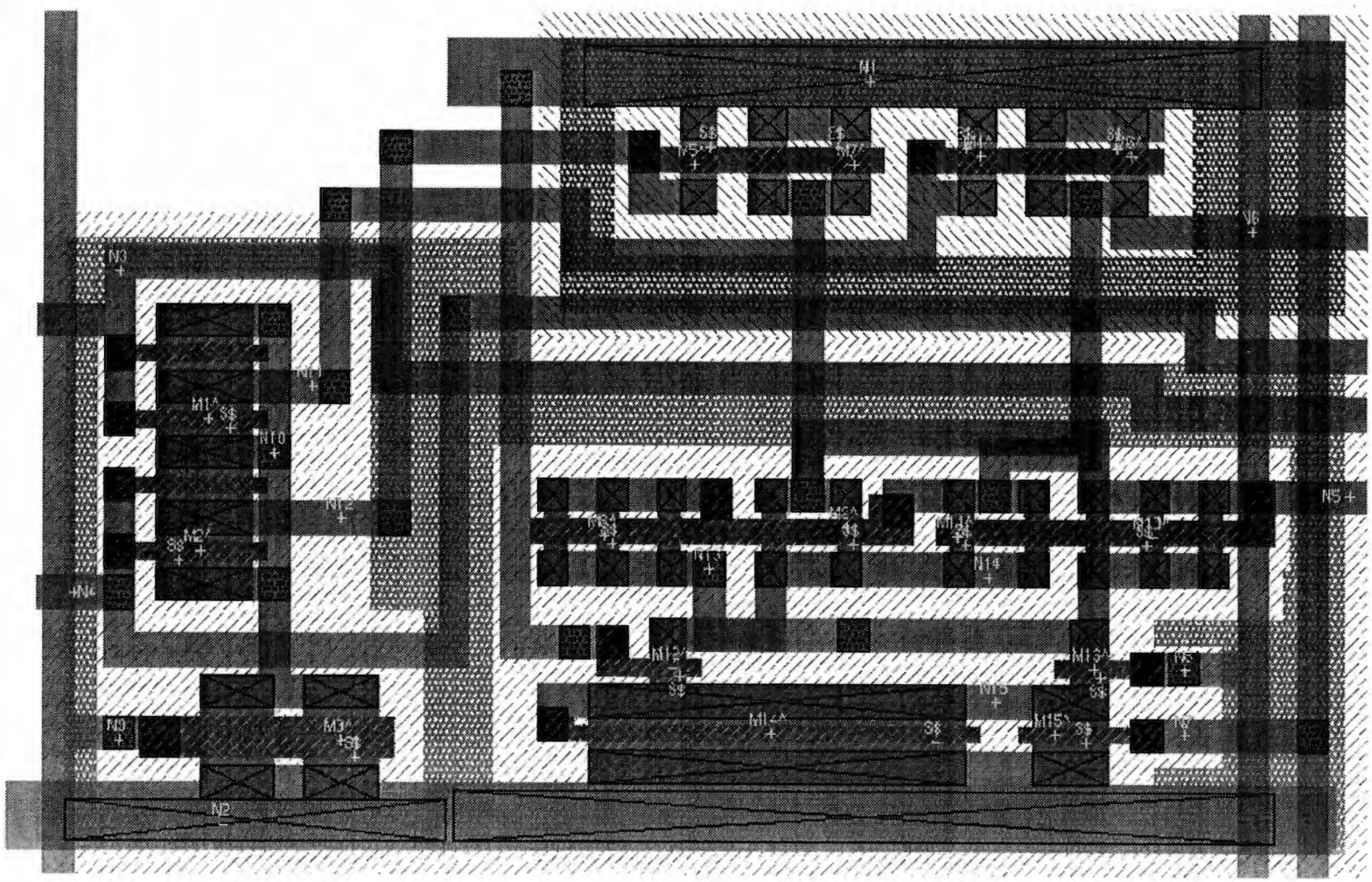


Figure 4-13. Integrated circuit layout plot of the regenerative latch.

effects. The regenerative latch occupies a silicon area of 51 μm x 92 μm and dissipates 1.1 mW from a single 5 V supply.

4.3 Comparator Channel Design, Layout, and Simulation

Since the MSB and OSB comparator channels are essentially identical with the exception of the reference selection network in the OSB channel, the layout and simulation of only the MSB comparator channel is presented. One of the main objectives in the comparator channel simulation process is to evaluate the offset correction performance of the comparator channel and to verify correct operation with a given set of timing conditions. In a SPICE simulation, all transistors are assumed identical for a given set of bias conditions, and therefore random offset effects associated with circuit design is generally not modeled or covered in the simulation. Since the comparator channel has zero systematic offset error and random offset effects are not modeled, a unique challenge exists to evaluate the offset correction functionality and performance of the comparator channel with SPICE simulations.

The anticipated residual input-referred comparator offset voltage after calibration has been presented in Chapter 3. However, evaluation of the offset correction process and performance of the calibration technique applied to the comparator channel is fundamental. This was accomplished with SPICE simulations by artificially inserting offset voltage generators into the comparator channel and corresponding simulation file. A schematic diagram illustrating the implementation of offset voltage generators to emulate random offset effects is shown in Figure 4-14. In Figure 4-14, the voltage source

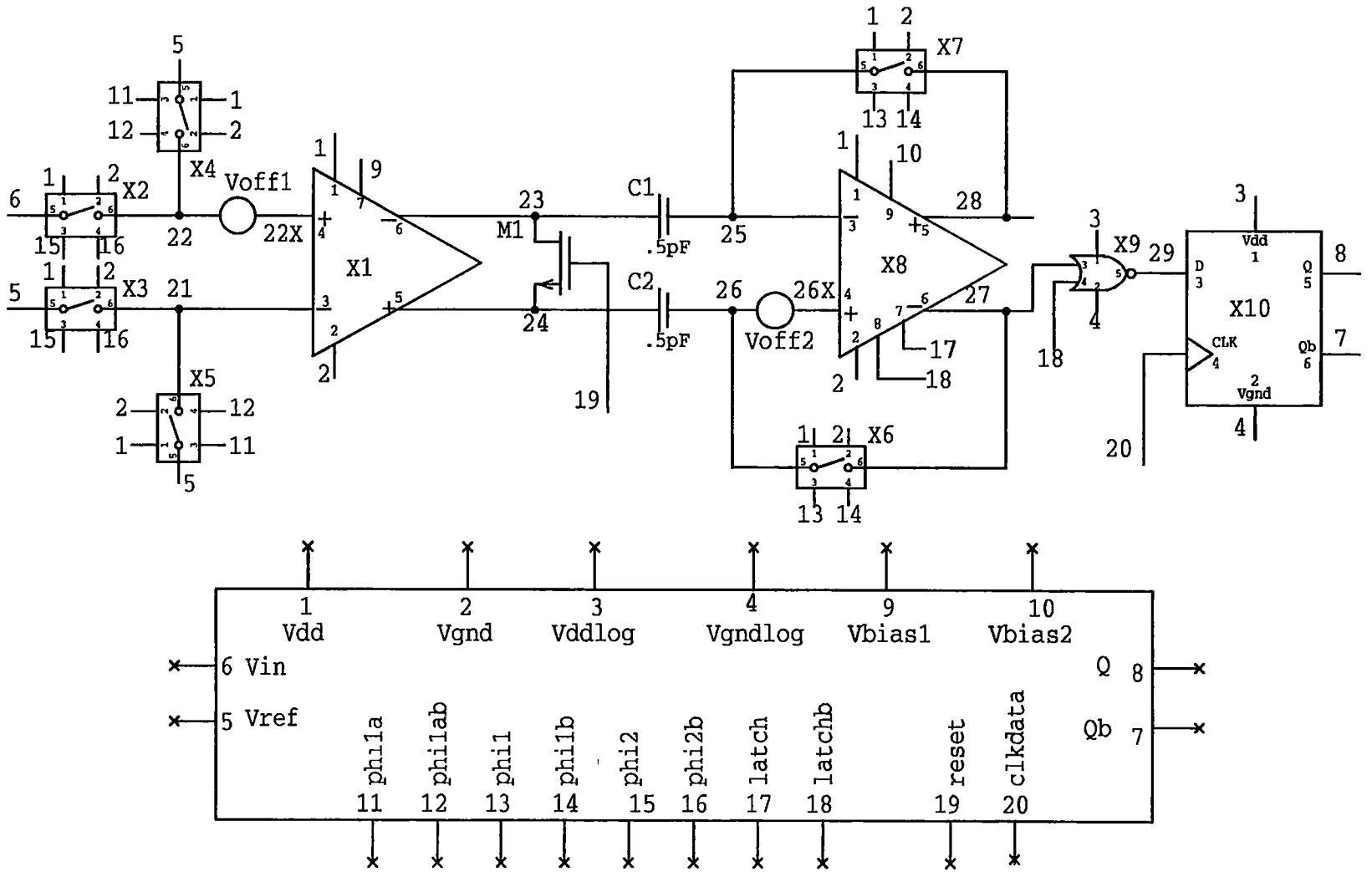


Figure 4-14. Schematic diagram of the MSB comparator channel with offset voltage generators.

V_{off1} represents the uncorrected offset voltage of the preamplifier while the voltage source V_{off2} emulates the uncalibrated offset voltage of the latch circuitry The differential mismatch in charge injection of CMOS switches represented by *X6* and *X7* are not modeled in this simulation due to the absence of detailed experimental data and characterization on the charge injection mismatch between adjacent pairs of CMOS transistors. Differential charge injection mismatch is a complicated process that is a function of a number of parameters such as device area, channel length, gate voltage slew rate, carrier mobility, and input and output impedances [31, 32]. The offset correction architecture should be robust against charge injection effects due to the implementation of a differential topology combined with the utilization of CMOS transmission gates as switches.

Based upon the circuit in Figure 4-14, SPICE simulations were performed to evaluate the offset correction performance of the comparator channel. Figures 4-15 and 4-16 show simulations results for a comparator channel conversion with a ±1 mV input signal (relative to the reference voltage) and 5 mV offset voltage generators for V_{off1} and V_{off2}. Figures 4-15 and 4-16 are results from the same simulation except that the bottom set of traces in Figure 4-16 show the timing information of the offset correction process. Figure 4-17 illustrates the comparator's overdrive recovery response. Notice how the preamplifier's outputs quickly recover back to the baseline to begin the OOS auto-zero process The simulations shown in Figures 4-15, 4-16, and 4-17 verified the basic functionality of the comparator offset correction technique and overdrive recovery process. Finally, a simulation was performed to determine the limitations of the offset

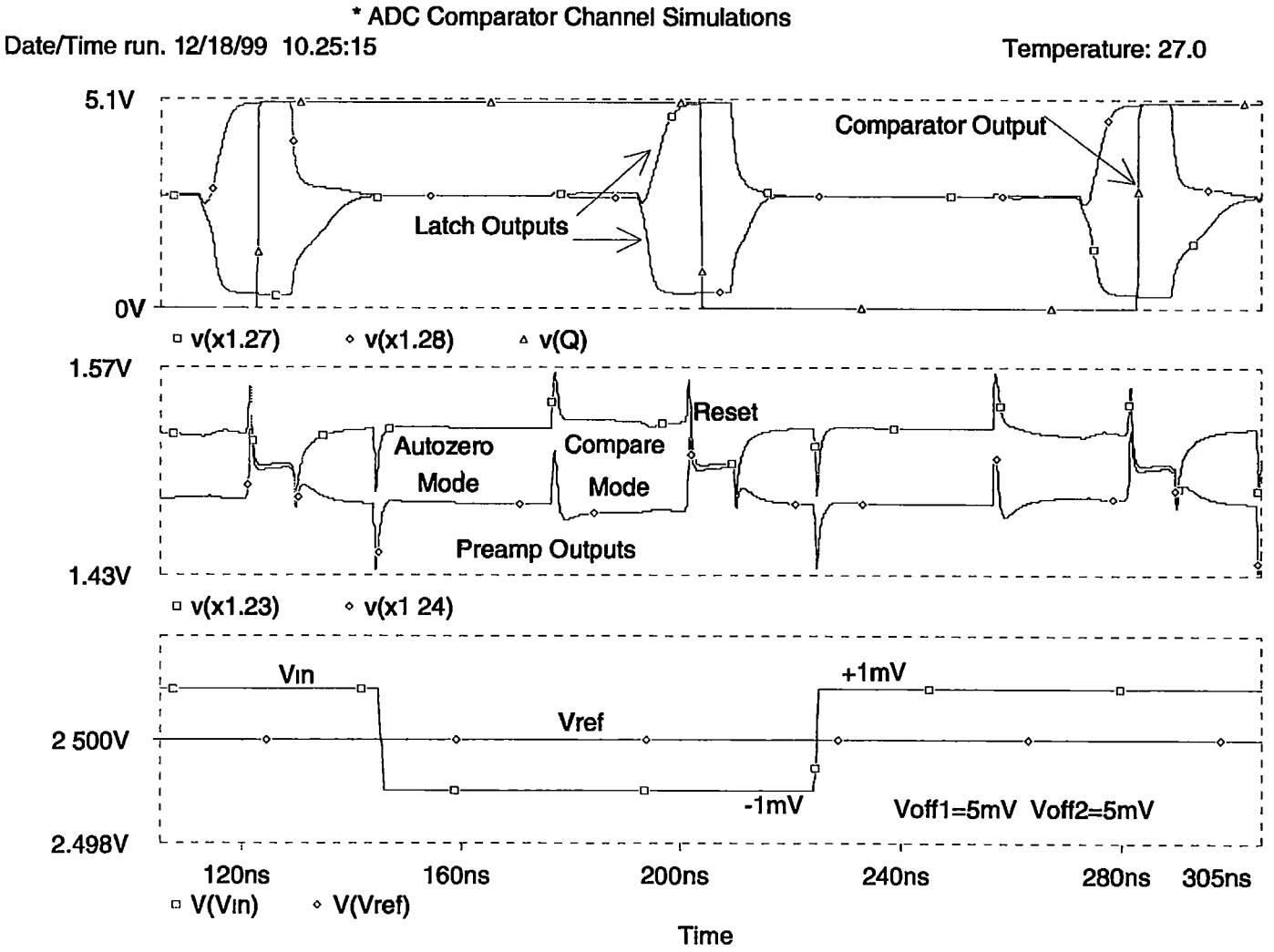


Figure 4-15. Transient response of comparator channel with 1 mV input overdrive and 5 mV offsets.

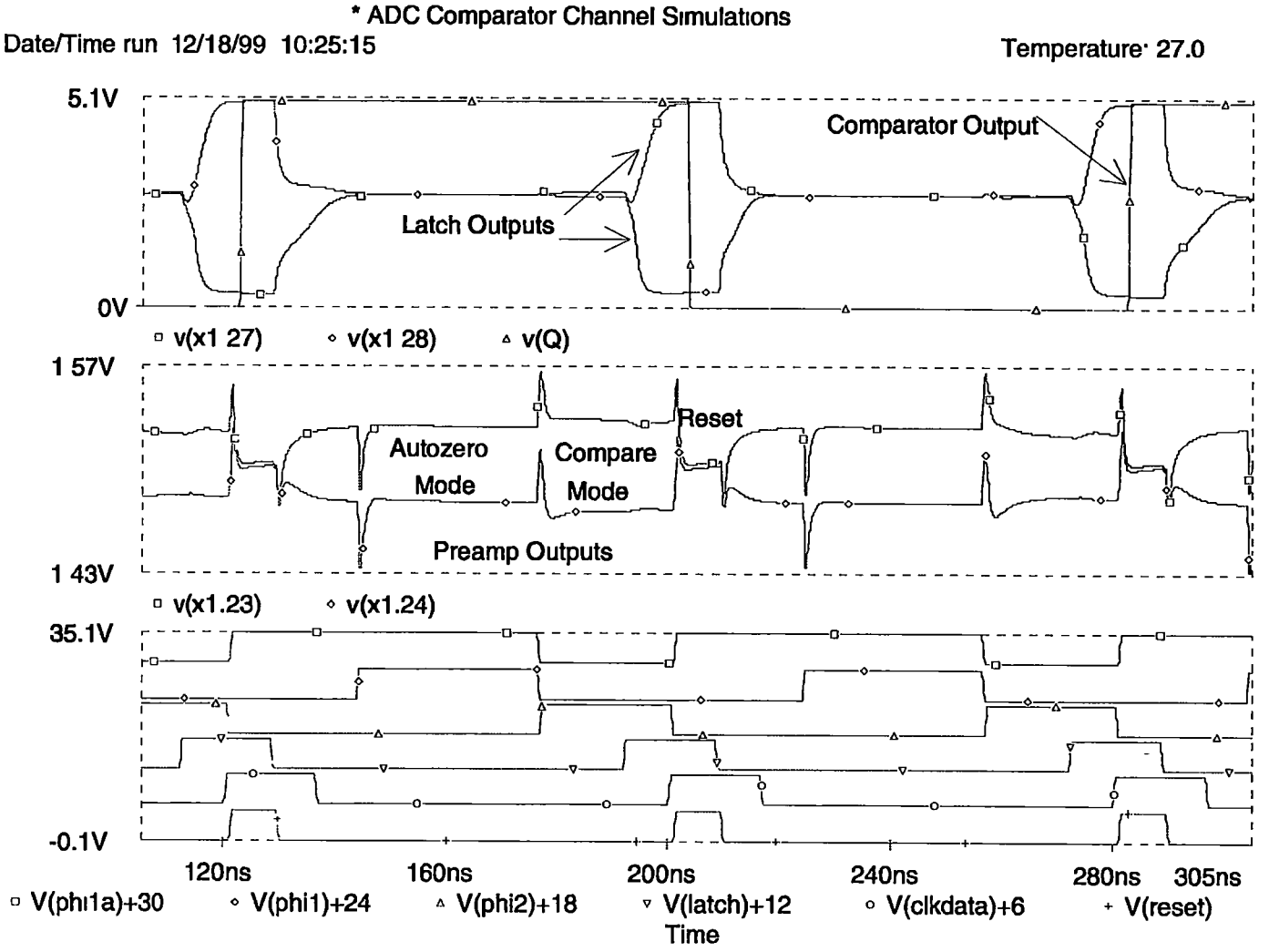


Figure 4-16. Transient response of comparator channel showing comparator control waveforms.

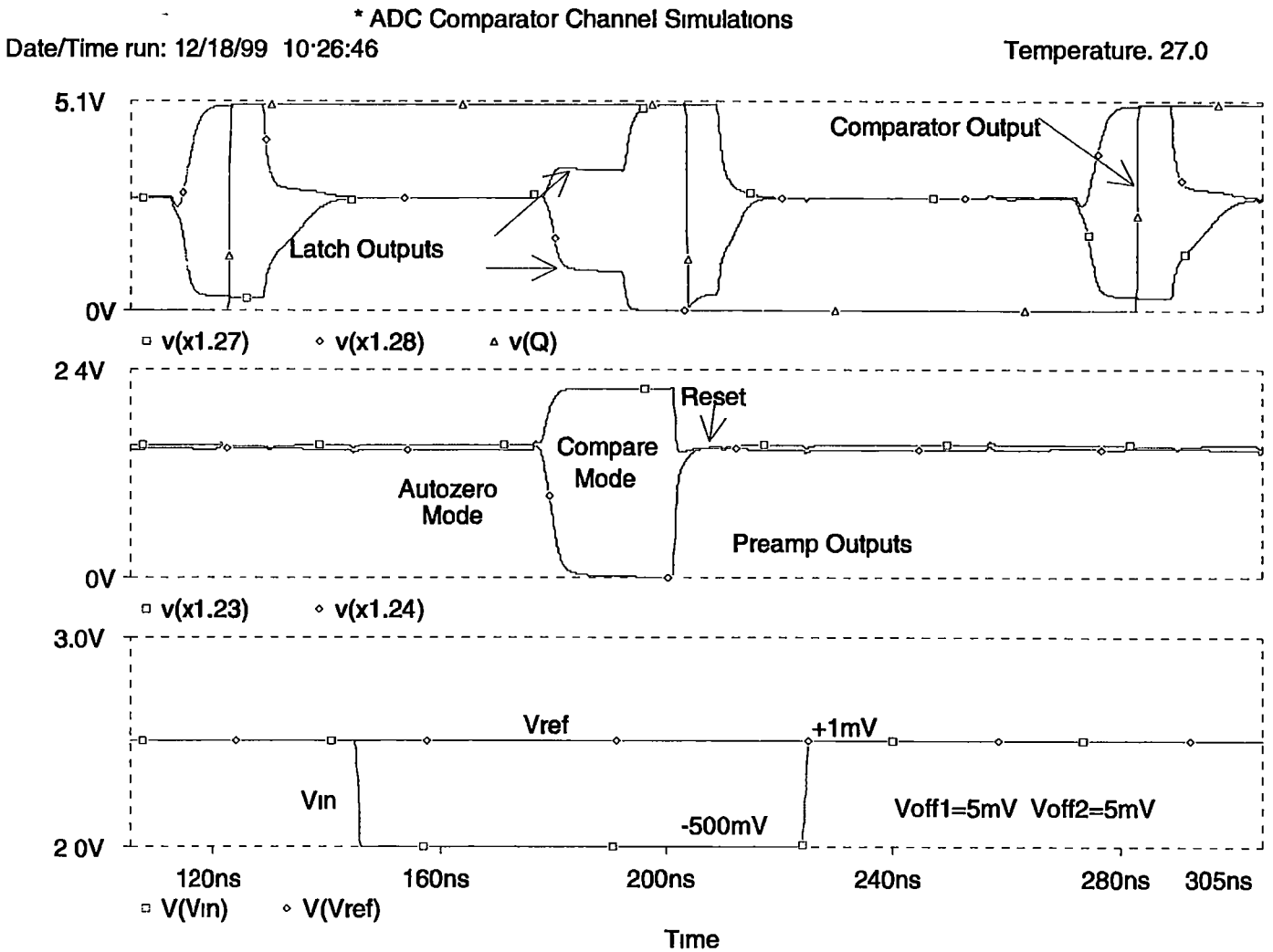


Figure 4-17. Transient response of comparator channel showing overdrive recovery performance.

correction process of the comparator channel. Figure 4-18 shows simulations results for a comparator channel conversion with a ±1 mV input signal (relative to the reference voltage) and 50 mV offset voltage generators for V_{off1} and V_{off2}. The simulated offset correction performance of the comparator channel under these conditions is very impressive. The comparator achieves a ±1 mV sensitivity even with offset voltage generators as large as 50 mV. All possible polarity combinations for V_{off1} and V_{off2} were simulated and the comparator still achieved the ±1 mV resolution. Based upon these simulation results, the comparator channel design should achieve the resolution and offset correction performance required for this 6-bit ADC application.

The integrated circuit layout plot of the MSB comparator channel is shown in Figure 4-19. Special attention was given to the layout process to develop a comparator channel that could be replicated to keep all common interconnects as short as possible while still making efficient use of silicon area. The MSB comparator channel occupies a silicon area of 51 µm x 586 µm and dissipates 2.6 mW from a single 5 V supply.

4.4 Reference Generation Design, Layout, and Simulation

A resistive ladder was used to create the necessary reference voltages for the comparators of the ADC. Based upon the linearity analysis of the reference generation circuitry presented in Chapter 3, a resistor matching of 1% is required. Resistors implemented in an integrated circuit typically have very poor absolute accuracy, but the relative accuracy or matching of resistors can be quite good. The implementation of polysilicon resistors were used in the reference generation circuitry. Polysilicon resistors

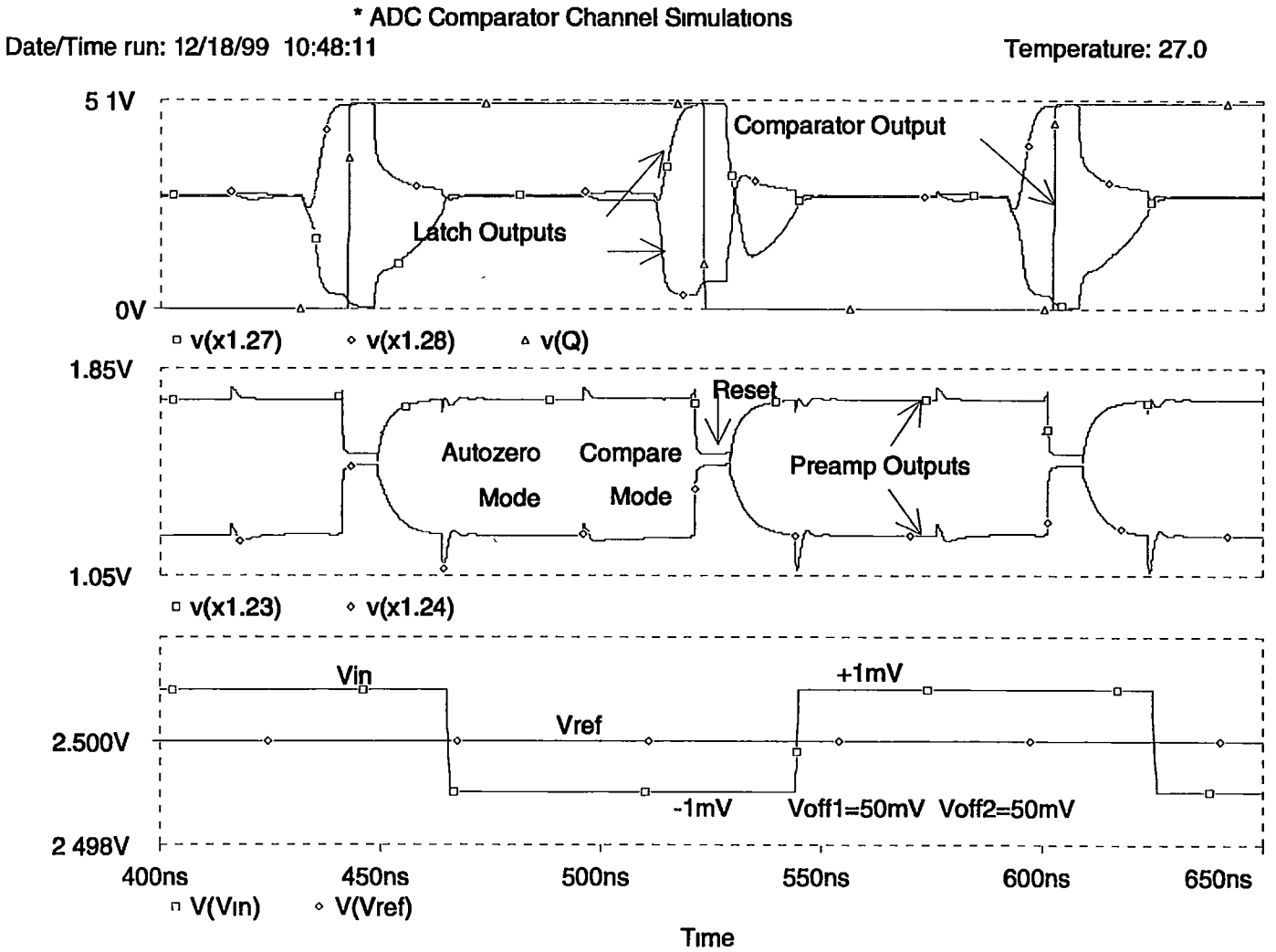


Figure 4-18. Transient response of comparator channel with 1 mV input overdrive and 50 mV offsets.

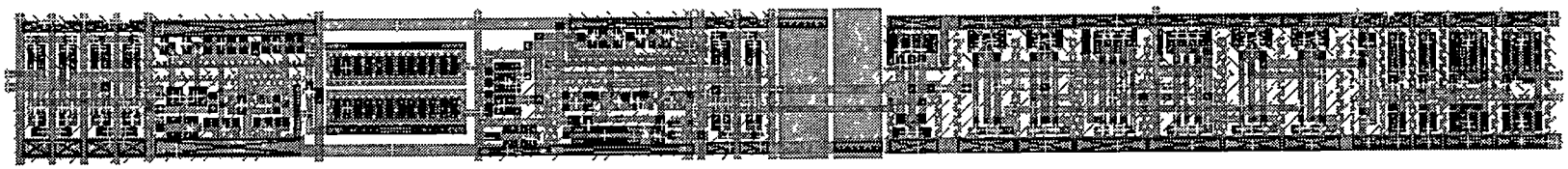


Figure 4-19. Integrated circuit layout plot of MSB comparator channel.

have very good matching characteristics and also exhibit excellent voltage and temperature coefficients. The selection of the size of the unit resistor cell replicated to create the resistive ladder was complicated by the absence of experimental data on the matching of polysilicon resistors in CMOS processes. As a result, the size or area of the resistor unit cell was chosen based upon other ADC designs reported in the literature [14]. The layout of the resistive ladder was folded once at its midpoint to reduce process gradients and to facilitate the connection of two reference voltages that are required for each OSB comparator channel. The ladder consists of 64 polysilicon resistors each with a width of 12.5 μm and length of 30 μm. With a sheet resistivity of about 25 Ω/□ for the polysilicon material, the unit resistor was about 60 Ω which resulted in an overall ladder impedance of 3.8 kΩ. A partial integrated circuit layout plot of the reference generation network is shown in Figure 4-20. The complete reference generation circuitry occupies a silicon area of 1578 μm x 72 μm and dissipates 0.4 mW from a reference voltage of 1.275 V.

4.5 ADC Prototype Chip Design, Layout, and Simulation

The ADC was developed based upon the integration of the major sections presented in Chapter 3. Each major section of the ADC was independently verified after layout for correct functionality and performance As a result, the integration of the mixed-signal system was a straight-forward process.

SPICE simulations of the entire 6-bit ADC were performed to verify correct integrated circuit layout, functionality, and performance. Simulation of a mixed-signal

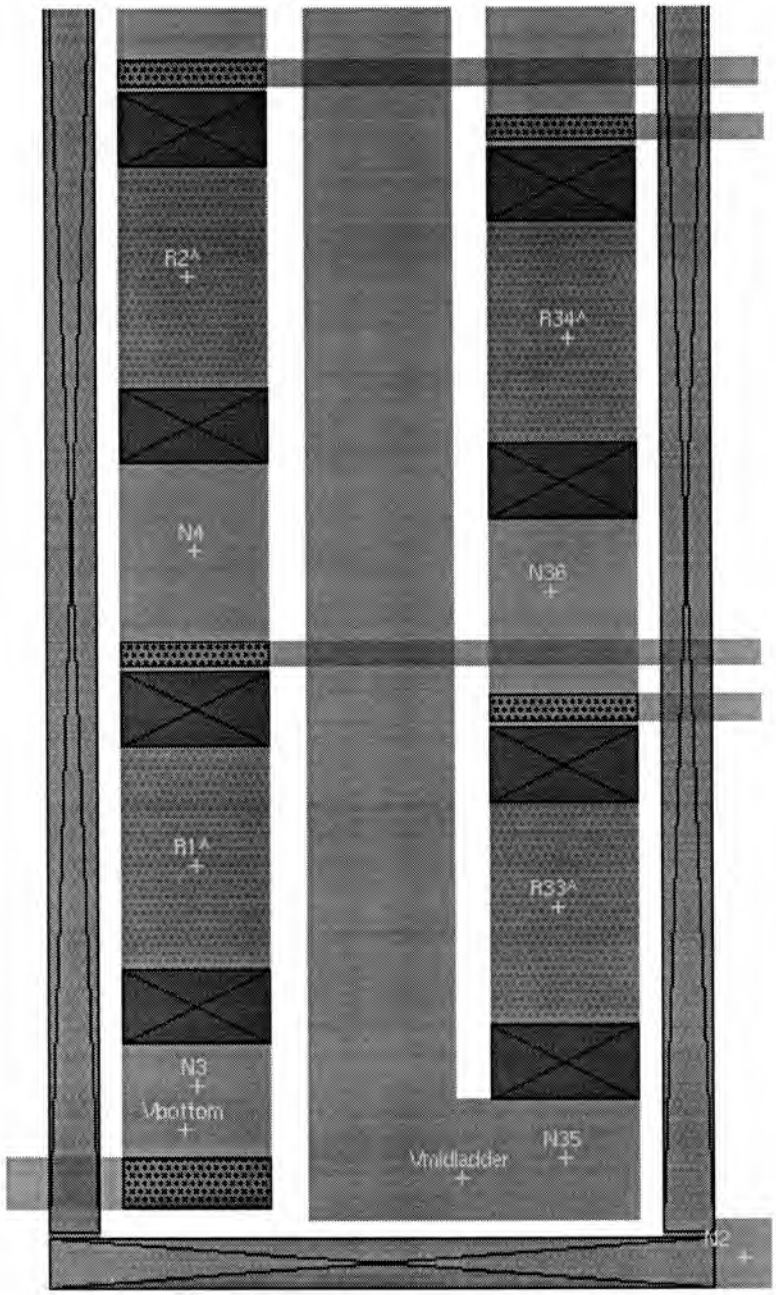


Figure 4-20. Partial integrated circuit layout of the resistive divider network.

system; such as an ADC, poses interesting challenges it terms of simulation efficiency and interpretation of results. A unique simulation technique was used to reduce the enormous amount of information and output data to an output data format that could easily be interpreted to verify correct ADC functionality.

The simulation methodology implemented to evaluate the ADC is a unique but simple process. The SPICE simulation file was created to set-up the ADC to run at a conversion rate of 15.625 MHz that resulted in synchronous ADC output data available every 80 ns. Thus, a synchronous and periodic conversion rate was achieved. Commands were written in the spice simulation file, to periodically record the voltages of all relevant waveforms required to verify correct ADC functionality and performance. As a result, a tabular text file was created which contained, for all conversions simulated, the analog input of the ADC and the corresponding output code that was available 80 ns later This SPICE simulation methodology allowed quick verification of the ADC functionality for all conversions simulated. An abbreviated listing of the simulation output file created is shown in Figure 4-21. If this technique had not been implemented, then an enormous amount of time would have been spent viewing and studying the ADC simulation results with a post-graphics display program.

Correct functionality of the ADC for all possible output codes was verified with SPICE simulations. Extensive ADC simulations revealed that switching transients were generated in the reference ladder when the reference voltages for the OSB comparators were changed. These transients were most prominent near the middle of the resistor ladder and affected the performance of the OSB comparators utilizing reference voltages

```
*                adc          simulations
******           transient    analysis    tnom=      25 temp=      25
******
m1_vin           =          2 50E+00 from=     1.24E-07 to=     1.25E-07
m1_vout0         =          5.00E+00 from=     1.62E-07 to=     1.63E-07
m1_vout1         =          -3 10E-07 from=    1.62E-07 to=     1 63E-07
m1_vout2         =          -3 07E-07 from=    1.62E-07 to=     1 63E-07
m1_vout3         =          -2.99E-07 from=    1.62E-07 to=     1 63E-07
m1_vout4         =          -3.00E-07 from=    1.62E-07 to=     1 63E-07
m1_vout5         =          -2.97E-07 from=    1.62E-07 to=     1 63E-07
m1_voflow        =          -2.89E-07 from=    1.62E-07 to=     1 63E-07
m2_vin           =          2.52E+00 from=     1.88E-07 to=     1.89E-07
m2_vout0         =          -3.06E-07 from=    2.26E-07 to=     2 27E-07
m2_vout1         =          5.00E+00 from=     2.26E-07 to=     2.27E-07
m2_vout2         =          -3.07E-07 from=    2.26E-07 to=     2 27E-07
m2_vout3         =          -2.99E-07 from=    2.26E-07 to=     2 27E-07
m2_vout4         =          -3 00E-07 from=    2 26E-07 to=     2.27E-07
m2_vout5         =          -2 97E-07 from=    2.26E-07 to=     2 27E-07
m2_voflow        =          -2.89E-07 from=    2.26E-07 to=     2.27E-07
m3_vin           =          2 54E+00 from=     2 52E-07 to=     2.53E-07
m3_vout0         =          5.00E+00 from=     2.90E-07 to=     2.91E-07
m3_vout1         =          5.00E+00 from=     2.90E-07 to=     2.91E-07
m3_vout2         =          -3.07E-07 from=    2 90E-07 to=     2 91E-07
m3_vout3         =          -2 99E-07 from=    2.90E-07 to=     2 91E-07
m3_vout4         =          -3.00E-07 from=    2.90E-07 to=     2.91E-07
m3_vout5         =          -2.97E-07 from=    2.90E-07 to=     2 91E-07
m3_voflow        =          -2.90E-07 from=    2.90E-07 to=     2 91E-07
m4_vin           =          2.56E+00 from=     3.16E-07 to=     3 17E-07
m4_vout0         =          -3.06E-07 from=    3.54E-07 to=     3.55E-07
m4_vout1         =          -3.08E-07 from=    3.54E-07 to=     3 55E-07
m4_vout2         =          5 00E+00 from=     3.54E-07 to=     3 55E-07
m4_vout3         =          -2.99E-07 from=    3.54E-07 to=     3.55E-07
m4_vout4         =          -3.00E-07 from=    3.54E-07 to=     3 55E-07
m4_vout5         =          -2.97E-07 from=    3.54E-07 to=     3 55E-07
m4_voflow        =          -2.89E-07 from=    3.54E-07 to=     3 55E-07
m5_vin           =          2 58E+00 from=     3.80E-07 to=     3 81E-07
m5_vout0         =          5.00E+00 from=     4.18E-07 to=     4 19E-07
m5_vout1         =          -3.10E-07 from=    4.18E-07 to=     4 19E-07
m5_vout2         =          5.00E+00 from=     4 18E-07 to=     4 19E-07
m5_vout3         =          -2.99E-07 from=    4.18E-07 to=     4 19E-07
m5_vout4         =          -3.00E-07 from=    4 18E-07 to=     4.19E-07
m5_vout5         =          -2.97E-07 from=    4.18E-07 to=     4.19E-07
m5_voflow        =          -2.90E-07 from=    4.18E-07 to=     4 19E-07
```

Figure 4-21. Abbreviated listing of the ADC simulation output file.

in this region. The switching transients created in the reference generation circuitry were minimized to acceptable levels by placing three external bypass capacitors along the resistor ladder. Due to time constraints, this design modification was deemed an acceptable solution and no additional measures or precautions were taken.

A large mixed-signal system such as an ADC requires careful floor planning and often iteration between design, simulation, and layout. Significant effort was spent in achieving an optimal ADC layout. Most of this time was consumed in developing a comparator channel that could be replicated with efficient use of silicon area. The integrated circuit layout was preformed in a manner such that sensitive analog sections were isolated from the digital circuitry. Extensive substrate and well connections were implemented throughout the mixed-signal layout. All comparator channels and individual subcircuits were surrounded by guard rings to minimize noise and substrate coupling. To isolate and de-couple critical power supple lines from transient noise generated in various sections of the ADC design, the integrated circuit layout employed three different power supply systems. One power system was dedicated to the sensitive analog sections of the ADC. A second set of power and ground connections was committed to the semi-analog sections of the layout. Finally, a third power supply system was connected to the digital sections of the ADC. All power and ground buses were made very wide with redundant connectivity to reduce the equivalent series resistance of the metal traces. Also, multiple power and ground pins with separate bond wires to package pins were used to reduce the equivalent series inductance of the packaging for improved noise immunity.

The 6-bit ADC design dissipates 90 mW and occupies a silicon area of 1.97 mm x

1.13 mm in 0.8 μm CMOS technology. The integrated circuit layout of the ADC prototype chip is shown in Figure 4-22. The ADC prototype chip, which measures 2.37 mm x 1.87 mm, contains the complete 6-bit two-step flash ADC, along with an entirely separate comparator channel with digital control logic.

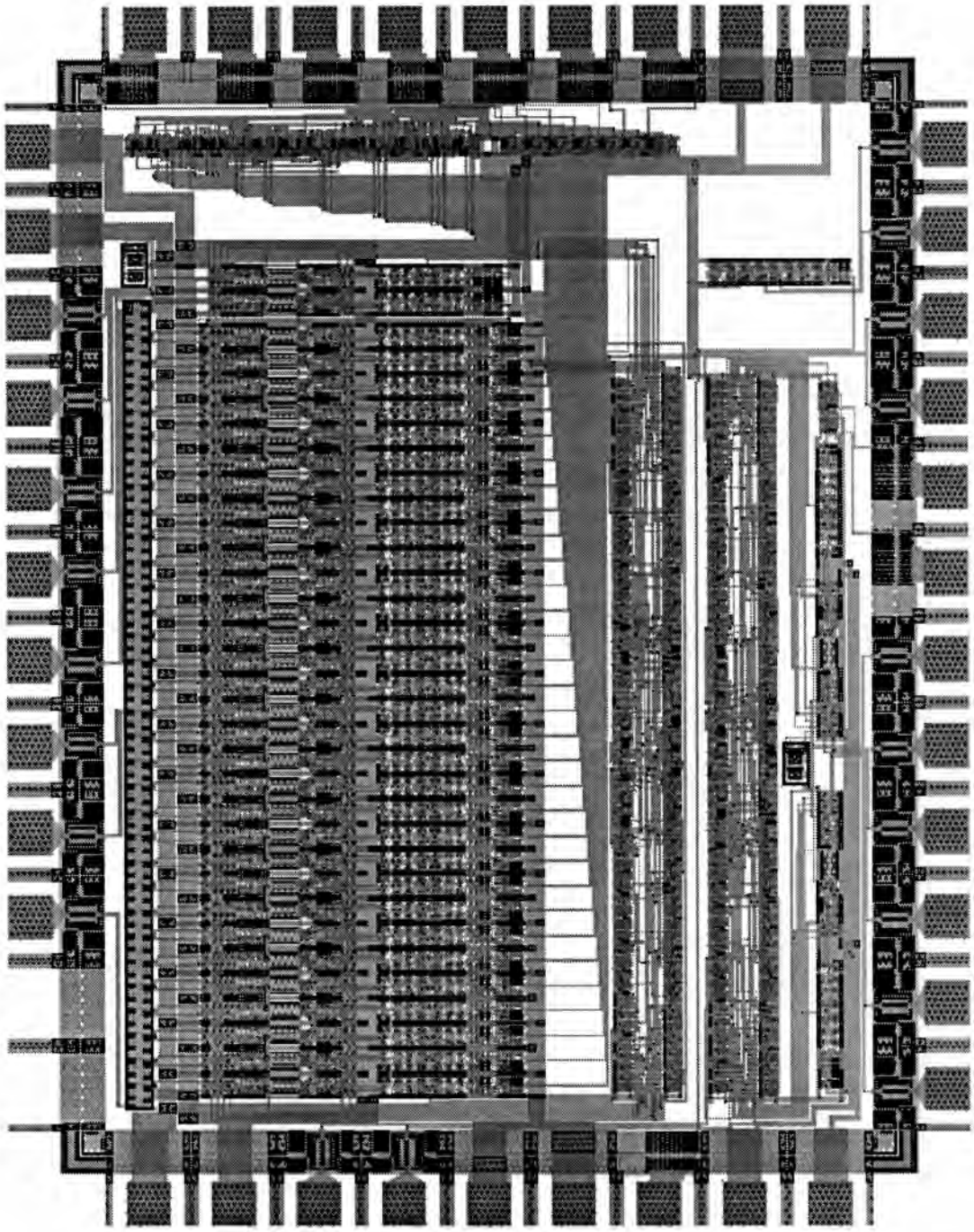


Figure 4-22. Integrated circuit layout plot of the ADC prototype chip.

Chapter 5

Experimental Results

5.1 ADC Evaluation and Characterization

5.1.1 ADC Test Methodology and Circuitry

Before testing and evaluating an ADC, a fundamental task is to determine what parameters of the ADC must be fully characterized because this affects the test methodology and circuitry. With most ADCs, gain and offset specifications are not the most critical parameters determining the ADC's performance in a specific application. Typically, these errors can be calibrated out either in software or hardware setup routines. The most important specifications of the ADC for this time measurement application are the differential non-linearity (DNL) and integral non-linearity (INL) performance of the converter because they represent irreducible errors that cannot be calibrated out at the system level. Many methods have been reported to test and characterize ADCs. Two of the common ADC test methodologies were adopted to evaluate the 6-bit CMOS two-step flash ADC.

The first test strategy implemented was a traditional method which involves the use of a digital voltmeter (DVM) to obtain high measurement accuracy with a static or slow varying input signal. This test method will be referred to as a dc sweep input test throughout the rest of this work. Linearity, gain, and offset errors can all be obtained and readily calculated from the knowledge of transition levels of the ADC transfer function. The dc sweep input test is performed with the converter free-running or continuously

converting and the output code of the ADC is recorded for various input signal voltage levels which span the entire dynamic input range of the converter. The recorded information of input signal and corresponding output code can be used to determine the transition levels that represent the ADC transfer function. This simple test methodology offers low complexity and provides good characterization of the ADC in the dc or slow varying amplitude domain.

The other test strategy implemented was to test the ADC as it would be used in the time measurement application. This test method involved a computer-based system with a data acquisition card and extensive support circuitry, which allows testing the ADC at full-speed with full-range dynamic inputs. Also, this computer-aided ADC characterization methodology provides tremendous flexibility since almost any test pattern or condition can be generated with the corresponding results recorded.

A block diagram of the experimental setup for testing the ADC by both test methodologies is shown in Figure 5-1. A CMOS clock oscillator is used to provide the 16 ns system clock for the ADC and external control logic. The control logic is required to provide synchronization and timing information between the data acquisition card of the computer and the test board. Two high-speed first-in-first-out memories (FIFOs) are used for data management and a high-speed 10-bit digital-to-analog converter (DAC) is used to create the dynamic analog input signal to the ADC. The input FIFO is used to store the input test pattern that is loaded by the computer via the data acquisition board. During the full-speed testing process, data is transferred from the input FIFO and presented to the DAC The DAC interprets these digital numbers and then generates the

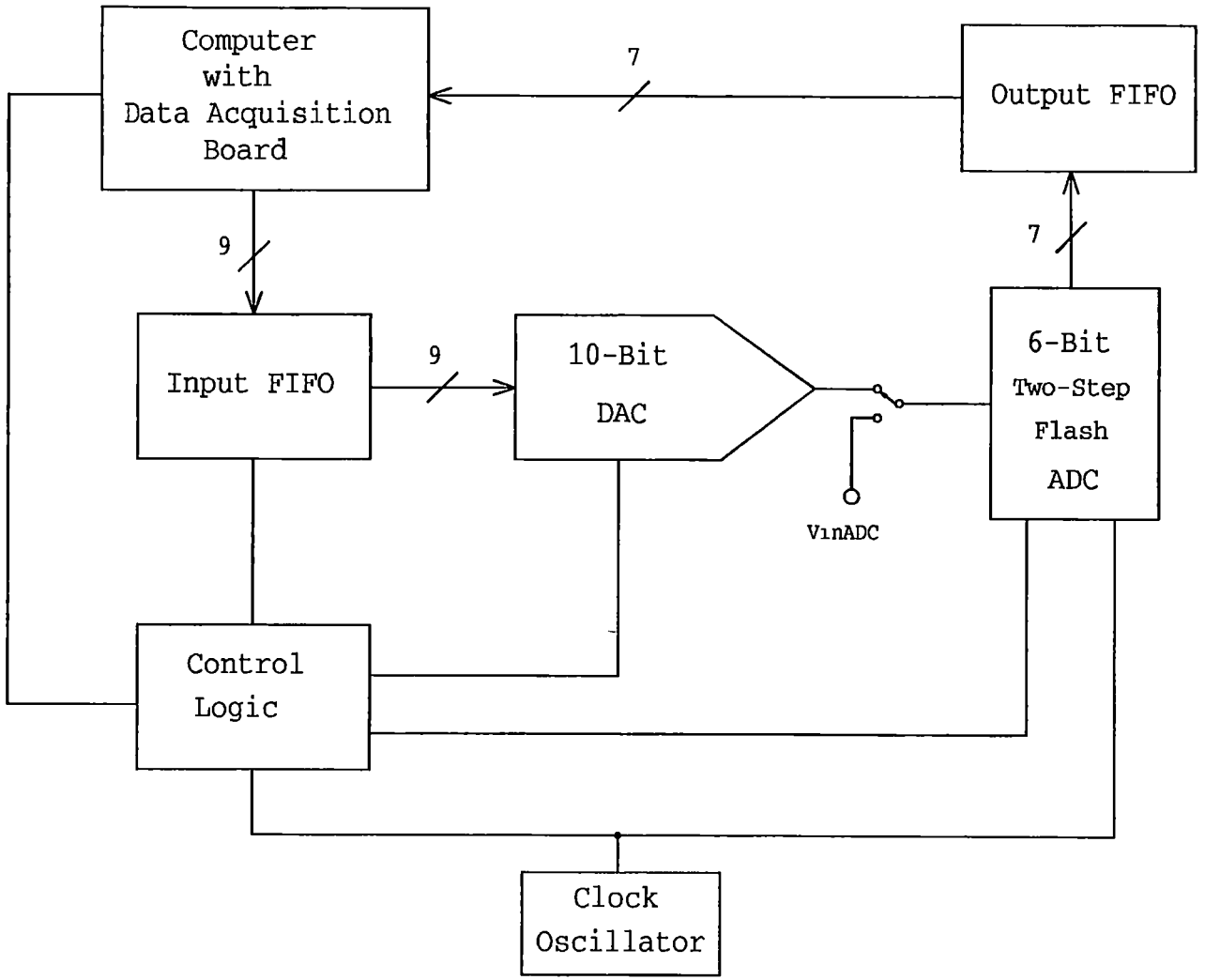


Figure 5-1. Block diagram of experimental setup for testing the ADC.

corresponding voltage levels to the ADC. The output FIFO is used to record the ADC output codes during the full-speed testing process. The data recorded by the output FIFO during testing is then read by the computer with the data acquisition board. The data can then be processed and analyzed by the computer to determine and characterize the performance of the ADC.

Only the most significant 9-bits of the 10-bit DAC are utilized due to data management constraints. Since only 9-bits of the 10-bit DAC are used, the normal non-linearity errors associated with the DAC are drastically reduced and the DAC should perform very well. Using the DAC in this configuration should provide clear separation between the errors of the ADC and errors that are normally present in the DAC. Therefore, to first order, the errors of the DAC are considered negligible when compared to the errors of the ADC. With the same reference voltage, the 9-bits of the DAC can determine the non-linearity errors of the 6-bit ADC to 1/8-bit or 2.5 mV precision, which is sufficient accuracy for this application.

A detailed schematic of the test circuitry developed to characterize the ADC by both test methodologies is shown in Figure 5-2. The test circuit is simple in concept but in reality is complicated by synchronization issues between the data acquisition card of the computer and the test board. Also, realization of the circuitry requires an enormous amount of connectivity due to several data paths present in the design. The mixed-signal circuit was constructed on a copper-clad board that served as a solid ground plane. Component placement was implemented in a manner to isolate analog and digital components when possible. Signal routing was performed to separate low-level analog

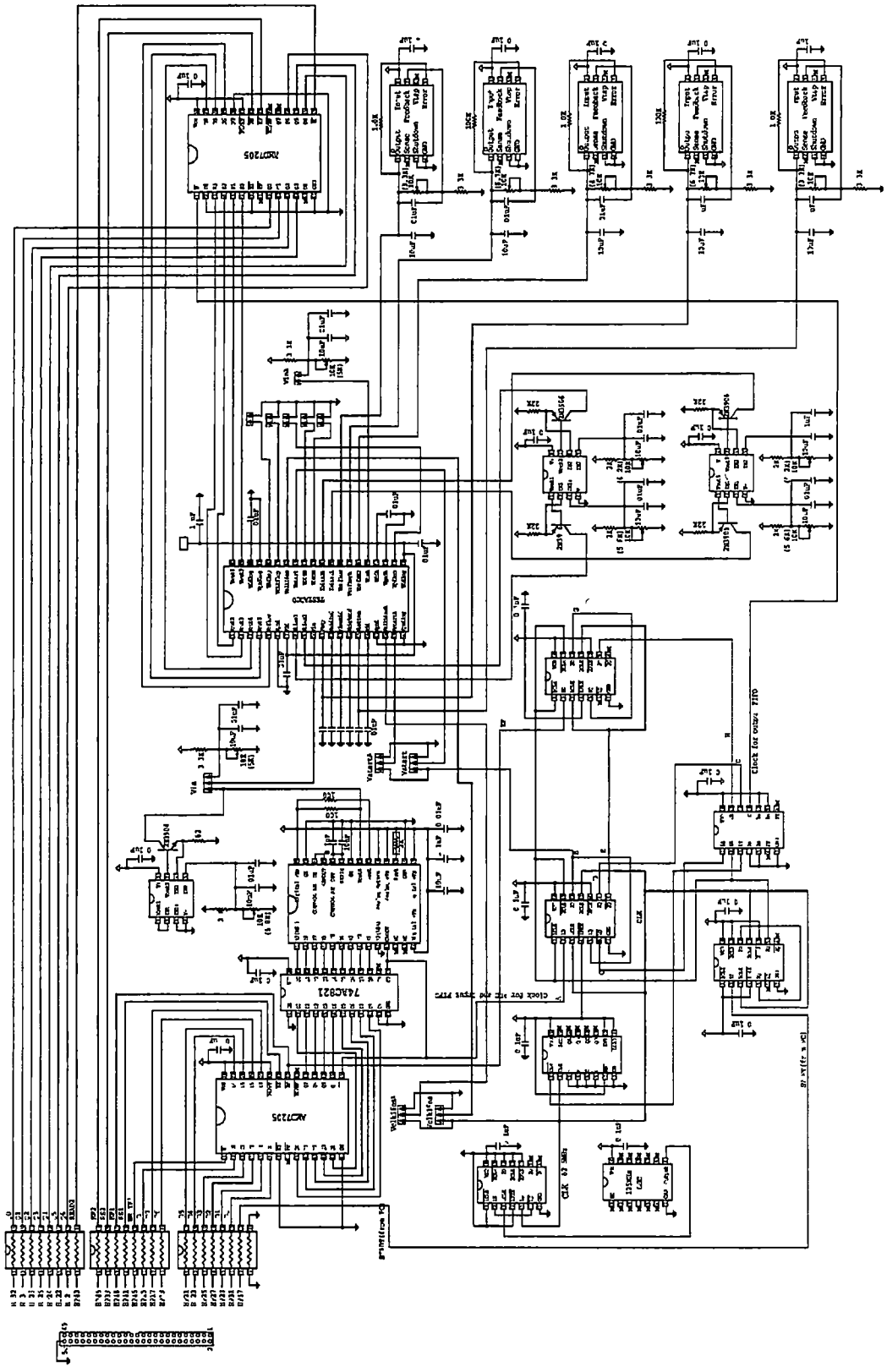


Figure 5-2. Schematic diagram of test circuitry to fully characterize the ADC.

input signals and high-level digital output or clock signals. Also, de-coupling capacitors were extensively used with tight connections between components power pins and ground. A photograph of the test board developed to characterize the ADC is shown in Figure 5-3. After extensive troubleshooting and verification of the test board functionality, evaluation and characterization of the ADC was performed.

5.1.2 DC Sweep Input Measurements

A dc sweep input test was the first type of test performed on all twenty-three ADC prototype chips. This test was performed by manually varying the input voltage to the ADC over the entire dynamic input range and recording the corresponding output code to determine the converter's transition levels. Results from these measurements indicated that the ADC design was entirely functional and demonstrated acceptable linearity performance for this dc sweep input test. Also, the converter satisfied the condition of no missing codes since every possible output code was represented in the ADC transfer function.

The measured and ideal transfer function of the ADC is shown in Figure 5-4 The two lines plotted in the figure are inseparable, which indicates good linearity characteristics of the converter. After analyzing the data of all twenty-three ADC prototype chips evaluated by the dc sweep input test, the worst-case deviation between an actual transition and ideal transition voltage was determined to be less than 4.6 mV. This impressive conclusion implies that the sum of corrected comparator offsets and reference generation errors were maintained less than ¼ LSB for all channels. Typical INL and

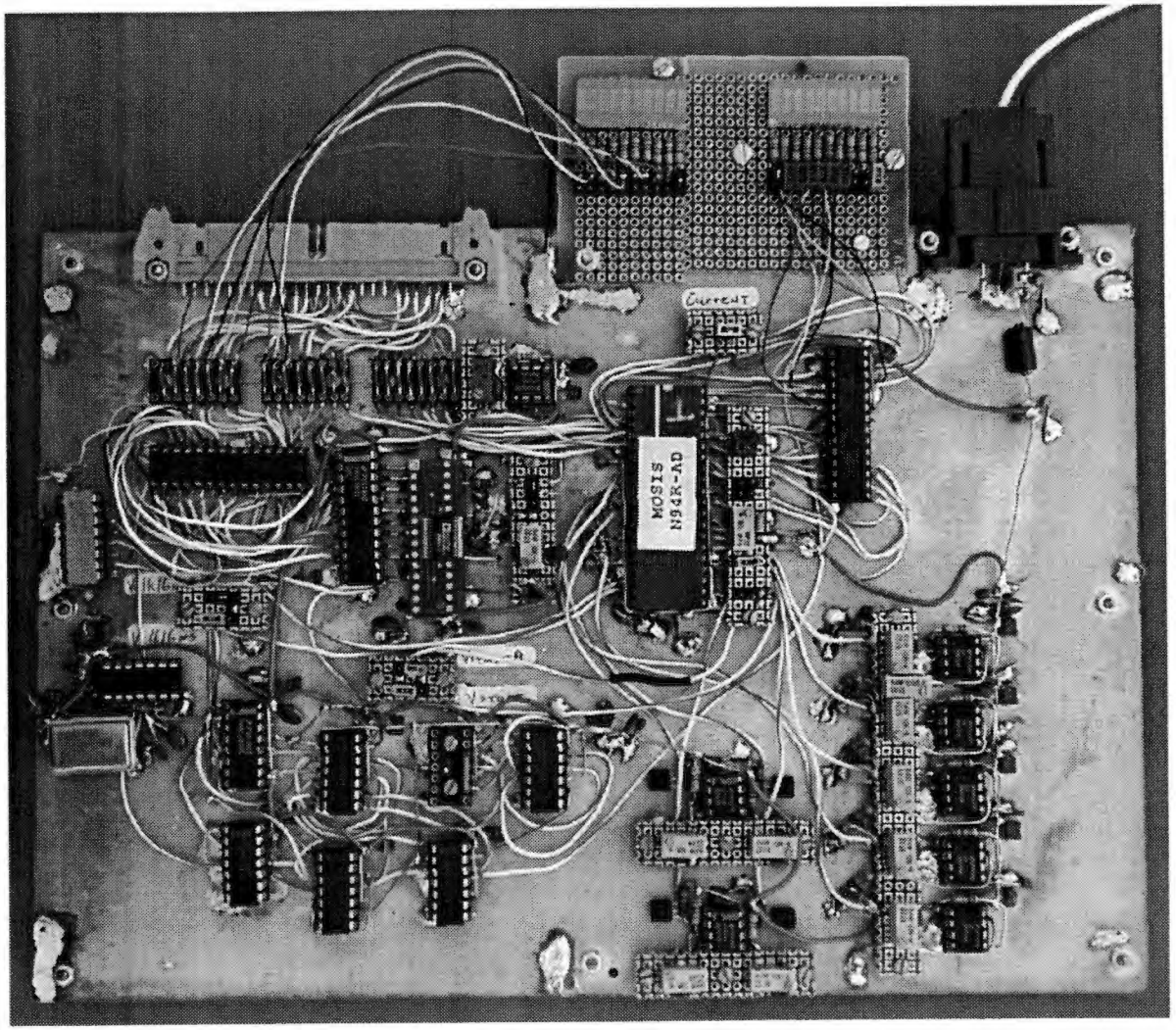


Figure 5-3. Photograph of test board developed to evaluate the ADC.

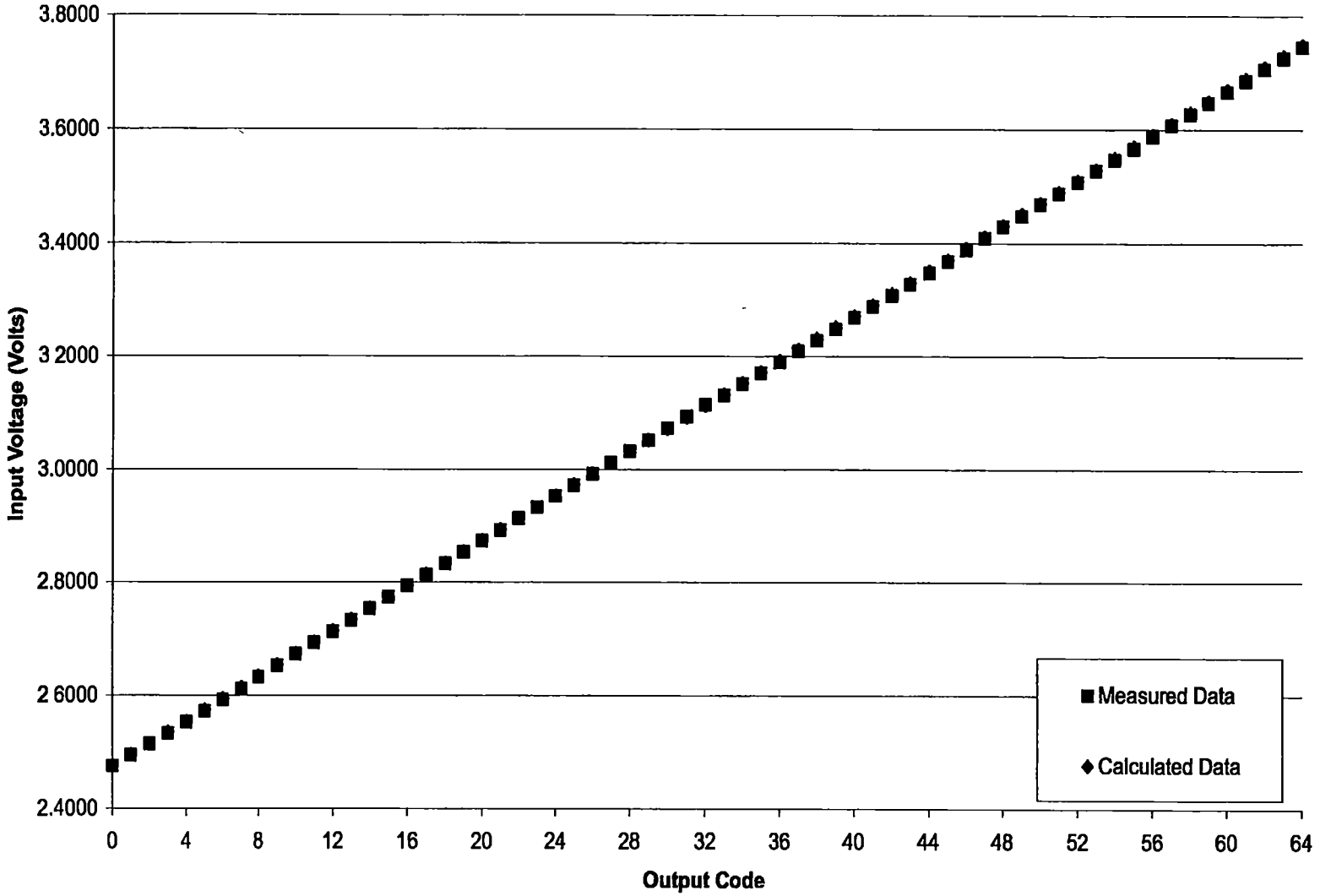


Figure 5-4. Typical measured versus ideal transfer function characteristics of the ADC.

DNL performance of the ADC ascertained by dc sweep input measurements are shown in Figure 5-5. Also, the INL and DNL performance for all chips evaluated by the dc sweep test method is illustrated in Figure 5-6 and Figure 5-7, respectively. Figures 5-6 and 5-7 show that the non-linearity errors of the ADC are maintained well below the required ±½ LSB specification. Also, the most severe linearity errors occur at the ADC output code transition of 31 to 32. Further investigation of these linearity errors revealed that these errors are the result of reference voltage generation errors at or near the middle point of the resistive divider.

The reference voltage errors are a direct result of resistor mismatch in the resistive divider and switching transients present in the reference ladder network. The resistive divider is used to create all the reference voltages to the comparators of the ADC Measurements on the three available taps of the reference ladder on all prototype chips indicate that the worst-case reference voltage error occurs at the middle tap of the ladder and is on average about 7 mV below the nominal value of 3.1125 V. From the limited reference voltage measurements performed, an average resistor matching of 1 1% was achieved in the reference generation network. Switching transients occur in the reference ladder when the reference voltages on the OSB comparators are switched or changed from the previous conversion. The decision of whether to change the reference voltage on the OSB comparators is based upon the output decision of the MSB comparator. When the ADC output code transitions from 31(011111) to 32 (100000), continuous switching of the reference voltages for the OSB comparators occurs because the output of the MSB comparator toggles between 0 and 1 during this transition region. These switching

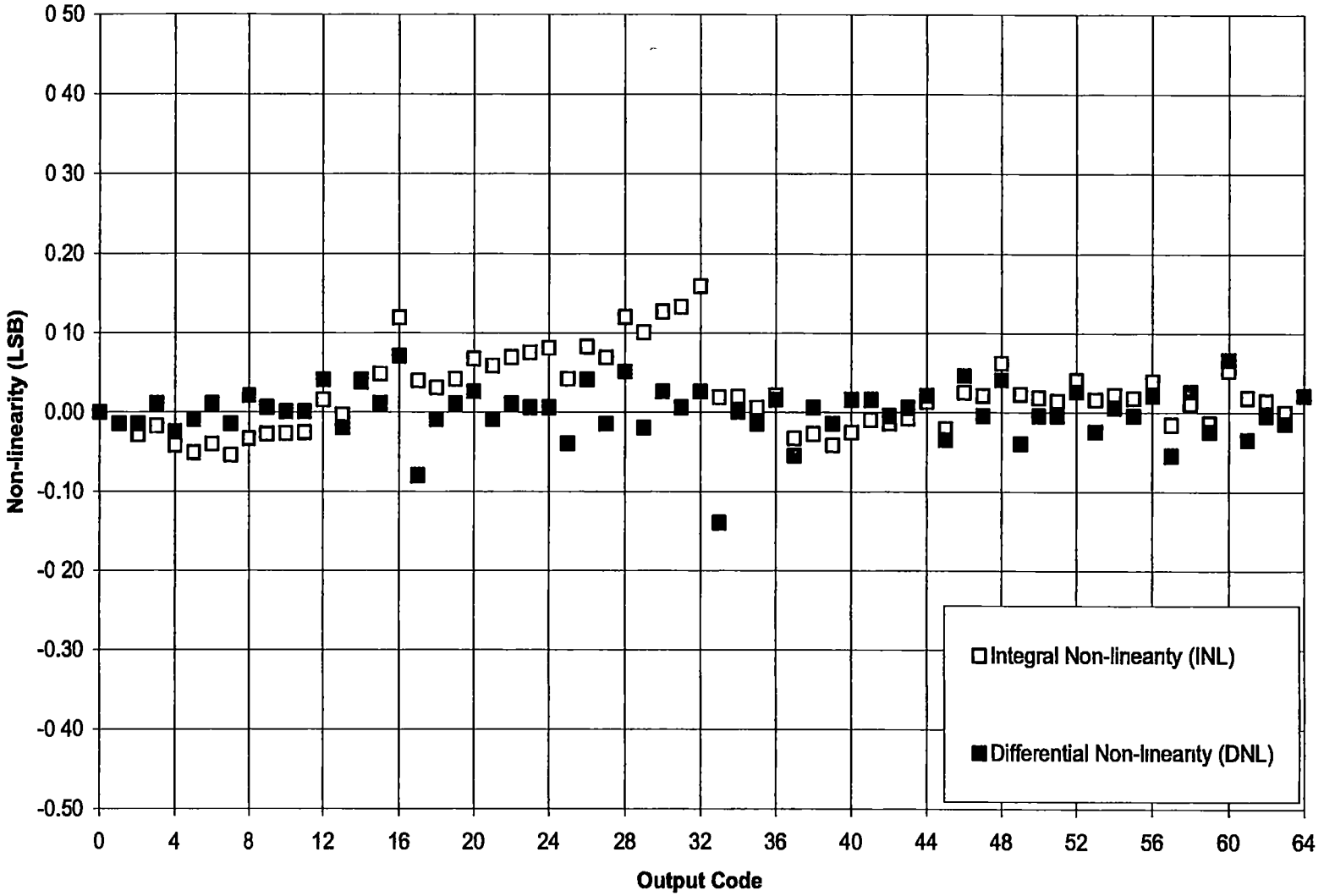


Figure 5-5. Typical ADC non-linearity performance from DC sweep input measurements.

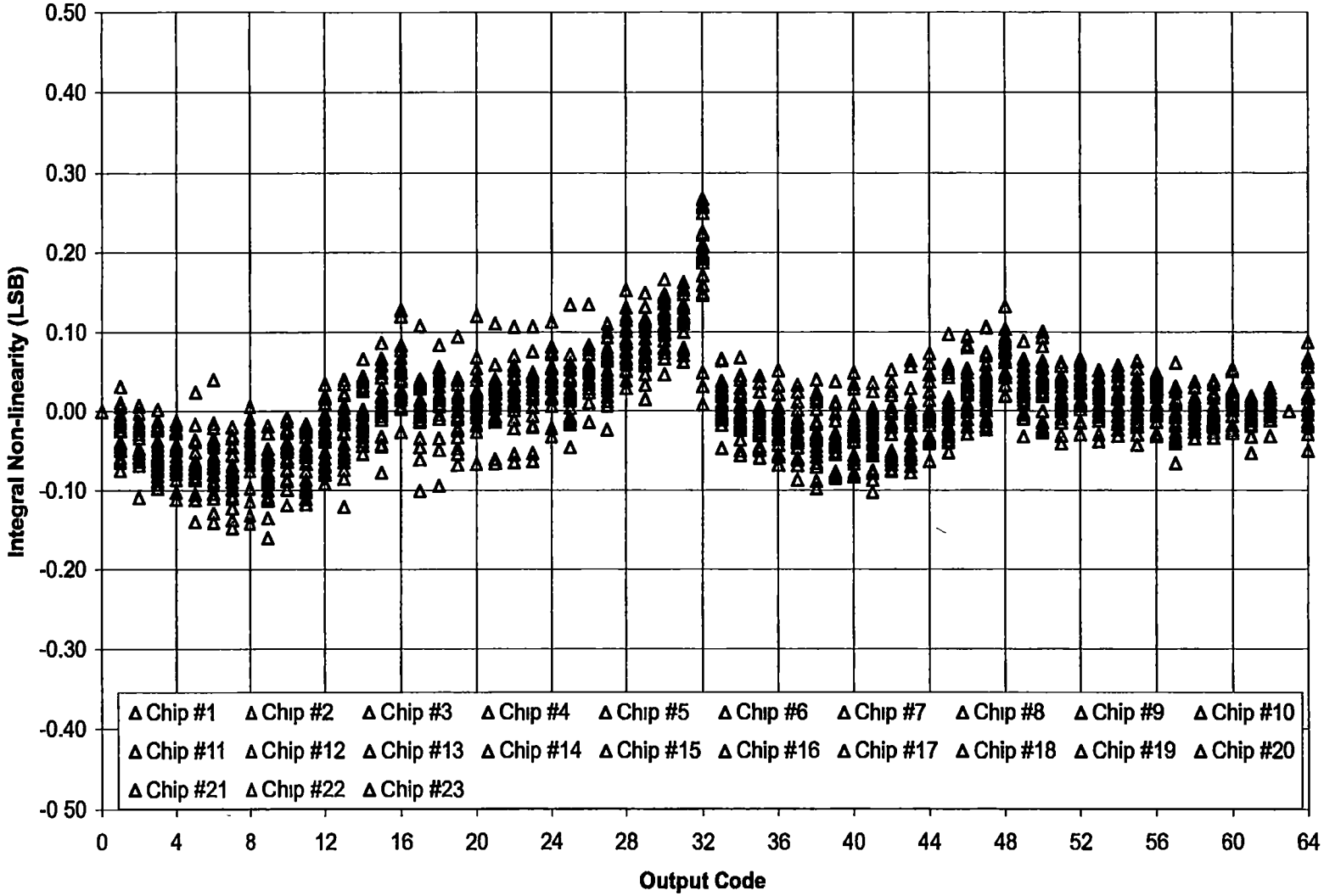


Figure 5-6. Integral non-linearity performance of all ADC chips from DC sweep input measurements.

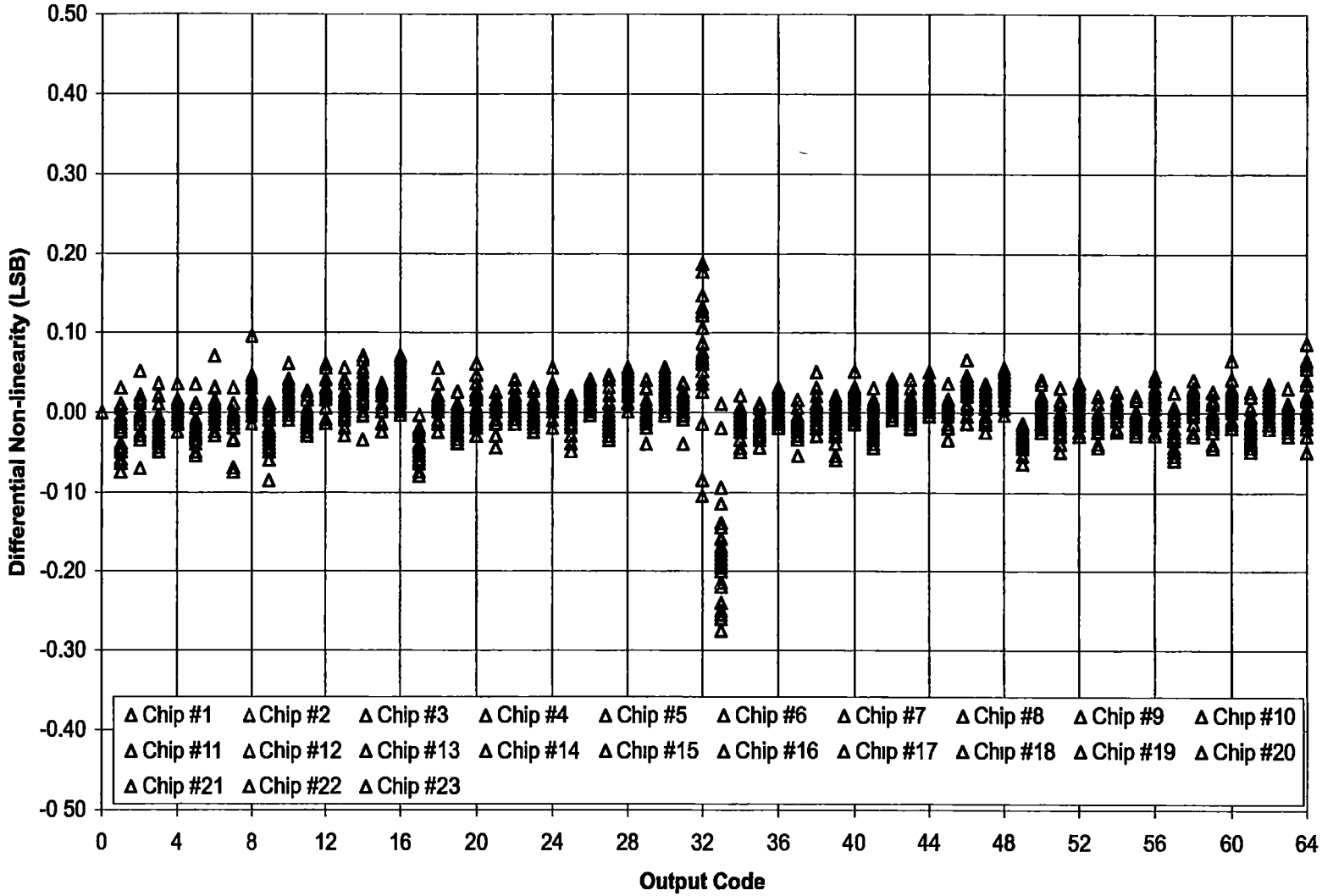


Figure 5-7. Differential non-linearity performance of all ADC chips from DC sweep input measurements.

transients are believed to be significant enough to cause reference voltage generation errors especially near the middle of the resistive ladder, which leads to non-linearity errors of the ADC at these transition regions.

5.1.3 Dynamic Code Density Measurements

The next test methodology performed on the ADC prototype chips was a dynamic code density test. This test method emulates the real application and actually evaluates the ADC as it would be used in the time measurement application The dynamic code density test is a computer-based test methodology of characterizing ADCs at full-speed and full dynamic range [38]. The code density test produces a histogram of the digital output codes of an ADC sampling a known input signal. The histogram or output code density is a record of the number of times every individual output code has occurred. Note that any output code density or histogram bin that is equal to zero corresponds to a missing code in the converter's transfer function. The statistical nature of the code density test gives a more accurate characterization of the converter compared to traditional tests in which each output code is only recorded once.

Although other information about an ADC can be obtained with this type of test, histograms are used more often in evaluating the DNL of the device. The code density test will be used here to only determine the DNL of the ADC. With a uniform random input signal applied to the converter, the number of counts in a particular bin is directly related to its bin width. Thus, the information accumulated in the histogram can be used to determine the DNL of the ADC. The DNL expressed as a fraction of LSB can be found

from the histogram by taking the number of counts in the *i-th* bin and dividing by the ideal number of counts in each bin, and then subtracting one LSB from the expression. The DNL expressed as a fraction of a LSB is given by

$$DNL(i) = \frac{N(i)}{N_B} - 1 \ , \tag{5-1}$$

where $N(i)$ is the measured number of counts in the *i-th* bin. Also, note that N_B is the ideal number of counts in each bin and can be calculated by

$$N_B = \frac{S}{2^N} \ , \tag{5-2}$$

where S is the total number of samples and N is the number of bits of the ADC.

The dynamic code density test described was performed on all of the ADC prototype chips. A random input test pattern for the code density test was generated by using the rand( ) function and a macro in the C programming language. Using this function, random numbers between 0 to 511 were generated and loaded into the input FIFO. The random numbers loaded into the FIFO were used so that the DAC could generate random input signal levels that spanned the entire input dynamic range of the ADC. The converted output codes of the ADC were recorded by the output FIFO. The codes were read from the output FIFO by the computer via the data acquisition board. These codes were then used to create a histogram of all ADC channels. This histogram was used to calculate the DNL characteristics of the ADC using Equations 5-1 and 5-2.

For the dynamic code density test methodology, a total of 320,000 random samples were taken which for the 6-bit ADC corresponds to a nominal value of 5,000 counts per bin or channel. Special attention was given to the random number generation

process to ensure that the random distribution of numbers produced was uniform enough so that the results from this test methodology could not be misinterpreted as ADC linearity errors. Figure 5-8 shows the linearity of the random data generated for the code density test measurements. The number of samples recorded was deemed sufficient since this number overcame any variation in the measurements due to noise or any other effects and a large increase in the number of samples taken produced essentially the same results. The DNL performance for all twenty-three ADC chips evaluated with the code density test is shown in Figure 5-9.

The data presented in Figure 5-9 shows that the DNL errors of the ADC are maintained well below the required ±½ LSB specification. Also, the most severe linearity errors occur at the ADC output code transitions near or at the middle of the output code region. Similar results were measured by the dc sweep input test methodology. Again, these linearity errors are believed to be the result of reference voltage generation errors which are a result of resistor mismatch in the resistive divider and switching transients present in the reference ladder network. The non-linearity errors are more prevalent with the code density test because of the full-speed dynamic test evaluation and the random input signal applied to the ADC. With a uniform random input signal applied to the ADC, all codes are equally probable and thus the output of the MSB comparator is equally probable. Therefore, the output of the MSB comparator constantly toggles between 0 and 1 during this test and non-negligible transients in the reference ladder network are produced. These switching transients are believed to be significant enough to cause reference voltage generation errors, especially for OSB comparators that utilize reference

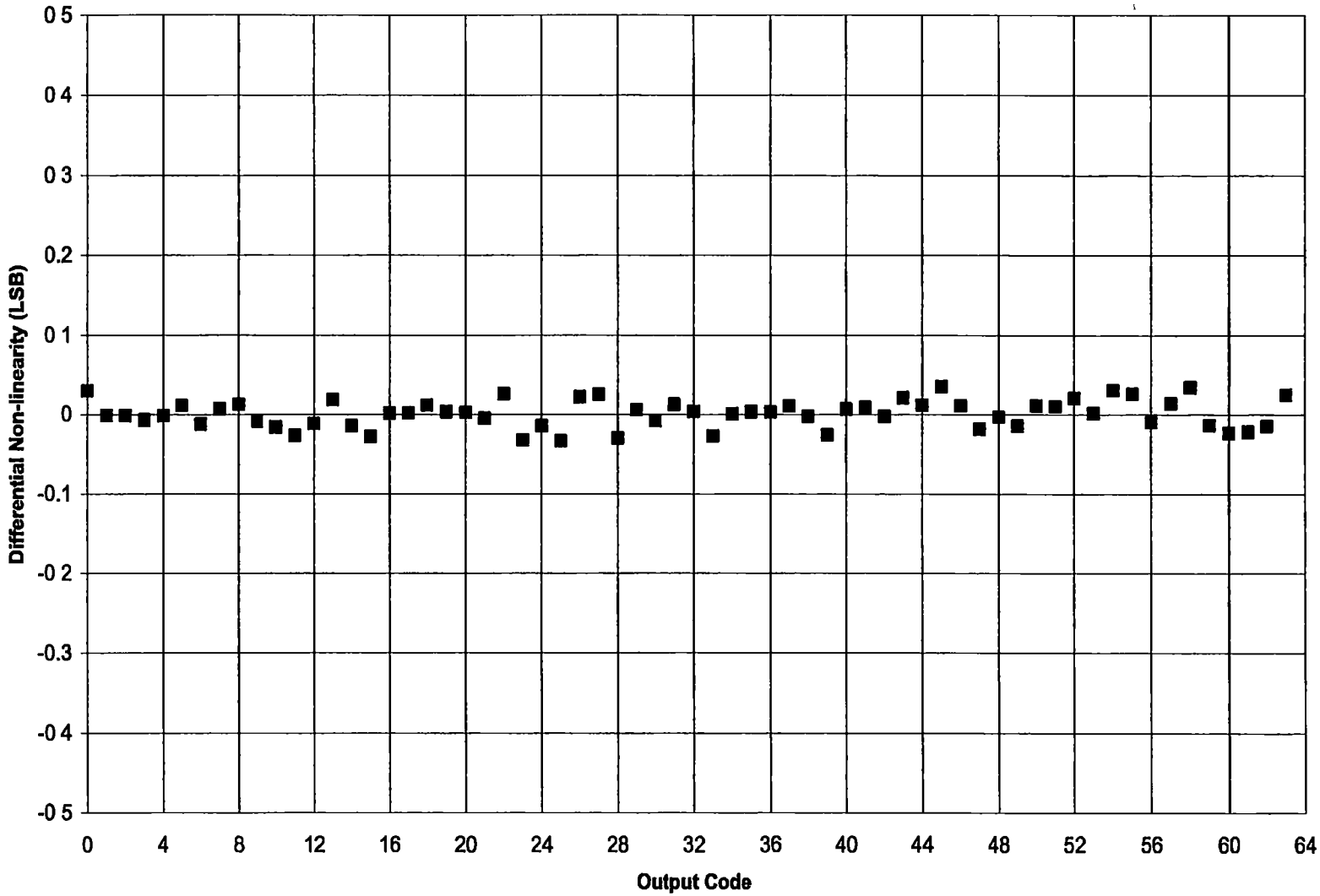


Figure 5-8. Differential non-linearity of random data generated for code density test measurements.

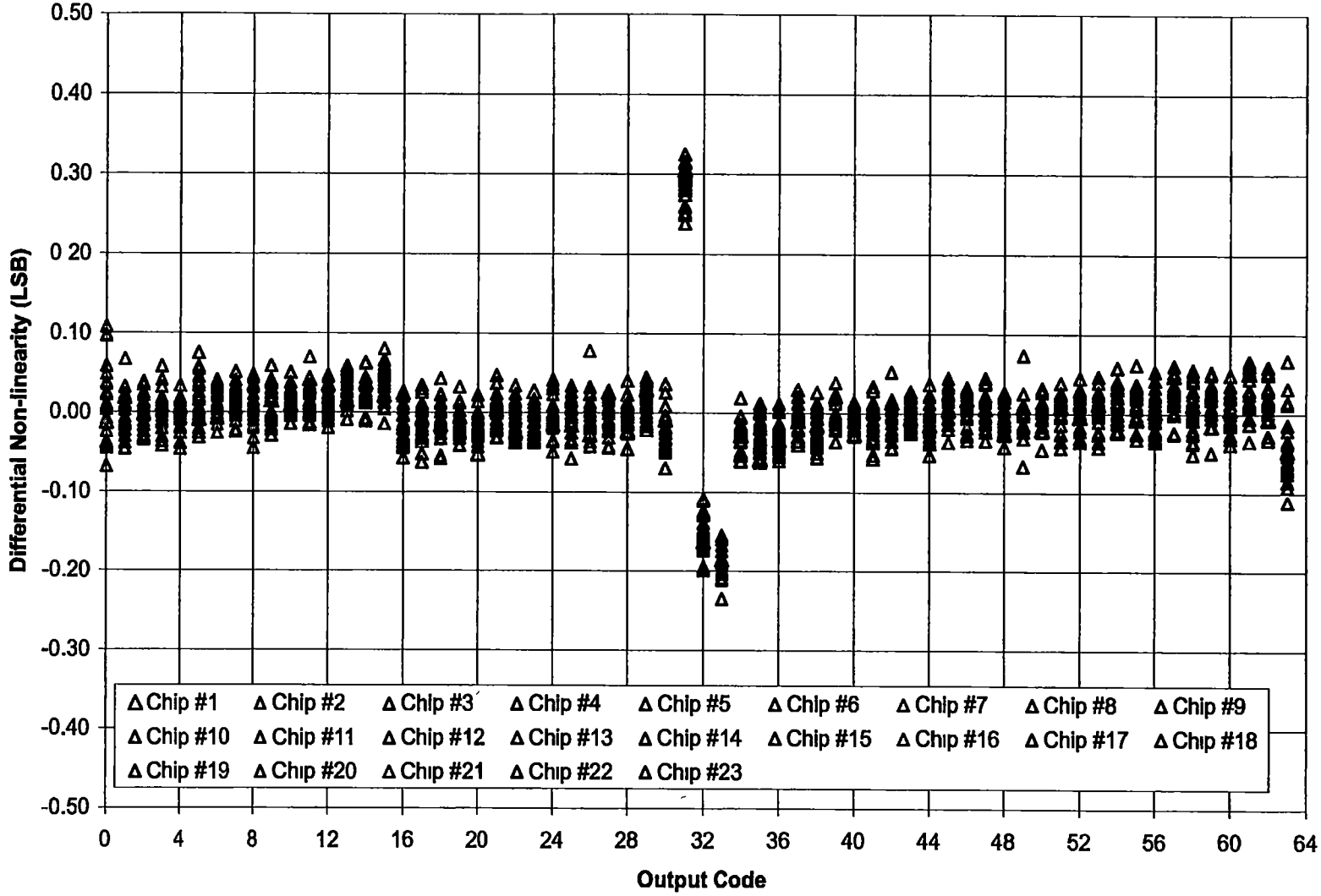


Figure 5-9. Differential non-linearity performance of all ADC chips from code density measurements.

voltages near the middle of the resistive ladder, and these transients lead to non-linearity errors of the ADC near these transitional regions. Nevertheless, the measured linearity performance of the ADC evaluated with the code density test is within the required linearity specifications and therefore is adequate for this time measurement application.

5.2 Comparator Offset Measurements

An entirely separate test board was designed and constructed to measure comparator offset performance. A detailed schematic of this test board is shown in Figure 5-10. Since sensitive millivolt signal levels were under evaluation, special attention was given to the design and layout of the test board. The circuit was constructed on a copper-clad board that served as a ground plane. Component placement and signal routing was performed to separate low-level input signals and high-level output or clock signals. Also, de-coupling capacitors were extensively used with tight connections between components power pins and ground. Three separate regulated power supply systems were implemented for power supply de-coupling. All bias and reference generation circuitry were powered from one supply system. The prototype chip with output buffers and filter circuits shared a second supply system. The clock oscillator was provided an entirely separate third supply system, which no other additional circuitry utilized. A photograph of the test board developed to evaluate the corrected offset performance of the CMOS comparator channel is shown in Figure 5-11.

The offset correction performance of the comparator channel was evaluated with a dc or very slow varying input signal. Both inputs of the comparator were available for

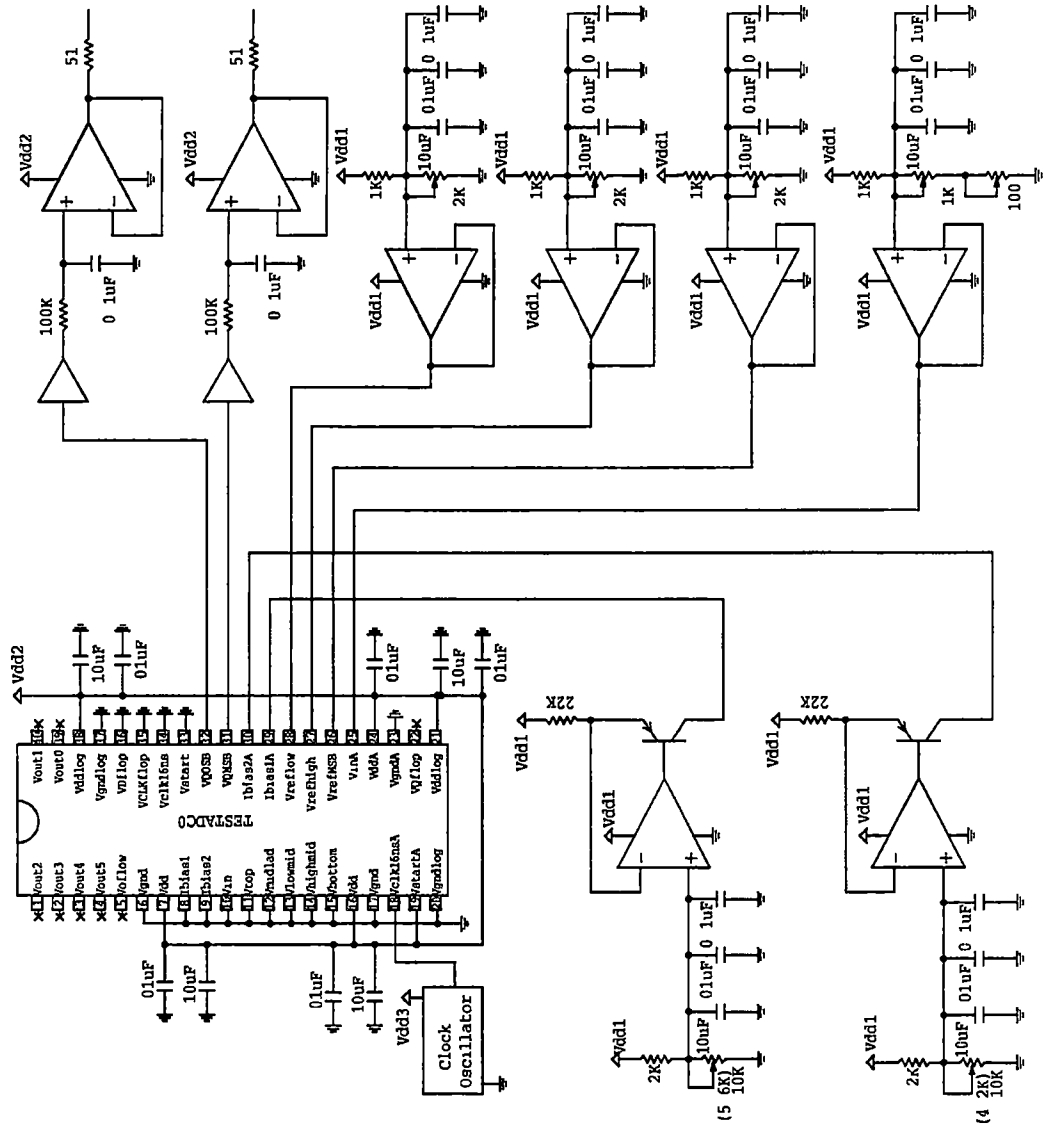


Figure 5-10. Schematic diagram of test circuitry designed to evaluate comparator offset performance.

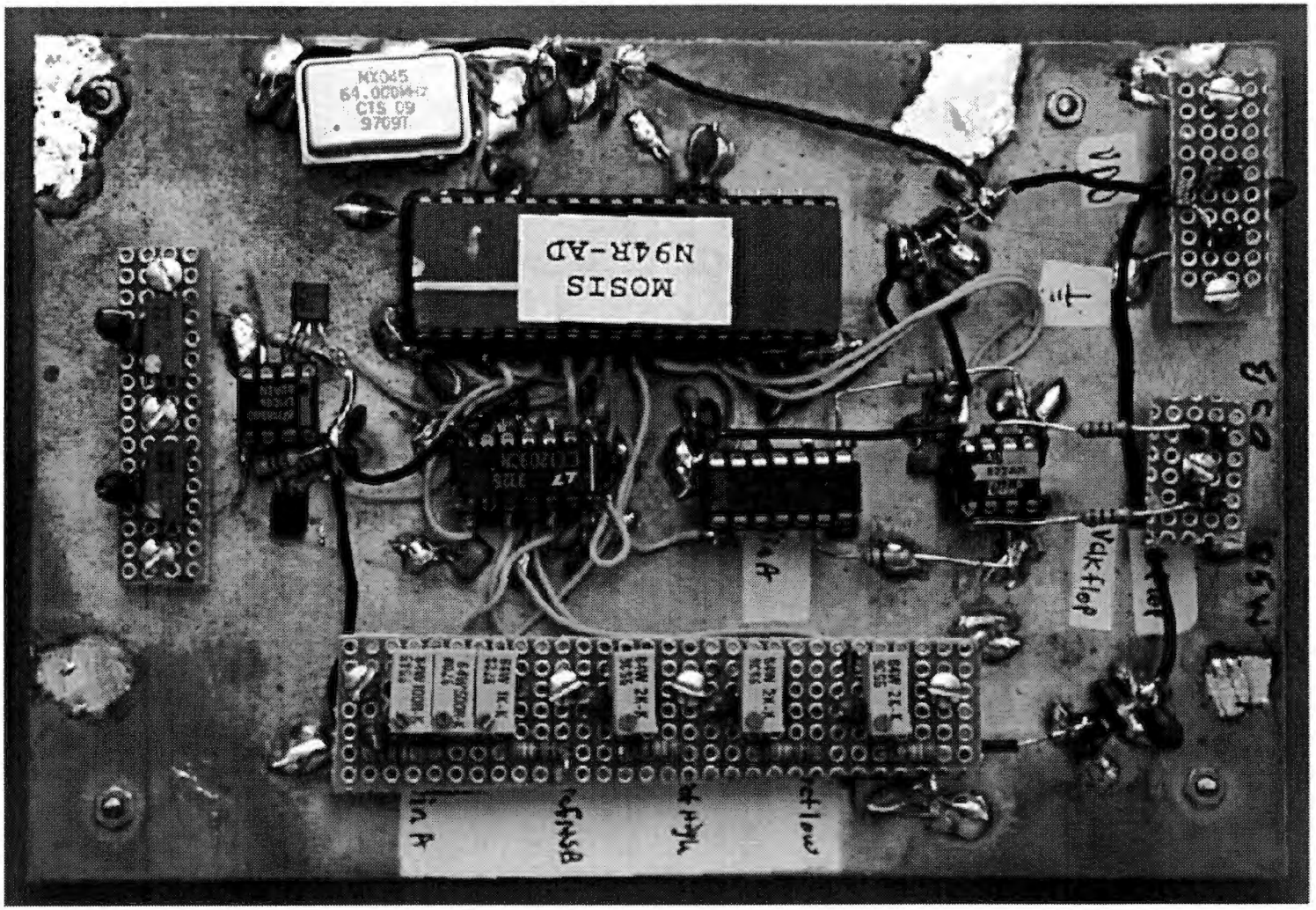


Figure 5-11. Photograph of test board developed to perform comparator offset measurements.

testing and a CMOS logic level at the output of the comparator channel was available to determine the comparator decision. The output of the comparator was buffered and low pass filtered to achieve an average dc level of the comparator output. Offset measurement testing was performed by applying a reference voltage to the minus input of the comparator and then slowly varying the positive input. These dc sweep measurements were performed with the comparator free running or continuously comparing the input signals while the filtered comparator output voltage was monitored. When the filtered dc output level of the comparator was approximately half the power supply voltage, the input differential voltage of the comparator was measured and this value was taken to be the corrected offset voltage of the comparator.

Corrected comparator offset measurements were made on all twenty-three prototype chips at two different comparison rates. Table 5-1 contains corrected comparator offset measurements on all twenty-three comparator channel prototypes at comparison rates of 8 MHz and 16 MHz. These measurements reveal that the CMOS comparator channel maintains a worst case input-referred offset of less than 1 mV at a conversion rate of 8 MHz and less than 2 mV at a comparison rate of 16 MHz while dissipating less than 2.6 mW. The variation of offset voltage with comparison rate or frequency has been reported with comparator circuits [33]. A significant portion of the variation of offset voltage with frequency is believed to be contributed to clock coupling in the package and test board. The measurements made on the comparator design also show that the corrected offset voltages are tightly controlled with a large systematic offset component in the offset voltages recorded. Again this phenomenon is probably due

Table 5-1. Corrected comparator offset measurements at 8 MHz and 16 MHz.

Chip	Offset at 8 MHz (mV)	Offset at 16 MHz (mV)
1	0.950	1.97
2	0.760	1 70
3	0.830	1.73
4	0.660	1.65
5	0.830	1.70
6	0.860	1.62
7	0.810	1.76
8	0.770	1.66
9	0 870	1.85
10	0.930	1.80
11	0.820	1.77
12	0.870	1.80
13	0.890	1.84
14	0.720	1 48
15	0.990	1.87
16	0.930	1.70
17	0.880	1.80
18	0.920	1 82
19	0.780	1.65
20	0.851	1 85
21	0.890	1.83
22	0.930	1.93
23	0.800	1.74
Max Offset	0.99	1.97
Min Offset	0.66	1.48
Average Offset	0.85	1.76

to clock and signal coupling in the integrated circuit layout, package, or test board. From the corrected offset measurements obtained, the offset performance of the CMOS comparator is more than adequate for application in the 6-bit ADC with a 20 mV/LSB resolution. This conclusion is further substantiated by the measured INL and DNL performance of the ADC.

Chapter 6

Conclusions

6.1 Summary

The development of a 6-bit 15.625 MHz CMOS two-step analog-to-digital converter (ADC) has been presented. The ADC was developed for use in a low dead time high-performance sub-nanosecond time-to-digital converter (TDC), which will be incorporated in a new generation front-end application specific integrated circuit for positron emission tomography imaging.

The ADC architecture was based upon a two-step approach, which reduced the comparator count by a factor-of-two when compared to the traditional flash ADC architecture. As a result, a significant reduction in area, power dissipation, and input capacitance of the converter was achieved. A key element in the design of the ADC was the development of an offset corrected CMOS comparator. The comparator utilized a unique offset calibration technique, which employed offset correction in both the preamplifier and subsequent regenerative latch stage to guarantee good performance over extreme process variations. A complete non-linearity analysis of the ADC was presented which related reference generation errors and comparator offsets to integral and differential non-linearity performance of the converter. This analysis was critical in identification of error contributors in the ADC, which were then minimized to achieve acceptable linearity performance. Also, digital error correction was employed to overcome most major metastability problems and errors associated with flash or flash-

type converters.

Significant effort was spent evaluating and characterizing the performance of the CMOS ADC and the offset corrected comparator designs. A fully automated test board including computer control was developed to evaluate the ADC for static and dynamic linearity performance. Also, an independent test board was developed to measure the corrected offset performance of the comparator channel.

Characterization of twenty-three ADC prototype chips indicated that the converter maintained differential and integral non-linearity performance well below the required ±½ LSB specification while achieving a 20 mV/LSB resolution. Also, independent corrected comparator offset measurements revealed that the CMOS comparator design maintained a worst case input-referred offset of less than 1 mV at a comparison rate of 8 MHz and less than 2 mV at conversion rates as high as 16 MHz while dissipating less than 2.6 mW.

6.2 Suggested Design Improvements

It should be noted that the 6-bit ADC developed and presented in this work satisfies all specifications and requirements for the envisioned application in the sub-nanosecond time measurement system. However, as with most designs, some improvements can be made to the ADC provided the opportunity.

Based upon the measured data, switching transients are believed to have been generated in the reference circuitry which caused errors in the reference voltages and significantly contributed to the linearity errors of the converter. These switching

transients and resulting reference voltage errors are most prominent at the center portion of the resistor ladder, which are the highest impedance nodes. These transients can be further minimized by several methods. One possible solution to minimize the effects of switching transients in the reference generation network could be to modify the ADC timing scheme. This timing modification would decrease the MSB comparator decision time and allocate the time to a transient recovery period. This new timing methodology would allow the transients in the reference generation network to settle out and the reference voltages would recover before the OSB comparison process begins. Another technique could be to implement a lower impedance resistive divider at the cost of increased power dissipation for the same reference voltage. This would lower the recovery time constant of the switching transients and perhaps minimize reference voltage generation errors. A third possible solution to minimize switching transients in the reference generation circuitry could be to apply an additional reference voltage to the middle tap of the resistive divider. This technique would also effectively lower the overall impedance of the ladder especially at the middle tap of the ladder, which should reduce switching transients and possibly correct or eliminate any error in the reference voltage at this node.

Another potential ADC design improvement could be to improve the resistor matching in the reference generation circuitry to below the 1% resistor mismatch specification. Integrated circuit layout techniques could possibly improve the resistor matching in the reference generation circuitry. The contact resistance in the resistive ladder varies widely and can degrade matching behavior. This is especially the case in

converters featuring moderate to high-resolution in which low-valued resistors are used to achieve a low impedance reference generation network. To minimize or eliminate this problem, the resistor network should be arranged in which no resistor contacts are used in the current path of the resistive divider. This technique has been reported to improve resistor string matching in ADCs and should improve the resistor matching in the reference generation network [36].

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Vita

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