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A low-noise microluminometer for a bioluminescent bioreporter integrated circuit

Gregory Wayne Patterson

To the Graduate Council:

I am submitting herewith a thesis written by Gregory Wayne Patterson entitled "A low-noise microluminometer for a bioluminescent bioreporter integrated circuit." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

James M. Rochelle, Major Professor

We have read this thesis and recommend its acceptance:

Michael L. Simpson, T. Vaughn Blalock

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A Low-Noise Microluminometer for a Bioluminescent Bioreporter Integrated Circuit

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Gregory Wayne Patterson

August 2000

Dedication

This thesis is dedicated to my parents,

Mr Robert L Patterson

And

Mrs Shirley A Patterson

who have given me love and encouragement throughout my academic career

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I would like to thank several people without whom this thesis could never have been completed I would first like to thank the members of my thesis committee I thank my major professor, Dr James M Rochelle, for the many hours he spent with me in the laboratory during testing and the helpful advice he gave me concerning design issues and the direction of my thesis He has been an excellent mentor I thank Dr Michael L Simpson for giving me the opportunity to be a part of this research and giving me valuable instruction throughout my work I thank Dr T V Blalock for his help during the writing of this thesis, particularly in the area of noise analysis I also thank him for the outstanding undergraduate education I received in analog electronics

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Finally, I want to thank my family for their love and support I thank God for them and all of the blessings He has given me in my life

Abstract

This thesis presents the analysis and design of a low-noise microluminometer for a hybrid electronic/biological chemical sensor known as a Bioluminescent Bioreporter Integrated Circuit (BBIC) The microluminometer consists of photodetection and signal processing Both functions are integrated in a standard bulk CMOS process (HP 0 5 μm CMOS)

The photodetection is first described in terms of physical operation The implementation of photodetectors in a CMOS integrated circuit process is then presented The signal processing system is analyzed, and the errors introduced by individual system components are described A detailed system-level noise analysis is also presented The design of a low-noise amplifier is the focus of this thesis The amplifier design is described in detail Finally, the results from testing of the fabricated prototype are presented

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Distributed Chemical Sensing

Distributed sensing is a scheme in which a collection of remote sensors is deployed throughout a region to be monitored It allows for parallel testing and quicker access to comprehensive test data than a more centralized measurement [1] Various measurement applications benefit from distributed chemical sensing Among these are environmental monitoring and therapeutic drug discovery Many measurement systems do not lend themselves easily to these types of applications The large detection devices, cabling, and cost involved in some systems often make them impractical for applications in which remote sensing, small volumes, or multiple parallel sensing are involved These applications require an instrumentation solution that is small, inexpensive, and accurate [2]

1.2 Biosensors

Biosensors are one class of sensors that may be used in distributed systems A biosensor is the combination of a biological sensing component, or bioreporter, with a transducer device The biological element reacts with a targeted substance, and the

transducer then detects this reaction The most common bioreporters make use of enzymes and antibodies, surface plasmon resonance (SPR) sensors being a popular example SPR sensor technology has been shown to be feasible for distributed chemical sensing [1]

1.2.1 Whole-cell Biosensors

Whole-cell biosensors use intact living cells as the biological component One of the advantages of using a whole-cell biosensor is that not only is analytical information such as the concentration of a substance obtained, but functional information is gained also Functional information describes how a stimulus affects a living system This information is particularly useful for environmental monitoring, drug screening and other applications requiring the measurement of biological outcomes One type of important functional information is bioavailability, or the availability of a substance to living organisms In environmental monitoring, for example, the total bioavailability of a pollutant is a concern Whole-cell biosensors are well suited to environmental sensing, because they can be made small enough for use in the field, are able to survive in the field, and are capable of continuous monitoring [3]

1.2.2 Bioluminescent Bioreporters

Bioluminescence is the production of light by a living organism Measuring bioluminescence is a convenient means of continuously monitoring cell activity in a whole-cell biosensor Calorimetric means (e g measuring the heat of metabolism) have commonly been used as a signaling mechanism between cells and transducers

However, this method suffers from many biological and non-biological sources of heat noise Fortunately, bioluminescent bioreporters can be made to selectively interact with a targeted substance This is done by fusing bioluminescent genes with the genes of the bioreporter cell The end result is a luminescent response that is tightly coupled to a very specific metabolic response Genetically engineered bioluminescent bioreporters have been developed, using both prokaryotic and eukaryotic cells, for use in environmental monitoring applications [2]

1.3 The Bioluminescent Bioreporter Integrated Circuit

A solution to some of the problems of distributed sensing lies in system integration Current integrated circuit (IC) technology allows signal processing, communication, and other functions to be implemented in a single chip, minimizing both size and cost The use of CMOS technology is particularly desirable The benefits of CMOS include low cost and the ability to easily integrate both digital and analog circuits CMOS is also particularly useful in low-power applications The combination of a CMOS IC with a bioluminescent bioreporter provides a powerful integrated sensor technology

The Bioluminescent Bioreporter Integrated Circuit (BBIC) concept is shown in Figure 1 Here, the bioreporters are placed on a CMOS IC that detects bioluminescence, performs low-noise signal processing, and transmits the sensor data The IC can be divided into two main sections the microluminometer (which includes

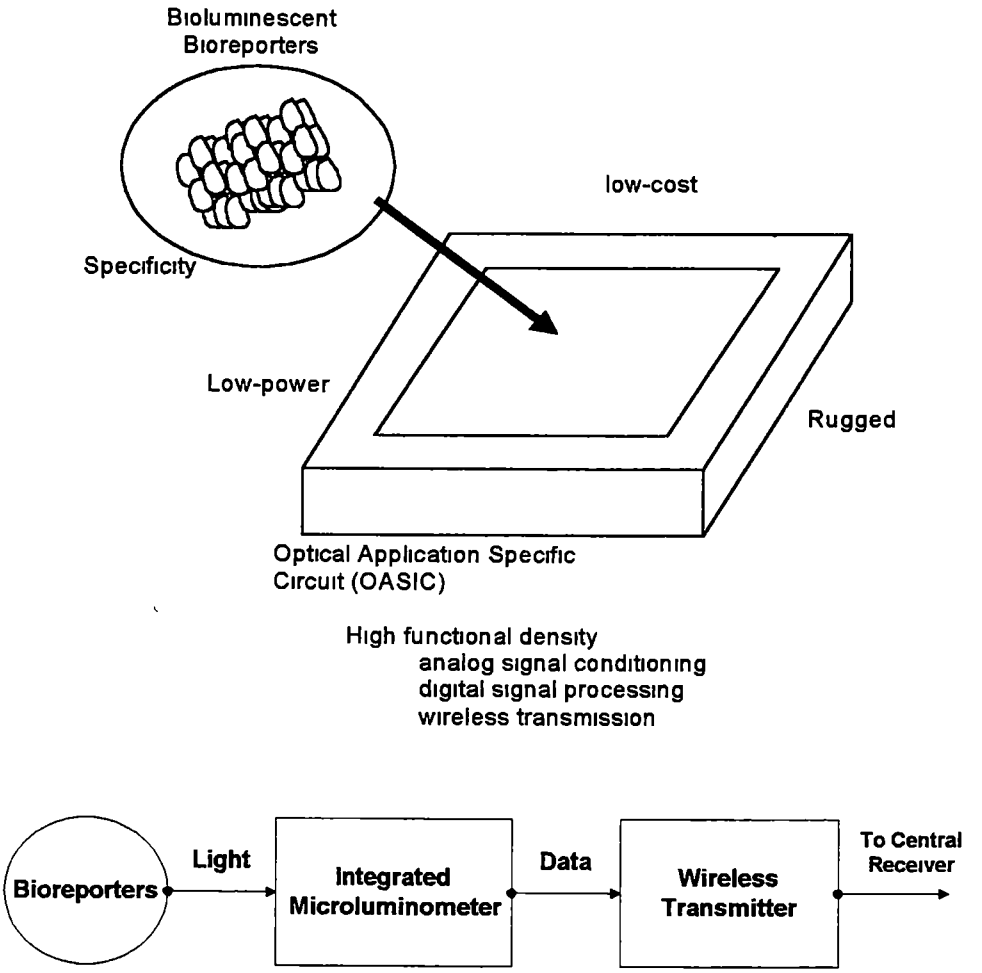

Figure 1 - The Bioluminescent Bioreporter Integrated Circuit Concept

integrated photodetection and signal processing), and the transmitter (which performs wireless data transmission) The BBIC is novel in that it integrates the biological element with the rest of the sensor In this situation, the bioreporter can be seen as a component of the integrated circuit, analogous to a resistor or transistor [2]

An advantage of the BBIC concept is the close proximity of the sensing element to the transducer Having the bioreporters affixed to an IC with an integrated microluminometer eliminates the need for external optical devices Many optical biosensors, such as the SPR sensors previously mentioned, require devices to couple the signal from the detector to the rest of the measurement system Fiber-optic cables, lenses, gratings, and waveguides, which are commonly used, are not needed in the BBIC. An integrated wireless transmitter also replaces the cabling often needed for communication with the sensor This method produces a stand-alone sensor that is selective, sensitive, low-power, rugged, and inexpensive

1.3.1 Low-noise Microluminometer

1.3.1.1 Integrated Photdetection

The light produced by the bioreporters must first be converted to an electrical signal Photodetection must be done with maximum quantum efficiency and minimum addition of noise, allowing for the detection of the smallest possible optical signal Measurement of the bioluminescent signal can be integrated easily in bulk CMOS N-well/p-substrate, n-diffusion/p-substrate, and p-diffusion/n-well junctions are available in a standard n-well process for use as photodiodes The performance of such devices

has been demonstrated in a fully integrated CMOS photo-spectrometer [4]

1.3.1.2 Low-noise Signal Processing

The level of photocurrent is proportional to the light output of the bioreporters, which is proportional to the concentration of the targeted substance The signal-processing section of the microluminometer must digitize the information contained in the level of photocurrent, making it available for data transmission This system should introduce as little measurement error as possible, again allowing for the smallest possible detectable signal, since the bioreporters produce low-level light in response to low concentrations of the targeted substance The system must be optimized for low-noise performance, having as a key component some form of low-noise amplification

1.3.2 BBIC Design Challenges

The BBIC is an innovative solution to distributed sensing, but it does present certain design challenges not yet mentioned Whole-cell biosensors present the problems of dealing with living organisms The bioreporters must first be kept alive for as long as possible. Proposed methods to increase cell lifetime are the inclusion of a food source on the IC and a freeze-drying technique in which the cells are stored until needed The bioreporters also must be protected from the environment, while allowing contact with the substances to be measured The protective structure must also have the proper optical properties Currently, a sol-gel process is being used, in which the cells are entrapped in a glass matrix Finally, the growth of the cells must be accounted for Cell growth is accompanied by an increase in bioluminescent intensity, which is

detected as an increase in the concentration of the targeted substance Similarly, a decrease in cell population is detected as a decrease in concentration Any cell growth that is not the directly correlated to an increase in chemical concentration can be seen as a form of biological noise Genetic engineering methods to regulate bioreporter cell growth are being considered

The IC itself presents certain challenges A coating is needed to protect the IC from the cells and the environment Any protective coating must provide optical shielding and must not be detrimental to the cells Thin-film, amorphous silicon nitride is currently being investigated for this purpose The fact that the BBIC is a wireless sensor also presents a problem The BBIC cannot be connected to a power source via any type of cabling, the initial solution being battery power Therefore, the electronics must be both accurate and power efficient

1.4 Scope of Thesis

This thesis will describe the development of a low-noise microluminometer for the BBIC sensor A prototype of the microluminometer has been fabricated in the HP 0 5 μm CMOS process available through the MOSIS fabrication service [5] This prototype includes a large-area, integrated photodetector coupled to a low-noise signal processing system

Chapter 2 presents a system-level design analysis of the microluminometer The requirements of the microluminometer are outlined A discussion of the integrated

photodetection is first presented, describing both the physical operation and IC implementation of the photodetector A description of the signal processing system is then given. The basic system topology is presented, and its operation is explained The various system components and their error contributions to the system are each examined A system-level noise analysis is also performed The optimization of the system for low-noise performance is explained in detail Finally, the implementation of the system in CMOS and results of computer simulation are given

Chapter 3 details the development of a low-noise amplifier (LNA) incorporated in the signal processing The design of this amplifier is the focus of the design work in this thesis The optimization of the LNA for low noise contribution is described in great detail Simulation results are presented, as is the implementation of the amplifier in CMOS

Chapter 4 presents the results from testing of the aforementioned microluminometer prototype Results using a laboratory light source are given Chapter 5 gives some conclusions and proposes future improvements that could be implemented

Chapter 2

Microluminometer System Analysis and Design

2.1 Microluminometer System Overview

The microluminometer is composed of two main sections photodetection and low-noise signal processing, as shown in Figure 2 The sensor data (chemical concentration) is contained in the intensity of light from the bioreporters The light is converted to an analog electrical signal by a photodetector This signal must then be converted to a form that can be reported by the BBIC The BBIC sensor data is reported through the use of a digital transmitter, therefore the signal processing section of the microluminometer must perform some form of analog-to-digital conversion

The main design goal of the microluminometer is that it be sensitive to the lowest possible level of light, thereby making the BBIC sensitive to the lowest possible concentration of the targeted chemical substance The minimum detectable signal (MDS) is determined by such factors as the quantum efficiency of the photodetector, detector leakage current, and the intrinsic noise of the detector and signal processing electronics It is also necessary that all of the microluminometer functions, including photodetection, be realized in a standard CMOS process Finally, power consumption must be considered, because the BBIC is a wireless sensor

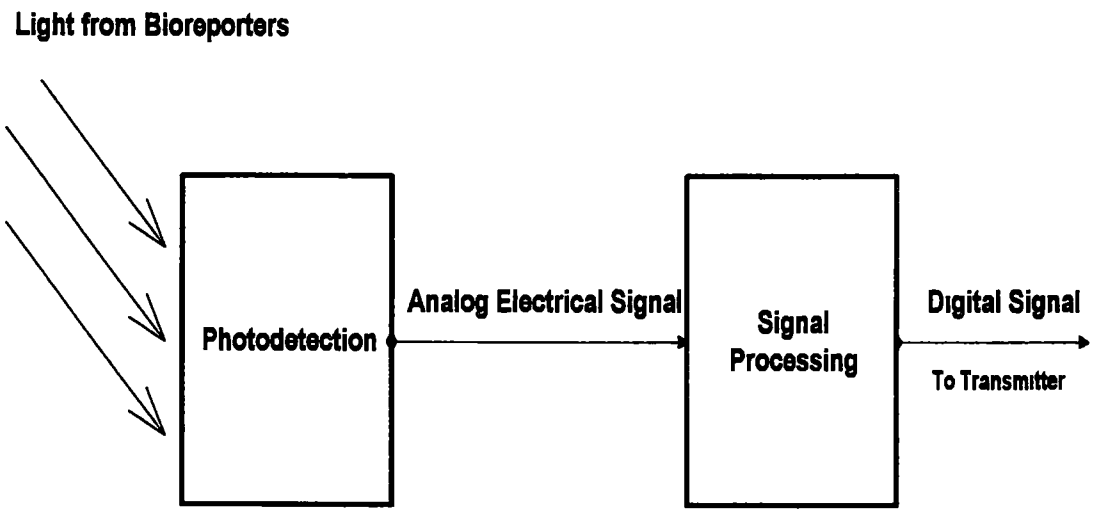

Figure 2 – Basic Microluminometer Operation

2.2 Photodetection

2.2.1 Photodiode Operation

A simple p-n junction diode can be used to convert light into an electrical signal Figure 3 [6] illustrates the mechanism by which this conversion takes place The energy of incident photons is absorbed by the atoms of the semiconductor This energy transfer moves electrons in the valence band to the conduction band, producing electron-hole pairs The carriers then may or may not contribute to a detectable photocurrent Carriers that are optically generated in the depletion region (or diffuse there from the neutral regions) are accelerated toward the diode contacts by the "built-in" electric field produced by the bound ions present there These carriers almost certainly contribute to the photocurrent The carriers that recombine before they reach the contacts do not contribute to a current These are generated mostly in the neutral regions, sufficiently far from the edges of the depletion region This method of photodetection does not allow for single photon counting, as do photomultiplier tubes

Quantum efficiency (η) describes the effectiveness of a detector in producing a detectable signal and is given by [7]

$$\eta = \frac{I_p \; h \cdot \nu}{P_{op} \cdot A_{det} \cdot q} \cdot 100\% \quad , \qquad (2\,1)$$

where I_p is the photocurrent(A), h is Planck's constant(6 626 x 10^{-34} Jsec), ν is the optical frequency(Hz), P_{op} is the optical power(W/cm^2), A_{det} is the detector area(cm^2),

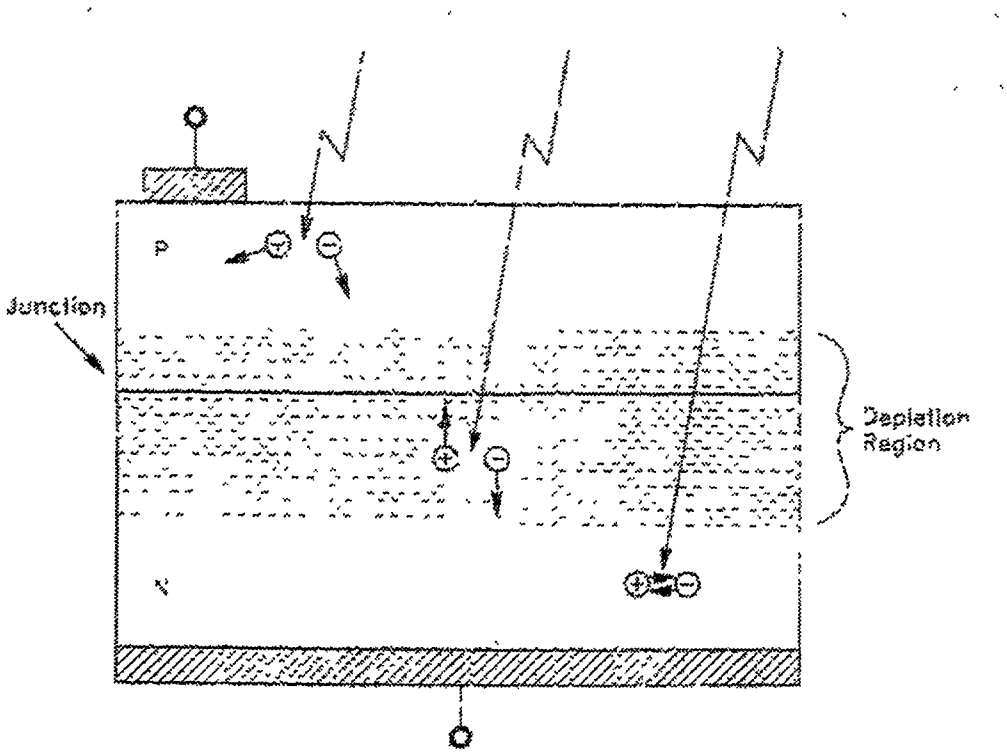

Figure 3 - Photodiode Operation

and q is the charge of an electron(1 602 x 10^{-19} C) Quantum efficiency can be expressed more simply as the transfer function for a photodetector Photons strike a detector at a certain rate and result in the emission of carriers at another rate (photocurrent), giving

$$\eta = \frac{I_p}{q \cdot R_{ph}} \frac{electrons}{photon} \quad , \tag{2 2}$$

where R_{ph} is the rate at which photons strike the detector (photons/sec) Quantum efficiency is the most important figure of merit for a photodetector, and is expressed as a percentage An ideal detector would have a quantum efficiency of 100 percent, signifying that each photon produces a detectable signal

Real photodiodes have quantum efficiencies that are less than ideal due to the loss of carriers through recombination The likelihood that a free electron or hole will recombine is dependent on several factors, one being the location of its generation in relation to the depletion region As previously discussed, carriers that reach the depletion region (or are generated there) most likely become part of the signal current Carriers generated in the neutral regions are driven primarily by diffusion, because there is only a weak electric field there due to concentration gradients Therefore, carriers released at a distance greater than a diffusion length from the depletion region have a low probability of becoming part of the photocurrent [6] The location of photon absorption in a photodiode is a function of the properties of the semiconductor and the wavelength of the incident light This function can be expressed as [4]

$$F_{abs}(d) = F_0 \cdot [1 - e^{-(\alpha\, d)}] \quad , \tag{2 3}$$

where $F_{abs}(d)$ is the number of photons absorbed at a distance d from the surface of the semiconductor, F_0 is the number of incident photons, and α is the absorption coefficient for a particular semiconductor The absorption coefficient is a function of the wavelength of incident light, and is plotted for silicon in Figure 4 [4] The absorption coefficient is inversely proportional to the wavelength of incoming light, indicating that detectors with shallower junction depths are more effective at detecting short wavelengths of light The bioreporters that have been developed for the BBIC produce light at a wavelength near 490 nm [2], suggesting the use of such a detector

The location of the depletion region is dependent on the location of the junction (see Figure 3) This can be controlled, in a limited sense, through the choice of detector type in a given IC process (as explained in section 2 2 4) The width of the depletion region and its arrangement about the junction are determined by bias and doping profile Taking the simple case of an abrupt p-n junction, the depletion region width is given by [8]

$$W_{dep} = \sqrt{\frac{2 \cdot \varepsilon_s}{q} \cdot \left(\frac{N_A + N_D}{N_A \cdot N_D} \right) \cdot \left(V_{bi} + V_R \right)} \quad , \tag{2 4}$$

where ε_s is the permittivity of the semiconductor , V_{bi} is the "built-in" potential of the junction, V_R is the applied reverse bias voltage, and N_A and N_D are the acceptor and donor concentrations respectively The geometry for this simple case is described by

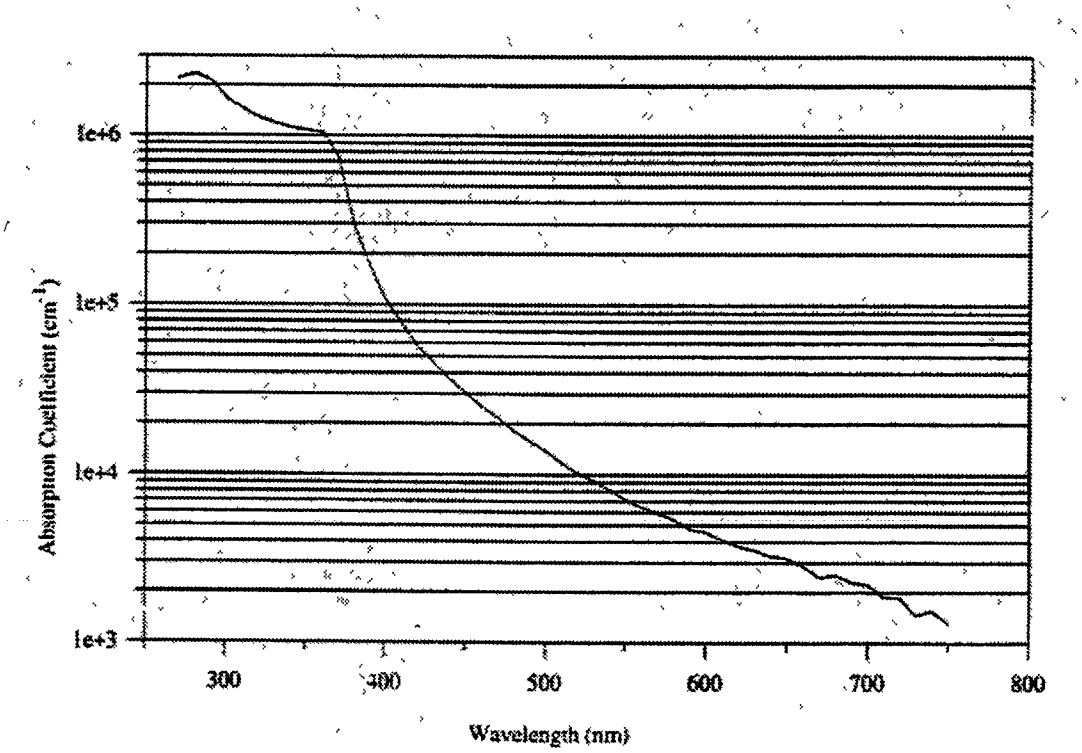

Figure 4 - Absorption Coefficient for Crystalline Silicon

[8]

$$N_A \cdot x_p = N_D \cdot x_n \quad , \tag{2 5}$$

where x_p and x_n are the distances that the depletion region extends into the p and n sides of the junction respectively Two important characteristics of the depletion region are seen in these equations First, its width increases with an increase in applied reverse bias, improving the charge collection of the detector Second, it extends further into the side of the junction that is more lightly doped Knowledge of the size and location of the depletion region and the absorption characteristics of the semiconductor are important in photodiode design

2.2.2 Photodiode Modeling

A model for the photodiode is necessary for system design A simple model for a reverse-biased photodiode is shown in Figure 5

2.2.2.1 Photodiode Currents

The current generator, $I_p + I_L$, represents the sum of the photocurrent and leakage current These currents flow in the same direction The value of the photocurrent, I_p, is determined by the intensity of the optical signal and the quantum efficiency of the detector The leakage current, or dark current, of the detector is represented by I_L To first order, this leakage can be determined from the ideal diode equation [9]

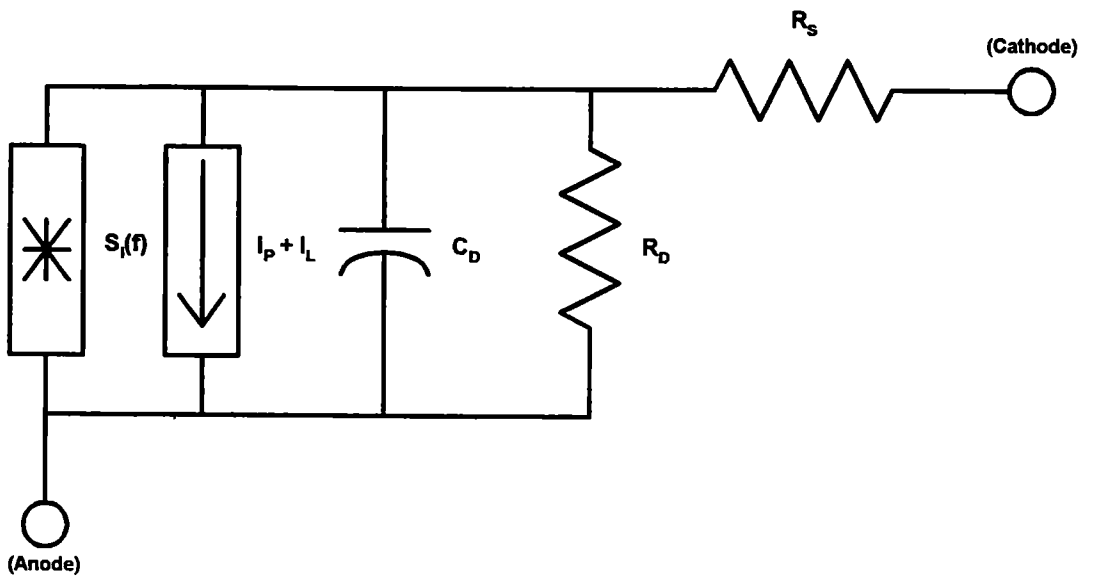

Figure 5 - Simple Photodiode Model

$$I_d = I_S \cdot \left(e^{\frac{V_D}{V_t}} - 1 \right) \quad , \tag{2 6}$$

where I_d is the forward diode current, I_S is the reverse saturation current of the diode, V_D is the applied forward bias voltage, and V_t is the thermal voltage (approximately equal to 26mV at room temperature) For sufficient reverse bias, the leakage current is therefore approximately equal to the saturation current This current is directly proportional to junction area and approximately doubles for every 5 °C increase in temperature [9]

The ideal diode equation adequately predicts the current for low-bandgap semiconductors (GaAs) at low current densities, but only gives qualitative agreement otherwise, due to generation or recombination in the depletion region [8] The current due to generation in the depletion region for reverse bias is given by [8]

$$I_{gen} = \frac{q \cdot A_{det} \cdot n_i \ W_{dep}}{\tau_g} \tag{2 7}$$

where n_i is the intrinsic carrier concentration (approximately 1 45 x 10^{10} cm^{-3} for silicon at room temperature) and τ_g is the generation lifetime Generation current may dominate the leakage for reverse bias at room temperature in silicon, due to the relatively low value of n_i in silicon At higher temperatures, the dark drift current (I_S) eventually dominates [8]

Another non-ideal effect occurs at the surface of the semiconductor Here, the

lattice structure of the semiconductor is disrupted, producing "dangling" bonds This creates generation-recombination centers at the surface, leading to increased recombination of carriers and the reduction of signal current The recombination rate is directly proportional to the recombination center density per unit area at the surface, which can be reduced through processing [8]

2.2.2.2 Photodiode Resistance

The shunt resistance of the photodiode is modeled by R_D This is the resistance of the zero-biased diode, which is very large R_D is so large that it can generally be neglected R_S represents the series resistance of the semiconductor material This resistance is low and again can usually be ignored [6]

2.2.2.3 Photodiode Capacitance

The capacitance of the detector is represented by C_D. For reverse bias, this capacitance is essentially the junction capacitance and is given for an abrupt junction diode as [10]

$$C_D = \sqrt{\frac{q\ \varepsilon_s}{2\ (V_{bi}+V_R)} \cdot \frac{N_A \cdot N_D}{N_A + N_D}} \cdot A_{\text{det}} \qquad (2\ 8)$$

This capacitance is directly proportional to area and decreases with increased reverse bias A lowered detector capacitance has several benefits, including decreased noise in charge-sensitive applications (to be discussed in section 2 4)

2.2.2.4 Photodiode Noise

The intrinsic noise spectral density of the photodiode is modeled by the current source $S_i(f)$ (A^2/Hz) A major component of diode noise is shot noise, which is the result of carriers crossing a junction Shot noise is broadband noise with a "white" power spectral density (PSD) The diode current is due to both dark current and photocurrent Neglecting the effects of generation in the depletion region, the dark current is equal to I_S for sufficient reverse bias The one-sided PSD of the shot noise for a reverse-biased photodiode is therefore equal to

$$I_{shot}^2 = 2 \cdot q \cdot \left(I_S + I_p\right) \frac{A^2}{Hz} \qquad (2\ 9)$$

For the special case of the zero-biased detector, the forward diffusion current exactly cancels out the reverse drift current This results in zero net diode current, but the noise powers of the two opposing currents add directly [11], giving

$$I_{shot}^2 = 2 \cdot q \cdot \left(2 \cdot I_S + I_p\right) \frac{A^2}{Hz} \qquad (2\ 10)$$

The zero-biased diode, therefore, may have higher noise than that of a reverse-biased diode

Another component of photodiode noise, not predicted by the ideal diode equation, is due to the generation/recombination of carriers in the depletion region Generation/recombination noise (g-r noise) often dominates the noise of

photodetectors [11]. For reverse-bias and low frequencies, the one-sided power spectrum of g-r noise is given by [12]

$$I_{g-r}^2 = 2 \cdot q \cdot I_D \cdot \frac{e_p^2 + e_n^2}{\left(e_p + e_n\right)^2} \frac{A^2}{Hz} \quad , \tag{2.11}$$

where e_p is the emission rate of holes from a center, and e_n is the emission rate of electrons from a center This noise has a white power spectrum for frequencies well below a frequency determined by the lifetime of the carriers in the photodetector [13].

Flicker noise in a diode is due to fluctuations in the surface recombination processes [12], and can be simply modeled (one-sided PSD) as

$$I_{flicker}^2 = \frac{K \ I_D^a}{f} \frac{A^2}{Hz} \quad , \tag{2 12}$$

where K is a flicker noise coefficient that depends on process and geometry, a is the flicker noise exponent (usually near unity), and f is frequency (Hz). Flicker noise is commonly referred to as "1/f noise", because its power spectrum is inversely proportional to frequency

The total diode noise is the composite of all the noise mechanisms described above. The power spectra of each of these noise sources add directly. A representative frequency spectrum of the total noise in a photodiode is given in Figure 6 [11] At low frequencies, flicker noise dominates At intermediate frequencies, the shot noise and g-r noise combine to give the diode noise a flat (or white) spectrum.

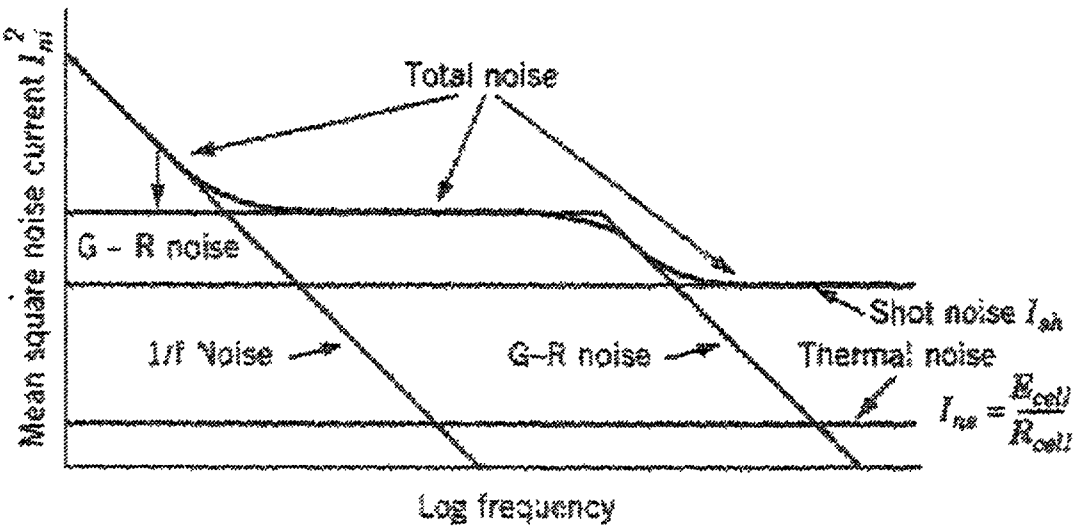

Figure 6 - Composite Photodiode Noise Current Spectrum

The g-r noise eventually decays at higher frequencies, leaving the shot noise as the dominant noise source. Also shown in Figure 6 is the thermal noise due to the series resistance of the diode (shown as E_{cell}/R_{cell}). As previously stated, this resistance is usually very small, so its noise can also be neglected in most cases

2.2.3 Detector Biasing

A photodiode should obviously be reverse-biased or zero-biased for low-level light detection. A large value of reverse bias creates a large depletion region in the diode (Equation 2.4). This increases the collection area of the detector, and thereby improves quantum efficiency The increased width of the depletion region also decreases detector capacitance. A major disadvantage of a large reverse bias is increased leakage current, partly due to the fact that a larger depletion region leads to higher g-r current (Equation 2.7) The leakage is minimized at zero bias, but the shot noise is increased (Equation 2.10). Also, detector capacitance is increased, and the quantum efficiency suffers The reduction of leakage current is essential for low-level detection Lower levels of signal current become increasingly difficult to distinguish from a large leakage current, and the variation of the leakage current with temperature is measured as a change in signal. Therefore, zero bias is the optimum configuration (even at the expense of lower quantum efficiency and higher noise).

2.2.4 Integrated Photodetection in CMOS

Figure 7 shows three types of photodiodes available in a standard n-well CMOS IC process. These detectors are formed by the junctions between: p-diffusion/n-well, n-well/p-substrate, and n-diffusion/p-substrate The diffusions are

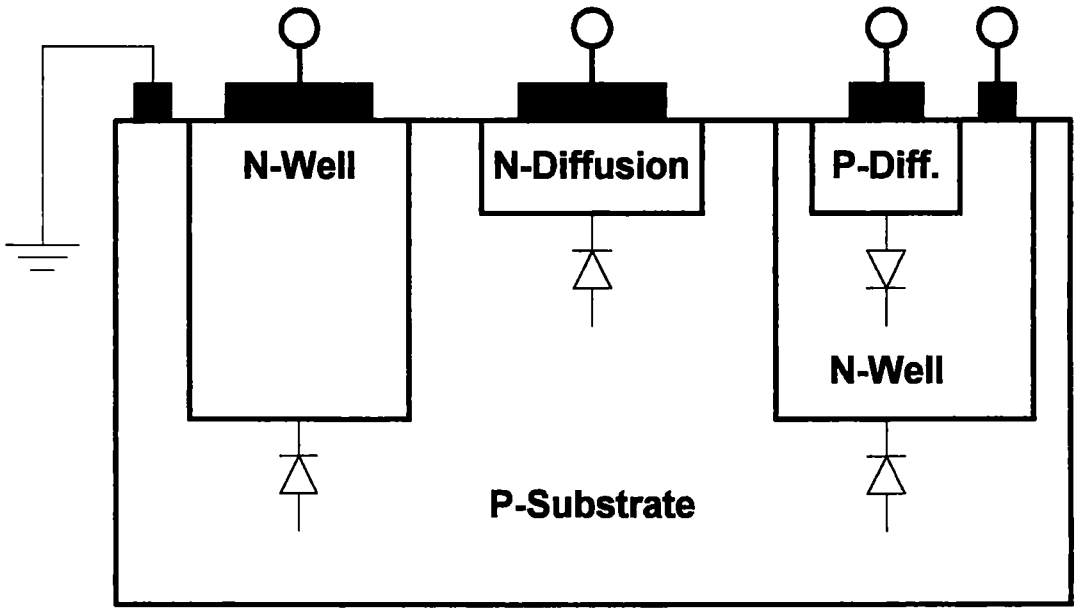

Figure 7 - CMOS-compatible Photodetectors

highly doped and are used to form the sources/drains of transistors The p-diffusion/n-well type (which is actually a combination of two diodes) has a shallow junction, making it a reasonable candidate for detection of the blue-green light (approximately 490 nm) produced by the bioreporters The junction extends mostly into the n-well, because it is much more lightly doped than the diffusion The n-well/p-substrate type of detector has a deeper junction, but can be biased at 0V for low leakage The n-diffusion/p-substrate detector has a shallow junction and can also be biased at 0V Its depletion region extends mostly into the substrate Initially, it would seem that the n-diffusion/p-substrate is best suited for use in the BBIC

2.2.4.1 CMOS Photodetector Evaluation

An IC was fabricated in the HP 0 5 μm CMOS (n-well) process to evaluate the relative performance of the different types of photodetectors Figure 8 is a photograph of the actual test chip The large center section is an array of photodetectors containing variations of the three basic detector types The array is surrounded by 18 channels of an early signal-processing prototype Each detector is connected to a channel of signal processing, and the output is brought off-chip for evaluation

Testing showed both the p-diffusion/n-well and n-diffusion/p-substrate detector types to have very poor collection efficiency The n-well/p-substrate detector type, however, had a measured quantum efficiency of 66% at 490 nm It also had a low measured leakage current of approximately 70 fA for a 1-V reverse bias and a bottom junction area of 8,600 μm^2 The n-well detector type was therefore chosen for use in the BBIC Figure 9 is a photograph of the actual n-well photodetector used in

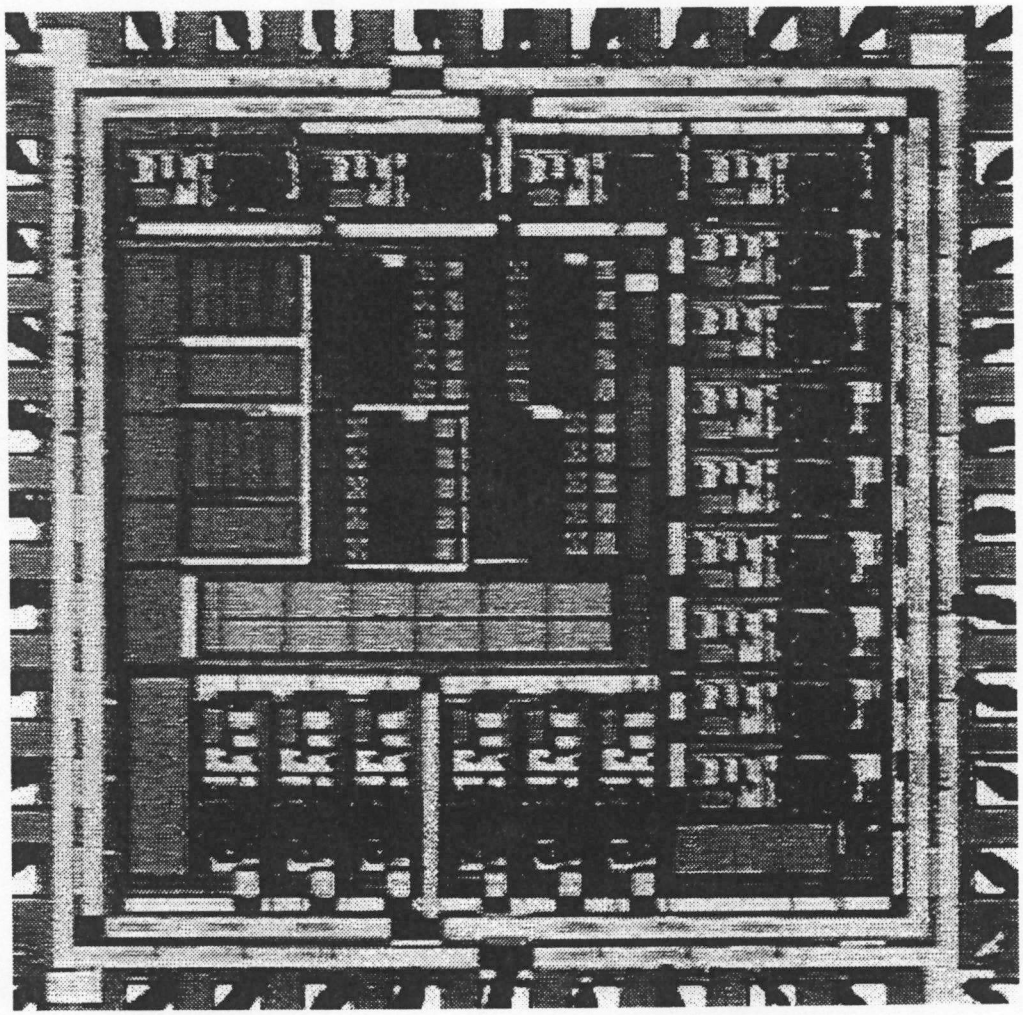

Figure 8 - CMOS Photodetector Evaluation Test Chip

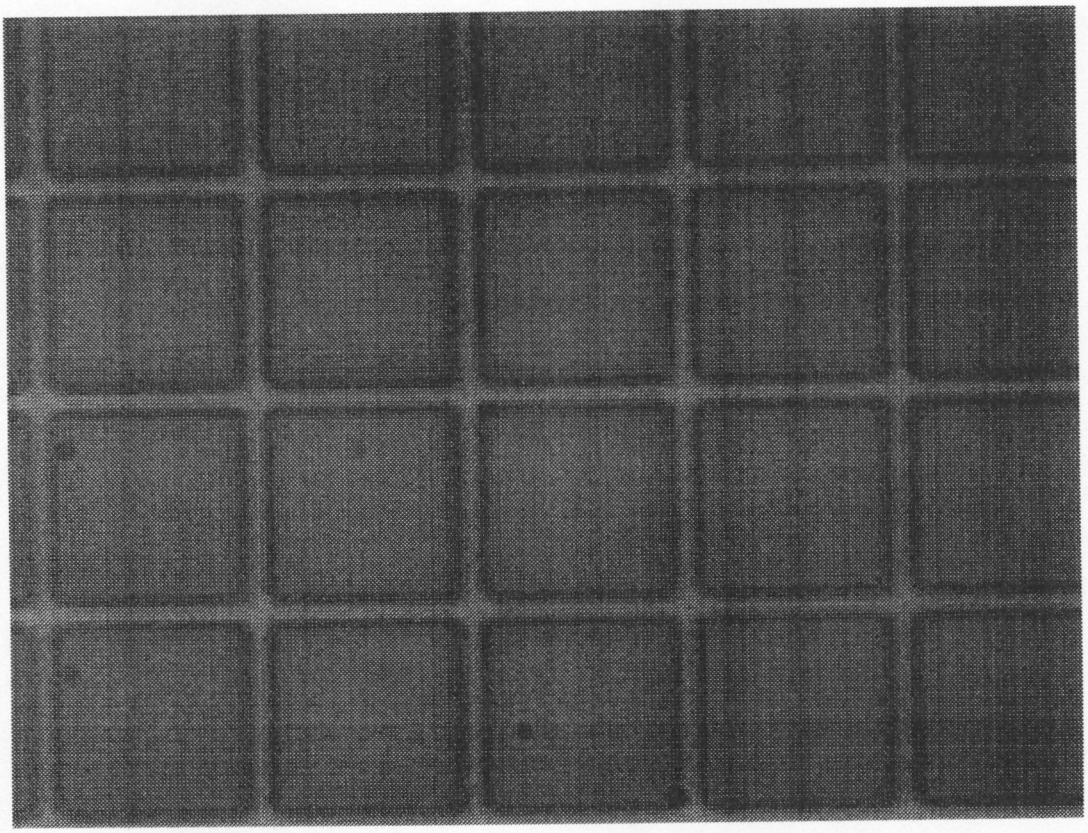

Figure 9 – N-well Photodetector

the microluminometer prototype The detector is formed by an array of small, parallel, n- well electrodes in the p-substrate This method is intended to reduce detector capacitance and leakage by decreasing the junction area of the total detector, while retaining a large active collection area For this design, the individual electrodes have an area of 5 6 μm × 5 6 μm and are spaced 12 6 μm apart The total detector area is approximately 1 2 mm^2

Initially, the diffusion-type detectors were expected to have higher quantum efficiencies at 490 nm, due to their shallower junctions A possible reason for their poor performance comes from analysis of the IC processing steps The diffusion areas (and wells) are created through a high-energy ion-implantation process that allows for greater precision and repeatability in processing This process damages the silicon lattice, and thereby creates generation-recombination centers that lead to signal loss (carrier recombination)

After ion-implantation, an annealing process occurs, in which the silicon wafer is held at a moderate temperature for a period of time (about 1000°C for 15 to 30 minutes), and then allowed to slowly cool This repairs some of the lattice damage done in ion implantation by thermally vibrating the atoms and allowing bonds to reform [10] The amount of lattice repair is dependent on the time and temperature of the annealing process Higher temperature and/or longer annealing time results in greater repair to the lattice This also leads to deeper diffusion of the ions into the lattice, both vertically and laterally (lateral diffusion) A great deal of lateral diffusion in the drain/source regions of transistors cannot be tolerated in a process with

sub-micron feature lengths The annealing process, and therefore the lattice repair, is limited in the p/n-diffusion regions In the creation of an n-well, however, a broad diffusion profile is intended, so greater restoration of the lattice occurs through a longer annealing This would explain the adequate performance of the n-well detectors and the inferior performance of the diffusion-type detectors

2.3 Signal Processing

2.3.1 Signal Processing Requirements

The signal processing system converts the photocurrent signal to digital form The signal processing must be compatible with the photodiode, allowing for a current input and proper biasing of the detector Low power consumption is also a priority As previously stated the main goal for this system is to be sensitive to the smallest possible signal The minimum detectable signal (MDS) in photons for a photodiode approaches a limit given by [2]

$$MDS = \frac{1}{q\ \eta}\sqrt{\frac{4 \cdot q \cdot A_{det} \cdot I_S}{T_{meas}}}\ , \qquad (2\ 13)$$

where T_{meas} is the total integration time of the measurement This equation assumes zero bias and zero dark current It also does not account for the noise of the signal processing electronics Equation 2 13 indicates that a measurement system capable of a long measurement time could be sensitive to very low levels of light

2.3.2 Basic System Topology and Operation

A signal processing system that meets these requirements is a current-to-frequency converter (CFC) The use of a CFC with a photodiode results in a light-to-frequency converter (LFC), as shown in Figure 10 Light produces a photocurrent in the detector that is collected (integrated) on the feedback capacitor of the integrator The integrator presents a low impedance to the detector and sets the detector bias As the charge collects on the feedback capacitor, the output voltage of the integrator increases at a rate (S) directly proportional to the photocurrent (I_p) and inversely proportional to the value of the integration capacitor (C_{int})

$$S = \frac{I_p}{C_{\text{int}}} \frac{V}{\text{sec}} \qquad (2\ 14)$$

The output voltage continues to increase at this rate until it reaches a value equal to the threshold voltage (V_{TH}) of the comparator When this happens, the output of the comparator goes from "low" to "high" The transition produces a pulse at the output of a monostable multivibrator ("one-shot") that resets the output of the integrator to the baseline level (V_{bias}) This series of operations continues indefinitely, producing digital pulses at a frequency dependent on the level of photocurrent

Figure 11 shows the waveforms at several points in the system The time required for the integrator output to ramp from the baseline (V_{bias}) to the threshold (V_{TH}) is equal to

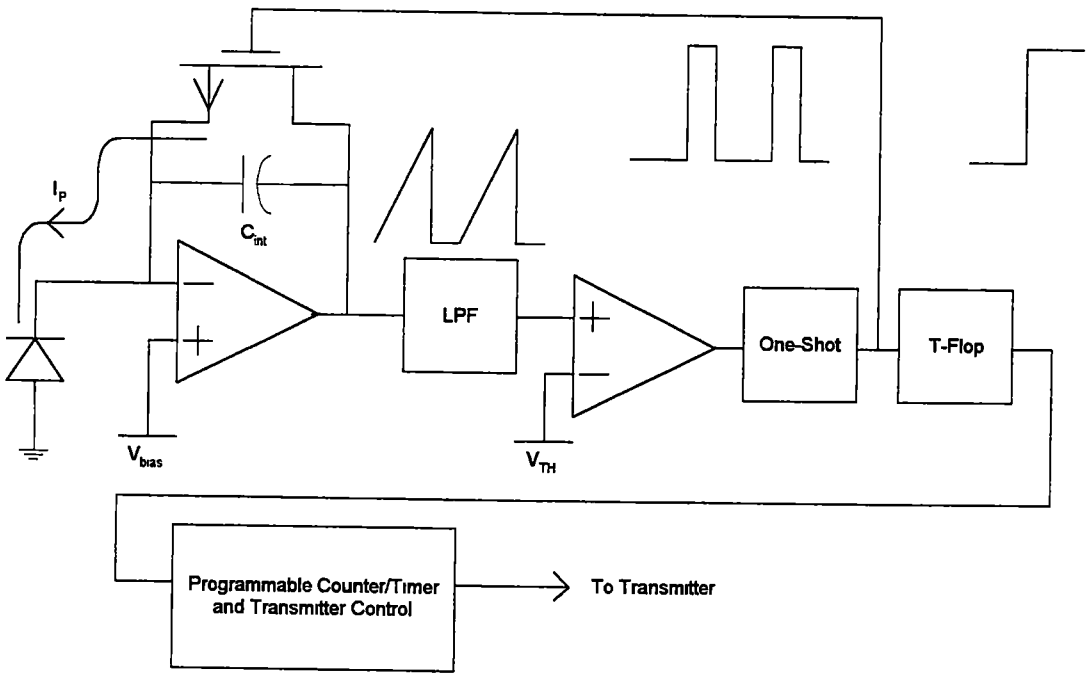

Figure 10 - Light-to-Frequency Converter

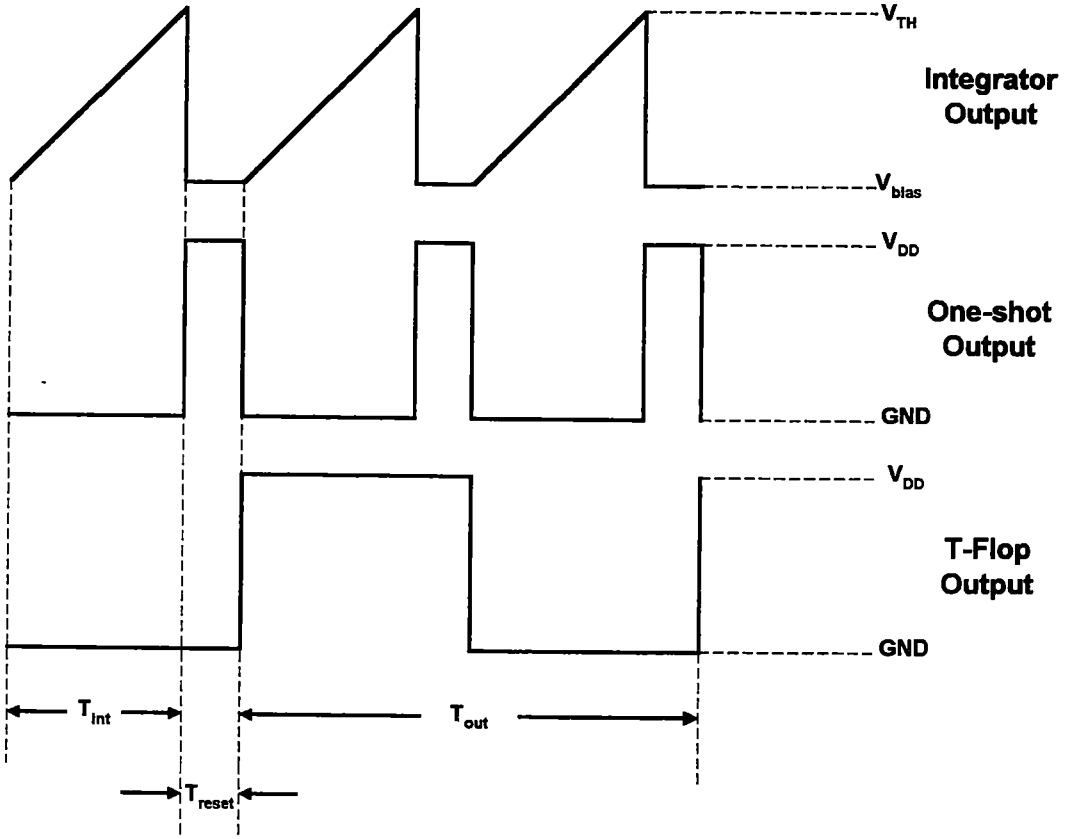

Figure 11 - System Timing

$$T_{\text{int}} = \frac{C_{\text{int}} \cdot \left(V_{TH} - V_{bias}\right)}{I_p} = \frac{V_{TH} - V_{bias}}{S} \qquad (2\ 15)$$

The pulse width of the one-shot output is equal to the reset time (T_{reset}) The period of the one-shot output (T_{os}) is equal to the sum of these two times

$$T_{os} = T_{\text{int}} + T_{reset} \qquad (2\ 16)$$

The output of the one-shot drives a D flip-flop connected as a toggle flop (T-flop) The output of the T-flop changes states only when a high-to-low transition occurs at its input The T-flop performs a frequency divide-by-two function and corrects the duty cycle to 50% for a constant photocurrent The period of the output waveform (T_{out}) is therefore twice that given by Equations 2 15 and 2 16, and its frequency is

$$f_{out} = \frac{1}{T_{out}} = \frac{1}{2 \cdot \left(T_{\text{int}} + T_{reset}\right)} = \frac{1}{2 \cdot \left[\frac{V_{TH} - V_{bias}}{S} + T_{reset}\right]} \qquad (2\ 17)$$

For the normal case in which the integration time is much longer than the reset time, Equation 2 17 reduces to

$$f_{out} = \frac{I_p}{2 \cdot C_{\text{int}} \cdot \Delta V} \quad , \qquad (2\ 18)$$

where

$$\Delta V = V_{TH} - V_{bias} \tag{2 19}$$

The output pulses are at digital logic levels and contain the sensor information via their frequency The pulses are counted by a digital counter for a set (programmable) measurement time If N pulses are counted in a measurement time (T_{meas}) then an average photocurrent level can be calculated as

$$\bar{I}_p = \frac{2 \cdot N \cdot C_{int} \cdot \Delta V}{T_{meas}} \tag{2.20}$$

The average photocurrent can then be related to an average concentration of the targeted chemical substance The pulse count at the end of the measurement interval is available in digital form at the output of the counter Digital circuitry serializes this data and sends it to the on-chip transmitter The counter is then reset for the next measurement

This signal-processing scheme performs a long-time, integrated measurement that is practically limited by such factors as the size (number of bits) of the digital counter and the lifetime of the bioreporters An averaged measurement such as this has the benefit of improved accuracy through the "averaging out" of noise An added benefit is lowered power consumption in the IC, due to the fact that it is not necessary for the transmitter to run continuously Data is only available for transmission at the

end of each measurement interval During the measurement, the transmitter can be in a low-power, or "sleep", mode Control of the transmitter mode can be achieved with additional digital circuitry This power reduction is extremely important, since the transmitter consumes an enormous amount of power, relative to the rest of the IC, when it is active

2.3.3 Signal Processing Components

The performance of the signal processing system is dependent on the performance of the individual components Measurement errors can be directly traced to non-ideal effects in these components Effects such as leakage, offset, and noise limit the sensitivity of the system to low-level signals The operation of the major system components is discussed in this section, as are their contributions to the measurement error of the system

2.3.3.1 Integrator

The integrator provides the interface between the photodiode and signal processing system The feedback of the integrator sets the bias on the photodetector and presents a low input impedance A voltage ramp waveform (Figure 11) is produced in response to input photocurrent according to the relationship in Equation 2 14 The integrator is the first stage of the processing electronics and can easily become a dominant source of error in the system Care must therefore be taken to recognize the sources of integrator error and minimize them Figure 12 shows the integrator modeled with some of its error sources and the detector bias set for 0V The reset switch is treated as a separate component and is discussed in section 2 3 3 2

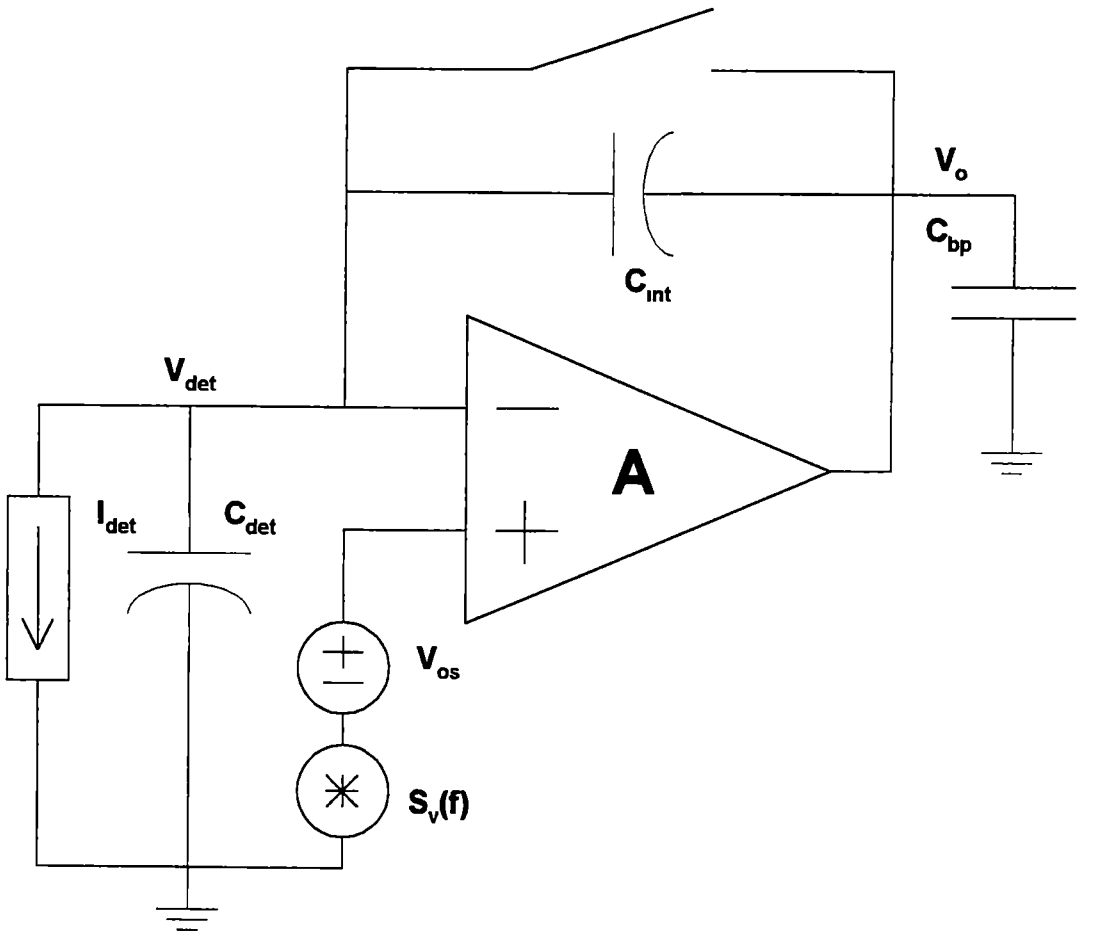

Figure 12 - Integrator with Error Sources

2.3.3.1.1 Integration Capacitor

The integrator error is mostly due to non-ideal effects in the amplifier, but the integration capacitor (C_{int}) must also be considered A common problem with integrated capacitors is linearity The simple MOS capacitor, for example, has a value that is highly voltage-dependent, as shown in Figure 13 for low frequencies The variation of capacitance with voltage is due to the fact that the bottom "plate" of the MOS capacitor(in the substrate) can be in one of three modes of operation depending on the applied gate voltage accumulation, depletion, or inversion In depletion mode, the depletion region that forms adds to the separation between the capacitor plates, decreasing the capacitance [14]

The IC capacitor structure shown in Figure 14 has improved linearity over that of the simple MOS capacitor The bottom plate of the capacitor is a highly doped area or "capwell" This technique helps to prevent the voltage coefficient problem in the simple MOS structure [15] This linearized capacitor structure is available in the HP 0 5 μm CMOS process [5] and is used to form the integration capacitor The improved structure has better linearity, but there is still the problem of a parasitic, back-plate capacitance that exists between the well and substrate (C_{bp}) Back-plate capacitance can have a value of up to 20 percent of the nominal capacitor value [10] Therefore, the feedback capacitor of the integrator is oriented with the back plate connected to the amplifier output, as shown in Figure 12 If this capacitance appeared at the input, it would contribute to the same problems that the detector capacitance causes (increased noise, etc)

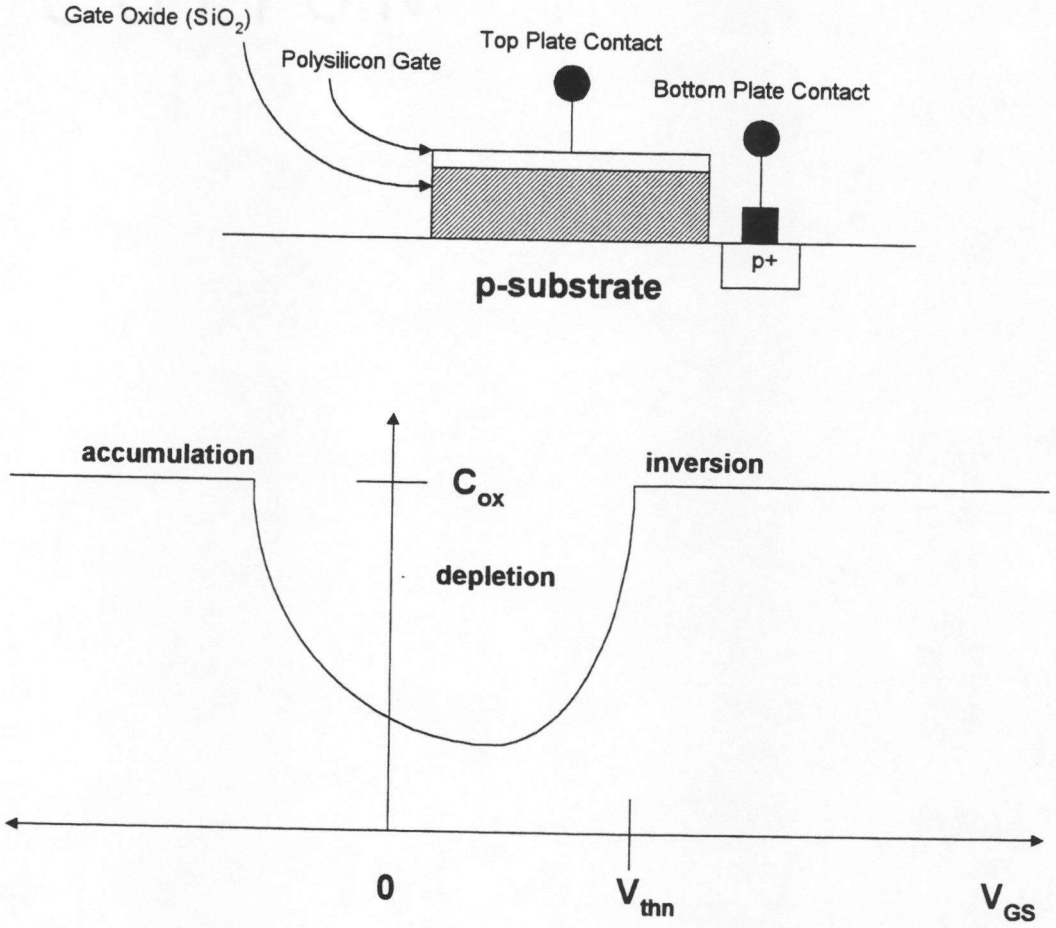

Figure 13 - Simple MOS IC Capacitor

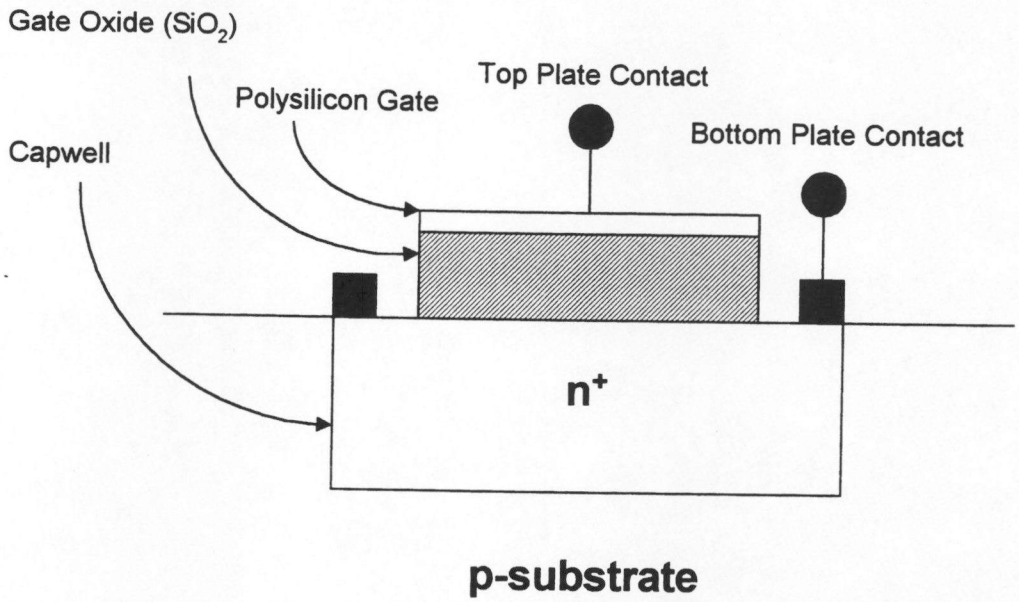

Figure 14 - Linearized IC Capacitor

2.3.3.1.2 Gain Error

One error that may result from a large input capacitance, other than increased noise, can be described as a gain error The input capacitance (C_i) is approximately equal to the sum of the detector capacitance and input capacitance of the amplifier Ideally, the integrator holds the voltage across the input capacitance equal to the voltage at its non-inverting input (0V in this case) An amplifier with a finite gain (A) actually requires the detector voltage to increase as the integrator output voltage increases

$$V_{det} = \frac{V_o}{A} \tag{2 21}$$

The change in voltage across the input causes the flow of a charging current onto the input capacitance This means that some of the detector photocurrent actually flows onto the input capacitance instead of the integration capacitor The output no longer increases at a rate given by Equation 2 14, but at a lower rate equal to

$$S_{eff} = \frac{I_p}{C_{eff}} \quad , \tag{2 22}$$

where

$$C_{eff} = \frac{C_i + C_{int} \cdot (A+1)}{A} \tag{2 23}$$

The resulting error in the integrator output pulse period is given by

$$\%error = [1 - \frac{C_{int}\ A}{C_{int} \cdot (A+1) + C_i}] \times 100\% \qquad (2\ 24)$$

This error becomes negligible as the product of the amplifier gain and integration capacitance becomes much larger than the input capacitance A large gain is required if the input capacitance is much larger than the integration capacitor, which is likely the case

The gain should also remain constant A change in gain, especially for low values of gain, will result in a change in the measured signal As the gain decreases, the slope of the integrator output decreases as given by Equations 2 22 and 2 23 The gain can change significantly due to the nonlinearity of the amplifier A drastic decrease in gain occurs if the integrator output exceeds the amplifier's dynamic range, presenting the challenge of designing a single-supply amplifier with an output dynamic range that includes 0V (described in Chapter 3) The gain can also change as a result of temperature change The temperature dependence of the amplifier gain is an important consideration for the BBIC, because it will be used as an environmental sensor This effect can, again, be made negligible if the amplifier is designed for high gain

2.3.3.1.3 Reset Error

Integrator errors can occur due to improper reset Ideally, the amplifier output is reset to the baseline (0V) before the reset switch opens The ramp waveform at the output then begins its rise from the baseline to the threshold During the time that the

reset switch is closed, the amplifier is connected in a unity-gain configuration This leads to the obvious requirement that the amplifier be unity-gain stable If the amplifier is unstable during reset, it will oscillate (or possibly saturate) If the amplifier is stable but has a poor phase margin, its transient response will exhibit excessive "ringing" when the switch closes, and integrator output may not settle before the switch opens The amplifier must, therefore, be adequately compensated to allow for a full reset

In order to analyze the stability of this system the open-loop transfer function must be known The loop transmission of the integrator during reset is approximately given by

$$T(s) = \frac{H_a(s) \cdot (1 + s \cdot R_{on} \ C_f)}{1 + s \cdot R_{on} \cdot (C_i + C_f)} \quad , \qquad (2\ 25)$$

where $H_a(s)$ is the open-loop transfer function of the amplifier and R_{on} is the on-resistance of the reset switch The amplifier transfer function is affected by loading and will be explained in more detail in chapter 3 The feedback network introduces both a pole and a zero to the loop transmission

$$f_p = \frac{1}{2 \cdot \pi \ R_{on} \cdot (C_i + C_f)} Hz \qquad (2\ 26)$$

and

$$f_z = \frac{1}{2 \cdot \pi \cdot R_{on} \cdot C_f} Hz \qquad (2\,27)$$

The pole and zero nearly cancel each other out for relatively low values of input capacitance (C_i) However, for a large input capacitance, the pole occurs at a frequency much lower than the zero frequency, producing significant phase shift This situation presents a stability against oscillations problem, since the system will oscillate if the phase shift around the loop reaches 180 degrees at a frequency where the magnitude of the transfer function is greater than one [9] Luckily, the value of R_{on} should be relatively small, and both the pole and zero should occur at relatively high frequencies If the bandwidth of the amplifier can be held much lower than these frequencies, their effect will be negligible The stability analysis will be carried out further in Chapter 3

A large-signal, transient effect can also occur during reset Just before the reset switch closes, the output of the integrator is at the threshold voltage (V_{TH}) Just after the switch closes, the output voltage is applied to the input capacitance through the on-resistance of the switch This fast voltage change on a large capacitance can result in the flow of a large charging current from the amplifier output If the charging current required is more than that available at the amplifier's output, the amplifier is pulled out of linear operation toward the lower supply rail Feedback then slowly pulls the system back to linear operation, and the output settles to its final value This 'slewing" effect can take a great deal more time than any ringing in the small-signal,

linear response If the reset switch opens during this time, integration will begin while the amplifier is in a low-gain state (gain error) The output voltage will then ramp upward until linear operation is restored Both this effect and small-signal ringing increase the required reset time, limiting the maximum frequency of the system operation and the upper limit of the sensor's dynamic range

2.3.3.1.4 Amplifier Offset Voltage

The offset voltage of the amplifier is modeled as the voltage V_{os} in Figure 12 The offset voltage is the differential voltage that must be applied to the amplifier's input to bring the output to zero [16] The polarity of the offset, though shown in Figure 12, is not known for from one amplifier to the next Offset voltage has two components random offset and systematic offset Random offset is due to random mismatches in devices, which can be reduced through proper layout Systematic offset is an offset inherent in the amplifier design This type of error is removed through careful design [10]

The offset voltage presents an error, because there is an unintentional bias on the detector It is intended to put a zero bias on the detector in the BBIC for low leakage, so this error must be considered The offset voltage also results in a shift in the baseline of the integrator output, which leads to a measurement error in the average photocurrent (Equations 2 19, 2 20) If this error remains constant, it can be calibrated out of the measurement However, the offset voltage changes, or "drifts", with temperature, resulting in an error similar to that produced by low-frequency

noise. Offset cancellation techniques, such as autozeroing, have been used effectively [17], but are limited by errors from the switching involved

2.3.3.1.5 Amplifier Noise

The intrinsic noise of the amplifier is modeled as $S_v(f)$ in Figure 12 This voltage source is an equivalent, input-referred noise voltage spectrum An input current noise current due to gate leakage can also be modeled, but it is usually negligible in CMOS [10] at low frequencies The noise spectral density of the amplifier has two main components white thermal noise with a flat spectrum and flicker noise with a spectrum that varies inversely with frequency The composite spectrum can be represented as

$$S_v(f) = E_{th}^2 \cdot (1 + \frac{f_c}{f}) \frac{V^2}{Hz} \quad , \tag{2 28}$$

where E_{th}^2 is the thermal noise power, and f_c is the flicker noise corner frequency The corner frequency is the frequency at which the white noise power spectral density is equal to that of the flicker noise power

The intrinsic noise of the amplifier and detector cause random voltage variations at the output of the integrator, resulting in random variations in the output pulse period A large input capacitance, as previously mentioned, amplifies this problem The averaging involved in this system, however, reduces the error The time-variant nature of this system leads to a complicated noise analysis This analysis is reserved for Section 2 4

2.3.3.2 Reset Switch

The switch is implemented with a single NMOS transistor, as shown in Figure 15 The gate voltage controls the operation of the switch When the gate voltage is high, the gate-source voltage is above the threshold voltage of the device, and the transistor is in the deep ohmic region The on-resistance of the switch is given by [10]

$$R_{on} = \frac{1}{\mu_n \cdot C_{ox} \cdot (\frac{W}{L}) \cdot (V_{GS} - V_T)} \quad , \tag{2 29}$$

where W and L are the effective gate width and length respectively, C_{ox} is the gate oxide capacitance per unit area, V_{GS} is the gate-source voltage, and V_T is the threshold voltage of the device The switch provides a discharge path for the integration capacitor, resetting the integrator output When the gate voltage is low, the transistor is in the deep subthreshold region, and the switch is effectively turned off Two important errors that occur in the simple MOS switch are charge injection and leakage

2.3.3.2.1 Charge Injection

Charge injection error is an offset that occurs when a MOS switch is opened Charge injection actually occurs in two phases During the first phase, the gate voltage is above the threshold voltage, and a channel charge exists When the switch is on, there is no voltage between the drain and source, and the channel charge is equal to [10]

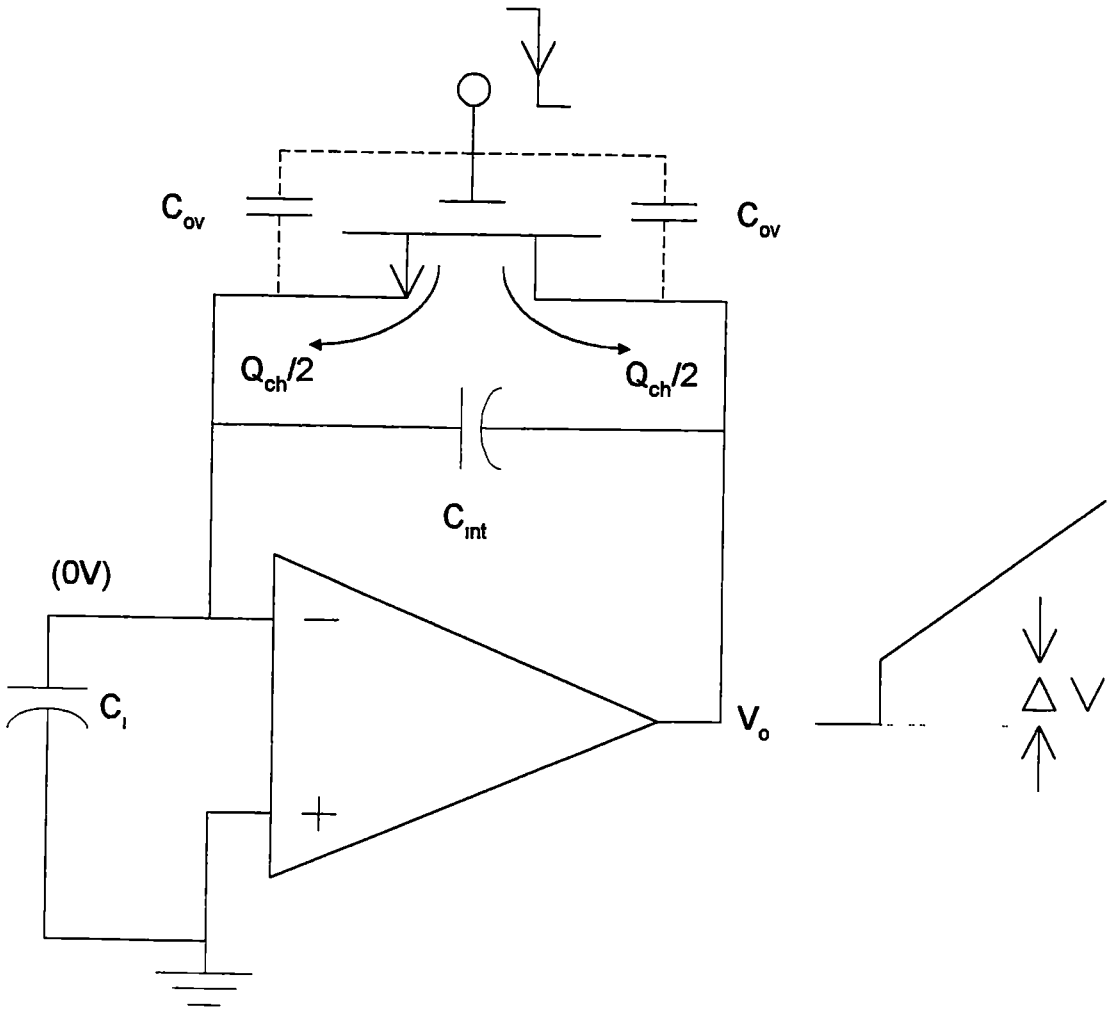

Figure 15 - Charge Injection Error

$$|Q_{CH}| = W \cdot L \cdot C_{ox} \cdot (V_{GS} - V_T) \tag{2 30}$$

This charge is negative for an NMOS switch As the switch is being turned off, the gate voltage falls, and the channel charge exits the device If the transistor is switched quickly, this charge splits evenly between both drain/source terminals [18] as shown in Figure 15. The charge that flows to the output of the amplifier has little effect, but the charge that flows to the input is collected on the integration capacitor, producing an offset voltage at the output equal to

$$\Delta V_{o_1} = \frac{|Q_{CH}|}{2 \cdot C_{\text{int}}} \tag{2 31}$$

The expelling of channel charge is usually the dominant charge injection effect

When the gate voltage falls below the threshold voltage, the channel charge has been expelled, but an error still occurs through the gate-diffusion overlap capacitance (C_{ov}) of the transistor shown in Figure 15 The falling gate voltage is coupled to the integrator through this capacitance, producing an additional offset If feedback holds the integrator input at baseline voltage, this offset is equal to

$$\Delta V_{o_2} = \frac{C_{ov} \cdot \Delta V_{sw}}{C_{\text{int}}} \quad , \tag{2 32}$$

where ΔV_{sw} is the voltage difference between the maximum and minimum values of the switching voltage at the gate The two offsets add to produce the offset voltage

error shown in Figure 15

Several techniques can be used to reduce charge injection error Equations 2 30 and 2 31 show that the offset can be reduced by using a small-area switch transistor, switching the transistor with a low-amplitude control signal, and using a large integration capacitor An additional technique involves the switching speed . If the gate of the transistor is switched at a slower rate, the channel charge will not exit equally through the two ends of the switch [18]. This property can be used to reduce the charge that flows onto the integration capacitor. Other common techniques are the use of a "dummy transistor", as described in [19], or a complementary CMOS switch that provides partial charge cancellation More drastic measures, such as active charge-injection compensation [20], are even possible Fortunately, the offset due to charge injection should remain signal-independent in this case, because the source voltage of the switch transistor is held constant through feedback This offset can be calibrated out of the measurement if it remains constant

2.3.3.2.2 Switch Leakage

Switch leakage is the current that flows in the switch when turned off As shown in Figure 16, the switch leakage current subtracts from the detector current This presents a serious problem when trying to detect low levels of photocurrent The switch leakage is a combination of subthreshold current, surface leakage current, and even package leakage current [19] Subthreshold current will be the primary focus A MOS switch in the off condition can be modeled as being in the deep subthreshold region of operation The drain current of a MOS transistor in weak inversion

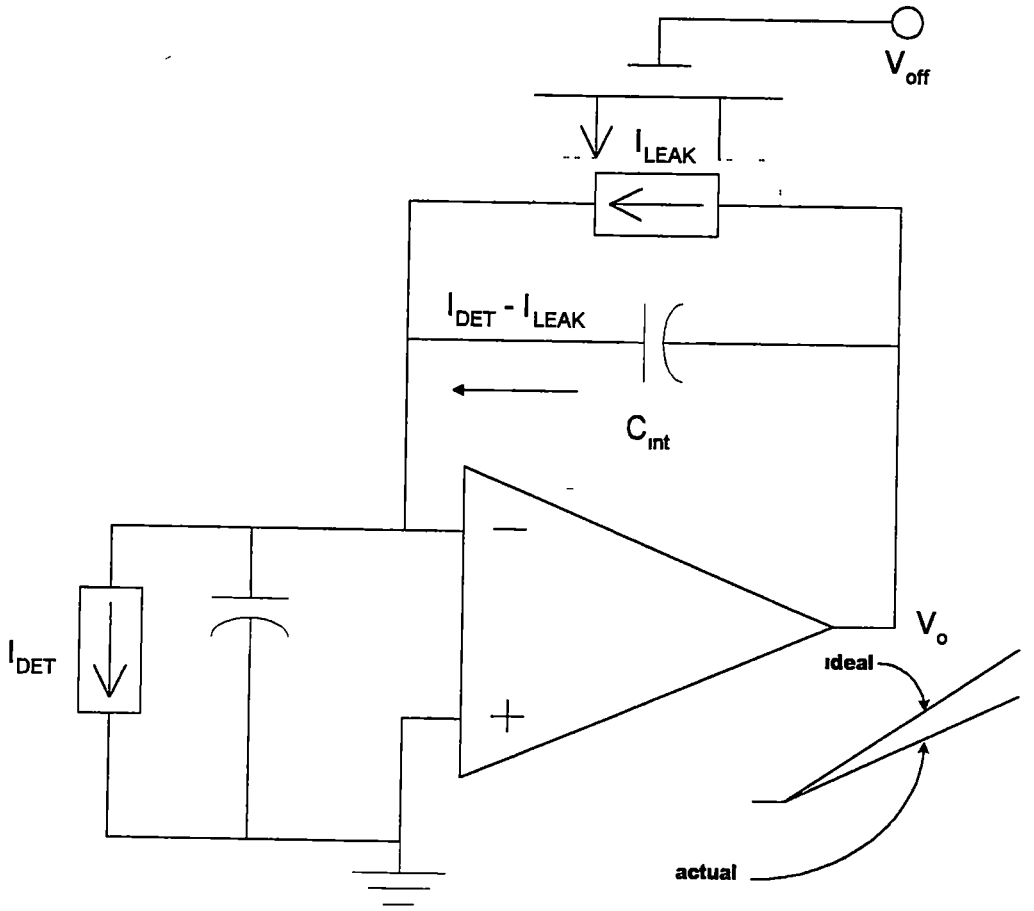

Figure 16 - Switch Leakage Error

(subthreshold) is given by [21]

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{V_{GS}-V_T}{nV_t}} \cdot \left(1 - e^{\frac{-V_{DS}}{V_t}}\right) \quad , \tag{2.33}$$

where I_{D0} is a process-dependent (and temperature-dependent) coefficient, and n is given by [21]

$$n = \frac{C_{ox} + C_{depl}}{C_{ox}} \approx 1.5 \quad , \tag{2.34}$$

where C_{depl} is the depletion capacitance. For a drain-source voltage above a few thermal voltages (about 75mV at room temperature), Equation 2.32 reduces to

$$I_D \approx I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{V_{GS}-V_T}{nV_t}} \tag{2.35}$$

The subthreshold drain current of (2.35) seems to have no dependence on drain-source voltage. For short-channel devices, this is far from true. In short-channel devices, the drain bias interacts with the gate bias by lowering the barrier potential between the source and body regions [21]. This effect, known as Drain Induced Barrier Lowering (DIBL), lowers the threshold voltage of the device as the drain-source voltage increases. The decrease in threshold voltage results in an increase in drain current (switch leakage). It can be shown [21] that the DIBL contribution to the output impedance is exponentially related to the drain voltage. The DIBL effect

becomes more pronounced as the effective gate length decreases [22]

Switch leakage is affected by several factors Increasing temperature increases the leakage current The leakage, as reported in [19], doubles for every 8°C increase in temperature This increase is partly due to the diffusion-to-body leakage, which approximately doubles for every 5°C increase Switch leakage also increases with the drain-source voltage of the transistor, due the DIBL effect From (2 33) the subthreshold current becomes zero for zero drain-source voltage In this application, however, the drain voltage of the NMOS switch increases as the detector current is integrated Increasing the gate length of the switch device can reduce the effects of subthreshold current This solution, however, is in opposition to the considerations for low charge injection

2.3.3.3 Low-pass Filter

The output of the integrator passes through a low-pass filter before it reaches the comparator The purpose of the filter is to remove some of the noise due to the integrator and detector at higher frequencies The simple R-C low-pass filter is shown in Figure 17 The diode is present to provide a fast discharge path for the capacitor during reset This filter produces a single-pole response given by

$$H_{filter}(s) = \frac{1}{1 + s \cdot R_{filter} \cdot C_{filter}} \qquad (2\ 36)$$

The bandwidth of the filter should be low to filter out as much noise as possible (but not low enough to distort the integrator output)

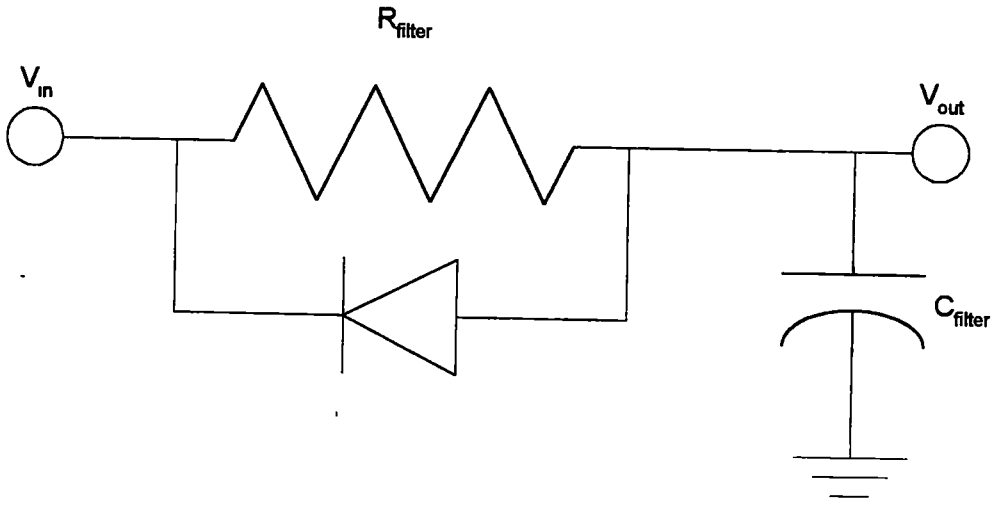

Figure 17 - Low-pass Filter

2.3.3.4 Comparator

The comparator can be simply described as a high-gain amplifier that intentionally saturates, thereby detecting whether one of its input voltages is higher or lower than the other The comparator in this system produces a high output voltage when the integrator output reaches the threshold voltage As previously discussed, this transition causes the system to reset Two main sources of error in the comparator are intrinsic noise and offset These errors can be modeled as they were for the amplifier in the integrator (Figure 12) The offset voltage for a comparator is simply the input differential voltage, ideally zero, at which an output transition occurs Both the offset voltage and noise of the comparator affect the system timing The comparator ideally causes the reset to occur exactly when the integrator output reaches the threshold Noise causes random fluctuations in the reset transition time The offset voltage causes a timing offset that can drift with temperature as the offset voltage drifts The timing errors are imposed on the integration time T_{int} in Figure 11, resulting in error in the measurement

2.3.3.5 One-shot

The one-shot produces the pulse that resets the system The width of the pulse is controllable by some design parameter In the case of the one-shot used in this system, the pulse width is adjustable by the bias current, more current producing a longer pulse width The reset time should be negligible when compared with the integration time, so the performance requirements of the one-shot should not be as stringent as those for the other system components

2.3.3.6 Toggle Flop

The toggle flop performs a frequency division of the one-shot output signal, as previously discussed The toggle is a simple D flip-flop connected as shown in Figure 18 The logic level present at the D input is clocked to the Q output when a high-to-low transition (from the one-shot) occurs at the CLK input The level at the "Q-bar" output, which is fed back to the D input, becomes the opposite logic of the D input The result is that the Q output only changes states on the falling edge of the one-shot output This produces a signal at one half of the frequency and with a 50% duty cycle The toggle-flop output produces the pulses that are counted by the digital counter

2.3.3.7 Counter and Other Digital Circuitry

The counter and other digital circuits beyond the toggle-flop in the system were described in section 2 3 2 The design of these components can be accomplished through the use of a digital hardware description language such as VHDL The functions of the various circuits can be translated to VHDL code A synthesis program can then be used to convert this code to a form that may be used to generate the actual digital functions VHDL synthesis is commonly used to program field-programmable gate arrays (FPGA) An FPGA is a chip containing a large matrix of basic digital gates (such as AND, OR, and NOT functions), with programmable interconnects When the FPGA is programmed, the basic gates are connected in such a way to implement the desired logic function (combinational logic, state-machine, etc) VHDL synthesis can also be used to generate an actual IC layout of the digital system, using standard-cell digital circuit layouts as building blocks This method is

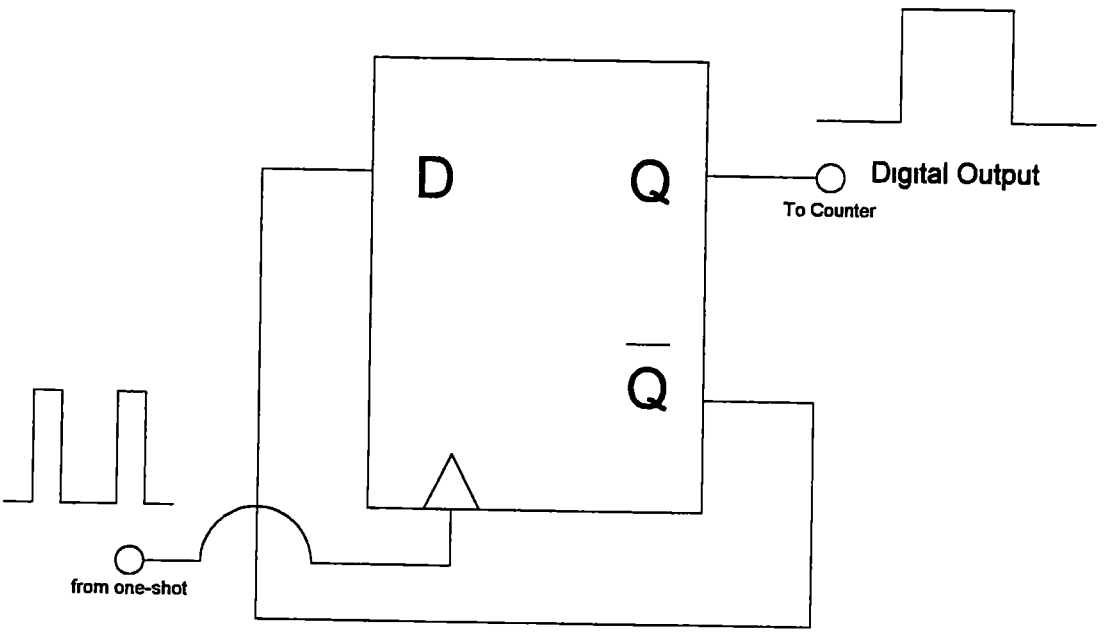

Figure 18 - Frequency Divider

very efficient in terms of design time, and synthesis programs can even be used to maximize the layout area efficiency of the design

2.4 System Noise Analysis

The accuracy of the measurement is dependent on the accuracy of the system timing, as described in Equations 2 14 through 2 20 Intrinsic noise in the system devices is translated into a timing jitter, thereby producing a random error in the measurement The noise analysis of this system is complicated by several factors First, the current-to-frequency converter is an oscillator, and the time-variant nature of the system requires a time-domain analysis of the noise Second, this microluminometer is a sampled system The pulse width of each of the output digital pulses can be thought of as a sample of the average pulse width over the measurement interval Also, the system naturally performs a sampling of the amplifier noise that is similar to an "autozeroing" function (to be discussed later). Finally, the use of CMOS technology has its benefits, but one of the definite penalties for using MOS devices is an increased level of 1/f noise over that found in bipolar transistors This low-frequency noise complicates the analysis considerably due to its long-term memory, or autocorrelation Flicker noise presents a mathematical difficulty, particularly due to the fact that it represents infinite power at zero frequency (DC) Due to this difficulty, the following analysis will be separated into two main sections, the first discussing the effects of white noise and the second discussing 1/f noise The analysis in the second section will not be carried out quite as thoroughly as that in the first because of the

mathematical complexity Also, the system analysis will be limited to the effects of the detector and amplifier noise Further, it will be assumed that the system noise is ergodic, so that ensemble averages are equivalent to time averages The main purpose of this analysis is to determine, at least qualitatively, how the various system parameters affect noise performance

2.4.1 White Noise Analysis

2.4.1.1 Detector Noise

Figure 19 shows the photodetector, modeled with a shunt noise current, and the switched integrator The detector bias, which is also the baseline level, is set to 0V Excluding all sources of error, the time needed for the integrator output to ramp from the baseline to the threshold voltage of the comparator (V_{TH}) is equal to

$$T = \frac{C_{\text{int}} \cdot V_{TH}}{I_p} \tag{2 37}$$

for a constant photocurrent, I_p In order to quantify the effect of detector noise on the measurement, one must determine how noise causes variations from the ideal result of Equation 2 37

The noise current of the detector is integrated along with the signal current, producing random voltage fluctuations at the output of the integrator These voltage fluctuations produce an uncertainty in the time at which the output level reaches the comparator threshold, as shown in Figure 20 The statistics of the output voltage noise

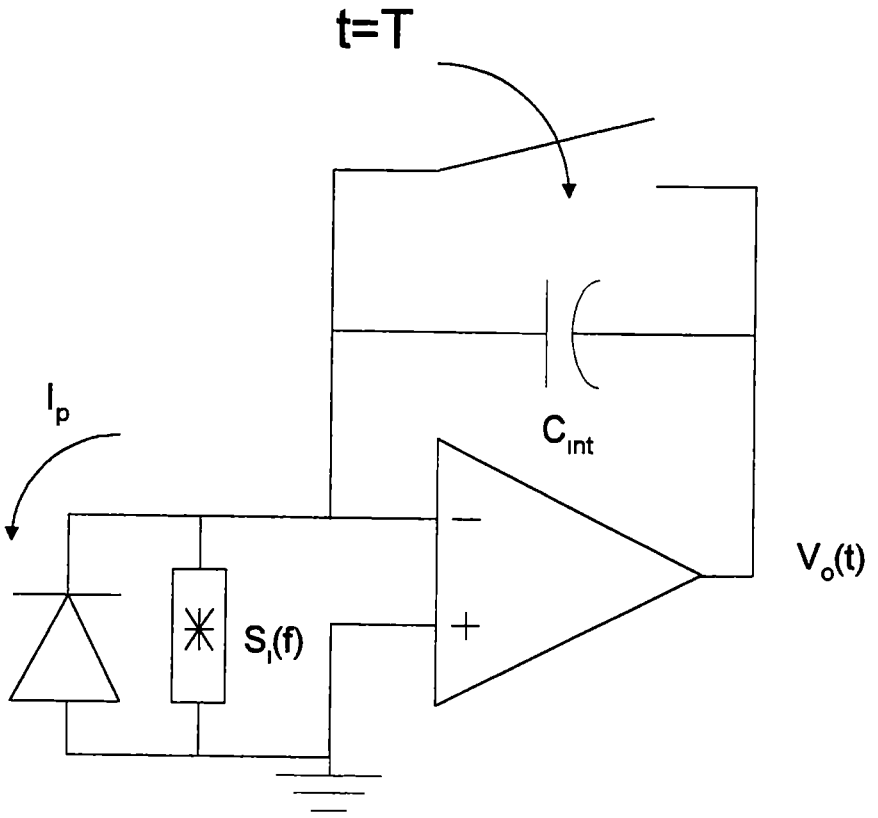

Figure 19 – Switched Integrator with Detector Noise

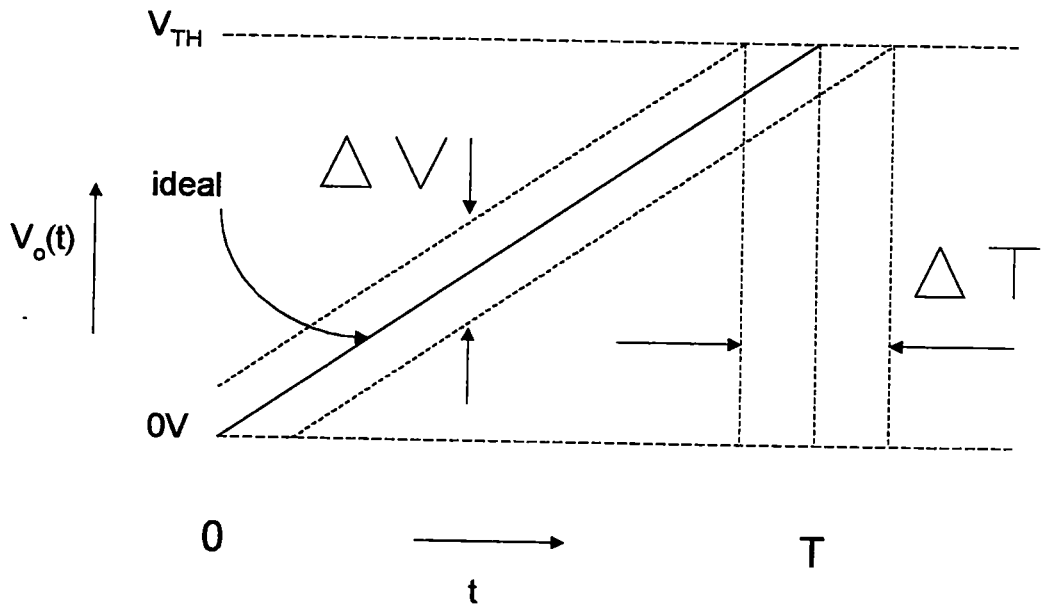

Figure 20 – Translation of Voltage Noise to Timing Jitter

change with time in this system The mean-squared value of the output voltage noise (not the output voltage), due to the shot noise (white) of the detector, at a time, t, can be derived for this switched system using the results presented in [23].

$$\overline{V_{no}^2(t)} = 2 \cdot \int_0^t h(v) \cdot \left[\int_0^v h(u) \cdot \frac{I_{shot}^2}{2} \cdot \delta(u - v) du \right] dv \qquad (2\ 38)$$

In this equation, the one-sided shot noise power spectral density of Equation 2 10 (zero detector bias) is used The function $\delta(t)$ denotes the impulse function The function $h(t)$ is the impulse response of the system during the integration phase of operation, which is given by

$$h(t) = \frac{1}{C_{int}} \quad , \qquad (2\ 39)$$

for a causal system Assuming a zero-mean random process, the mean-squared value equals the variance [24] The variance of the output voltage noise at a time, T, is therefore obtained from Equation 2 38 as

$$\overline{V_{no}^2(T)} = \sigma_v^2(T) = \frac{I_{shot}^2 \cdot T}{2 \cdot C_{int}^2} \qquad (2\ 40)$$

This result can be made more general by adding the effect of a low-pass filter to the impulse response given in Equation 2 40 The filter has negligible effect, however, if the integration time is much larger than the time constant of the filter

The next step in this analysis is to relate the output voltage noise to a timing jitter The variance in the integration time is related to the voltage variance by [25]

$$\sigma_t^2 = \frac{\sigma_v^2}{\left|\overline{\frac{dV_o(t)}{dt}}\right|^2} = \frac{\sigma_v^2}{S^2} = (\frac{T}{V_{TH}})^2 \cdot \sigma_v^2 \quad , \tag{2 41}$$

where T, is defined by Equation 2 37 In determining a signal-to-noise ratio, it is necessary to know the variation in the reciprocal of the integration time This reciprocal represents a rate, and the ideal integration rate is given by

$$R = \frac{1}{T} \tag{2 42}$$

The variance in the rate can be related to the variance in the integration time in the same way that timing jitter was derived from voltage noise (although in this case it is an approximation [25]) The result of this analysis is the variance in the integration rate

$$\sigma_r^2 \cong \frac{\sigma_t^2}{T^4} = \frac{\sigma_v^2}{T^2 \cdot V_{TH}^2} \tag{2 43}$$

At this point in the analysis, it should be noted that the final measurement is an integrated measurement Pulses are counted over a set amount of time, and an average pulse rate is determined The uncertainty in this average is the uncertainty in the final

system measurement As previously explained, the counting of a pulse can be thought of as taking a sample of the average pulse rate When only considering the effects of detector shot noise, the assumption may be made that these samples are statistically independent White noise is highly uncorrelated, so the instantaneous values of the integrator output noise voltage between system resets are independent (uncorrelated) If a number of pulses, N, are counted, and these N "samples" are statistically independent, then the variance in the sample mean of the integration rate is given by

$$\sigma_{\hat{r}}^2 = \frac{\sigma_r^2}{N} \tag{2 44}$$

A signal-to-noise ratio can now be defined as

$$SNR = \frac{R^2}{\sigma_{\hat{r}}^2} \tag{2 45}$$

After various substitutions, the signal-to-noise ratio can be expressed as

$$SNR = \frac{2 \cdot N \cdot I_p \ C_{\text{int}} \cdot V_{TH}}{I_{shot}^2} = \frac{N \cdot I_p \ C_{\text{int}} \cdot V_{TH}}{q \cdot (2 \cdot I_S + I_p)} \tag{2 46}$$

If the total measurement time is approximated as

$$T_{meas} = N \ T \quad , \tag{2 47}$$

then the signal-to-noise ratio can be expressed as

$$SNR = \frac{2\ I_p^2 \cdot T_{meas}}{I_{shot}^2} \qquad (2\ 48)$$

This same result is reached if the system is analyzed as a non-switched integrator with integration time, T_{meas} [26]

The results of this analysis are not surprising The accuracy of the measurement is improved by increasing the measurement time The signal-to-noise ratio was shown to be directly proportional to the values of N, C_{int}, and V_{TH} The value of N is limited by the number of bits in the digital system counter, which is constrained by chip area Also, the timer, which actually sets the measurement time, has the same area constraint The value of C_{int} is also limited by size The comparator threshold voltage, V_{TH}, is limited by voltage "headroom" These physical limitations notwithstanding, there is a practical limit on measurement time One problem encountered with long-time measurements is that factors such as temperature (which affects the measurement) can vary a great deal from the beginning to the end of the measurement Also, there is a finite amount of time that one is willing to wait for the measurement results

2.4.1.2 Amplifier Voltage Noise

Analysis of the effect of amplifier voltage noise is complicated by the sampling action that occurs during system reset This action is illustrated in Figure 21 At first, the amplifier will be assumed ideal (except for noise) If the reset switch

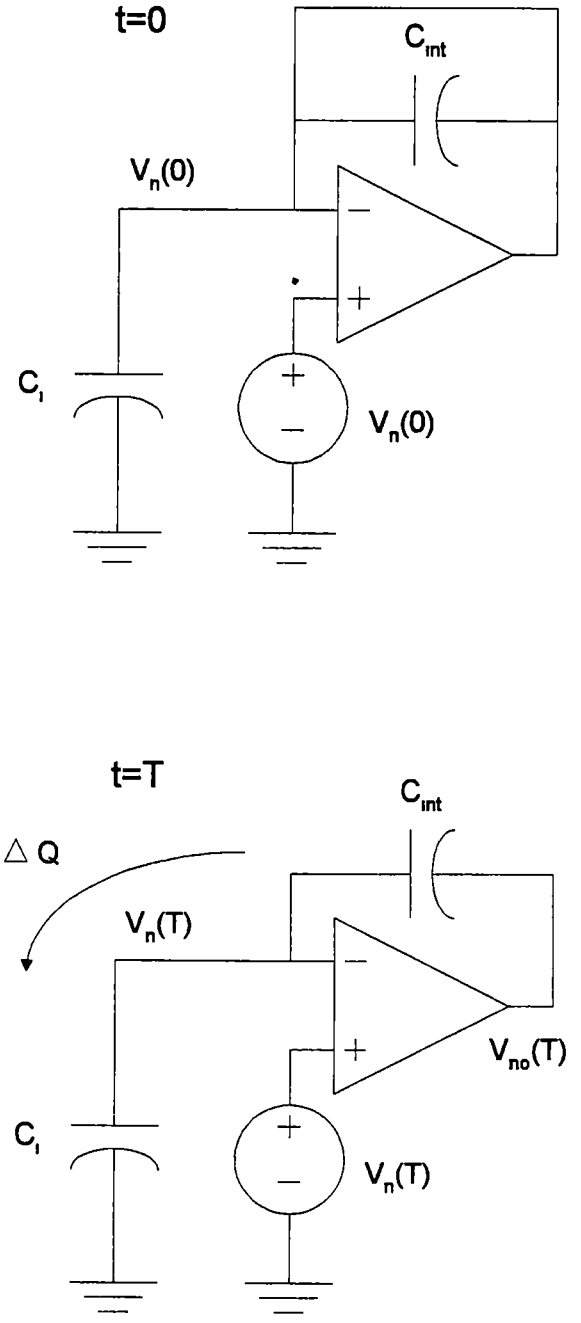

Figure 21 – Noise Sampling During Reset

opens at time, t=0, the instantaneous value of the amplifier noise at t=0 ($V_n(0)$) is sampled onto the input capacitance, C_i Neglecting any leakage, this voltage is held at the input until the next system reset The deviation of the instantaneous noise voltage from this initial value is amplified to the output by a capacitance ratio The instantaneous value of the output noise voltage at time T after reset can be expressed as

$$V_{no}(T) = V_n(0) + (1 + \frac{C_i}{C_{int}}) \cdot [V_n(T) - V_n(0)] \tag{2 49}$$

Equation 2 49 may be rewritten as

$$V_{no}(T) = (1 + \frac{C_i}{C_{int}})\ V_n(T) - (\frac{C_i}{C_{int}}) \cdot V_n(0) \tag{2 50}$$

The mean-squared value of $V_{no}(T)$, in the ensemble sense, is given by [24]

$$\overline{V_{no}^2(T)} = \lim_{k \to \infty} \left\{ \frac{1}{k} \sum_{i=1}^{k} [V_{no}^2(T)]_i \right\} \tag{2 51}$$

The product inside the summation can be expanded as follows

$$V_{no}^2(T) = (1 + \frac{C_i}{C_{int}})^2 \cdot V_n^2(T) - 2 \cdot (1 + \frac{C_i}{C_{int}}) \cdot (\frac{C_i}{C_{int}})\ V_n(T) \cdot V_n(0) + (\frac{C_i}{C_{int}})^2 \cdot V_n^2(0) \tag{2 52}$$

The second term above corresponds to the autocorrelation of the random process when

substituted back into Equation 2 51 As previously stated, white noise is highly uncorrelated, so the second term in Equation 2 52 can be omitted in this analysis The ensemble average of the integrator output voltage noise at time T can now be written as

$$\overline{V_{no}^2(T)} = (1+\frac{C_i}{C_{int}})^2 \cdot \overline{V_n^2(T)} + (\frac{C_i}{C_{int}})^2 \cdot \overline{V_n^2(0)} \qquad (2\ 53)$$

The two mean-squared values on the right side of Equation 2 51 are calculated as follows

$$\overline{V_n^2(0)} = E_{th}^2 \cdot \Delta f_1 \quad \text{and} \qquad (2\ 54)$$

$$\overline{V_n^2(T)} = E_{th}^2 \ \Delta f_2 \quad , \qquad (2\ 55)$$

where Δf_1 is the noise bandwidth during reset, and Δf_2 is the noise bandwidth during integration The term E_{th}^2 is the one –sided power spectral density of the amplifier thermal noise (Equation 2.28)

Following the same analysis procedures presented in section 2 4.1 1, the signal-to-noise ratio (considering only amplifier thermal noise) is equal to

$$SNR = \frac{N \cdot (V_{TH} \cdot C_{int})^2}{(C_i + C_{int})^2 \cdot E_{th}^2 \cdot \Delta f_2 + C_i^2 \ E_{th}^2 \ \Delta f_1} \quad , \qquad (2\ 56)$$

or

$$SNR = \frac{(I_p \cdot V_{TH} \cdot C_{\text{int}}) \cdot T_{meas}}{(C_i + C_{\text{int}})^2 \cdot E_{th}^2 \cdot \Delta f_2 + C_i^2 \cdot E_{th}^2 \cdot \Delta f_1} \quad (2\ 57)$$

Again, accuracy is improved by longer measurement time In addition, the input capacitance of the integrator should be minimized The input capacitance is reduced by reducing the area of both the detector and amplifier input devices Both of these actions, however, carry a penalty Reducing the detector area makes detecting low levels of light increasingly difficult Using a parallel grid of small detectors, as described in section 2 2 4 1, is a compromise in this situation. Reducing the amplifier device sizes reduces input capacitance, but also increases the amount of flicker noise produced by the amplifier There is an optimization in this situation that will be discussed in Chapter 3 Finally, the amplifier bandwidth should be held as low as possible The amplifier bandwidth can be limited by reducing its current Reduced current, however, results in an increase in thermal noise Bandwidth can also be limited by a large compensation capacitance Not only is this solution limited by chip area, but the combination of low amplifier current and large compensation capacitance leads to a slewing problem during reset

2.4.1.3 Combined White Noise Analysis

Both the detector current noise and amplifier voltage noise produces voltage noise at the output of the integrator The noise powers (mean-squared values) produced by these two sources can be added directly by superposition A white noise analysis including both detector and amplifier noise begins by adding these mean-

squared values, given by Equations 2 40 and 2 53 A combined signal-to-noise ratio is then derived in the same way that the individual SNR's were derived This analysis gives the following result

$$SNR = \frac{N \cdot (C_{\text{int}}\ V_{TH})^2}{q \cdot (2 \cdot \frac{I_S}{I_p} + 1) \cdot (C_{\text{int}} \cdot V_{TH}) + E_{th}^2 \cdot \left[(C_i + C_{\text{int}})^2 \cdot \Delta f_2 + C_i^2 \cdot \Delta f_1 \right]} \qquad (2\ 58)$$

Here, Equation 2 10 (zero-bias detector shot noise) was used This result suggests the same procedures for improving system accuracy that the individual analyses suggested It should be noted that the noise of the reset switch was neglected in this analysis

2.4.2 1/f Noise Analysis

The following analysis will be limited in comparison to that for white noise The simplification of the analysis is partly due to the fact that the effect of averaging on the flicker noise measurement error is not straightforward Flicker noise remains correlated for long periods of time, so that not all sample pulse periods are statistically independent The simple relationship in Equation 2 44, therefore, cannot be used In general, the variance of the sample mean of a random variable, X, is given by [24]

$$\sigma_{\hat{\bar{X}}}^2 = \frac{1}{N^2} \cdot \sum_{i=1}^{N} \sum_{j=1}^{N} (\overline{X_i\ X_j}) - (\overline{X})^2 \quad , \qquad (2\ 59)$$

for N samples If this random variable has zero mean and the samples are separated in time by a constant interval, Δt, then Equation 2 59 can be written as

$$\sigma_{\hat{\bar{X}}}^2 = \frac{1}{N^2} \cdot \left\{ N \cdot \overline{X^2} + \sum_{i=1}^{N-1} 2 \cdot i \cdot \Phi_X [(N-i) \cdot \Delta t] \right\} \quad , \tag{2 60}$$

where Φ_X denotes the autocorrelation function of the random process Note that if the autocorrelation is allowed to go to zero, the simple result for white noise results In the subsequent analyses, averaging will not be considered It will be assumed that the system is at rest before the switch opens at t=0, and only the statistics of a single pulse will be analyzed

2.4.2.1 Detector Noise

Instead of using the transient relationship of Equation 2 38, the detector flicker noise may be translated into an output voltage noise through frequency-domain analysis Time dependence can be introduced into the analysis by assuming that the low limit of the measurement bandwidth is equal to the reciprocal of the time that the system has been "turned on" Assuming that the system was at rest before time t=0 and considering only one pulse, the "on time" of the system is equal to one pulse period (T), as ideally given by Equation 2 37 The mean-squared value of the integrator output voltage at time, T, after t=0 is then ideally given by [25]

$$\overline{V_{no}^2(T)} = \frac{1}{2 \cdot \pi} \int_{\frac{1}{T}}^{\infty} S_i(\omega) \cdot H(j\omega) \cdot H(-j \cdot \omega) d\omega \quad , \tag{2 61}$$

where J is the complex variable, ω is radian frequency, $H(J\omega)$ is the transfer function of the ideal integrator, and $S_i(\omega)$ is the one-sided power spectral density of the detector current noise The transfer function is given by

$$H(J\cdot\omega)=\frac{1}{J\cdot\omega\cdot C_{\text{int}}} \tag{2 62}$$

The one-sided noise spectral density, considering only flicker noise, is given in Equation 2 12 If the exponent, a, is set equal to one, then

$$I^2_{flicker}=\frac{K\cdot I_p}{2\cdot\pi}\frac{A^2}{\omega\, rad}\quad , \tag{2 63}$$

neglecting any leakage current It should be noted that the response of a physically realizable integrator deviates greatly from the ideal, as the integration time becomes longer The actual integrator output voltage varies exponentially with time for a constant current input (instead of having a constant slope) With this adjustment, the resulting mean-squared voltage noise at $t=T$ is

$$\overline{V^2_{no}(T)}=\frac{K\cdot I_p\cdot T^2}{4\cdot C^2_{\text{int}}} \tag{2 64}$$

The signal-to-noise ratio must now be redefined as

$$SNR=\frac{R^2}{\sigma_r^2}\quad , \tag{2 65}$$

since there is no averaging Following the same procedure as that in the previous analyses gives

$$SNR = \frac{4\ I_p}{K} \tag{2 66}$$

This simple result only states the obvious the level of photocurrent should be maximized, and the accuracy is inversely proportional to the flicker noise level

Adding a high-frequency limit, ω_h, to the system represents a more realistic situation The resulting mean-squared noise voltage is

$$\overline{V_{no}^2(T)} = \frac{K \cdot I_p \cdot T^2}{4 \cdot C_{\text{int}}^2} - \frac{K \cdot I_p}{4 \cdot \omega_h^2 \cdot C_{\text{int}}^2} \quad , \tag{2 67}$$

and

$$SNR = \frac{4 \cdot I_p T^2}{K \cdot \left[T^2 - \frac{1}{\omega_h^2} \right]} \tag{2 68}$$

Equation 2 68 suggests that the signal-to-noise ratio is not improved significantly unless the upper bandwidth limit is made comparable to the reciprocal of the integration time This situation is not physically realizable on-chip for any significant integration time

2.4.2.2 Amplifier Voltage Noise

The analysis of the amplifier flicker noise is similar to that presented for the amplifier white noise One difference is that the autocorrelation of the voltage noise, Φ_{Vn}, cannot be neglected

$$\overline{V_{no}^2(T)} = (1+\frac{C_i}{C_{int}})^2 \cdot \overline{V_n^2(T)} - 2 \cdot (1+\frac{C_i}{C_{int}}) \cdot (\frac{C_i}{C_{int}}) \cdot \Phi_{V_n}(T) + (\frac{C_i}{C_{int}})^2 \cdot \overline{V_n^2(0)} \qquad (2\ 69)$$

The effect of the long-term correlation of the flicker noise may be seen more clearly in the time-domain relationship of Equation 2 49 If the noise is highly correlated, its instantaneous value will not change as much from the opening of the switch (t=0) to the closing of the switch (t=T) The difference in instantaneous voltages is the quantity that gets multiplied by the capacitance ratio to the output This effect is similar to what occurs in an autozeroed amplifier [17]

The analysis can be simplified by analyzing each of the terms in Equation 2 69 separately If the input-referred (one-sided) power spectral density of the amplifier flicker noise is equal to

$$S_{v(flicker)}(f) = \frac{K_v}{f}\frac{V^2}{Hz} \quad , \qquad (2\ 70)$$

then the first term in Equation 2 69 may be written as

$$\overline{V_{no1}^2(T)} = \frac{K_v}{2} \cdot (1 + \frac{C_i}{C_{int}})^2 \cdot \ln(\omega_h \cdot T) \qquad (2\ 71)$$

The signal-to-noise ratio (as defined in Equation 2 65) for this first term is then

$$SNR = \frac{2 \cdot (C_{int} \cdot V_{TH})^2}{K_v \cdot (C_i + C_{int})^2 \cdot \ln(\omega_h \ T)} \qquad (2\ 72)$$

Again, the system accuracy is improved by longer integration time The analysis of the third term in Equation 2 67 is similar to this one, and is therefore omitted

The second term represents the autocorrelation of the amplifier flicker noise The autocorrelation function for 1/f noise is difficult to handle mathematically, because of its divergence at zero This difficulty may be handled somewhat by introducing the effect of finite observation time A time-dependent autocorrelation function for 1/f noise is given in [27] as

$$\Phi_{\frac{1}{f}}(t,\tau) = \frac{K_v}{2} \cdot \ln\left[\frac{\sqrt{(t^2 - t \cdot \tau)} + t - \frac{\tau}{2}}{\sqrt{\frac{1+\tau}{\omega_h}} + \frac{1}{\omega_h} + \frac{\tau}{2}} \right] , \qquad (2\ 73)$$

where ω_h is again the high-frequency limit Without going into further analysis, it can be said that the autocorrelation of 1/f noise decays slowly with time and increases as the bandwidth is reduced The autocorrelation term actually reduces (negative sign)

the output mean-squared noise voltage (Equation 2 69) The significance of this term decreases with increasing integration time However, maximizing integration time still leads to better signal-to-noise ratio This statement can be proved by following the same type of analyses previously presented

2.5 System Simulation

The system schematic and some of the component schematics are given in Figures 22 through 25 The low-noise amplifier is the primary focus of the design work in this thesis and is described thoroughly in Chapter 3 The comparator and one-shot (Figures 23 and 24) used in the system design were previously designed [28]. The D flip-flop was obtained from a "standard-cell" library of digital blocks
The system in Figure 22 was simulated in HSPICE using a netlist extracted from the circuit layout file (explained in section 2 6) This netlist is given in the Appendix The photodiode was simulated as an ideal current source (10 pA) in parallel with a capacitor (3 pF) representing the parasitic detector capacitance The threshold voltage of the comparator was set to 1 V and the detector bias (baseline) was set to 0 V

Figure 26 shows the waveforms at the output of the integrator and the system The integrator output voltage ramps up until it reaches the threshold voltage (1V) and then resets to a baseline level The system output changes digital states at each reset transition, performing a frequency divide-by-two function This plot qualitatively verifies the operation of the system The slope of the ramp should be equal to approximately 18 4 V/sec (10 pA/0 545 pF), but simulation shows it to be

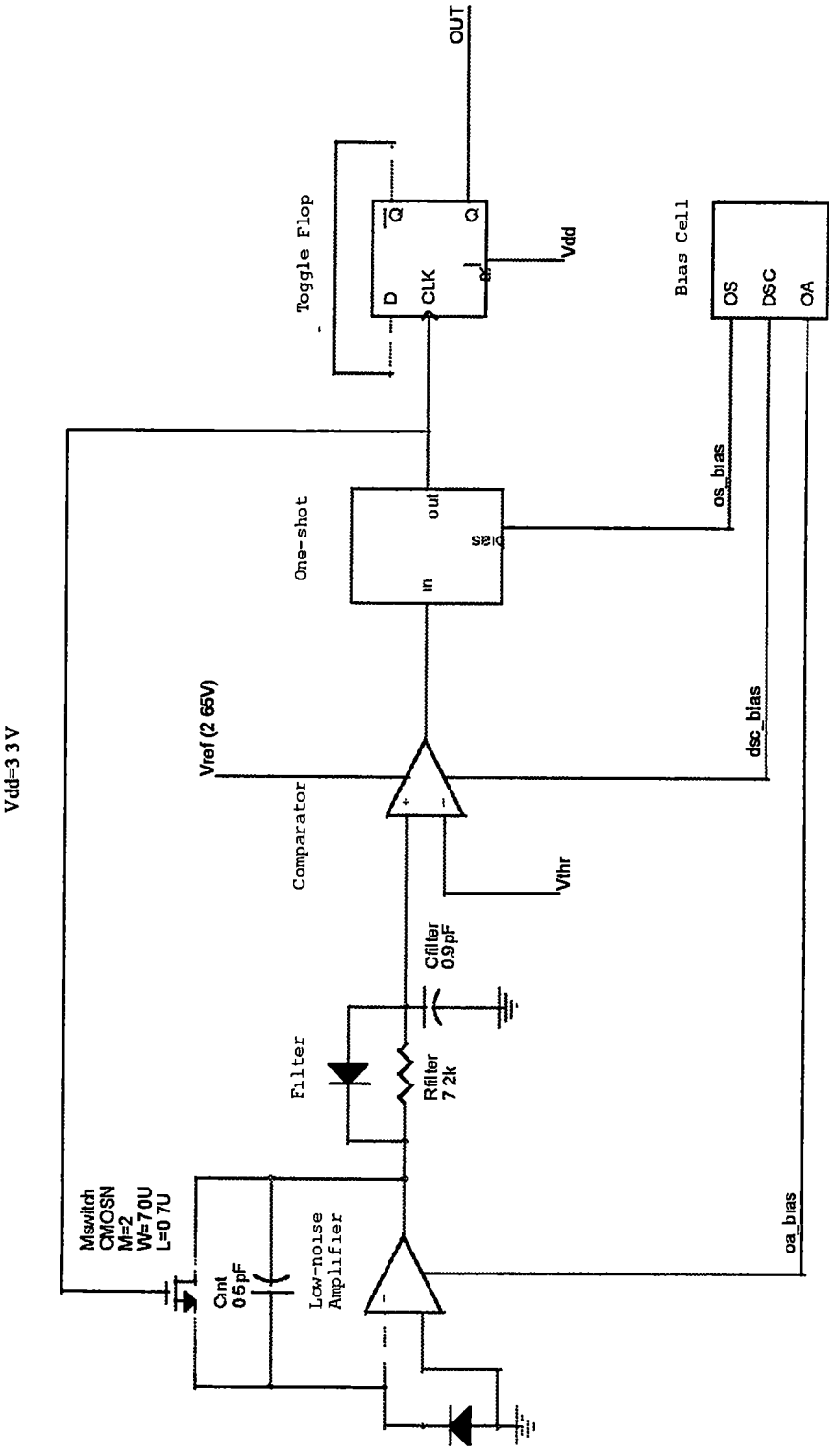

Figure 22 – Microluminometer System Schematic

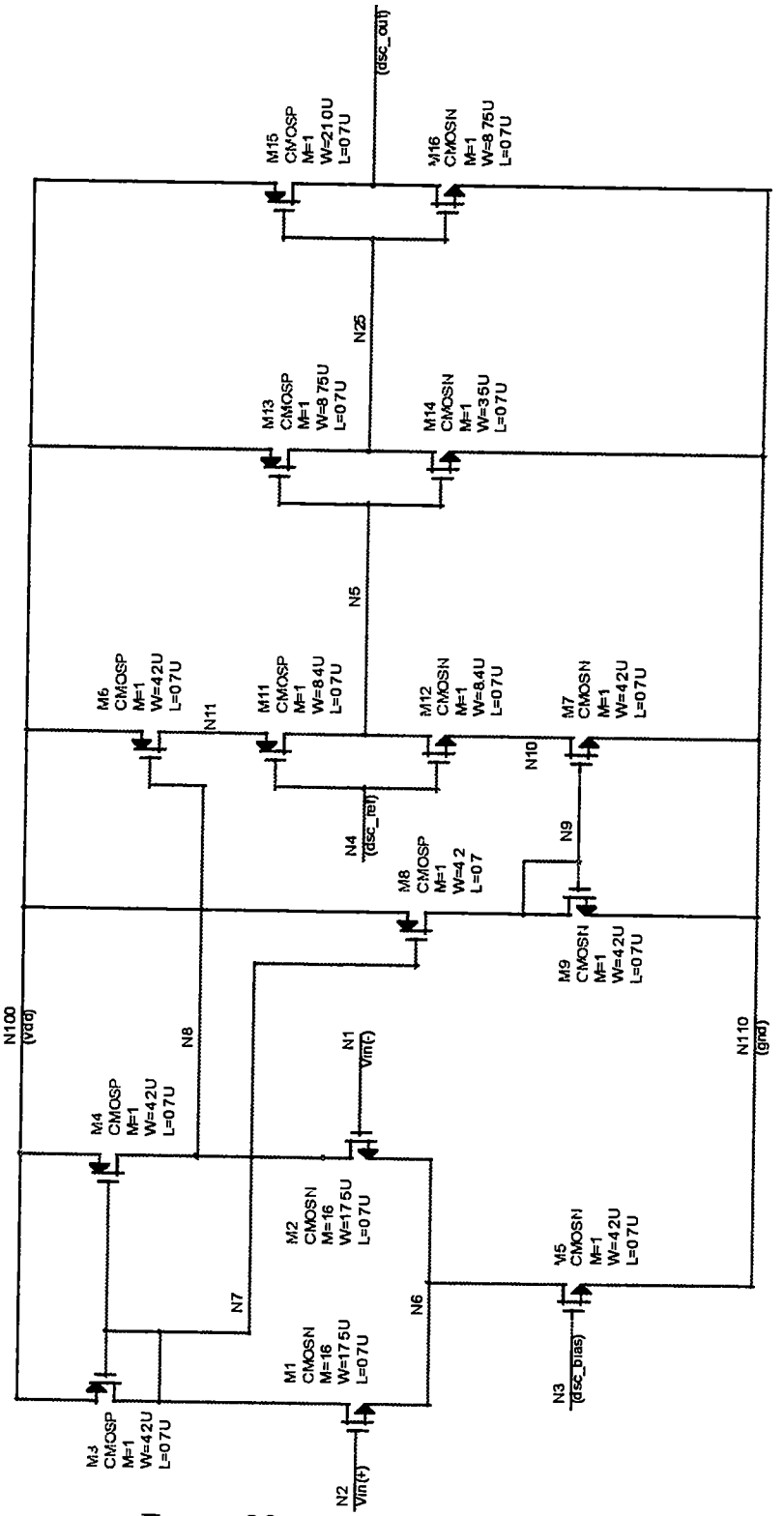

Figure 23 - Comparator Schematic

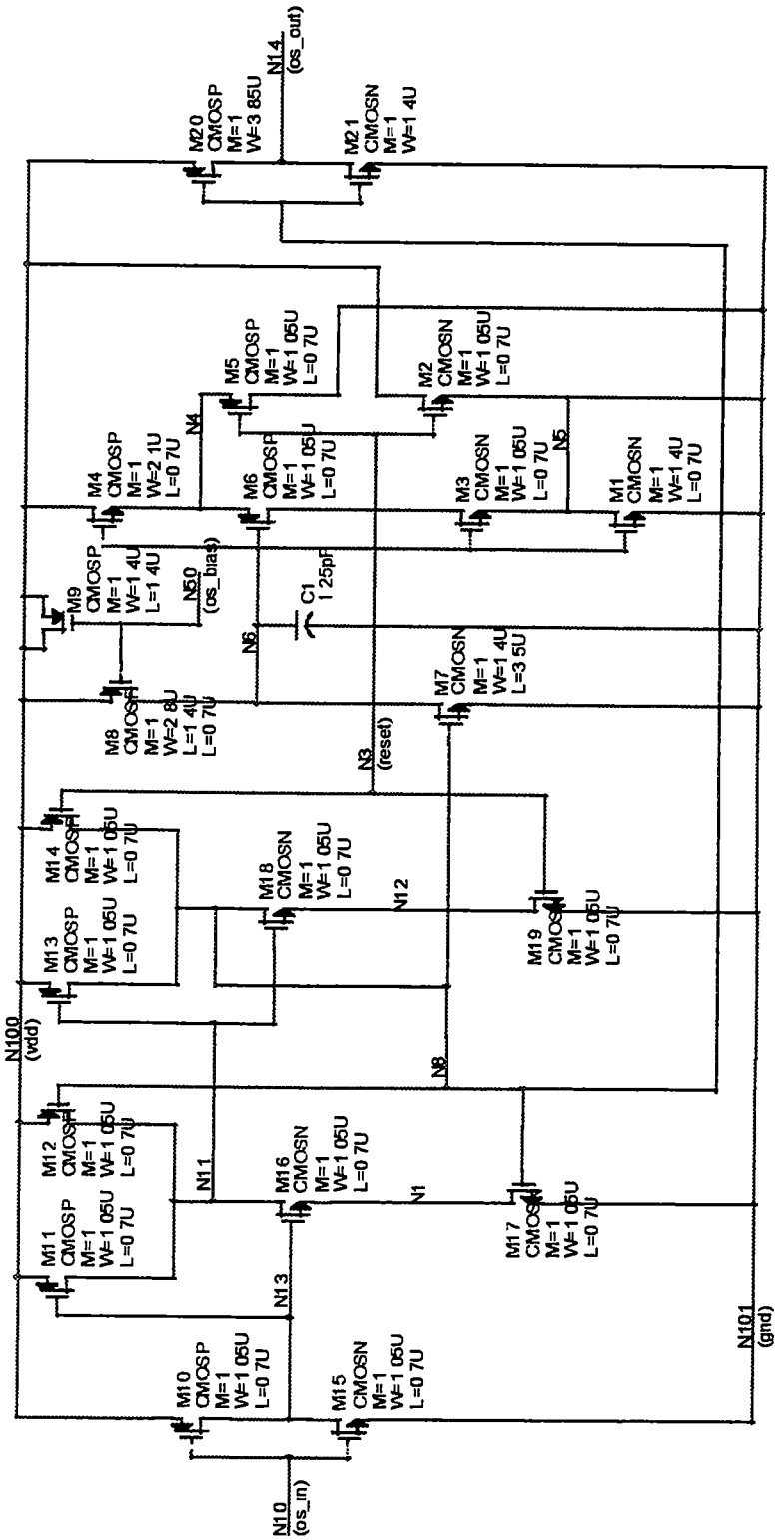

Figure 24 - One-Shot Schematic

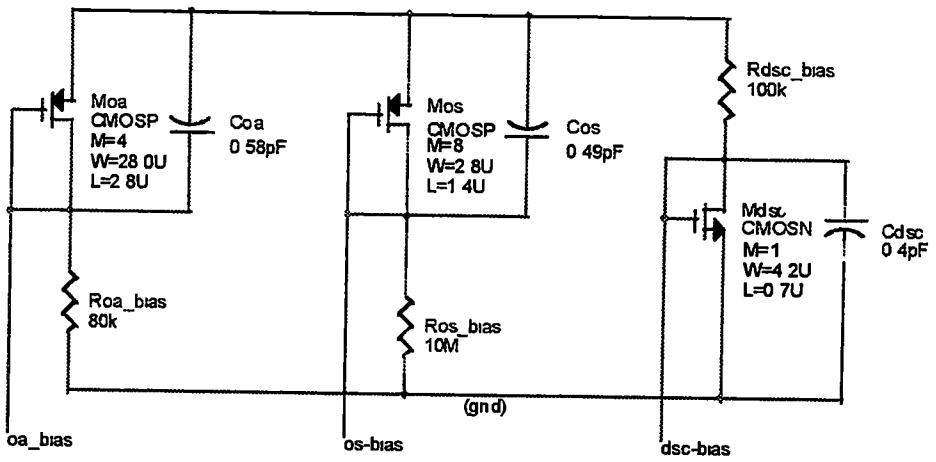

Figure 25 - Bias Cell (External Resistors)

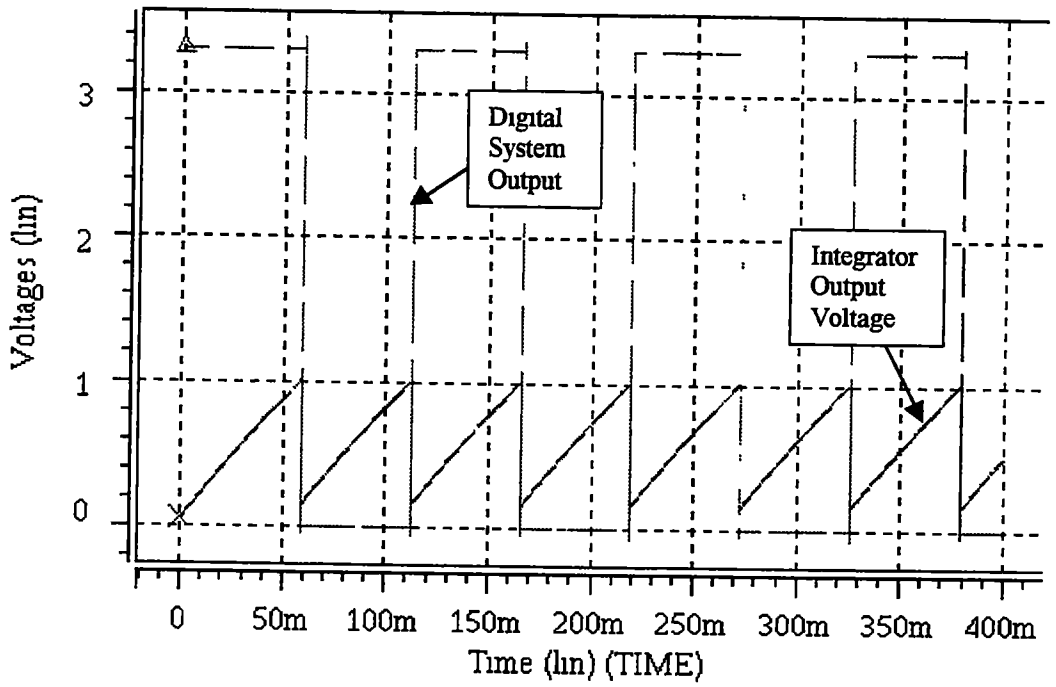

Figure 26 – Simulated Integrator and System Outputs

approximately 16 2 V/sec This result would indicate a gain error of –12% Also, a noticeable offset (147 mV) appears after the switch opens, indicating charge injection This offset is shown in greater detail in Figure 27, which shows the integrator output and one-shot output at the end of reset Figure 28 shows the integrator output at reset Simulation showed that the output took approximately 6μsec to settle to the baseline level and the one-shot reset pulse width was 66μsec The reset time can be varied by changing the external resistor that biases the one-shot

Although the simulations showed a considerable gain error, the accuracy of the simulation is questionable The simulator had a great deal of difficulty in converging for this closed-loop system, and relaxed some of the tolerances (such as GMIN) to come to an operating point The accuracy of the integrator is investigated again in chapter 3, and further simulation is done with only the integrator to determine its gain error

2.6 CMOS Implementation

After design and initial simulations, a physical layout of the system was created This layout was created with the MAGIC integrated circuit layout program and is shown in Figure 29 The chip layout includes the signal processing system and a large (approximately 1 2 mm^2) n-well type photodetector The layout of the signal processing alone is shown in Figure 30 Notable features of the layout include the common-centroid layout of the amplifier input devices and the interdigitated

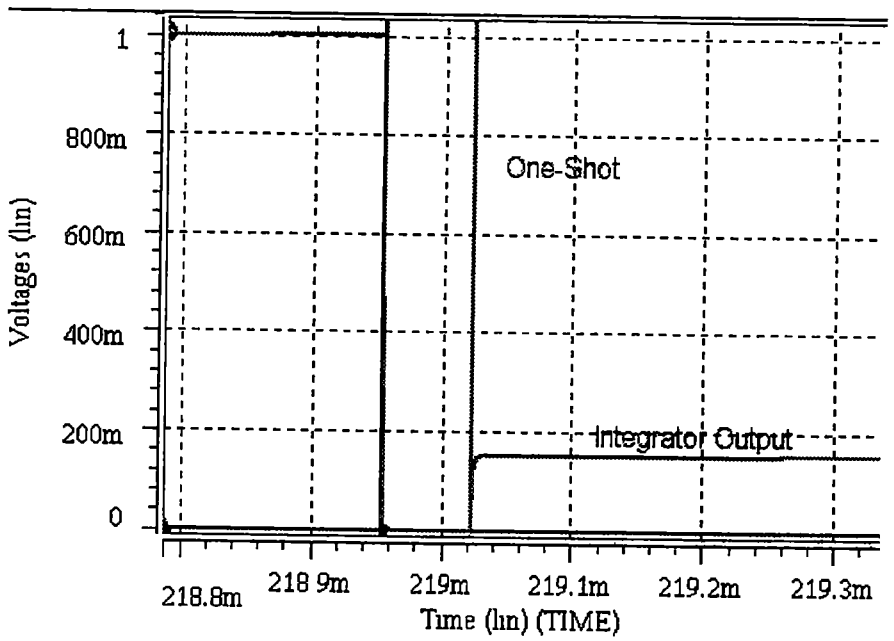

Figure 27 – Integrator Offset Voltage

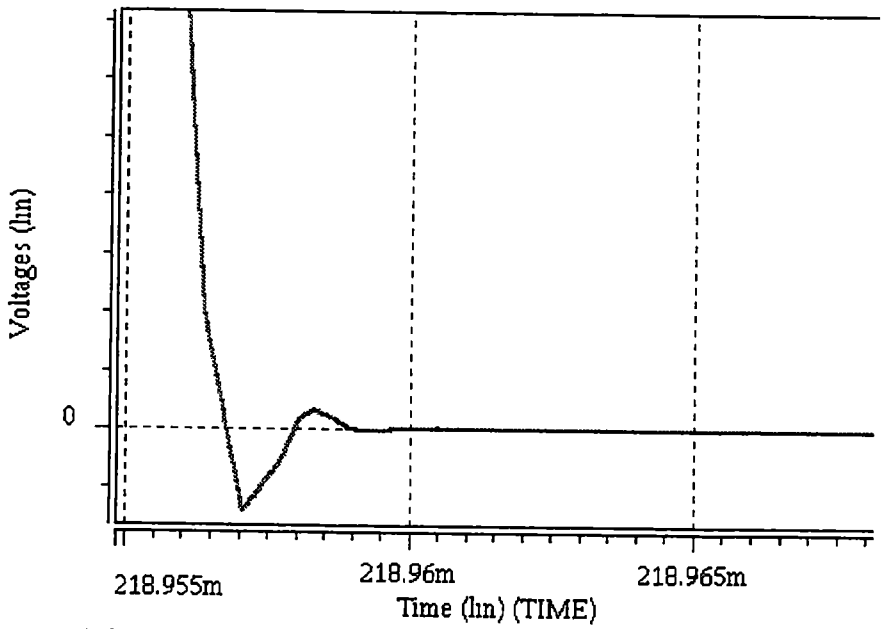

Figure 28 - Integrator Output Settling at Reset

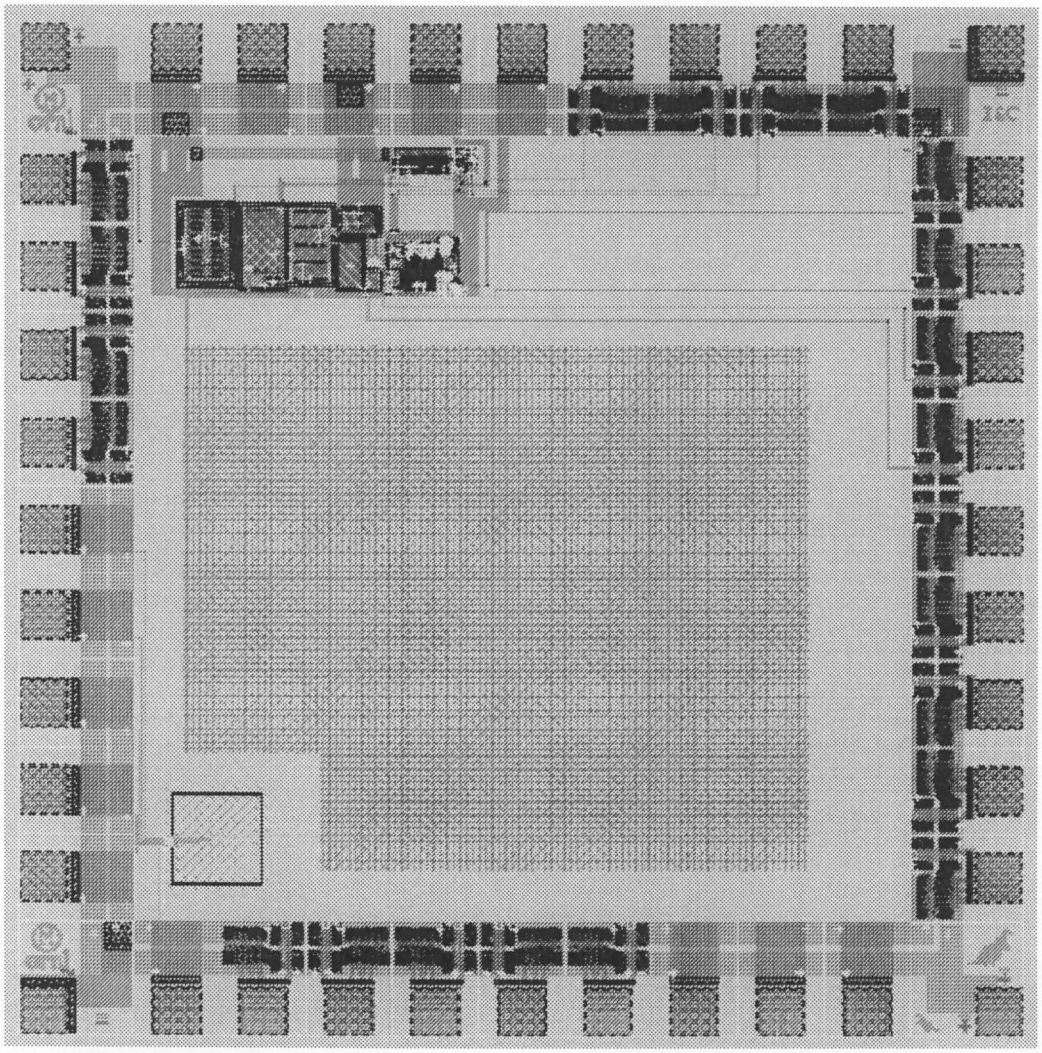

Figure 29 – Microluminometer Prototype IC Layout

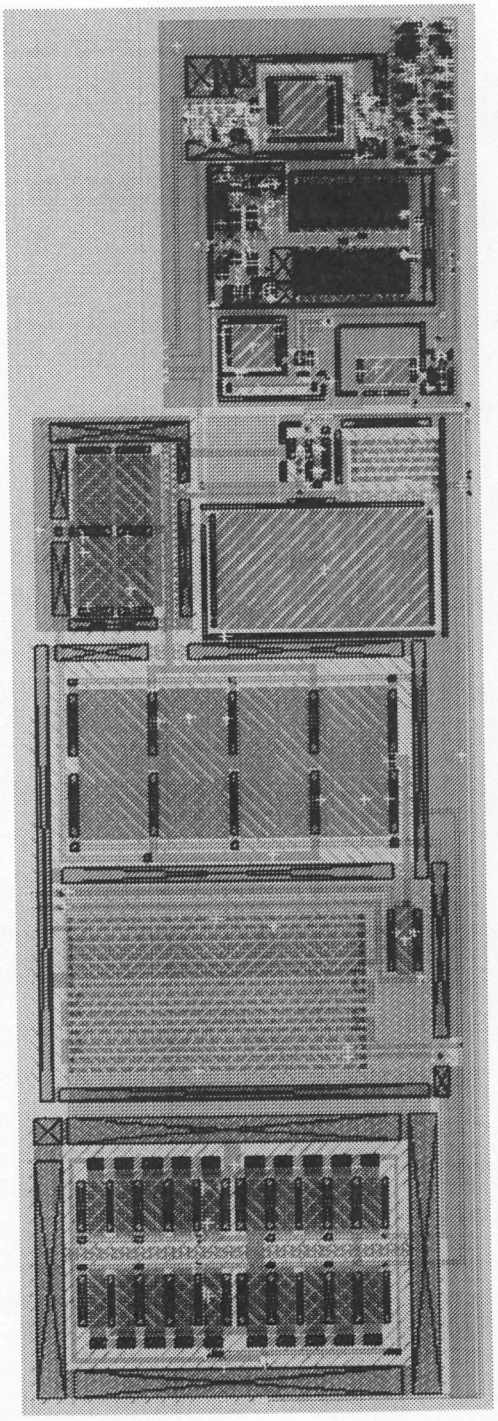

Figure 30 - Signal Processing Layout

layout of the resistors in the amplifier Both of these techniques are used to improve matching Resistor matching was also improved by the use of "dummy resistors" as described in [10] Also, the power-supply grids for the analog and digital circuitry were kept separate to minimize the charge injection (spikes) and other effects that can occur when digital and analog circuits are integrated on the same chip [29] As mentioned in the last section, a netlist was extracted from this layout and used for simulation Not only does the use of this netlist account for the parasitic stray capacitances in the layout; it also verifies the accuracy of the layout After verification, the layout file was submitted to the MOSIS fabrication service [5] Figure 31 shows an actual photograph of chip, fabricated in the HP 0 5 μm CMOS process The active area of the integrated circuit, excluding bonding pads and the associated protection circuitry, is approximately 2 mm × 2 mm

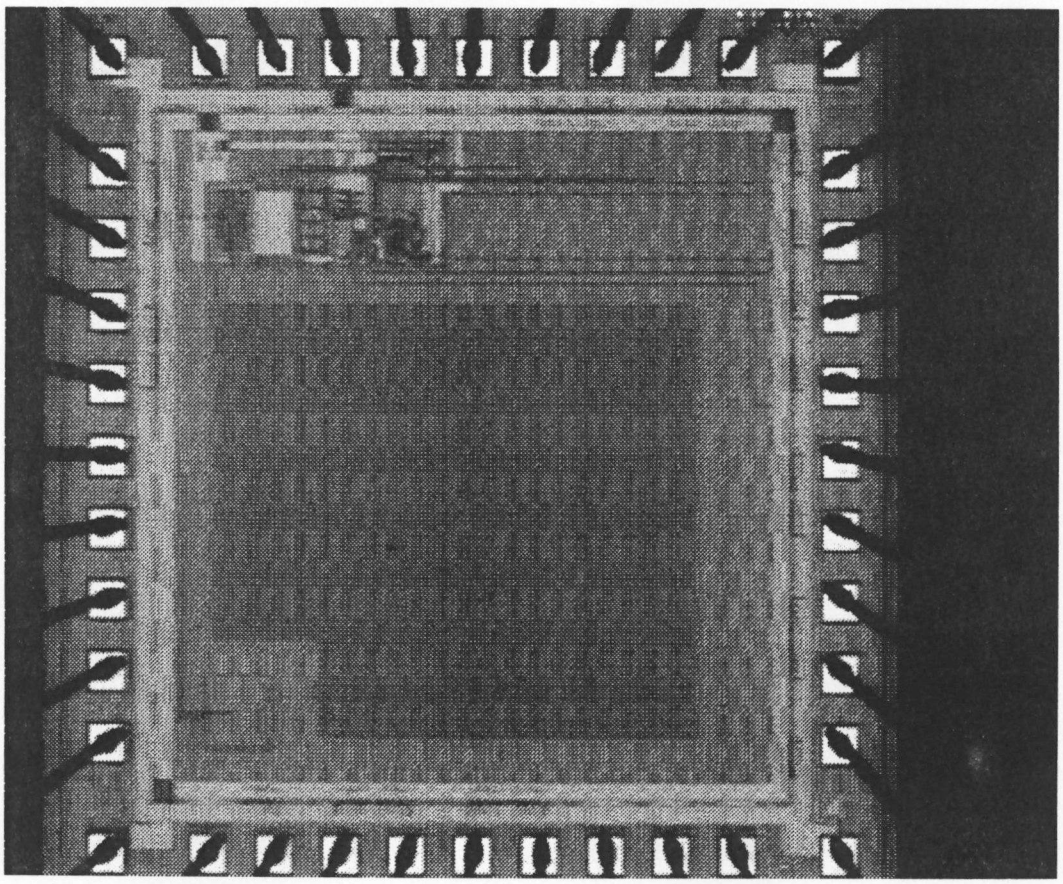

Figure 31 – Microluminometer Prototype Chip Photograph

Chapter 3

Low-Noise Amplifier Design

3.1 Amplifier Requirements

The discussion of the previous chapter made clear the importance of the integrator amplifier design Its performance is critical to the accuracy of the BBIC sensor Intrinsic noise is a definite concern for this design In particular, the 1/f noise of the MOS devices should be minimized, because the averaging of the system does not reduce the 1/f noise error in the same way that thermal noise error is reduced (Equation 2 60) In addition to low noise, the amplifier should be designed to have high gain The accuracy of the integrator is dependent on high gain, but the amplifier must also be unity-gain stable These two requirements are in direct opposition Luckily, this application does not require a great deal of amplifier bandwidth, because the bioreporters [2] have a low-frequency response (essentially DC) A lowered bandwidth not only makes the task of compensation easier, but system noise is also reduced Another requirement of the amplifier is that both its output and input dynamic ranges extend to 0V, allowing for zero bias on the photodetector Finally, power consumption should be held as low as possible

3.2 Amplifier Topology

Choosing an amplifier topology can begin with a consideration of the input Considering only device noise, a single-ended input would be preferable, since this represents a 40% reduction in rms noise voltage over a differential stage [11] A differential stage, however, is needed in this situation to accurately set the detector bias With this decision made, the type of input devices must be chosen Based on flicker noise considerations, the lateral pnp bipolar device available in n-well CMOS [30] would be preferable This device, however, has a base current that is intolerable in this charge-sensitive application The next best alternative (of the two remaining) is the p-channel MOSFET PMOS devices have flicker noise levels that are commonly an order of magnitude lower than those of NMOS devices of the same size in the same process [31] PMOS input devices are also necessary so that the input dynamic range includes ground Finally, the question arises as to the connection of the body (n-well) of the input devices The body connection can be made to either the power supply or the source of the transistor As described in [32], connecting the body to the power supply is a poor choice in charge-sensitive applications, because supply variations result in charge injection to the input

Amplifiers of several basic topologies could be made to meet the gain and stability requirements of this design Therefore, low-noise performance becomes the deciding factor A basic technique of low-noise design is to minimize the noise contribution of the input stage and then design the amplifier so that this is the dominant contribution This technique usually involves making the gain of the input

stage large, so that the noise of the rest of the amplifier, when referred to the input, is insignificant

A reasonable candidate for this design is the simple topology shown in Figure 32 The first stage is a differential pair with resistive loads While an active load would produce higher gain, it would also introduce significant noise In particular, the flicker noise introduced by an NMOS active load would be intolerably high The question then becomes whether or not an adequate gain can be achieved with this resistively loaded stage The differential gain of this input stage is equal to

$$|A_v| = g_m \; R_L \qquad , \tag{3 1}$$

where g_m is the transconductance of the input devices and R_L is the value of a load resistor This gain is proportional to the voltage drop across the load resistors The available headroom limits the load voltage drop This is an unfortunate situation, since the gates of the input devices are to be biased at ground potential The body connections of the input devices are also connected to their sources, further reducing the voltage headroom compared to the situation in which the body is connected to the power supply Simulations using the models for this process showed that a maximum gain of nearly 10 was achievable for this stage This level of gain was not deemed sufficient

The basic folded cascode topology, shown in Figure 33, has been successfully used in low-noise amplifier design [33] The noise of this circuit, however, can easily

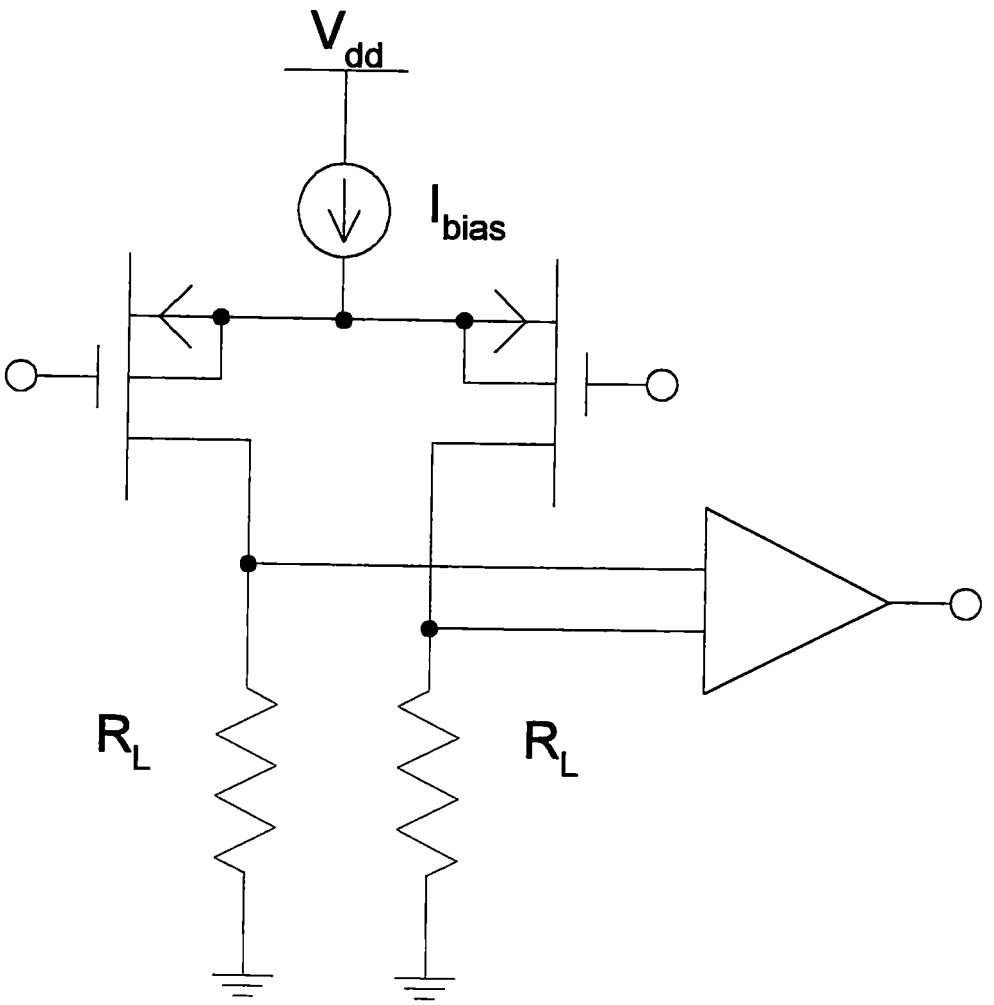

Figure 32 – Resistively Loaded Amplifier Topology

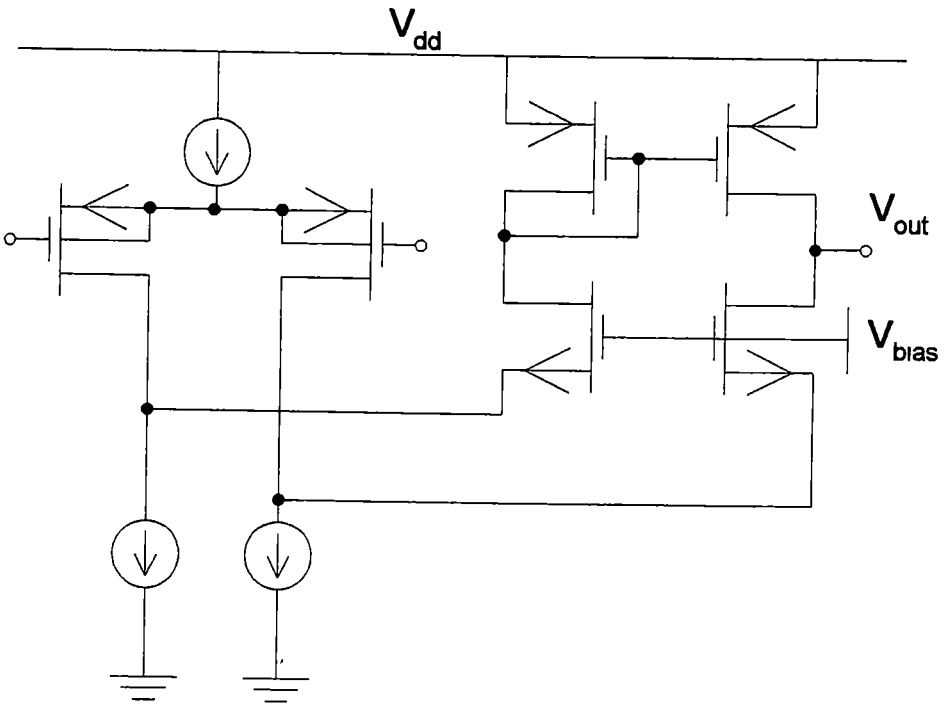

Figure 33 – Folded Cascode Amplifier

become dominated by the current sources at the "fold" of the amplifier This is particularly true when considering 1/f noise, since these current sources are formed by NMOS devices A common technique to reduce the noise contribution of current sources is resistive source degeneration [34] This method places a resistor in series with the source of the transistor, employing a localized negative feedback to reduce the noise current output of the current source The effectiveness of this method is dependent on the amount of voltage drop across the degeneration resistor As previously stated, the amount of voltage headroom available is limited by the input biasing Having a significant voltage drop across the degeneration resistors and keeping the current sources in saturation would be very difficult in this situation An alternative is to replace the current sources with resistors This topology was chosen for the design

While the folded cascode may be a suitable low-noise amplifier, its output dynamic range not does meet the requirements for this application A simple source-follower buffer, as shown in Figure 34, can be added to the output of the cascode stage This buffer provides a level shift, extending the output dynamic range closer to ground Its noise should also prove insignificant due to the high gain of the cascode stage In order to actually reach 0V at the output, the source of the buffer transistor can be connected to a slightly negative voltage (V_{neg}) In simulation, V_{neg} was set to – 0 3V

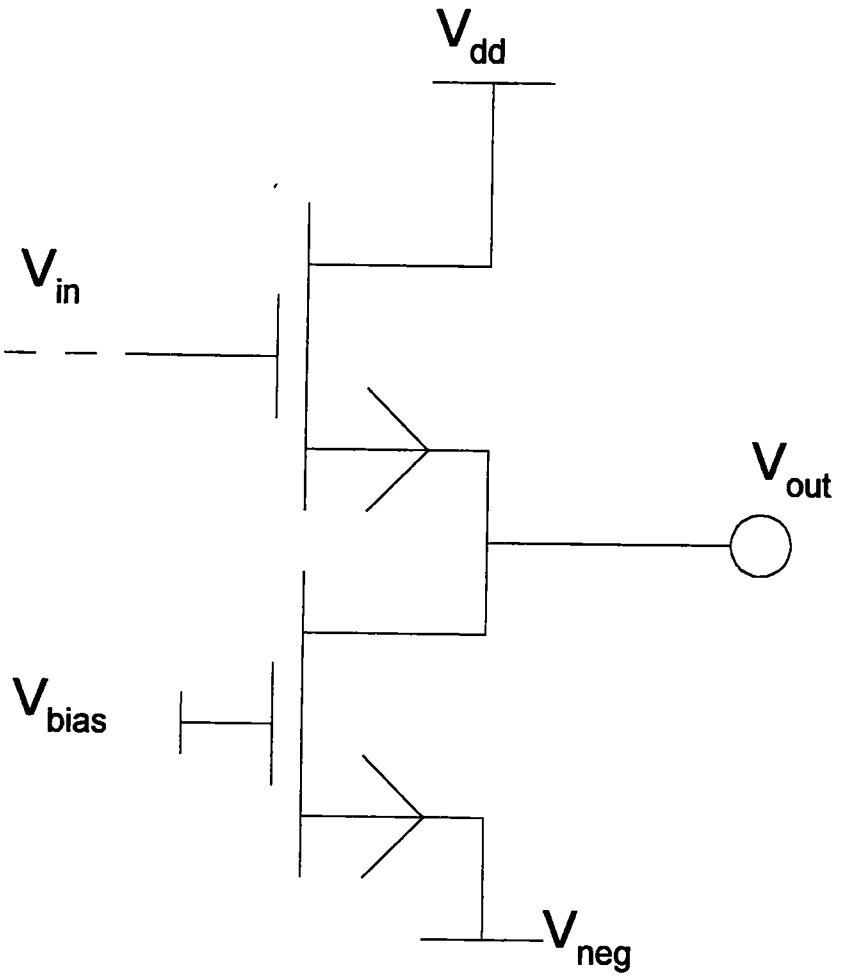

Figure 34 – Output Buffer

3.3 Amplifier Noise Analysis

A goal of this analysis is to find an expression for the input-referred noise voltage of the amplifier In doing so, insight into noise optimization is obtained

3.3.1 Noise Modeling

Before proceeding with the mathematical analysis, the noise models must be established There are two device types (in addition to the detector) that require a model resistors and MOSFETS The resistor thermal noise may be modeled as a shunt current generator, as shown in Figure 35 The noise current PSD is inversely proportional to the value of the resistance [35]

$$i_r^2 = \frac{4 \cdot k \cdot T}{R} \frac{A^2}{Hz} \quad , \tag{3 2}$$

where k is Boltzmann's constant ($1\ 38 \times 10^{-23}$ J/K), T is absolute temperature (K), and R is the value of the resistor (Ω)

The noise of a MOS device may also be represented by a shunt current generator, as in Figure 36 The noise of the transistor has both a white component and a 1/f component The white noise is thermal noise generated by the conductance of the channel 1/f noise is generated by charge trapping at the interface of the oxide to the channel [12] The composite noise spectrum is equal to [10]

$$i_n^2 = 4 \cdot k \cdot T \left(\frac{2}{3}\right) \cdot g_m + \frac{K_f \ g_m^2}{W \cdot L \cdot C_{ox} \cdot f^a} \frac{A^2}{Hz} \quad , \tag{3 3}$$

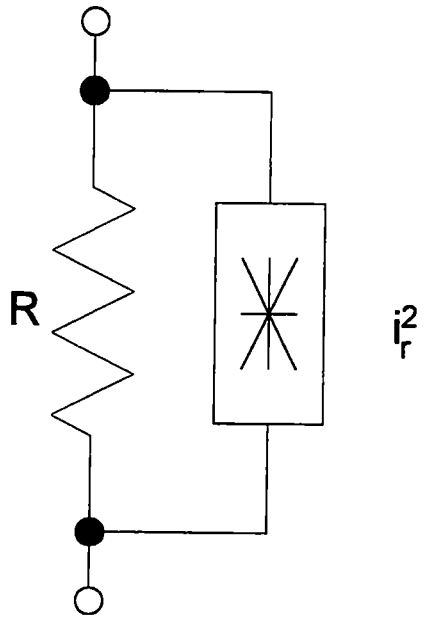

Figure 35 – Resistor Noise Model

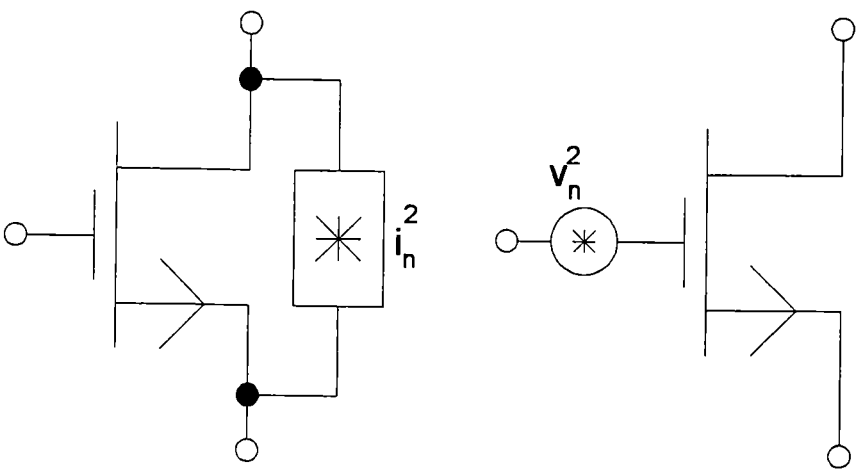

Figure 36 – MOS Noise Model

where K_f is a process-dependent coefficient, C_{ox} is the oxide capacitance per area, and a is a process-dependent exponent (usually near unity) The 2/3 factor comes from an approximation of the channel conductance in "pinch-off" The MOS noise current may also be referred to the gate as an equivalent noise voltage at the gate Dividing Equation 3 3 by the transconductance squared gives

$$v_n^2 = \frac{4 \cdot k \cdot T \cdot (\frac{2}{3})}{g_m} + \frac{K_f}{W \cdot L \cdot C_{ox} \cdot f} \frac{V^2}{Hz} \qquad (3\ 4)$$

MOS thermal noise is reduced by increasing the bias current (g_m) Flicker noise is reduced by increasing the device area Equation 3 4 indicates that the gated-referred flicker noise is independent of biasing Experimentally, the voltage noise of NMOS devices has been shown to be nearly independent of biasing, while PMOS devices show a definite bias dependence [31]

3.3.2 Mathematical Analysis

Figure 37 shows the basic amplifier modeled with individual device noises The PSD's of the individual noise sources can be summed (by superposition) and referred to the input as an equivalent noise voltage generator (Figure 12) A methodology for calculating the equivalent input noise is to refer each noise source to the amplifier output, add the resulting PSD's, and then divide this result by the power gain from the input to output The gain of the amplifier, for low frequencies and low source impedance, is approximately given by

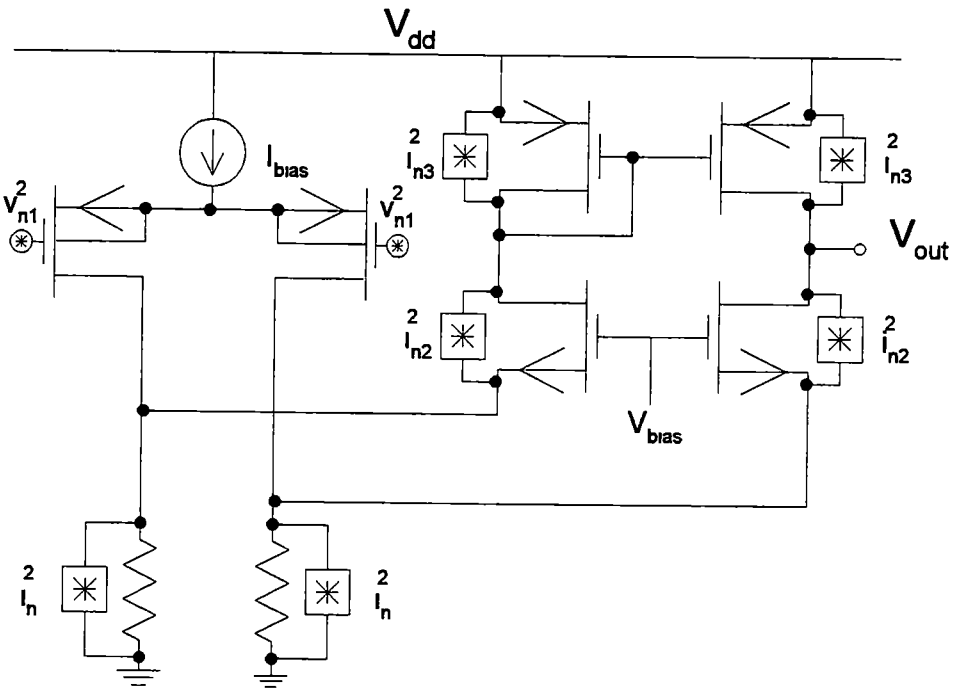

Figure 37 – Folded Cascode Amplifier with Noise Sources

$$A_v \cong \frac{g_{m1}\ (g_{m2}+g_{mb2})\cdot R_{fold}\cdot R_{out}}{1+(g_{m2}+g_{mb2})\cdot R_{fold}} \quad , \qquad (3\ 5)$$

where g_{mb2} models the body effect of the cascode devices, R_{out} is the output impedance of the amplifier, and the numerical subscripts denote the various device pairs (1=input devices, 2=cascode devices, and 3=load devices) The output impedance is given by

$$R_{out} \cong r_{o3} // \{r_{o2}\ \left[1+(g_{m2}+g_{mb2})\cdot R_{fold}\right]+R_{fold}\} \quad , \qquad (3\ 6)$$

where r_o is the output impedance of a MOS device Using this expression for the gain of the amplifier, the input-referred noise power spectral density was derived as

$$V_n^2(f) = 2\cdot v_{n1}^2 + \frac{2\ i_r^2}{g_{m1}^2} + \frac{2\cdot i_{n2}^2}{\left[g_{m1}\cdot(g_{m2}+g_{mb2})\cdot R_{fold}\right]^2} + \frac{2\cdot i_{n3}^2\cdot[1+(g_{m2}+g_{mb2})\cdot R_{fold}]^2}{[g_{m1}\cdot(g_{m2}+g_{mb2})\cdot R_{fold}]^2} \qquad (3\ 7)$$

The first term is the contribution of the input devices, the second is due to the resistors, the third is due to the cascode devices, and the fourth is due to the load devices

The white component of this noise is given by

$$V_n^2(f)_{white} = \frac{16 \cdot k \cdot T}{3 \cdot g_{m1}} + \frac{8 \cdot k \cdot T}{g_{m1}^2 \cdot R_{fold}} + \frac{16 \cdot k \cdot T \cdot g_{m2}}{3\left[g_{m1} \cdot (g_{m2} + g_{mb2}) \cdot R_{fold}\right]^2}$$

$$+ \frac{16\ k \cdot T \cdot g_{m3}\left[1 + (g_{m2} + g_{mb2}) \cdot R_{fold}\right]^2}{3 \cdot \left[g_{m1} \cdot (g_{m2} + g_{mb2}) \cdot R_{fold}\right]^2} \frac{V^2}{Hz} \qquad (3\ 8)$$

The analysis of this expression indicates that the following parameters should be maximized for low white noise g_{m1}, g_{m2}, and R_{fold} The transconductance of the load devices, g_{m3}, should be minimized These requirements lead to large voltage drops across both the fold resistors and the load devices, so low-noise performance is somewhat compromised for dynamic range purposes

The flicker noise component of the input-referred noise voltage, neglecting body effect, is

$$V_n^2(f)_{1/f} = \frac{2 \cdot K_{fp}}{(W \cdot L)_1 \cdot C_{ox}\ f} + \frac{2 \cdot K_{fn}}{(W \cdot L)_2 \cdot C_{ox} \cdot (g_{m1} \cdot R_{fold})^2 \cdot f}$$

$$+ \frac{2 \cdot K_{fp} \cdot [g_{m3} \cdot (1 + g_{m2} \cdot R_{fold})]^2}{(W\ L)_3 \cdot C_{ox} \cdot (g_{m1} \cdot g_{m2} \cdot R_{fold})^2 \cdot f} \frac{V^2}{Hz} \qquad (3\ 9)$$

One obvious design technique to reduce flicker noise is to use large-area devices Not only is this technique limited by chip area, but it leads to large parasitic capacitances Large input capacitance has been shown to increase system noise, so the size of the input devices is of particular concern Increasing their size reduces their flicker noise production, but this also increases the gain that the amplifier noise experiences to the integrator output The optimum size for the input devices is such that the input

capacitance of the amplifier is matched to the sum of the detector and integration capacitances [36]

With the size of the input devices set, the design task becomes making the input devices the dominant flicker noise contributors The second term in Equation 3 9 presents the greatest challenge This term represents the effect of the NMOS cascode devices The NMOS devices present a difficulty because they naturally have a higher level of flicker noise than PMOS devices ($K_{fn} > K_{fp}$) Two techniques can be used to limit their noise contribuition relative to the input devices. First, the NMOS devices can be made larger than the input devices Using this technique alone would result in intolerably large cascode devices, since K_{fn} is often an order of magnitude larger than K_{fp} Luckily, the fold resistors reduce the NMOS flicker noise through source degeneration The $g_{m2}R_{fold}$ product, and subsequently the voltage drop across the resistors, should be maximized

The load devices are not as great a concern as the cascode devices, but they must be considered Some insight can be gained from making the substitution [10]

$$g_{m3}^2 = 2\mu_p \cdot C_{ox} \cdot (\frac{W}{L})_3 \cdot I_{D3} \quad , \tag{3 10}$$

where μ_p is the mobility of holes The result is that, surprisingly, the flicker noise of the load devices is independent of their widths for a given bias current The noise is, however, inversely proportional to the square of the device length The lengths of the load devices should, therefore, be made several times larger than those of the input

devices This design choice will make the load device noise relatively small compared to that of the input

3.4 Frequency Response/Stability Analysis

The amplifier must be made unity-gain stable to allow for integrator reset In order to design for stability, one must know the frequency locations of the significant poles and zeroes The "dominant" pole is located at the output node, and occurs at a frequency

$$f_{pdom} = \frac{1}{2 \cdot \pi \cdot R_{out} \; C_{out}} Hz \quad , \tag{3 11}$$

where R_{out} is the output impedance of the cascode gain stage(Equation 3 6) and C_{out} is the total output capacitance Two "non-dominant" poles occur at the sources of the cascode devices The cascode devices carry signals of the same amplitude but opposite phase The two poles combine to form a single pole at [37]

$$f_{p2} = \frac{g_{m2} + g_{mb2} + \frac{1}{R_{fold}}}{2 \cdot \pi \; C_2} Hz \quad , \tag{3 12}$$

where C_2 is the total capacitance at the source of one of the cascode devices A third pole is located at the diode-connected load device

$$f_{p3} = \frac{g_{m3}}{2 \cdot \pi \cdot C_3} Hz \quad , \tag{3 13}$$

where C_3 is the total capacitance at the gate of the diode-connected transistor A zero also occurs in this amplifier due to the fact that there are two signal paths (differential) At frequencies well beyond f_{p3}, the gain in one of the signal paths (through the diode-connected device) has decayed Ideally, the other signal path is still active, resulting in an amplifier gain equal to half of the gain at DC The zero, therefore, occurs at a frequency of approximately

$$f_{z3} = 2 \cdot f_{p3} Hz \tag{3 14}$$

Normally, the folded cascode can be made stable through simple dominant node compensation, since there is only one high-impedance node (output) The complication in this case comes from the need to make the MOS devices large for flicker noise reduction The parasitic poles introduced by the devices become significant because of the large values of capacitance Lead compensation is possible in this case by adding a series combination of a capacitor and resistor [10], as shown in Figure 38 The RC network introduces a zero at

$$f_{zc} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} Hz \quad , \tag{3 15}$$

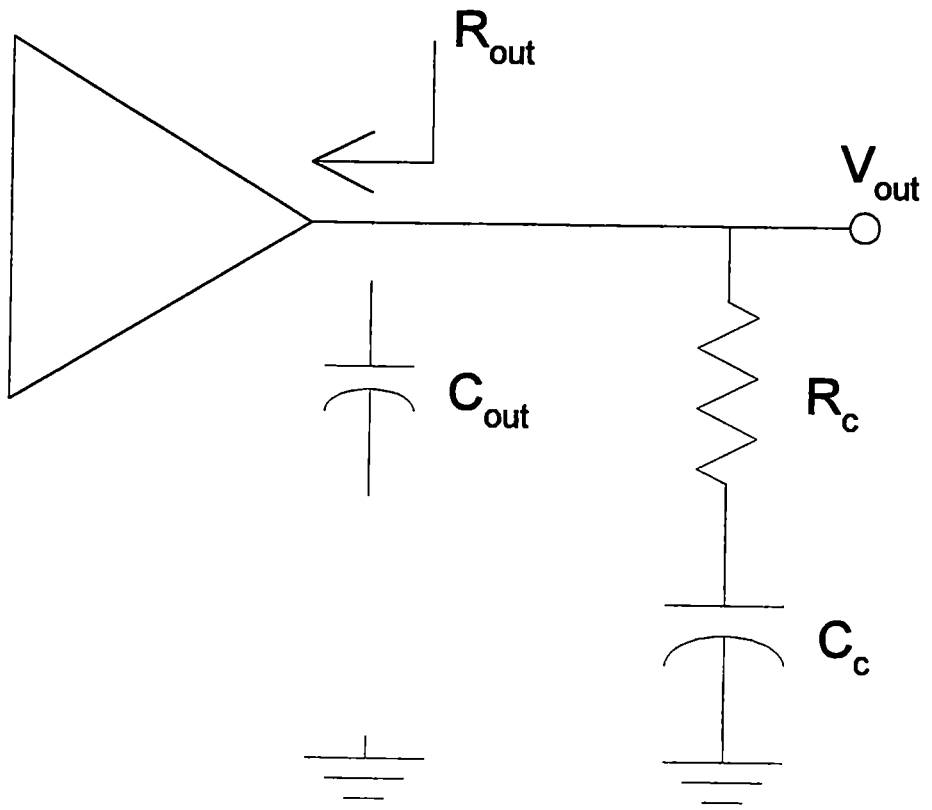

Figure 38 – Lead Compensation

where R_c and C_c are the compensation resistance and capacitance respectively This zero may be used to compensate for the phase shift produced by the parasitic poles The compensation also alters the pole that occurs at the output (Equation 3 11) If the compensation capacitor is much larger than the capacitance appearing at the output (C_{out}) and the output impedance (R_{out}) is much larger than the compensation resistor (R_c) then Equation 3 11 becomes

$$f_{pdom} \approx \frac{1}{2 \cdot \pi \cdot (R_{out} \cdot C_c)} Hz \qquad (3\ 16)$$

The lead compensation, therefore, also reduces the dominant pole frequency, improving the stability of the amplifier

In addition to the poles of the amplifier, a pole and zero are introduced by the feedback network of the integrator during reset (Equations 2 26 and 2 27) This effect should not be a concern unless the input capacitance (detector) is very large The source-follower also introduces a zero and a set of poles that may be real or complex conjugate [10] The follower device, however, should be very much smaller than the other devices in the amplifier signal path, making its frequency response of less concern The follower also attenuates the total gain of the amplifier, due mainly to the body effect [10]

3.5 Final Amplifier Design

Figure 39 is a schematic of the final amplifier design, showing all of the device sizes and values The ratio of the input device bias current to cascode device current should be large, with 4 1 being a practical upper limit [10] This method increases the gain and reduces thermal noise [10] The biasing of the input stage, therefore, is such that 20μA flows through each of the input transistors, and 5μA flows through the cascode and load devices The voltage drop across the fold resistors is approximately 750mV The results of an HSPICE DC operating point analysis are given in the Appendix

3.6 Simulation Results

The amplifier shown in Figure 39 was simulated with the HSPICE circuit simulation program A BSIM1 model obtained from MOSIS [5] was used in simulation The listing for this model is given in the Appendix

3.6.1 Noise Simulation

The input equivalent noise voltage (ENV) of the amplifier was determined via simulation The SPICE parameter NLEV was set to 3 in order to more accurately model the thermal noise The model provided by MOSIS did not include flicker noise coefficients, so value of K_f for both PMOS and NMOS devices were added For PMOS devices, a value of 5 28×10^{-26} V^2F was used, and NMOS flicker noise was modeled using a value of 1 32×10^{-24} V^2F These values were obtained by scaling the

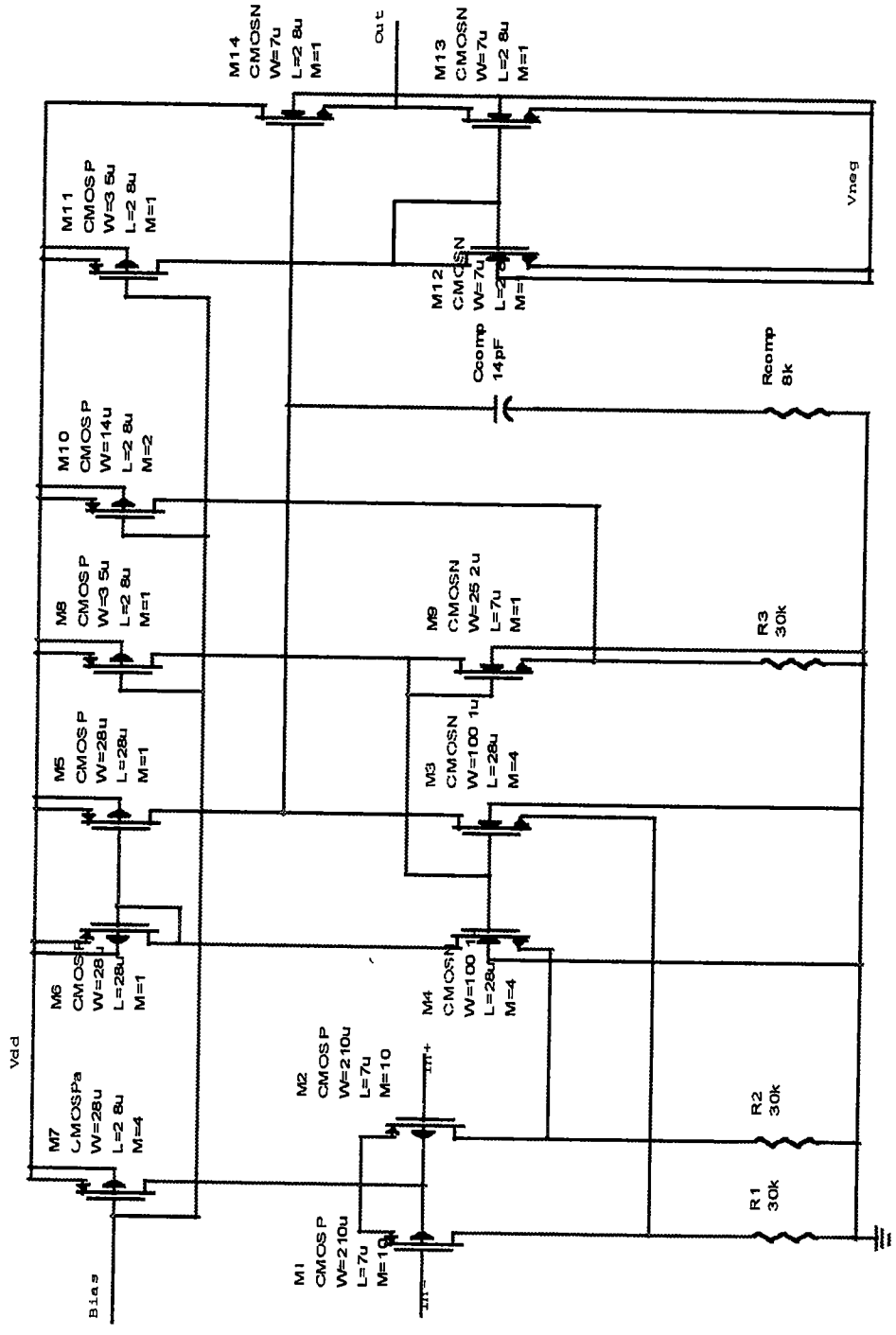

Figure 39 – Low-Noise Amplifier Schematic

values available for a 2 μm CMOS process [31]

The thermal noise component of the ENV was found to be just under 13 nV/rtHz, as shown in Figure 40 A SPICE noise analysis at 10kHz showed that the input devices account for 81 6% of the ENV, the fold resistors contribute 9 2%, the load devices add 7%, and the cascode devices generate 2 2% of the noise The l/f noise corner is the frequency at which the thermal and 1/f noise PSD's are equal From Figure 40, the corner frequency is 153Hz This result does not necessarily represent the actual performance of the amplifier, since the flicker noise model was not obtained for this IC process The relative noise contributions, however, are a useful simulation result A noise simulation at 1 Hz (where flicker noise is dominant) showed that the input devices contribute 89 7% of the input-referred env, the cascode devices add 8 8%, and the load devices account for the remaining 1 5% The input devices, therefore, dominate both the thermal and 1/f noise of the amplifier Finally, the noise bandwidth of the amplifier was measured in simulation The open–loop (unloaded) noise bandwidth is equal to 500Hz in simulation This result was obtained by squaring the open-loop voltage gain, integrating the product over frequency, and dividing the whole expression by the square of the DC value of the voltage gain [11] The noise simulation results are summarized in Table 3 1 along with the corresponding hand calculations

3.6.2 Frequency Response/Stability Simulation

The stability of the amplifier was analyzed in the closed-loop configuration, including the effect of the feedback network The reset switch device was biased

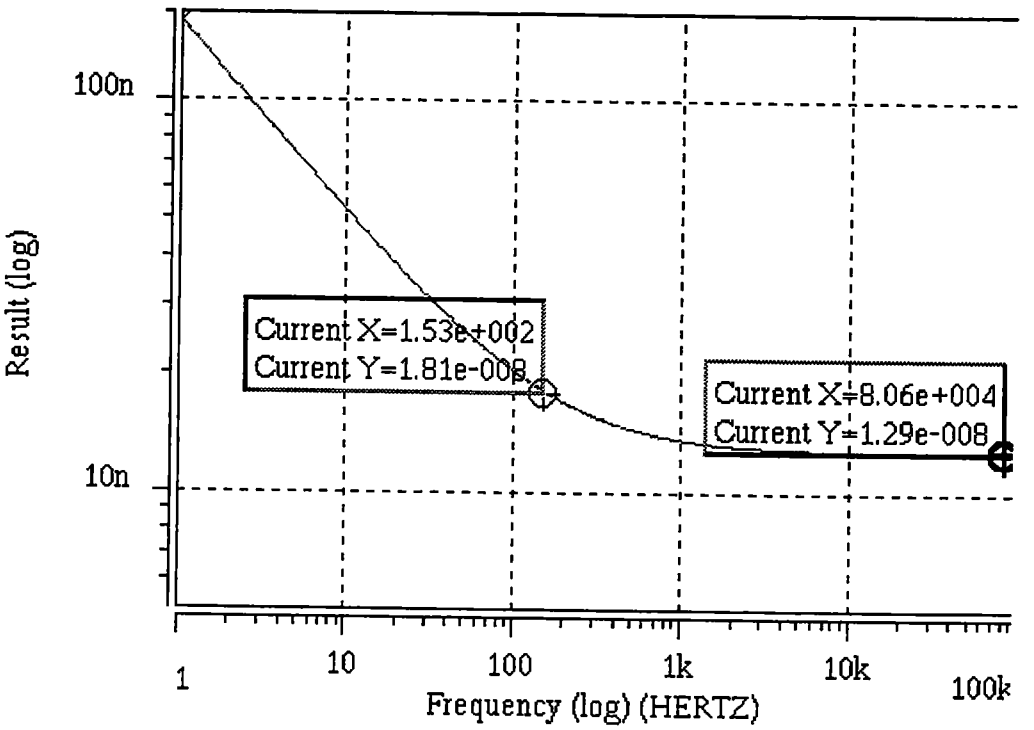

Figure 40 – Input Equivalent Noise Voltage (nV/rtHz)

Table 3.1 LNA Noise Simulation Results

	Hand Calculation	Simulation	Units
ENV	12.6566	12.6602	nV/rtHz
1/f Noise Corner	-	153	Hz
Noise Bandwidth	-	500	Hz

Input-referred White Noise PSD Device Contributions

Input Devices	1.0655×10^{-16}	1.0665×10^{-16}	V^2/Hz
Fold Resistors	2.5880×10^{-17}	2.5860×10^{-17}	V^2/Hz
Cascode Devices	6.4900×10^{-18}	6.4900×10^{-18}	V^2/Hz
Load Devices	2.1270×10^{-17}	2.1280×10^{-17}	V^2/Hz

Input-referred 1/f Noise PSD Device Contributions (at 1Hz)

Input Devices	1.9970×10^{-14}	$2\ 0510\times10^{-14}$	V^2/Hz
Cascode Devices	4.2190×10^{-15}	$4\ 2550\times10^{-15}$	V^2/Hz
Load Devices	6.8100×10^{-16}	6.9560×10^{-16}	V^2/Hz

"on", and a 3 pF capacitor was added to the input to model the detector capacitance The open-loop response was obtained by placing a test generator (0V DC, 1V AC) in the feedback loop and measuring the return signal [38] The result is shown in Figure 41 In simulation, the amplifier was found to have a DC gain of 4 93 kV/V (74 dB), a 3-dB bandwidth of 251Hz, and a phase margin of 85° Table 3 2 summarizes the frequency response simulation data The locations of the significant poles and zeroes (as defined in section 3 4) from simulation are compared with theoretical predictions

3.6.3 Gain Error Analysis

The simulation results of the previous chapter showed the integrator to have a considerable gain error (-12%) The previous simulation was done using an extracted netlist of the entire signal processing chain The simulator had difficulty in calculating an operating point, due mainly to the bi-stable nature of the frequency divider (toggle flop) The accuracy of this simulation was therefore in question Figure 42 shows the results of a simulation including only the switched integrator and detector Since the rest of the current-to-frequency converter was omitted, an ideal pulse voltage source (with 200msec period, 50% duty cycle, and 0-3V levels) was used to drive the reset switch The detector capacitance was again modeled as 3 pF, the detector current was set to 10 pA, and the integration capacitor was 0 545 pF (extracted value) The slope of the integrator output was measured as 18 32 V/V while it should ideally be 18 35 V/V (10 pA/0 545 pF) This result represents a gain error that is less than 0 2% Using the simulated value of DC amplifier open-loop gain (4 93kV/V), theory predicts an error of 0 29% (neglecting any leakage)

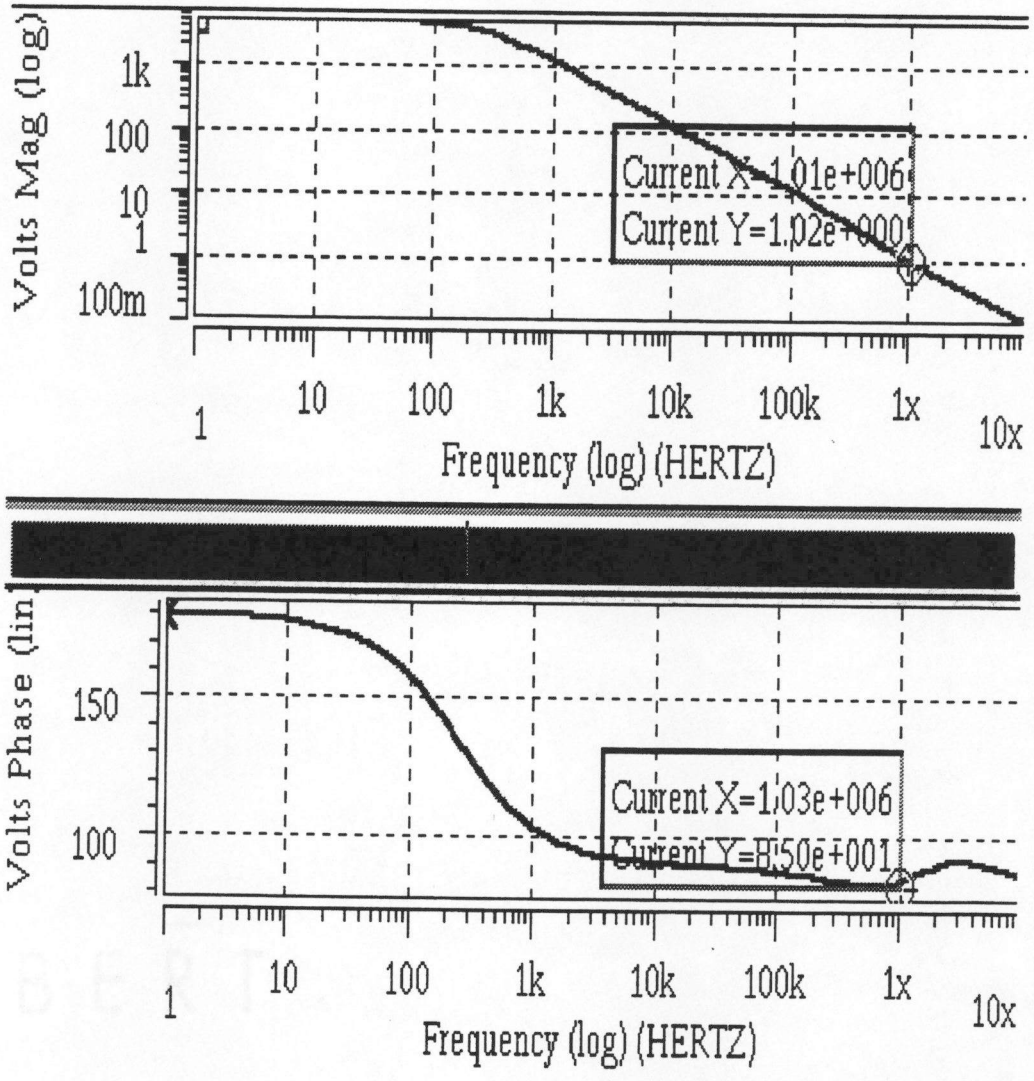

Figure 41 – LNA Frequency Response (Magnitude - upper trace, Phase – lower trace)

Table 3.2 LNA Frequency Response/Stability Simulation Results

	Hand Calculation	Simulation	Units
A_{v0} (DC Gain)	4.937	4.934	kV/V
f_{pdom}	253	251	Hz
f_{p2}	2 719	2 678	MHz
f_{p3}	765.628	772.842	KHz
f_{z3}	1.531	1.547	MHz
f_{zc}	1.420	1.421	MHz
Phase Margin	86	85	°

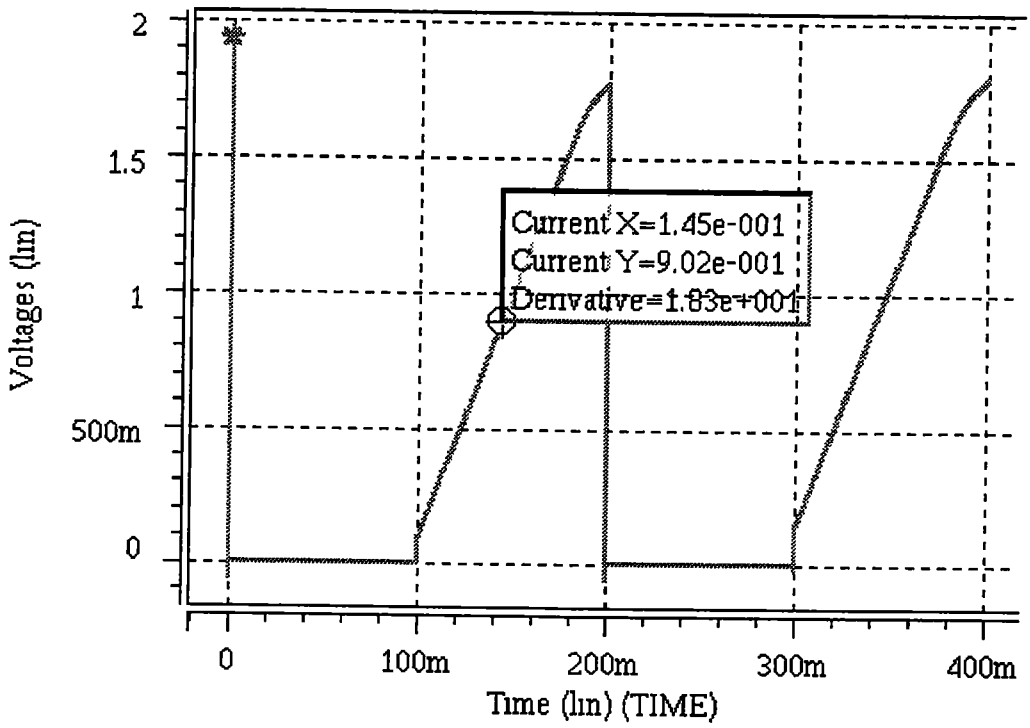

Figure 42 – Gain Error Measurement (Switched Integrator Output)

Chapter 4

Measurement Results

4.1 Test Setup

Figure 43 shows the basic test setup used in the evaluation of the microluminometer prototype The fabricated chip received from MOSIS was packaged in a standard 40-pin ceramic package This chip was mounted (socket) on an evaluation board that included external biasing and test fixtures The compensation node of the low-noise amplifier (see Figure 39) was brought out to a pin to allow for external compensation, if necessary The voltage on this pin was measured with a Tektronix TDS430A digital storage oscilloscope to monitor the operation of the amplifier The digital output of the system was monitored by an AT MIO-16X National Instruments data acquisition card (DAQ) inside a personal computer In addition, a program was created with Labview to control the DAQ and process the measurement data This program measured the pulse widths of the microluminometer digital output, converted these numbers to effective photocurrents, and calculated the statistics of the measured pulses

In order to simulate the bioluminescent output of the bioreporters [2], an optical instrument known as a monochrometer (ORIEL MS257) was used This

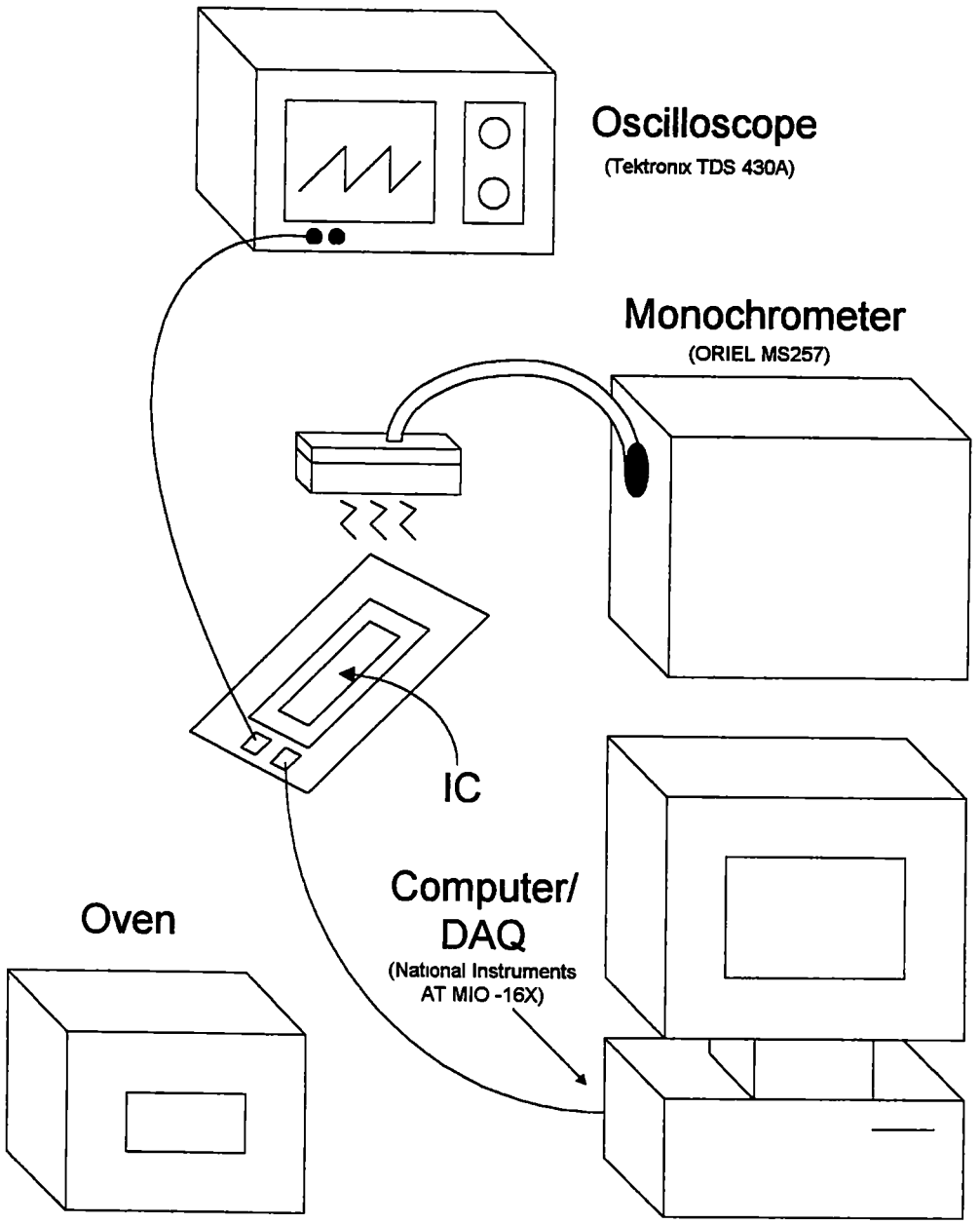

Figure 43 – Microluminometer Prototype Test Setup

device produces light purely at a specific wavelength In this testing, the wavelength of the light was set to 490 nm, corresponding to the candidate bioreporters The test fixture of the monochrometer consisted of a fiber-optic cable connected to a structure called an integrating sphere The purpose of the integrating sphere is to produce a uniform light output This particular structure was designed to fit directly on the ceramic chip package Also, measures were taken to eliminate any ambient light leakage Finally, a temperature-controlled oven was used to measure the effects of temperature change on the prototype performance

4.2 Initial Evaluation

Before test data was taken, the functionality of the prototype had to be verified As seen in Figure 44, the microuminometer did not function correctly at first The upper trace in this graph is the voltage at the compensation node of the amplifier (Figure 38), the bottom trace is the digital output (Figure 11) Ideally, the upper trace should have resembled the "sawtooth" waveform seen in simulaton (Figure 26) The plot in Figure 44 shows a waveform having two distinct regions, one with a low slope and one with a high slope It was determined that this error was caused by an inadequate reset time The system was not given enough time to settle during reset (25 μsec), and integration began with the amplifier in a low-gain state (low slope) Eventually, as seen in the figure, linear operation is restored and the system operates correctly (high slope) Luckily, the reset time was adjustable by the external biasing on the test board With the reset time adjusted to 70 μsec, the system functioned

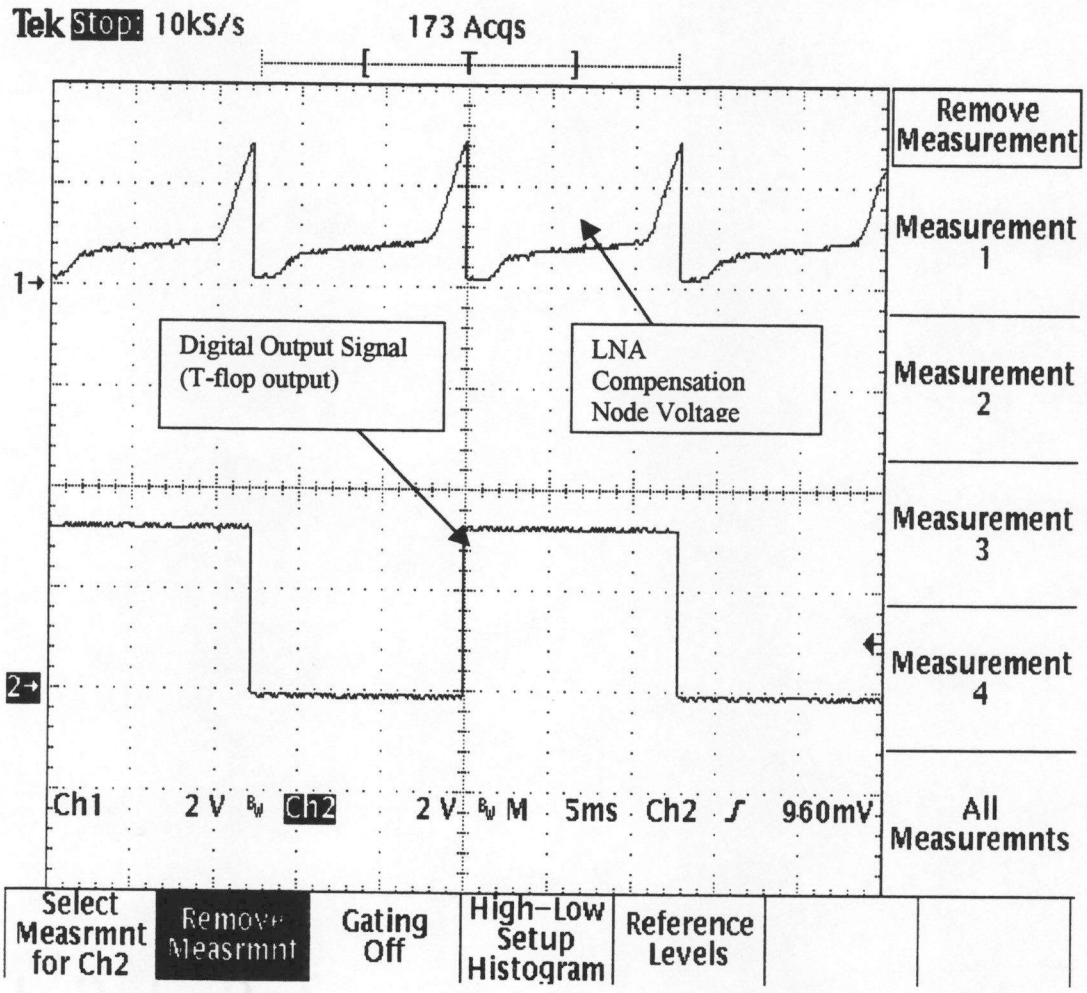

Figure 44 – System Error due to Inaccurate Reset

correctly, as seen in Figure 45.

Upon closer examination of the voltage waveforms at the time of reset, it was noticed that a large slewing effect, as described in section 2 3 3.1 3, was occurring The large voltage "dip" seen in Figure 46 indicates a large charging current flowing onto the detector capacitance This result indicates that the detector capacitance is actually much larger than modeled in simulation (3pF) Upon close inspection of the waveforms in Figure 46, one sees an offset that occurs at the beginning of the integration Initially, this error was attributed mainly to charge injection of the reset switch Observation of consecutive pulses showed, however, that the polarity of the offset was positive during a low-to-high transition of the digital output and negative during high-to-low transitions Figure 47 shows two traces superimposed on one another One shows the compensation node voltage at a low-to-high transition, and the other at a high-to-low transition This measurement indicated that spurious current injections from the digital circuitry were largely responsible for the offset Using separate power supplies for the digital and analog circuitry improved the situation

A final difficulty that was observed in initial testing was a level of measured leakage current that was much higher than expected Through testing, it was observed that the level of "leakage" could be varied by varying the value of the negative voltage used to bias the output buffer of the amplifier (Figure 34) Figure 48 illustrates the phenomenon that was occurring The source-to-bulk junction of the current source transistor of the buffer was being significantly forward-biased Since the photodiode is formed in the bulk, the forward current of the junction was being collected through

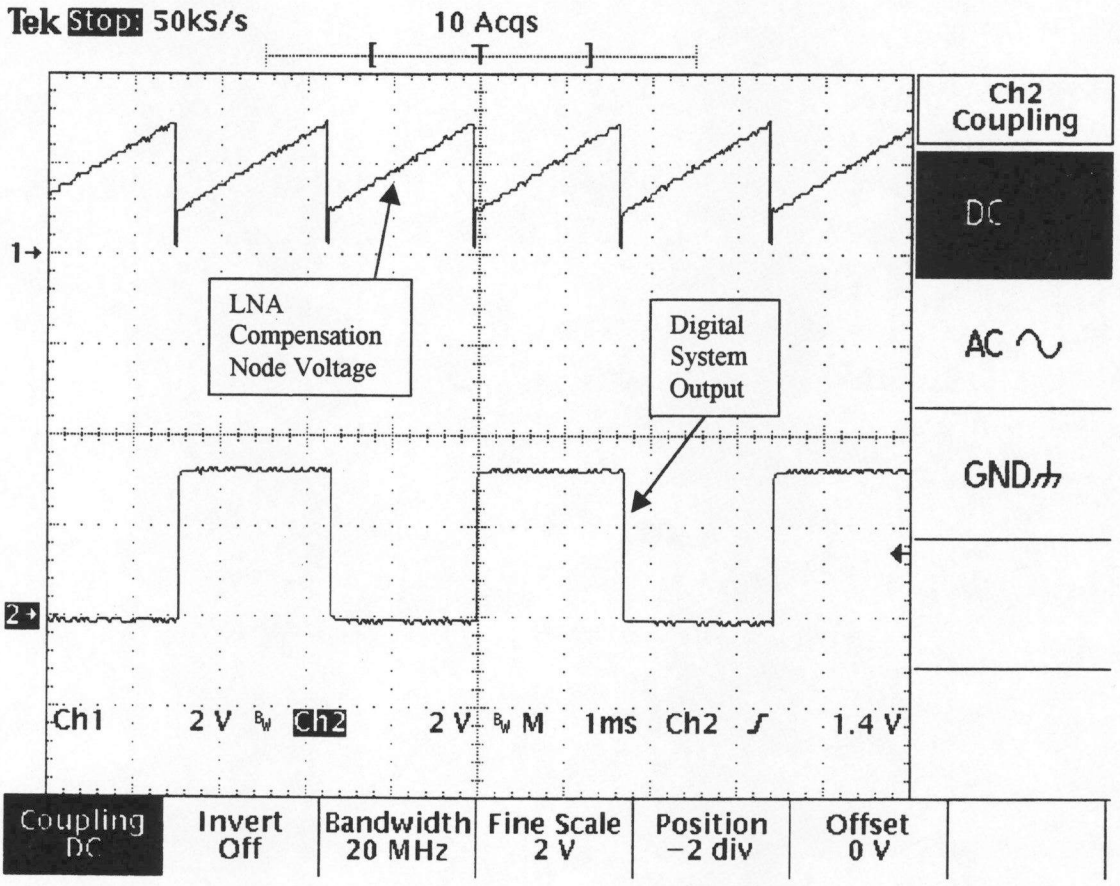

Figure 45 – System Operation with Adjusted Reset Time

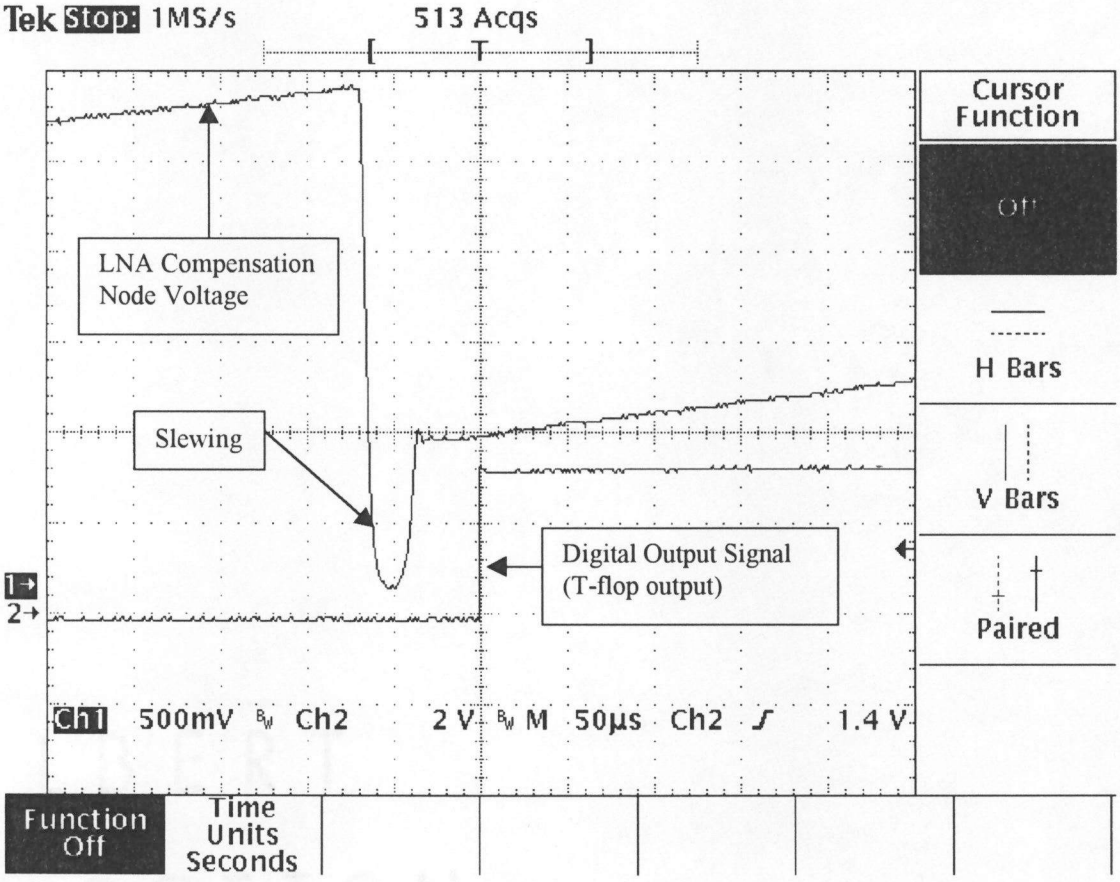

Figure 46 – Integrator Slewing during System Reset

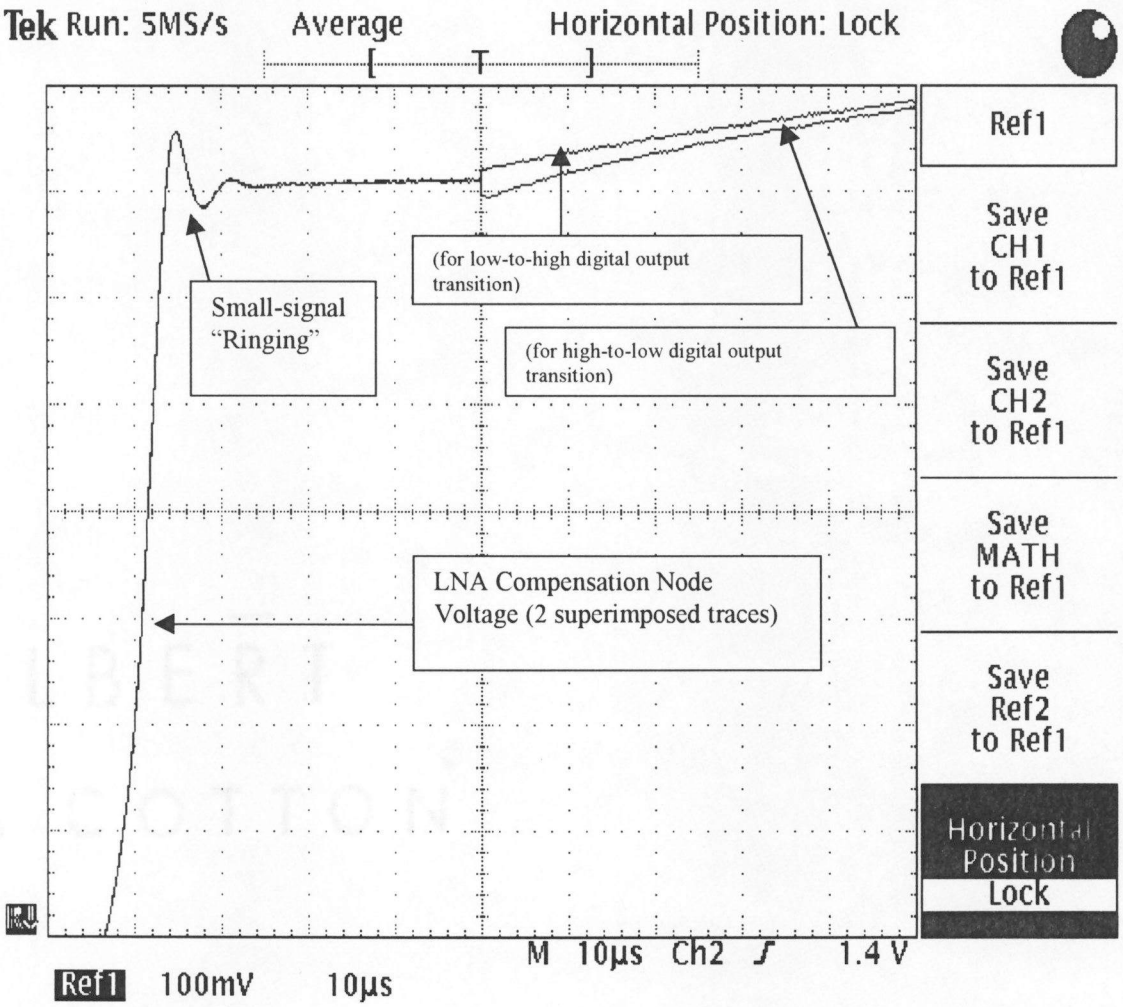

Figure 47 – Integrator Offset at System Reset

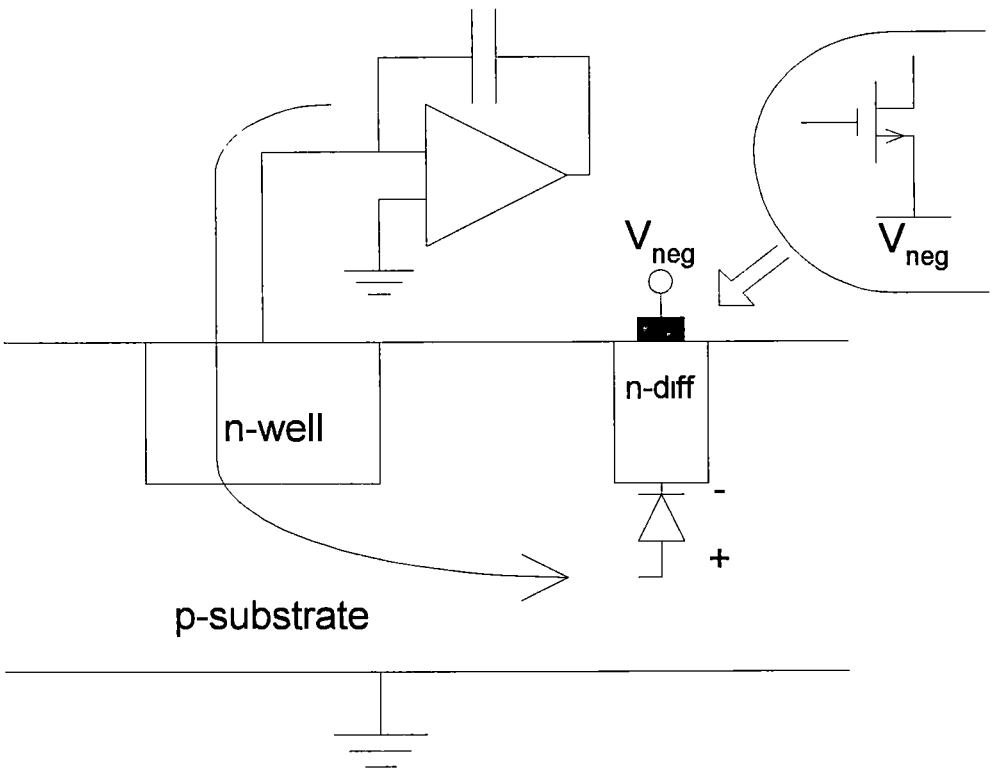

Figure 48 – Integration of Spurious Leakage in the Substrate

the detector and integrated as photocurrent by the integrator This problem was made negligible by lowering the magnitude of the negative voltage from –300 mV to –100mV

4.3 Test Results

4.3.1 Room Temperature Testing

4.3.1.1 Leakage Current

The first data taken in system testing was the measurement of the leakage current at room temperature The measured leakage for increasing reverse bias on the detector is shown in Figure 49 The detector bias was brought out to a pin on the IC package, allowing for adjustment Each photocurrent was calculated as the average of 100 sample pulse periods The leakage at zero-bias could not be measured One possible explanation for the inability to measure zero-bias detector leakage is that, for low detector bias, the diode leakage and the leakage of the reset switch can become equal This current cancellation would cause the integrator to be "locked up" indefinitely in the absence of luminescence Another possible explanation is that the offset voltage of the amplifier and input error signal actually apply a forward bias to the detector when the detector bias is set to zero This forward current would cause the integrator output to saturate at the lower supply rail

Figure 50 shows the sample standard deviation (σ) and normalized σvalues of the measured leakage current for increasing detector bias The data was obtained by

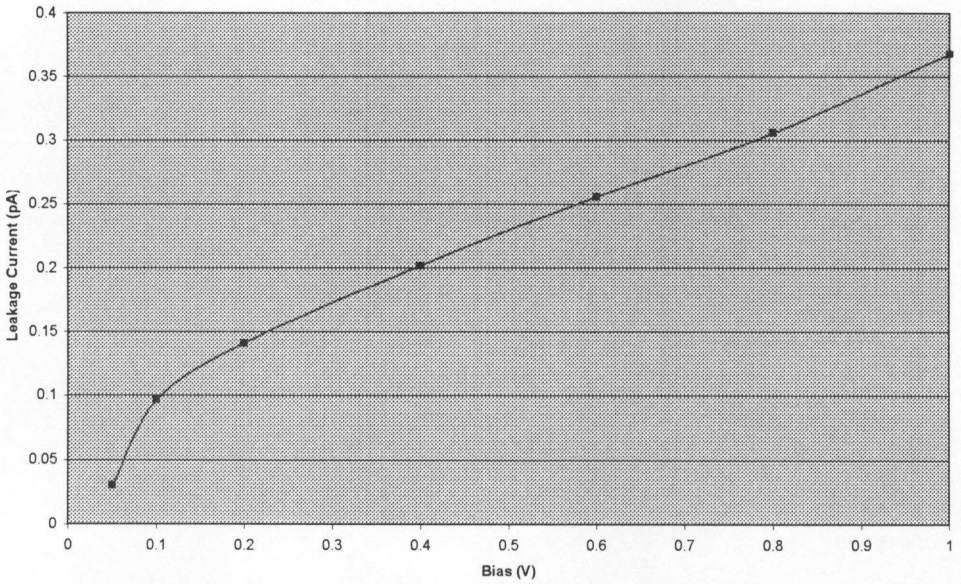

Figure 49 – Detector Leakage vs. Reverse Bias (Room Temp.)

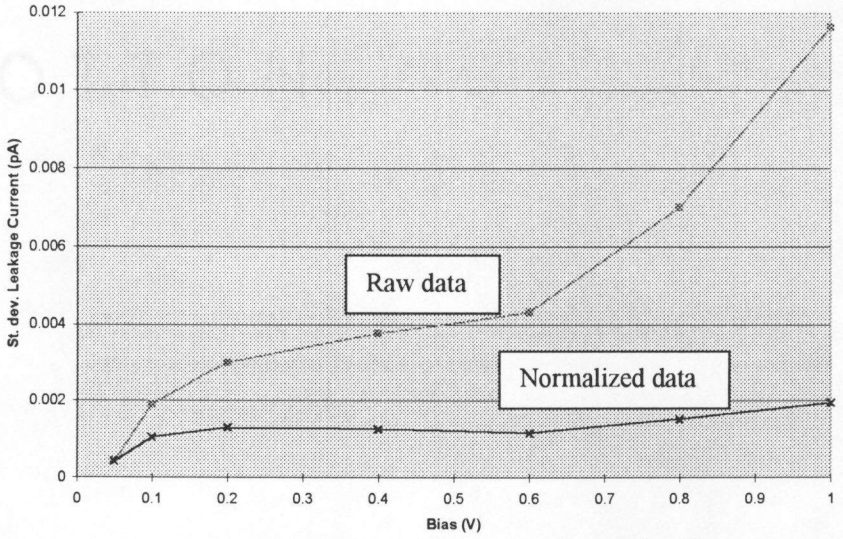

Figure 50 – σ and Normalized σ Leakage vs. Reverse Bias (Room Temp.)

calculating the standard deviation of the data (100 samples) taken at each detector bias The raw data indicates that the standard deviation of the effective detector leakage increases with increasing detector bias Increased detector bias increases the leakage current, and therefore the detector noise One fact that must be remembered is that the integration period is decreased when the detector bias voltage is increased, since the detector bias is also the baseline level of the integrator output ramp Normalizing the σ of the leakage current data to the longest integration period (the average measured pulse period at 50mV detector bias) results in a value that remains nearly constant, with increasing bias The normalization is performed through the following multiplication

$$(Normalized\_\sigma\_data) = (\sigma\_Data)\sqrt{\frac{T_{int(max)}}{T_{int}}}\quad , \qquad (4\ 1)$$

where T_{int} is the integration period, or pulse width of the integrator output Figure 51 shows the σ leakage versus integration period Unfortunately, all of the measurements were done with a comparator threshold voltage of 1 5 V By varying the threshold, the integration period could have been varied without changing the detector bias (leakage)

The leakage current data gives an indication of the minimum detectable signal (MDS) Unfortunately the leakage could not be measured at zero bias, so a true MDS could not be determined However, an MDS was calculated at the other detector bias

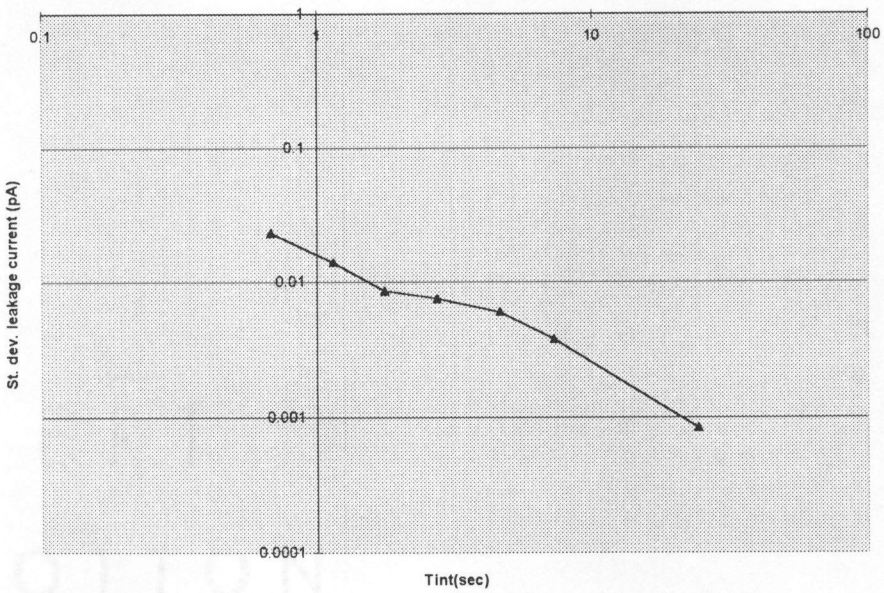

Figure 51 – σ Leakage vs. Integration Period (log-log scale)

points The MDS was defined as a level that is equal to two standard deviations of the measured leakage data The minimum detectable signal is shown in Figure 52 versus detector bias

4.3.1.2 Photocurrent Measurement

Figure 53 shows the measured photocurrent versus detector bias (at room temperature) This graph was generated by subtracting the mean leakage current of Figure 49 from the measured current of the illuminated chip The four traces represent four different intensities of light The photon rates were approximated using data from a calibration diode and knowledge of the photodetector active area Figure 54 shows this same data converted to a quantum efficiency for the lowest light level (1.6×10^7 photons/ sec) Figure 54 shows the detector to have a an effective quantum efficiency that varies between 39% and 80% for a detector bias voltage from 0V to 1V The quantum efficiency was calculated using the calculated photon rate and the area of the calibration diode

A signal-to-noise ratio was defined as the mean photocurrent (Figure 53) divided by the σ value of the measured photocurrent Figure 55 shows this data for the four measured intensities of light The numbers (1, 2, 3,and 4) on the graph legend denote increasing levels of light The SNR decreases with increasing detector bias The increase in bias not only increases leakage, but decreases integration period Figure 56 shows the SNR data normalized to the longest integration period (as defined by Equation 4 1) This graph, shows the normalized SNR to be close to 35dB, except

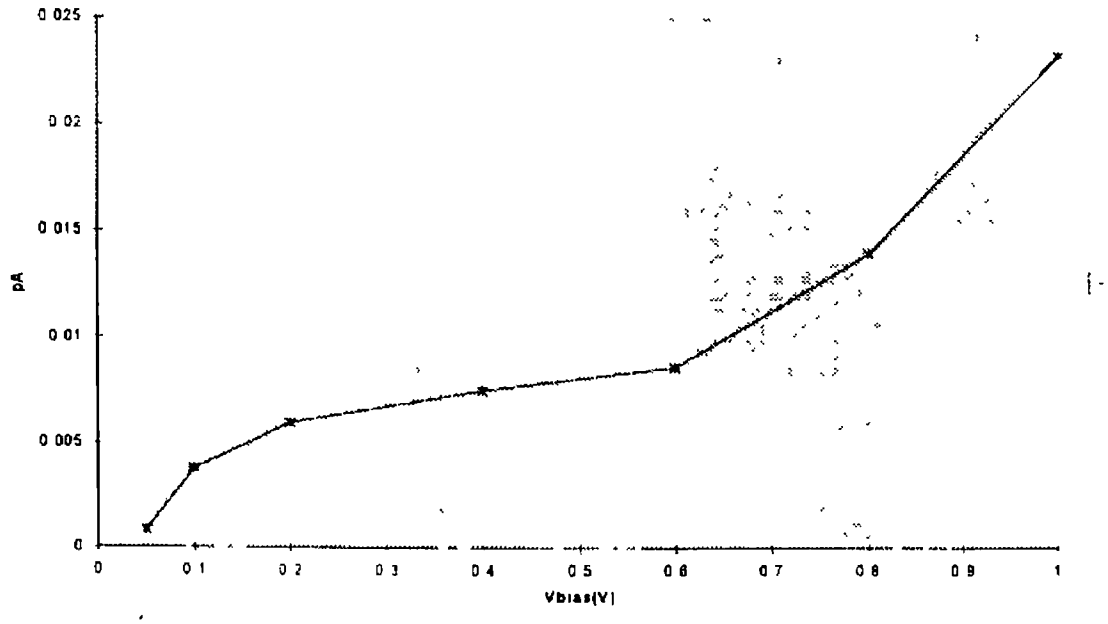

Figure 52 – Minimum Detectable Signal (Detector Current)

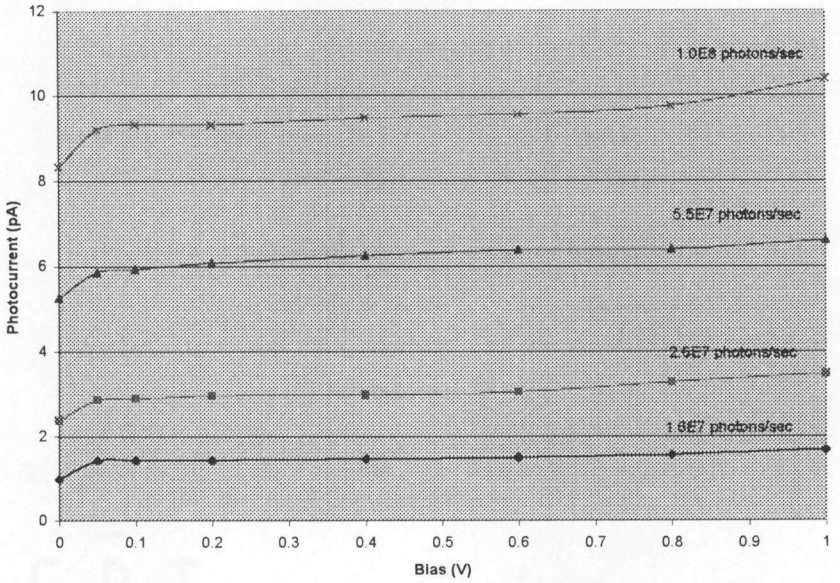

Figure 53 – Average Photocurrent vs. Detector Bias (Room Temperature)

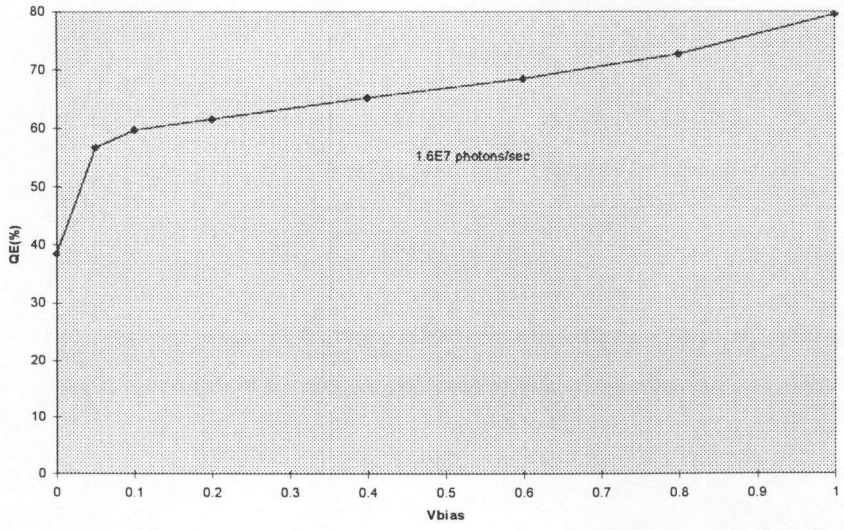

Figure 54 – Quantum Efficiency vs. Detector Bias (lowest light level)

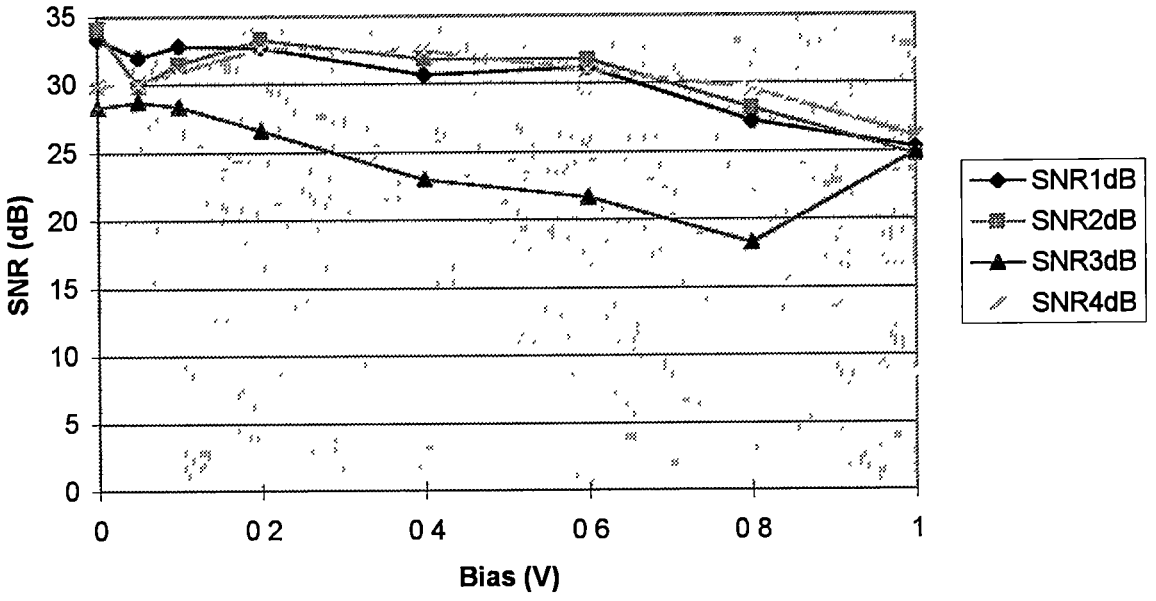

Figure 55 – Signal-to-Noise Ratio (dB)

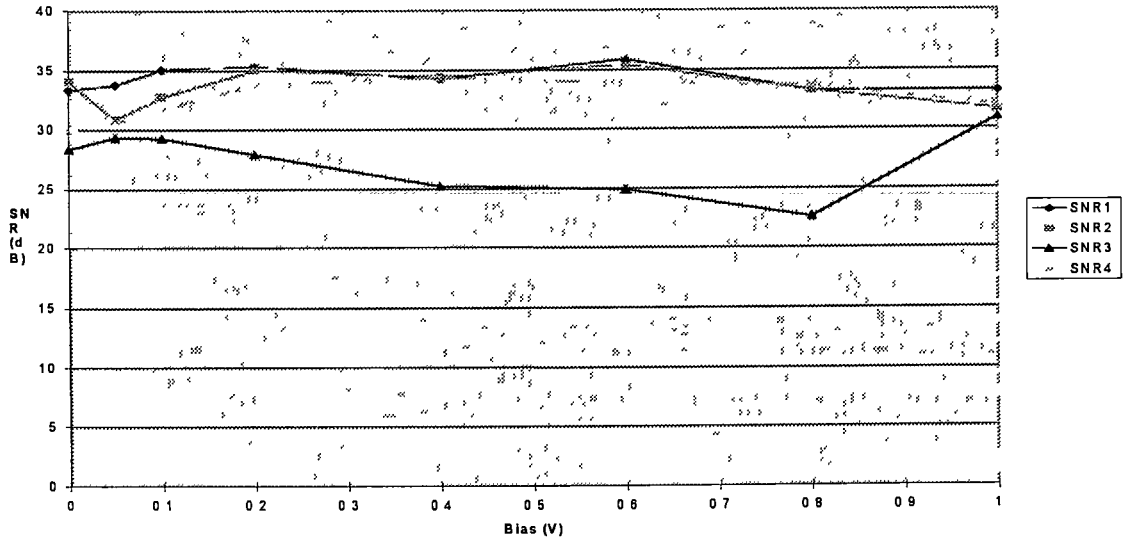

Figure 56 – Normalized Signal-to-Noise Ratio (dB)

for the one trace that represents the data for a light intensity of 5 5×10^7 photons/sec The reason for this discrepancy is unknown

4.3.2 Temperature Effects

Since the BBIC is intended for use as an environmental sensor, the effect of temperature changes should be considered One obvious effect is increased detector leakage current Figure 57 shows the measured leakage current for three different temperatures 40, 42 5, and 45 degrees Celsius The increase in leakage with temperature becomes greater at larger reverse biases This graph shows that a change of as much as 1 pA occurred for a 5 degree Celsius increase in temperature This increase would be seen as a signal increase in a measurement

The effect of temperature change on the photocurrent level was also measured Figure 58 shows the measured photocurrent for the lowest light level (1 6×10^7 photons/sec) at 40 and 45 degrees Celsius This graph shows a decrease of approximately 200 fA for a 5-degree increase in temperature This effect is not predicted by the detector physics, and is believed to be due to measurement error Finally, Figure 58 shows no photocurrent for zero bias on the detector It was postulated that, at these higher temperatures, the leakage of the switch became comparable to the detector current, causing the system to "lock up"

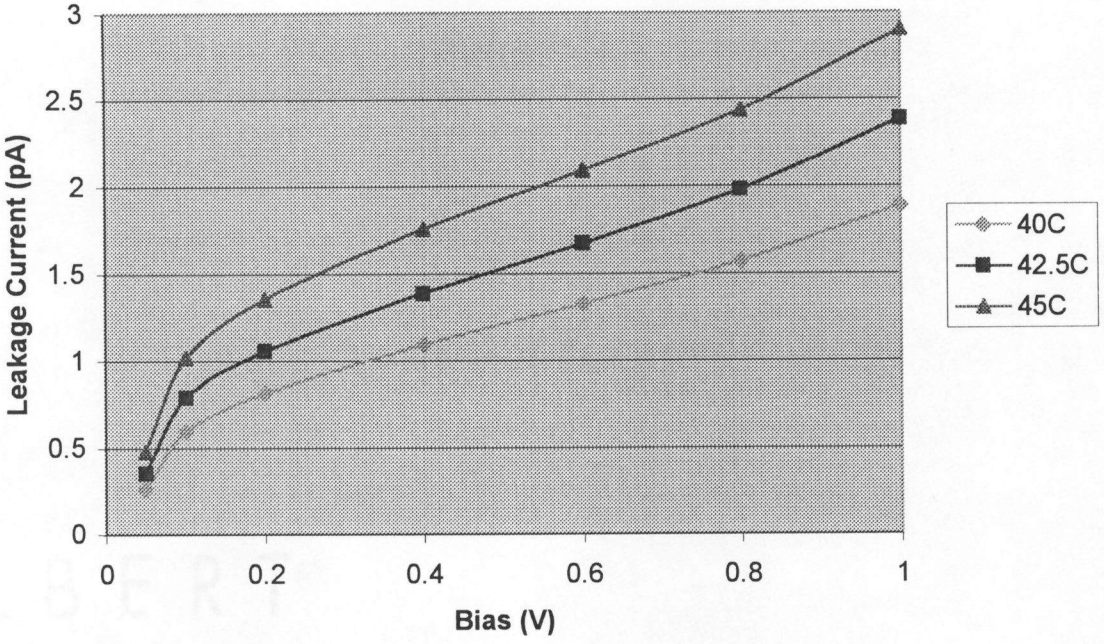

Figure 57 – Detector Leakage vs. Temperature and Bias

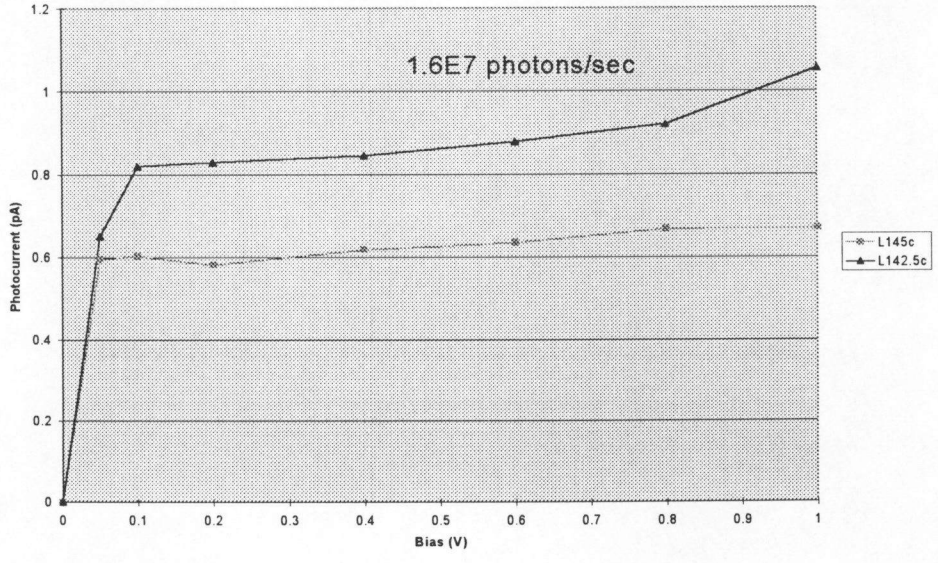

Figure 58 – Photocurrent vs. Temperature and Bias

Chapter 5

Conclusions and Future Work

5.1 Conclusions

A low-noise microluminometer was designed, and a prototype was fabricated in the HP 0 5 μm CMOS process The microluminometer was designed as part of a bioluminescent bioreporter integrated circuit (BBIC), a hybrid electronic/biological chemical sensor The prototype, after initial adjustments, demonstrated the ability to detect luminescence and produce a digital signal in response The performance of the system was evaluated through laboratory testing with a calibrated light source Analysis of the digital data allowed for an evaluation of the detection limits of the system It was found that the integrated photodetector had a quantum efficiency on the order of 60% to 70% The leakage of the detector at room temperature increased with increasing bias, varying from less than 50 fA (at 50 mV bias) to just over 350 fA at (1 V bias) The noise of the measurement was found to vary inversely with integration time

In this testing, the minimum light level (at 490 nm) produced by the laboratory light source (1 6× 10^7 photons/sec) was successfully detected, producing a measured photocurrent of approximately 1 75 pA The lowest MDS would be achievable for

this system at zero detector bias Unfortunately, the system showed peculiar performance at low detector bias Below 50 mV, the response of the system was seen to drop off dramatically Possible explanations for this behavior involve switch leakage and amplifier offset voltage Another possible explanation would be a collapse of the detector quantum efficiency at low bias

5.2 Future Work

There is a definite opportunity for future work on this project One area of future study should be the performance of the system at low detector bias Zero bias ideally represents the optimum configuration for this measurement, so any system problem preventing this optimum performance should be dealt with Possible future solutions include an improved low-leakage reset switch and an autozeroing function to reduce any amplifier offset Another future improvement would be to increase the open-loop gain of the low-noise amplifier This improvement is believed to be necessary, since the detector capacitance is likely two orders of magnitude higher than initially modeled The detector capacitance could also be reduced through modification of the detector layout Another improvement would be the elimination of the negative bias voltage used in the amplifier output buffer A low-dropout output structure could be used to allow for very low detector bias without the need to generate a negative voltage This improvement would also eliminate the "leakage" problem associated with the negative voltage Still another improvement would involve the use of a "dummy" channel in the system This channel would be matched

to the actual signal channel, but would only measure detector leakage This method would allow for a leakage cancellation scheme (through subtraction of the two output digital signals) that should track temperature variations

Another area of future work should be in the area of testing The results presented in this thesis successfully validated design theory, but did not truly push the detection limits of the system Future testing should explore the effects of increasing the integration time Studies should be made in which the comparator threshold voltage is varied Also, one limitation of the results in this thesis is that all data points were averages of only 100 sample pulses The effect of increasing sample size should be explored Finally, there are areas in this project that have yet to be worked on These include "temperature-independent" biasing, low-noise comparator design, and synthesis of the digital circuitry (counter/timer and transmitter control)

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APPENDICES

Appendix 1

```
* N71S SPICE BSIM1 (Berkeley Level 4; HSPICE Level 13) PARAMETERS

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*NMOS PARAMETERS
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+  8.77145E-01, 0.00000E+00, 0.00000E+00
+  7.89767E-01, 2.98087E-02, 3.40730E-02
+  3 29058E-02, 5 64098E-02,-3.49985E-03
+ -2 01339E-03, 1.21136E-02, 1.65202E-03
+  4.85180E+02,1.64434E-001,4.21899E-001
+  2.01813E-01, 1.35619E-01,-9.80703E-02
+  3 49401E-02, 4.12031E-02,-1.05688E-02
+  1.20726E+01,-9.73262E+00, 1.33355E+01
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+ -9 94060E-04,-1.58519E-03,-1.49013E-03
+ -2.86039E-03,-9.74303E-03, 1.58243E-02
+ -1.37325E-03, 2 31179E-03, 3.27748E-04
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+  1.90705E+00,-1 98358E+00, 1 54775E+01
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+KF=1 32E-24
*
* Gate Oxide Thickness is 96 Angstroms
*
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*PMOS PARAMETERS
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+  7.90466E-01, 0.00000E+00, 0.00000E+00
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Appendix 2

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* Ext2spice Version      ORNL 2.6 4 <=> Tue Jan 27 17:32:51 EST 1998
*           Options      -m -n -M -N -m -n -mg -M -N -h -g -n -mm -V
*
** Subcircuit definition for dfrf311
** Extraction file is /msd23/patterson/lnafb/dfrf311.ext
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M2 4 1 3 3 CMOSP W=10.15U L=0.70U GEO=0
M3 5 6 3 3 CMOSP W=9.10U L=0.70U GEO=0
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M5 7 4 8 3 CMOSP W=7.70U L=0.70U GEO=0
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M26 21 1 13 11 CMOSN W=4.55U L=0.70U GEO=0
M27 13 4 22 11 CMOSN W=5.95U L=0.70U GEO=0
M28 22 15 23 11 CMOSN W=5.95U L=0.70U GEO=0
M29 23 10 11 11 CMOSN W=5.95U L=0.70U GEO=0
M30 15 13 11 11 CMOSN W=7.35U L=0.70U GEO=0
M31 16 15 11 11 CMOSN W=4.20U L=0 70U GEO=0
C1 3 10 1.0F
C2 1 3 1.0F
C3 11 2 1.0F
C4 7 3 1.0F
C5 9 11 1.0F
C6 3 15 1.0F
C7 11 10 2.0F
```

```
C8 1 11 1.0F
C9 7 11 1.0F
C10 3 4 2.0F
C11 11 15 1.0F
C12 13 3 1.0F
C13 11 4 1.0F
C14 8 3 1.0F
C15 9 1 2 0F
C16 13 4 1.0F
C17 9 7 1.0F
C18 13 11 1.0F
C19 9 3 1 0F
C20 16 0 4.0F
C21 15 0 9.0F
C22 9 0 9.0F
C23 4 0 9.0F
C24 7 0 11.0F
C25 1 0 22.0F
C26 13 0 9.0F
C27 10 0 14.0F
C28 6 0 3.0F
C29 11 0 23.0F
C30 2 0 3.0F
C31 3 0 26.0F
C32 8 0 2.0F
*** Node Listing for subckt:  dfrf311
** N0                          ==  IdealGND
** N1                [U=8]     ==  21
** N2                [U=3]     ==  CLK2
** N3                [U=27]    ==  Vdd'
** N4                [U=7]     ==  25
** N5                [U=2]     ==  120
** N6                [U=3]     ==  DATA1
** N7                [U=6]     ==  22
** N8                [U=3]     ==  121
** N9                [U=6]     ==  24
** N10               [U=6]     ==  RST3
** N11               [U=26]    ==  GND'
** N12               [U=2]     ==  123
** N13               [U=7]     ==  28
** N14               [U=2]     ==  124
** N15               [U=7]     ==  Q
** N16               [U=3]     ==  Q_b
** N17               [U=2]     ==  150
** N18               [U=2]     ==  152
** N19               [U=2]     ==  151
** N20               [U=2]     ==  153
** N21               [U=2]     ==  154
** N22               [U=2]     ==  155
** N23               [U=2]     ==  156
.ENDS
** Subcircuit definition for dsc
** Extraction file is /msd23/patterson/lnafb/dsc.ext
.SUBCKT dsc 1 2 3 4 26 100 110
```

```
M1 7 2 6 110 CMOSN M=16 W=17.50U L=0.70U GEO=3
M2 8 1 6 110 CMOSN M=16 W=17.50U L=0.70U GEO=3
M3 7 7 100 100 CMOSP W=4.20U L=0.70U GEO=0
M4 8 7 100 100 CMOSP W=4.20U L=0.70U GEO=0
M5 6 3 110 110 CMOSN W=4.20U L=0.70U GEO=0
M6 11 8 100 100 CMOSP W=4.20U L=0.70U GEO=0
M7 10 9 110 110 CMOSN W=4.20U L=0.70U GEO=0
M8 9 7 100 100 CMOSP W=4.20U L=0.70U GEO=0
M9 9 9 110 110 CMOSN W=4.20U L=0.70U GEO=0
M11 5 4 11 100 CMOSP W=8.40U L=0.70U GEO=0
M12 5 4 10 110 CMOSN W=8.40U L=0.70U GEO=0
M13 25 5 100 100 CMOSP W=8.75U L=0.70U GEO=0
M14 25 5 110 110 CMOSN W=3.50U L=0.70U GEO=0
M15 26 25 100 100 CMOSP W=21.00U L=0.70U GEO=0
M16 26 25 110 110 CMOSN W=8.75U L=0.70U GEO=0
C1 7 6 2.0F
C2 2 1 3.0F
C3 8 6 2.0F
C4 7 8 1.0F
C5 7 0 55.0F
C6 100 0 24.0F
C7 10 0 4 0F
C8 11 0 5.0F
C9 25 0 11.0F
C10 26 0 9 0F
C11 110 0 67.0F
C12 1 0 44.0F
C13 2 0 42.0F
C14 3 0 3.0F
C15 4 0 8.0F
C16 6 0 80 0F
C17 8 0 56.0F
C18 9 0 24.0F
C19 5 0 13.0F
*** Node Listing for subckt:  dsc
** N0                          ==  IdealGND
** N1                [U=2]     ==  IN+
** N2                [U=2]     ==  IN-
** N3                [U=2]     ==  IBIAS
** N4                [U=3]     ==  Vmid
** N5                [U=4]     ==  8_256_171#
** N6                [U=3]     ==  N6
** N7                [U=5]     ==  M10
** N8                [U=3]     ==  N8
** N9                [U=4]     ==  N9
** N10               [U=2]     ==  N10
** N11               [U=2]     ==  N11
** N25               [U=4]     ==  N25
** N26               [U=3]     ==  N26
** N100              [U=14]    ==  Vdd
** N110              [U=14]    ==  Vss
 ENDS
** Subcircuit definition for one_shot2r
** Extraction file is /msd23/patterson/lnafb/one_shot2r.ext
```

```
.SUBCKT one_shot2r 10 14 50 100 101
C1 6 101 HPCAP50 SCALE=350.59
C1P 101 101 HPCAP50P SCALE=350.6
* C1=1248.12FF C1P=0.04FF
M1 5 6 101 101 CMOSN W=1.40U L=0.70U GEO=0
M2 100 3 5 101 CMOSN W=1.05U L=0.70U GEO=0
M3 3 6 5 101 CMOSN W=1.05U L=0.70U GEO=0
M4 4 6 100 100 CMOSP W=2.10U L=0.70U GEO=0
M5 101 3 4 100 CMOSP W=1.05U L=0.70U GEO=0
M6 3 6 4 100 CMOSP W=1.05U L=0.70U GEO=0
M7 6 8 101 101 CMOSN W=1.40U L=3.50U GEO=0
M8 6 50 100 100 CMOSP W=2.80U L=1.40U GEO=0
M9 100 50 100 100 CMOSP W=1.40U L=1.40U GEO=0
M10 13 10 100 100 CMOSP W=1.05U L=0.70U GEO=0
M11 11 13 100 100 CMOSP W=1 05U L=0.70U GEO=0
M12 11 8 100 100 CMOSP W=1.05U L=0.70U GEO=0
M13 8 11 100 100 CMOSP W=1.05U L=0.70U GEO=0
M14 8 3 100 100 CMOSP W=1.05U L=0.70U GEO=0
M15 13 10 101 101 CMOSN W=1.05U L=0.70U GEO=0
M16 1 13 11 101 CMOSN W=1.05U L=0.70U GEO=0
M17 1 8 101 101 CMOSN W=1 05U L=0.70U GEO=0
M18 12 11 8 101 CMOSN W=1.05U L=0.70U GEO=0
M19 12 3 101 101 CMOSN W=1 05U L=0.70U GEO=0
M20 14 8 100 100 CMOSP W=3 85U L=0.70U GEO=0
M21 14 8 101 101 CMOSN W=1.40U L=0.70U GEO=0
C2 6 101 1.0F
C3 101 8 3.0F
C4 100 3 1.0F
C5 11 0 5.0F
C6 6 0 56.0F
C7 50 0 3.0F
C8 101 0 97.0F
C9 10 0 4.0F
C10 13 0 4.0F
C11 14 0 6.0F
C12 3 0 34.0F
C13 8 0 34.0F
C14 100 0 102.0F
*** Node Listing for subckt·  one_shot2r
** N0                          ==  IdealGND
** N1                 [U=2]     ==  8_275_228#
** N3                 [U=6]     ==  reset
** N4                 [U=3]     ==  N4
** N5                 [U=3]     ==  N5
** N6                 [U=7]     ==  top_plate
** N8                 [U=8]     ==  Q_B
** N10                [U=3]     ==  IN
** N11                [U=5]     ==  Q
** N12                [U=2]     ==  N12
** N13                [U=4]     ==  N13
** N14                [U=3]     ==  N14
** N50                [U=3]     ==  Vbias
** N100               [U=23]    ==  N100
** N101               [U=20]    ==  BOT_PLATE
```

```
.ENDS
** Subcircuit definition for switch_prot
** Extraction file is /msd23/patterson/lnafb/switch_prot.ext
.SUBCKT switch_prot 1 2 3 4 110
C1 2 3 HPCAP50 SCALE=153.12
C1P 3 3 HPCAP50P SCALE=153.1
* C1=545.12FF C1P=0.02FF
Msw 3 1 4 110 CMOSN M=2 W=7.00U L=0 70U GEO=0
C2 3 2 2.0F
C3 110 0 71.0F
C4 2 0 17.0F
C5 3 0 15.0F
C6 1 0 3.0F
C7 4 0 6.0F
*** Node Listing for subckt:  switch_prot
** N0                          ==  IdealGND
** N1                [U=2]     ==  bias
** N2                [U=2]     ==  top_plate
** N3                [U=4]     ==  bottom_plate
** N4                [U=2]     ==  8_5_3#
** N110              [U=2]     ==  N110
.ENDS
** Subcircuit definition for rc2
** Extraction file is /msd23/patterson/lnafb/rc2.ext
.SUBCKT rc2 1 2 3
Cint 2 1 HPCAP50 SCALE=253.57
CintP 1 1 HPCAP50P SCALE=253.6
* Cint=902.73FF CintP=0.03FF
Rlp 3 2 RHPNWELL50 SCALE=8 80
* Rlp=7224.8 (width=3.50U)
C1 1 0 35.0F
C2 2 0 36.0F
C3 3 0 7.0F
*** Node Listing for subckt:  rc2
** N0                          ==  IdealGND
** N1                [U=3]     ==  BOT_PLATE
** N2                [U=3]     ==  Anode
** N3                [U=2]     ==  Cathode
************************************************************
.ENDS
** Subcircuit definition for lna
** Extraction file is /msd23/patterson/lnafb/prot1.ext
.SUBCKT lna 1 2 3 4 7 10 11 12 13 14 15
Cc 10 1 HPCAP50 SCALE=3915 59
CcP 1 1 HPCAP50P SCALE=3915.6
* Cc=13939.50FF CcP=0.39FF
M1 5 3 2 2 CMOSP M=10 W=21.00U L=7.00U GEO=1
M2 6 4 2 2 CMOSP M=10 W=21.00U L=7.00U GEO=1
M3 8 7 5 1 CMOSN M=4 W=25.20U L=28.00U GEO=1
M4 9 7 6 1 CMOSN M=4 W=25.20U L=28.00U GEO=1
M5 8 8 13 13 CMOSP M=2 W=14.00U L=28.00U GEO=1
M6 9 8 13 13 CMOSP M=2 W=14.00U L=28.00U GEO=1
M7 7 7 11 1 CMOSN W=25.20U L=7.00U GEO=1
M8 13 9 12 1 CMOSN W=7.00U L=2.80U GEO=1
```

```
M9 12 14 15 1 CMOSN W=7.00U L=2.80U GEO=1
M10 14 14 15 1 CMOSN W=7.00U L=2 80U GEO=1
R1 5 1 RHPPOLYSB50 SCALE=335.00
* R1=30150.0 (width=1.75U)
R2 6 1 RHPPOLYSB50 SCALE=335.00
* R2=30150.0 (width=1.75U)
R3 11 1 RHPPOLYSB50 SCALE=335.00
* R3=30150.0 (width=1.75U)
Rc 10 9 RHPPOLYSB50 SCALE=90.00
* Rc=8100.0 (width=1.75U)
*Rdummy1 16 17 RHPPOLYSB50 SCALE=67.00
* Rdummy1=6030.0 (width=1.75U)
*Rdummy2 30 31 RHPPOLYSB50 SCALE=67.00
* Rdummy2=6030.0 (width=1.75U)
C1 5 6 4.0F
C2 12 1 1.0F
C3 8 13 1.0F
C4 9 6 1.0F
C5 5 1 2.0F
C6 15 1 1.0F
C7 8 5 1.0F
C8 10 1 1.0F
*C9 2 4 17.0F
C10 1 6 30.0F
C11 14 13 1 0F
C12 7 5 1.0F
C13 2 3 17.0F
C14 9 8 1.0F
C15 10 0 50.0F
C16 3 0 196.0F
C17 4 0 199.0F
*C18 17 0 1.0F
*C19 31 0 1.0F
C20 15 0 8.0F
C21 7 0 257.0F
C22 11 0 81.0F
*C23 16 0 1.0F
C24 12 0 7.0F
C25 2 0 558.0F
C26 5 0 212.0F
C27 6 0 236 0F
C28 1 0 870.0F
C29 8 0 173.0F
C30 9 0 126.0F
C31 13 0 231.0F
*C32 30 0 1.0F
C33 14 0 31.0F
*** Node Listing for subckt:  lna
** N0                          ==  IdealGND
** N1              [U=12]      ==  GND'
** N2              [U=5]       ==  N2
** N3              [U=2]       ==  Vin+
** N4              [U=2]       ==  Vin-
** N5              [U=3]       ==  N5
```

```
** N6                    [U=3]      ==  N6
** N7                    [U=5]      ==  Ivb1
** N8                    [U=4]      ==  N8
** N9                    [U=4]      ==  N9
** N10                   [U=3]      ==  Comp
** N11                   [U=3]      ==  Ivb2
** N12                   [U=3]      ==  OUT
** N13                   [U=6]      ==  Vdd'
** N14                   [U=4]      ==  Ibuff
** N15                   [U=3]      ==  Vneg
** N16                   [U=1]      ==  8_2500_1342#
** N17                   [U=1]      ==  8_2500_2024#
** N30                   [U=1]      ==  8_2852_1342#
** N31                   [U=1]      ==  8_2852_2024#
.ENDS
** Subcircuit definition for dsc_bias2
** Extraction file is /msd23/patterson/lnafb/dsc_bias2.ext
.SUBCKT dsc_bias2 1 110
C1 1 110 HPCAP50 SCALE=110.25
C1P 110 110 HPCAP50P SCALE=110.2
* C1=392.49FF C1P=0 01FF
M1 1 1 110 110 CMOSN W=4.20U L=0.70U GEO=0
C2 110 0 38.0F
C3 1 0 21.0F
*** Node Listing for subckt:  dsc_bias2
** N0                          ==  IdealGND
** N1                  [U=4]   ==  top_plate
** N110                [U=5]   ==  BOT_PLATE
.ENDS
** Subcircuit definition for os_bias
** Extraction file is /msd23/patterson/lnafb/os_bias.ext
.SUBCKT os_bias 1 2 100
C1 1 100 HPCAP50 SCALE=136 71
C1P 100 100 HPCAP50P SCALE=136.7
* C1=486.69FF C1P=0.01FF
M1 1 1 100 100 CMOSP M=8 W=2 80U L=1 40U GEO=0
C2 100 2 1.0F
C3 1 0 25.0F
C4 2 0 21 0F
C5 100 0 32.0F
*** Node Listing for subckt:  os_bias
** N0                          ==  IdealGND
** N1                  [U=4]   ==  bias
** N2                  [U=1]   ==  guard
** N100                [U=5]   ==  N100
.ENDS

** Subcircuit definition for cfc
** Extraction file is /msd23/patterson/blue_spec/strip/prot1sp.ext
.SUBCKT cfc 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 21 22 23
** Instance-id:   dfrf311_0
X1 17 9 18 19 9 1 13 19 dfrf311
** Instance-id:   dsc_0
X2 20 14 8 4 21 9 1 dsc
```

```
** Instance-id.   one_shot2r_0
X3 21 17 10 9 1 one_shot2r
** Instance-id:   switch_0
X4 17 22 23 22 1 switch_prot
** Instance-id:   rc2_0
X5 1 20 23 rc2
** Instance-id.   prot1_0
X6 15 5 6 22 12 7 2 23 11 16 3 lna
*Vsw 100 0 3
C1 3 15 2.0F
C2 1 9 2.0F
C3 19 1 2.0F
C4 18 9 1.0F
C5 1 19 1.0F
C6 3 15 3.0F
C7 22 15 1 0F
C8 22 1 3.0F
C9 8 9 6 0F
C10 20 1 11.0F
C11 16 9 4.0F
C12 21 9 7.0F
C13 17 1 10.0F
C14 14 1 1.0F
C15 10 9 16.0F
C16 8 1 3.0F
C17 23 1 3.0F
C18 4 9 8.0F
C19 7 0 1 0F
C20 1 0 291.0F
C21 6 0 1.0F
C22 19 0 16.0F
C23 4 0 13.0F
C24 21 0 13.0F
C25 10 0 29.0F
C26 3 0 16.0F
C27 12 0 1 0F
C28 2 0 1.0F
C29 8 0 14.0F
C30 20 0 23.0F
C31 22 0 146.0F
C32 13 0 4.0F
C33 17 0 34.0F
C34 23 0 11.0F
C35 14 0 3.0F
C36 9 0 359.0F
C37 16 0 6.0F
*** Node Listing for subckt:  cfc
** N0                          ==  IdealGND
** N1                [U=6]     ==  GND'
** N2                [U=2]     ==  Ivb2
** N3                [U=2]     ==  Vneg
** N4                [U=2]     ==  dsc_ref
** N5                [U=2]     ==  prot1_0/N2
** N6                [U=2]     ==  Vin+
```

```
** N7                  [U=2]      ==  prot1_0/Comp
** N8                  [U=2]      ==  dsc_bias
** N9                  [U=5]      ==  Vdd'
** N10                 [U=2]      ==  os_bias
** N11                 [U=2]      ==  prot1_0/Vdd'
** N12                 [U=2]      ==  Ivb1
** N13                 [U=2]      ==  OUT
** N14                 [U=2]      ==  Vthr
** N15                 [U=2]      ==  prot1_0/GND'
** N16                 [U=2]      ==  Ibuff
** N17                 [U=3]      ==  os_out
** N18                 [U=1]      ==  dfrf311_0/25
** N19                 [U=2]      ==  dfrf311_0/Q_b
** N20                 [U=2]      ==  dsc_in
** N21                 [U=2]      ==  dsc_out
** N22                 [U=3]      ==  Iin
** N23                 [U=3]      ==  oa_out
.ENDS

** Subcircuit definition for bias
** Extraction file is /msd23/patterson/blue_spec/strip/bias_prot1 ext
.SUBCKT bias 1 2 3 4 5 6 7 8 9 10
** Instance-id:   dsc_bias2_0
X1 7 10 dsc_bias2
** Instance-id    os_bias_0
X2 9 10 8 os_bias
C1 2 1 HPCAP50 SCALE=1131.65
C1P 1 1 HPCAP50P SCALE=1131.7
* C1=4028.69FF C1P=0.11FF
M11 2 2 1 1 CMOSP W=28.00U L=2.80U GEO=1
M12 6 2 1 1 CMOSP W=28.00U L=2.80U GEO=1
M13 5 2 1 1 CMOSP W=3.85U L=2.80U GEO=1
M14 3 2 1 1 CMOSP W=3.85U L=2.80U GEO=1
M15 4 2 1 1 CMOSP W=14.00U L=2.80U GEO=1
C2 2 1 3.0F
C3 1 10 1.0F
C4 7 10 3.0F
C5 2 0 79.0F
C6 6 0 9 0F
C7 1 0 190.0F
C8 9 0 2.0F
C9 4 0 6.0F
C10 5 0 4.0F
C11 7 0 4.0F
C12 10 0 131.0F
C13 8 0 32.0F
C14 3 0 4.0F
*** Node Listing for subckt:  ~/blue_spec/strip/bias_prot1
** N0                         ==  IdealGND
** N1                  [U=13]     ==  Vdd_analog
** N2                  [U=8]      ==  Ibias_amp
** N3                  [U=2]      ==  Ibuff
** N4                  [U=2]      ==  Ivb1
** N5                  [U=2]      ==  Ivb2
```

```
** N6                    [U=2]      ==  amp_bias
** N7                    [U=2]      ==  dsc_bias
** N8                    [U=2]      ==  Vdd'
** N9                    [U=2]      ==  os_bias
** N10                   [U=3]      ==  GND'
.ENDS

****** top level cell is /msd23/patterson/lnafb/prot1_chip.ext

X1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 21 22 23 cfc
X2 9 24 16 12 2 5 8 9 10 1 bias

R1 1 15 0.001
R2 9 11 0.001
Ramp 24 0 80k
Rdsc 8 9 100k
Ros 10 0 10MEG
Vgnd 1 0 0
Vdd 9 0 3.3
Vneg 3 0 -0.3
Vdsc_ref 4 0 1.65
Vbaseline 6 0 0
Vthr 14 0 1
Iin 22 0 10pA


.MODEL RHPNWELL50 R RES=821.0
.MODEL RHPPOLYSB50 R RES=90 0
.MODEL CHPPOLY50 C CAP=0.570FF
 MODEL HPCAP50P C CAP=0.000FF
.MODEL HPCAP50 C CAP=3.560FF
*0 errors and 0 warnings found


 include 'n71s13.mod'
.options METHOD=GEAR GMIN=1E-12
.OP
 tran 0.1m 400m
.options post
.end
```

Appendix 3

```
*low-noise folded cascode amplifier
Vdd 13 0 3.3
*Ibias 1 0 40uA
Rbias 1 0 80k

M11 1 1 13 13 CMOSP W=28U L=2.8U
M12 2 1 13 13 CMOSP W=28U L=2.8U
M13 7 1 13 13 CMOSP W=3.85U L=2.8U
M14 14 1 13 13 CMOSP W=3 85U L=2.8U

Vg1 3 0 0 AC=1
Vg2 4 0 0
M1 5 3 2 2 CMOSP W=210U L=7U *(+)
M2 6 4 2 2 CMOSP W=210U L=7U *(-)
R1 5 0 30k
R2 6 0 30k

M3 8 7 5 0 CMOSN W=100.1U L=28U
M4 9 7 6 0 CMOSN W=100.1U L=28U
M5 8 8 13 13 CMOSP W=28U L=28U
M6 9 8 13 13 CMOSP W=28U L=28U

M7 7 7 11 0 CMOSN  W=25.55U L=7U
M15 11 1 13 13 CMOSP W=14U L=2.8U
R3 11 0 30k

Vneg 15 0 -0 3
M8 13 9 12 0 CMOSN W=7U L=2.8U
M9 12 14 15 0 CMOSN W=7U L=2.8U
M10 14 14 15 0 CMOSN W=7U L=2.8U


*Vsw 100 0 PULSE(0 3 0 10n 10n 100m 200m)
*Msw 12 100 4 0 CMOSN W=14U L=0.7U
*Cint 12 4 0 545pF
Cdet 4 0 3pF
*Idet 4 0 10pA

.include 'n71s13.mod'
 options METHOD=GEAR GMIN=1E-16
.OP
RComp 9 10 8k
Ccomp 10 0 14pF
.noise v(12) Vg1 1
.print noise
.AC DEC 1 1Hz 1Hz
.plot AC VM(12) VP(12)
* tran 0.1m 400m
 pz v(12) Vg1 1
```

```
.options post
.end
```

Appendix 4

**** mosfets

subckt												
element	0 m11		0 m12		0 m13		0 m14		0 m1		0 m2	
model	0 cmosp		0 cmosp		0 cmosp		0 cmosp		0 cmosp		0 cmosp	
id	-40	0000u	-40	3766u	-5	0119u	-5	0612u	-8	6039u	-31	7727u
ibs	0		0		0		0		0		0	
ibd	13	8906f	22	3710f	14	6971f	28	5196f	4	0486f	1	0959f
vgs	-1	3891	-1	3891	-1	3891	-1	3891	-1	0629	-1	2118
vds	-1	3891	-2	2371	-1	4697	-2	8520	-404	8577m	-109	5870m
vbs	0		0		0		0		0		0	
vth	-980	2540m	-980	1391m	-977	6065m	-977	9727m	-986	7765m	-986	7765m
vdsat	-375	2007m	-375	4753m	-376	2796m	-376	1953m	-70	0920m	-207	1206m
beta	501	7982u	505	9779u	62	3120u	62	9784u	1	5441m	1	4993m
gam eff	320	2203m	320	2203m	331	3682m	331	3682m	323	3651m	323	3651m
gm	179	8365u	181	6319u	22	4656u	22	7323u	113	.8312u	158	9472u
gds	528	8499n	359	0871n	33	9765n	34	3641n	885	5635p	161	3006u
gmb	38	2112u	38	4646u	4	9080u	4	9800u	24	7557u	35	5556u
cdtot	12	6892f	12	6892f	1	5727f	1	5727f	96	4660f	3	.4302p
cgtot	207	2705f	207	2705f	26	6810f	26	6810f	3	6539p	5	2248p
cstot	212	5159f	212	5159f	26	4874f	26	4874f	3	8848p	4	2330p
cbtot	37	9360f	37	9360f	5	8616f	5	8616f	731	0294f	750	0391f
cgs	182	6586f	182	6586f	22	.6188f	22	6188f	3	3122p	3	0623p
cgd	12	6892f	12	6892f	1	5727f	1	5727f	96	4660f	2	1431p

subckt												
element	0 m3		0 m4		0 m5		0 m6		0 m7		0 m15	
model	0 cmosn		0 cmosn		0 cmosp		0 cmosp		0 cmosn		0 cmosp	
id	13	3309u	4	4244n	-13	3309u	-4	4300n	5	0119u	-19	9267u
ibs	-6	5804f	-9	5331f	0		0		-7	4816f	0	
ibd	-15	0199f	-32	9989f	17	9801f	1	074e-18	-18	3029f	25	5184f
vgs	1	1722	876	9784m	-1	7980	-1	7980	1	0821	-1	3891
vds	843	9468m	2	3466	-1	7980	-107	4279u	1	0821	-2	5518
vbs	-658	0441m	-953	3147m	0		0		-748	1578m	0	
vth	959	3689m	1	0397	-989	0611m	-989	0611m	974	2927m	-979	9850m
vdsat	175	3782m	0		-744	7905m	-744	6696m	89	0160m	-375	4778m
beta	614	7099u	610	3916u	43	.7614u	43	.7609u	651	5757u	249	6011u
gam eff	747	9411m	743	9657m	326	8674m	326	8674m	743	1899m	321	8479m
gm	105	5377u	171	7980n	30	3743u	4	0646n	58	1343u	89	6708u
gds	486	6326n	0		2	5640n	41	2225u	206	5263n	119	5253n
gmb	29	8735u	44	2370n	6	9368u	1	0809n	15	7053u	19	0485u
cdtot	44	2177f	44	2177f	12	6892f	2	2601p	11	1470f	6	2449f
cgtot	7	2484p	2	4464p	1	9494p	2	7964p	357	7584f	102	5810f
cstot	8	6565p	44	.2177f	2	1230p	2	3445p	344	7231f	104	6733f
cbtot	2	9854p	2	3579p	384	3633f	417	4436f	170	9577f	19	3423f
cgs	6	3030p	44	2177f	1	8229p	1	3925p	254	9769f	89	8819f
cgd	44	2177f	44	2177f	12	6892f	1	3924p	11	1470f	6	2449f

subckt						
element	0 m8		0 m9		0 m10	
model	0 cmosn		0 cmosn		0 cmosn	
id	5	5179u	5	5179u	5	0612u
ibs	-19	3597f	1	1781n	1	1781n
ibd	-33	0000f	-19	3597f	-4	.4804f
vgs	1	3639	748	0374m	748	0374m
vds	1	3640	2	2360	748	0374m

element	0 msw
model	0 cmosn
id	4 4887p
ibs	3 2776p
ibd	-19 3597f
vgs	148 8925m
vds	2 0849

vbs	-1	9360	300	0000m	300	0000m	148	8925m
vth	1	2128	594	3558m	599	0202m	539	0418m
vdsat	127	7938m	118	8318m	115	2867m	0	
beta	438	0392u	463	1971u	439.	0068u	4	4176m
gam eff	716	0602m	765	4025m	765	4025m	730	1896m
gm	55	0264u	54	0904u	49	8420u	174	7116p
gds	517	9387n	145	4314n	455	4748n	2	7572p
gmb	10	1770u	25	1843u	23	3154u	59	2410p
cdtot	2	9181f	2	9181f	2	9181f	6	0233f
cgtot	19	0128f	51	7118f	51	7118f	22	8856f
cstot	2	9181f	62	7404f	62	7404f	6	0233f
cbtot	13	1766f	30	9194f	30	9194f	10	8389f
cgs	2	9181f	38	6135f	38	6135f	6	0233f
cgd	2	9181f	2	9181f	2	9181f	6	0233f

Vita

Gregory W Patterson was born in Knoxville, Tennessee on January 22, 1974 He graduated as class valedictorian from Central High School in Knoxville, Tennessee in May of 1992 In August of 1992, he enrolled at the University of Tennessee in Knoxville While an undergraduate, Gregory worked at the Electric Power Board of Chattanooga as part of the Cooperative Engineering Program During his undergraduate years, he was also a member of the UT Honors Program, Tau Beta Pi, Eta Kappa Nu, and IEEE He graduated Magna Cum Laude with a Bachelor of Science Degree in Electrical Engineering in December of 1997 He began his graduate studies at UT in January of 1998 He was accepted into the UT/ORNL Joint Program in Mixed Signal VLSI and Monolithic Sensors as a graduate research assistant His thesis research was conducted at the Oak Ridge National Laboratory in Oak Ridge, Tennessee as part of this program Gregory worked as an engineering intern for IBM in Research Triangle Park, North Carolina in the summer of 1999 In February of 2000, he began work as a Mixed-Signal IC Design Engineer for Analog Devices in Greensboro, North Carolina He finally graduated with a Master of Science Degree in Electrical Engineering in the summer of 2000