INTEGRATED FEED FORWARD SYSTEM FOR CHEMICAL MECHANICAL POLISHING OXIDE REMOVAL PROCESS AUTOMATION TO IMPROVE PRODUCTIVITY

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DOCTOR OF ENGINEERING

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Faculty of Manufacturing Engineering

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A thesis submitted
in partial fulfillment of the requirements for the degree of
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DECLARATION

I declare that this Choose an item. entitled "INTEGRATED FEED FORWARD SYSTEM FOR CHEMICAL MECHANICAL POLISHING OXIDE REMOVAL PROCESS AUTOMATION TO IMPROVE PRODUCTIVITY is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : 

Name : Samad bin Ramlan

Date : 21 September 2022

APPROVAL

I hereby declare that I have checked this thesis and in my opinion, this thesis is adequate in terms of scope and quality for the award of the degree of Doctor of Engineering.

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DEDICATIONS

All praises belongs to ALLAH.

To my beloved wife and children

ABSTRACT

Chemical Mechanical Planarization (CMP) is one of the main processes in semiconductor wafer fabrication. It is the only process that has contact physically with the wafer, where a pad is placed directly onto the wafer and polished in a circular motion at a particular speed to planarize the wafer surface. For a typical CMOS devices, the downstream process for CMP is the film depositions process and the upstream is the lithography process in which both requires high precision machine capabilities. The process is repeated 10 to 15 times with 300 to 1000 process steps of a wafers cycle dependings on the Integrated Circuit device complexities. Due to the acceptance process tolerance which is measured at a nanometer level and with very tight process controls, excessive polishing on the oxide layer cannot be reworked. Therefore, there is a need to control and monitor closely for each recipe used to process the wafer. Additionally, SilTerra wafer fabrication facility is loaded with more than 200 devices that require to process 5000 to 6000 wafers daily. These devices require variations of processing sequences as well as different settings to be manually conducted. Subsequently, these devices eventually contribute to longer setup times, and commonly lead to human mistakes and equipment interruption of up to about 3000 events a year. That could lead to the need for further inspections or corrections of more than 60,000 wafers. The CMP process for this study is on oxide process. In order to achieve the consistency of an ideal process scenario which is to polish at the appropriate targeted removal rate, an integrated feed forward system is proposed to collect, integrate the information and automate the decision making process. This system is proposed to bridge the gaps particularly for process qualifications and the targeting procedures. Failure Mode and Effect Analysis (FMEA) method is applied to breakdown the process of obtaining the data, computing the data to as the input to the required parameter and applying the parameter to polish the wafers. From FMEA, it is then translated to feed forward system to collect and to integrate between process qualification data on non-production wafer until to apply targeting procedures on production wafers. Supporting functions are developed based on the SECS/GEM equipment interface protocol by Semiconductor Equipment Materials International (SEMI). Based on the observations and data collected, it is found that the system is successful in reducing the cycle time for about 17% from an average of 6 hours to 5 hours as well as reducing the wafers scrap rate from an average of 17 wafers per year to zero scrapped.

ABSTRAK

SISTEM SUAPAN HADAPAN BERSEPADU BAGI PROSES PENGAUTOMATAN PENYINGKIRAN OKSIDA PENGGILAP MEKANIK KIMIA UNTUK MENINGKATKAN PRODUKTIVITI

Penggilap Mekanik Kimia (CMP) adalah merupakan salah satu proses utama dalam fabrikasi wafer semikonduktor. Proses ini adalah satu-satunya proses di mana adanya sentuhan fizikal dengan wafer. Pad diletakkan secara terus ke atas wafer dan penggilapan berlaku dengan gerakan membulat pada kelajuan yang tertentu. Untuk peranti Semikonduktor Pelengkap Logam Oksida (CMOS) kebiasaannya proses hiliran CMP ialah pengendapan filem dan proses huluan ialah litografi yang mana kedua-duanya menggunakan mesin-mesin yang tinggi kemampuan kepersisan. Proses ini diulangi untuk 10 hingga 15 kali dengan 300 hingga 1000 langkah di dalam kitaran wafer bergantung kepada kekompleksan litar bersepadu itu. Oleh kerana tolerans proses penerimaan diukur dalam had terima nanometer dan kawalan proses yang amat ketat, penggilapan yang berlebihan pada lapisan oksida akan menyebabkan wafer tidak dapat dikerjakan semula. Oleh itu, kawalan serta pemantauan ketat menjadi keperluan setiap resipi yang digunakan untuk memproses wafer diperlukan. Tambahan pula, kemudahan fabrikasi wafer di Silterra mempunyai lebih dari 200 peranti yang perlu memproses 5000 hingga 6000 wafer setiap hari. Peranti-peranti ini memerlukan penyediaan pelbagai jujukan proses dan pelarasan secara insani. Kemudiannya, ini menyumbang kepada masa penyediaan yang panjang dan kebiasaannya terdedah kepada kesilapan manusia dan sampukan pada kelengkapan sehingga 3000 peristiwa setahun. Ini juga menyumbang kepada lebih 60000 wafer yang perlu diperiksa atau diperbetulkan. Proses yang dipilih untuk kajian adalah proses oksida. Lantaran itu, untuk mencapai konsistensi dalam proses penggilapan yang unggul, sistem suap-depan bersepadu dicadangkan untuk mengumpul, menyatukan maklumat dan melaksanakan proses membuat keputusan secara automatik. Sistem ini dibangunkan untuk mengisi sela terutamanya dalam proses kelayakan dan tatacara pensasaran. FMEA (Analisis Ragam Kegagalan dan Kesan) kaedah dipilih untuk penghuraian proses mendapatkan data, pengiraan data untuk parameter yang diperlukan dan seterusnya menggunakan parameter untuk menggilap wafer. Dari analisis tadi, ia diterjemahkan kepada sistem suapan ke hadapan untuk mengumpul dan menyepadukan di antara proses kelayakan data pada wafer bukan-pengeluaran sehingga diaplikasikan pada tatacara penyasaran pada wafer pengeluaran. Rangkap sokongan dibangunkan menggunakan perisian dagangan berdasarkan pada protokol antaramuka kelengkapan SECS/GEM yang dikawal selia oleh Badan Antarabangsa Bahan Kelengkapan Semikonduktor (SEMI). Berdasarkan kepada pemerhatian dan data yang dikumpul, sistem ini telah berjaya mengurangkan masa kitaran di sekitar 17% dari purata 6 jam kepada 5 jam dan menurunkan kadar wafer yang rosak dari purata 17 wafer setahun kepada sifar wafer rosak.

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LIST OF SYMBOLS AND ABBREVIATIONS

SMSB	Silterra Malaysia Sdn. Bhd.
SIA	Semiconductor Industries Association
BKM	Best Known Method
IC	Integrated Circuit
ASICs	Application-Specific Integrated Circuits
CMP	Chemical-Mechanical Polishing/Planarization
SMIF	Standard Mechanical Interface
FMEA	Failure Mode and Effect Analysis
PFMEA	Process Failure Mode and Effect Analysis
RPN	Risk Priority Number
CIM	Computer Integrated Manufacturing
MES	Manufacturing Execution System
SAH	Send Ahead
SPC	Statistical Process Control
BR	Business Rules
MCS	Material Control System
FFS	Feed Forward System
SFC	Shop Floor Control
API	Application Programmer's Interface
GUI	Graphical User Interface
FW	FACTORYworks
DTPF	Distributed Transaction Processing Framework
SEMI	Semiconductor Equipment and Materials International
SECS	Semiconductor Equipment Communication Standard
GEM	Generic Model for Communications and Control of Manufacturing Equipment