Missouri University of Science and Technology
Scholars' Mine

Electrical and Computer Engineering Faculty Research & Creative Works

Electrical and Computer Engineering

01 Apr 2018

Equivalent Capacitance Approach To Calculate Effective Roughness Dielectric Parameters For Copper Foils On Printed Circuit Boards

Marina Y. Koledintseva
Missouri University of Science and Technology, marinak@mst.edu

Tracey Vincent

Follow this and additional works at: https://scholarsmine.mst.edu/ele_comeng_facwork

Part of the Electrical and Computer Engineering Commons

Recommended Citation

M. Y. Koledintseva and T. Vincent, "Equivalent Capacitance Approach To Calculate Effective Roughness Dielectric Parameters For Copper Foils On Printed Circuit Boards," *Journal of Microelectronics and Electronic Packaging*, vol. 15, no. 2, pp. 49 - 62, International Microelectronics Assembly and Packaging Society, Apr 2018.
The definitive version is available at https://doi.org/10.4071/IMAPS.654479

This Article - Conference proceedings is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Electrical and Computer Engineering Faculty Research & Creative Works by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

Journal of Microelectronics and Electronic Packaging (2018) **15**, 49-62
Copyright © International Microelectronics Assembly and Packaging Society
ISSN: 1551-4897

Equivalent Capacitance Approach to Calculate Effective Roughness Dielectric Parameters for Copper Foils on Printed Circuit Boards

Marina Y. Koledintseva[1,]* and Tracey Vincent[2]

***Abstract*—Effective roughness dielectric (ERD) is a homogeneous lossy dielectric layer of certain thickness with effective (averaged) dielectric parameters. The ERD layer is used to model copper foil roughness in printed circuit board interconnects by being placed on a smooth conductor surface to substitute an inhomogeneous transition layer between a conductor and laminate substrate dielectric. This work derives the ERD parameters based on the understanding that there is a gradual variation of concentration of metallic inclusions in the transition layer between the dielectric and foil. The gradual variation can be structured as thin layers that are obtained using the equivalent capacitance approach. The concentration profile is extracted from scanning electron microscopy or high-resolution optical microscopy. As the concentration of metallic particles increases along the axis normal to the laminate dielectric and foil boundary, two regions can be discerned: an insulating (prepercolation) region and a conducting (percolation) region. The rates of increase in effective loss (or corresponding conductivity) in these two regions differ significantly. The proposed model of equivalent capacitance with gradient dielectric is applied to a number of different types of copper foils. The frequency-dependent dielectric parameters of the homogenized ERD are calculated from the equivalent capacitance. The results are validated using 3D numerical electromagnetic simulations. There are two types of numerical models: with homogeneous ERD parameters and layered. Both models show excellent agreement with measurements.**

***Keywords*—printed circuit board, signal integrity, stripline, copper foil, roughness, electric percolation, numerical electromagnetic simulations, S-parameters, dielectric constant, dissipation factor, complex permittivity, loss constant, phase constant**

INTRODUCTION

Printed circuit boards (PCBs) used in high-speed digital design are known to have a substantial level of copper foil roughness which compromises signal integrity (SI) and may also cause electromagnetic compatibility problems. Therefore, knowledge of the correct parameters of laminate PCB dielectrics refined from any copper foil roughness impact and the proper foil roughness characterization are important constituents of modeling high-speed digital electronics designs, e.g., Refs. [1-3] and references therein.

There are numerous models to characterize conductor surface roughness. All these models could be systematized in a few groups. The first group is based on introduction of roughness correction coefficients for attenuation in planar transmission lines. A good overview of models with roughness correction coefficients is given in Shlepnev [4]. This group includes such models as Morgan's [5]; Hammerstad and Bekkadal [6], Hammerstad and Jensen [7]; Groiss's model [8]; Bushminskiy's model [4, 9]; Huray's "snowball" model [10, 11]; Hall-Pytel's hemisphere model [12]; stochastic models for power spectral density of rough surfaces such as Sanderson's [13], Braunisch-Tsang's [14-16], Chen and Wong's [17]; and approximation of roughness by periodic functions and using small perturbation technique as in Refs. [13, 18-21]. The second group of models is based on introducing equivalent boundary conditions, or surface impedance, due to roughness on a smooth conducting surface [13, 19-22]. The direct or hybrid electromagnetic modeling of surface roughness by various numerical simulation techniques and tools comprises the third group of surface roughness models. Some numerical models can be found in Refs. [23-27] and references therein. The fourth group relates to experimental separation of conductor losses into smooth part associated with skin depth only and roughness part that could be associated with both inductive (similar to skin depth, $\sim\sqrt{\omega}$) and capacitive (as in a lossy dielectric, with $\sim\omega$ and $\sim\omega^2$ frequency behavior) effects on loss and phase constant in a PCB transmission line [28-31].

Note that the capacitive effect of roughness on phase constant was first mentioned in Ref. [23], although some authors consider only inductive effects associated with roughness, e.g., Refs. [32-34]. In Ref. [35], the gradient model for effective conductivity and permeability associated with conductor roughness is considered, corresponding surface impedance is calculated, and it affects both loss and phase delay on the line. Note that recently, indeed, the excess of both capacitance and inductance due to conductor surface roughness has been recommended to consider in the roughness models [4, 36]. In this work, we stand on the position of mainly capacitive effect of a PCB foil roughness, although roughness also contributes to skin depth through a positive or even negative $\sim\sqrt{\omega}$ term, increasing or decreasing

The manuscript was received on March 28, 2018; revision received on May 8, 2018; accepted on May 9, 2018

This paper and Presentation "Equivalent capacitance approach to obtain effective roughness dielectric parameters for copper foils" was first presented at the 2018 IPC Apex Expo Technical Conference and published in the 2018 Technical Conference Proceedings.

[1]Oracle, Santa Clara, California
[2]CST of America, Framingham, Massachusetts
*Corresponding author; email: koledintseva@gmail.com

doi:10.4071/imaps.654479
1551-4897 © 2018 International Microelectronics Assembly and Packaging Society

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

loss due to skin depth in a smooth conductor. A negative $\sim\sqrt{\omega}$ term resulting in some reduction in skin depth loss can be observed because of significantly rough surfaces which are as if pushing electromagnetic field out of the conductor, and this effect is shown in Refs. [13, 29].

The effective roughness dielectric (ERD) concept, which is a consequence of capacitive effect of conductor surface roughness on both loss and phase constants of propagating wave in a PCB transmission line, was introduced in Refs. [37-40]. ERD is a homogeneous lossy dielectric layer of certain thickness T_r with effective (averaged) dielectric constant DK_r and dissipation factor DF_r. ERD is placed on a smooth conductor surface to substitute an inhomogeneous transition layer between a conductor and laminate substrate dielectric. Although the concept is simple, it is physically illuminating, meaningful, and powerful. It has been successfully applied to model conductor (copper foil) roughness in PCBs for SI and electromagnetic interference purposes when designing high-speed digital electronics devices [41, 42]. The ERD model has been implemented and tested in a number of numerical electromagnetic modeling tools, e.g., Refs. [43-46].

In our previous publications [39, 47, 48], the ERD "design curves," determining the ranges of the DK_r and DF_r parameters for different types of PCB copper foils were developed. The methodology of generating these "design curves" is based on the following procedures:

- stripline S-parameter sweep (S3) technique to measure S-parameters of single-ended comparatively long (~40 cm, or 16 inches) striplines with TRL calibration to remove connector effects [21, 49];
- scanning electron microscopy (SEM) or high-resolution optical microscopy of cross sections of PCB samples with signal traces and the proper quantification of surface roughness profile parameters [50-52];
- differential extrapolation roughness measurement technique [28-31]; and
- two-dimensional finite element method and/or three-dimensional finite integral technique (3D-FIT) numerical modeling that allow for accurately fitting the measured S-parameters of the striplines and extract the data for DK_r and DF_r of the roughness layers [37, 39, 47, 48]. This fitting may include an optimization procedure, e.g., a genetic algorithm to minimize the discrepancy between the modeled and measured S-parameters.

The "design curves" in the abovementioned papers were generated using SEM and/or optical microscopy to quantify foil roughness. Any designer can use these "design curves" and does not necessarily need to cut a PCB and prepare samples of the line cross sections for microscopic inspection. It is sufficient to know which type of foil is used in the PCB under test—this may be standard (STD) foil, very low profile (VLP) foil, reverse-treated foil (RTF), or hypervery low profile (HVLP)/supervery low profile (SVLP) foil. Each foil type (group) has some ranges of DK_r, DF_r, and roughness thickness T_r values, and a designer may take average values of DK_r, DF_r, and T_r within these ranges for the reasonable estimation of the data which then could be used in modeling of the PCB designs. In our articles [29, 30], different foils were subdivided in a few groups depending on the average peak-to-valley roughness amplitudes: for STD foils, $R_z \sim$ 5-15 μm, but in some roughest cases may reach 20 μm; for VLP and RTF foils, the typical values of $R_z \sim$ 3-5 μm; and for HVLP/SVLP foils, R_z may be as low as 1-3 μm. The present-day PCB foil technology even reduces roughness on the smoothest foils, although they remain comparatively expensive. Note that these R_z values are traditionally measured by a mechanical or optical profiler on a standalone foil, and therefore differ from the values of average peak-to-valley amplitudes measured using pictures of PCB cross sections.

Although the "design curves" were developed using fitting between the experimental data and modeling results, it is always desirable to have a simple and physically meaningful analytical model. In this work, the DK_r and DF_r parameters are derived based on the understanding that the transition layer between the dielectric and foil contains gradual variation of concentration of metallic inclusions: from zero concentration in laminate dielectric through some percolation limit to 100% at the smooth copper foil level. The equivalent material parameters of this layered structure can be obtained using equivalent capacitance approach. In the equivalent capacitor, the dielectric properties vary according to the concentration profile of metallic particles in the roughness layer. The concentration profile can be obtained from SEM or high-resolution optical microscopy. As concentration of metallic particles increases along the axis normal to the laminate dielectric and foil boundary, two regions can be determined: insulating (prepercolation) and conducting (percolation). Rates of increase in effective loss (or effective conductivity) in these two regions significantly differ. The proposed model of equivalent capacitance with gradient dielectric has been applied to STD, VLP, and HVLP foils, and the results are validated using 3D full-wave numerical electromagnetic simulations.

Description of Equivalent Capacitance Model

A roughness profile on a PCB conductor surface can be tested using optical or SEM microscopy, or a surface profiler. The average contents (volume concentration) of metallic particles in the roughness layer vary as a function of the coordinate z normal to the surface. It can be approximated by an exponential function:

$$v_{\mathrm{incl}}(z) = a \times \exp(K_1 z), \tag{1}$$

where a and K_1 are the fitting parameters.

Two separate regions of ERD can be considered:

Region I: $0 < z < T_p$, where the concentration of metallic inclusions is below the percolation threshold, i.e., where the mixture remains in the dielectric phase; this is the region adjacent to the dielectric matrix of the PCB. Herein, T_p is the distance within the layer at which percolation is reached.

Region II: $T_p < z < T$, where the concentration of metallic inclusions is higher than the percolation threshold; this is the region adjacent to the smooth foil level and is conducting.

The percolation threshold is understood as the volume fraction of metallic inclusions, at which they start forming a conducting path, or net. As one cuts roughness in slices starting from peaks, the metallic regions in these slices first will be separated by significant amount of surrounding dielectric; as

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

cutting slices further, more metallic inclusions will be in the deeper slices, and at some point, the concentration will be such that percolation starts.

Herein, T is the entire thickness of ERD layer. It includes

$$T = T_p + \Delta T, \tag{2}$$

where ΔT is the thickness of the region above the percolation.

The concentration v_p, at which percolation will occur for the metallic particles in the roughness dielectric layer, can be obtained empirically, i.e., estimated from the microscopy pictures, or from the profiler data. By solving the equation

$$v_p = a \times \exp(K_1 T_p) \tag{3}$$

with respect to T_p, one can get the height of the dielectric phase of ERD.

First, let us consider the region $0 < z < T_p$. This is the dielectric layer with relative permittivity varying according to the profile function (1) from the matrix dielectric properties ε_m (at $z = 0$) to the final prepercolation value ε_p (at $z = T_p$). Because dielectric function varies with z as

$$\varepsilon(z) = \varepsilon_m v_{incl}(z), \tag{4}$$

the effective permittivity of such a layer can be calculated through the equivalent partial-layered capacitor consisting of series connection of sublayer capacitors. The capacitance of the resultant capacitor with variable properties of the dielectric is

$$C = C_0 d / \int_0^d dz/(1 + \varepsilon(z)), \tag{5}$$

where C_0 is the capacitance of the corresponding air-filled rectangular parallel-plate capacitor of thickness d. Herein, $d = T_p$.

The effective dielectric properties of such dielectric layer can be easily derived from (5) as

$$\varepsilon_d = T_p / \int_0^{T_p} dz/(\varepsilon_m(1 + v_{incl}(z))). \tag{6}$$

This permittivity is complex, and its real and imaginary parts can be separated as

$$\varepsilon_d = \varepsilon'_d - j\varepsilon''_d. \tag{7}$$

If the imaginary part is represented through the equivalent conductivity, the corresponding equivalent conductivity is

$$\sigma_d = -\omega\varepsilon_0\varepsilon''_d. \tag{8}$$

This conductivity will not be high because it is coming from a lossy ERD in the dielectric phase. Its value is on the order of 10^{-2} S, which is similar to a comparatively lossy dielectric.

However, in Region II, the conductivity increases exponentially toward smooth copper level until it reaches the conductivity of the pure copper used on a PCB. Therefore,

$$\sigma_p = \sigma_d \times e^{K_2 T}, \tag{9}$$

where K_2 is the exponent parameter for conductivity after percolation, and it can be solved from the equation, when σ_p reaches the level at the beginning of percolation, e.g., $\sigma_p = 0.01\sigma_{Cu}$. Percolation threshold is assumed to be 25% of volume concentration of metallic inclusions in the epoxy-resin fiber-filled dielectric matrix; this is based on numerous experimental studies of composites containing copper powder inclusions in a polymer base [53]. The conductivity at which percolation starts, i.e., 1% of the conductivity of pure copper, is also an empirical value. Note that in reality, it is difficult to state that particles in this "roughness dielectric" are pure copper because for adhesion purposes, foils are treated chemically. Most likely, there is oxidation on each copper dendrite, and even if particles touch each other, the oxide films may prevent from percolation. Still, ~25% percolation threshold is a reasonable estimate.

As a reminder, T is the entire thickness of the ERD layer.

Then the conductivity profile function with respect to the coordinate z will be

$$\sigma(z) = \sigma_d \times e^{K_2 z}. \tag{10}$$

The dielectric profile function in the second conducting layer will be defined as

$$\varepsilon_p(z) = \varepsilon_d + \frac{\sigma_d}{j\omega\varepsilon_0} \times e^{K_2 z}. \tag{11}$$

The effective permittivity of the two lossy dielectric layers is calculated through the equivalent capacitor containing two capacitors in series. Both capacitors have gradient fillers. The filler of the first layer is in the nonconducting dielectric phase, and the other is close to percolation, i.e., conducting phase.

$$\varepsilon_{eff} = T / \left(\int_0^{T_p} dz/(\varepsilon_m(1 + v_{incl}(z)) + \int_{T_p}^{T} dz/(\varepsilon_p(1 + v_{incl}(z)) \right). \tag{12}$$

From (12), separating real and imaginary parts, the following ERD parameters can be calculated: $DK_r = \varepsilon'_{eff}$ and $DF_r = \tan\delta_{eff} = \varepsilon'_{eff}/\varepsilon'_{eff}$.

Metal Inclusion Profiles in Different Foils

Cross-sectional microscopic (SEM or optical) analysis is used to characterize roughness profile of the foil. For this purpose, typically a signal trace is cut perpendicular to the direction of the electromagnetic wave propagation. The procedure of image processing is described in detail in Refs. [50-52]. An example of a binary (black-and-white) image of the trace cross section of VLP foil on polyphenylene oxide (PPO) blend substrate is shown in Fig. 1. The bottom ("foil" or "matte") side of this foil is rougher than the top ("oxide" or "drum") side.

The surface roughness profile can be extracted and then quantified using digital image processing based on the analysis of pixels. The average peak-to-valley magnitude of the roughness profile corresponding to the bottom of Fig. 1 is shown in Fig. 2.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

Fig. 1. Binary image of the cross section of the signal trace of black oxide VLP foil on PPO blend substrate.

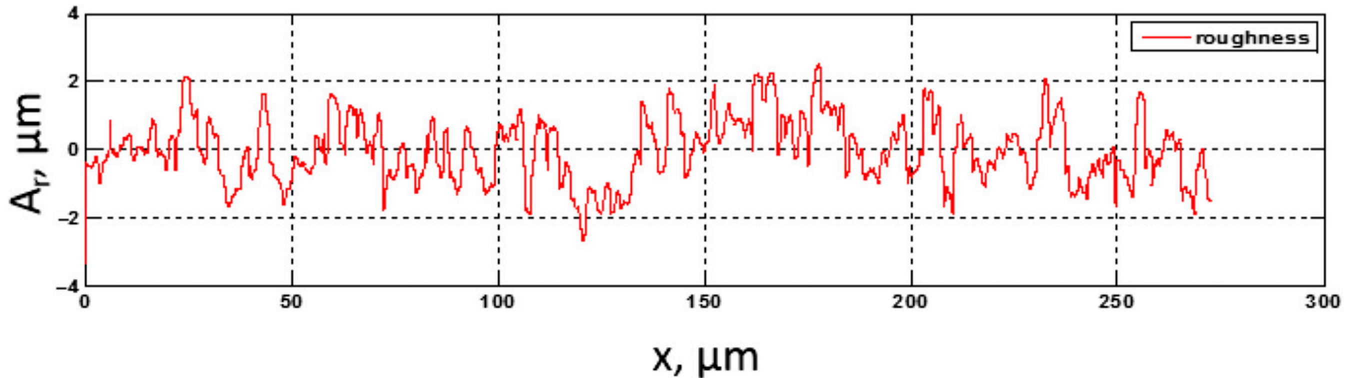

Fig. 2. An example of foil roughness profile extracted from the bottom side of the binary image.

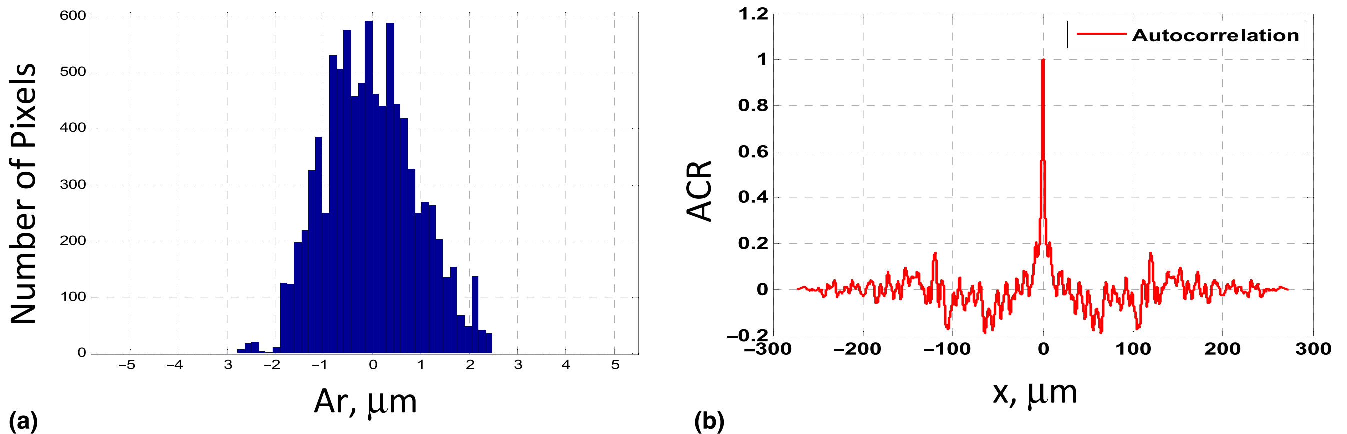

Fig. 3. (a) Histogram of pixels to determine PDF and (b) ACR.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

Foil surface roughness has the stochastic nature; therefore, along with peak-to-valley values, it can be characterized in terms of the probability density function (PDF) and autocorrelation function (ACR). A histogram of pixels for calculating PDF and ACR curves for VLP foil type (the same as is shown in Fig. 2) are presented in Fig. 3. The PDF shows that copper foil surface roughness has normal (Gaussian) distribution, and from ACR, it is clearly seen that the roughness is uncorrelated and does not contain any periodicity.

In many cases (although not always), surface roughness is isotropic, i.e., the PDF is invariant with respect to any direction of the wave propagation. Because the parameters of PDF can be obtained from the profile, the roughness 3D profile can be reconstructed for the future investigation using, e.g., Gaussian filter or any other low-pass filter widely used in digital image processing. The parameters of this filter should be adjusted to get the best correlation with the measured roughness profile [54].

The PDF and ACR of the generated 3D roughness profile shown in Fig. 4 agree well with those shown in Fig. 3. The 3D-generated roughness profiles are useful for roughness quantification, e.g., as in Refs. [29-31], including ERD "design curves" [40, 47] and for metallic concentration variation study needed for equivalent capacitance approach.

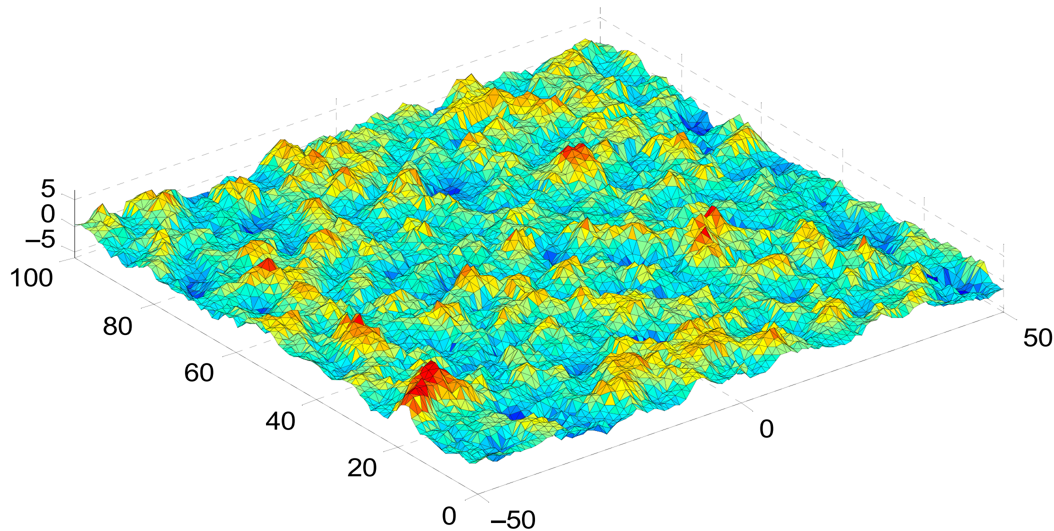

Fig. 4. 3D roughness profile surface generated using PDF and Gaussian filter.

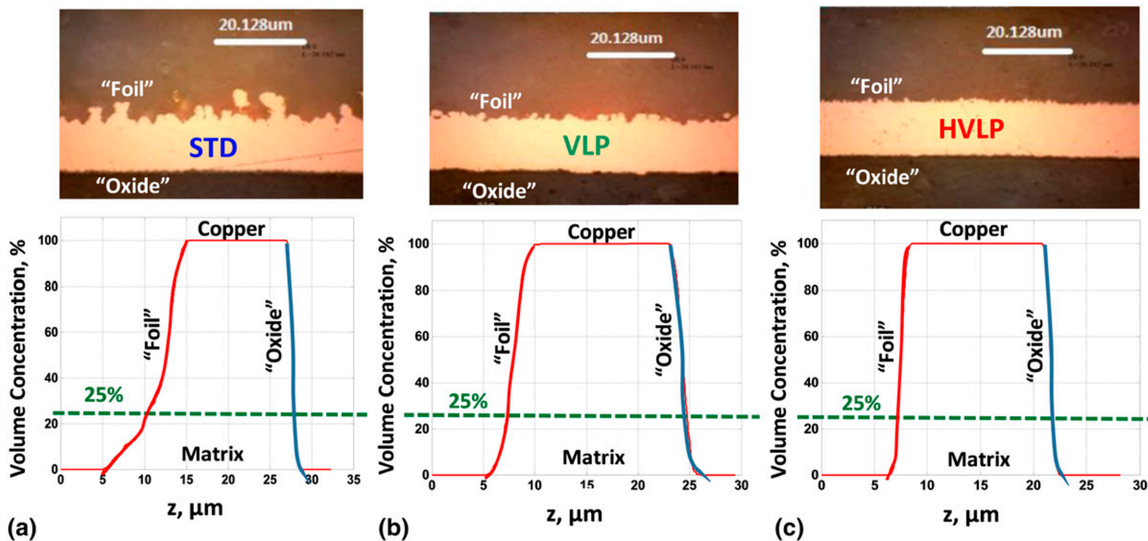

Fig. 5. Volume concentration of metallic inclusions in black oxide (a) STD, (b) VLP, and (c) HVLP foil on PPO blend substrate.

Applying the same image processing technique as for the roughness magnitude extraction, but performing summation for each column of pixels, one can get the volume concentration of metallic inclusions in the transition between pure dielectric to pure metal. Fig. 5 shows the function $v_{\mathrm{incl}}(z)$ for different types of foils. It is seen that 0% concentration corresponds to dielectric matrix, whereas 100% to smooth copper. The transitions are comparatively smooth—the left-hand front corresponds to the "foil" side and the right-hand side to the "oxide" side. The smoother the conductor side, the more abrupt the metallic concentration slope.

The profiles on the "foil" and "oxide" sides can be fitted using exponential or polynomial functions as is shown in Figs. 6-8. For simplicity of calculating integrals analytically in (5), (6), and (12), the exponential approximation ae^{bz} will be further used. Note that the parameter b herein is the same as K_1 in (1).The approximation data for a number of studied samples of black-oxide foils on PPO blend substrates are presented in Table I. The parameter δ_{rms} herein is the root mean square error at the approximation. T_{p} is the height of the prepercolation region from dielectric matrix and T is the total roughness height (note that T is typically close to the R_{z} value measured by a profiler on the corresponding standalone foil but not exactly the same).

Calculation of ERD Parameters Using the Proposed Analytical Model

The proposed equivalent capacitance model was applied to calculate the ERD parameters of the three types of foils as in Table I. Figs. 9-11 show the calculated frequency dependences for $\mathrm{DK_r}$ and $\mathrm{DF_r}$ of the corresponding ERD layers. The thicknesses of the layers are also determined from the metallic concentration profiles. Note that in the previous publications [37, 40, 47, 48], the ERD parameters were independent of frequency. However, the new analytical model shows that there

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

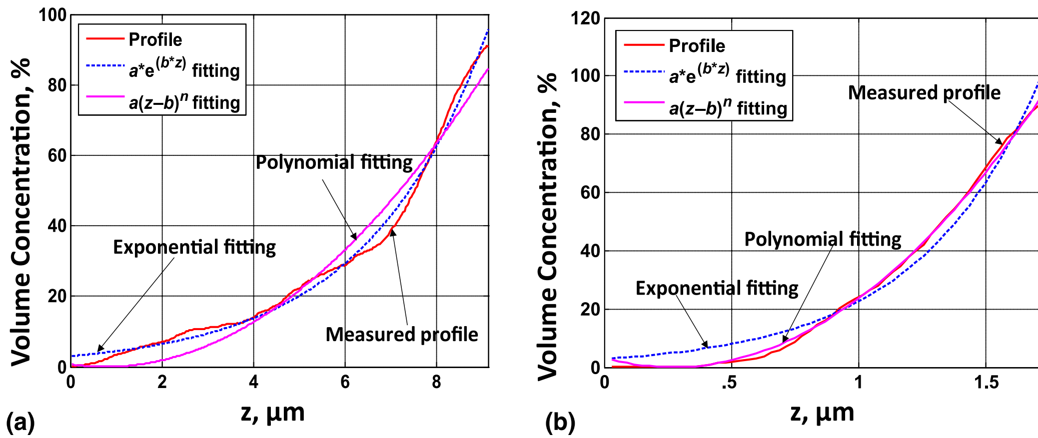

Fig. 6. Approximation of volume concentration of metallic inclusions as a function of distance from the smooth conductor: (a) "foil" side and (b) "oxide" side on STD foil.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

is frequency dependence. The ERD parameters for the STD foil on its "foil" and "oxide" sides differ significantly because the "foil" side is much rougher than the "oxide" side. The corresponding differences for the sides on the VLP and HVLP foils do not differ that much, although they are not equal. Although the extracted ERD parameters for the VLP foil herein are close to those of the HVLP, the thicknesses of the layers to be modeled differ: the HVLP layers are thinner than those of VLP. Note that the calculated ERD results are not the same as reported in Refs. [40, 47] because the test samples studied herein are different. In the present study, the roughness parameters of HVLP and VLP samples are not much different, whereas in Refs. [40, 47], the VLP and HVLP foils are quite distinct.

PCB dielectric matrix complex permittivity ε_m is present in the eqs. (4) and (6) for calculating ERD parameters through the equivalent capacitance approach. Therefore, to extract ERD parameters for the particular foil on a dielectric substrate, one should know the parameters of the PCB dielectric. Dielectric parameters of core and prepreg on a stripline may slightly differ; however, the properties of stripline dielectrics extracted from measurements are typically averaged over the entire stripline space where electromagnetic waves propagate. There are various dielectric spectra measurement techniques, including various traveling-wave, resonator, and free-space methods, to obtain characteristics of stripline dielectrics—an overview is given, e.g., in Refs. [29, 55].

To have causal dielectric responses satisfying Kramers-Krönig relations [56], the extracted complex permittivity may be represented as rational functions with poles of the first order using vector fitting [57, 58] or series of Debye-like terms the parameters of which are obtained using an optimization procedure [59], or as wideband Debye response (also called Djordjevic-Sarkar model [2, 60]). In this particular work, the dielectric parameters of PCB substrate were extracted using S3 technique [21, 49] and then the improved differential extrapolation roughness technique as in [31] that uses extrapolation zero roughness of curve fitting coefficients for $\sqrt{\omega}$, ω, ω^2 terms

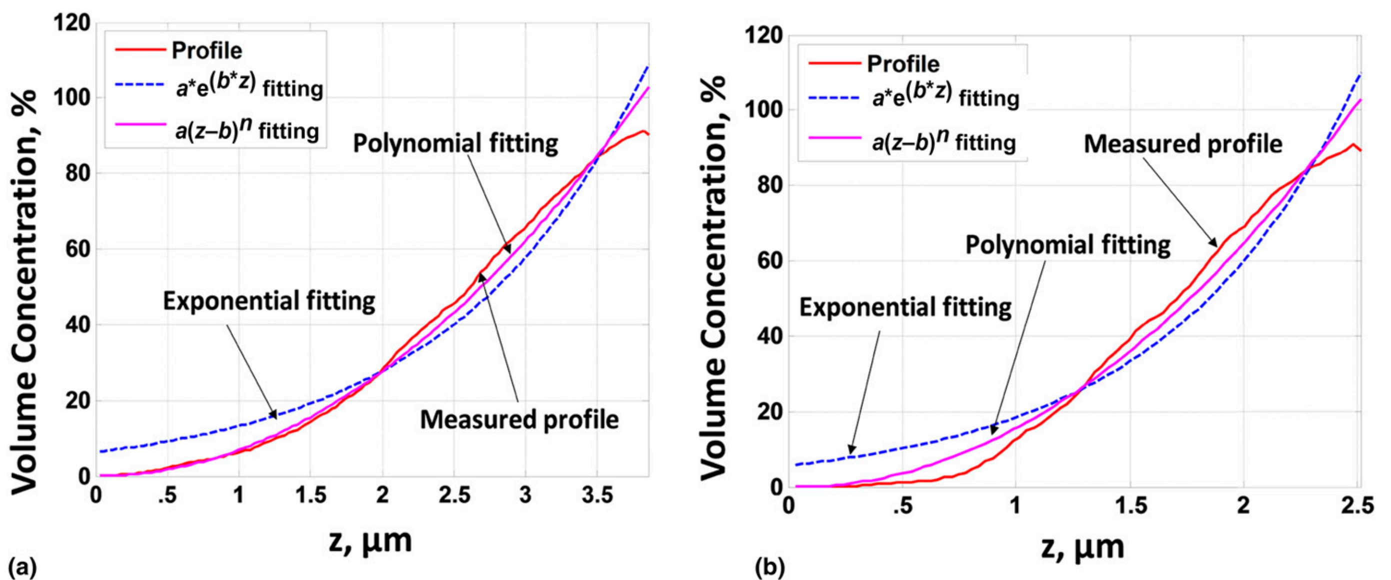

Fig. 7. Approximation of volume concentration of metallic inclusions as a function of distance from the smooth conductor: (a) "foil" side and (b) "oxide" side on VLP foil.

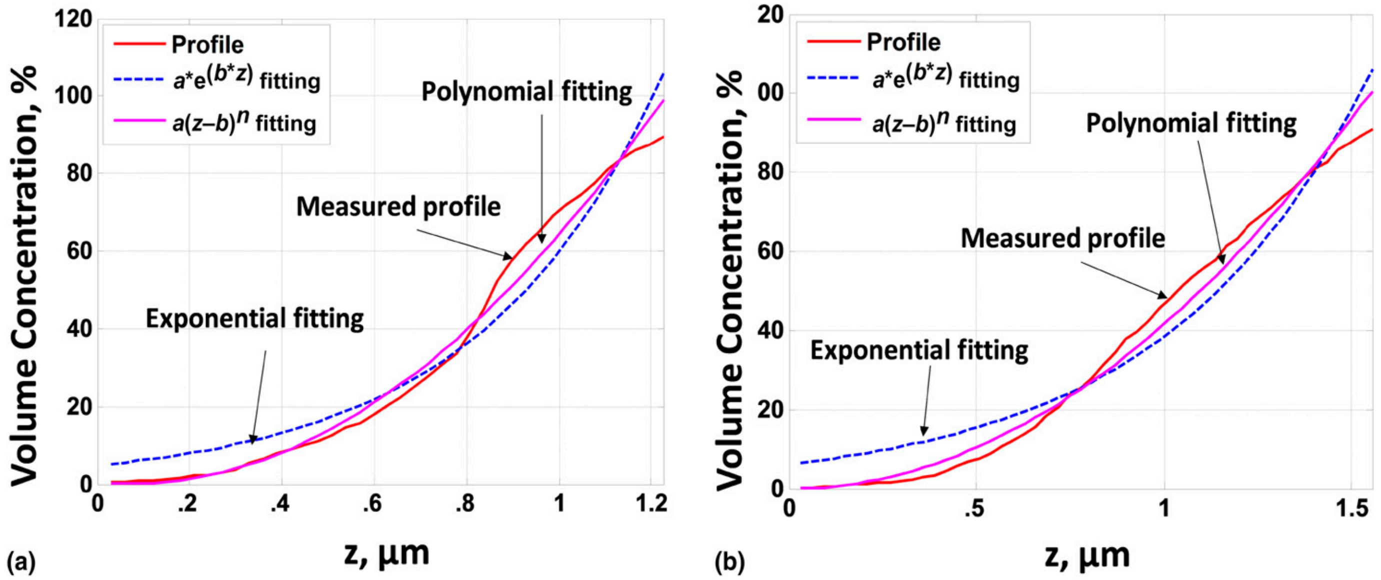

Fig. 8. Approximation of volume concentration of metallic inclusions as a function of distance from the smooth conductor: (a) “foil” side and (b) “oxide” side on HVLP foil.

in attenuation and phase constants as functions of frequency. The resulting extracted DK for the PPO blend matrix keeps almost constant (3.65), slightly reducing in the third decimal digit as frequency increases and DF is linearly increasing with frequency from about .005 at 5 GHz to .0074 at 40 GHz [31].

Note that the proposed equivalent capacitance model is not very sensitive to the accuracy of the dielectric matrix determination. Even if DK and DF vary within $\pm 10\%$, the extracted DK_r and DF_r of ERD remain practically the same (changing by less than 1%). This is because the ERD parameters are mainly determined by the concentration of metallic inclusions in the dielectric matrix, and the volume fraction of these inclusions in the roughness layer is high even in the pre-percolation layer (varying from 0% to 25%).

Measurements of Insertion Loss and Phase Delay

The measured insertion loss $|S_{21}|$, dB, and time delay τ on a transmission line, i.e., a single-ended stripline, increase as conductor roughness magnitude increases, and hence, the values DK_r and DF_r of the corresponding ERD layers increase. This is illustrated by Fig. 12.

The phase delay increases as conductor roughness increases, which is the direct consequence of the capacitive (dielectric) nature of the ERD. Because phase progression in a TEM transmission line of the length l and with the homogeneous dielectric filling $\varepsilon_r$is [61]

$$\varphi = \beta l = 2\pi f l \sqrt{\mu_0 \varepsilon_0}\sqrt{\varepsilon_r}, \quad (13)$$

the corresponding time delay is calculated as

$$\tau = \frac{\partial \varphi}{\partial f} = \frac{2\pi l}{c}\sqrt{\varepsilon_r}. \quad (14)$$

The corresponding magnitude of $|S_{21}|$, determining the insertion loss on the line, is approximately

$$|S_{21}|, \text{dB} = -8.686\alpha l, \quad (15)$$

where the total loss constant α for the TEM mode on the line comprises the conductor and dielectric loss parts [61],

$$\alpha = \alpha_C + \alpha_D, \quad (16)$$

and

$$\alpha_D = \frac{\omega}{c}\tan\delta\sqrt{\varepsilon_r}. \quad (17)$$

Note that herein, ε_r is the dielectric constant (real part of permittivity) of the effective dielectric inside the transmission line, which includes both the substrate dielectric matrix and ERD.

Table I
Exponential Approximation of Profile Functions on “Foil” and “Oxide” Sides of Copper Foils

Foil type/model		$f(z) = ae^{b\cdot z}$ coefficients (with 95% confidence bounds)	T_p (µm)	T (µm)
STD	“Foil” side	a = 3.03 (2.91, 3.15), b = 0.3787 (0.3737, 0.3837), and δ_{rms} = 2.0962	4.99	9.0
	“Oxide” side	a = 2.829 (2.233, 3.425), b = 2.075 (1.937, 2.213), and δ_{rms} = 4.9168	0.93	1.7
VLP	“Foil” side	a = 5.991 (5.253, 6.73), b = 0.7479 (0.7103, 0.7855), and δ_{rms} = 6.1539	1.61	3.8
	“Oxide” side	a = 5.665 (4.518, 6.812), b = 1.18 (1.086, 1.275), and δ_{rms} = 8.0289	1.07	2.6
HVLP	“Foil” side	a = 5.537 (3.922, 7.152), b = 2.182 (1.936, 2.428), and δ_{rms} = 8.4887	0.46	1.3
	“Oxide” side	a = 6.193 (4.762, 7.624), b = 1.827 (1.653, 2.001), and δ_{rms} = 7.3620	0.64	1.6

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

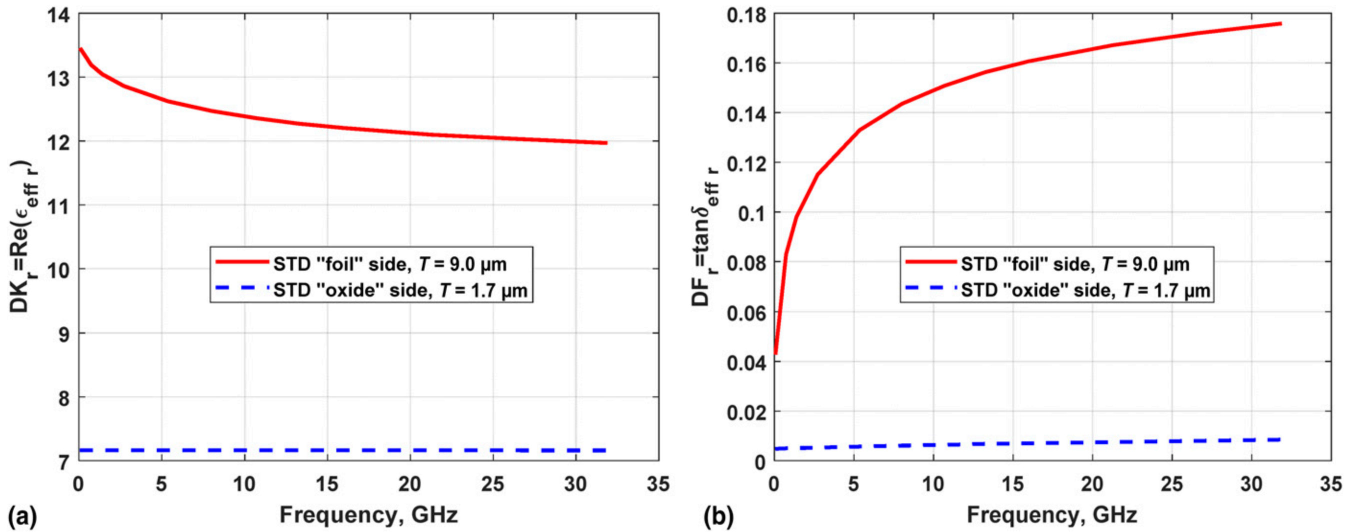

Fig. 9. Effective roughness dielectric parameters as functions of frequency for STD foil: (a) DK_r and (b) DF_r.

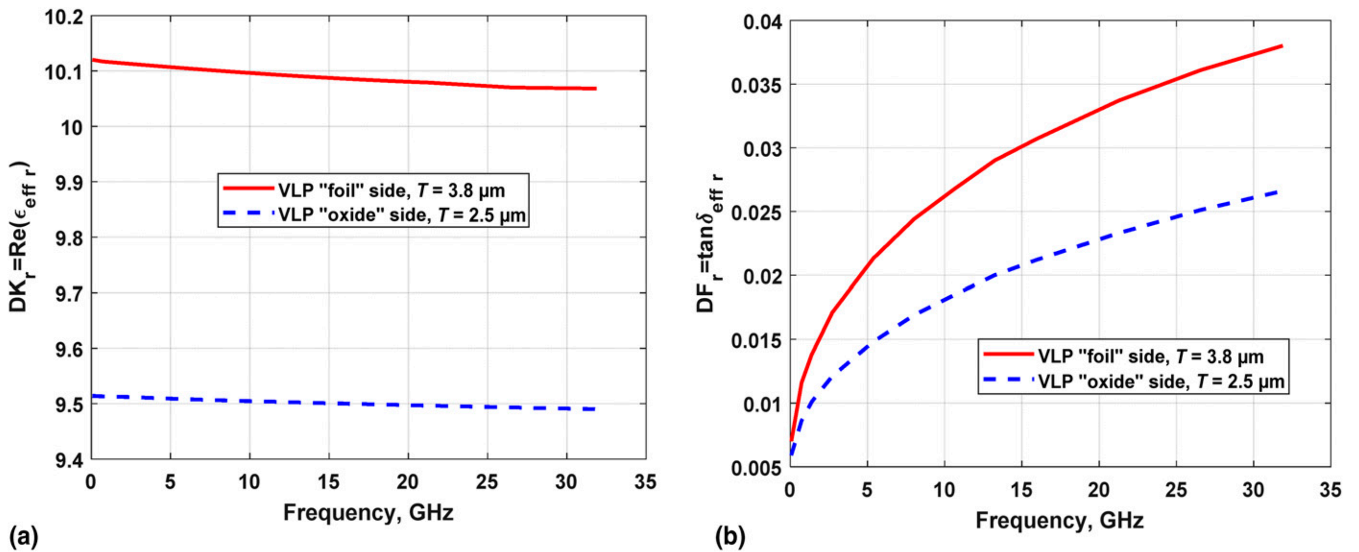

Fig. 10. Effective roughness dielectric parameters as functions of frequency for VLP foil: (a) DK_r and (b) DF_r.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

Model Setup for Numerical Simulations

Similar to the previous studies [40, 47], the stripline simulation numerical electromagnetic model has been created. It includes the dielectric matrix having the dielectric properties as discussed in the previous section and thin layer-like objects representing conductor surface roughness as the ERD: above the trace ("foil" side) and below the trace ("oxide" side). The corresponding ERD layers are also placed on the reference (ground/return) planes. Fig. 13 shows a cross-sectional view of the numerical model setup. The line length of the stripline structure was 391.414 mm (15.4 inches); stripline traces were 17.5-μm thick (0.5-oz copper) and 340-μm (13.5 mil) wide. The impedance of the single-ended line was 50 Ohms. Cross-sectional dimensions for all the three test lines were identical, except for the foil roughness. Because the length of the modeled line is comparatively long, to make the models more computationally efficient, each model was subdivided into two equal segments, and then cascading of the corresponding ABCD matrices was performed.

Numerical Simulation Results with Homogenized Frequency-dependent ERD

The models were simulated using the FIT, a time domain solver [43]. Time domain solvers are suited to capturing phase results across wide frequency bands. A mesh size in the

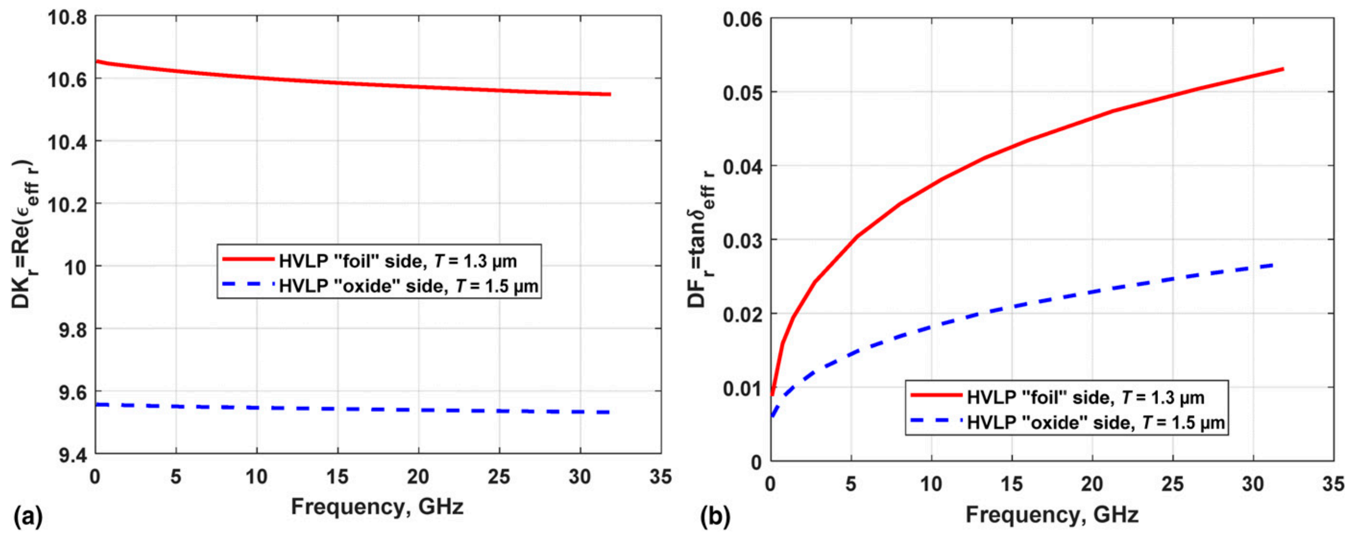

Fig. 11. Effective roughness dielectric parameters as functions of frequency for HVLP foil: DK_r (a) and DF_r (b).

models was about 2 million cells. The waveguide ports were used for excitation. The measured and modeled data for S_{21} parameter as a function of frequency are shown in Figs. 14-16. The dielectric parameters of the homogeneous ERD layers in these models are as those shown in Figs. 9-11. The agreement of the modeled and measured results for all the three test scenarios with STD, VLP, and HVLP foils validates the proposed analytical approach. The discrepancy between the modeled and the measured magnitude $|S_{21}|$ is less than .5 dB over the entire frequency range; the phase difference is within $\pm 10^0$ but depends on the particular frequency. The high-frequency behavior is captured better as than the nondispersive models as in [40, 47, 48] because of the frequency-dependent DK_r and DF_r parameters extracted using the equivalent capacitance ERD model.

Numerical Model of Layered ERD Structure

Another way of roughness dielectric numerical modeling was also tested. The layered model was set up in the same way as the other models, but the "foil" layer is specified differently from the previous models with homogeneous ERD parameters. In the layered model for the roughest STD foil, the roughness dielectric properties are split into three parts: the top 1/3rd part (close to metal) has independent frequency $DK_r = 16$, the middle 1/3rd part has $DK_r = 12$, and bottom 1/3rd part (next to matrix) has $DK_r = 8$. In this case, each sublayer is very thin (thickness of each is $T_r/3 = 4.13$ μm), adding significant mesh count and, therefore, increasing simulation time. Therefore, a different approach was proposed, and it is based on so-called "space mapping" technique, e.g., Ref. [62] and references therein. This space implemented in a number of full-wave 3D numerical simulation tools, including those based on FIT solver. When this space mapping for the layered model is applied, the object is not split into three separate layers/objects with homogeneous dielectric constants, but the object material properties change depending on the position within the object according to the specified "space map." Note that a "space map" based model does not introduce a new kind of material, but is used to define, for a normal (or anisotropic) material, a generic

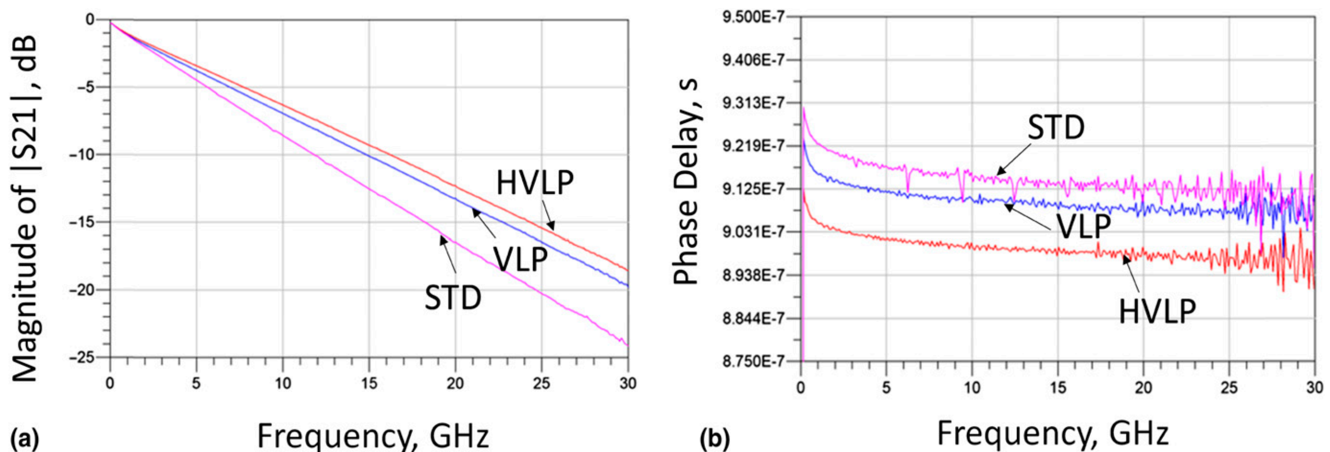

Fig. 12. (a) Magnitude $|S_{21}|$, dB, and (b) phase delay on 16-inch stripline with PPO blend dielectric and different foil types.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

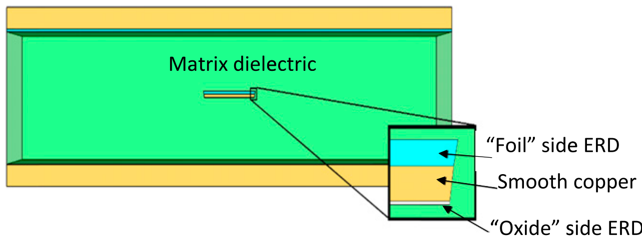

Fig. 13. Numerical model setup.

spatial distribution. This allows for modeling complicated and arbitrary materials. In this work, the ERD itself is specified this way within the matrix material.

This "space mapping" has been applied to the three-layer "foil" side in the STD model only. However, the "space mapping" approach does not allow for modeling lossy layers as the ERD dielectrics are. Therefore, in the space mapping model, loss, or $|S_{21}|$ magnitude, is underestimated because of the lossless model of the STD "foil" roughness dielectric. Nevertheless, it was still reasonable to test this approach with a perspective of extending "space mapping" functionality to lossy materials in future. Because loss was not included in the space-mapped three-layer region, only phases of S_{21} were of interest. Note that for the low-loss PCB materials, phase of S_{21} does not depend much on the loss in the foil; it mainly depends on the corresponding DK_r value. Moreover, phase of S_{21} is more sensitive to model parameter settings than the magnitude $|S_{21}|$, and the $|S_{21}|$ trend with frequency could be easily corrected by adding slightly more loss in the other regions of the model.

In the present "space mapping" model, matrix dielectric and very thin "oxide" ERD sides (STD foils are known to have comparatively smooth "oxide" side) were modeled as regular lossy dielectrics without applying space mapping. The corresponding ERD layers were modeled both on traces and on the ground planes. Therefore, "space mapping" was applied to the "foil" sides of STD conductors only.

In Fig. 17, the measured phase is compared with that of the modeled using "space map" of the ERD layer. The tested cases are the dielectric constants of all three ERD sublayers having first $DK_r = 12$; then all of them having $DK_r = 16$; and finally, the layered roughness dielectric "space map" object with three different $DK_r = 8$, 12, and 16 values defined consequently as moving from the matrix toward smooth conductor. The total ERD thicknesses in all three cases are $T_r = 12.4$ μm.

As Fig. 17 shows, there is an excellent agreement between the measured and the layered model results. The models with a single layer of "foil" ERD having either $DK_r = 12$, or $DK_r = 16$, result in slightly different unwrapped phase than those in the layered model and in measurements. From Table II, the difference between these two results is indeed small (within a few degrees) as compared with the overall unwrapped phase. This result indicates that modeling conductor surface roughness as a multilayered structure is perspective, especially if loss is also implemented in such a "space mapping" model. Note that the aforementioned equivalent capacitance approach to model ERD is also a kind of a multilayer model because it includes slices with incrementally varying dielectric properties that then are integrated and also includes two distinct regions—prepercolation and percolation.

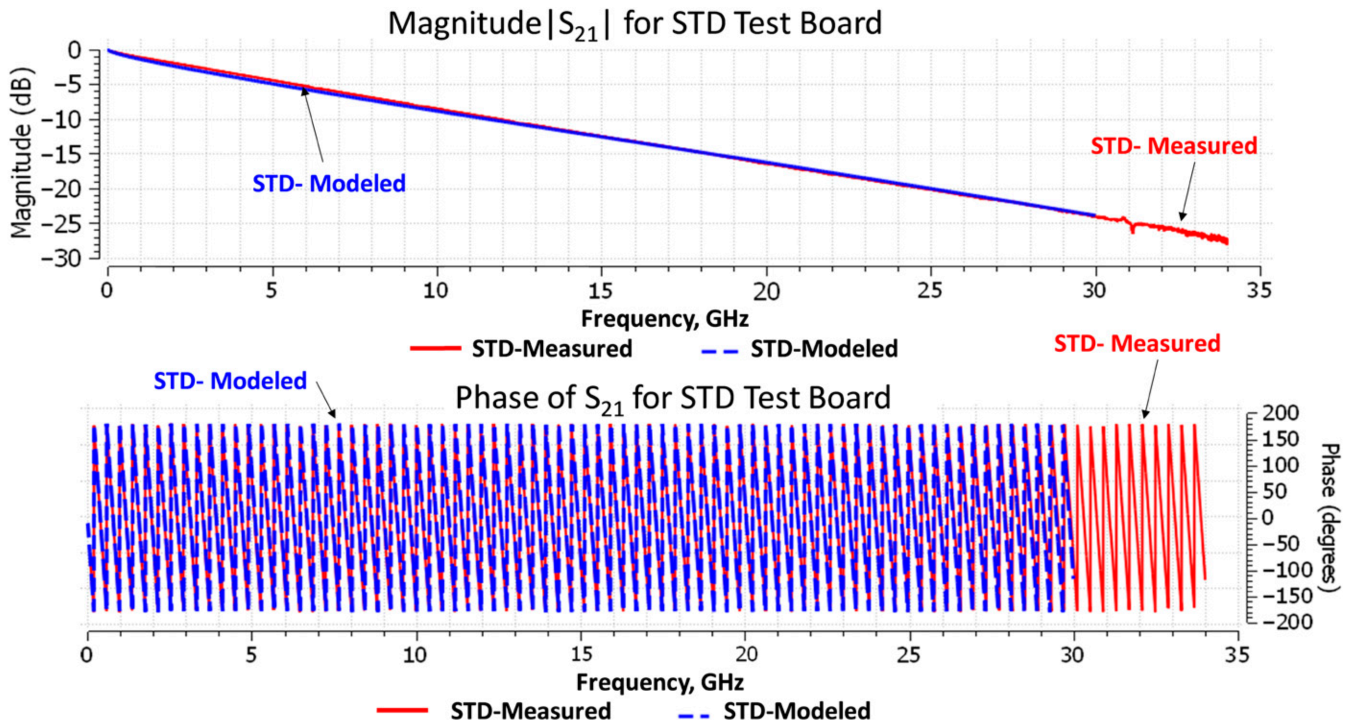

Fig. 14. Measured and modeled S_{21} results for a stripline structure with STD foil.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

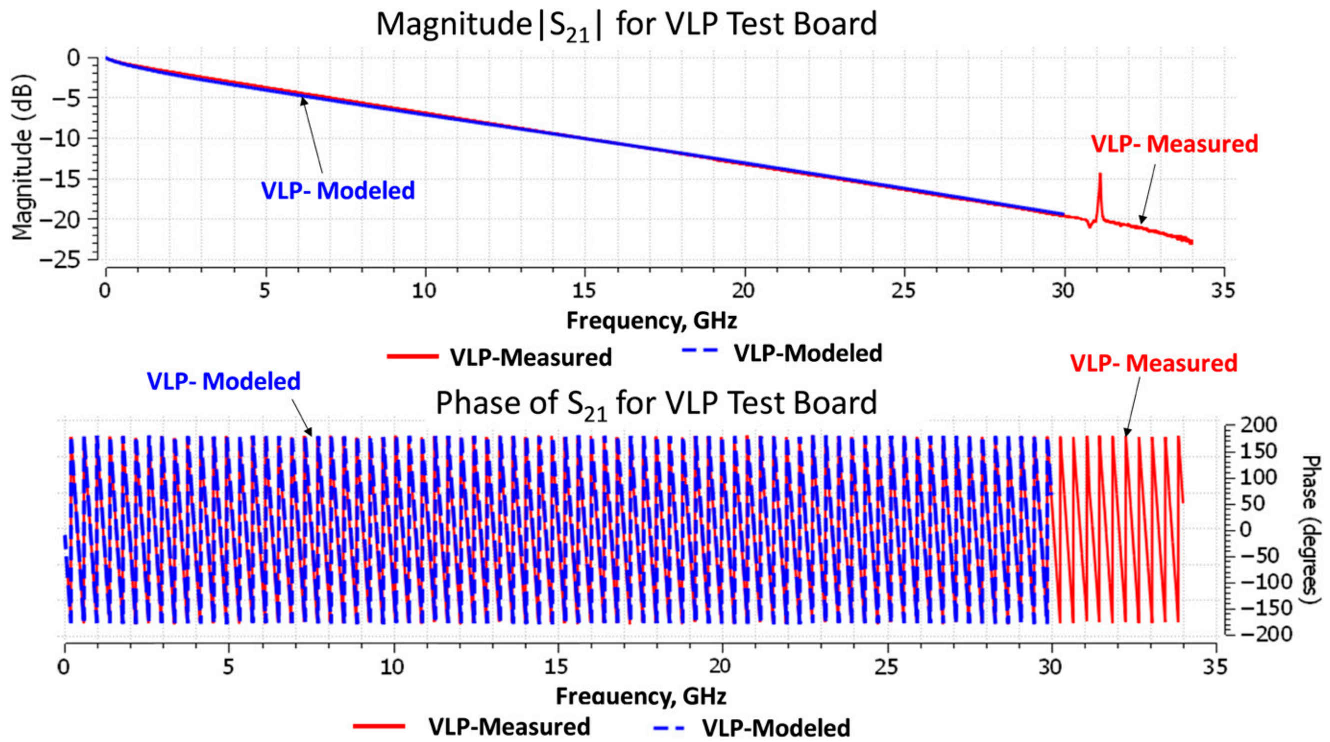

Fig. 15. Measured and modeled S_{21} results for a stripline structure with VLP foil.

Note that the idea of presenting a conductor of planar transmission line as a multilayer structure refers back to the work as in Ref. [63]. However, multilayer approach was applied in Ref. [63] to modeling skin depth in a conductor of a microstrip or stripline rather than conductor surface roughness. In this article, we have considered two models that practically extend this idea to surface roughness consideration—through calculating the equivalent capacitance

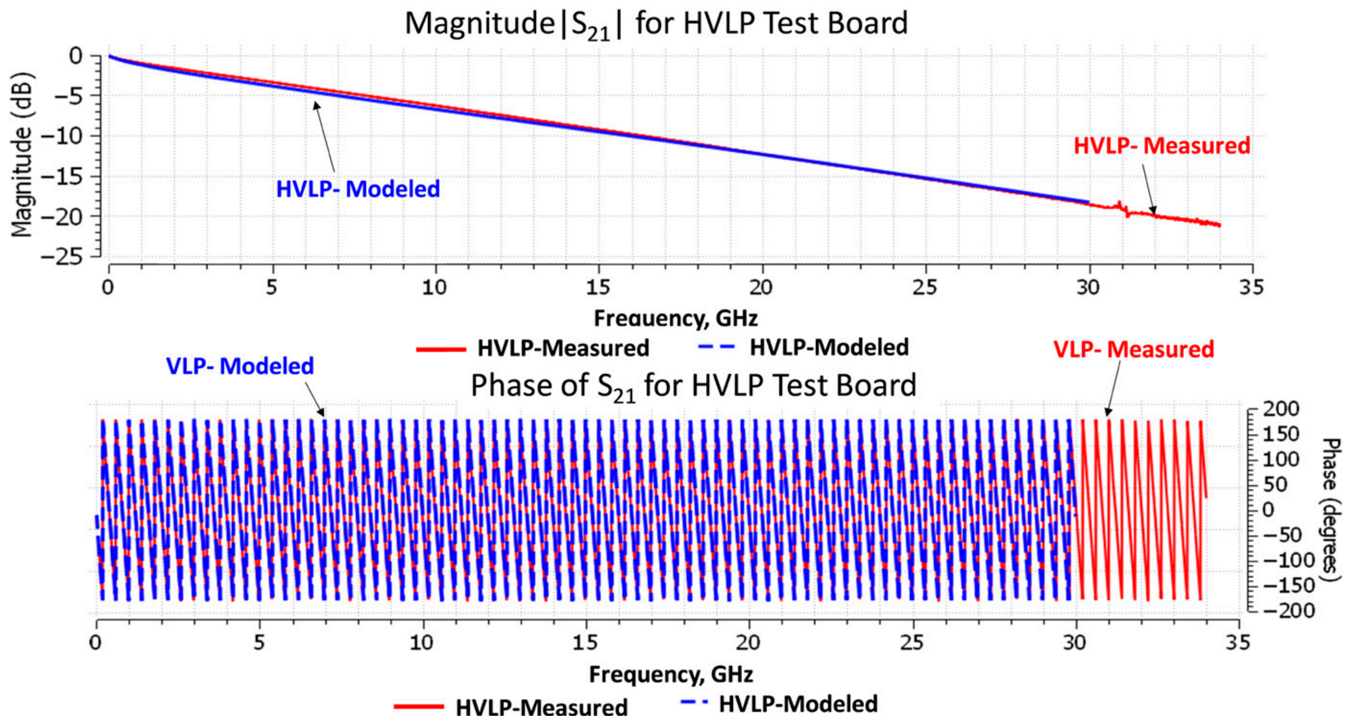

Fig. 16. Measured and modeled S_{21} results for a stripline structure with HVLP foil.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

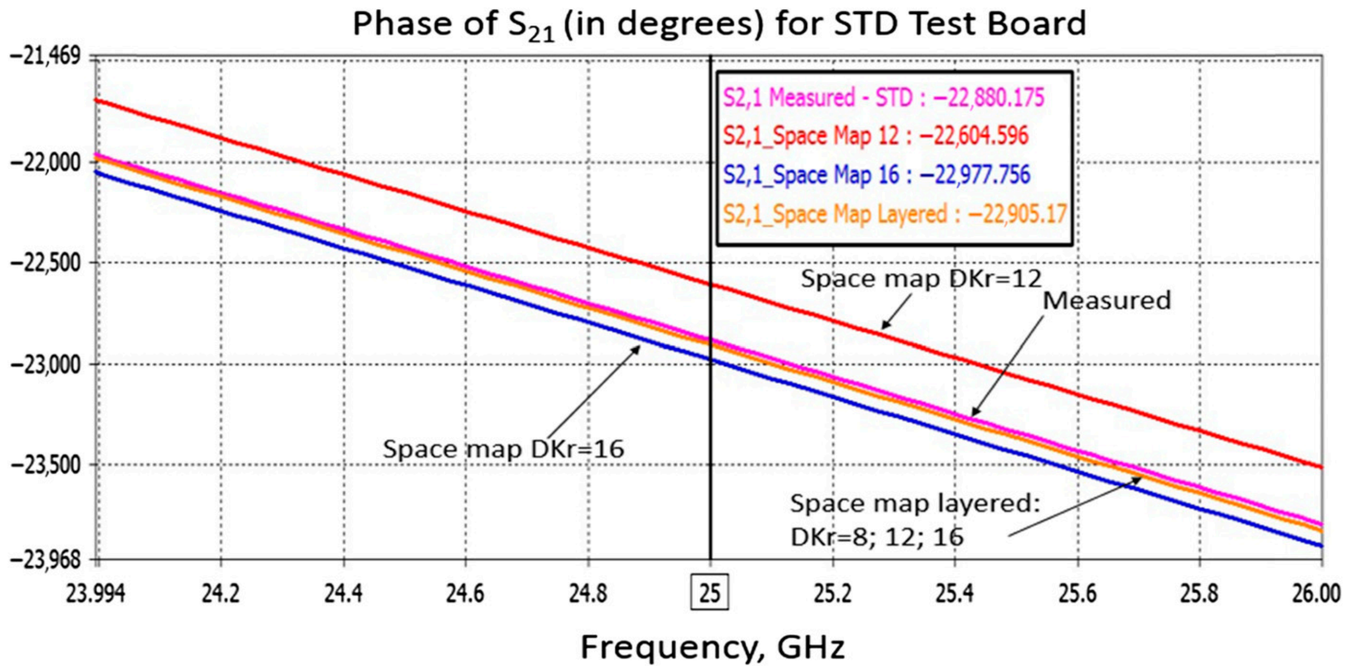

Fig. 17. The phase of measured and modeled structures over a narrow frequency band of ~24-26 GHz: ERD with $DK_r = 12$, with $DK_r = 16$, and with space map–layered structure.

and implementing it in a numerical model and through the direct numerical modeling using "space mapping."

Conclusions

In this work, an analytical model to calculate ERD parameters for conductor surface roughness of a PCB foil is presented. Based on the microscopic analysis of the roughness profile, a concentration dependence of metallic inclusions in the transition between the ambient dielectric matrix and copper is obtained. Using such a concentration dependence, the equivalent capacitance associated with the roughness layer is calculated analytically. Then the parameters of the ERD are extracted from this equivalent capacitance. The ERD parameters obtained from the analytical model are frequency dependent unlike in the previous works; therefore, they describe the high-frequency behavior (at data rates of a few dozen Gbps) of PCB interconnects more accurately than the frequency-independent models. The proposed model is applied to three stripline test scenarios with three different types of foils—STD, VLP, and HVLP—and is validated by an excellent agreement between the full-wave FIT numerical modeling and measurements over a wide frequency range from 10 MHz to 30 GHz. Two types of numerical models are obtained: using homogeneous ERD and using space mapping when modeling a layered ERD. The layered ERD provides the closest to the measured result when S_{21} phases are compared. This proves that the conductor surface roughness has mainly capacitive effect on the phase constant.

Table II
Phase of Analytical and Layered ERD Model at a Number of Frequencies

Discrete frequencies	Phase, degrees (modeled with $DK_r = 12$)	Phase, degrees (modeled with $DK_r = 16$)	Phase, degrees (modeled as layered)	Phase, degrees (measured)
$f = 7$ GHz	−6,334.4757	−6,442.2698	−6,426.1821	−6,436.3764
Difference as compared with measured	101.9007	−5.8934	10.1943	0
$f = 15$ GHz	−13,563.894	−13,790.774	−13,752.316	−13,753.362
Difference as compared with measured	189.468	−38.46	1.046	0
$f = 20$ GHz	−18,080.365	−18,380.305	−18,325.425	−18,318.775
Difference as compared with measured	238.41	−61.53	−6.65	0
$f = 25$ GHz	−22,604.596	−22,977.756	−22,905.17	−22,880.175
Difference as compared with measured	275.579	−97.581	−24.995	0
$f = 30$ GHz	−27,127.231	−27,573.701	−27,482.865	−27,435.057
Difference as compared with measured	307.826	−138.644	−47.808	0
$f = 34$ GHz	−30,755.643	−31,262.769	−31,156.153	−31,078.478
Difference as compared with measured	322.835	−184.291	−77.675	0

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

References

[1] E. Bogatin, D. DeGroot, P.G. Huray, and Y. Shlepnev, "Which one is better? Comparing options to describe frequency dependent losses," *DesignCon 2013*, Santa Clara, CA, USA, January 28-31, 2013, paper 5-WA4.

[2] Y. Shlepnev, "PCB and packaging design up to 50 GHz: identifying dielectric and conductor roughness models," *The PCB Design Magazine*, vol. 2, pp. 12-28, 2014.

[3] L. Simonovich, "Practical method for modeling conductor surface roughness using cubic close-packing of equal spheres", *2016 IEEE International Symposium on Electromagnetic Compatibility*, Ottawa, ON, Canada, 25-29 July 2016, pp. 917-920.

[4] Y. Shlepnev, "Unified approach to interconnect conductor surface roughness modelling," *Proceedings of the 2017 IEEE 26th Conference Electrical Performance of Electronic Packaging and Systems (EPEPS)*, San Jose, CA, USA, October 15-18, 2017, pp. 1-3.

[5] S.P. Morgan, Jr., "Effect of surface roughness on eddy current losses at microwave frequencies," *Journal of Applied Physics*, Vol. 20, pp. 352-362, 1949.

[6] E.O. Hammerstad and F. Bekkadal, *Microstrip Handbook*, ELAB Report, STF 44 A74169, University of Trondheim, Norwegian Institute of Technology, Trondheim, Norway, 1975.

[7] E.O. Hammerstad and O. Jensen, "Accurate models for microstrip computer aided design," *IEEE MTT-S Microwave Symposium Digest*, pp. 407-409, Washington, DC, USA, May 1980.

[8] S. Groiss, I. Bardi, O. Brio, K. Preis, and K. Richter, "Parameters of lossy cavity resonators calculated by the finite element method," *IEEE Transactions on Magnetics*, Vol. 32, No. 3, pp. 894-897, 1996.

[9] I.P. Bushminskiy, A.G. Gudkov, and L.N. Yakuben', "Losses in a microstrip line," *Voprosy Radioelectroniki*, No. 2, pp. 73-87, Ser. Radiotekhnika, Moscow, Russia, February 1982 (in Russian).

[10] P.G. Huray, "Surface roughness," Chapter 6, *The Foundations of Signal Integrity*, pp. 216-276, IEEE Press and Wiley, Hoboken, NJ, USA, 2010.

[11] P.G. Huray, O. Oluwafemi, J. Loyer, E. Bogatin, and X. Ye, "Impact of copper surface roughness texture on loss: a model that works," *DesignCon 2010*, Santa Clara, CA, USA, 1-4 Feb. 2010.

[12] S. Hall, S.G. Pytel, P.G. Huray, D. Hua, A. Moonshiram, G.A. Brist, and E. Sijercic, "Multigigahertz causal transmission line modeling methodology using a 3-D hemispherical surface roughness approach," *IEEE Transactions on Microwave Theory and Technique*s, Vol. 55, No. 12, pp. 2614-2623, 2007, paper 5-TA2.

[13] A.E. Sanderson, "Effect of surface roughness on propagation of the TEM mode," *Advances in Microwaves*, vol. 7, pp. 1-57, Leo Young, editor, Academic Press, Cambridge, MA, 1971.

[14] H. Braunisch, X. Gu, A. Camacho-Bragado, and L. Tsang, "Off-chip rough-metal-surface propagation loss modeling and correlation with measurements," *Proceeding of the 57th IEEE Electronic Components and Technology Conference (ECTC'07)*, Reno, NV, USA, pp. 785-791, May 29-June 1, 2007.

[15] X. Gu, L. Tsang, and H. Braunisch, "Modeling effects of random rough interface on power absorption between dielectric and conductive medium in 3D problem," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 55, No. 3, pp. 511-517, 2007.

[16] R. Ding, L. Tsang, and H. Braunisch, "Wave propagation in a randomly rough parallel-plate waveguide," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 57, No. 5, pp. 1216-1223, 2009.

[17] Q. Chen and N. Wong, "An efficient stochastic integral equation method for modeling the influence of conductor surface roughness on interconnect ohmic loss," *Proceedings of the 50th Midwest Symposium Circuits Systems (MWSCAS)*, Montreal, Que., Canada, pp. 1417-1420, Aug. 5-8, 2007.

[18] S. Sundstroem, "Stripline models with conductor surface roughness," MS thesis, Helsinki University of Technology, Espoo, Finland, Feb. 2004.

[19] M.V. Lukic, "Modeling of 3-D surface roughness effects with application to μ-coaxial lines," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 55, No. 3, pp. 518-525, 2007.

[20] C.L. Holloway and E.F. Kuester, "Power loss associated with conducting and superconducting rough interfaces," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 48, No. 10, pp. 1601-1610, 2000.

[21] S. Hinaga, M. Koledintseva, P. Anmula, and J. Drewniak, "Effect of conductor surface roughness upon measured loss and extracted values of PCB laminate material dissipation factor," *Proceedings of the Technology Conference, IPC APEX EXPO 2009*, Las Vegas, NV, 31 Mar. to 2 Apr. 2009, paper S20-2.

[22] M. Koledintseva, A. Koul, F. Zhou, J. Drewniak, and S. Hinaga, "Surface impedance approach to calculate loss in rough conductor coated with dielectric layer," *Proceedings of the IEEE Symposium Electromagnetic Compatibility*, pp. 790-795, Fort Lauderdale, FL, July 25-30, 2010.

[23] A. Deutsch, A. Huber, G.V. Kopcsay, B.J. Rubin, R. Hemdinger, D. Carey, W. Becker, T. Winkel, and B. Chamberlin, "Accuracy of dielectric constant measurement using the full-sheet-resonance technique IPC-T650 2.5.5.6," *Proceedings of the 2002 IEEE 11th Topical Meeting on Electrical Performance of Electrical Packaging*, Monterey, CA, USA, pp. 311-314, Oct. 21-23, 2002.

[24] A. Deutsch, C.W. Surovic, R.S. Krabbenhoft, G.V. Kocsay, and B.J. Chamberlin, "Prediction of losses caudes by roughness of metallization in printed-circuit boards," *IEEE Transactions on Advanced Packaging*, Vol. 30, No. 2, pp. 279-287, 2007.

[25] X. Chen, "EM modeling of microstrip conductor losses including surface roughness effect," *IEEE Microwave and Wireless Components Letters*, Vol. 17, No. 2, pp. 94-96, 2007.

[26] Y. Shlepnev and C. Nwachukwu, "Roughness characterization for interconnect analysis," *Proceedings of the IEEE International Symposium Electromagnetic Compatibility*, pp. 518-523, Long Beach, CA, USA, August 14-19, 2011.

[27] X. Guo, D.R. Jackson, J. Chen, M.Y. Koledintseva, S. Hinaga, and J.L. Drewniak, "An analysis of conductor surface roughness effects on signal propagation for stripline interconnects," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 56, No. 3, pp. 707-714, 2014.

[28] M. Koledintseva, J. Drewniak, S. Hinaga, F. Zhou, A. Koul, and A. Gafarov, "Experiment-based separation of conductor loss from dielectric loss in PCB striplines," *DesignCon 2011*, Santa Clara, CA, USA, January 31 to February 3, 2011, paper 5-TP5.

[29] A. Koul, M.Y. Koledintseva, J.L. Drewniak, and S. Hinaga, "Differential extrapolation method for separating dielectric and rough conductor losses in printed circuit boards," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 54, No. 2, pp. 421-433, 2012.

[30] M. Koledintseva, A. Koul, S. Hinaga, and J.L. Drewniak, "Differential and extrapolation techniques for extracting dielectric loss of printed circuit board laminates," *Proceedings of the 2011 IEEE MTT-S International Microwave Symposium (IMS-2011)*, Baltimore, MD, USA, 5-10 June 2011, art. no. 5972948, pp. 1-4.

[31] M.Y. Koledintseva, A.V. Rakov, A.I. Koledintsev, J.L. Drewniak, and S. Hinaga, "Improved experiment-based technique to characterize dielectric properties of printed circuit boards," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 56, No. 6, pp. 1556-1559, 2014.

[32] A.F. Horn, III, J.W. Reynolds, P.A. LaFrance, and J. Rautio, "Effect of conductor profile on the insertion loss, phase constant, and dispersion in thin high-frequency transmission lines," *DesignCon*, Santa Clara, CA, USA, February 1-4, 2010, paper 5-TA1.

[33] J.C. Rautio, B.J. Rautio, S. Arvas, A.F. Horn, III, and J.W. Reynolds, "The effect of dielectric anisotropy and metal surface roughness," *Proceedings of the Asia-Pacific Microwave Conference*, Yokohama, Japan, 2010, paper FR3C-4.

[34] A.F. Horn, III, J.W. Reynolds, and J.C. Rautio, "Conductor profile effects on the propagation constant of microstrip transmission lines," *Proceedings of the 2010 IEEE MTT-S International Microwave Symposium*, Anaheim, CA, USA, May 24-27, 2010, paper WE4B-03, pp. 868-871.

[35] G. Gold and K. Helmreich, "A physical surface roughness model and its applications," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 65, No. 10, pp. 3720-3732, 2017.

[36] A.F. Horn, III, C.J. Caisee, P.A. LaFrance, K. Pance, and J.C. Rautio, "Effect of conductor profile on the impedance and capacitance of transmission lines," *DesignCon*, Santa Clara, CA, USA, February 2018, paper 05-WA4.

[37] M.Y. Koledintseva, A. Razmadze, A. Gafarov, S. De, S. Hinaga, and J.L. Drewniak, "PCB conductor surface roughness as a layer with effective material parameters," *Proceedings of the IEEE Symposium Electromagnetic Compatibility*, pp. 138-142, Pittsburgh, PA, USA, 2012.

[38] M.Y. Koledintseva, S. Hinaga, and J.L. Drewniak, "Effect of anisotropy on extracted dielectric properties of PCB laminate dielectrics," *Proceedings of the IEEE Symposium Electromagnetic Compatibility*, pp. 514-517, Long Beach, CA, USA, August 14-19, 2011, pp. 514-517.

[39] M.Y. Koledintseva, A.V. Rakov, A.I. Koledintsev, J.L. Drewniak, and S. Hinaga, "Elimination of conductor foil roughness effects in characterization of dielectric properties of printed circuit boards," *DesignCon 2014*, Santa Clara, CA, USA, January 28-31, 2014, paper 14-TH1.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022

[40] M.Y. Koledintseva, T. Vincent, A. Ciccomancini Scogna, and S. Hinaga, "Method of effective roughness dielectric in a PCB: measurement and full-wave simulation verification," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 57, No. 4, pp. 807-814, 2015.
[41] M. Koledintseva, T. Vincent, and S. Radu, "Full-wave simulation of an imbalanced differential microstrip line with conductor surface roughness," *Proceedings of the IEEE Symposium Electromagnetic Compatibility and Signal Integrity*, pp. 34-39, Santa Clara, CA, USA, March 15-20, 2015.
[42] M.Y. Koledintseva and T. Vincent, "Comparison of mixed-mode S-parameters in weak and strong coupled differential pairs," *Proceedings of the IEEE Symposium EMC*, pp. 610-615, Ottawa, Canada, July 25-30, 2016.
[43] CST STUDIO SUITE, "Dassault systems simulia," [Online]. www.cst.com, 2017.
[44] T. Vincent, "Simulating dielectric and conductor loss including surface roughness," iMAPS, 43rd Symposium and Expo, Boxborough, MA, USA [Online]. http://www.imapsne.org/virtualCDs/2016/2016%20Presentations/A/A4.pdf, May 2016.
[45] Simbeor Electromagnetic Signal Integrity Software, [Online]. www.simberian.com.
[46] Y. Shlepnev, "How interconnects work: conductor roughness modeling with effective roughness dielectric," Simbeor® demo-videos, 2016 [Online]. www.simberian.com/, [Online, also: YouTube, https://www.youtube.com/watch?v=PsM2Wu0pkRo], May 20, 2016.
[47] T. Vincent, M. Koledintseva, A. Ciccomancini, and S. Hinaga, "Effective roughness dielectric in a PCB: measurement and full-wave simulation verification," *Proceedings of the IEEE Symposium Electromagnetic Compatibility*, pp. 798-802, Raleigh, NC, USA, August 3-8, 2014.
[48] M.Y. Koledintseva, O.Y. Kashurkin, T. Vincent, and S. Hinaga, "Effective roughness dielectric to represent copper foil roughness in printed circuit boards," *DesignCon 2015*, Santa Clara, CA, USA, January 27-30, 2015, paper 14-TH4.
[49] S. Hinaga, M. Koledintseva, J. Drewniak, A. Koul, and F. Zhou, "Thermal effects on PCB laminate material dielectric constant and dissipation factor," *Proceeding of the Technology Conference IPC Expo/APEX 2010*, Las Vegas, NV, USA, April 5-8, 2010, paper # S16-1.
[50] S. De, A.Y. Gafarov, M.Y. Koledintseva, S. Hinaga, R.J. Stanley, and J.L. Drewniak, "Semi-automatic copper foil surface roughness detection from PCB microsection images," *Proceedings of the IEEE Symposium Electromagnetic Compatibility*, pp. 132-137, Pittsburgh, PA, USA, 2012.
[51] S. Hinaga, S. De, A.Y. Gafarov, M.Y. Koledintseva, and J.L. Drewniak, "Determination of copper foil surface roughness from microsection photographs," *Proceedings of the Technology Conference IPC Expo/APEX 2012*, Las Vegas, NV, USA, April 2012.
[52] A.V. Rakov, S. De, M.Y. Koledintseva, S. Hinaga, J.L. Drewniak, and R.J. Stanley, "Quantification of conductor surface roughness profiles in printed circuit boards," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 57, No. 2, pp. 264-273, 2015.
[53] Z. Jankovic, M.M. Pavlovich, M.R. Pantovic Pavlovic, M.G. Pavlovic, N.D. Nikolic, J.S. Stevanovic, and S. Prsic, "Electrical and thermal properties of poly(methylmetacrylate) composites filled with electrolytic copper powder," *International Journal of Electrochemical Science*, Vol. 13, pp. 45-57, 2018.
[54] O.Y. Kashurkin, "Measurements and simulation of conductor-related loss of PCB transmission lines," MSEE thesis, Missouri S&T, Rolla, MO, USA, 2016.
[55] J. Baker-Jarvis, M.D. Janezic, B. Riddle, C.L. Holloway, N.G. Paulter, and J.E. Blendell, "Dielectric and conductor-loss characterization and measurements on electronic packaging materials," NIST Technical Note 1520, National Institute of Standards and Technology, U.S. Department of Commerce, Boulder, CO, USA, July 2001.
[56] J.S. Toll, "Causality and the dispersion relation: logical foundations," *Physical Review*, Vol. 104, No. 6, pp. 1760-1770, 1956.
[57] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions on Power Delivery*, Vol. 14, No. 3, pp. 1052-1060, 1999.
[58] B. Gustavsen, "Relaxed vector fitting algorithm for rational approximation of frequency domain responses," *Proceeding of the IEEE Workshop Signal Propagation on Interconnects*, pp. 97-100, Berlin, Germany, May 2006.
[59] M.Y. Koledintseva, J. Wu, J. Zhang, J.L. Drewniak, and K.N. Rozanov, "Representation of permittivity for multi-phase dielectric mixtures in FDTD modeling," *Proceedings of the IEEE Symposium Electromagnetic Compatibility*, vol. 1, pp. 309-314, Santa Clara, CA, USA, August 9-13, 2004.
[60] A.R. Djordjevic, R.M. Biljic, V.D. Likar-Smiljanic, and T.K. Sarkar, "Wideband frequency-domain characterization of FE-r and time-domain causality," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 43, No. 4, pp. 662-667, 2001.
[61] D.M. Pozar, *Microwave Engineering*, 2nd ed., Wiley, Hoboken, NY, 1998, Chapter 2.
[62] New Features 2016, CST Studio Suite, Particle Dynamics Workshop Series, CST – Computer Simulation Technology, [Online] www.cst.com, 2016.
[63] J.C. Rautio and V. Demir, "Microstrip conductor loss models for electromagnetic analysis," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 51, No. 3, pp. 915-921, 2003.

Downloaded from http://meridian.allenpress.com/jmep/article-pdf/15/2/49/2246970/imaps_654479.pdf by guest on 31 October 2022