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A Physics-Based Model for Snapback-Type ESD Protection Devices

Xin Yan, *Member, IEEE*, Seyed Mostafa Mousavi, *Senior Member, IEEE*, Li Shen, Yang Xu, Wei Zhang, *Member, IEEE*, Sergej Bub, Steffen Holland, and Daryl G. Beetner, *Senior Member, IEEE*

***Abstract*—A simplified physical-based model for deep-snapback transient voltage suppressors (TVS) is developed in this article. While based on physics, the number of parameters and components is minimized, so the model can be tuned easily from available measurements of the packaged TVS. SPICE convergence issues seen in previous snapback device models are eliminated by adding nonlinear damping components to the model. No convergence issues were seen among any of the simulations performed for this study, which includes transmission-line pulse tests with multiple levels and rise times. The proposed model was used to represent two different TVS devices and was validated in both device- and system-level simulations. Simulations of quasi-static and transient behavior matched measurement results within about 20% among all the tested cases.**

***Index Terms*—Electrostatic discharge (ESD) protection, silicon-controlled rectifier (SCR), snapback, system-efficient ESD design (SEED) simulation, transient voltage protection.**

I. Introduction

ELECTROSTATIC discharge (ESD) and other similar transient electrical overstress events are common causes of failure in integrated circuits (ICs). Although ESD events typically only last between 1 ns and 1 μs, the peak current can reach tens of amperes. In order to provide system-level ESD protection, the ON- and OFF-chip protection must be designed to shunt the ESD current away from sensitive components during an ESD event while still ensuring the normal operation of ICs. As the ON-chip protection is often not effective against system-level ESD events, carefully designed and implemented OFF-chip protection is often required to achieve high levels of robustness. Critical to optimizing the OFF-chip protection strategy is system-efficient ESD design (SEED) simulations, which require highly accurate transient device models [1], [2].

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Many transient voltage suppression (TVS) devices used for OFF-chip protection are based on a silicon-controlled rectifier (SCR) response, which features a deep-snapback characteristic. SCR-type TVS devices are increasingly popular as they can handle large currents with a small holding voltage in a relatively small-sized package and with low capacitance. A number of models for snapback-type TVS devices have been proposed in the literature. The models in [3], [4], and [5] closely represent the physics behind the operation of SCR-type devices. While these models can be highly accurate, they cannot reasonably be used by an engineer who has little information about the detailed properties of the device, such as its layout and doping characteristics. Tuning the models based on transmission-line pulse (TLP) measurements would be extremely challenging due to many equations and parameters contained within the model. The models in [6] and [7] were developed to represent the fundamental behavior of TVS devices and to be easy to tune, but they only account for the steady-state *I–V* curve of the device and not its transient characteristics. The model in [8] is a behavioral model, which captures some transient characteristics, but its ability to determine the voltage overshoot is limited. Zhou et al. [9] develop a behavioral model, which is capable of accurately capturing the transient characteristics of the TVS, but tuning becomes more difficult as the model becomes more complex and SPICE convergence issues have been observed during in-system simulations [10]. The model in [11] uses a voltage-controlled current source to model ESD metal-oxide-semiconductor (MOS) snapback and is capable of reproducing double snapback behavior but is only built to capture quasi-static *I–V* characteristics and not the transient response. Machine learning techniques are used in [12], [13], and [14] to model snapback and nonsnapback ESD devices. While manual tuning of the model is no longer needed in this case, the large amount of raw silicon data required to train the neural network presents challenges.

In addition to achieving good accuracy and being relatively easy to tune, models should also be robust to SPICE convergence issues. Such issues can be especially problematic in SEED simulations when both OFF-chip and ON-chip protection devices are present, where the simultaneous highly nonlinear response of the two models presents significant challenges [10], [15]. Adding more components to dampen the device response is a typical way to solve convergence issues for the TVS behavior model [8], [10]. These convergence issues were seen with the physics-based model in [5] and were eliminated within the

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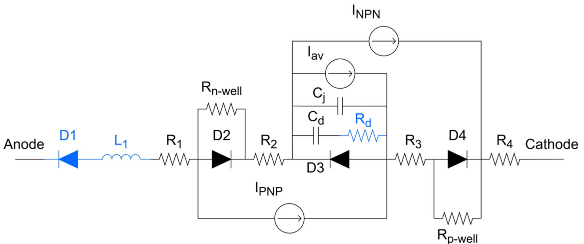

Fig. 1. High-level circuit model of an SCR-type TVS. L_1 and D_1 were added to the model in [5] (shown in blue) to capture the transient behavior and to ease the tuning process. R_d was added to eliminate convergence issues.

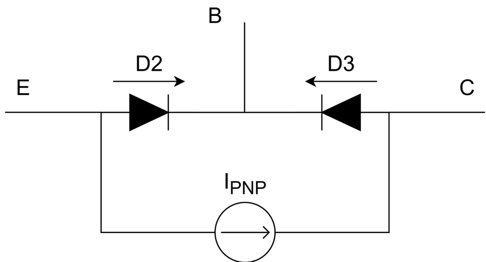

Fig. 2. p-n-p transistor represented by the modified Ebers-Moll model.

simulations shown in that study, but the convergence robustness in SEED simulations is still unknown.

In this article, we propose a simplified physics-based model for the SCR snapback-type TVS device. The number of parameters, which must be tuned, is limited to allow model creation using only data easily obtained from transient and quasi-static measurements of the packaged device. Convergence issues are solved by determining which portions of the model are responsible for instabilities and adding controlled damping components to prevent them. Validation results will be shown for two different snapback TVS devices.

The rest of this article is organized as follows. A detailed description of the model is given in Section II. In Section III, issues with convergence are studied and ways to eliminate these issues are described. Section IV presents the details of device- and system-level validations of the model. The model tuning process is presented in Section V. Finally, Section VI concludes this article.

II. Model Description

The proposed model is based on a modified Ebers-Moll model of coupled n-p-n and p-n-p transistors, with additional components to capture the transient behavior, as shown in Fig. 1 [5].

A. Coupled n-p-n and p-n-p Transistors

The n-p-n or p-n-p transistors are represented by two ideal diodes and a controlled current source [5], as shown in Fig. 2. The currents through the diodes and the current source are given by

$$I_{D2} = \frac{I_s}{\beta_F}\left(e^{\frac{V_{\mathrm{EB}}}{V_T}} - 1\right) \tag{1}$$

$$I_{D3} = \frac{I_s}{\beta_R}\left(e^{\frac{V_{\mathrm{CB}}}{V_T}} - 1\right) \tag{2}$$

$$I_{\mathrm{p-n-p}} = I_s\left(e^{\frac{V_{\mathrm{EB}}}{V_T}} - e^{\frac{V_{\mathrm{CB}}}{V_T}}\right) \tag{3}$$

where I_s is the leakage current, V_T is the thermal voltage, β_F and β_R are the forward and reverse gain of the bipolar junction transistor, respectively, and V_{EB} and V_{CB} are the emitter-to-base and collector-to-base voltages, respectively. The gains are assumed to be constant to help simplify this model. The coupled n-p-n and p-n-p transistors form the basic structure of the SCR-type TVS device, along with the well resistances $R_{\mathrm{n-well}}$ and $R_{\mathrm{p-well}}$.

B. Conductivity Modulation

Conductivity modulation describes the change in conductivity due to the change in carrier concentration of (typically) low-doped regions of the SCR. Conductivity modulation and the device inductance together determine the voltage overshoot across the TVS during turn-ON. In the proposed model, conductivity modulation is included in the (presumably lightly doped) base resistors R_2 and R_3, as [16], [17]

$$R_2(t), R_3(t) = \frac{R_0}{1 + \frac{Q_{\mathrm{charge}}(t)}{Q_0}} \tag{4}$$

where R_0 is the resistance when the current starts to flow, and Q_0 is the threshold charge required to establish increased conduction. The ON-resistance of the device is separated from the modulated resistance and represented by R_1 and R_4. R_2 and R_3 are set equal to each other for simplicity in tuning. Q_{charge} is the charge injected into diode D_3, given by

$$Q_{\mathrm{charge}} = I_s\,\tau\left(e^{\frac{V_{D3}}{V_T}} - 1\right) \tag{5}$$

where τ is the transit time of the p-n junction. R_0 and Q_0 determine the conductivity modulation voltage overshoot and the falling edge of the voltage waveform at the end of a TLP excitation. They can be tuned from transient measurements of the TVS.

C. Avalanche Breakdown

Avalanche breakdown, which occurs in the middle junction D_3 causes the SCR to turn ON. The breakdown behavior needs to be accurately modeled to obtain the correct *I–V* curve and transient waveforms. An approach similar to the one presented in [5] is used to model this behavior. The equation for the avalanche breakdown current is broken into two parts

$$I_{\mathrm{av}} = (I_s + I_{\mathrm{p-n-p}} + I_{\mathrm{n-p-n}})\left(\frac{1}{1 - \frac{V}{V_{\mathrm{BV}}}^{\,n}} - 1\right)$$
$$\text{when } V < kV_{\mathrm{BV}},\ k = 0.99 \tag{6}$$

$$I_{\mathrm{av}} = (I_s + I_{\mathrm{p-n-p}} + I_{\mathrm{n-p-n}})\left(\frac{1}{1 - k^n} - 1\right) + \frac{V - kV_{\mathrm{BV}}}{R}$$
$$\text{When } V \geq kV_{\mathrm{BV}},\ k = 0.99,\ R = 0.01. \tag{7}$$

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The standard Miller multiplication expression is utilized in (6) when the reverse voltage on D_3 is smaller than or close to the breakdown voltage. When the reverse voltage is at or above the breakdown voltage, the relationship between voltage and current is changed to a linear one to avoid singularity issues. In (6) and (7), $V_{\rm BV}$ is the breakdown voltage, and n is a constant, which depends on the transistor's semiconductor characteristics (fixed here to 3, a typical value for silicon, for simplicity). The value of k is set close to 1 to ensure that the breakdown occurs close to $V_{\rm BV}$.

D. Junction and Diffusion Capacitances

In a p-n junction, the junction capacitance C_j dominates when the diode is reverse biased and the diffusion capacitance C_d dominates when the diode is forward biased. Only the capacitance of the middle junction (D_3) was considered in the proposed model, as it plays the most important role in the transient waveform when the device is turning ON. In practice, once the diode is turned ON, the junction capacitance could be fixed to a constant value. The current through the nonlinear diffusion capacitance was modeled as

$$I = \frac{dQ_{\rm charge}}{dt} = \frac{d}{dt}\left[I_s\tau\left(e^{\frac{V_{D3}}{V_T}} - 1\right)\right] = \frac{I_s\tau}{V_T}\cdot e^{\frac{V_{D3}}{V_T}}\cdot\frac{dV_{D3}}{dt}$$
$$\text{where } \frac{I_s\tau}{V_T}\cdot e^{\frac{V_{D3}}{V_T}} = C \quad (8)$$

and C_d is the diffusion capacitance. When the device is reverse biased, the diffusion capacitance given by this equation is small and could cause numerical simulation issues. The diffusion capacitance is, therefore, set to zero when $V_{D3} < 0$.

E. Other Components

R_1 and R_4 are used to represent the series resistance of the device and determine the slope of the quasi-static *I–V* curve after the holding voltage is reached. L_1 is the inductance of the device and contributes to the peak level of the voltage overshoot. An ideal reversed diode D_1 was placed in series with other components to provide an additional voltage drop, which can be tuned to match the measured characteristics of a variety of TVS devices.

III. Convergence Issues

The proposed model was implemented in Keysight advanced design system (ADS). While this model performed better in terms of convergence than in our experience with the previous TVS behavioral models based on switches [10], [15], convergence issues were still observed. For example, Fig. 3(a) shows a plot of the peak transient waveform voltage across the TVS versus the TLP voltage when using the proposed model in a system-level simulation. The estimated peak voltage oscillates with the TLP voltage as a result of numerical oscillations in the simulation. While these oscillations could be mitigated by decreasing the simulation time step or changing the SPICE integration method, a TVS model, which is naturally robust to convergence problems, is preferred.

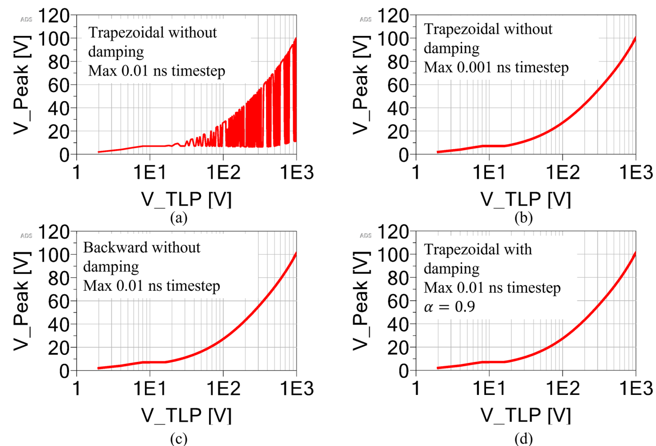

Fig. 3. Comparisons of the peak TVS voltage versus TLP voltage simulated with different strategies to mitigate convergence issues. (a) Trapezoidal integration with maximum 0.01 ns time step, without damping. (b) Trapezoidal integration with maximum 0.001 ns time step, without damping. (c) Backward integration with maximum 0.01 ns time step, without damping. (d) Trapezoidal integration with maximum 0.01 ns time step, with damping $\alpha = 0.9$.

Two common events leading to numerical oscillations are a step change in current through an inductor or a step change in voltage across a capacitor. The trapezoidal integration method, which is an easily implemented second-order numerical integration technique used by SPICE and is the default integration method in ADS, is susceptible to such numerical oscillations. The iteration equation for this method is given by [18]

$$y\ (t) = y\,(t-\Delta t) + \frac{\Delta t}{2}\,(x\,(t) + x\,(t-\Delta t)) \quad (9)$$

where $x = ky'$ (and $k = 1$ is assumed for simplicity), Δt is the time step, and $x(t)$ an unknown to be solved. Equation (9) can be rewritten as follows:

$$x\ (t) = -x\,(t-\Delta t) + \frac{2}{\Delta t}\,(y\,(t) - y\,(t-\Delta t)). \quad (10)$$

From (10), if there is a step change of the input y from $t = t - \Delta t$ to $t = t$, and the value of y remains the same afterward, x will take on a value equal to the negative of the previous value of x and then will oscillate between those values. That is

$$x\ (t+n\Delta t) = -x\,(t+(n-1)\,\Delta t)$$
$$\text{when } y\ (t+n\Delta t) = y\,(t+(n-1)\,\Delta t)\,,\ n = 1,2,3. \quad (11)$$

These oscillations could be mitigated using the backward or Gear 2 integration method, as shown in (12) and (13), respectively, as the value of x at the previous time step is not a part of the calculation

$$y\ (t) = y\,(t-\Delta t) + \Delta t\,(x\,(t)) \quad (12)$$

$$y\ (t) = \frac{4}{3}\,y\,(t-\Delta t) - \frac{1}{3}y\,(t-2\Delta t) + \frac{2}{3}\Delta t\,(x\,(t))\,. \quad (13)$$

One way to eliminate the numerical oscillations is to introduce damping [18]. The trapezoidal integration method with an added

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damping factor α is given by

$$y\ (t)=y\,(t-\Delta t)+\frac{\Delta t}{2}\left((1+\alpha)\,x\,(t)+(1-\alpha)\,x\,(t-\Delta t)\right)\ . \tag{14}$$

Rewriting (14) gives

$$x\ (t)=-\frac{1-\alpha}{1+\alpha}x\,(t-\Delta t)+\frac{2}{\Delta t}\frac{1}{1+\alpha}\left(y\,(t)-y\,(t-\Delta t)\right)\ . \tag{15}$$

The damping factor α ranges in value from 0 to 1. Equation (15) shows that the damping is equivalent to a linear interpolation between the trapezoidal and backward integration methods. When α is equal to 1, trapezoidal integration with damping becomes the backward integration method. By adding an appropriate value for the damping factor, numerical oscillations could be suppressed in a few time steps without significantly impacting other simulation results.

Modeling an ideal capacitor using (14) is equivalent to using ordinary trapezoidal integration in a capacitor with a series "damping" resistance. Assuming an ideal capacitor with a capacitance C_0, the expression for the voltage and current using trapezoidal integration with damping is

$$V\ (t)=V\ (t-\Delta t)+\frac{\Delta t}{2C_0}\left[(1+\alpha)\,I\ (t)+(1-\alpha)\,I\ (t-\Delta t)\right] \tag{16}$$

$$V\ (t)-V\ (t-\Delta t)$$
$$=\frac{\Delta t}{2C_0}\left[I\ (t)+I\ (t-\Delta t)\right]+\frac{\alpha\Delta t}{2C_0}\left[I\ (t)-I\ (t-\Delta t)\right] \tag{17}$$

where (17) is a rewritten form of (16). The right-hand side of (17) has two terms. The first term is the ordinary trapezoidal integration for an ideal capacitor, and the second term comes from the damping, which is equivalent to a series resistor with $R=\alpha\Delta t/(2C_0)$. The resistance is determined by the damping factor α, the time step Δt, and the capacitance C_0.

In the proposed model, the numerical oscillation occurs during the turn-ON of the device. The voltage on the middle junction changes dramatically within a few time steps as does the value of the diffusion capacitance. Although there is no warning or error when numerical oscillations are present, and the transient simulation completes "successfully," unreasonably large currents and voltages were observed in simulations at the junction after breakdown, which suggested that the diffusion capacitance was the root cause. To eliminate the numerical oscillation in the proposed model, a nonlinear damping resistance R_d was added in series with the diffusion capacitance with a value determined by an equation derived from (8) and (17) as follows:

$$R_d=\frac{\alpha\Delta t}{2\frac{I_s\tau}{V_T}\cdot e^{\frac{V_n}{V_T}}}. \tag{18}$$

The damping resistance R_d was implemented in ADS by setting the value of Δt to the internal variable "time step." During the default ADS simulation approach based on truncation error, this time step will change throughout the simulation. By allowing the value of R_d to change accordingly ensures that only the required level of damping is used and no more at each simulation interval.

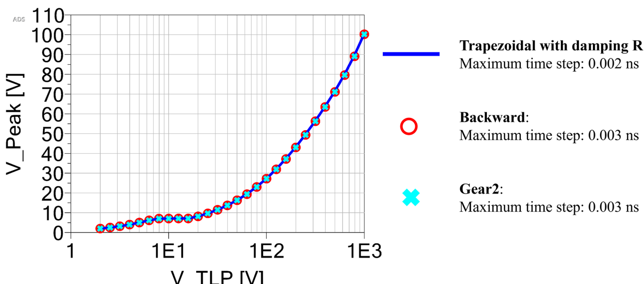

Fig. 4. Comparisons of the peak TVS voltage versus TLP voltage for different integration methods when using a fixed time step. Results are shown for the maximum simulation time step, which yields consistently stable results.

Fig. 3 shows the impact of different convergence mitigation strategies when using the model to predict the peak transient voltage across the TVS in a system-level simulation. Numerical oscillations in the results are observed in Fig. 3(a) when using a maximum 0.01 ns time step as no damping. These oscillations could be eliminated by reducing the time step, as shown in Fig. 3(b), although simulation time will increase and the user must be on the lookout for such issues and be ready to modify the simulation time if required. Fig. 3(c) shows that the oscillations can also be eliminated using the backward integration method without reducing the 0.01 ns time step. Fig. 3(d) shows the results when adding the proposed dynamic damping resistance R_d to the model. The numerical oscillations were eliminated in this case without reducing the time step or requiring additional actions from the user.

If this model was implemented in a SPICE tool, where the time step was unavailable, a value of R_d could be used, which was sufficiently large to make convergence issues unlikely, or a fixed simulation time step could be used along with an appropriate value of R_d. In this case, the maximum time step should be smaller than those encountered using the truncation error method to avoid unstable results or errors, no matter which integration method is used. Fig. 4 shows that the three integration methods can have a similar performance if the correct maximum time step is chosen. The disadvantage compared with the proposed damping resistance, however, is that the user must be aware of how to tune the simulation to ensure convergence and, in fact, must be aware that a convergence issue occurred.

IV. Model Validation

A. Device-Level Modeling

The model was validated through application to two commercial SCR-type TVS devices, the Nexperia PESD3V3Y1BSF [19] and the Nexperia PESD1V2Y1BSF [20]. The turn-ON behavior of each TVS was measured through very fast TLP testing. An ESD-EMC TLP-ES620-50 compact pulsed *I*–*V* curve system along with a 2 GHz 10 GSa/s Rohde & Schwarz oscilloscope was used to create and record the 10 ns TLP waveforms with a rise time of 0.65 ns. Both quasi-static *I*–*V* curves and the

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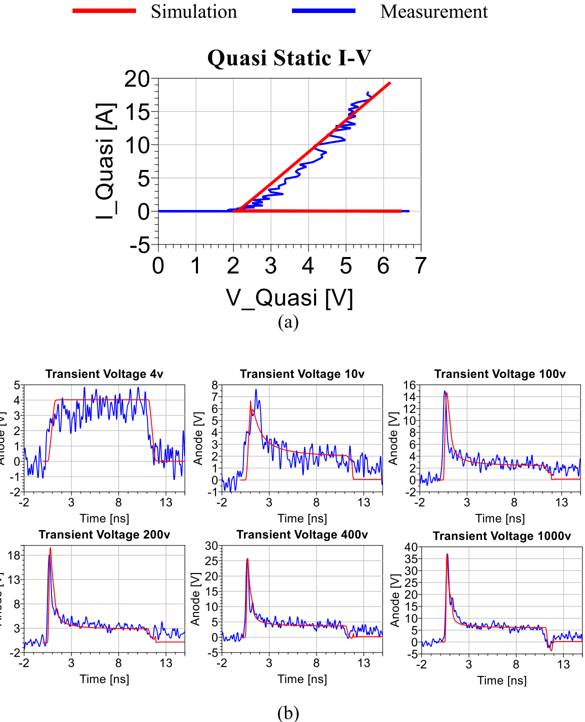

Fig. 5. Measured and simulated response of the Nexperia PESD3V3Y1BSF TVS device. Measurements are shown in blue and simulations in red. (a) Quasi-static *I*–*V* curve. (b) Transient responses for six TLP voltages.

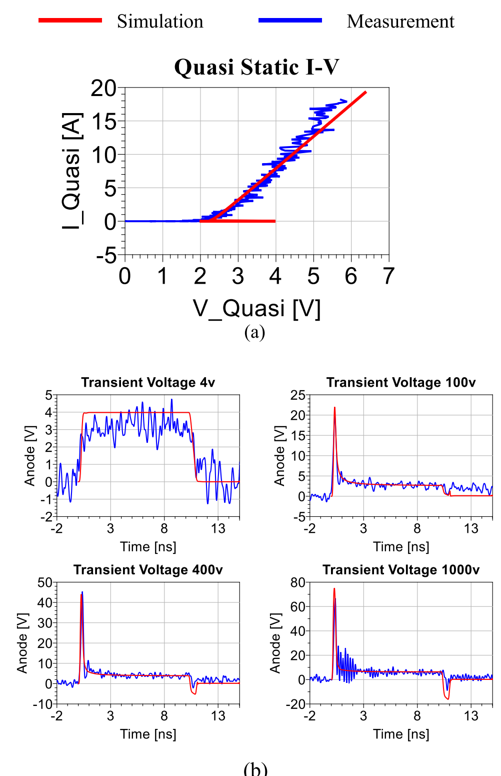

Fig. 6. Measurement and simulation comparisons for the Nexperia PESD1V2Y1BSF TVS device. Measurements are shown in blue and simulations in red. (a) Quasi-static *I*–*V* curve. (b) Transient responses for four TLP voltages.

transient responses were captured using the TLP software. The proposed model was then tuned based on the measured results. The examples of the measured and simulated quasi-static and transient results for the PESD3V3Y1BSF TVS device are shown in Fig. 5.

Simulations were performed using an ideal voltage source representing the TLP pulse. The quasi-static *I*–*V* curve was obtained by calculating the average voltage and current in a time window from 7 to 9 ns, similar to the measured results. As shown in Fig. 5(a), the simulated quasi-static *I*–*V* curve matches with the measured curve well, within about a 10% error. As the TLP pulse was only 10 ns long, self-heating can be ignored. Fig. 5(b) compares the transient response for two example TLP voltages. Although there is a small discrepancy between simulations and measurements at low TLP levels (e.g., at 10 V), the overall simulation matches measurements well, particularly at higher voltages (e.g., above 100 V). The voltage overshoot and the falling edges of the waveform were captured well.

Fig. 6 shows the measured and simulated results when modeling the Nexperia PESD1V2Y1BSF TVS device. The simulated results also closely match the measured quasi-static *I*–*V* and transient curves, within about 10% maximum error.

B. System-Level Modeling

The ability to predict the interaction between two ESD protection devices is more challenging than capturing the behavior of one device alone. The proposed model was validated in a SEED simulation, where an OFF-chip protection device protected an IC with an ON-chip diode, with a 50-Ω trace in between, as shown in Fig. 7. The IC was represented by a protection diode and the two modeled TVS devices were used as the OFF-chip protection in subsequent simulations. A 20-ns TLP pulse was injected into one end of the trace. The rise time of the pulse was varied from 0.65 to 5 ns and the level from 10 to 94 V with a linear step of 6 V. The transient voltages and currents at the IC and at the OFF-chip TVS device were captured as described in [9] and [15]. The measured TLP voltage when injecting into a 50-Ω load was also captured and used as the source waveform in the SEED simulations.

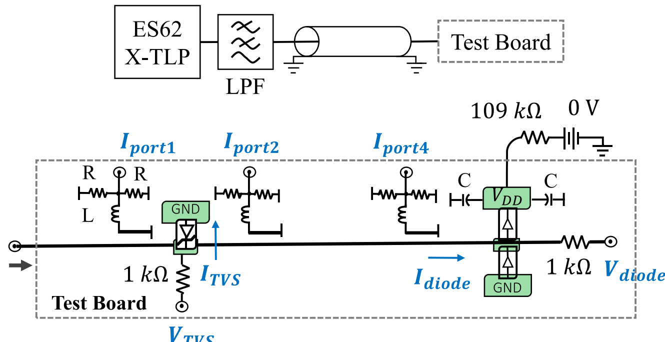

Fig. 7. SEED test schematic.

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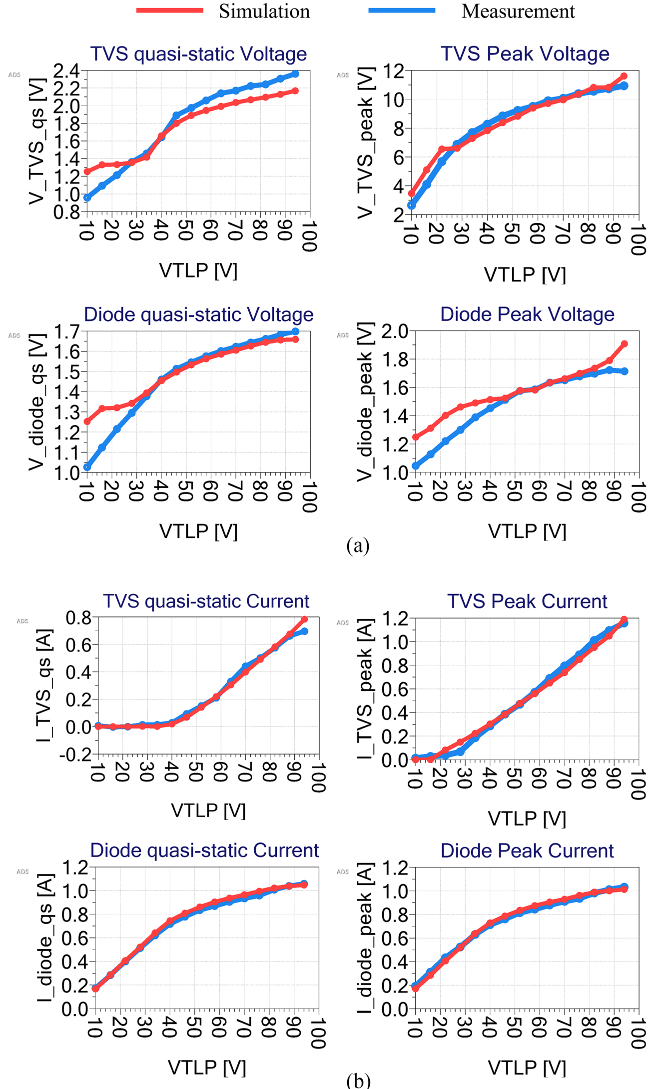

Fig. 8. Measured and simulated SEED simulation results for the PESD3V3Y1BSF TVS device when using a 1 ns TLP rise time. Measurements are shown in blue and simulations in red. (a) Voltage across the OFF-chip TVS and ON-chip diode. (b) Current through the OFF-chip TVS and ON-chip diode.

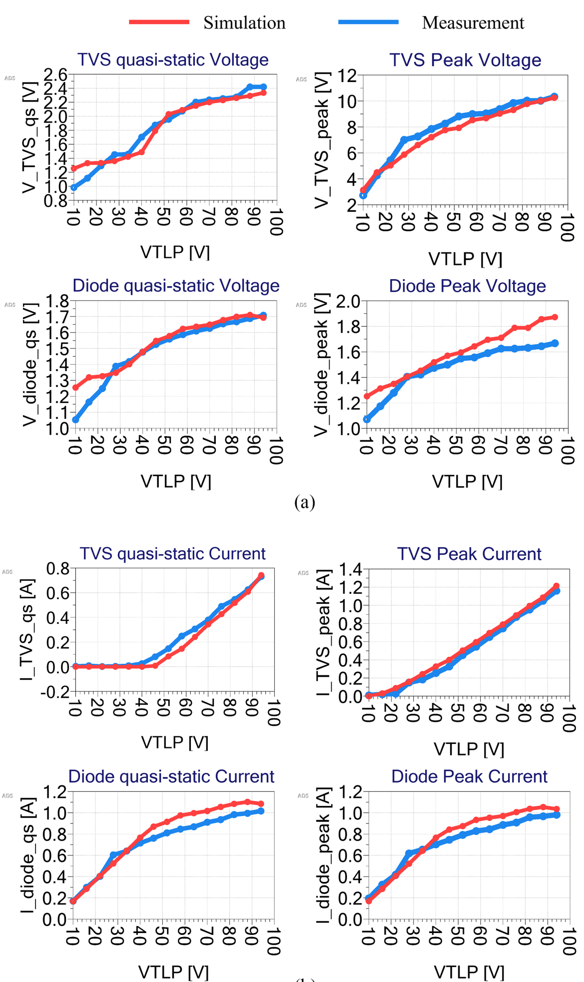

Fig. 9. Measured and simulated SEED simulation results for the PESD1V2Y1BSF TVS device when using a 1 ns TLP rise time. Measurements are shown in blue and simulations in red. (a) Voltage across the OFF-chip TVS and ON-chip diode. (b) Current through the OFF-chip TVS and ON-chip diode.

Comparisons between the measured and simulated results when the PESD3V3Y1BSF TVS was used as the OFF-chip protection are shown in Fig. 8. Results are shown for the quasi-static and peak values of the current and voltage at both the OFF-chip and ON-chip devices for a 1 ns rise time. The simulated peak and quasi-static voltages and currents were within a maximum error of 20% and 15% of rms error for each case. Fig. 9 shows similar comparisons when the PESD1V2Y1BSF TVS was used as the OFF-chip protection. Similar to the first TVS, the overall prediction accuracy was within a maximum error of 20% and 12% of rms error. Similar results were observed for the other three rise times tested.

Example transient responses for the PESD3V3Y1BSF and PESD1V2Y1BSF TVS devices are shown in Figs. 10 and 11, respectively. The ringing of the ON-chip diode voltage in the measurements is caused by multiple reflections between the TVS

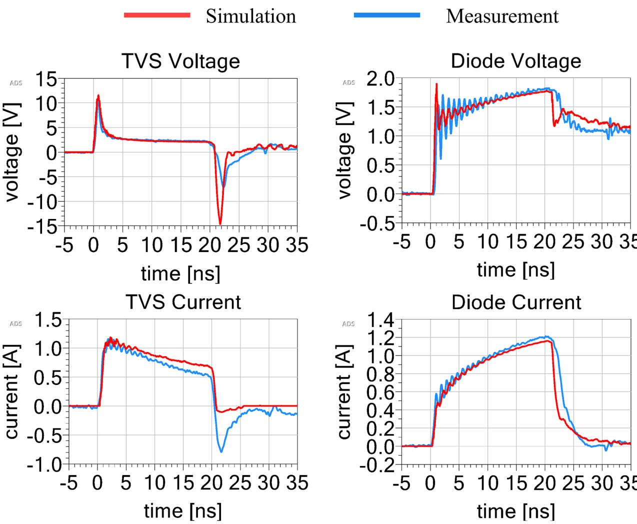

Fig. 10. Simulated (red) and measured (blue) transient currents and voltages associated with components in the SEED simulation when using TVS device PESD3V3Y1BSF and a 1 ns TLP rise time.

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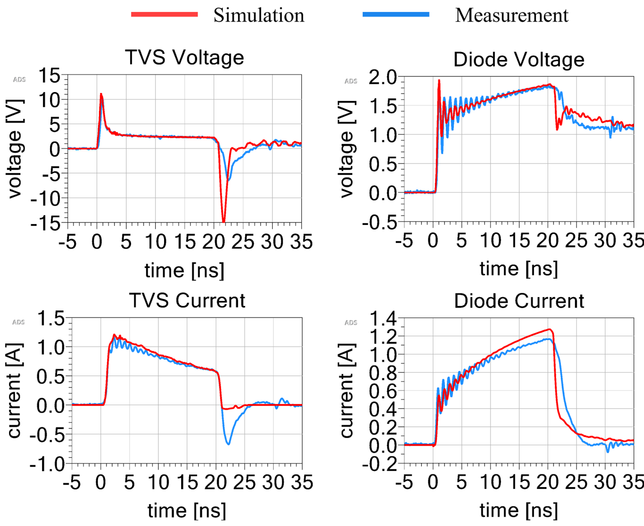

Fig. 11. Simulated (red) and measured (blue) transient currents and voltages associated with components in the SEED simulation when using TVS device PESD1V2Y1BSF and a 1 ns TLP rise time.

and ON-chip diode once they turn ON and appear as "shorts." There is also some difference in the response after the TLP injection ends because of the nonideal behavior of the TLP, which is not included in our model, although this difference is not critical and can be ignored. Overall, the proposed model did a good job of capturing and predicting the most important behaviors in this SEED simulation (i.e., peak voltage and current, and quasi-static voltage and current, for both TVS and ON-chip diode).

It is noteworthy that no convergence issues or numerical oscillations were observed among all 1120 simulations performed here for the two devices, for different TLP levels and rise times, and for both device-level and system-level simulations.

V. Model Tuning

The proposed model was designed to be tuned using only measurements easily performed at the package level. For simplicity, some parameters were fixed to reasonable "known" values before tuning. These parameters are typical for most SCR-type TVS diodes [21], so can be assumed to be known and do not need to be tuned during the normal tuning process. The well resistances $R_{\mathrm{n-well}}$ and $R_{\mathrm{p-well}}$ were fixed at 200 Ω. The junction capacitance was set to 0.1 pF. The junction capacitance cannot be set too large or *dv/dt* triggering caused by the well resistance and junction capacitance could cause the device to incorrectly turn ON at low voltages. The forward and reverse gains of the n-p-n and p-n-p were set to 2 and 1, respectively. The forward gain could change the turn-ON behavior. A forward gain that is too high may result in an underestimated peak voltage, while a forward gain that is too low may result in the device failing to turn ON at the desired breakdown voltage [5]. The damping factor was set to $\alpha = 0.9$, which was found to be a reasonable value to avoid numerical oscillations. While these parameter values worked well here and should be appropriate

TABLE I
Parameters of the TVS Diode Models

PESD3V3Y1BSF		PESD1V2Y1BSF	
V_{BV}	4 V	V_{BV}	2 V
V_{D1}	0.7 V	V_{D1}	1 V
R_1, R_4	0.09 Ω	R_1, R_4	0.09 Ω
L_1	0.2 nH	L_1	0.6 nH
R_0	90 Ω	R_0	100 Ω
Q_0	1e-11	Q_0	5e-12
Other Parameters			
C_j		0.1 pF	
R_{n-well}, R_{p-well}		200 Ω	
β_F		2	
β_R		1	
τ		50e-9	
I_s		1e-15	
α (damping)		0.9	

for many SCR-type TVS diodes, users may find that they need to be modified for other devices.

The other parameters were tuned one at a time based on the measurements. The quasi-static *I–V* curve should be tuned first. The reverse breakdown voltage of the ideal diode D_1 should next be tuned to match the holding voltage. Then, the parameter V_{BV} in (6) should be tuned to match the breakdown voltage. The breakdown voltage of D_1 and V_{BV}, and the initial voltage drop from the coupled n-p-n and p-n-p transistors together determine the breakdown voltage of the model, as follows:

$$V_{\mathrm{Breakdown}} = V_{D1} + V_{\mathrm{BV}} + V_{\mathrm{CE(sat)}} + V_{\mathrm{EB(on)}}. \quad (19)$$

$V_{\mathrm{CE(sat)}}$ is the voltage drop across the n-p-n and $V_{\mathrm{EB(on)}}$ is the voltage between the emitter and the base of p-n-p. R_1 and R_4 are the series resistance in the device and determine the slope of the quasi-static *I–V* curve after the holding voltage and current is reached.

After matching the quasistatic *I–V* curve, the values of R_0 and Q_0 determining conductivity modulation should be tuned to match the voltage overshoot and the falling edge of the transient waveforms. The inductance L_1 also contributes to the voltage overshoot, but as the relationship between the TLP voltage versus overshoot is different for inductance and conductivity modulation [17], it is possible to get reasonable values for all three L_1, R_0, and Q_0. To tune these values, a relatively slow rise time should be chosen (e.g., 1 ns or 2 ns), and the double peaks in the transient overshoot may be seen [17]. The first peak is caused by the conductivity modulation and the second peak is from the inductance. The R_0 and Q_0 are tuned for the first peak and L_1 is tuned for the second peak, respectively. Once initial values of parameters are tuned to roughly capture the behavior of the device, then the parameters can be fine-tuned together or separately, as appropriate, to better capture the results at different rise times.

The parameters of the TVS diode models used in this article are listed in Table I as a reference.

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VI. Conclusion

In this article, we proposed a simplified physics-based model for SCR-type snapback TVS devices. By reducing the number of components and parameters, the model can be relatively easily tuned using only the measurements performed on the package device, without the need for detailed silicon-level information. Issues with convergence were studied to determine its root cause and were eliminated by adding a nonlinear damping resistance in series with the p-n junction capacitance of the junction responsible for turn-ON. The damping resistance was set according to the simulation time step to ensure stability in a wide variety of simulation setups, although could also be set to a constant value if required for compatibility with a specific SPICE tool. By adding this damping resistance to the model, the model's stability could be assured without requiring additional intervention from the user. This feature is important as not all users may understand how to modify the SPICE tool setup to ensure stability or even recognize when a stability issue is present, as not all convergence issues are obvious. Device- and system-level (SEED) simulations with two commercially available TVS devices were utilized to validate the model. Simulation results demonstrate matched measurements within about 20% for both quasi-static and transient results for each of the TLP conditions tested. No convergence issues or numerical oscillation were observed for all 1120 simulations of the two devices, the device- and system-level setups, and the various TLP levels and rise times. We found this physics-based model to be both easier to tune and more stable than previous behavioral models built for similar purposes [9], [15]. Overall, this model shows promise as a tool for representing TVS devices in SEED simulations.

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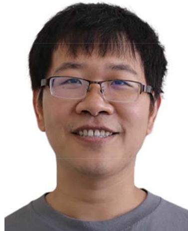

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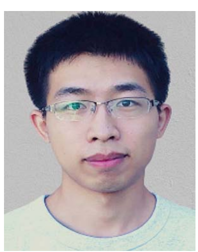

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