August 2023

Self-Adaptive Capacitor for Micro-Display Sub-Pixels

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SELF-ADAPTIVE CAPACITOR FOR MICRO-DISPLAY SUB-PIXELS

FIELD OF THE INVENTION

[0001] This disclosure relates generally to micro-displays (e.g., for artificial reality systems), and more specifically to capacitors for micro-displays.

BACKGROUND

[0002] A display device can be used in a virtual reality (VR), augmented reality (AR), or a mixed reality (MR) system as a head-mounted display (HMD) or a near-eye display (NED). A micro-display enables high resolution images for VR, AR, or MR systems. A silicon backplane of a micro-display allows pixels having a smaller pitch relative to pixels of existing screens that use thin-film transistors (TFT). However, to support the increased number of pixels that the smaller pitch enables and the higher frame rate at which each of these pixels operate (e.g., to display high resolution images), display devices reduce the amount of time allocated to prepare and write data to these pixels. Especially when organic light emitting diode (OLED) display devices are used, operations associated with compensating the threshold voltage of driving transistors by using a reference voltage tend to take up an extended amount of time. Furthermore, threshold voltage compensation becomes less effective at lower gray levels, degrading image quality.

SUMMARY

[0003] Display devices and methods described herein may enable high resolution images in display devices by adjusting threshold voltage compensation at a driving transistor through

reducing a discharge time of a capacitor coupled to the driving transistor. In particular, the current supplied to the driving transistor may correspond to the discharge time of the capacitor that is the source of a current through the driving transistor to a light emitting element (e.g., an OLED). In one embodiment, a pixel of a display device includes a light emitting element (e.g., an OLED) that is coupled to a low voltage source, a select transistor that selectively passes through pixel data from a data line, a switch transistor that is configured to selectively connect to a high voltage source, a driving transistor coupled to the light emitting element, and a capacitor coupled to the driving transistor. The driving transistor has a drain coupled to the light emitting element, a gate coupled to the select transistor to receive the pixel data, and a source coupled to the switch transistor. The driving transistor is configured to perform threshold voltage compensation according to adjustments of a current received at the drain of the driving transistor. The capacitor includes a gate coupled to the source of the driving transistor, a source coupled to the gate of the driving transistor, and a non-uniform channel region. The capacitance of the capacitor increases with a decrease of a gate-source voltage applied to the gate and decreases with an increase of the gate-source voltage applied to the gate.

[0004] In another embodiment, a method for operating a pixel includes providing, via a switch transistor and a driving transistor, a first current from a high voltage source to a light emitting element. The driving transistor may be located between the high voltage source and the light emitting element. A data signal may be provided from a data line to a gate of the driving transistor. A capacitor can be charged in response to turning on the select transistor and the switch transistor. The capacitor may be operated according to a non-uniform capacitance-voltage curve to decrease a discharging time constant of the capacitor at a low brightness level of the light emitting element. In some embodiments, the capacitor may be embodied as a non-uniform channel transistor. Operating the capacitor may include operating the capacitor at a

different amounts of channel inversion in response to a different gate-source voltage provided at a gate of the capacitor. For example, the capacitor may be operated at a whole channel inversion in response to a first gate-source voltage provided to the gate, a partial channel inversion in response to a second gate-source voltage that is greater than the first gate-source voltage, and an absence of channel inversion in response to a third gate-source voltage that is greater than the second gate-source voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1A is a perspective view of a headset implemented as an eyewear device, in accordance with one embodiment.

[0006] FIG. 1B is a perspective view of a headset implemented as a head-mounted display, in accordance with one embodiment.

[0007] FIG. 2 is a circuit diagram illustrating a pixel, in accordance with one embodiment.

[0008] FIG. 3 shows a cross section of a capacitor of a subpixel of a display element, in accordance with one embodiment.

[0009] FIG. 4 shows a cross section of a capacitor having varying threshold voltages, in accordance with one embodiment.

[0010] FIG. 5 shows a capacitance-voltage (C-V) profile in a capacitor, in accordance with one embodiment.

[0011] FIGS. 6A-6D show C-V profiles for different implant region configurations in a capacitor, in accordance with some embodiments.

[0012] FIGS. 7A-7C show C-V profiles for various capacitor shapes, in accordance with some embodiments.

[0013] FIG. 8 is a flowchart of a process for operating a capacitor for providing current to a driving transistor to perform threshold voltage compensation, in accordance with one embodiment.

[0014] FIG. 9 is a system that includes a headset, in accordance with one embodiment.

[0015] The figures depict various embodiments for purposes of illustration only. One skilled in the art will readily recognize from the following discussion that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles described herein.

DETAILED DESCRIPTION

[0016] Embodiments of the invention may include or be implemented in conjunction with an artificial reality system. Artificial reality is a form of reality that has been adjusted in some manner before presentation to a user, which may include, e.g., a virtual reality (VR), an augmented reality (AR), a mixed reality (MR), a hybrid reality, or some combination and/or derivatives thereof. Artificial reality content may include completely generated content or generated content combined with captured (e.g., real-world) content. The artificial reality content may include video, audio, haptic feedback, or some combination thereof, any of which may be presented in a single channel or in multiple channels (such as stereo video that produces a three-dimensional effect to the viewer). Additionally, in some embodiments, artificial reality may also be associated with applications, products, accessories, services, or some combination thereof, that are used to create content in an artificial reality and/or are otherwise used in an artificial reality. The artificial reality system that provides the artificial reality content may be implemented on various platforms, including a wearable device (e.g., headset) connected to a host computer system, a standalone wearable device (e.g., headset), a mobile device or

computing system, or any other hardware platform capable of providing artificial reality content to one or more viewers.

[0017] FIG. 1A is a perspective view of a headset 100 implemented as an eyewear device, in accordance with one or more embodiments. In some embodiments, the eyewear device is a near eye display (NED). In general, the headset 100 may be worn on the face of a user such that content (e.g., media content) is presented using a display assembly and/or an audio system. However, the headset 100 may also be used such that media content is presented to a user in a different manner. Examples of media content presented by the headset 100 include one or more images, video, audio, or some combination thereof. The headset 100 includes a frame, and may include, among other components, a display assembly including one or more display elements 120, a depth camera assembly (DCA), an audio system, and a position sensor 190. While FIG. 1A illustrates the components of the headset 100 in example locations on the headset 100, the components may be located elsewhere on the headset 100, on a peripheral device paired with the headset 100, or some combination thereof. Similarly, there may be more or fewer components on the headset 100 than what is shown in FIG. 1A.

[0018] The frame 110 holds the other components of the headset 100. The frame 110 includes a front part that holds the one or more display elements 120 and end pieces (e.g., temples) to attach to a head of the user. The front part of the frame 110 bridges the top of a nose of the user. The length of the end pieces may be adjustable (e.g., adjustable temple length) to fit different users. The end pieces may also include a portion that curls behind the ear of the user (e.g., temple tip, ear piece).

[0019] The one or more display elements 120 provide light to a user wearing the headset 100. As illustrated the headset includes a display element 120 for each eye of a user. In some embodiments, a display element 120 generates image light that is provided to an eyebox of the

headset 100. The eyebox is a location in space that an eye of user occupies while wearing the headset 100. For example, a display element 120 may be a waveguide display. A waveguide display includes a light source (e.g., a two-dimensional source, one or more line sources, one or more point sources, etc.) and one or more waveguides. Light from the light source is in-coupled into the one or more waveguides which outputs the light in a manner such that there is pupil replication in an eyebox of the headset 100. In-coupling and/or outcoupling of light from the one or more waveguides may be done using one or more diffraction gratings. In some embodiments, the waveguide display includes a scanning element (e.g., waveguide, mirror, etc.) that scans light from the light source as it is in-coupled into the one or more waveguides. Note that in some embodiments, one or both of the display elements 120 are opaque and do not transmit light from a local area around the headset 100. The local area is the area surrounding the headset 100. For example, the local area may be a room that a user wearing the headset 100 is inside, or the user wearing the headset 100 may be outside and the local area is an outside area. In this context, the headset 100 generates VR content. Alternatively, in some embodiments, one or both of the display elements 120 are at least partially transparent, such that light from the local area may be combined with light from the one or more display elements to produce AR and/or MR content.

[0020] In some embodiments, a display element 120 does not generate image light, and instead is a lens that transmits light from the local area to the eyebox. For example, one or both of the display elements 120 may be a lens without correction (non-prescription) or a prescription lens (e.g., single vision, bifocal and trifocal, or progressive) to help correct for defects in a user's eyesight. In some embodiments, the display element 120 may be polarized and/or tinted to protect the user's eyes from the sun.

[0021] In some embodiments, the display element 120 may include an additional optics block (not shown). The optics block may include one or more optical elements (e.g., lens,

Fresnel lens, etc.) that direct light from the display element 120 to the eyebox. The optics block may, e.g., correct for aberrations in some or all of the image content, magnify some or all of the image, or some combination thereof.

[0022] The DCA determines depth information for a portion of a local area surrounding the headset 100. The DCA includes one or more imaging devices 130 and a DCA controller (not shown in FIG. 1A), and may also include an illuminator 140. In some embodiments, the illuminator 140 illuminates a portion of the local area with light. The light may be, e.g., structured light (e.g., dot pattern, bars, etc.) in the infrared (IR), IR flash for time-of-flight, etc. In some embodiments, the one or more imaging devices 130 capture images of the portion of the local area that include the light from the illuminator 140. As illustrated, FIG. 1A shows a single illuminator 140 and two imaging devices 130. In alternate embodiments, there is no illuminator 140 and at least two imaging devices 130.

[0023] The DCA controller computes depth information for the portion of the local area using the captured images and one or more depth determination techniques. The depth determination technique may be, e.g., direct time-of-flight (ToF) depth sensing, indirect ToF depth sensing, structured light, passive stereo analysis, active stereo analysis (uses texture added to the scene by light from the illuminator 140), some other technique to determine depth of a scene, or some combination thereof.

[0024] The audio system provides audio content. The audio system includes a transducer array, a sensor array, and an audio controller 150. However, in other embodiments, the audio system may include different and/or additional components. Similarly, in some cases, functionality described with reference to the components of the audio system can be distributed among the components in a different manner than is described here. For example, some or all of the functions of the controller may be performed by a remote server.

[0025] The transducer array presents sound to user. The transducer array includes a plurality of transducers. A transducer may be a speaker 160 or a tissue transducer 170 (e.g., a bone conduction transducer or a cartilage conduction transducer). Although the speakers 160 are shown exterior to the frame 110, the speakers 160 may be enclosed in the frame 110. In some embodiments, instead of individual speakers for each ear, the headset 100 includes a speaker array comprising multiple speakers integrated into the frame 110 to improve directionality of presented audio content. The tissue transducer 170 couples to the head of the user and directly vibrates tissue (e.g., bone or cartilage) of the user to generate sound. The number and/or locations of transducers may be different from what is shown in FIG. 1A.

[0026] The sensor array detects sounds within the local area of the headset 100. The sensor array includes a plurality of acoustic sensors 180. An acoustic sensor 180 captures sounds emitted from one or more sound sources in the local area (e.g., a room). Each acoustic sensor is configured to detect sound and convert the detected sound into an electronic format (analog or digital). The acoustic sensors 180 may be acoustic wave sensors, microphones, sound transducers, or similar sensors that are suitable for detecting sounds.

[0027] In some embodiments, one or more acoustic sensors 180 may be placed in an ear canal of each ear (e.g., acting as binaural microphones). In some embodiments, the acoustic sensors 180 may be placed on an exterior surface of the headset 100, placed on an interior surface of the headset 100, separate from the headset 100 (e.g., part of some other device), or some combination thereof. The number and/or locations of acoustic sensors 180 may be different from what is shown in FIG. 1A. For example, the number of acoustic detection locations may be increased to increase the amount of audio information collected and the sensitivity and/or accuracy of the information. The acoustic detection locations may be oriented

such that the microphone is able to detect sounds in a wide range of directions surrounding the user wearing the headset 100.

[0028] The audio controller 150 processes information from the sensor array that describes sounds detected by the sensor array. The audio controller 150 may comprise a processor and a computer-readable storage medium. The audio controller 150 may be configured to generate direction of arrival (DOA) estimates, generate acoustic transfer functions (e.g., array transfer functions and/or head-related transfer functions), track the location of sound sources, form beams in the direction of sound sources, classify sound sources, generate sound filters for the speakers 160, or some combination thereof.

[0029] The position sensor 190 generates one or more measurement signals in response to motion of the headset 100. The position sensor 190 may be located on a portion of the frame 110 of the headset 100. The position sensor 190 may include an inertial measurement unit (IMU). Examples of position sensor 190 include: one or more accelerometers, one or more gyroscopes, one or more magnetometers, another suitable type of sensor that detects motion, a type of sensor used for error correction of the IMU, or some combination thereof. The position sensor 190 may be located external to the IMU, internal to the IMU, or some combination thereof.

[0030] In some embodiments, the headset 100 may provide for simultaneous localization and mapping (SLAM) for a position of the headset 100 and updating of a model of the local area. For example, the headset 100 may include a passive camera assembly (PCA) that generates color image data. The PCA may include one or more RGB cameras that capture images of some or all of the local area. In some embodiments, some or all of the imaging devices 130 of the DCA may also function as the PCA. The images captured by the PCA and the depth information determined by the DCA may be used to determine parameters of the local area, generate a model of the local area, update a model of the local area, or some combination thereof. Furthermore,

the position sensor 190 tracks the position (e.g., location and pose) of the headset 100 within the room. Additional details regarding the components of the headset 100 are discussed below in connection with FIG 9.

[0031] FIG. 1B is a perspective view of a headset 105 implemented as a HMD, in accordance with one or more embodiments. In embodiments that describe an AR system and/or a MR system, portions of a front side of the HMD are at least partially transparent in the visible band (~380 nm to 750 nm), and portions of the HMD that are between the front side of the HMD and an eye of the user are at least partially transparent (e.g., a partially transparent electronic display). The HMD includes a front rigid body 115 and a band 175. The headset 105 includes many of the same components described above with reference to FIG. 1A, but modified to integrate with the HMD form factor. For example, the HMD includes a display assembly, a DCA, an audio system, and a position sensor 190. FIG. 1B shows the illuminator 140, a plurality of the speakers 160, a plurality of the imaging devices 130, a plurality of acoustic sensors 180, and the position sensor 190. The speakers 160 may be located in various locations, such as coupled to the band 175 (as shown), coupled to front rigid body 115, or may be configured to be inserted within the ear canal of a user.

[0032] FIG. 2 is a circuit diagram illustrating a subpixel 200, according to some embodiments. The subpixel 200, or sub-pixel 200, may be included in a display element (e.g., the display element 120). The display element may be an integrated circuit including a backplane, active display area, and a control circuit for controlling the active display area. The subpixel 200 may include, among other components, a select transistor SEL, a driving transistor MD, an OLED, a reset transistor REST, a switch transistor SW, and capacitor Cst1. The OLED is connected between a low voltage source ELVSS and a drain of the driving transistor MD. When the switch transistor SW is turned on and the reset transistor REST is turned off, the

driving transistor MD generates current in its drain that increases as a voltage stored by the storage capacitor Cst1 increases. Capacitor Cst1 stores a voltage difference between the high voltage source ELVDD and the source of the driving transistor MD when the switch transistor SW is turned off. The current generated in the drain of the driving transistor MD is then provided to the OLED to drive the OLED. The OLED then generates light of intensity that corresponds to the amount of current provided by the driving transistor MD.

[0033] The select transistor SEL controls a connection between the gate terminal of the driving transistor MD and the data line DL. When the gate line GL provides a gate-on signal (e.g., turns low), the select transistor SEL turns on, connecting the gate of the driving transistor MD to the data line DL and charging the storage capacitor Cst1 based on a voltage difference between the voltage of the pixel data at the data line DL and the high voltage level (ELVDD). When the gate-on signal is turned off in gate line GL, the select transistor SEL is turned off, disconnecting the gate of the driving transistor MD from the data line DL.

[0034] The reset transistor REST enables or disables the current from the driving transistor MD to flow in the OLED. When the reset transistor REST is turned on, current from the driving transistor MD flows through the reset transistor REST to ground or a lower voltage source (AGND) that has a lower potential. Conversely, when the reset transistor REST is turned off, the current from the driving transistor MD flows in the OLED.

[0035] In one or more embodiments, the transistors SEL, REST, SW and driving transistor MD are embodied as P-channel metal-oxide-semiconductor (PMOS) transistors. Further, these components are fabricated on a silicon substrate.

[0036] The subpixel 200 illustrated in FIG. 2 is merely an example, and pixels with different architecture may be used in other embodiments. For example, a pixel with only one capacitor (e.g., Cst1) may be used.

[0037] In a display device pixel, the resistance that contributes to the discharge time of the capacitor (i.e., discharging time constant τ = resistance R * capacitance C) may be dominated by the driving transistor channel resistance, which can increase as the gate voltage at the driving transistor increases, pulling the driving transistor into a subthreshold regime. This increased gate voltage and subthreshold regime may coincide with a higher signal voltage at the data line (Vdata) coupled to the driving transistor and/or a lower gray level at the pixel (i.e., a lower brightness level). Furthermore, some existing capacitors may have a capacitance-voltage (C-V) profile that exhibits an increased capacitance as the gate voltage increases. This may further drive the discharging time constant higher as gate voltage increases. To mitigate the increase of the discharging time constant τ, the display device described herein lowers the capacitance C at lower brightness levels.

[0038] In one non-limiting example, the capacitor may be embodied as an n-type metal-oxide-semiconductor (nMOS) with a non-uniform channel that enables a capacitance that is a function of Vdata: when Vdata is lower (e.g., at higher brightness levels), the capacitance is higher and when Vdata is higher, the capacitance is lower. By modifying a capacitor within the pixel design and not adding additional components to adjust threshold voltage compensation, the display device herein does not increase the size of the pixel. This avoids an increased discharge time at a high capacitance and higher brightness levels because of a higher discharging current or a lower driving transistor channel resistance. Furthermore, this avoids an increased discharge time at a low capacitance and lower brightness levels because the decreased capacitance contributes to a decreased discharging time of the capacitor. Thus, the display device described herein enables sufficient voltage threshold compensation within a range of low to high brightness levels. Additional examples of self-compensation of driving transistor threshold voltage are

found in U.S. Patent Application 17/709,989, filed March 31, 2022, which is incorporated herein by reference.

[0039] FIG. 3 shows a cross section of a capacitor 300 of a subpixel of a display element, in accordance with one embodiment. FIG. 3 shows one portion of the cross section to promote clarity. For example, a drain terminal is present in the capacitor 300 although the drain terminal is not depicted in FIG. 3. FIGS. 4-6 also show portions of cross sections, and additional components of the capacitors in FIGS. 4-6 may be omitted from the depiction to promote clarity.

[0040] The capacitor 300 may be embodied as a MOS transistor, as shown in FIGS. 3-6. The MOS transistor may have a substrate 301 that is p-doped (i.e., an n-channel MOS or nMOS) or have a substrate 301 that is n-doped (i.e., a p-channel MOS or pMOS).

[0041] The capacitor 300 includes the substrate 301, a gate 302, a source 303, and an implant region 304. A length across the surface of the substrate 301 from the source 303 to the drain may include a region having ion implantation of one or more ion concentrations. This region is referred to herein as an implant region. The length from location d_1 to location d_2 of the implant region 304 includes varying ion concentrations. An implant region with varying ion concentrations may be referred to as a non-uniform channel. Similarly, a transistor having such an implant region may be referred to as a non-uniform channel transistor. The implant region 304 may include a threshold voltage implant, which can be an area of ion implantation within the substrate 301 that is configured to adjust a threshold voltage of the MOS transistor.

[0042] A threshold voltage graph 310 shows the threshold voltage as a function of a position from location d_1 to location d_2 at the surface of the substrate to which the graph 310 is aligned. The graph 310 shows that the threshold voltage across the implant region 304 is a non-uniform voltage: the threshold voltage across the surface of the substrate 301 absent an implant region is a voltage that is less than the threshold voltage at the threshold voltage implant. In some

embodiments, the threshold voltage closer to the source 303 is lower than the threshold voltage closer to the drain.

[0043] FIG. 4 shows a cross section of a capacitor 400 having varying threshold voltages, in accordance with one embodiment. The capacitor 400 is embodied as a MOS transistor that includes a substrate 401, a gate 402, a source 403, and the implant region 404. The implant region 404 spans across the surface of the substrate 401 from location d_3 to location d_4. The implant region 404 has multiple threshold voltages corresponding to the varying ion concentration from location d_3 to location d_4. For example, the threshold voltage Vt may vary within a range of -0.7 to 0.2 volts (V). This may be achieved by applying annealing and diffusion to a single voltage threshold implant. For example, the gradient ion concentration may be implemented by forming an ion implant at a portion of the surface of the substrate 401 and using annealing and diffusion to disperse the ion dopant concentrations along the surface of the substrate 401 from location d_4 towards location d_3. Although FIG. 4 depicts discrete areas in different stippling patterns to show the different ion implant concentrations, the ion concentrations may not necessarily be embodied in discrete portions of the implant region 404.

[0044] The varying threshold voltages are shown through a voltage graph 410 that depicts the threshold voltage as a function of a position from location d_3 to location d_4 at the surface of the substrate 401 to which the graph 410 is aligned. The graph 410 shows that the threshold voltage across the implant region 404 is a non-uniform voltage. Similar to the threshold voltage of the capacitor 300, the threshold voltage may be larger closer to the drain of the capacitor 400 than towards the source 403. The varying values of threshold voltages in one capacitor may be represented by multiple capacitors having the respective values of threshold voltages (e.g., transistors in series sharing the same bias voltage at the gates).

[0045] An implant region of a capacitor of a subpixel of a display element may have different configurations than shown in FIGS. 3 and 4. For example, a non-uniform channel may include implant regions that are spaced apart (i.e., noncontiguous ion implant regions separated by region(s) without ion implantation). Each implant region may have the same or different ion concentrations. Implant regions with different ion concentrations produce different voltage thresholds at respective implant regions.

[0046] FIG. 5 shows a capacitance-voltage (C-V) profile 500 in a capacitor, in accordance with one embodiment. In particular, the profile 500 shows how the capacitance of the capacitor 400, which has multiple threshold voltages, depends on the gate-source voltage, or "the bias voltage." The inversion channel of the capacitor 400 is a function of the bias voltage applied to the capacitor 400. For example, within a particular range of bias voltages, as the bias voltage increases, the inversion channel decreases. Additionally, an increase in bias voltages applied to the capacitor 400 may correspond with a decreasing gray level at the subpixel having the capacitor. An amount of the inversion channel present for a particular bias voltage is depicted via the shading areas 501a-501c. A smaller shaded area corresponds to a decreased channel inversion. As the amount of channel inversion decreases, the capacitance of the capacitor 400 may also decrease. The shaded areas 501a-501c are used for convenience and do not represent a realistic depiction of a decrease in an inversion layer in the channel.

[0047] In response to a bias voltage 511 applied to the capacitor 400, the whole channel is inverted, depicted by the shaded area 501a, which may extend to the drain of the transistor although it is not depicted. In response to a bias voltage 512 applied to the capacitor, the channel is not fully inverted, as depicted by the shaded area 501b, and the capacitance decreases as compared to the capacitance exhibited when the channel is fully inverted. In response to a bias voltage 513 applied to the capacitor 400, the inversion of the channel further decreases, as

depicted by the shaded area 501c which is smaller than the shaded area 501b. In response to a bias voltage 514 applied to the capacitor 400, the inversion layer of the channel disappears fully, as depicted by the absence of a shaded area similar to 501a-501c. When the inversion layer is absent, the capacitance of the capacitor 400 may be at a minimum. As the capacitance of the capacitor decreases, the RC time constant of the capacitor also decreases (i.e., the discharging time decreases), and consequently, the driving transistor may be sufficiently compensated as the capacitor discharges.

[0048] FIGS. 6A-6D show C-V profiles for different implant region configurations in a capacitor, in accordance with some embodiments. In addition to a non-uniform channel enabling various capacitances in a C-V profile, the distribution of the non-uniform ion implantation (e.g., the locations of different ion implant concentrations at the surface of the substrate) can contribute to a shape of the C-V profile. This is demonstrated by various non-uniform distributions in the capacitors 600, 610, 620, and 630 of FIGS. 6A-6D. Different C-V profiles may be obtained by varying a doping species, the annealing process (e.g., temperature, time duration of exposure to the heating temperature, etc.), implant opening areas (e.g., layouts), or a combination thereof. For example, arsenic is a doping species that can be used and is less diffusive than the doping species of phosphorous. In another example, a higher temperature or longer annealing time induces more diffusion. In yet another example, multiple masked implants can also lead to different doping concentrations at pre-defined regions.

[0049] FIG. 6A shows a capacitor 600 having a C-V profile 601. The capacitor 600 has varying threshold voltages across the implant region, as shown by the Vt line below the implant region. The Vt line shows the threshold voltage at the corresponding position above the line in the implant region. The capacitor and threshold voltage line are similarly shown in FIG. 4 and the C-V profile is similarly shown in FIG. 5. The gradual change in ion concentration across a

larger length of the surface of the substrate may be commensurate to a larger window of bias voltages for which different capacitances may be achieved (i.e., the sloped region of the C-V profile 601). This may be further evident through a comparison of the C-V profile 601 with the C-V profiles 611, 621, and 631.

[0050] FIG. 6B shows a capacitor 610 having a C-V profile 611. The threshold voltage of the capacitor 610 across the length of the implant region 614 is shown by the Vt line below the implant region 614. The implant region 614 has a greater proportion of a lower ion concentration, depicted by the lighter shade of stippling, than a higher ion concentration, depicted by the darker shade of stippling. The portion of the implant region 614 having a lower ion concentration is located towards the source 613 and the portion having a higher ion concentration is located towards the drain. The greater proportion of the lower ion concentration towards the source causes a higher, constant capacitance for a large window of bias voltages applied to the capacitor 610, as shown in C-V profile 611. There is a smaller window of bias voltages corresponding to the different capacitances of the capacitor 610.

[0051] FIG. 6C shows a capacitor 620 having a C-V profile 621. The threshold voltage of the capacitor 620 across the length of the implant region 624 is shown by the Vt line below the implant region 624. The implant region 624 has a greater proportion of a higher ion concentration, depicted by the darker shade of stippling, than a lower ion concentration, depicted by the lighter shade of stippling. The portion of the implant region 624 having a higher ion concentration is located towards the drain and the portion having a lower ion concentration is located towards the source 623. The greater proportion of the higher ion concentration towards the drain causes a lower, constant capacitance for a large window of bias voltages applied to the capacitor 620, as shown in the C-V profile 611. Similar to the C-V profile 601, there is a smaller window of bias voltages corresponding to the different capacitances of the capacitor 620.

[0052] FIG. 6D shows a capacitor 630 having a C-V profile 631. The threshold voltage of the capacitor 630 across the length of the implant region 634 is shown by the Vt line below the implant region 634. The implant region 634 has a greater portion of both a highest and a lowest ion concentration, depicted by the darkest and lightest stippling, respectively, than intermediate amounts of ion concentrations, depicted by other shades of stippling. The portion of the implant region 634 having the highest concentration of ions is located towards the drain and the portion of the implant region 634 having the lowest concentration of ion is located towards the source 633. The greater proportion of the highest and lowest ion concentrations causes constant capacitances for two windows of bias voltages (e.g., a first window having a lower range of bias voltages and a second window having a higher range of bias voltages). The C-V profile 631 has a smaller window of bias voltages for producing different capacitances at the capacitor 630 than the capacitor 610. This may be due to the smaller proportion of intermediate amounts of ion concentrations as compared to the highest and lowest ion concentrations at the implant region 634.

[0053] FIGS. 7A-7C show C-V profiles for various capacitor shapes, in accordance with some embodiments. Each of the C-V profiles 700, 710, and 720 are depicted using the same tick marks (i.e., the same increment of capacitance along the y-axis and the same increment of bias voltage along the x-axis for each of the graphs). Capacitance of a capacitor may be proportional to the total area of the capacitor. FIG. 7A shows the C-V profile 700 decreasing with an increasing gate voltage, where the decreasing occurs at a first rate. The first rate may occur when the inversion layer area decreases at a uniform rate. FIG. 7B shows the C-V profile 710 decreasing at a second rate greater than the first rate. The second rate may occur when the inversion layer area decreases at an accelerated rate relative to the uniform rate. FIG. 7C shows

the C-V profile 720 decreasing at a third rate less than the first rate. The third rate may occur when the inversion layer area decreases at a decelerated rate relative to the uniform rate.

[0054] FIG. 8 is a flowchart of a process 800 for operating a capacitor for providing current to a driving transistor to perform threshold voltage compensation, in accordance with one embodiment. A display assembly may perform the process 800. In particular, a control circuit of the display assembly may perform the process 800 to operate subpixels within the display assembly. Embodiments may include different and/or additional operations, or perform the operations in different orders. Reference is made to the components of the subpixel 200 of FIG. 2 in the examples described with reference to the operations of FIG. 8.

[0055] A control circuit provides 810, via a switch transistor and a driving transistor between a high voltage source and an organic light emitting diode (OLED), a first current from the high voltage source to the OLED. For example, a first current can be provided 810 from ELVDD of the subpixel 200 to the OLED, where the first current travels through the driving transistor M_D and the switch transistor SW.

[0056] The control circuit provides 820, via a select transistor, a data signal from a data line to a gate of the driving transistor. Continuing the previous example, a data signal may be provided 820 from the data line DL to the gate of the driving transistor M_D via the select transistor SEL.

[0057] The control circuit charges 830 a capacitor in response to turning on the select transistor and the switch transistor. Continuing the previous example, the capacitor Cst1 of the subpixel 200 may be one of the capacitors described in the description of FIGS. 3-7, where the capacitor can be embodied by a non-uniform channel transistor. Furthermore, the capacitor Cst1 may be charged 830 in response to the select transistor SEL and the switch transistor SW being turned on.

[0058] The control circuit operates 840 the capacitor according to a non-uniform capacitance-voltage (C-V) curve to decrease a discharging time constant of the capacitor at a low brightness level of the OLED. Continuing the previous example, the capacitor Cst1 may be operated 840 according to a non-uniform C-V curve, or C-V profile, to decrease the discharging time constant of Cst1 at a low brightness level of the OLED. The capacitor may be operated 840 in any of the various C-V profiles described with respect to FIGS. 5-7. Some examples of the operation are described further with reference to operations 841, 842, and 843. Additionally, although the operations 841, 842, and 843 are shown in a sequence, not all of the operations 841, 842, or 843 may occur to operate 840 the capacitor. Similarly, the order of the sequence may vary when operating 840 the capacitor.

[0059] The control circuit operates 841 the capacitor at a first amount of channel inversion in response to providing a first gate-source voltage (Vgs) to a gate of the capacitor. For example, the capacitor Cst1 of the subpixel 200 may be the capacitor 400 of FIG. 4, which is one embodiment of a capacitor, that can operate according to a capacitance corresponding to the gate-source voltage 511 of FIG. 5. As depicted through the shading 501a, the capacitor 400 exhibits a full inversion at channel in response to an application of the voltage 511 at the gate of the capacitor 400. Thus, the capacitor Cst1 of the subpixel 200 may operate 841 at a first amount of channel inversion (e.g., a fully inverted channel) in response to a first Vgs (e.g., -0.1 V) applied at the gate.

[0060] The control circuit operates 842 the capacitor at a second amount of channel inversion in response to providing a second Vgs to the gate of the capacitor. Continuing the previous example, the capacitor Cst1 of the subpixel 200 can exhibit a partially inverted channel, as depicted through the shading 501b, in response to an application of the voltage 512 at the gate of the capacitor 400. Thus, the capacitor Cst1 of the subpixel 200 may operate 842 at a second

amount of channel inversion (e.g., a partially inverted channel) in response to a second Vgs (e.g., 0.2 V) applied at the gate.

[0061] The control circuit operates 843 the capacitor at a third amount of channel inversion in response to providing a third Vgs to the gate of the capacitor. Continuing the previous example, the capacitor Cst1 of the subpixel 200 can lack any channel inversion, as depicted through the lack of shading in the implant region in the embodiment of capacitor 400 that is drawn aligned with the voltage 514. The absence of an inverted channel may occur in response to an application of the voltage 514 at the gate of the capacitor 400. Thus, the capacitor Cst1 of the subpixel 200 may operate 843 at a third amount of channel inversion (e.g., no channel inversion) in response to a third Vgs (e.g., 0.7 V) applied at the gate.

[0062] FIG. 9 is a system 900 that includes a headset 905, in accordance with one or more embodiments. In some embodiments, the headset 905 may be the headset 100 of FIG. 1A or the headset 105 of FIG. 1B. The system 900 may operate in an artificial reality environment (e.g., a virtual reality environment, an augmented reality environment, a mixed reality environment, or some combination thereof). The system 900 shown by FIG. 9 includes the headset 905, an input/output (I/O) interface 910 that is coupled to a console 915, the network 920, and the mapping server 925. While FIG. 9 shows an example system 900 including one headset 905 and one I/O interface 910, in other embodiments any number of these components may be included in the system 900. For example, there may be multiple headsets each having an associated I/O interface 910, with each headset and I/O interface 910 communicating with the console 915. In alternative configurations, different and/or additional components may be included in the system 900. Additionally, functionality described in conjunction with one or more of the components shown in FIG. 9 may be distributed among the components in a different manner than described

in conjunction with FIG. 9 in some embodiments. For example, some or all of the functionality of the console 915 may be provided by the headset 905.

[0063] The headset 905 includes the display assembly 930, an optics block 935, one or more position sensors 940, and the DCA 945. Some embodiments of headset 905 have different components than those described in conjunction with FIG. 9. Additionally, the functionality provided by various components described in conjunction with FIG. 9 may be differently distributed among the components of the headset 905 in other embodiments, or be captured in separate assemblies remote from the headset 905.

[0064] The display assembly 930 displays content to the user in accordance with data received from the console 915. The display assembly 930 displays the content using one or more display elements (e.g., the display elements 120). A display element may be, e.g., an electronic display. In various embodiments, the display assembly 930 comprises a single display element or multiple display elements (e.g., a display for each eye of a user). Examples of an electronic display include: a liquid crystal display (LCD), an organic light emitting diode (OLED) display, an active-matrix organic light-emitting diode display (AMOLED), a waveguide display, some other display, or some combination thereof. Note in some embodiments, the display element 120 may also include some or all of the functionality of the optics block 935.

[0065] The optics block 935 may magnify image light received from the electronic display, corrects optical errors associated with the image light, and presents the corrected image light to one or both eyeboxes of the headset 905. In various embodiments, the optics block 935 includes one or more optical elements. Example optical elements included in the optics block 935 include: an aperture, a Fresnel lens, a convex lens, a concave lens, a filter, a reflecting surface, or any other suitable optical element that affects image light. Moreover, the optics block 935 may include combinations of different optical elements. In some embodiments, one or more of the

optical elements in the optics block 935 may have one or more coatings, such as partially reflective or anti-reflective coatings.

[0066] Magnification and focusing of the image light by the optics block 935 allows the electronic display to be physically smaller, weigh less, and consume less power than larger displays. Additionally, magnification may increase the field of view of the content presented by the electronic display. For example, the field of view of the displayed content is such that the displayed content is presented using almost all (e.g., approximately 110 degrees diagonal), and in some cases, all of the user's field of view. Additionally, in some embodiments, the amount of magnification may be adjusted by adding or removing optical elements.

[0067] In some embodiments, the optics block 935 may be designed to correct one or more types of optical error. Examples of optical error include barrel or pincushion distortion, longitudinal chromatic aberrations, or transverse chromatic aberrations. Other types of optical errors may further include spherical aberrations, chromatic aberrations, or errors due to the lens field curvature, astigmatisms, or any other type of optical error. In some embodiments, content provided to the electronic display for display is pre-distorted, and the optics block 935 corrects the distortion when it receives image light from the electronic display generated based on the content.

[0068] The position sensor 940 is an electronic device that generates data indicating a position of the headset 905. The position sensor 940 generates one or more measurement signals in response to motion of the headset 905. The position sensor 190 is an embodiment of the position sensor 940. Examples of a position sensor 940 include: one or more IMUs, one or more accelerometers, one or more gyroscopes, one or more magnetometers, another suitable type of sensor that detects motion, or some combination thereof. The position sensor 940 may include multiple accelerometers to measure translational motion (forward/back, up/down, left/right) and

multiple gyroscopes to measure rotational motion (e.g., pitch, yaw, roll). In some embodiments, an IMU rapidly samples the measurement signals and calculates the estimated position of the headset 905 from the sampled data. For example, the IMU integrates the measurement signals received from the accelerometers over time to estimate a velocity vector and integrates the velocity vector over time to determine an estimated position of a reference point on the headset 905. The reference point is a point that may be used to describe the position of the headset 905. While the reference point may generally be defined as a point in space, however, in practice the reference point is defined as a point within the headset 905.

[0069] The DCA 945 generates depth information for a portion of the local area. The DCA includes one or more imaging devices and a DCA controller. The DCA 945 may also include an illuminator. Operation and structure of the DCA 945 is described above with regard to FIG. 1A.

[0070] The audio system 950 provides audio content to a user of the headset 905. The audio system 950 may comprise one or acoustic sensors, one or more transducers, and an audio controller. The audio system 950 may provide spatialized audio content to the user. In some embodiments, the audio system 950 may request acoustic parameters from the mapping server 925 over the network 920. The acoustic parameters describe one or more acoustic properties (e.g., room impulse response, a reverberation time, a reverberation level, etc.) of the local area. The audio system 950 may provide information describing at least a portion of the local area from e.g., the DCA 945 and/or location information for the headset 905 from the position sensor 940. The audio system 950 may generate one or more sound filters using one or more of the acoustic parameters received from the mapping server 925, and use the sound filters to provide audio content to the user.

[0071] The I/O interface 910 is a device that allows a user to send action requests and receive responses from the console 915. An action request is a request to perform a particular action.

For example, an action request may be an instruction to start or end capture of image or video data, or an instruction to perform a particular action within an application. The I/O interface 910 may include one or more input devices. Example input devices include: a keyboard, a mouse, a game controller, or any other suitable device for receiving action requests and communicating the action requests to the console 915. An action request received by the I/O interface 910 is communicated to the console 915, which performs an action corresponding to the action request. In some embodiments, the I/O interface 910 includes an IMU that captures calibration data indicating an estimated position of the I/O interface 910 relative to an initial position of the I/O interface 910. In some embodiments, the I/O interface 910 may provide haptic feedback to the user in accordance with instructions received from the console 915. For example, haptic feedback is provided when an action request is received, or the console 915 communicates instructions to the I/O interface 910 causing the I/O interface 910 to generate haptic feedback when the console 915 performs an action.

[0072] The console 915 provides content to the headset 905 for processing in accordance with information received from one or more of: the DCA 945, the headset 905, and the I/O interface 910. In the example shown in FIG. 9, the console 915 includes an application store 955, a tracking module 960, and an engine 965. Some embodiments of the console 915 have different modules or components than those described in conjunction with FIG. 9. Similarly, the functions further described below may be distributed among components of the console 915 in a different manner than described in conjunction with FIG. 9. In some embodiments, the functionality discussed herein with respect to the console 915 may be implemented in the headset 905, or a remote system.

[0073] The application store 955 stores one or more applications for execution by the console 915. An application is a group of instructions, that when executed by a processor,

generates content for presentation to the user. Content generated by an application may be in response to inputs received from the user via movement of the headset 905 or the I/O interface 910. Examples of applications include: gaming applications, conferencing applications, video playback applications, or other suitable applications.

[0074] The tracking module 960 tracks movements of the headset 905 or of the I/O interface 910 using information from the DCA 945, the one or more position sensors 940, or some combination thereof. For example, the tracking module 960 determines a position of a reference point of the headset 905 in a mapping of a local area based on information from the headset 905. The tracking module 960 may also determine positions of an object or virtual object. Additionally, in some embodiments, the tracking module 960 may use portions of data indicating a position of the headset 905 from the position sensor 940 as well as representations of the local area from the DCA 945 to predict a future location of the headset 905. The tracking module 960 provides the estimated or predicted future position of the headset 905 or the I/O interface 910 to the engine 965.

[0075] The engine 965 executes applications and receives position information, acceleration information, velocity information, predicted future positions, or some combination thereof, of the headset 905 from the tracking module 960. Based on the received information, the engine 965 determines content to provide to the headset 905 for presentation to the user. For example, if the received information indicates that the user has looked to the left, the engine 965 generates content for the headset 905 that mirrors the user's movement in a virtual local area or in a local area augmenting the local area with additional content. Additionally, the engine 965 performs an action within an application executing on the console 915 in response to an action request received from the I/O interface 910 and provides feedback to the user that the action was

performed. The provided feedback may be visual or audible feedback via the headset 905 or haptic feedback via the I/O interface 910.

[0076] The network 920 couples the headset 905 and/or the console 915 to the mapping server 925. The network 920 may include any combination of local area and/or wide area networks using both wireless and/or wired communication systems. For example, the network 920 may include the Internet, as well as mobile telephone networks. In one embodiment, the network 920 uses standard communications technologies and/or protocols. Hence, the network 920 may include links using technologies such as Ethernet, 802.11, worldwide interoperability for microwave access (WiMAX), 2G/3G/4G mobile communications protocols, digital subscriber line (DSL), asynchronous transfer mode (ATM), InfiniBand, PCI Express Advanced Switching, etc. Similarly, the networking protocols used on the network 920 can include multiprotocol label switching (MPLS), the transmission control protocol/Internet protocol (TCP/IP), the User Datagram Protocol (UDP), the hypertext transport protocol (HTTP), the simple mail transfer protocol (SMTP), the file transfer protocol (FTP), etc. The data exchanged over the network 920 can be represented using technologies and/or formats including image data in binary form (e.g. Portable Network Graphics (PNG)), hypertext markup language (HTML), extensible markup language (XML), etc. In addition, all or some of links can be encrypted using conventional encryption technologies such as secure sockets layer (SSL), transport layer security (TLS), virtual private networks (VPNs), Internet Protocol security (IPsec), etc.

[0077] The mapping server 925 may include a database that stores a virtual model describing a plurality of spaces, wherein one location in the virtual model corresponds to a current configuration of a local area of the headset 905. The mapping server 925 receives, from the headset 905 via the network 920, information describing at least a portion of the local area and/or location information for the local area. The user may adjust privacy settings to allow or prevent

the headset 905 from transmitting information to the mapping server 925. The mapping server 925 determines, based on the received information and/or location information, a location in the virtual model that is associated with the local area of the headset 905. The mapping server 925 determines (e.g., retrieves) one or more acoustic parameters associated with the local area, based in part on the determined location in the virtual model and any acoustic parameters associated with the determined location. The mapping server 925 may transmit the location of the local area and any values of acoustic parameters associated with the local area to the headset 905.

[0078] One or more components of system 900 may contain a privacy module that stores one or more privacy settings for user data elements. The user data elements describe the user or the headset 905. For example, the user data elements may describe a physical characteristic of the user, an action performed by the user, a location of the user of the headset 905, a location of the headset 905, an HRTF for the user, etc. Privacy settings (or "access settings") for a user data element may be stored in any suitable manner, such as, for example, in association with the user data element, in an index on an authorization server, in another suitable manner, or any suitable combination thereof.

[0079] A privacy setting for a user data element specifies how the user data element (or particular information associated with the user data element) can be accessed, stored, or otherwise used (e.g., viewed, shared, modified, copied, executed, surfaced, or identified). In some embodiments, the privacy settings for a user data element may specify a "blocked list" of entities that may not access certain information associated with the user data element. The privacy settings associated with the user data element may specify any suitable granularity of permitted access or denial of access. For example, some entities may have permission to see that a specific user data element exists, some entities may have permission to view the content of the specific user data element, and some entities may have permission to modify the specific user

data element. The privacy settings may allow the user to allow other entities to access or store user data elements for a finite period of time.

[0080] The privacy settings may allow a user to specify one or more geographic locations from which user data elements can be accessed. Access or denial of access to the user data elements may depend on the geographic location of an entity who is attempting to access the user data elements. For example, the user may allow access to a user data element and specify that the user data element is accessible to an entity only while the user is in a particular location. If the user leaves the particular location, the user data element may no longer be accessible to the entity. As another example, the user may specify that a user data element is accessible only to entities within a threshold distance from the user, such as another user of a headset within the same local area as the user. If the user subsequently changes location, the entity with access to the user data element may lose access, while a new group of entities may gain access as they come within the threshold distance of the user.

[0081] The system 900 may include one or more authorization/privacy servers for enforcing privacy settings. A request from an entity for a particular user data element may identify the entity associated with the request and the user data element may be sent only to the entity if the authorization server determines that the entity is authorized to access the user data element based on the privacy settings associated with the user data element. If the requesting entity is not authorized to access the user data element, the authorization server may prevent the requested user data element from being retrieved or may prevent the requested user data element from being sent to the entity. Although this disclosure describes enforcing privacy settings in a particular manner, this disclosure contemplates enforcing privacy settings in any suitable manner.

Additional Configuration Information

[0082] The foregoing description of the embodiments has been presented for illustration; it is not intended to be exhaustive or to limit the patent rights to the precise forms disclosed. Persons skilled in the relevant art can appreciate that many modifications and variations are possible considering the above disclosure.

[0083] Some portions of this description describe the embodiments in terms of algorithms and symbolic representations of operations on information. These algorithmic descriptions and representations are commonly used by those skilled in the data processing arts to convey the substance of their work effectively to others skilled in the art. These operations, while described functionally, computationally, or logically, are understood to be implemented by computer programs or equivalent electrical circuits, microcode, or the like. Furthermore, it has also proven convenient at times, to refer to these arrangements of operations as modules, without loss of generality. The described operations and their associated modules may be embodied in software, firmware, hardware, or any combinations thereof.

[0084] Any of the steps, operations, or processes described herein may be performed or implemented with one or more hardware or software modules, alone or in combination with other devices. In one embodiment, a software module is implemented with a computer program product comprising a computer-readable medium containing computer program code, which can be executed by a computer processor for performing any or all the steps, operations, or processes described.

[0085] Embodiments may also relate to an apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, and/or it may comprise a general-purpose computing device selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a non-transitory, tangible

computer readable storage medium, or any type of media suitable for storing electronic instructions, which may be coupled to a computer system bus. Furthermore, any computing systems referred to in the specification may include a single processor or may be architectures employing multiple processor designs for increased computing capability.

[0086] Embodiments may also relate to a product that is produced by a computing process described herein. Such a product may comprise information resulting from a computing process, where the information is stored on a non-transitory, tangible computer readable storage medium and may include any embodiment of a computer program product or other data combination described herein.

[0087] Finally, the language used in the specification has been principally selected for readability and instructional purposes, and it may not have been selected to delineate or circumscribe the patent rights. It is therefore intended that the scope of the patent rights be limited not by this detailed description, but rather by any claims that issue on an application based hereon. Accordingly, the disclosure of the embodiments is intended to be illustrative, but not limiting, of the scope of the patent rights, which is set forth in the following claims.

What is claimed is:

1. A pixel of a display device comprising:

a light emitting element coupled to a low voltage source;

a select transistor selectively passing through pixel data from a data line;

a switch transistor configured to selectively connect to a high voltage source;

a driving transistor having a drain coupled to the light emitting element, a gate coupled to the select transistor to receive the pixel data, and a source coupled to the switch transistor, the driving transistor configured to perform threshold voltage compensation according to adjustments of a current received at the drain of the driving transistor; and

a capacitor comprising:

a gate coupled to the source of the driving transistor,

a source coupled to the gate of the driving transistor, and

a non-uniform channel region, wherein a capacitance of the capacitor increases with a decrease of a gate-source voltage applied to the gate and decreases with an increase of the gate-source voltage applied to the gate.

2. The pixel of claim 1, wherein the non-uniform channel region comprises a threshold voltage implant region configured to generate a threshold voltage profile characterized by a plurality of threshold voltages along the non-uniform channel region.

3. The pixel of claim 2, wherein the threshold voltage implant region comprises a plurality of threshold voltage implants.

4. The pixel of claim 2, wherein the plurality of threshold voltages are formed using annealing and diffusion of one or more threshold voltage implants.

5. The pixel of claim 2, wherein the threshold voltage implant region comprises an implant having a non-zero length that is at most half a length of the substrate of the capacitor.

6. The pixel of claim 1, wherein a threshold voltage profile of the non-uniform channel region comprises a maximum threshold voltage at a first end of the non-uniform channel region and a minimum threshold voltage at a second end of the non-uniform channel region.

7. The pixel of claim 1, wherein a plurality of shapes of the non-uniform channel region correspond to a plurality of ratios of a maximum capacitance to a minimum capacitance of the capacitor.

8. The pixel of claim 1, wherein a decreased capacitance adjusts the current flowing from the drain of the driving transistor to the light emitting element to enable the threshold voltage compensation of the driving transistor.

9. A capacitor comprising:

a gate coupled to a source of a driving transistor configured to perform threshold voltage compensation according to adjustments of a current received at a drain of the driving transistor;

a source coupled to a gate of the driving transistor; and

a non-uniform channel region, wherein a capacitance of the capacitor increases with a decrease of a gate-source voltage applied to the gate and decreases with an increase of the gate-source voltage applied to the gate.

10. The capacitor of claim 9, wherein the non-uniform channel region comprises a threshold voltage implant region configured to generate a threshold voltage profile characterized by a plurality of threshold voltages along the non-uniform channel region.

11. The capacitor of claim 10, wherein the threshold voltage implant region comprises a plurality of threshold voltage implants.

12. The capacitor of claim 10, wherein the plurality of threshold voltages are formed using annealing and diffusion of one or more threshold voltage implants.

13. The capacitor of claim 10, wherein the threshold voltage implant region comprises an implant having a non-zero length that is at most half a length of the substrate of the MOS capacitor.

14. The capacitor of claim 9, wherein a threshold voltage profile of the non-uniform channel region comprises a maximum threshold voltage at a first end of the non-uniform channel region and a minimum threshold voltage at a second end of the non-uniform channel region.

15. The capacitor of claim 9, wherein a plurality of shapes of the non-uniform channel region correspond to a plurality of ratios of a maximum capacitance to a minimum capacitance of the capacitor.

16. The capacitor of claim 9, wherein a decreased capacitance adjusts the current flowing from the drain of the driving transistor to a light emitting element to enable the threshold voltage compensation of the driving transistor.

17. A method for operating a pixel, the method comprising:

providing, via a switch transistor and a driving transistor between a high voltage source and a light emitting element, a first current from the high voltage source to the light emitting element;

providing, via a select transistor, a data signal from a data line to a gate of the driving transistor;

charging a capacitor in response to turning on the select transistor and the switch transistor; and

operating the capacitor according to a non-uniform capacitance-voltage curve to decrease a discharging time constant of the capacitor at a low brightness level of the light emitting element, wherein operating the capacitor comprises:

in response to providing a first gate-source voltage to a gate of the capacitor, operating the capacitor at a first amount of channel inversion,

in response to providing a second gate-source voltage to the gate of the capacitor, operating the capacitor at a second amount of channel inversion, wherein the second amount is less than the first amount, and

in response to providing a third gate-source voltage to the gate of the capacitor, operating the capacitor at a third amount of channel inversion, wherein the third amount is less than the second amount.

18. The method of claim 17, wherein the first amount corresponds to a whole channel inversion.

19. The method of claim 17, wherein the third amount corresponds to an absence of channel inversion.

20. The method of claim 17, wherein the decreased discharging time constant adjusts current flowing from the drain of the driving transistor to the light emitting element during a compensation of a threshold voltage of the driving transistor.

ABSTRACT OF THE DISCLOSURE

Embodiments relate to a display device including pixels that compensate a threshold voltage of a driving transistor through decreasing the discharge time of a capacitor coupled to the driving transistor. The capacitor may be embodied as a metal-oxide-semiconductor (MOS) transistor. The capacitor may include a non-uniform channel region having a capacitance that increases with a decrease of a gate-source voltage applied to the capacitor and decrease with an increase of the gate-source voltage applied to the capacitor.

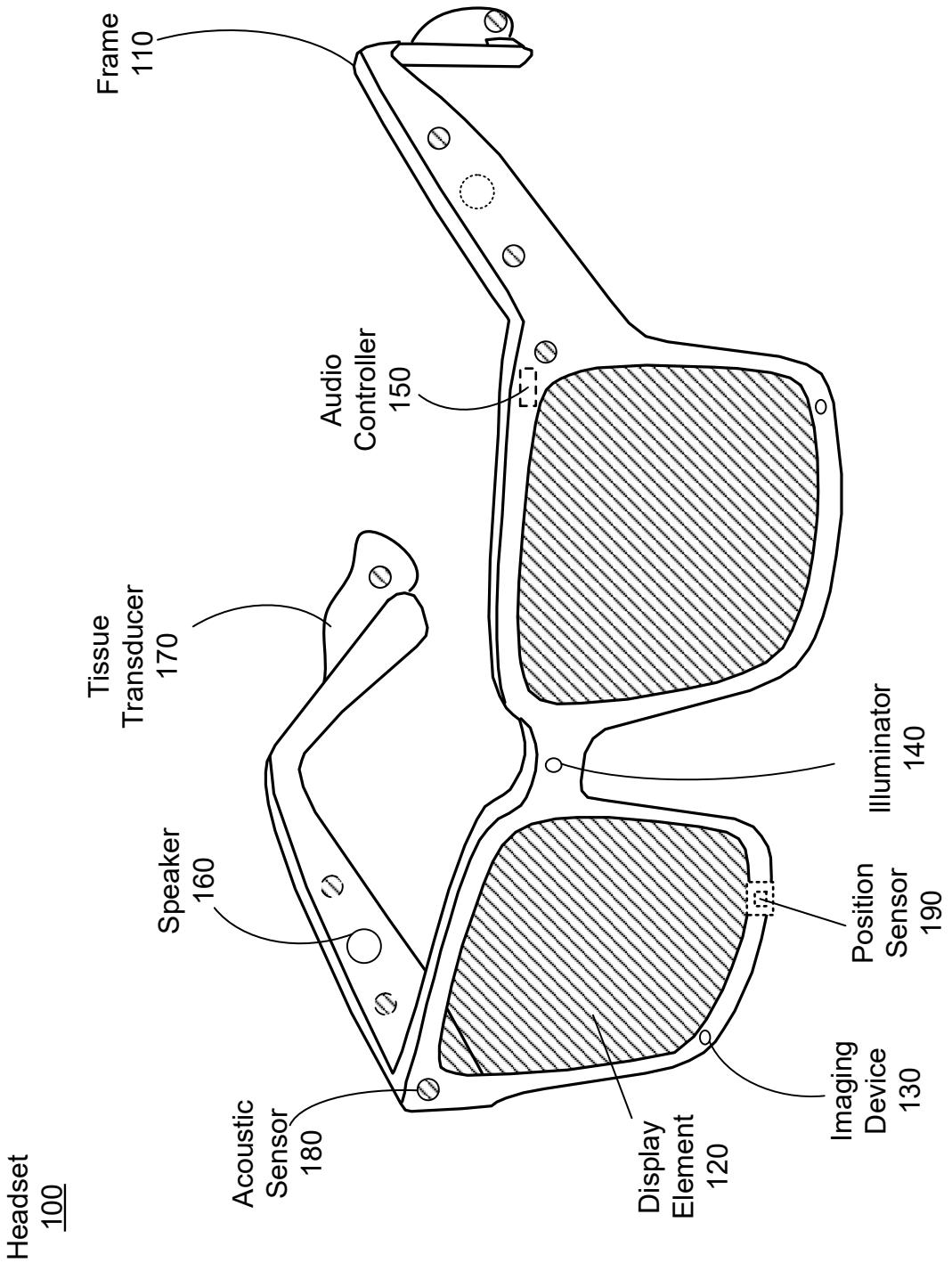
Headset
100
Frame
110
Audio
Controller
150
Tissue
Transducer
170
Speaker
160
Acoustic
Sensor
180
Display
Element
120
Imaging
Device
130
Position
Sensor
190
Illuminator
140

FIG. 1A

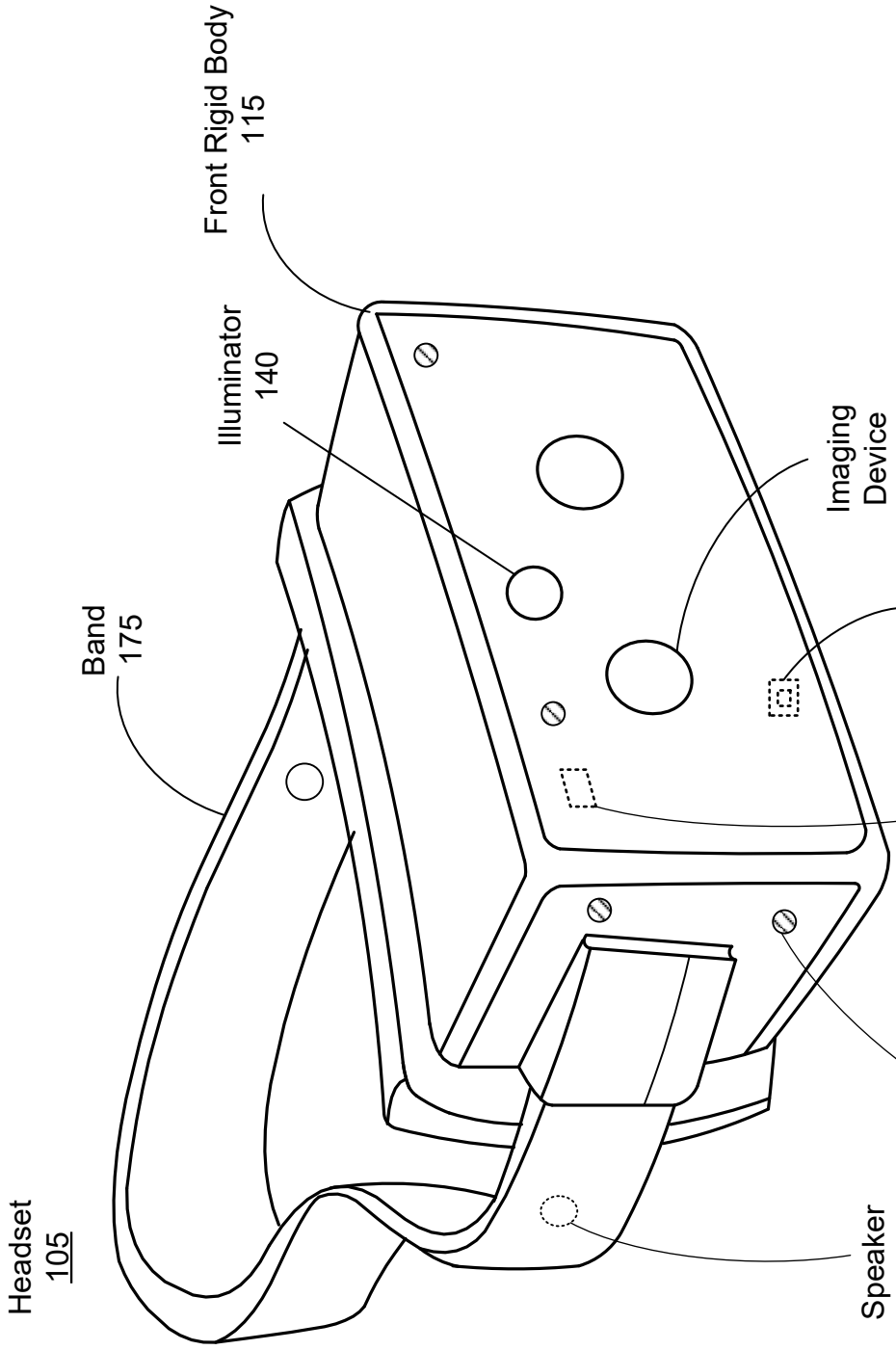
Front Rigid Body
115
Illuminator
140
Band
175
Imaging
Device
130
Position
Sensor
190
Audio
Controller
150
Acoustic Sensor
180
Speaker
160
Headset
105

FIG. 1B

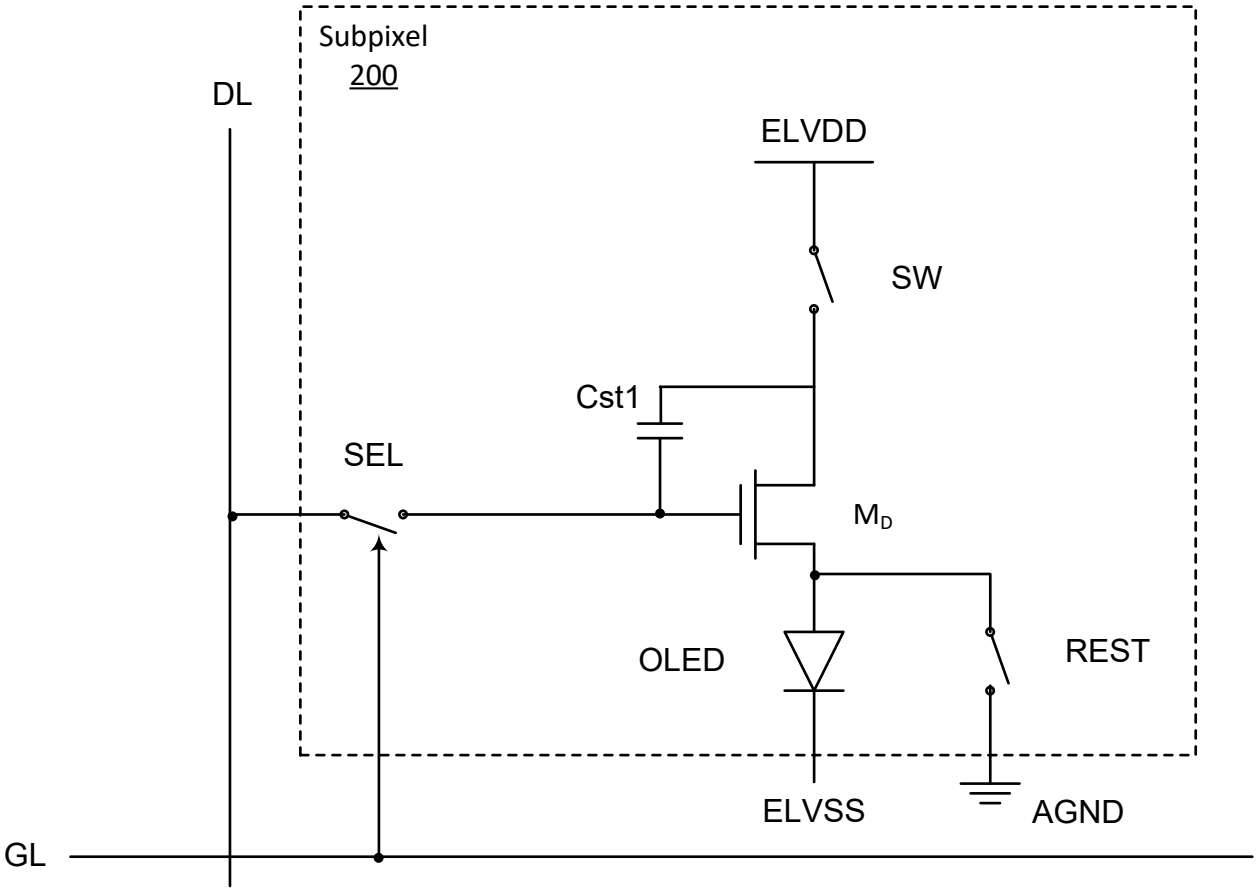

FIG. 2

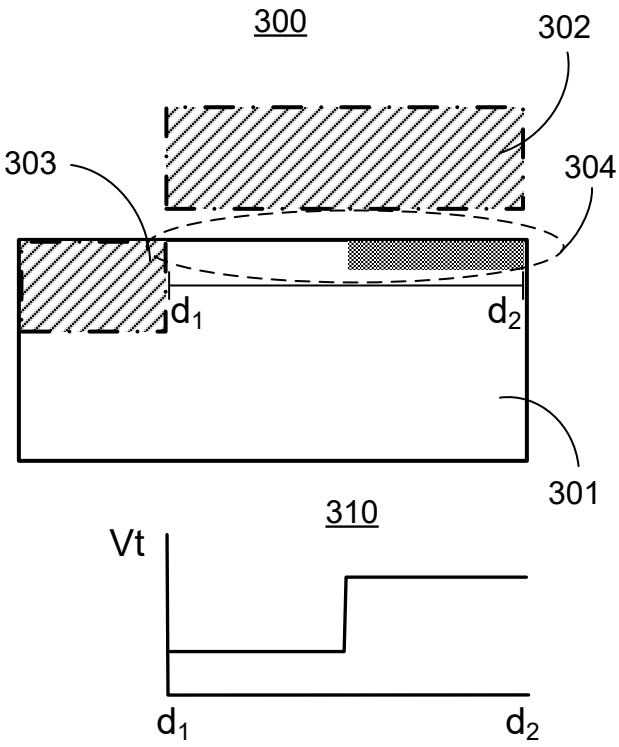

FIG. 3

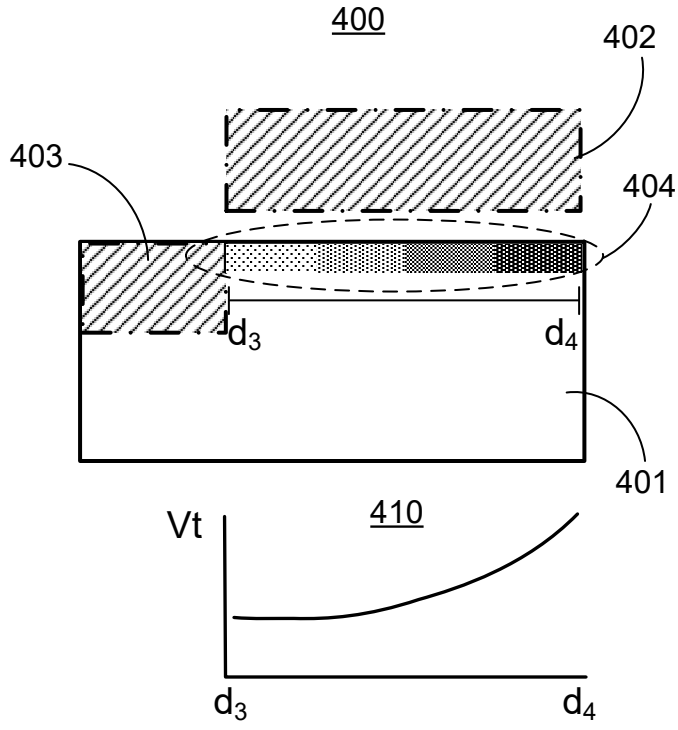

FIG. 4

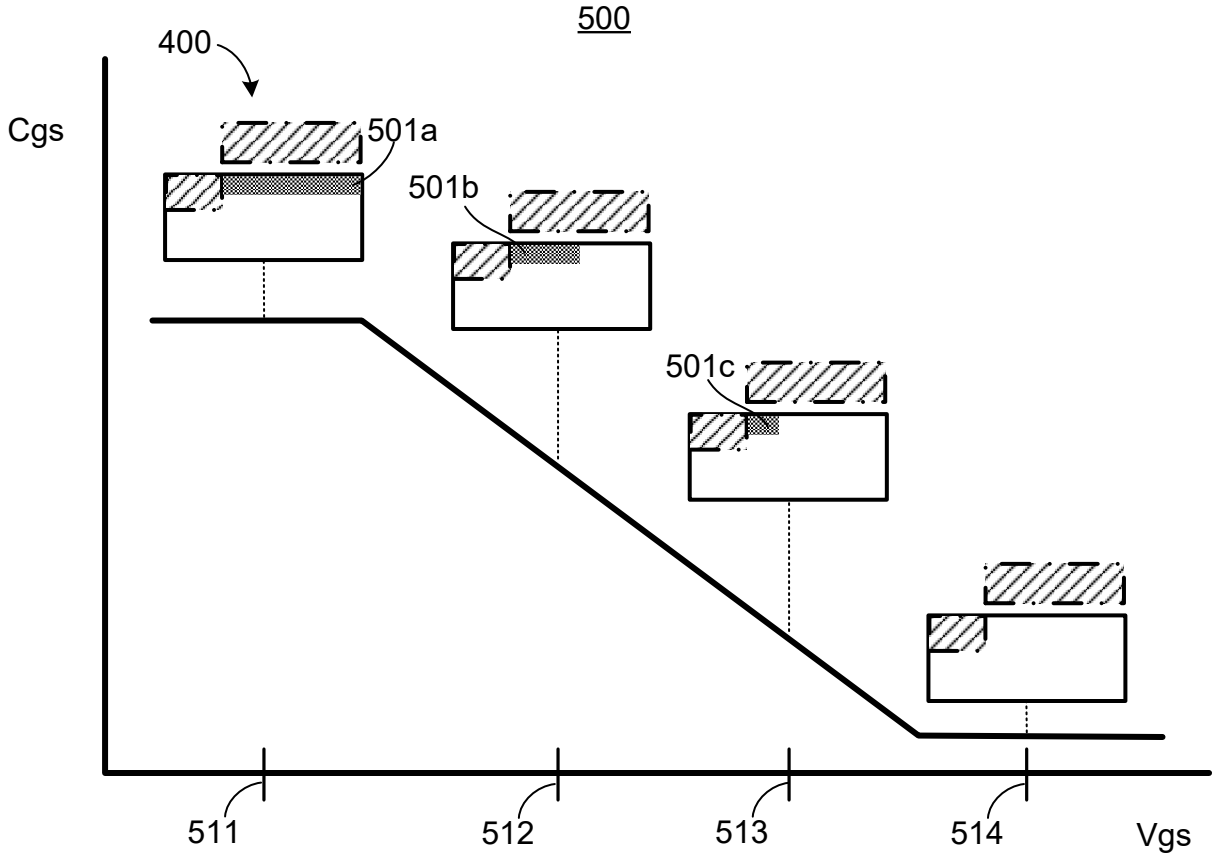

FIG. 5

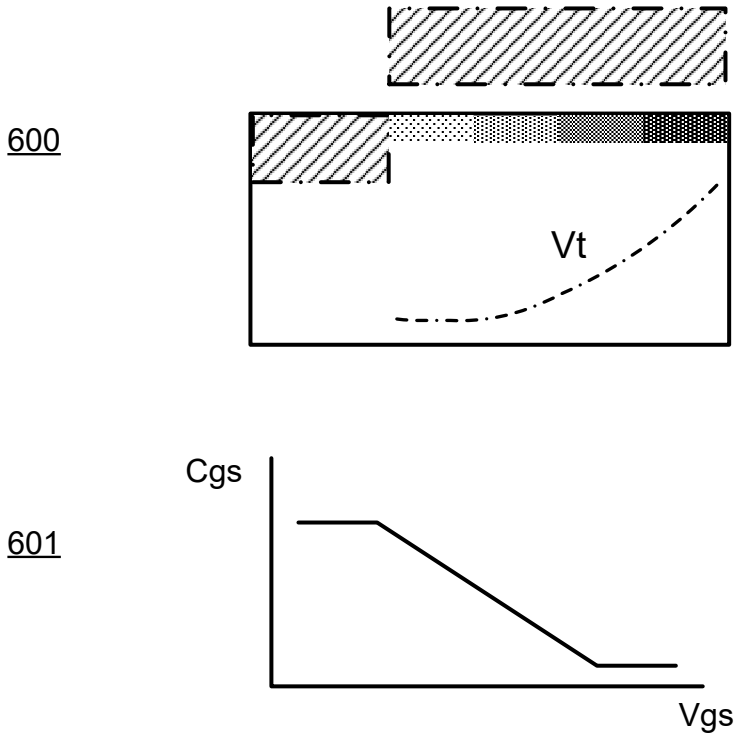

FIG. 6A

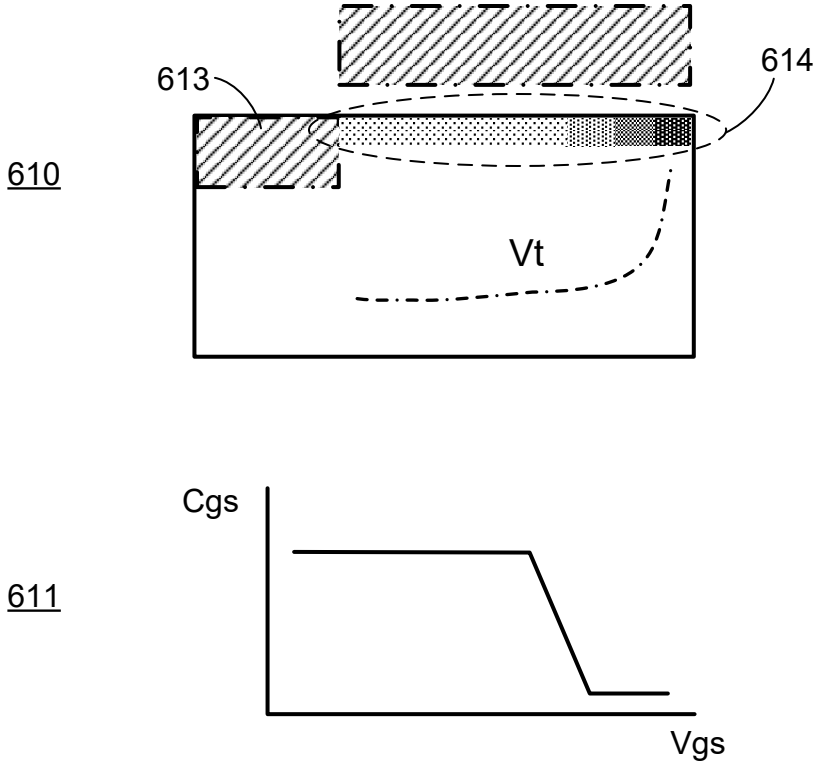

FIG. 6B

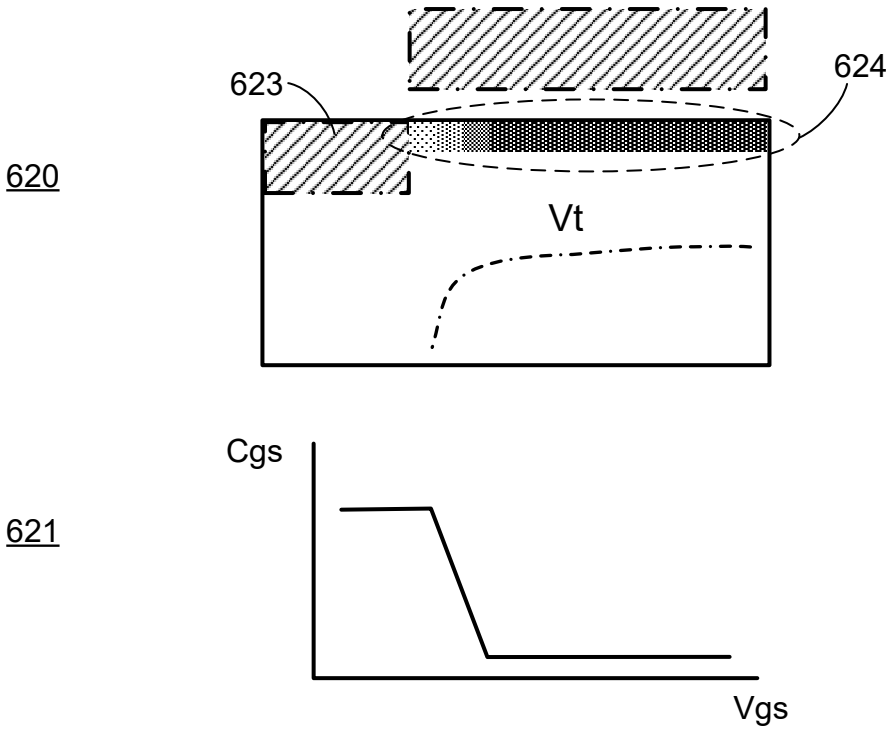

FIG. 6C

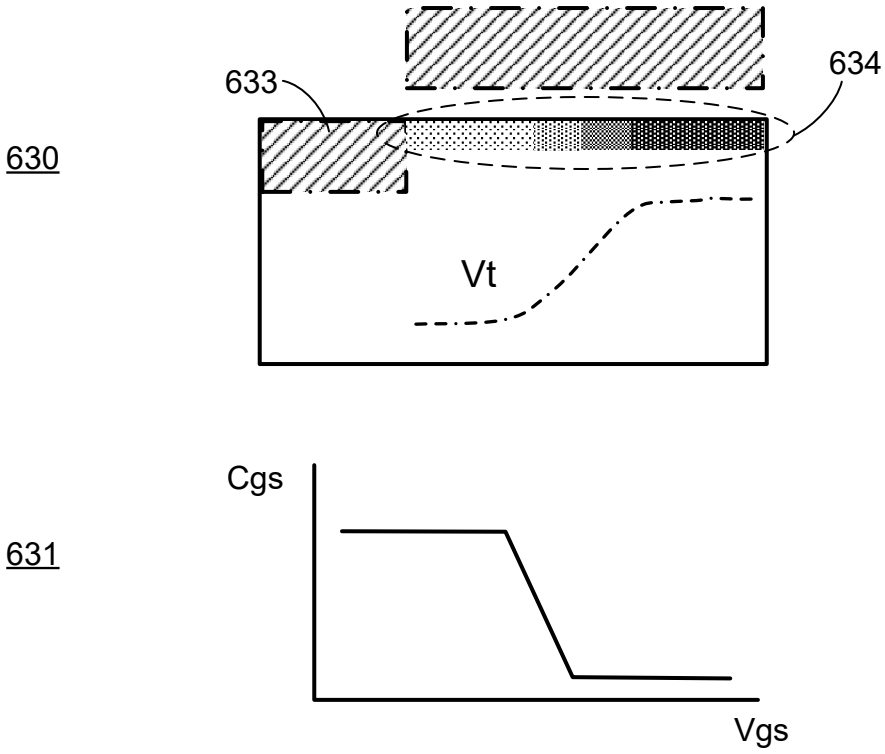

FIG. 6D

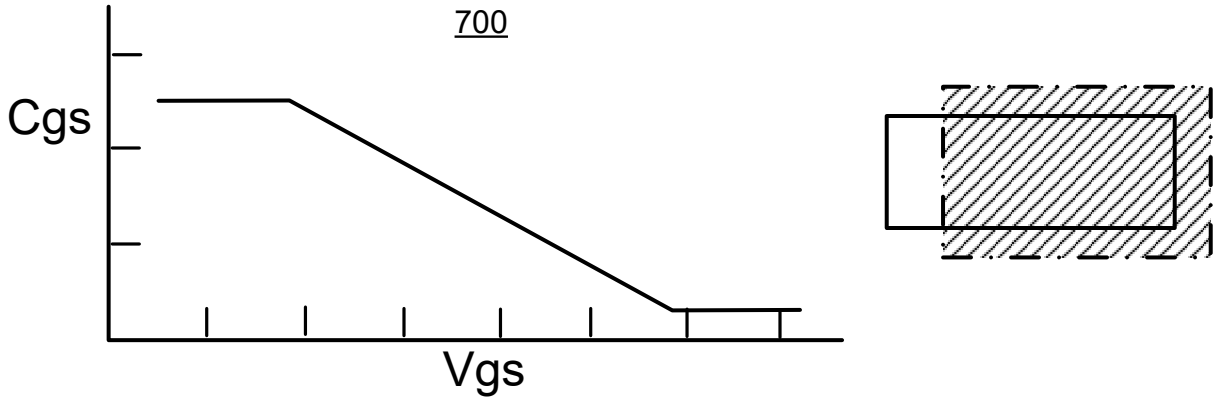

FIG. 7A

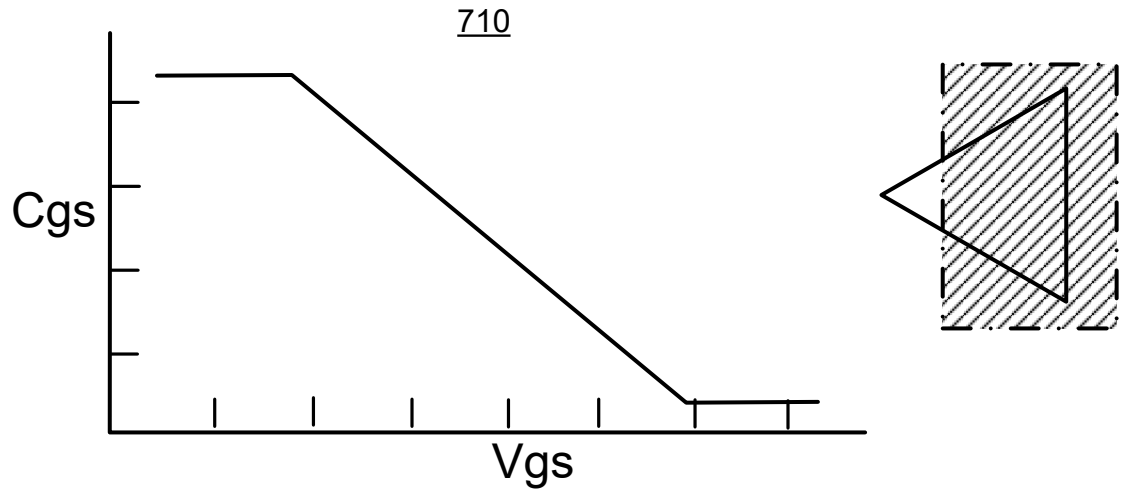

FIG. 7B

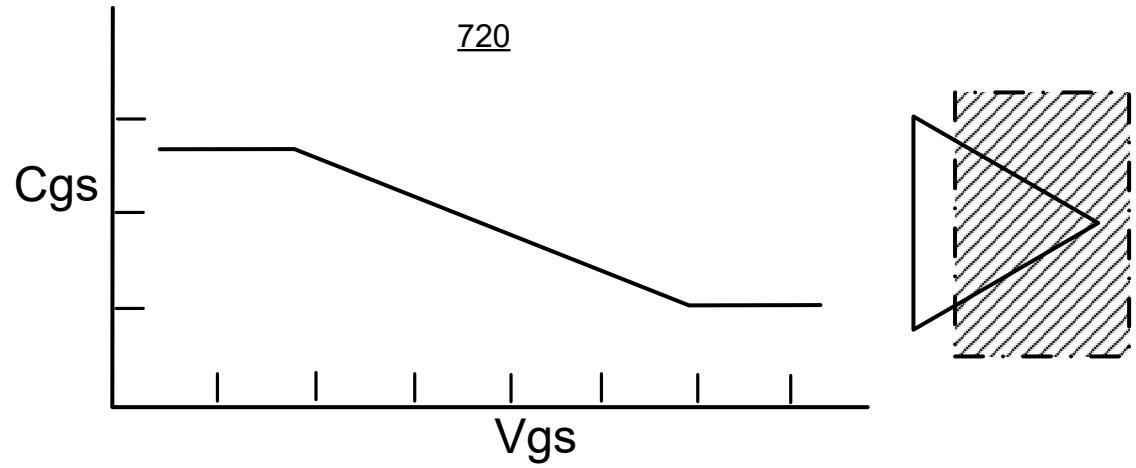

FIG. 7C

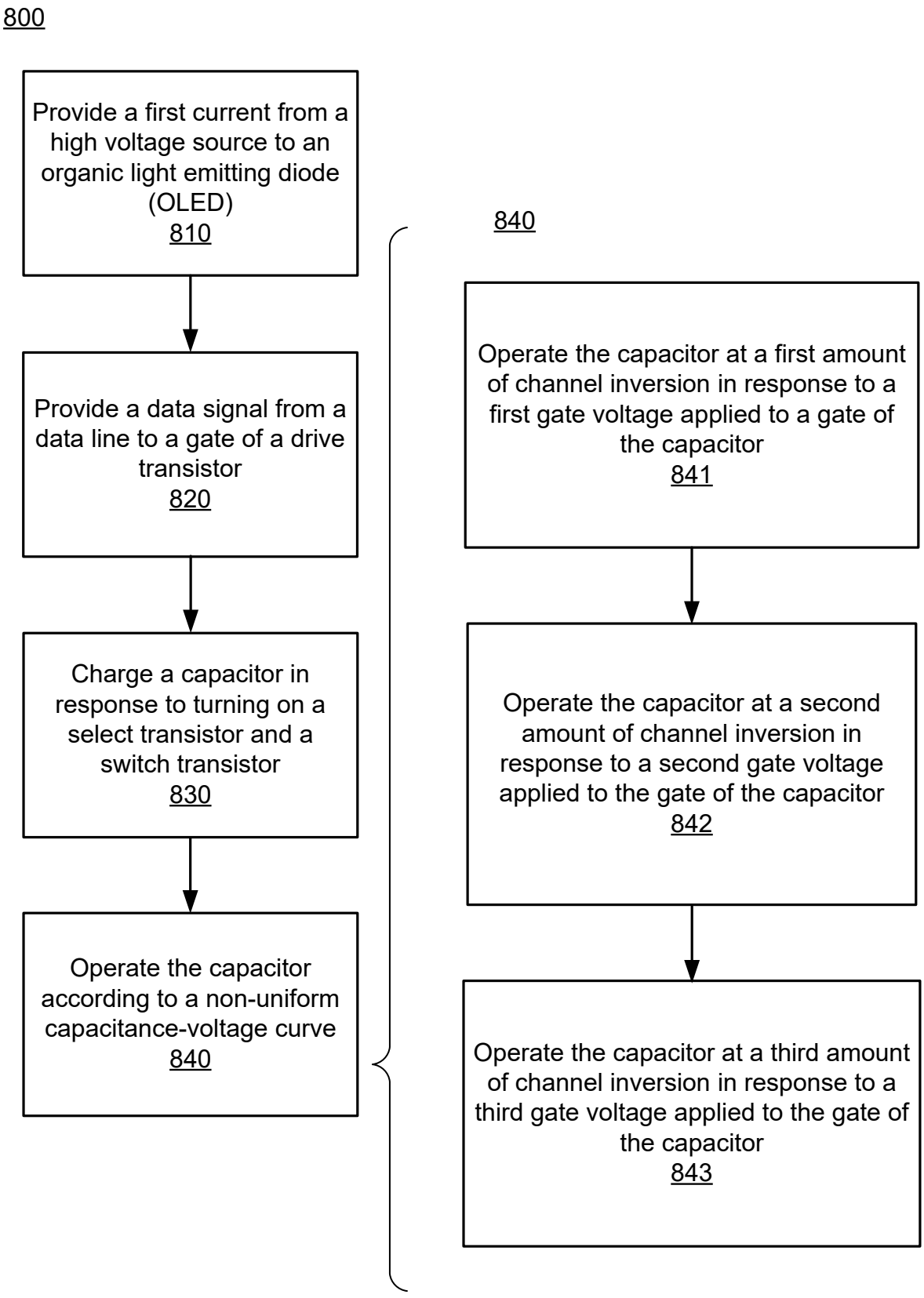
800
Provide a first current from a high voltage source to an organic light emitting diode (OLED)
810
Provide a data signal from a data line to a gate of a drive transistor
820
Charge a capacitor in response to turning on a select transistor and a switch transistor
830
Operate the capacitor according to a non-uniform capacitance-voltage curve
840
840
Operate the capacitor at a first amount of channel inversion in response to a first gate voltage applied to a gate of the capacitor
841
Operate the capacitor at a second amount of channel inversion in response to a second gate voltage applied to the gate of the capacitor
842
Operate the capacitor at a third amount of channel inversion in response to a third gate voltage applied to the gate of the capacitor
843

FIG. 8

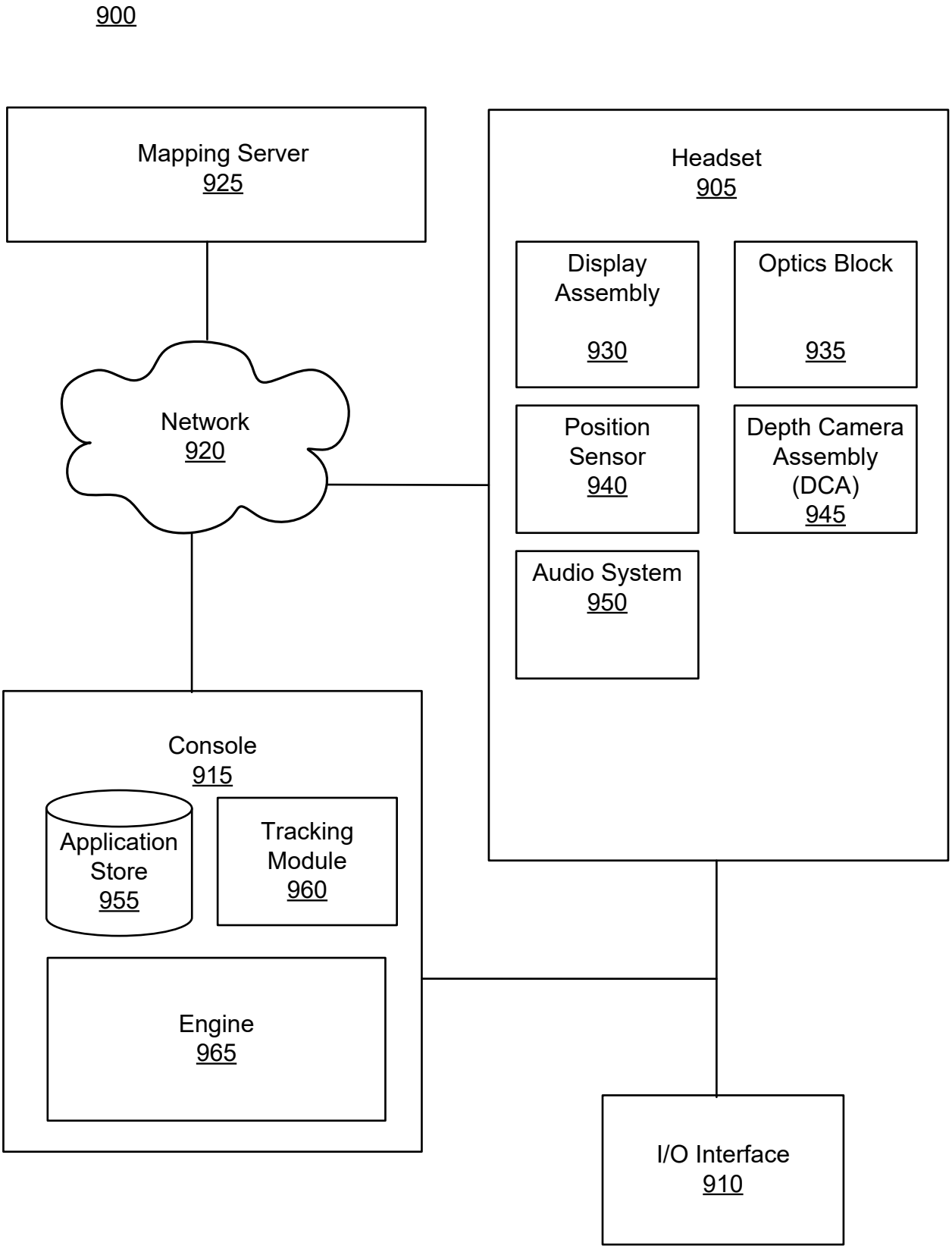
900
Mapping Server
925
Network
920
Headset
905
Display Assembly
930
Optics Block
935
Position Sensor
940
Depth Camera Assembly (DCA)
945
Audio System
950
Console
915
Application Store
955
Tracking Module
960
Engine
965
I/O Interface
910

FIG. 9