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INTERCONNECT STRUCTURE TO IMPROVE CHIP SIGNAL INTEGRITY AND MECHANICAL RELIABILITY

Yuqing (Bryce) Zhu

Wenbin Ma

Mike Sapozhnikov

Dewen Xu

Mingjian Gao

See next page for additional authors

Inventor(s)
Yuqing (Bryce) Zhu, Wenbin Ma, Mike Sapozhnikov, Dewen Xu, Mingjian Gao, Weiying Ding, and Xinghai (Sean) Tang

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ABSTRACT

Techniques are presented herein that support a novel chip interconnect structure, encompassing convex- and concave-shaped copper joint pillars, for connecting a chip (that follows the Optical Internetworking Forum (OIF) next generation (NG) common electrical input/output (CEI)-224 gigabit per second (G) framework) to a printed circuit board (PCB). Aspects of the presented techniques provide excellent signal integrity (SI) performance (including return loss, insertion loss, and impedance discontinuity) in support of, for example, a 102.4 terabit (T) per second switch comprising, among other things, an application-specific integrated circuit (ASIC) having 512 lanes of 224G Serializer/Deserializer (SerDes) capacity. Under further aspects of the techniques, mechanical performance and long-term reliability are significantly improved.

DETAILED DESCRIPTION

In support of different chip packaging arrangements (such as a pin grid array (PGA), a land grid array (LGA), and a ball grid array (BGA)), a great many chip-to-printed circuit board (PCB) interconnection mechanisms and materials have been introduced. As chip packages have become larger and Serializer/Deserializer (SerDes) data rates have quickly increased, the overall performance of a system tends to be dictated by a chip-to-PCB assembly approach, mechanical reliability, and signal integrity (SI).

One of the most widely used chip-to-PCB interconnection materials is lead-free solder. However, during the solder reflowing process chip warpage and other joints defects (including cracking, shorting, etc.) will impact system reliability and SI. In addition to such soldering issues, the spherical shape of a BGA's 'solder ball' may contribute an extra

capacitive effect and therefore negatively impact SI performance (specifically a return loss and an impedance discontinuity).

As an example, a 102.4 terabit (T) per second switch may comprise, among other things, a high-density application-specific integrated circuit (ASIC). Such a circuit may encompass a large number of SerDes functional blocks and may follow the Optical Internetworking Forum (OIF) next generation (NG) common electrical input/output (CEI)-224 gigabit per second (G) framework. Such a switch may have 512 lanes of 224G SerDes capacity and a power consumption of more than 1,200 watts.

The package (PKG) size of a chip as described above will exceed 95x95 millimeters (mm) and incorporate a lower pitch (of approximately 0.9mm) due to manufacturing concerns regarding solderability and coplanarity. It has been observed that the impedance drop and return loss (RL) are poor at each solder section due to an additional capacitive effect that arises from the spherical solder ball.

Consequently, achieving acceptable SI performance in a 112G or 224G system becomes very challenging. Additionally, as a chip's PKG size increases beyond 75x75mm soldering and reliability become primary concerns and substrate warpage may become severe during the assembly process.

The characteristics of a current BGA solder ball structure may be illustrated through a simulation model, elements of which are depicted in Figure 1, below.

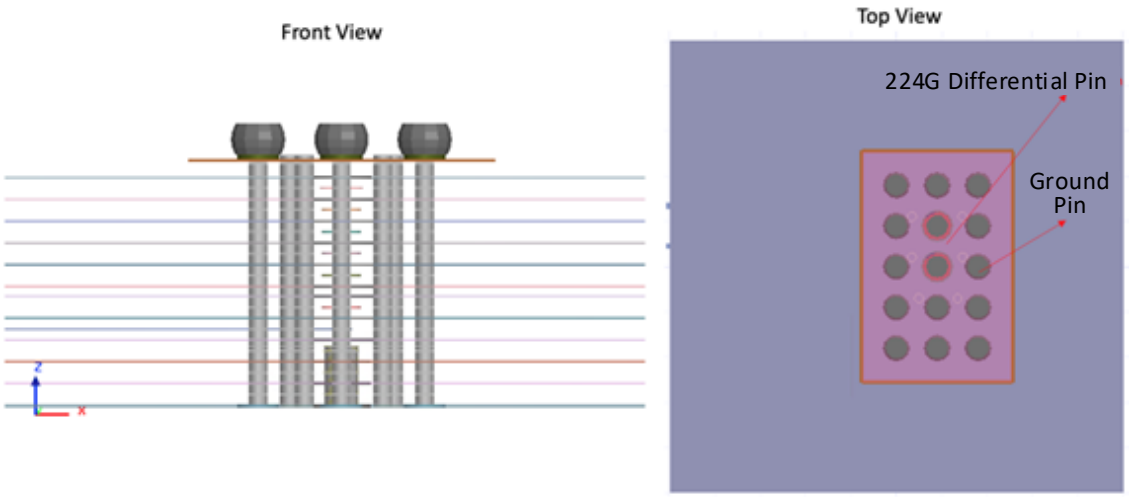

Figure 1: Front and Top View of Simulation Model

The left-hand side of the model that is shown in Figure 1, above, presents a front view of a mounting arrangement that employs a BGA solder ball structure while the right-hand side of the model presents a top view of such an arrangement. Figures 2, 3, and 4 (all below) graphically depict different SI performance simulation results for the solder ball model from Figure 1, above.

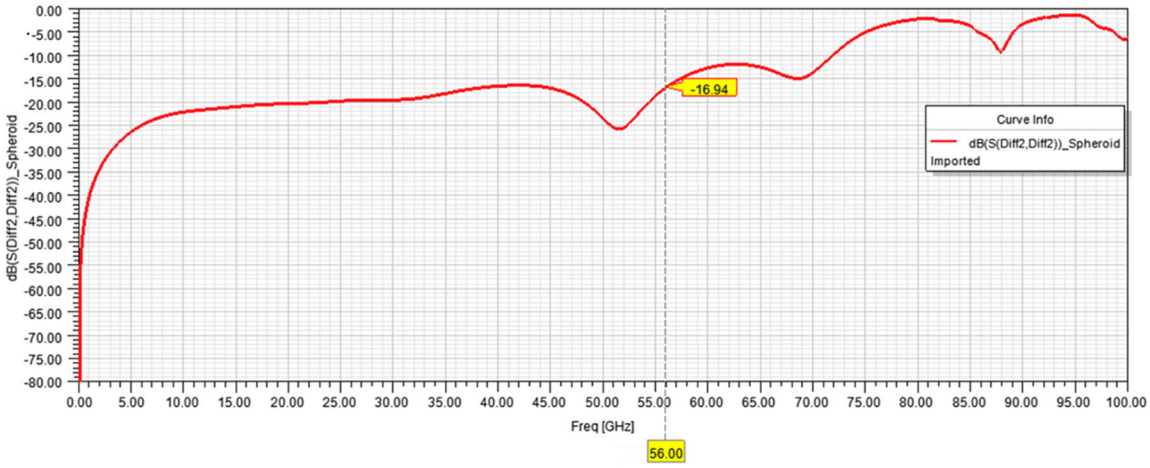

Figure 2: SI Performance Simulation Results – Return Loss

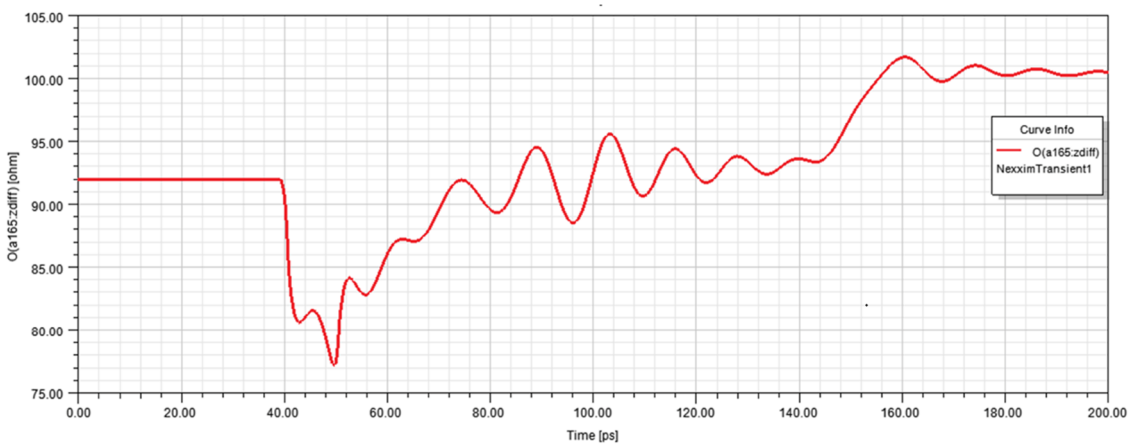

Figure 3: SI Performance Simulation Results –Time Domain Reflectometry

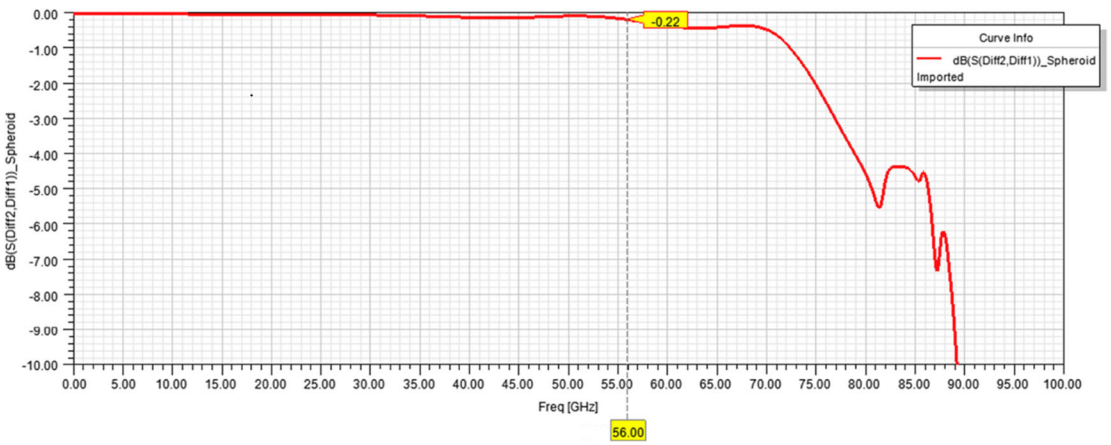

Figure 4: SI Performance Simulation Results – Insertion Loss

Techniques are presented herein that support a novel interconnection joint for a flip chip BGA (FCBGA). Under the presented techniques, the BGA pads of a PCB and a PKG may be copper plated and then successively shaped (through drilling and other treatments) to form convex and concave bodies. A joint that is formed by the mating of such bodies may take the shape of cylinder after the PKG is mounted to the PCB. This new joint structure can minimize a capacitive effect and achieve a better electrical and mechanical performance compared to the current assembling technology (involving, for example, a LGA or a BGA packaging arrangement).

The presented techniques may be further understood through an example that illustrates various of the steps that may occur during the fabrication of the above-described convex and concave bodies (which may mimic a rivet connection). Under the instant example, a first step encompasses the electroplating of all of a PCB's BGA pads to grow copper (Cu) pillars, as depicted in Figure 5, below.

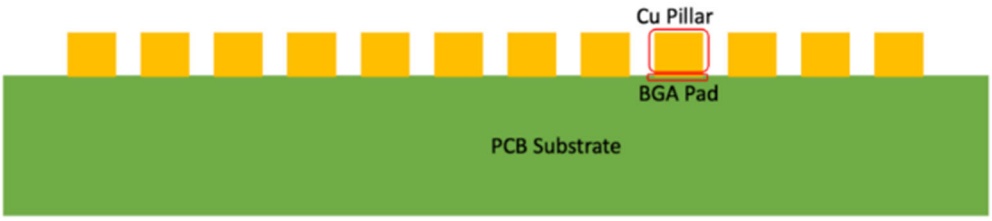

Figure 5: Step 1 – Electroplating PCB BGA Pads

During a second step, an electroplated Cu pillar may be drilled as shown in Figure 6, below, and then under a third step a drilled Cu pillar may be cleaned as depicted in Figure 7, below.

Figure 6: Step 2 – Drilling PCB Cu Pillar

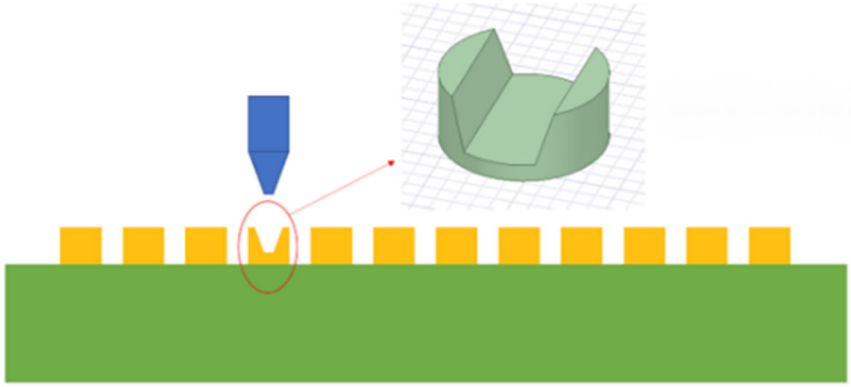

Figure 7: Step 3 – Cleaning PCB Cu Pillar

The emphasized portion of Figure 7, above, provides a three-dimensional view of a shaped PCB Cu pillar, highlighting the previously noted concave form.

A fourth step encompasses repeating each of the preceding two steps (i.e., the second and third steps) for the PCB's other Cu pillars. Figure 8, below, depicts the PCB's pillars at the end of this step.

Figure 8: Step 4 – Shaped PCB Cu Pillars

A fifth step encompasses the electroplating of each of a PKG's BGA pads to grow Cu pillars, as depicted in Figure 9, below.

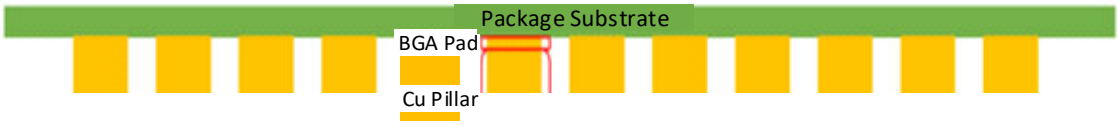

Figure 9: Step 5 – Electroplating PKG BGA Pads

A sixth step encompasses drilling the right side of a PKG's Cu pillar while a seventh step encompasses cleaning following such a drilling operation, as depicted in Figures 10 and 11, both below.

Figure 10: Step 6 – Drilling Right Side of PKG Cu Pillar

Figure 11: Step 7 – Cleaning PKG Cu Pillar

An eighth step encompasses drilling the left side of a PKG's Cu pillar while a ninth step encompasses cleaning after such a drilling operation, as depicted in Figures 12 and 13, both below.

Figure 12: Step 8 – Drilling Left Side of PKG Cu Pillar

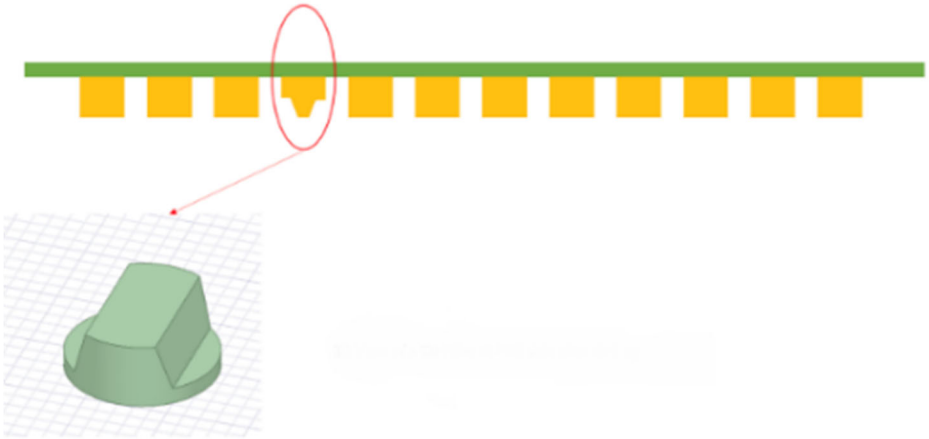

Figure 13: Step 9 – Cleaning PKG Cu Pillar

The emphasized portion of Figure 13, above, provides a three-dimensional view of a shaped PKG Cu pillar, highlighting the previously noted convex form.

A tenth step encompasses repeating each of the preceding four steps (i.e., the sixth step through the ninth step) for the PKG's other Cu pillars. Figure 14, below, illustrates the PKG's pillars at the end of this step.

Figure 14: Step 10 – Shaped PKG Cu Pillars

An eleventh step encompasses the application of solder paste to each of the PCB's concave shaped Cu pillars and then the placement of the PKG and the PCB so that all of the shaped pillars are aligned, as depicted in Figure 15, below.

Figure 15: Step 11 – Alignment of Shaped Cu Pillars

A twelfth, and final, step encompasses the completion of a surface mount process and the application of heat to achieve solder reflow, as shown in Figure 16, below.

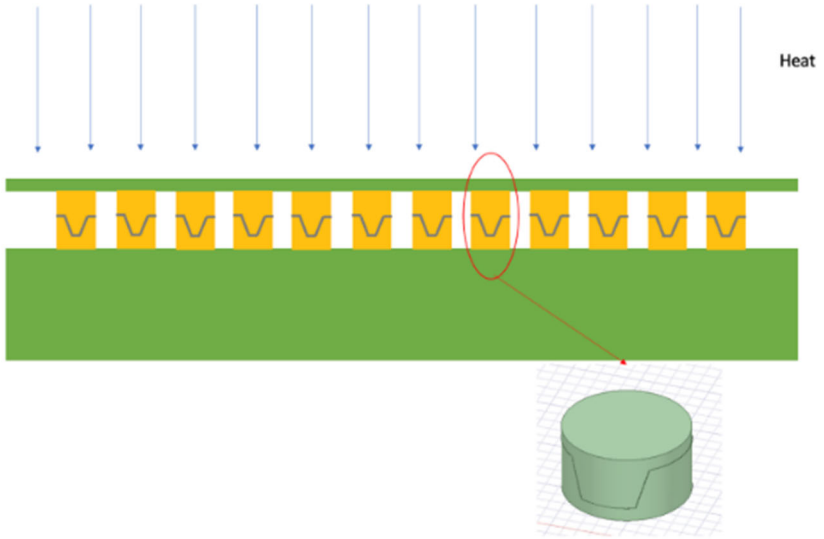

Figure 16: Step 12 – Completion

The emphasized portion of Figure 16, above, provides a three-dimensional view of a joined PCB Cu pillar and PKG Cu pillar, highlighting the precise, cylinder-like mating of the above-described concave and convex pillar shapes.

In the above illustrative example, the PCB's pads were processed to yield a concave shape (as depicted by the different views of Figure 17, below) and the PKG's pads were processed to yield a convex shape.

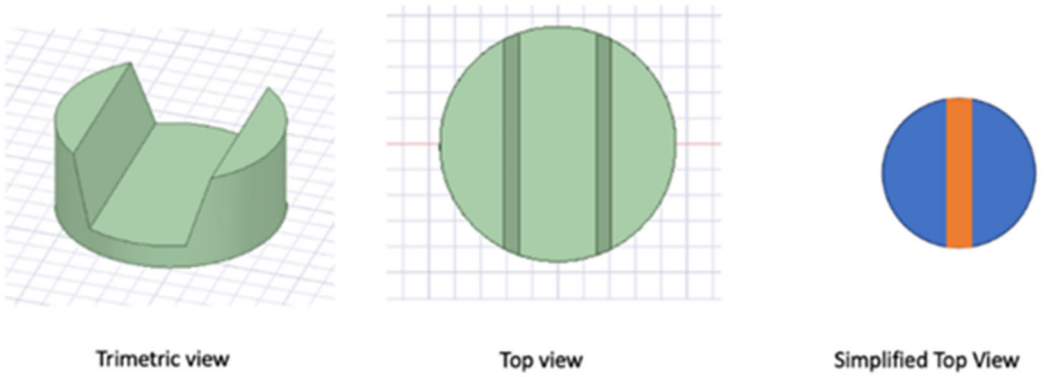

Figure 17: PCB Pad Concave Shape

It is important to note that alternative shape selections are possible under the presented techniques. As just one example, a PCB's pads maybe processed to yield a convex shaped pillar and a PKG's pads may be processed to yield a concave shaped pillar.

Further, to enhance mechanical reliability and improve mechanical design validation and testing (MDVT), the angle of the slot that is formed during the above-described shaping operations may be varied across all of the rows or columns of a BGA array, as shown in Figure 18, below.

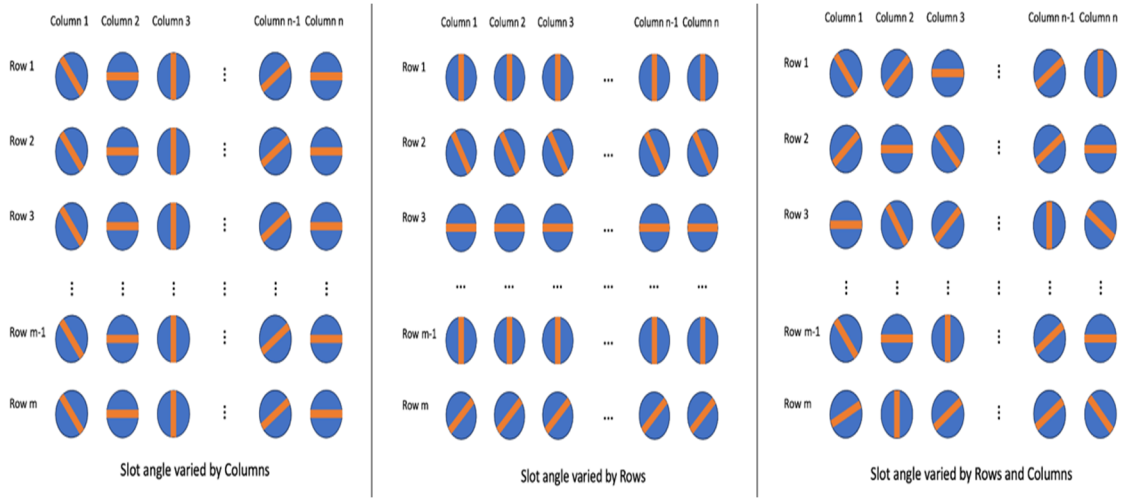

Figure 18: Slot Variability

Further still, under the presented techniques the conductive adhesive may take the form of a solder paste (as noted previously) or some other material.

Various of the benefits of the presented techniques may be illustrated through a simple comparative model, elements of which are depicted in Figure 19, below.

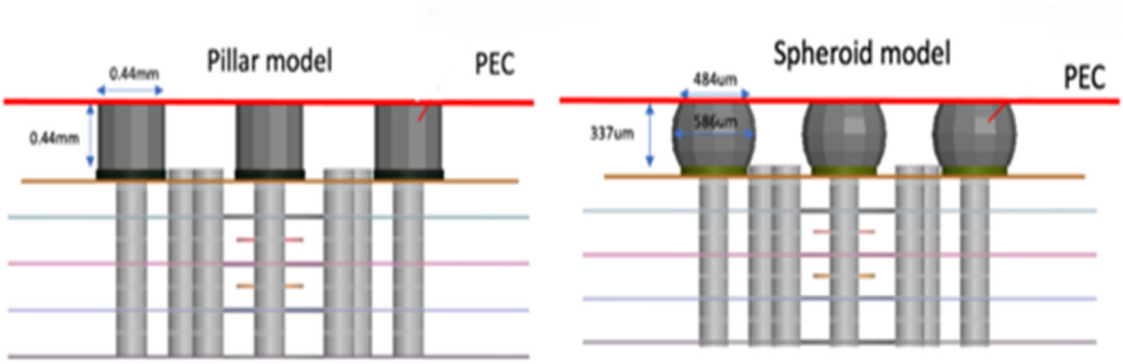

Figure 19: Comparative Model

The left-hand side of the model that is illustrated in Figure 19, above, employs a mounting approach using copper-based pillars that are shaped according to the presented techniques. The right-hand side of the model employs a mounting approach using conventional solder-based spheres or balls. Figures 20 through 22, all below, graphicly depict different SI performance simulation results for the model from Figure 19, above. In each of the following graphs, a blue trace captures the behavior of the copper-based pillars, and a red trace captures the behavior of the solder-based balls.

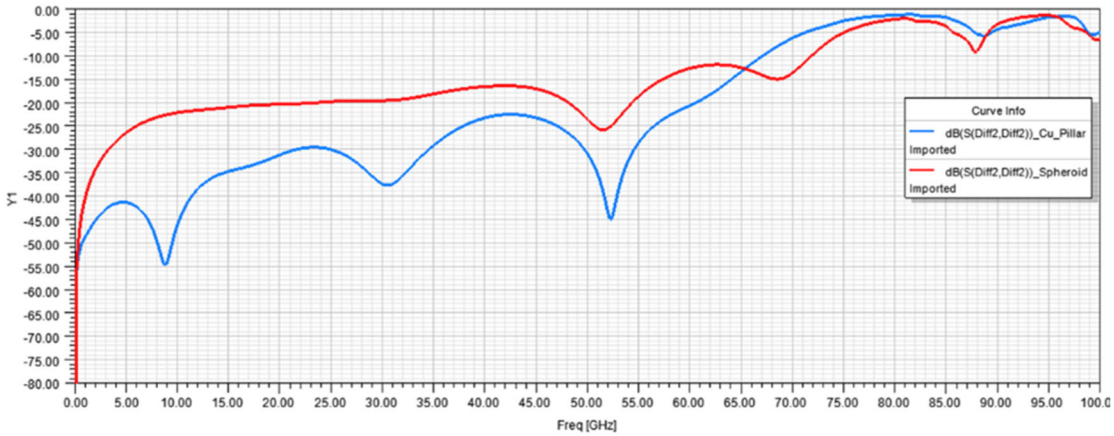

Figure 20: SI Performance Simulation Results – Return Loss

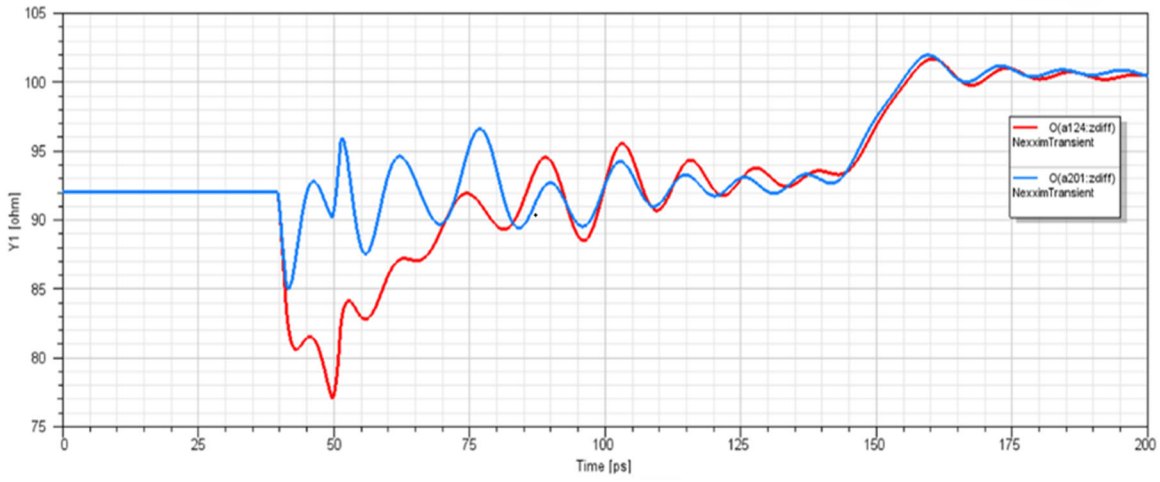

Figure 21: SI Performance Simulation Results – Time Domain Reflectometry (Blue Trace: Cu Pillar Model; Red Trace: Spheroid Model)

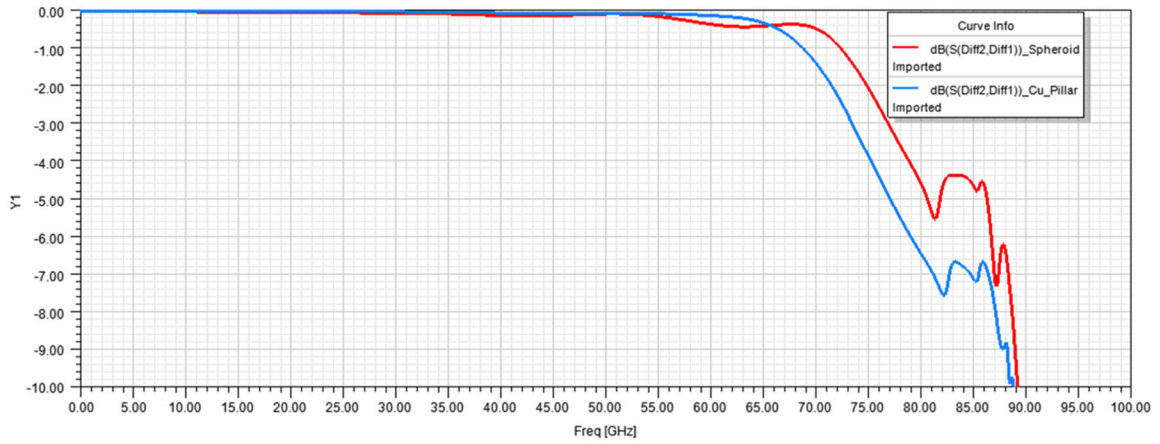

Figure 22: SI Performance Simulation Results – Insertion Loss

As shown in the above figures, compared to conventional solder joints (under, for example, a BGA or LGA packaging arrangement), shaped Cu pillar joints (according to the presented techniques) experience less loss and impedance discontinuity at the joint region.

In summary, techniques have been presented herein that support a novel chip interconnect structure, encompassing convex- and concave-shaped copper joint pillars, for connecting a chip (that follows the OIF NG CEI-224G framework) to a PCB. Aspects of the presented techniques provide excellent SI performance (including return loss, insertion loss, and impedance discontinuity) in support of, for example, a 102.4T switch comprising, among other things, an ASIC having 512 lanes of 224G SerDes capacity. Under further

aspects of the techniques, mechanical performance and long-term reliability are significantly improved.