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Full Utilization of the Four Degrees of Freedom in the Modulation and Control for Five-Level Hybrid-Clamped Converters

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Abstract—**This article demonstrates how to simultaneously utilize three degrees of modulation freedom, e.g. switching state selection (SSS), zero-sequence signal injection (ZSI) and redundant level modulation (RLM) to enable the voltage balancing in certain multilevel topologies, such as the presented five-level (5L), hybrid-clamped (HC) converter topologies, 5L-HC-E and 5L-HC-2E, as reference examples. Phase opposition disposition (POD), is another degree of modulation freedom used for the common-mode voltage (CMV) mitigation. The proposed control scheme is developed for the two most challenging 5L-HC device-reduced high-voltage topologies, which cannot be balanced with traditional modulation freedoms because voltage balance of one capacitor would worsen the balance of other capacitors. Only full utilization of degrees of modulation freedom with higher control ability can solve the balancing problem. A comprehensive explanation of these four control degrees of freedom is presented in this article. Power loss analysis is also provided with high modulation index and power factor. The proposed closed-loop control method can be easily implemented in a digital controller without requiring any mandatory proportional-integral (PI) controllers, since it only relies on closed-form analytical models and basic logic operators. The effectiveness of the control method has been verified in simulation and experiments covering the range of full modulation indexes (0-1.15), full power factors (0-1), various fundamental frequencies (5-50Hz), unequal load and capacitor degradation.**

Index Terms— *switching state selection, zero-sequence signal injection, redundant level modulation, phase opposition disposition, capacitor voltage balance, common-mode voltage mitigation, multilevel converters.*

I. INTRODUCTION

MULTILEVEL converters have been widely used in power grids, such as distributed generation systems and HVDC transmission systems since multilevel converters have lower switching loss, lower *dv/dt* and less harmonic distortion compared to the two-level converters. Multilevel converter topologies have been an active research topic since the 1980s. The classic multilevel converter topologies include neutral-point clamped (NPC) converters, flying capacitor (FC) converters and cascaded H-bridge (CHB) converters. New multilevel topologies have been actively proposed for various
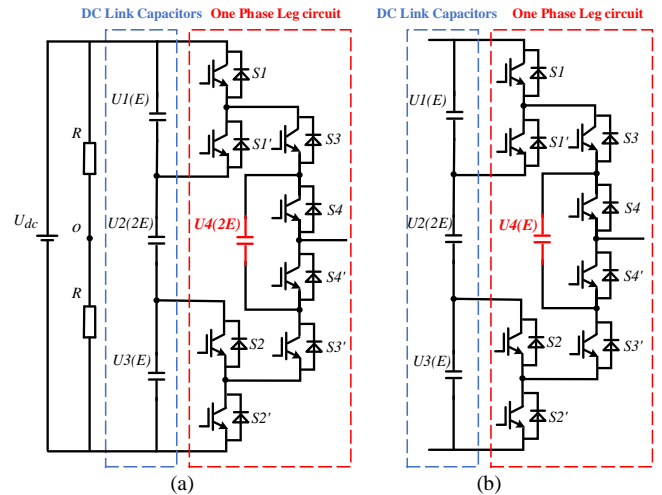
Fig.1. Two hybrid clamped five-level inverter structures. (a) 5L-HC-2E. (b) 5L-HC-E.

applications. For example, modular multilevel converters (MMC) [1, 2] have received substantial attention in the past decades due to its modularity, redundancy and scalability, especially for HVDC applications. Active NPC (ANPC) converters are another attractive group of topologies since they can realize better loss distribution [3] and soft switching [4] of devices by replacing diodes with bidirectional switches. A generalized derivation framework of voltage source multilevel topologies is summarized in [5] and [6], which reflects the connections and logics behind many existing topologies and still inspires new topologies to be derived. Fig.1. (a) and (b) show two five-level, hybrid-clamped converters [7, 8] derived from the generalized topology in [6] as examples, which offers the five-level capability with reduced number of devices as a result of 'topology simplification' [9]. Point *o* is the reference ground. These two topologies have different switching states (SS) and therefore need different control methods. 5L-HC-E was firstly proposed in [8] with a relatively large uncontrollable region: Modulation index (MI) ≤ 0.7 when power factor (PF) is near unity. In each phase, two topologies both only use 8 power switches and one capacitor. E is ¼ of the dc-link voltage (U_{dc}). Power switches suffer from only E except that switch *S4* and *S4*' suffer from 2E for 5L-HC-2E and switch *S3* and *S3*' suffer from 2E for 5L-HC-E. Therefore, these topologies are suitable for high-voltage power systems.

However, these simplified topologies are found to be very challenging to maintain the voltage balance among the internal capacitors, which is the fundamental requirement for them to operate as intended. Conventional single-degree-of-freedom methods, such as the zero-sequence signal injection [10, 11],
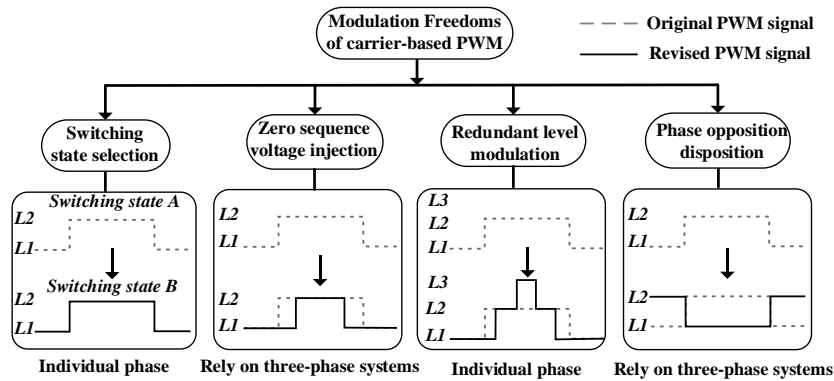
Fig.2. Illustration of four degrees of freedom in the CBPWM.

are unable to solve the voltage balancing issue in this type of topologies. As an example, a control scheme utilizing two degrees of freedom to achieve the voltage balance in a similar topology is proposed in [12]. However, the capacitor voltage balancing/control issue has not been completely solved in the two topologies in Fig. 1. In a later section of this article, the analysis will show that these two topologies are likely to be the most difficult examples to control due to their own properties resulting in multiple control objectives conflicting with each other, while the control ability of only one degree of freedom in modulation is limited. In this case, unless auxiliary voltage balancing circuits are implemented (e.g. [13]), which brings extra cost, volume and power loss, it calls for more advanced modulation-based control schemes to address the voltage balancing issue for these novel topologies to become practically usable.

There are several degrees of freedom in the carrier-based pulse-width modulation (CBPWM) of multilevel converters to be utilized to achieve various control objectives for the fundamental operation (e.g. capacitor voltage balancing) and performance improvement of them (e.g. CMV reduction), as shown in Fig. 2. These degrees of freedom are:

1. Switching state selection: to select switching states under the same voltage level within each phase leg [5];
2. Zero sequence voltage injection [10, 11]: to add a DC voltage offset to all three phase voltages;
3. Redundant level modulation [12, 14-15]: to utilize more voltage levels to replace one voltage level within a switching cycle;
4. Phase opposition disposition [17]: to adjust SS sequences of three phases in one switching cycle.

As the contribution, for the first time, this article cohesively utilizes SSS, ZSI, RLM and POD to realize the voltage balancing control of certain multilevel topologies, such as the two 5L-HC topologies shown in Fig. 1 and reduce the CMV over the full operation range: $0 \leq MI \leq 1.15$ and $0 \leq PF \leq 1$. 5L-HC-2E is firstly proposed and shown in Fig. 1(a). 5L-HC-E, shown in Fig. 1(b), was proposed in [8] with limited operation range. The method proposed in this article removes the need of auxiliary balancing circuits and PI/PID controllers, because it only relies on closed-form analytical models and basic logic operators [18], and thus saves the cost and tuning time. Built on the preliminary work reported in the conference paper [7], this work summarizes four modulation degrees and

improves the performance such as CMV reduction. Also, more operational conditions have been analyzed, such as variable MI, variable PF, capacitor degradation and unequal load. Furthermore, power loss analysis has been done with and without POD. This article is structured as follows: Firstly, a review of the four modulation freedoms is provided in Section II. Secondly, an analysis of the voltage balancing problem and the principle of the proposed control scheme is illustrated in Section III. Thirdly, the CMV control is considered with the modulation degree of POD. Simulation and experiments are presented to validate the effectiveness of the proposed control scheme under various operating conditions in the Section IV and V.

II. REVIEW OF DEGREES OF FREEDOM IN MODULATION AND CONTROL OBJECTIVES

The comparison of four degrees of modulation freedom is concluded in this Table I.

TABLE I
COMPARISON OF FOUR DEGREES OF MODULATION FREEDOM

	Advantages	Disadvantages
SSS	Easy to use	Weak control ability
		Need redundant SS
ZSI	Medium control ability	Rely on 3-phase systems
RLM	Strong control ability	More switching loss
		Worse harmonics
POD	Independent degree of freedom	No balancing ability
	Mitigate CMV	Rely on 3-phase systems

Firstly, switching state selection is a degree of modulation freedom if there is the redundancy of switching states in some types of topologies. Generally, more redundancy of switching states can be found in topologies with more devices. For example, traditional FC converters have a large degree of freedom in switching states because these topologies provide many current paths. Topologies with less devices are preferred nowadays because of lower cost and higher power density and therefore switching state selection alone cannot realize the control objectives, such as capacitor voltage balance, in some simplified topologies.

Modulation waveforms and carrier waveforms can provide degrees of freedom in the method of CBPWM. Zero sequence voltage injection is a common degree of freedom in three-phase systems from the point of modulation waveforms, which adds the same voltage offset into all three phase voltages, but does not change line voltages. It can balance capacitor voltage,
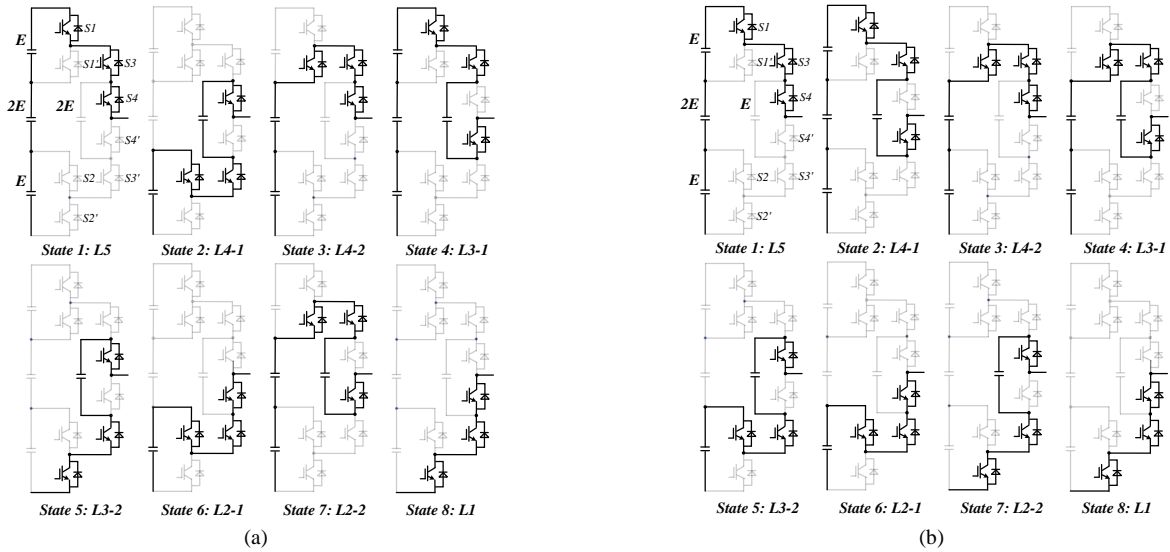
Fig.3. Current paths of all switching states in (a) 5L-HC-2E. (b) 5L-HC-E.

TABLE II
ALL CASES OF CAPACITOR CHARGING SITUATIONS OF 5L-HC-2E

Level	U_o	State	S_1	S_2	S_3	S_4	U_1 i>0	U_1 i<0	U_2 i>0	U_2 i<0	U_3 i>0	U_3 i<0	U_4 i>0	U_4 i<0
5	4E	L5	1	1	1	1	-	-	-	-	-	-	-	-
4	3E	L4-1	1	1	0	1	↑	↓	↑	↓	↓	↑	↓	↑
		L4-2	0	1	1	1	↑	↓	↓	↑	↓	↑	-	-
3	2E	L3-1	1	1	1	0	-	-	-	-	-	-	↑	↓
		L3-2	0	0	0	1	-	-	-	-	-	-	↓	↑
2	E	L2-1	0	1	0	0	↑	↓	↑	↓	↓	↑	-	-
		L2-2	0	0	1	0	↑	↓	↓	↑	↓	↑	↑	↓
1	0	L1	0	0	0	0	-	-	-	-	-	-	-	-

TABLE III
ALL CASES OF CAPACITOR CHARGING SITUATIONS OF 5L-HC-E

Level	U_o	State	S_1	S_2	S_3	S_4	U_1 i>0	U_1 i<0	U_2 i>0	U_2 i<0	U_3 i>0	U_3 i<0	U_4 i>0	U_4 i<0
5	4E	L5	1	1	1	1	-	-	-	-	-	-	-	-
4	3E	L4-1	1	1	1	0	-	-	-	-	-	-	↑	↓
		L4-2	0	1	1	1	↑	↓	↓	↑	↓	↑	-	-
3	2E	L3-1	0	1	1	0	↑	↓	↓	↑	↓	↑	↑	↓
		L3-2	0	1	0	1	↑	↓	↑	↓	↓	↑	↓	↑
2	E	L2-1	0	1	0	0	↑	↓	↑	↓	↓	↑	-	-
		L2-2	0	0	0	1	-	-	-	-	-	-	↓	↑
1	0	L1	0	0	0	0	-	-	-	-	-	-	-	-

reduce switching loss and reduce CMV. Searching optimization method is proposed in [10] to find the best ZSI signal. The accuracy is decided by the number of possible ZSI voltages and depends on the calculation ability of controllers, such as DSP. An interpolation method is proposed in [11] to obtain the theoretical optimum ZSI signal through deriving the nonlinear and discontinuous relationship between zero sequence voltage and neutral current in a three-level NPC inverter. This method improves the accuracy but increases the calculation complexity.

Redundant level modulation (RLM) [12], [14-15] is another degree of freedom in modulation waveforms at the cost of switching loss and CMV. This method splits the modulation waveform into several parts according to the voltage level and utilizes two or more voltage levels to replace one voltage level in a switching cycle based on the principle that the average voltage in the switching cycle should not change. It is usually used to realize the voltage balance when other freedoms cannot realize it. A control method using the RLM as least as possible is proposed in [14] to reduce the switching loss. Also, utilization of SiC switches can improve efficiency. Note that the unwanted voltage level in RLM still occupies few duty cycle to make sure that voltages only change between adjacent two levels. If the voltage jump can be larger than one level, it can become another control degree of freedom[16].

Traditional control degrees of freedom of carrier waveforms are phase degree, amplitude and frequency. POD is used to reduce CMV by using different phase degrees in [17]. DC-link capacitor voltage ripple is compensated by changing the amplitude of carrier waveforms in [19]. Optimal carrier waveform frequency can be analyzed in a MMC converter with phase-shifted PWM to achieve the least switching loss in [20].

Carrier-overlapped PWM (COPWM) [21], [22] is a newly proposed control method by changing carrier waveforms. Similar to RLM, COPWM also replaces the original voltage level with more voltage levels to achieve better performance. The difficulty of COPWM is to find a suitable fixed carrier waveform combination. PI regulators are needed in COPWM because influence on capacitor voltage caused by carrier waveforms is not easy to be expressed in mathematical formula. Also, control ability of COPWM is weaker than that of RLM because undesired voltage levels cannot be reduced to the least.

Voltage balance is one important control objective. Although different degrees of control freedom are used to realize voltage balance, the nature behind is the same. Capacitor voltage balance is decided by the current path. If current flowing in a capacitor equals current flowing out of the capacitor in a switching cycle, the capacitor voltage remains constant. In terms of voltage balance, some current paths have positive effects, some have no effects and some have negative effects. Current paths are decided by switching states. So, the way to balance the voltage is to find a good combination of switching states that can provide current paths having positive influence. Three types of switching state combinations are concluded in [6]: in the same voltage level (e.g. SSS), in any adjacent two
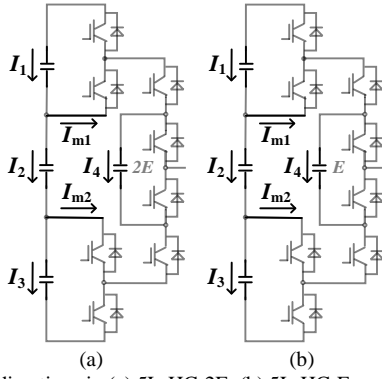
(a)   (b)

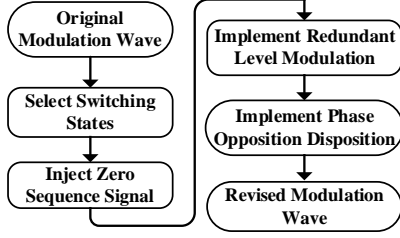Fig.4. Current directions in (a) 5L-HC-2E. (b) 5L-HC-E.

Fig.5. Structure of control method with four control degrees of freedom.

voltage levels (e.g. ZSI), in any voltage levels (e.g. RLM, COPWM).

Common-mode voltage reduction is another hot topic. One way in SVPWM is to only choose vectors with zero or less CMV, but it sacrifices the control ability. In CBPWM, approaches based on modulation waveform can also reduce CMV, such as ZSI. However, it may limit the usage of ZSI in other control objectives. POD achieves CMV mitigation without reducing control abilities. The function is that phase voltages countervail their effects on CMV when carrier waveforms have 180 phase shift degree. In essence, it uses the degree of freedom in switching state sequence.

III. PROPOSED VOLTAGE BALANCING SCHEMES WITH CMV REDUCTION

There are 8 switching states for both two converter topologies and current paths of them are shown in Fig. 3. They are divided into 5 groups depending on the output voltage: L1, L2, L3, L4 and L5 for 0, E, 2E, 3E and 4E respectively. Note that there are two kinds of switching states for L2, L3 and L4: L2-1 and L2-2, L3-1 and L3-2, L4-1 and L4-2. Capacitor voltage changes are illustrated in Table II and Table III. The upper side of capacitors is designed to be positive. The direction of current is shown in Fig. 4. '↑', '↓' and '-' show that the capacitor is charged, discharged and unchanged. The sequence selection of control degrees of modulation freedom is the same with both converters. It is SSS, ZSI, RLM and then POD as Fig. 5 shows. Detailed calculation will be explained in the following chapters.

A. Allocation of control degrees of freedom for 5L-HC-2E

It can be seen from the Table II that in L2, L3 and L4, capacitor voltage balance is challenging for the first example, 5L-HC-2E. Flying capacitor U_4 can only be regulated in its individual phase. Although SSS in L3 can be decided by the U_4 deviation, SSS in L2 and L4 should consider the other three

capacitors, especially U_2. In this way, U_4 cannot be balanced with traditional degrees of modulation freedom especially when voltage levels change between L1-L2 and L4-L5. Meanwhile, U_1 and U_3 balance needs ZSI through collective effect of three phases. Otherwise, the low frequency voltage oscillation would be large. Therefore, the method combining four degrees of modulation freedom is proposed to deal with the difficult voltage balance problem along with CMV mitigation.

Redundant switching states in L2, L3 and L4 have opposite influence on U_2 or U_4 voltage. For example, L2-1 charges U_2 while L2-2 discharges U_2. Thus, each voltage level should only use one switching state according to the capacitor voltage condition in a switching cycle. Switching states should be selected firstly because further control method is based on the them. For the first example, 5L-HC-2E, it is obvious that L3 only influences U_4. So the selection between L3-1 and L3-2 is decided by U_4 unbalance condition. Also, U_2 is only affected by L2 or L4. So the selection of L2 and L4 depends on U_2 unbalance condition.

Here, it is assumed that U_2 and U_4 need to be charged and $i > 0$ as an example to show further control method. L2-1, L3-1 and L4-1 are chosen for capacitor voltage balance.

It can be seen from Table II that U_1 and U_3 are affected by L2 or L4. No matter which state is selected, when $i > 0$, U1 is charged and U_3 is discharged in L2 or L4. When $i < 0$, U1 is discharged and U_3 is charged. In one phase system, U_1 and U_3 cannot balance because of the unidirectional charging situation. However, in a three-phase system, each phase has 120° phase shift degree with any other phase. In this way, even if two phases charge the capacitor, at least one phase discharges the capacitor. Thus, ZSI can be used to balance U_1 and U_3. Searching optimization method is chosen to find the best zero sequence voltage. The objective of ZSI is:

$$S = (U_{1\_trial} - E)^2 + (U_{3\_trial} - E)^2 \tag{1}$$

Here, U_{1_trial} and U_{3_trial} are modified capacitor voltages after ZSI.

$$U_{1\_trial} = U_1 + \frac{I_1}{C_1 * f_{sw}} \tag{2}$$

$$U_{3\_trial} = U_3 + \frac{I_3}{C_3 * f_{sw}} \tag{3}$$

f_{sw} is the switching frequency. I_1 and I_3 are current through capacitor U_1 and U_3 after ZSI. C_1, C_2 and C_3 are capacitance values of U_1, U_2 and U_3. I_{m1_trial} and I_{m2_trial} are defined to express the current through connecting points of dc-link capacitors, as shown in Fig. 4(a). Relationships can be derived by capacitor paralleling rule:

$$I_1 = \frac{C_2 + C_3}{C_1 + C_2 + C_3} I_{m1\_trial} + \frac{C_3}{C_1 + C_2 + C_3} I_{m2\_trial} \tag{4}$$

$$I_3 = -\frac{C_1}{C_1 + C_2 + C_3} I_{m1trial} - \frac{C_1 + C_2}{C_1 + C_2 + C_3} I_{m2\_trial} \tag{5}$$

The reason why I_{m1_trial} and I_{m2_trial} are introduced is that they can be easily expressed by phase currents and duty ratios:

$$I_{m1\_trial} = I_A \cdot ((L_{4A} - 1) \cdot D_{4A} + (L_{2A} - 1) \cdot D_{2A}) + I_B ((L_{4B} - 1) \cdot D_{4B} + (L_{2B} - 1) \cdot D_{2B}) + I_C \cdot ((L_{4C} - 1) \cdot D_{4C} + (L_{2C} - 1) \cdot D_{2C}) \tag{6}$$
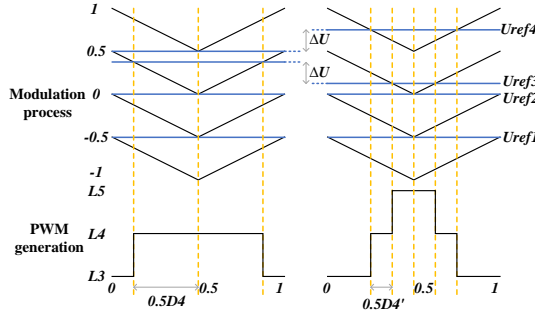
Fig. 6. Illustration of RLM implementation.

$$I_{m2\_trial} = I_A \cdot \big((2 - L_{4A}) \cdot D_{4A} + (2 - L_{2A}) * D_{2A}\big) + I_B \cdot \big((2 - L_{4B}) \cdot D_{4B} + (2 - L_{2B}) \cdot D_{2B}\big) + I_C \cdot \big((2 - L_{4C}) \cdot D_{4C} + (2 - L_{2C}) * D_{2C}\big) \quad (7)$$

Here, I_A, I_B and I_C are current of phase A, B and C respectively. Duty ratios of level 2, 3 and 4 are D_{2A}, D_{3A} and D_{4A} for phase A, D_{2B}, D_{3B} and D_{4B} for phase B and D_{2C}, D_{3C} and D_{4C} for phase C. They can be calculated easily according to the phase voltages. $L_{4A}, L_{2A}, L_{4B}, L_{2B}, L_{4C}, L_{2C}$ are integer variables. They are 1 when first switching state is chosen and 2 when second switching state is chosen. For example, L_{2A} is 1 when L2-1 is chosen and 2 when L2-2 is chosen.

S can be calculated with (1)-(7) by searching optimization method [10]. The step in this method should be small to maintain the accuracy of ZSI and selected according to the calculation capacitor of the processor.

Control method with SSS and ZSI cannot balance this converter, especially U_4, in the full range. It can be seen from Table II that selection of L2 and L4 may have undesired effect on U_4 balance since this selection is decided by U_2. RLM can be utilized to balance U4 by providing better current paths for U_4. Two groups of switching states are used for RLM in the example of 5L-HC-2E: L1, L2 and L3 or L3, L4 or L5.

Here, the process of replacing L4-1 with L3-1 and L5 in one phase is presented. Fig. 6 shows the implementation with carrier waveform based phase disposition modulation. The modulation waveform (U_{ref}) is split into four parts (U_{ref1}-U_{ref4}):

$$U_{ref1} = \begin{cases} U_{ref}, & U_{ref} < -\dfrac{1}{2} \\ 0, & U_{ref} \geq -\dfrac{1}{2} \end{cases} \quad (8)$$

$$U_{ref2} = \begin{cases} U_{ref}, & -\dfrac{1}{2} \leq U_{ref} < 0 \\ 0, & U_{ref} \geq 0 \text{ or } U_{ref} < -\dfrac{1}{2} \end{cases} \quad (9)$$

$$U_{ref3} = \begin{cases} U_{ref}, & 0 \leq U_{ref} < \dfrac{1}{2} \\ 0, & U_{ref} \geq \dfrac{1}{2} \text{ or } U_{ref} < 0 \end{cases} \quad (10)$$

$$U_{ref4} = \begin{cases} U_{ref}, & \dfrac{1}{2} \leq U_{ref} \\ 0, & U_{ref} < \dfrac{1}{2} \end{cases} \quad (11)$$

The core of the change is to move U_{ref4} up and U_{ref3} down by ΔU. ΔU should be calculated according to U_4 unbalance condition. ΔU can be derived from the geometry relationship:

$$\Delta U = \frac{1}{4}(D_{4-1} - D'_{4-1}) \quad (12)$$

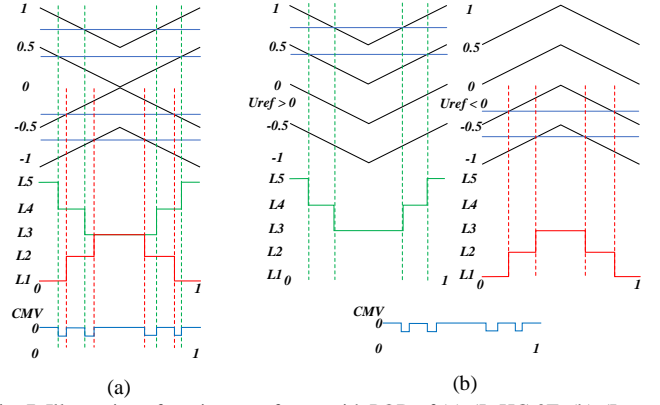(a)   (b)

Fig. 7. Illustration of carrier waveforms with POD of (a) 5L-HC-2E. (b) 5L-HC-E.

D_{4-1} and D'_{4-1} are duty ratios of original and revised L4-1. In a switching cycle, only L3-1, L4-1 and L5 are used:

$$D'_{3-1} + D'_{4-1} + D'_5 = 1 \quad (13)$$

The use of RLM follows the voltage-second principle:

$$D'_5 + \frac{1}{2}D'_4 = U_{ref} \quad (14)$$

ΔU_4 is the difference between ideal and measured U4 voltage:

$$\Delta U_4 = 2E - U_4 \quad (15)$$

As Table II shows, the U_4 voltage change in a switching cycle is described following the capacitor voltage-current rule:

$$I(-D'_{4-1} + D'_{3-1}) = C_4 \cdot \Delta U_4 \cdot f_{sw} \quad (16)$$

C_4 is the capacitance value of U_4. Combing (13)-(16), D'_{4-1} can be obtained:

$$D'_{4-1} = \frac{2}{3}\left(1 - U_{ref} - \frac{C_4 \cdot \Delta U_4 \cdot f_{sw}}{I}\right) \quad (17)$$

Note that the voltage level should change between adjacent two levels, so D'_{4-1} should at least exceed the set deadtime. Then the modulation signals, U'_{ref1} - U'_{ref4}, can be expressed as:

$$\begin{bmatrix} U'_{ref1} \\ U'_{ref2} \\ U'_{ref3} \\ U'_{ref4} \end{bmatrix} = \begin{bmatrix} U_{ref1} \\ U_{ref2} \\ U_{ref3} - \Delta U \\ U_{ref4} + \Delta U \end{bmatrix} \quad (18)$$

Common-mode voltage (U_{CM}) here can be expressed as:

$$U_{CM} = \frac{1}{3}(U_A + U_B + U_C) \quad (19)$$

U_A, U_B and U_C are three phase voltages. For 5L-HC-2E, carrier waveforms can be divided into two groups as Fig. 7(a) shows: the upper two waveforms and the below two waveforms. The phase shift is 180 degrees between two groups.

In a three-phase system, there is at least one phase voltage greater than zero and one less than zero respectively. Fig. 7(a) shows that CMV is highly reduced because these phase voltages offset their effect on CMV. The green lines and red lines are used to show how phase voltages and CMV are generated. The remaining process of modulation is the same as the traditional methods after both modulation and carrier waveforms are revised.

B. Allocation of control degrees of freedom for 5L-HC-E

The basic control process of the example of 5L-HC-E is the same with the first example, 5L-HC-2E. But the detailed control method is different because switching states differ. From Table III, it can be seen that SSS in the voltage level 2, 3 and 4 affect all four capacitors while in the first example, U_1, U_2 and U_3 are not affected by L3. In the example of 5L-HC-E, SSS should consider either U_2 or U_4 and the voltage balance of them cannot be realized at the same time in traditional modulation methods.

In a three-phase system, U_2 is influenced by all three phases, however, U_4 balance is only decided by its individual phase. So the balance of U_4 has priority over U_2. Strategy adopted in this article chooses switching states only considering U_4 balance. If U_4 needs charging, L2-1, L3-1 and L4-1 are chosen when $i > 0$ and L2-2, L3-2 and L4-2 are chosen when $i < 0$. If U_4 needs discharging, L2-2, L3-2 and L4-2 are chosen when $i > 0$ and L2-1, L3-1 and L4-1 are chosen when $i < 0$.

After SSS, ZSI is employed to balance dc-link capacitor U_1 and U_3. Influence of different switching states on the capacitor balance is quite similar to the first example which can be seen in Table II and Table III. Thus, the process of ZSI in 5L-HC-E is the same with 5L-HC-2E.

Next, RLM is utilized to solve the U_2 balance problem.

- *Condition I: L2-1, L3-1 and L4-1 are selected:*

If U_2 needs charging and $i > 0$ or U_2 needs discharging and $i < 0$, RLM should be adopted when $-0.5 \leq U_{ref} \leq 0.5$, replacing L3-1 with L2-1 and L4-1. If U_2 needs discharging and $i > 0$ or U_2 needs charging and $i < 0$, RLM should be adopted when $-1 \leq U_{ref} \leq 0$, replacing L2-1 with L1 and L3-1.

- *Condition II: L2-2, L3-2 and L4-2 are selected:*

If U_2 needs charging and $i > 0$, or U_2 needs discharging and $i < 0$, RLM should be adopted when $0 \leq U_{ref} \leq 1$, replacing L4-1 with L3-1 and L5. If U_2 needs discharging and $i > 0$ or U_2 needs charging and $i < 0$, RLM should be adopted when $-0.5 \leq U_{ref} \leq 0.5$, replacing L3-1 with L2-1 and L4-1.

Modulation waveform changes during RLM in detail can be obtained in the same way as (8)-(18) show. In terms of carrier waveforms, different strategy should be used. In the example of 5L-HC-E, switching state combinations include: voltage level 1, 2 and 3, voltage level 2, 3 and 4, voltage level 3, 4 and 5. During RLM, carrier waveforms cannot have phase shift, otherwise, voltage jumps will become a severe problem. New POD is shown as Fig. 7(b). When $U_{ref} \geq 0$, carrier waveform chooses the sag shape. When $U_{ref} \leq 0$, carrier waveform chooses the bulge shape. In this way, higher voltage levels in the phase voltage higher than zero can offset lower voltage levels in the phase voltage lower than zero.

IV. SIMULATION RESULTS

Simulations have been conducted in MATLAB Simulink with parameters listed in Table IV to verify the effectiveness of the control method in two five-level three-phase converters. Switching devices for power loss analysis are FZ400R17KE3 and FF1800R23IE7 from Infineon.

Fig. 8 shows the steady-state waveforms of two converter schemes at MI=1.15 and PF=0.999 respectively. Line voltages under two schemes obtain desired number of voltage levels. Voltage spike phenomenon during one switching cycle exists

TABLE IV
PARAMETERS OF SIMULATION

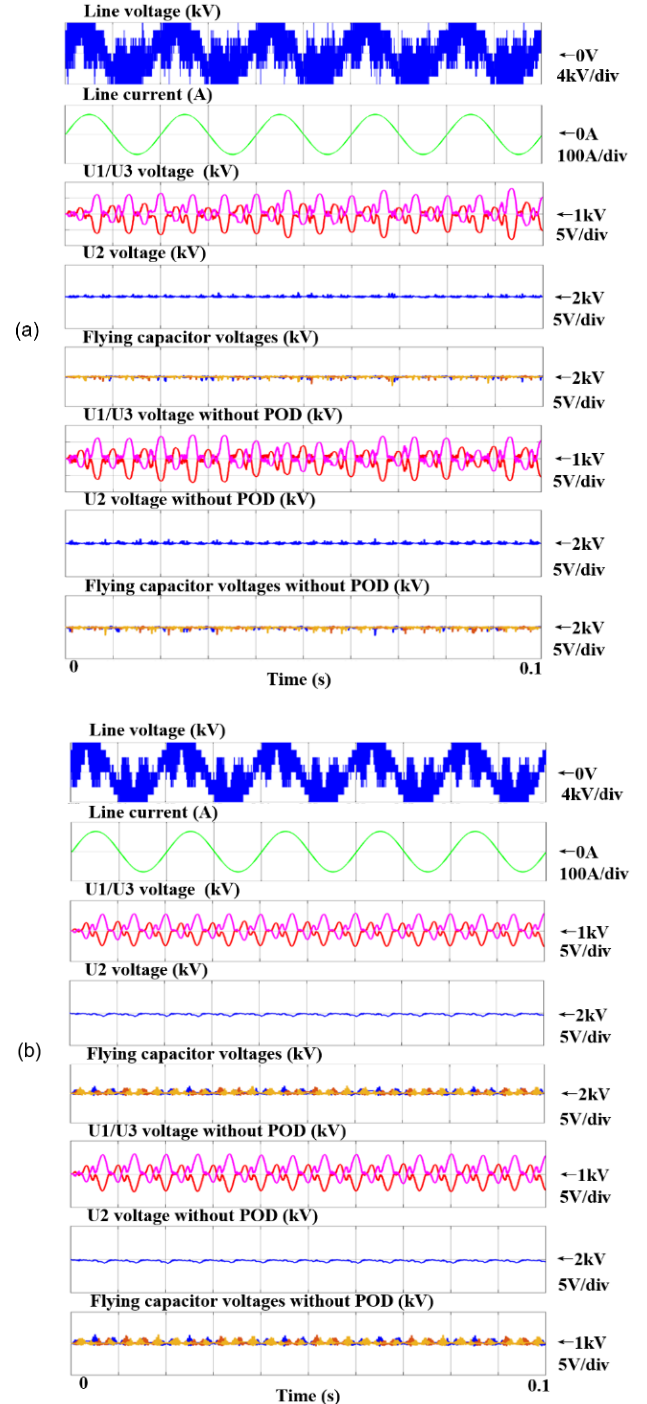| Parameters	Value
DC-link Voltage V_{dc}	4000V
Carrier Frequency f_{sw}	20kHz
Fundamental Frequency f_0	50Hz
DC-link Capacitors	C1=C3=1.47mF, C2=1mF
Flying Capacitors	C4=1mF
Modulation Index	0-1.15
Power Factor $cos\varphi$	0-1
Passive load	33ohms 3.68mH per phase ($cos\varphi = 0.999$)

Fig. 8. Simulation performance with steady state at MI=1.15 and PF=0.999 of (a) 5L-HC-2E. (b) 5L-HC-E.
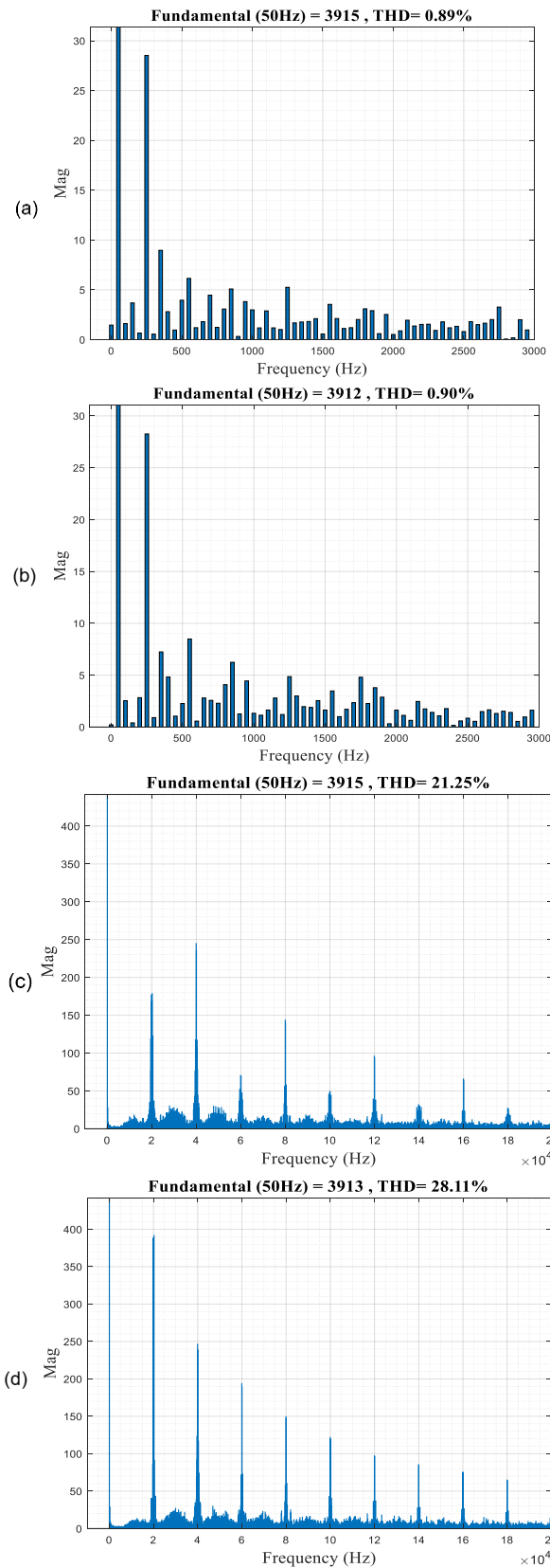
Fig. 9. FFT analysis of line voltage of 5L-HC-2E at MI=1.15 and PF=0.999. Harmonics at low frequency (a) without POD. (b) with POD. Harmonics at high frequency (c) without POD. (d) with POD.
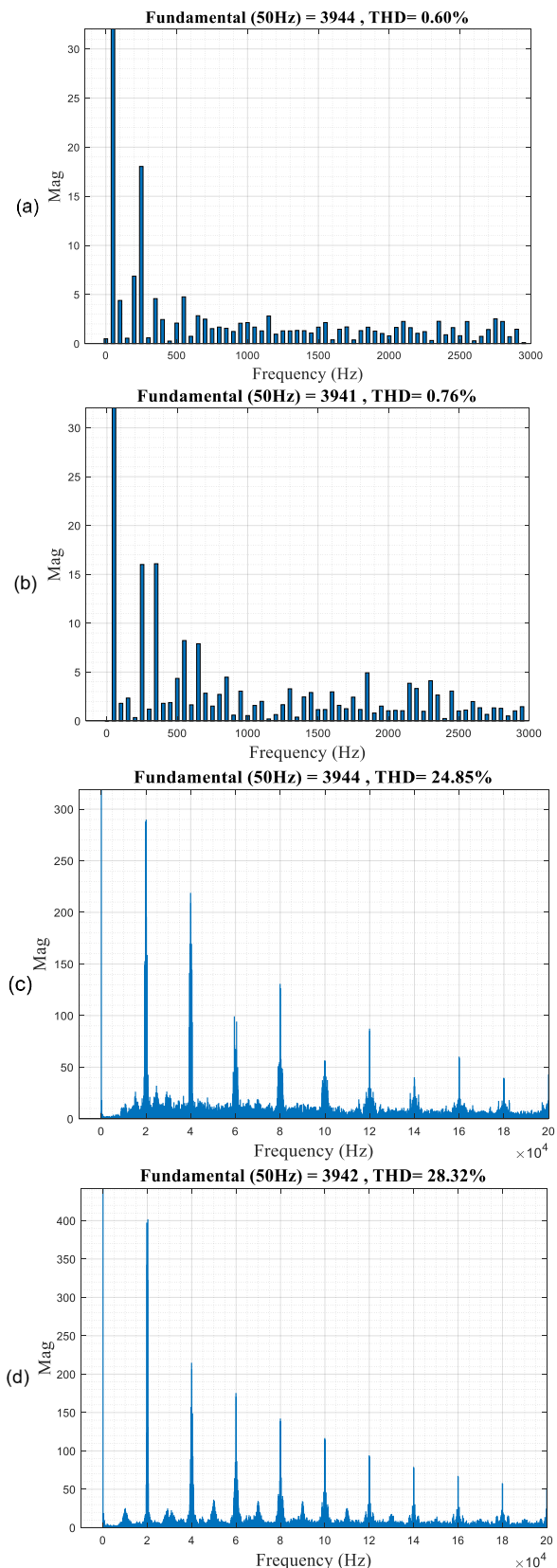

Fig. 10. FFT analysis of line voltage of 5L-HC-E at MI=1.15 and PF=0.999. Harmonics at low frequency (a) without POD. (b) with POD. Harmonics at high frequency (c) without POD. (d) with POD.

in 5L-HC-2E. This is caused by current freewheeling during the deadtime. Voltage spike during one switching cycle is avoided in 5L-HC-E due to better switching state selections. The quality of the line currents under both schemes are acceptable. All capacitor voltages fluctuate in the allowable region. No obvious voltage changes are found with the utilization of POD.
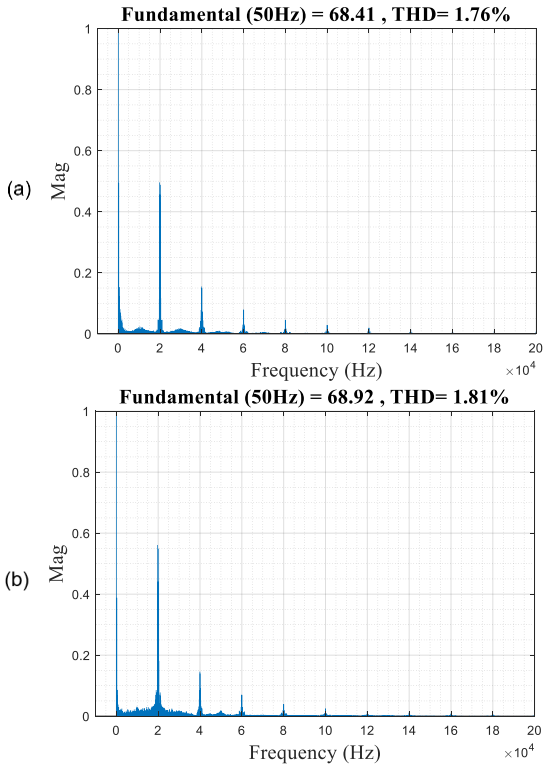
Fig. 11. FFT analysis of current at MI=1.15 and PF=0.999 of (a) 5L-HC-2E. (b) 5L-HC-E.

Fig. 12. Common mode voltage with and without POD at MI=1.15 and PF=0.999 in simulation of (a) 5L-HC-2E. (b) 5L-HC-E.

FFT analysis of the line voltages under both schemes is presented with the steady state in Fig. 9 and Fig. 10 respectively at MI=1.15 and PF=0.999. The max frequency is set as 200kHz to present total harmonic distortion (THD) and 3kHz to present harmonics near 50Hz. The THD values with and without POD are 28.11% and 21.25% for 5L-HC-2E scheme and 28.32% and 24.85% for 5L-HC-E scheme respectively. The harmonics at high frequency can be easily filtered out. Harmonics near 50Hz do not become large after POD. Both schemes show good THD performance especially near 50Hz.

FFT analysis of the currents under both schemes is presented with the steady state in Fig. 11. The THD values are good after the inductance filter in the load.

CMV with and without POD are compared in both schemes as shown in Fig. 12 at MI=1.15 and PF=0.999. The reduction in CMV can be found in schemes with POD. The percentage of the highest CMV is reduced in two schemes although the value remains the same. This is partly because some peak values are caused by voltage spikes during the deadtime. Also, an obvious reduction can be found in the average CMV in both schemes. The large improvement of the magnitude at multiple times of switching frequency in the frequency domain is also shown in Fig. 13. In order to better present the number of variations and the dv/dt, the magnified CMV is shown in Fig. 14. The number of high dv/dt is reduced along with the average CMV reduction under both schemes. However, the number of variations does not have an obvious reduction. This is because the proposed control method is not an active control for the CMV reduction. Future work can be done to reduce the number of variations along with the maximum CMV.

Dynamic performance of two schemes are verified under three conditions: variable fundamental frequencies (f_0), variable MI and variable PF. In theory, no matter what operating

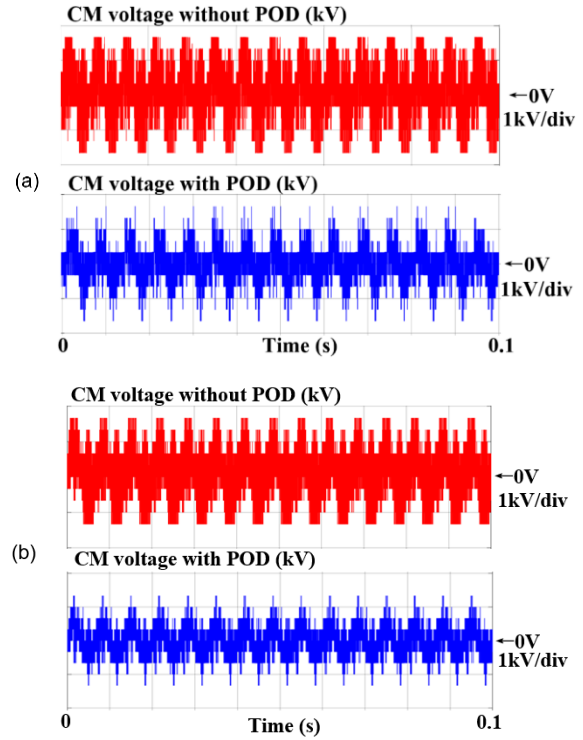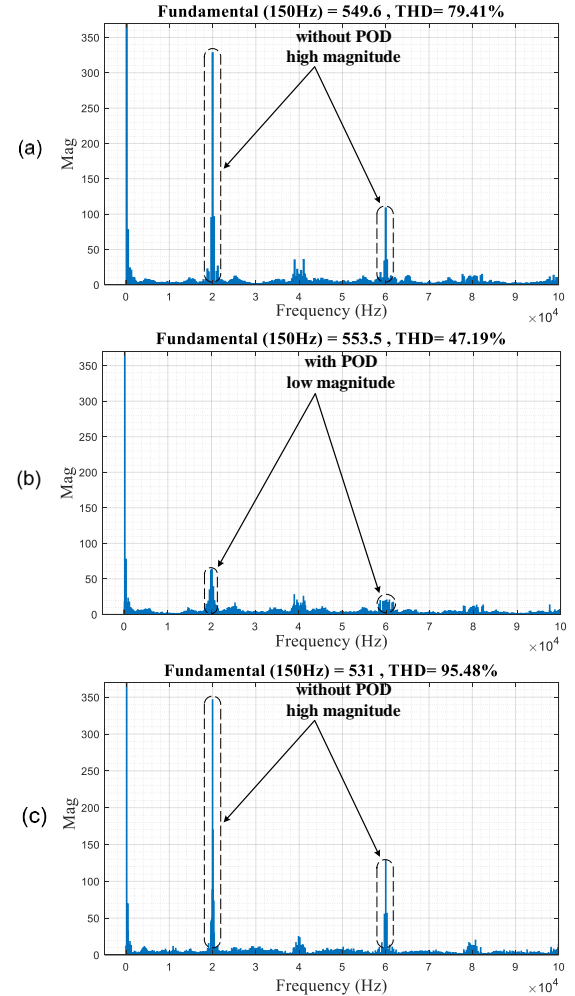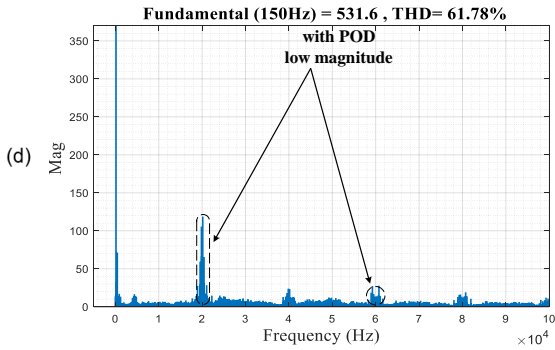Fig. 13. Common mode voltage reduction in frequency domain. 5L-HC-2E: (a) without POD. (b) with POD. 5L-HC-E: (c) without POD. (d) with POD.

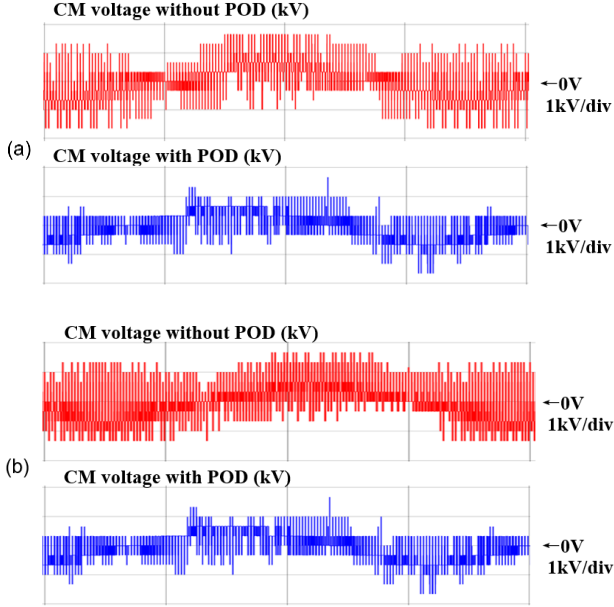Fig. 14. Magnified common mode voltage with and without POD at MI=1.15 and PF=0.999 in simulation of (a) 5L-HC-2E. (b) 5L-HC-E.
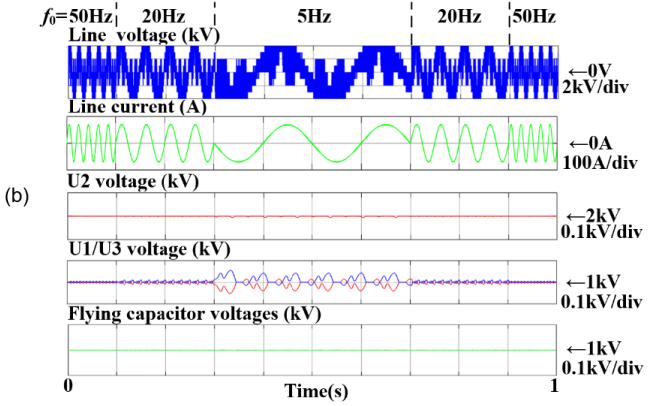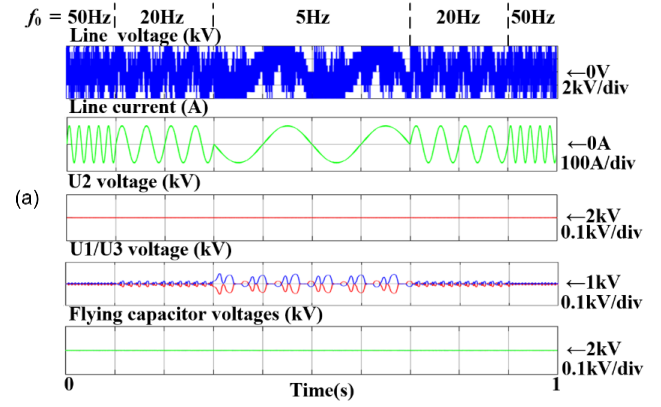

Fig. 15. Simulation performance with variable fundamental frequencies of (a) 5L-HC-2E. (b) 5L-HC-E.

Fig. 16. Simulation performance with variable modulation indexes at MI=0.3, 0.7 and 1 of (a) 5L-HC-2E. (b) 5L-HC-E.

conditions are, voltage balance can always been achieved. This is because there is always at least one switching state good for the voltage balance in adjacent three voltage levels, and then RLM is used to increase the usage of the desired switching state.

Fig. 15 shows that two schemes can be controlled when f_0 switches between 5 Hz and 50 Hz at MI=1.15 and PF=0.999. The line voltage and line current match the desired waveforms. U_2 and FC voltages are well balanced and the deviation of them under both schemes are less than 1%. U_1/ U_3 voltages fluctuate more largely when f_0 decreases. An error less than 5% can be found in U_1/ U_3 voltages when f_0 is 5 Hz under both example schemes.

Fig. 16 shows the performance of two schemes with MI varying and PF=0.999. The line voltages and currents are desired. Voltage deviation of all capacitors is less than 1% under both schemes.

Fig. 17 presents the control ability of two schemes when the power factor angle (PFA) changes from 0° to 90° at MI=1.15. The load current is set as 20A rms. In both schemes, the errors of U_2 and flying capacitor voltages are less 1%. U_1/ U_3 voltages fluctuate within 3% under two schemes.

Fig. 18 shows the efficiency with proposed control method under two schemes. The load is set as 20A. RLM is used to extend the controllable region at the cost of power loss, so it

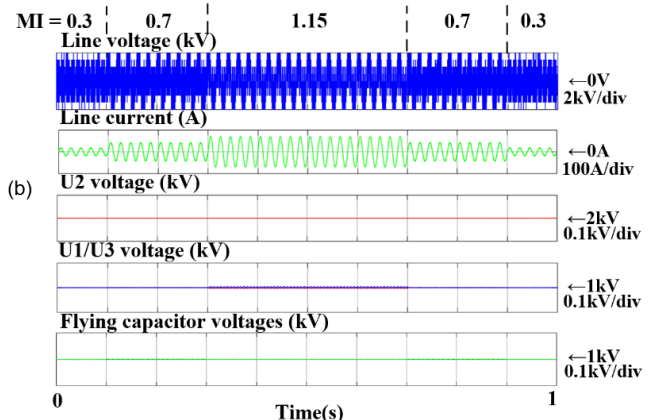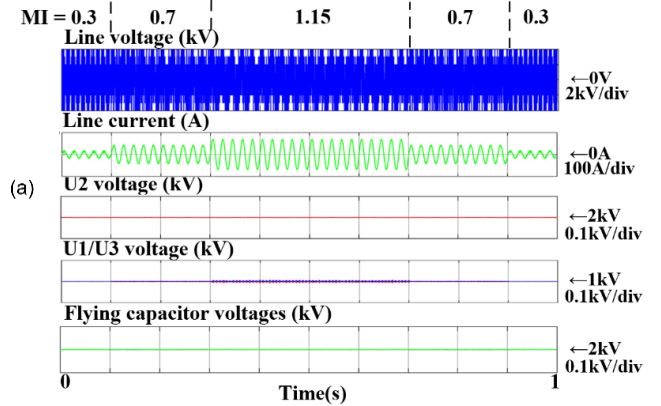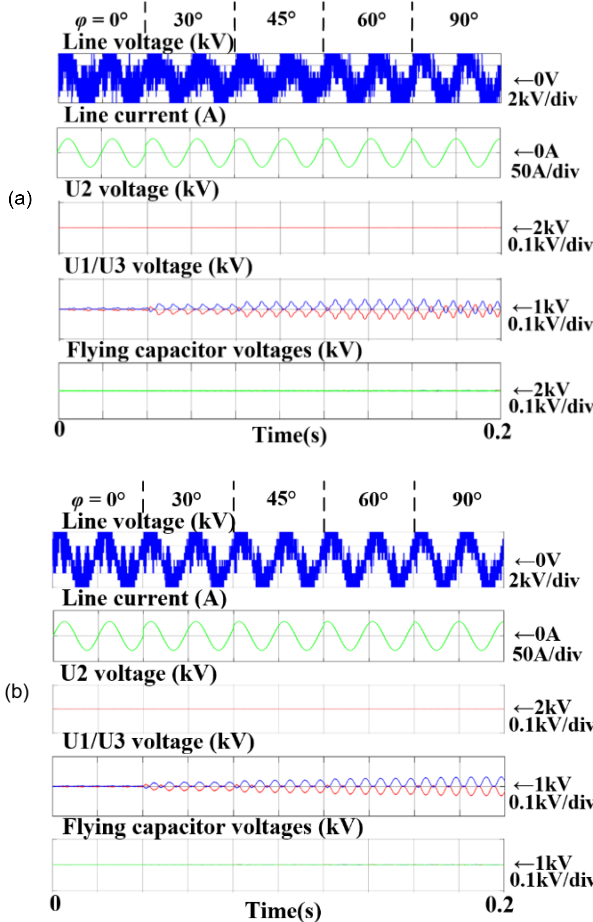Fig. 17. Simulation performance with variable power factors of (a) 5L-HC-2E. (b) 5L-HC-E.

Fig. 18. Power loss analysis with MI ≥ 0.6 and cosφ ≥ 0.6 of (a) 5L-HC-2E. (b) 5L-HC-E.

should be used as least as possible. When the topology can be controlled with SSS and ZSI, RLM is not needed [14]. Considering the uncontrollable area is usually when MI and PF is high [8], only the operational conditions with MI ≥ 0.6 and cosφ ≥ 0.6 are analyzed. It can be found in both schemes that the efficiency increases when the MI or PF increases with the proposed control method. The efficiencies near the unit MI and PF are around 96% while the efficiency of 5L-HC-2E scheme is a little higher than that of 5L-HC-E scheme. Also, when the MI and PF are low, efficiencies under both schemes are low, less than 90%. A control method using less RLM can be proposed in the future work.

As is the Table V and Table VI shown, the efficiency of both schemes does not have a large change after POD. Therefore, it can be concluded that POD does not influence the performance of other metrics after considering capacitor voltage ripples, THD and efficiency.

Fig. 19 shows the operations with parameter deviations with MI=1.15 and PF=0.999. The proposed control method is based on the analytical model. Therefore, parameter deviations can influence the accuracy of the model calculation. For 5L-HC-2E scheme, the conductance values of U_1, U_3 and flying capacitors are used in the model. For 5L-HC-E scheme, the conductance values of U_1, U_2 and U_3 are used. These values are reduced to the half of the parameters shown in Table. III to show the device degradation. For 5L-HC-2E scheme, voltage ripples of U_1/ U_3 and flying capacitors become large, however, these ripples are
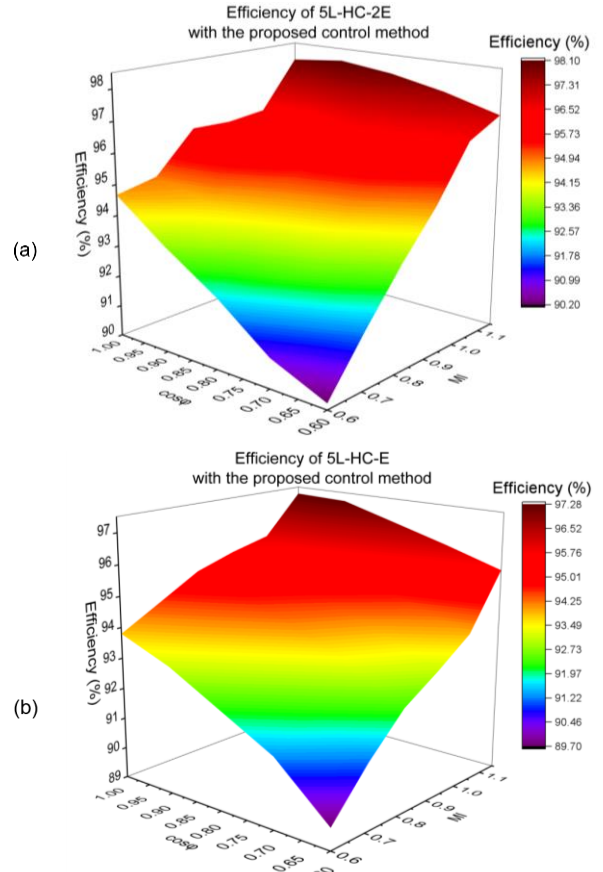
TABLE V
EFFICIENCY RATIO OF 5L-HC-2E WITH POD AND WITHOUT POD

	PF=0.6	PF=0.7	PF=0.8	PF=0.9	PF=1.0
MI=0.6	1.0137	1.0081	1.0095	1.0077	1.0059
MI=0.7	1.0084	1.0090	1.0069	1.0061	1.0054
MI=0.8	1.0065	1.0069	1.0036	1.0120	1.0054
MI=0.9	1.0051	1.0072	1.0054	1.0059	1.0076
MI=1.0	1.0061	1.0050	1.0089	1.0045	1.0090
MI=1.15	1.0033	1.0028	1.0026	1.0025	1.0024

TABLE VI
EFFICIENCY RATIO OF 5L-HC-E WITH POD AND WITHOUT POD

	PF=0.6	PF=0.7	PF=0.8	PF=0.9	PF=1.0
MI=0.6	0.9944	0.9978	0.9963	0.9982	0.9978
MI=0.7	0.9940	0.9959	0.9963	0.9953	0.9957
MI=0.8	0.9963	0.9968	0.9962	0.9960	0.9965
MI=0.9	0.9920	0.9931	0.9945	0.9933	0.9948
MI=1.0	0.9927	0.9932	0.9937	0.9949	0.9942
MI=1.15	0.9979	0.9975	0.9967	0.9973	0.9963

still less than 1.5% and 0.5% for U_1/ U_3 and flying capacitors respectively. For 5L-HC-E scheme, voltage ripples of U_1/ U_3 are increased, but are still only about 5%. It is shown that the proposed closed-loop control method has the self-adaptation ability to the parameter deviations.

V. EXPERIMENT VERIFICATION

Experiments have been done with a downscaled prototype to verify the control effectiveness for two inverters with the parameters in Table VII. The hardware for one phase is shown in Fig. 20(a). The control board consisting of DSP
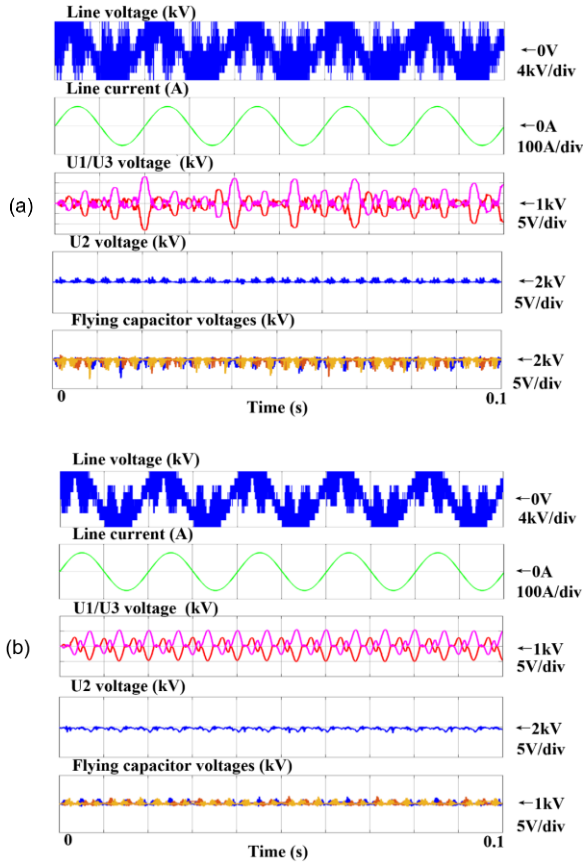
Fig. 19. Operations at MI=1.15 and PF=0.999 with parameter deviations of (a) 5L-HC-2E. (b) 5L-HC-E.

(TMS320F28335) and FPGA (Xilinx XC3S400) is shown in Fig. 20(b). Switches are MOSFET (C2M0160120D) from Wolfspeed.

TABLE VII
PARAMETERS OF EXPERIMENT

Parameters	Value
DC-link Voltage V_{dc}	200V
Carrier Frequency f_{sw}	5kHz
Fundamental Frequency f_0	50Hz
DC-link Capacitors	C1=C3=1.47mF, C2=1mF
Flying Capacitors	C4=1mF
Modulation Index	0-1.15
Power Factor φ	0-1
Passive Load	33ohms, 3.68mH (±10%) per phase ($\cos\varphi = 0.999$)

The operation of two inverters with MI=0.92 are shown in Fig. 21. Both line voltages have the desired level number. DC-link capacitor voltage ripples are maintained within $\pm2\%$ of the reference value. FC voltage ripples of 5L-HC-2E and 5L-HC-E schemes are about 4% and 8% respectively. CMV with and without POD of two examples are shown in Fig. 22. The percentage of CMV between $\pm33V$ is increased with POD for both topology schemes. Conclusion can been made that CMV is mitigated with POD although improvement can be made. Performance of two inverters with unequal load is shown in

Fig. 23. Resistors at three phases are 50Ω, 33Ω and 20Ω respectively. Capacitor voltages are maintained well within the desired range.

Fig. 24 shows the dynamic balancing process of two inverters. All capacitor voltages are set manually unbalanced and then get balanced by the proposed control method. The balancing ability
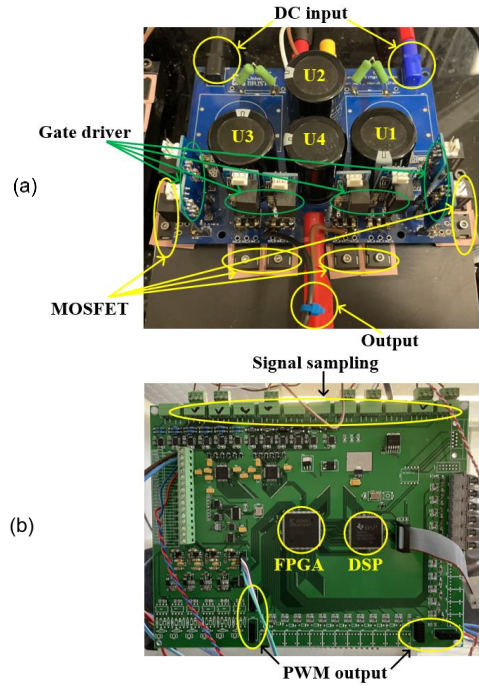

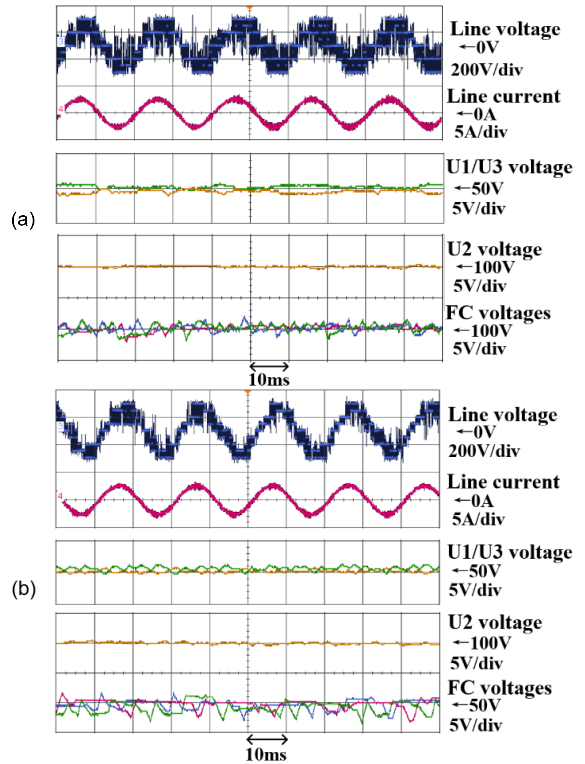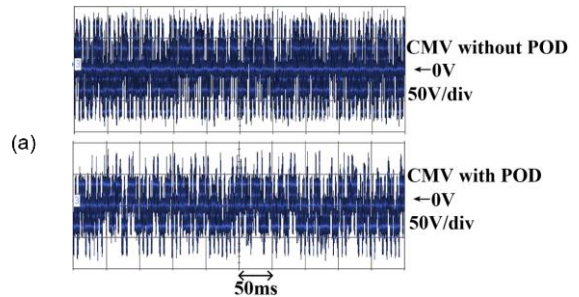Fig. 20. Experiment prototype. (a) One phase hardware. (b) Control board.

Fig. 21. Experiment performance with steady state at MI=0.92 of (a) 5L-HC-2E. (b) 5L-HC-E.
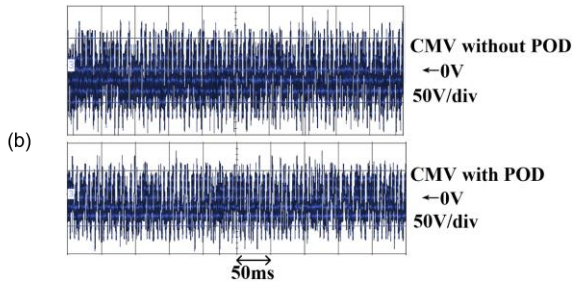
Fig. 22. Common mode voltage with and without POD in experiment of (a) 5L-HC-2E. (b) 5L-HC-E.
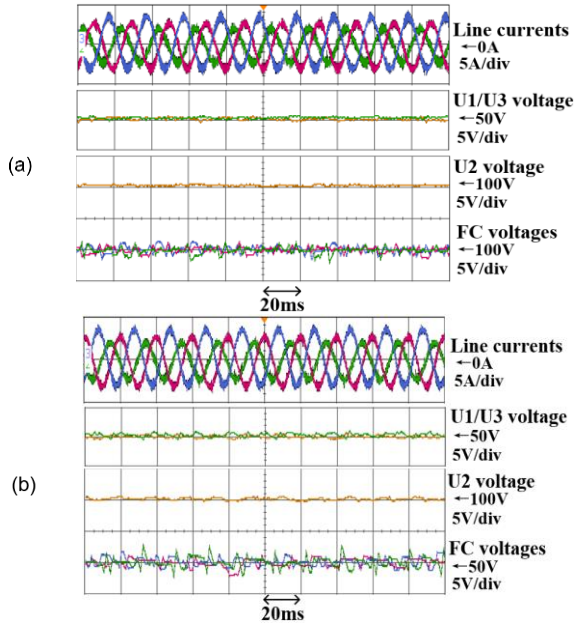

Fig. 23. Experiment performance with unequal load at 50Ω, 33Ω and 20Ω of (a) 5L-HC-2E. (b) 5L-HC-E.
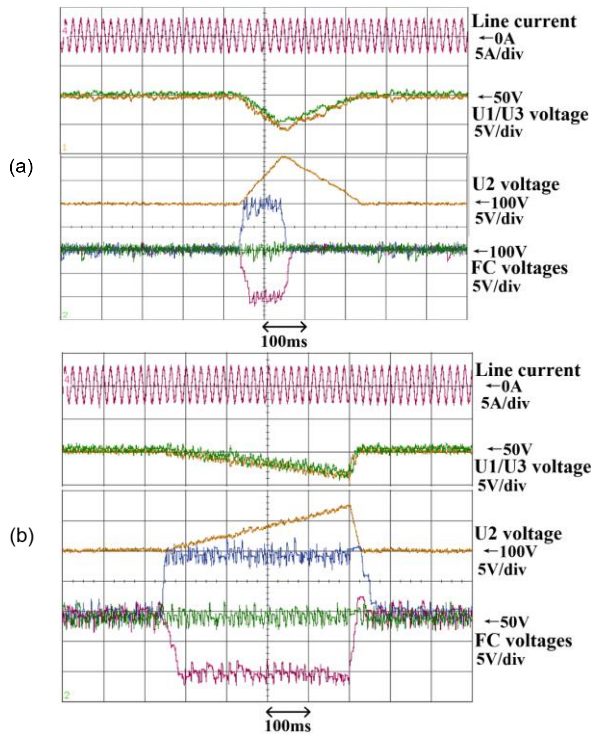

Fig. 24. Dynamic experiment performance with capacitor voltage unbalance of (a) 5L-HC-2E. (b) 5L-HC-E.
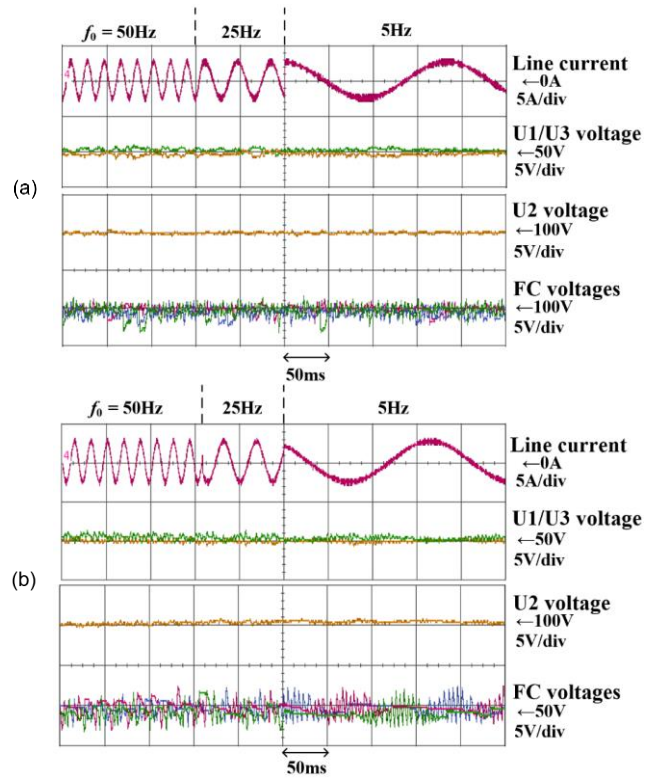
Fig. 25. Dynamic experiment performance with variable fundamental frequencies, 50Hz, 25Hz and 5Hz, of (a) 5L-HC-2E. (b) 5L-HC-E.

Fig. 26. Dynamic experiment performance with variable modulation indexes 0.92 and 0.3 of (a) 5L-HC-2E. (b) 5L-HC-E.
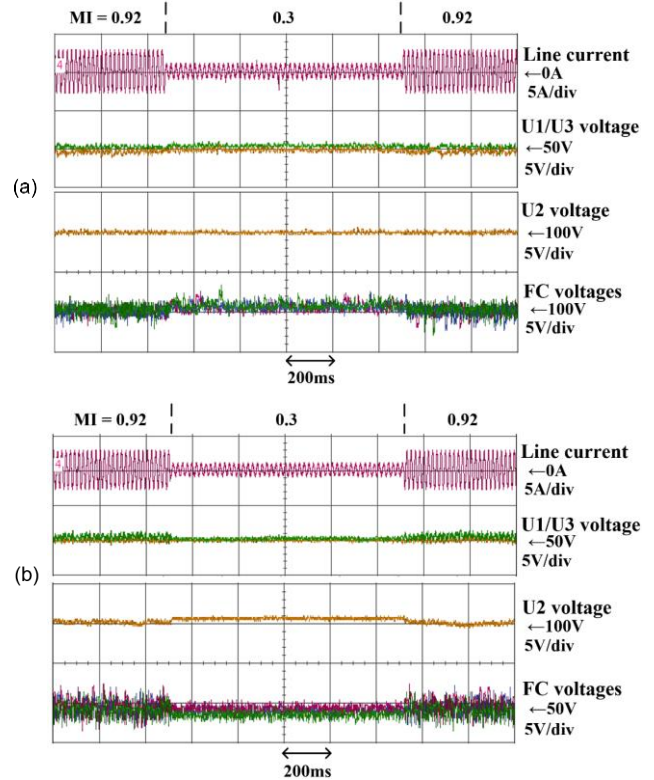
of U_1/ U_3 voltages in 5L-HC-2E scheme is weaker than that in 5L-HC-E scheme. FC voltages are maintained balanced during the manual voltage change.

Fig. 25 shows the performance of two topology schemes

Fundamental (50Hz) = 2.689 , THD= 10.10%

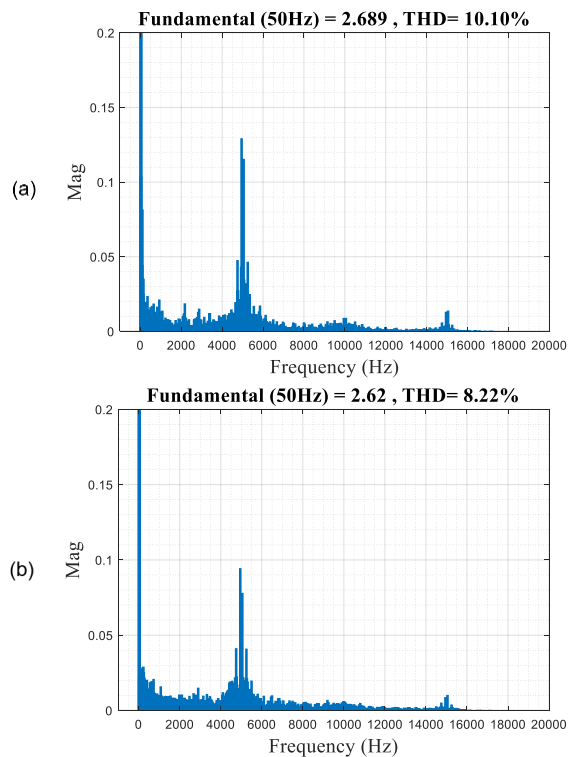**Fundamental (50Hz) = 2.62 , THD= 8.22%**

Fig. 27. FFT analysis of current waveforms in experiment of (a) 5L-HC-2E. (b) 5L-HC-E.

when f_0 decreases from 50Hz to 5Hz with MI=0.92. Since all capacitors maintain balanced, the algorithm is proven to be effective for both topology schemes under variable f_0. Fig. 26 shows the balancing process of two example schemes when MI changes between 0.92 and 0.3. Capacitor voltage ripples become larger when MI is larger.

Fig. 27 shows the FFT analysis results of currents in experiments. The THD values are 10.1% and 8.22% for 5L-HC-2E and 5L-HC-E schemes respectively.

VI. CONCLUSION

In this article, a control method combining four degrees of modulation freedom in carrier-based PWM, switching state selection, zero-sequence signal injection, redundant level modulation and phase opposition disposition, is utilized to balance two five-level inverters as examples and mitigate the common-mode voltage at the same time within full range of modulation indexes and power factors and variable fundamental frequencies. The function of four degrees of modulation freedom is explained comprehensively in this article. POD is proven to have no harm to other metrics. Power loss analysis is provided with the operational conditions when RLM is needed. Average CMV and the number of high dv/dt are reduced. The reduction is also shown in the frequency domain. This method is based on fully analytical model without PI-controllers and the calculation process is relatively simple and easy to understand. It is proven that the proposed method can adapt to the component deviations. The effectiveness of the control method has been verified in both simulation and downscaled experiments of two examples with different operational conditions.

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