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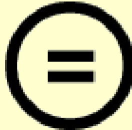

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Ph.D. DISSERTATION

Study on Noise in Metal Oxide-Based RRAM and Its Application

금속산화물 기반 저항변화메모리 소자의 노이즈 특성과 그것의 응용에 관한 연구

by

JUNGKYU LEE

February 2023

DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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Study on Noise in Metal Oxide-Based RRAM and Its Application

by

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the requirements for the degree of

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ABSTRACT

In the current pyramid-like structure's memory hierarchy, it consists of, from top to bottom, a processing core, cache memory by static random access memory (SRAM), main memory by dynamic random access memory (DRAM), and storage memory by solid-state disk (SSD), or hard disk drive (HDD). In general, the closer to the processing core, the more high-speed operation is required, whereas the farther away from the core, the higher storage capacity is demanded. Consequently, the performance gap between DRAM and NAND Flash memory, which are currently major memory technologies, is continuously increasing. However, the need for new memory technology is increasing in order to solve the problem of data processing speed due to the explosive increase in the amount of data and the physical limitation of the existing memory technologies that has been raised for a long time. In addition, research and development on the storage class memory (SCM) technology is in progress as method of implementing In-Memory Process, a concept to solve the problem of Von Neumann architecture in various research groups.

Among the candidates on the SCM, which satisfies both the high speed of DRAM and the density of NAND Flash, the resistive switching random access memory (RRAM) has been widely investigated as a leading candidate for next

generation nonvolatile memory applications due to RRAM's advantageous features such as simple structure, low cost, high density, fast operation, and CMOS compatibility. However, the reliability issues which PCM suffered from is also being reproduced in RRAM. RRAM's various issues such as endurance, retention, and uniformity stem from intrinsic variability because resistive switching mechanism of RRAM itself is fundamentally stochastic.

The main content of this dissertation is to develop a new electrical analysis technique to improve the reliability of RRAM.

First, the elementary low frequency noise (LFN) characteristics of various RRAM devices were analyzed, and the correlation between LFN characteristics and the conduction/resistive switching mechanisms was experimentally verified.

Also, it was suggested that the LFN measurement can be an additional analysis technique for device's degradation mechanism and multi-level cell (MLC) operation.

Finally, from the random telegraph noise (RTN) measurement, we conducted a study to extract the position and energy of traps that can cause cell's failure. The experiment on the extraction of trap's physical information using the RTN measurement was conducted for the first in this study, and then research findings provided researchers with guidelines for the RTN analysis of RRAM.

Keywords: Resistive switching memory, conduction mechanism, reliability, low frequency noise, RTN

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Chapter 1

Introduction

1.1 Memory trends

1.1.1 Memory wall

In order to apply information and communication technology (ICT) such as artificial intelligence (AI), augmented reality (AR), virtual reality (VR), self-driving to our daily life, it is expected that data will be generated three times more than the current level [1-3]. Also, as services including telecommuting, web conference, and streaming have proliferated around the globe due to COVID-19, data usage would be further increase. According to the statistics from international data corporation (IDC), the total amount of global data is expected to reach to 175 ZB by 2025 [4]. So, if the demand for memory performance and capacity surges due to the explosive increase in data, the "memory wall" between DRAM and NAND flash memory, which are the current major memory technologies, will also

reach an extreme [5-7]. In addition, current AI technology is hampered by the hardware bottleneck rather than software problems. To make full use of deep learning AI technologies, it is ideal for the CPU to communicate directly with the main memory, which can store the learning model and learning data departing from the traditional computer structure [8-10]. Fig 1.1 shows the pyramid-like structure's memory hierarchy [11]. From top to bottom, it is composed of the processing core, cache memory (SRAM), main memory (DRAM), and storage memory (NAND flash or HDD). In general, the closer to the processing core, the more high-speed operation is required, whereas the farther away from the core, the higher storage capacity is demanded. In the era of big date, the main issues of the current memory hierarchy in the big data era can be summarized in the following two categories [12-14].

- Growing gap in capacity and speed of main memory and storage memory.
- High power consumption of core, cache and main memory because they are based on volatile memory technologies.

Therefore, in order to solve the "memory wall" caused by the performance gap

between DRAM and NAND flash memory, there is an increasing need for the universal memory that can implement the functions of storage memory (high density and non-volatile) and working memory (high speed) at the same time [1,15,16].

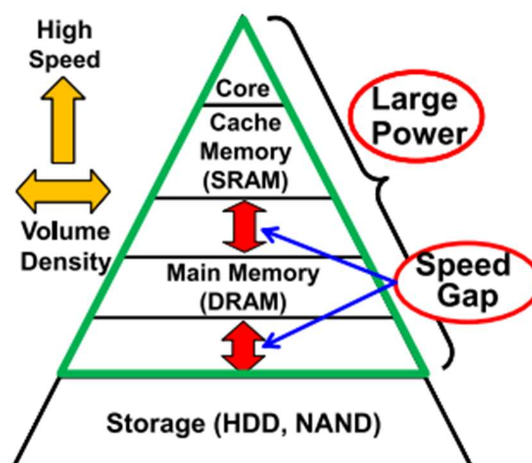


Fig. 1.1. Example of memory hierarchy in an ICT system [11].

1.1.2 In-memory processing

In-memory processing, namely, computing at the site where data is stored is considered as one of the ultimate solutions. This new computing architecture does not require data movement costs, and is expected to completely break the

limitations of the memory wall by high-throughput in situ data processing [17-19]. To meet aforementioned memory market's demands and in-memory processing, the concept of storage class memory (SCM) was introduced [20-22]. By definition, SCMs should be typically non-volatile memories (NVM), and should provide performance comparable to or better than that of the main memory. The promising candidates of SCM technologies are phase change memory (PCM), magnetic memory (MRAM), ferroelectric memory (FeFET), and resistive memory (RRAM).

1.2 SCM technologies

1.2.1 Phase change memory

After the concept of SCM was introduced, phase change memory (PCM) is a representative example of the realizing the potential of SCM for the first time. Fig 1.2 shows the schematic view of PCM cell and programing schemes of the device [23]. PCM is based on the reversible transition between crystalline phase and amorphous phase of the chalcogenide alloy. The most representative material is an alloy of Ge-Sb-Te (GST). The resistance of GST can be changed by the current

flow through the material between the amorphous state (high resistance) and the crystalline state (low resistance). PCM is among the most developed novel NVMs and has demonstrated remarkable performances such as the switching speed and the cycle endurance. Also, PCM has generally good CMOS-compatibility [16,23]. The key challenges of PCM are the relative poor access latency and the high programming current [24,25].

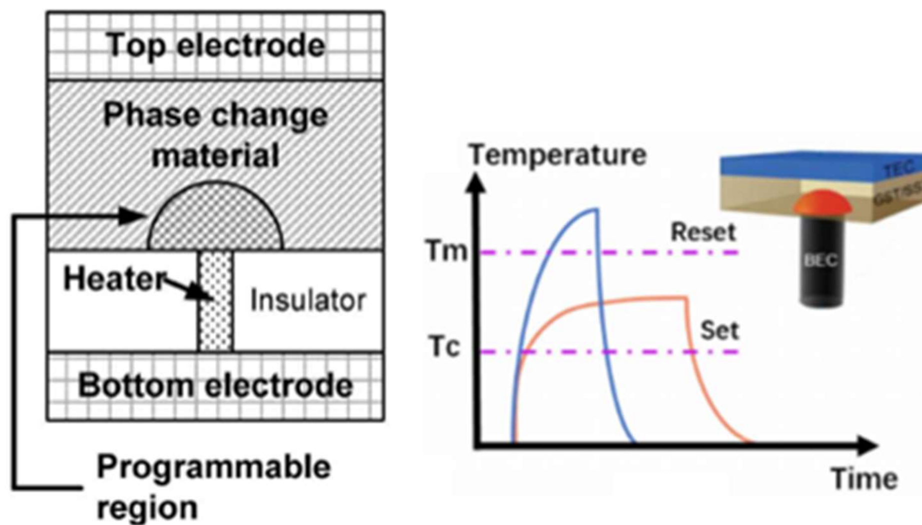


Fig. 1.2. Schematic view of PCM cell and programing schemes of the cell [23].

1.2.2 Magnetic memory

A magnetic memory is based on the magneto-resistive effect in thin films. The film called a magnetic tunnel junction (MTJ) is the memory element, which consisting of thin tunnel barrier sandwiched between two magnetic layers in series with an access transistor as shown in Fig. 1.3 [26]. The resistance difference between the parallel configuration and the anti-parallel configuration of the two ferromagnetic layers in the MTJ determines the resistance state. The advantages of magnetic random access memory (MRAM) are fast switching speed compared to other nonvolatile memories, with 1~10 ns read and write erase times and very good endurance (up to 10^{15} cycles) [11,16,26]. Nevertheless, MRAM still have some critical challenges. Small on/off current ratio compared to the other emerging memories is one major concern. Also, precise deposition and etching of the MTJ are required because MRAM's characteristics are highly sensitive to the fabrication process. fabrication process is complicated [27-29].

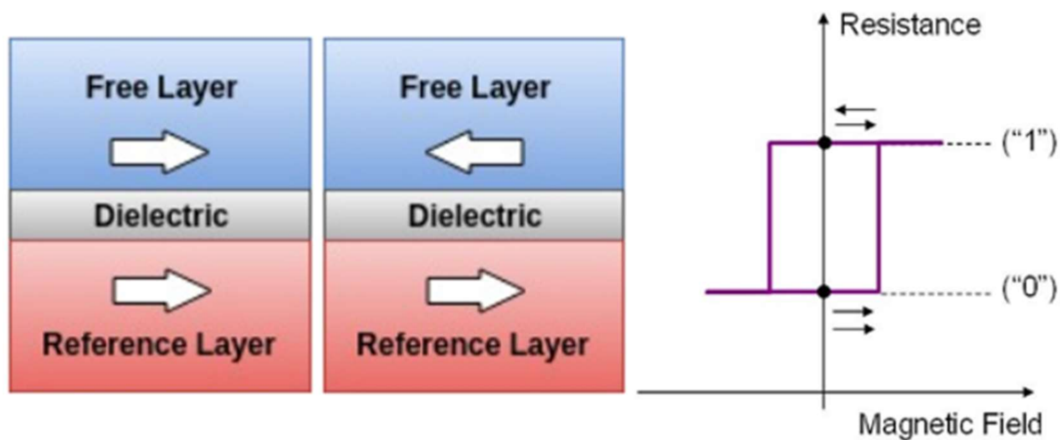


Fig. 1.3. Schematic drawing of a typical magnetic tunnel junction memory element and corresponding memory states [26].

1.2.3 Ferroelectric memory

A ferroelectric field-effect transistor (FeFET) is a type of field-effect transistor that includes a ferroelectric material sandwiched between the gate electrode and source-drain conduction region of the device (the channel) as shown in Fig.1.4 [30]. Permanent electrical field polarization in the ferroelectric causes this type of device to retain the transistor's state (on or off) in the absence of any electrical bias. The merits of FeFET (especially FeFET based on HfO2) are fully CMOS-compatible processes, simple 1-transistor (1T) structure, and the performance close to that of

DRAM [16,30,31]. However, the degradation of the interface layer between the ferroelectric and the semiconductor channel causes the reliability issues, in particular, due to trapped charge that affects the conduction of the FET below the ferroelectric [1,32].

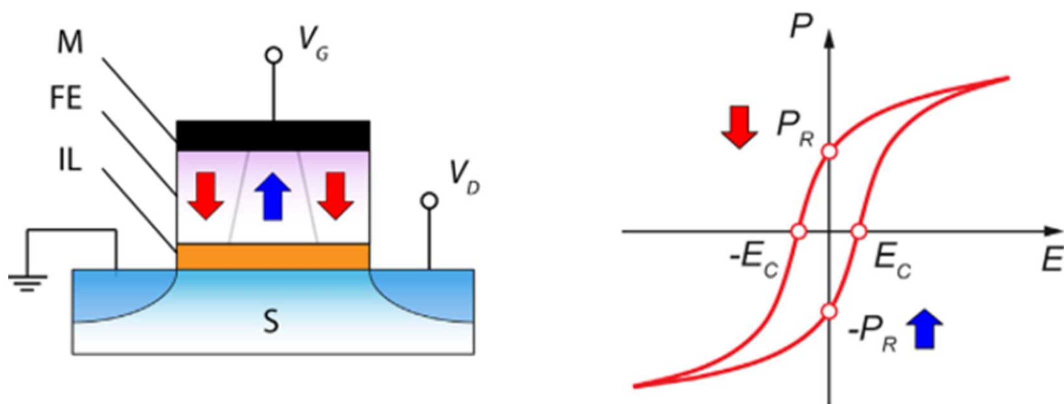


Fig. 1.4. Schematic structure of the MFIS FeFET and the *P*-*E* hysteresis curve [30].

1.2.4 Resistive memory

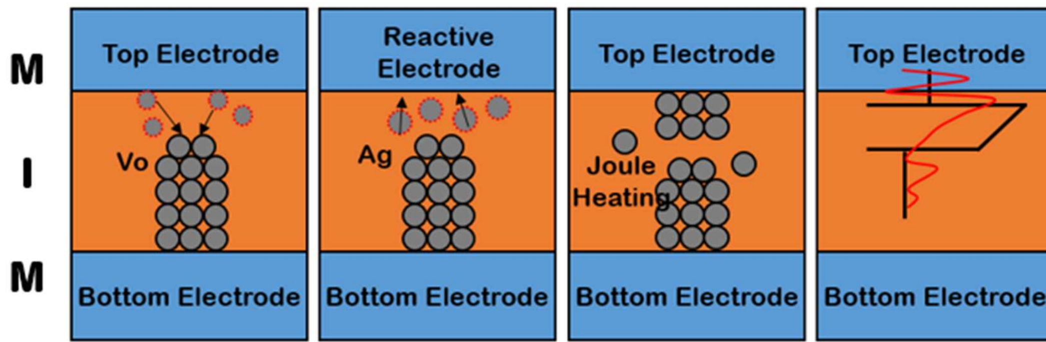
RRAMs are based on a simple metal-insulator-metal (MIM) structure as shown in Fig.1.5 (a). Reversible chemical and structural changes induced by reaction in response to electrical stimuli leads to resistive switching (RS) effects in MIM

structures. Fig. 1.5 (b) shows the basic operation of RRAM [33]. By applying an appropriate voltage across the electrodes, the resistive switching layer (insulator) can be switched between a high-resistance state (HRS) and a low-resistance state (LRS). These two states represent the digit ‘0’ and the ‘1’, respectively. The RS properties of materials originate from a large variety of physical and chemical phenomena. However, the mechanisms underpinning resistive switching are still not fully understood. To understand RS mechanisms of RRAM devices, many research groups have investigated RRAM over the past decade, and now they are classified according to the working principle as follows [33-36]. Commonly used terminologies are thermochemical mechanism (TCM), valence change mechanism (VCM), and electronic/electrostatic mechanism (EEM). The switching mechanisms for each of RRAMs are as follows.

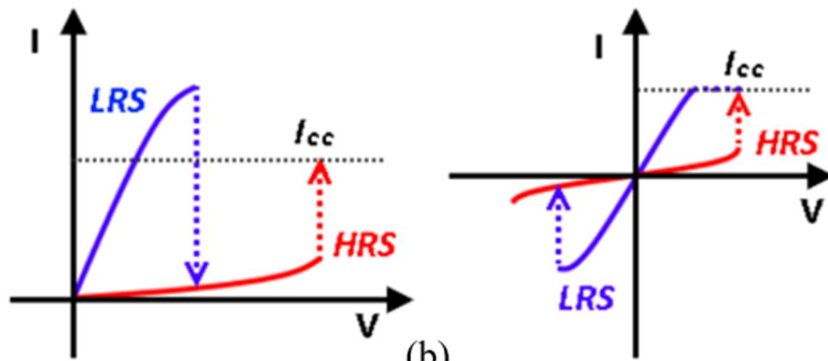
- TCM: TCM RRAM is based on thermally induced stoichiometry variations and redox reactions. The formation of conductive filaments (CF) in the switching layer corresponds to thermal decomposition by Joule heating, and the rupture of CFs is a thermal melting phenomenon by Joule heating.

- VCM: VCM RRAM is based on the formation and rupture of the CF, which consists of oxygen vacancies. The principle of RS is basically the redox-reaction between oxygen ions and oxygen vacancies in the metal oxide under an electric field.
- EEM: EEM RRAM, also called interfacial RRAM or non-filamentary RRAM, is based on the tunnel barrier modulation effect at the interface of the metal/switching layer through the migration of oxygen ions. Unlike CF RRAM, an additional oxide layer is present to act as a load resistor, which eliminate the need for the current compliance.

RRAMs have the simple 2-terminal MIM structure, which allows excellent scalability and easy 3D integration. Also, RRAM devices use fully CMOS compatible materials and can be fabricated using fab-friendly processes [16].



(a)



(b)

Fig. 1.5. (a) Simple MIM structure and (b) basic operation of RRAM devices [33].

1.3 Thesis content overview

1.3.1 Thesis objectives

Since the mid-2000s, many research groups have fabricated and studied RRAMs with various materials and structures, but the problems caused by the intrinsic variability of RRAM remains unresolved. In this work, we aim to develop a new electrical analysis technique to improve the reliability of RRAM. First, we investigate the basic noise characteristics through LFN measurement of RRAM, and then prove that LFN can be utilized in RRAM operation analysis. In addition, the correlation between the conduction mechanism and LFN characteristics in RRAMs is verified through experimental study. Based on the results proven through various devices, we propose that the LFN measurement can be a valuable analytical technique to clarify the physical mechanism associated with the RS phenomenon of RRAM. Additionally, by analyzing RTN characteristics, which is one of the LFN of semiconductor devices, we propose a methodology for RTN analysis in RRAMs.

1.3.2 Thesis outline

The structure of this dissertation is as follows: Chapter 1 provides an introduction of various types of RRAM, its RS mechanisms, and the prospect of RRAM as the SCM. Chapter 2 provides an overview on conduction mechanisms in dielectric films. Chapter 3 cover how LFN measurements are used for RRAM analysis such as indirect confirmation of filament, MLC operation, and failure mechanism. Chapter 4 offers the result of analyzing the conduction mechanism of RRAMs using the LFN measurement. thermochemical mechanism (TCM), valence change mechanism (VCM), and electrostatic mechanism (EEM) type of RRAMs are used for verification. Chapter 5 discusses the methodology to extract the position and energy of traps that can cause cell's failure. Finally, in Chapter 6, the conclusion of this thesis is summarized.

Chapter 2

Overview on conduction mechanisms

2.1 Electrode-limited conduction mechanisms

The electrode-limited conduction mechanisms depend on the electrical properties at the electrode/dielectric contact. The representative mechanisms are Schottky or thermionic emission, Fowler-Nordheim (F-N) tunneling, and direct tunneling (Fig. 2.1). In these conduction mechanisms, the energy barrier height at the electrode/dielectric interface is the most important parameter, which determines the current flow [37].

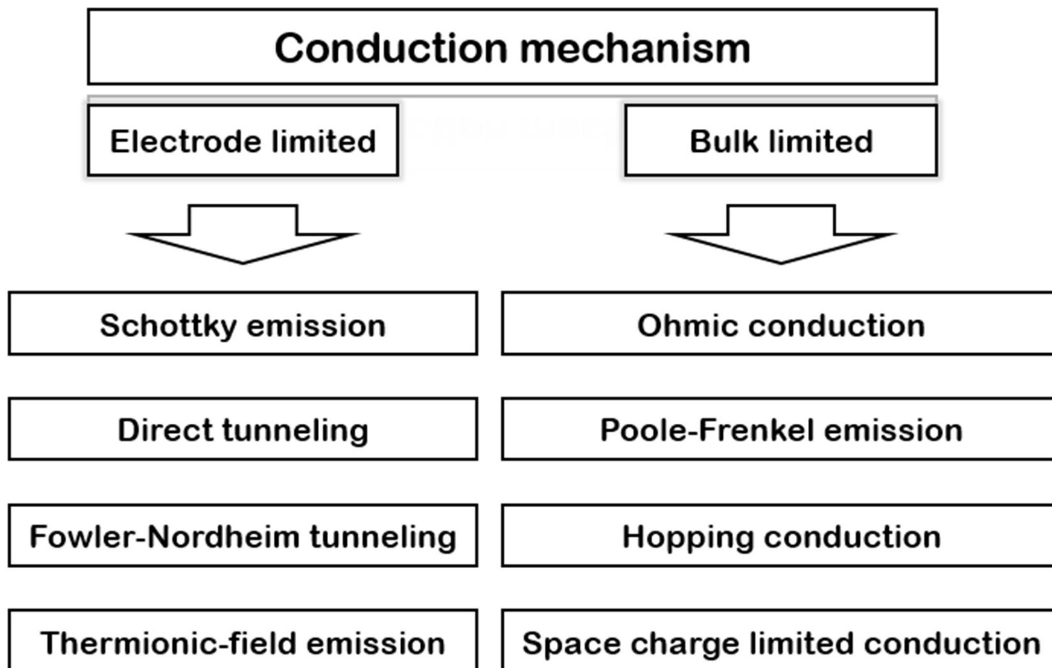


Fig. 2.1. Classification of conduction mechanisms in dielectric films.

2.1.1 Schottky emission

The Schottky or thermionic emission occurs when thermally-activated carriers injected over the energy barrier into the conduction band of the dielectric as shown in Fig. 2.2 (a) [38]. This mechanism is one of the most often observed conduction mechanism in dielectric films, especially at relatively high temperature. The current density is given by equation (1) [33]:

$$J = A^{*}T^{2}exp\left(\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_o}\right)}{kT}\right), \tag{1}$$

where J is the current density, A^{*} is the effective Richardson constant, T is the absolute temperature, q is the magnitude of the electronic charge, $q\phi_B$ is the Schottky barrier height without image-force lowering effect, E is the electric field across the dielectric, k is Boltzmann's constant, ε_r is the dynamic dielectric constant, and ε_o is the permittivity of free space.

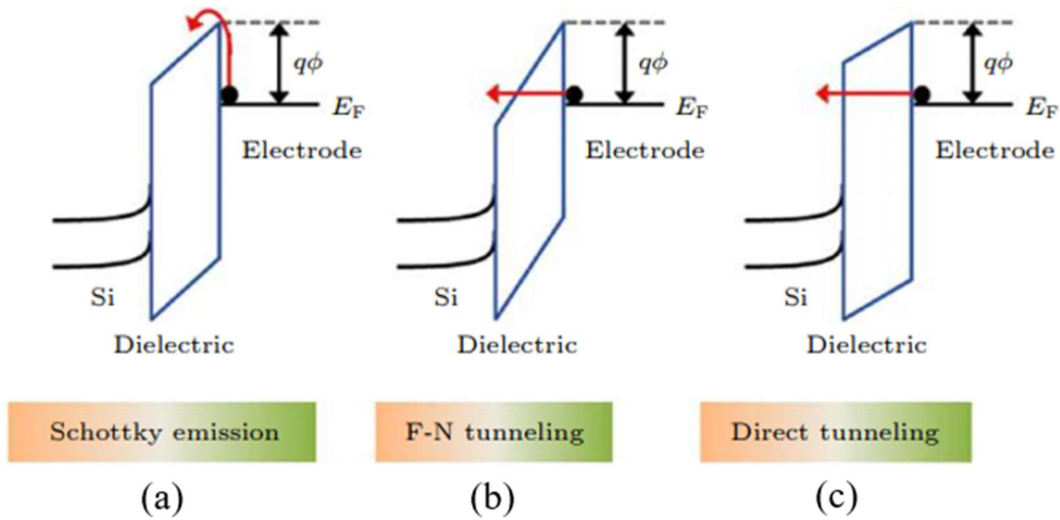


Fig. 2.2. Schematic energy band diagrams of (a) Schottky emission, (b) F-N tunneling, and (c) Direct tunneling [38].

2.1.2 Fowler-Nordheim (F-N) and direct tunneling

Fig. 2.2 (b) shows the schematic energy band diagram of F-N tunneling. F-N tunneling happens when the applied bias is sufficiently large so that the band bending of the dielectric film becomes very large, and electrons may penetrate through the triangular band edge into the dialectic. F-N tunneling current density can be expressed as equation (2) [33]:

$$J = \frac{q^2}{8\pi h\phi_B} E^2 exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE} \phi_B^{3/2}\right), \tag{2}$$

where m^* is the tunneling effective mass in dielectric and h is Planck's constant. The other notations are the same as defined before. Direct tunneling occurs when the dielectric film is thin enough so that electrons can tunnel across directly at low bias as shown in Fig. 2.2 (c). Generally, direct tunneling is more dominant in oxide thinner than 3 nm, and F-N tunneling dominates at thicker oxide. Direct tunneling can be approximated to equation (3) [33]:

$$J \approx exp\left(\frac{-8\pi\sqrt{2q}}{3h} (m^*\phi_B)^{1/2} \kappa \cdot t_{ox,eq}\right), \tag{3}$$

where κ is the relative dielectric constant of the oxide layer and $t_{ox,eq}$ is the equivalent oxide thickness (EOT).

2.2 Bulk-limited conduction mechanisms

The bulk-limited conduction mechanisms depend on the electrical properties at the dielectric itself, which include Poole–Frenkel (P–F) emission, hopping conduction, Ohmic conduction, and space charge limited conduction (SCLC) (Fig. 2.1). In these conduction mechanisms, several important physical parameters are the trap energy level, the trap spacing, the trap density, the dielectric relaxation time, the carrier drift mobility, and the density of states in the conduction band [37].

2.2.1 Poole-Frenkel (P-F) emission

P-F emission happens when electrons trapped in localized states of the dielectric is excited into the conduction band of the dielectric. The applied electric field decreases the Coulomb potential energy in a trap center, hence the probability of an electron being thermally excited out of the trap increases. Fig. 2.3 (a) shows the schematic energy band diagram of P-F emission. The current density can be expressed as equation (4) [33]:

$$J = q\mu N_c E exp\left(\frac{-q\left(\phi_T - \sqrt{qE/\pi\varepsilon_r\varepsilon_o}\right)}{kT}\right), \quad (4)$$

where μ is the electronic drift mobility, N_c is the density of states in the conduction band, and ϕ_T is the trap energy level.

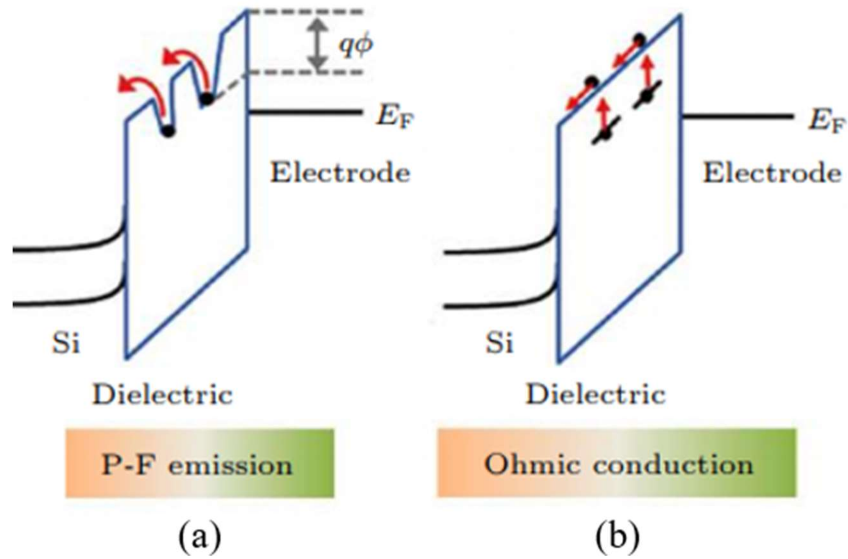


Fig. 2.3. Schematic energy band diagrams of (a) P-F emission and (b) Ohmic conduction [38].

2.2.2 Ohmic conduction

Ohmic conduction is caused by the movement of mobile carriers in the band due to thermal excitation. Fig. 2.3 (b) shows the schematic energy band diagram of

Ohmic conduction. Although the energy band gap of dielectric is large by definition, there are a small number of mobile electrons which is excited to the conduction band, either from the valence band or from the impurity level. These electrons attribute to Ohmic conduction. This current is generally observed at very low field in the dielectric and the current density of Ohmic conduction can be expressed as equation (5) [33]:

$$J = \sigma E = q\mu N_c E exp\left(\frac{-(E_C - E_F)}{kT}\right), \tag{5}$$

where σ is electrical conductivity, μ is the electronic mobility, N_c is effective density of states in the conduction band, E_C is the conduction band, and E_F is the Fermi energy level.

2.2.3 Space charge limited conduction (SCLC)

In RRAM devices, it is often the case that the current exhibits a non-exponential bias dependence. Such a characteristic is found in the SCLC model, which is frequently used to explain the conduction mechanism in RRAM cells [33,39-41]. The SCLC mechanism occurs when current through the insulator becomes limited

by the build-up of charge (Space charge) injected from the source electrode. Especially, trap-controlled SCLC is divided into three regions (Fig. 2.4) [42]. In linear region ($V < V_{tr}$) corresponding to Ohm's law ($I \propto V$), the conduction mechanism is dominated by the thermally generated free electrons in the dielectric film. In square region ($V > V_{tr}$) corresponding to Child's square law ($I \propto V^2$), the density of free electrons injected from the electrode gradually exceeds the equilibrium concentration and excess electrons accumulate in the space between two electrodes. As a consequence, the space charge starts to limit the total current flow. According to the SCLC model [43], the current density can be expressed as equation (6) [33]:

$$J = \frac{9}{8}\varepsilon\mu\theta\frac{V^2}{d^3}, \tag{6}$$

where μ is the electronic mobility, θ is the ratio of free charge carriers to total charge carriers, V is the applied voltage, and d is the film thickness.

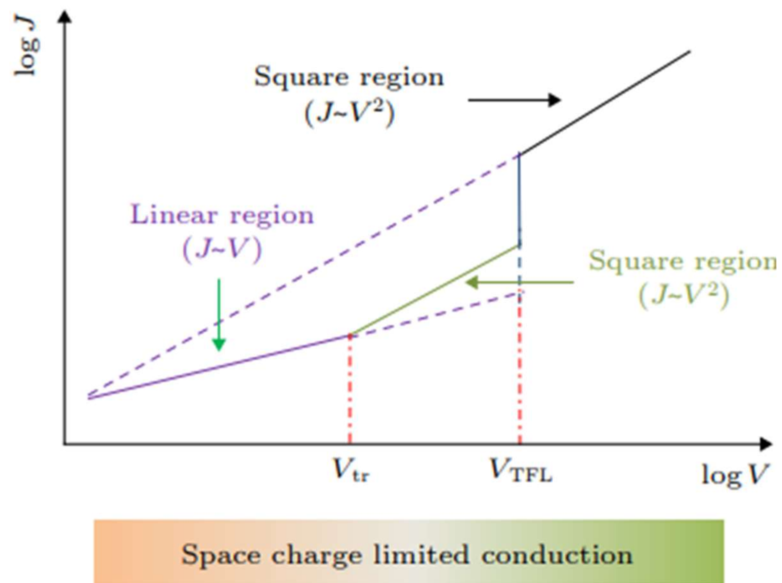


Fig. 2.4. A typical current density-voltage (*I*-*V*) characteristic of the SCLC mechanism. V_{tr} is the transition voltage. V_{TFL} is the trap-filled limit voltage [39].

Chapter 3

LFN applications for RRAM analysis

3.1 Introduction to 1/*f*

The four most common types of the electronic noise are thermal or Johnson noise, shot noise, generation-recombination (G-R) noise, and flicker or 1/*f* noise [44]. Thermal noise stems from the random thermal motion of charge carriers. Shot noise is caused by fluctuations of current across the potential barrier or hetero-interface due to the discrete nature of carriers. Thermal and shot noise types are called white noise because their spectral density does not depend on the frequency. Generation-recombination (G-R) noise in semiconductors originates from traps that randomly capture and emit carriers, thereby causing fluctuations in the number of carriers available for current transport. Another important noise component is flicker noise, also called 1/*f* noise. This type of noise is observed in most semiconductor systems, such as MOSFET, BJT, TFT, LED, MRAM, and RRAM

[45-50]. For this reason, no well-defined process or mechanism exists to account for all 1/*f* noise in various systems. The origin of 1/*f* noise is still a point of debate and often explained by two schools of thought: noise related to mobility fluctuations ($\Delta\mu$), and noise related to carrier density fluctuations (Δn). In the 1950s, McWhorter suggested that 1/*f* noise is caused by charge carrier number fluctuations at the interface between the semiconductor and oxide [51]. The number fluctuation model considers the 1/*f* noise origin to be the trapping/de-trapping-induced number fluctuation of channel carriers, primarily at the Si-SiO2 interface. Especially, this model has been successful in explaining the 1/*f* noise in MOS-transistors. In the 1960s, Hooge proposed a universal empirical relation from a number of noise measurements in metals and bulk semiconductors [51]. The basic concept behind the Hooge's empirical model is that carrier scattering by lattice vibrations cause fluctuations in mobility of the charge carriers.

The absence of a single mechanism to account for 1/*f* noise complicates the introduction of a figure of merit for 1/*f* noise. However, Hooge's empirical model has been used extensively to explain 1/*f* noise in MOSFET, diode, MRAM,

graphene FEF, etc. [45,49,52,53]. In addition, it has been used as a basic model when deriving 1/*f* noise model formulas for various conduction mechanisms such as Ohmic, Schottky emission, P-F emission and SCLC [52,54-56]. The most commonly used noise model equations for each mechanism are summarized in Fig. 3.1(a). From equations (7), (8), (9), and (10) in Fig. 3.1(a), we can predict the bias dependence of 1/*f* noise depending on the conduction mechanism. Fig. 3.1(b) shows the expected results of the noise power spectral density (S_i) corresponding to each conduction mechanism based on the noise model equation. For example, in case of Schottky emission, the S_i is proportional to I^2. In chapter 4, we use the 1/*f* noise characteristics when analyzing the conduction mechanism in RRAM devices. Based on the measurement results of various experimental devices, it will be proved that LFN characteristics are an effective technique for more accurately analyzing the conduction mechanism of RRAM devices.

(a)

Conduction mechanism	Expression	
Ohmic	$\frac{S_I}{I^2} = \frac{\alpha_H}{fN}$	(7)
SCLC	$\frac{S_I}{I^2} = \frac{4\alpha_H qL}{5A\varepsilon\theta fV}$	(8)
Schottky emission	$S_I = \frac{\alpha_H}{fN_d exp(-qV_{bi}/k_B T)AL_D}\frac{v_r}{(2D_n/L_D)}I^2$	(9)
P-F emission	$S_I = \frac{0.1N_d\beta^2}{\varepsilon^2 EWL}\frac{q^2}{f}I^2$	(10)

α_H: Hooge parameter, f: frequency, N: total number of free charge carriers, q: elementary charge, W: width, L: length, A: area, ε: permittivity, θ: effective mobility parameter, v_r: recombination velocity, D_n: electron diffusion constant, V_{bi}: built-in voltage, k_B: Boltzmann constant, L_D: Debye length, N_d: donor/trap density, β: P-F fitting parameter

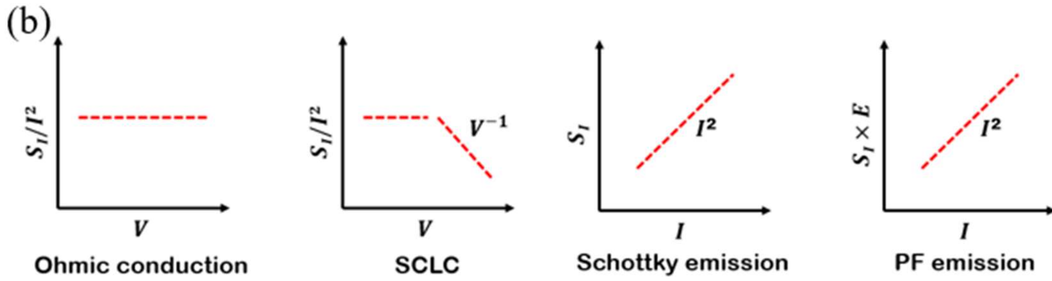


Fig. 3.1. (a) Conduction mechanism and its corresponding 1/f noise model. (b) Bias dependence of the current noise spectral density according to 1/f noise model.

3.2 LFN application (1): Resistive switching analysis

In order to analyze the resistive switching (RS) mechanism of the RRAM device from the LFN measurement, we first compare the normalized noise power spectral density (S_i/I^2) in two resistance states of the RRAM, the HRS and the LRS.

Fig. 3.2(a) shows the *I-V* characteristic of our experimental device (TiN/Ti/TiO_2/TiN VCM RRAM). Our VCM RRAM is based on the formation and rupture of the CF as shown in right inset of Fig. 3.2(a). Fig. 3.2(b) shows the S_i/I^2 for several devices in both resistance states (HRS and LRS). The normalized noise power measured in the HRS is about 10 times higher than that in the LRS. The difference in noise levels according to resistance states can be analyzed by referring to the schematic diagram in Fig. 3.2(c). Electrons are disturbed by various noise sources, such as lattice, impurity and columbic scattering, on the movement path, and it appears as a weighted sum as current variation and noise component [45]. In the LRS, only the noise component due to the localized path formed in the metal oxide exists, but in the HRS, it can be seen that the noise components due to the various current paths within the broken gap are added, as shown in Fig. 3.2(c). Therefore, the noise level in the HRS becomes larger. Additionally, in the LRS, the noise level does not change even if the device size is reduced, but in the HRS, that increases as the size decreases, which is a typical bulk effect characteristic. Fig. 3.2(d) shows the *I-V* characteristic of the interface-type RRAM

($TiN/Ti/TiO_2/HfO_2/TiN$ EEM RRAM). Unlike the CF-type RRAM, there is no change in the noise level depending on the resistance state in the interface-type RRAM, as shown in Fig. 3.2(e). Also, like the HRS of the CF-type, it has a bulk effect characteristic in which the noise level increases as the size decreases. From the LFN measurement, it is possible to indirectly confirm the configuration of the oxygen vacancy inside the RRAM according to the resistance states, and distinguish between the CF- and the interface-type. In addition, we present guidelines for noise sources according to resistance state or resistive switching mechanism of RRAMs, as shown in Fig. 3.3. For example, in MOSFETs, S/D contact noise can become dominant at high drain current level, and in TFTs, the noise source may be varied from the bulk to the interface with decreasing channel length [45,47]. Similarly, in the CF-type RRAM, localized oxygen vacancy is a dominant noise source in the LRS, and the noise characteristic of the HRS state is the bulk effect. Also, in the interface-type RRAM, the noise characteristics of both resistance states are the bulk effect.

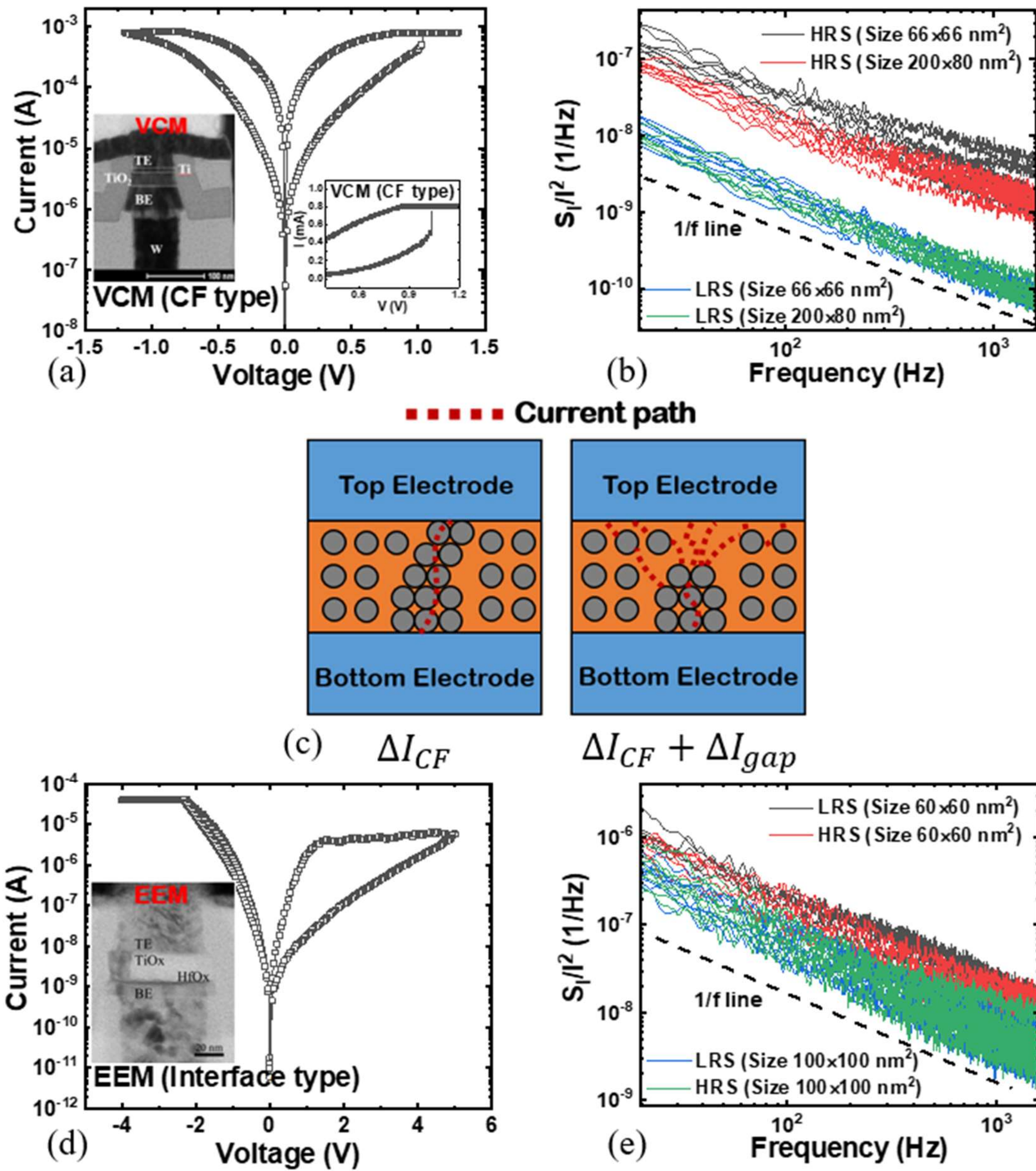


Fig. 3.2. (a) *I-V* characteristic and (b) S_i/I^2 of the CF-type RRAM. (c) Schematic illustration explaining the difference in noise level between the two resistance states. (d) *I-V* characteristic and (e) S_i/I^2 of the interface-type RRAM.

	MOS		TFT		RRAM
Low I_D	Channel	Long channel	Bulk effect /Channel	CF type (LRS)	Localized oxygen vacancy
High I_D	S/D contact	Short channel	Interface effect	CF type (HRS)	Bulk effect
				Interface type (LRS&HRS)	Bulk effect

Fig. 3.3. Predominant noise origin depending on device conditions in MOSFET, TFT, and RRAM.

3.3 LFN application (2): Analysis of mechanisms in MLC operation

One of the important traits of RRAMs, which makes it useful for high density application, is its MLC behavior. There are mainly two ways to obtain MLC characteristic: (i) changing compliance current (I_{cc}) [57,58], (ii) controlling reset voltage (V_{reset}) [59,60].

The mechanism of MLC in the I_{cc} control mode is understood to be due to the formation and subsequent lateral expansion of CFs with increasing the I_{cc}, as

schematically shown in Fig. 3.4(a). As the CF size (or diameter) increases, the resistance becomes smaller, results in multilevel LRS. This claim is supported by the fact that the I_{reset} also increases with the I_{cc} because higher power is required to break larger CFs. Fig. 3.4(b) shows the MLC operation in our experimental device (TiN/Ti/TiO_2/TiN VCM RRAM). When the I_{cc} is increased, the respective current of LRS also increases, which resulting in three different levels of LRS (LRS1, 2, 3). Whereas, the current of HRS remains the same because the V_{reset} is constant. These four distinct levels can be used in 2-bit per cell storage and can enhance the storage density as compared to a single level cell with the same area. Also, from Fig. 3.4(c), it can be seen that I_{reset} also increases with the I_{cc}.

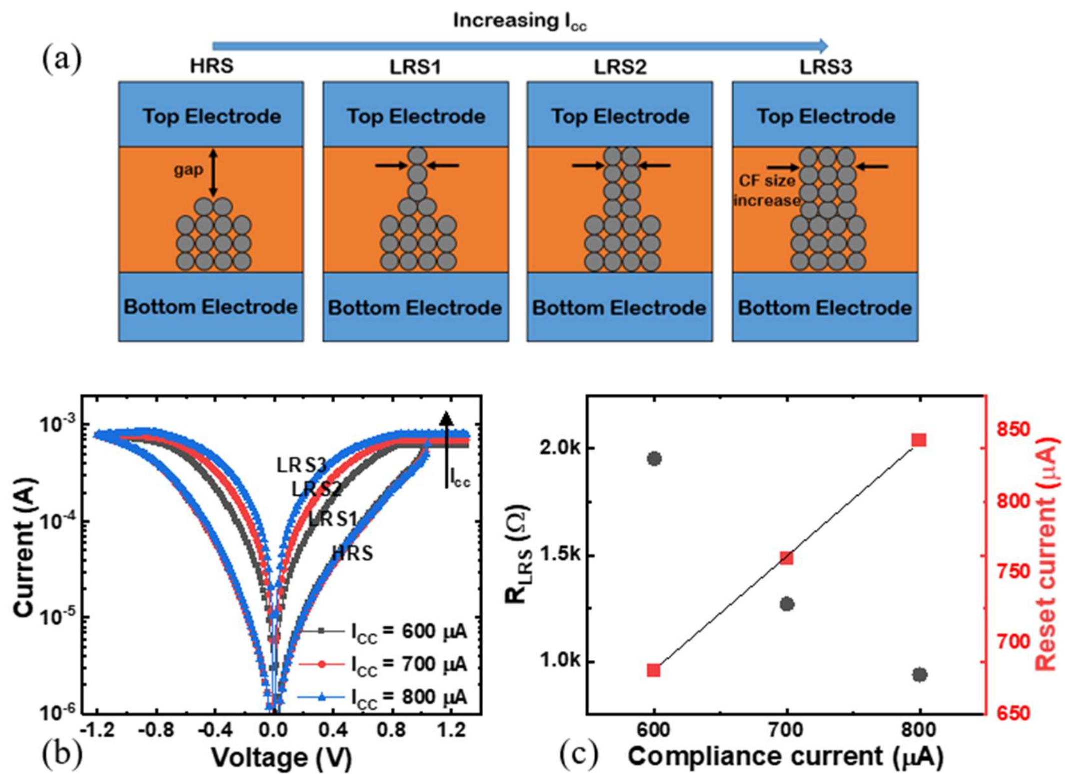


Fig. 3.4. (a) Schematic illustration and (b) *I-V* characteristics of MLC operation in the I_{cc} mode. (c) Dependence of resistance and reset current in LRS according to the I_{cc}.

The MLC characteristics can also be obtained by controlling the V_{reset} [59,60]. The MLC operation in the V_{reset} mode can also be explained by the structural change of the CF, similar to the I_{cc} mode. Fig. 3.5(a) shows the schematic illustration

showing the mechanism of MLC in the V_{reset} mode. As the V_{reset} increases, the gap between the electrode and the residual CF increases. This is because the redox reaction, which is the RS mechanism of our experimental RRAM device, is increased by a larger the V_{reset}. In the I-V_{read} characteristic of Fig. 3.5(b), four distinct resistance states (LRS, HRS1, 2, and 3) can be identified. It is possible to confirm from the LFN measurement that the mechanism of the MLC operation inferred by the I-V characteristics in the I_{cc} and V_{reset} mode, that is, the structural change of the CF inside the switching layer. Fig. 3.6(a) and (b) show the S_i/I^2 according to the MLC operation in (a) I_{cc} and (b) V_{reset} mode, respectively. In I_{cc} mode, the S_i/I^2 for Ohmic conduction is equal to eq. (7), where N is the total carrier number of free charge carriers. So, the S_i/I^2 in the HRS is constant, while the S_i/I^2 in the LRS decreases as the I_{cc} increases as shown in Fig. 3.6(a). In the V_{reset} mode, the S_i/I^2 for SCLC (verified on Chapter 4) is equal to eq. (8), where L is the device thickness. Therefore, the S_i/I^2 in the LRS is constant, while the S_i/I^2 in the HRS increases as the V_{reset} increases as shown in Fig. 3.6(b). These results show that the LFN measurement is a good electrical characterization technique to indirectly confirm

the CF's configuration and to analyze the mechanism of the MLC operation.

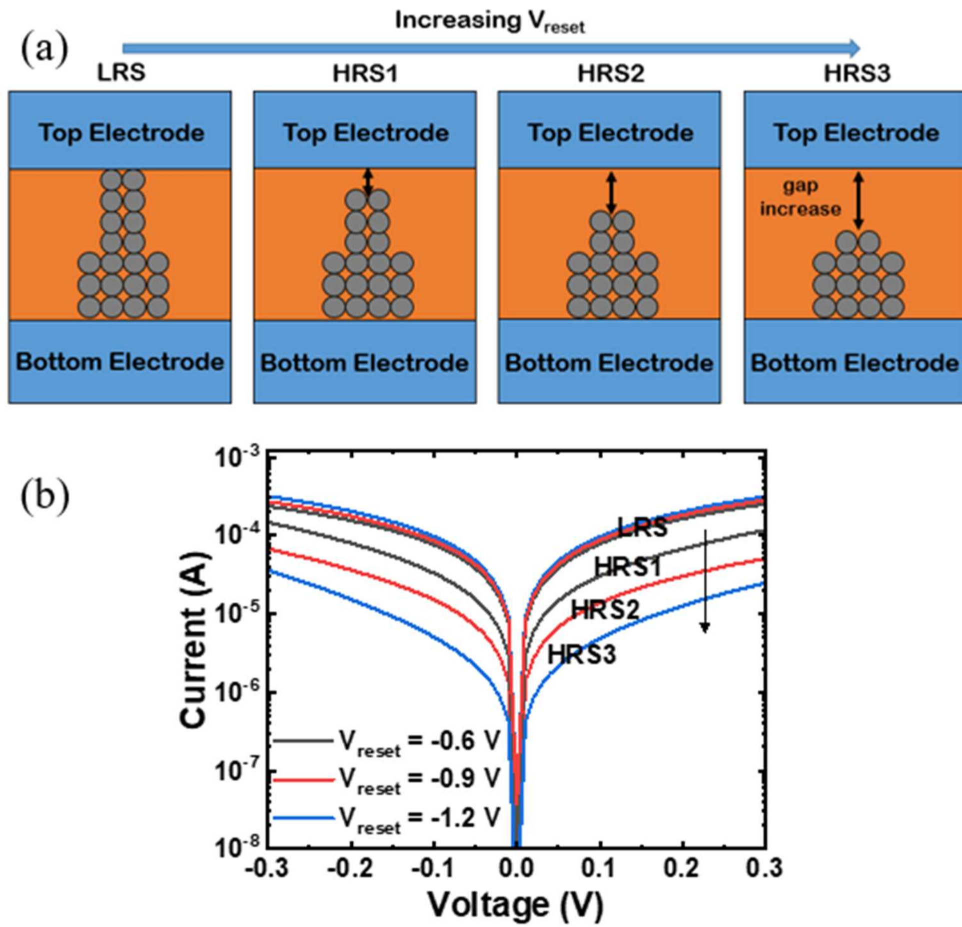


Fig. 3.5. (a) Schematic illustration and (b) I-V_{read} characteristics of MLC operation in the V_{reset} mode.

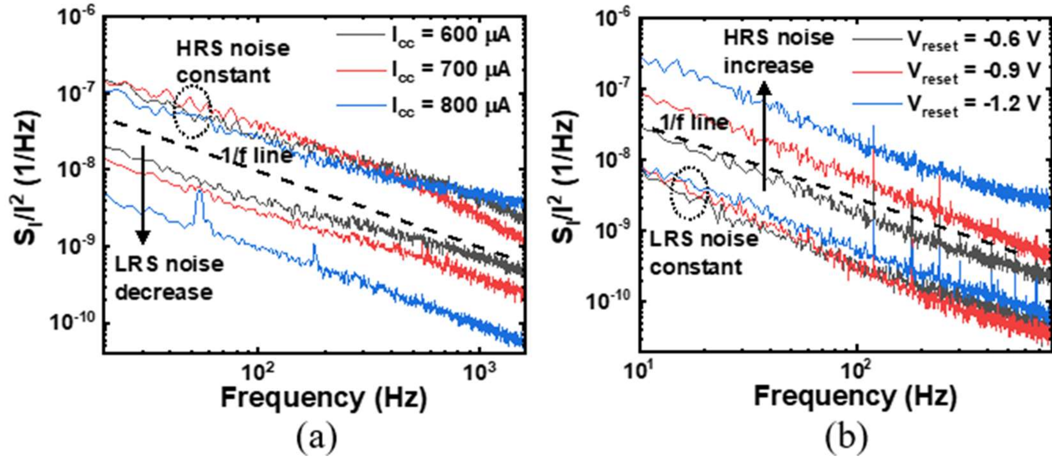


Fig. 3.6. S_i/I^2 according to the MLC operation in (a) I_{cc} and (b) V_{reset} mode.

3.4 LFN application (3): Degradation analysis

Switching endurance, which tells how many times a memory device can switch between cell states without the degradation, is one of the most important figures of merit for a memory device [61]. From this point of view, developing a technique to analyze the degradation mechanism of RRAM devices is a very good direction for RRAM optimization. Fig. 3.7(a) shows the *I-V* curves (HRS to LRS) of our experimental device (Al/αTiO$_2$/Al VCM RRAM) for 500 DC cycles. While the current variation in the LRS is insignificant, degradation in the HRS is noticeably clear, as shown in Fig. 3.7(b). As will be discussed in chapter 4, the conduction

mechanism of our experimental RRAM device is SCLC [62]. According to trap-controlled SCLC model [56,63], the SCLC arises when current through the bulk solid becomes limited by the build-up of charge injected from the electrode ($V_{tr} < \mathrm{V} < V_{TFL}$ in Fig. 2.4). When the applied voltage is raised to a threshold value (V_{TFL}), the injected carriers are just sufficient to fully fill the trap states, result in the rapid increment of the current. The degradation of our experimental RRAM device is closely related to this SCLC mechanism. We can infer that certain traps whose energy levels are far below the conduction band (deep traps) are likely to fail to release the trapped charge carriers during the reset process. So, repetitive RS process could induce more effective filling-up of the deep traps and prevent their effective de-trapping during the subsequent reset process. Our understanding of the endurance degradation mechanism is supported by LFN measurements below. Fig. 3.8(a) shows the S_i/I^2 according to the switching cycle. It can be seen that as the number of cycles increases, the S_i/I^2 in the LRS does not change significantly, while the S_i/I^2 in the HRS gradually decreases. The S_i/I^2 rapidly decreases for approximately 100 cycles and then saturates, as shown in Fig. 3.8(b). Our deduction

based on the *I-V* characteristic above is consistent with the LFN measurement results. Namely, the reduction of the trap, which is the scattering center of the charge carrier [64], causes the decrease of the S_i/I^2. These results show that LFN measurement can be a valuable analytical tool to clarify the physical mechanism associated with the degradation of RRAM.

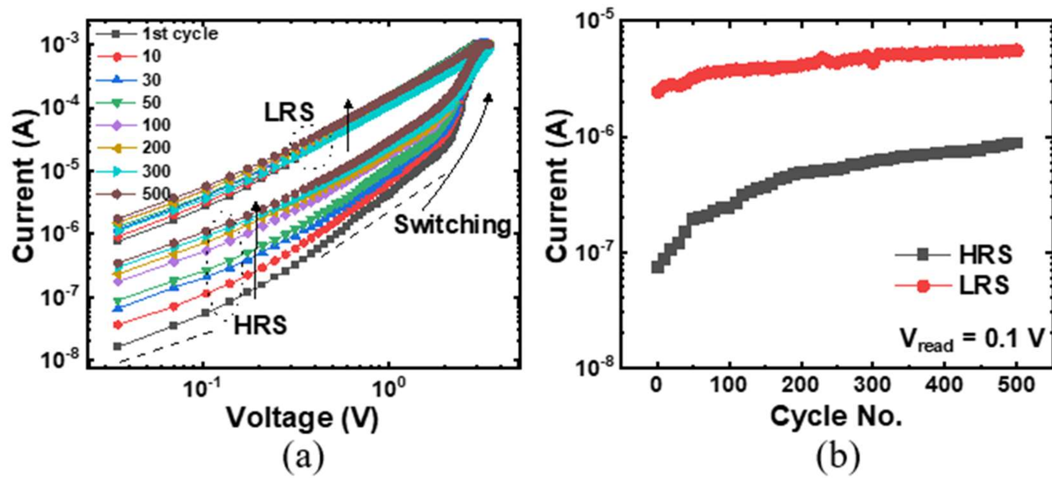


Fig. 3.7. (a) *I-V* curves (HRS to LRS) and (b) Cycle to cycle variation of the current in LRS and HRS at V_{read} of 0.1 V for 500 DC cycles.

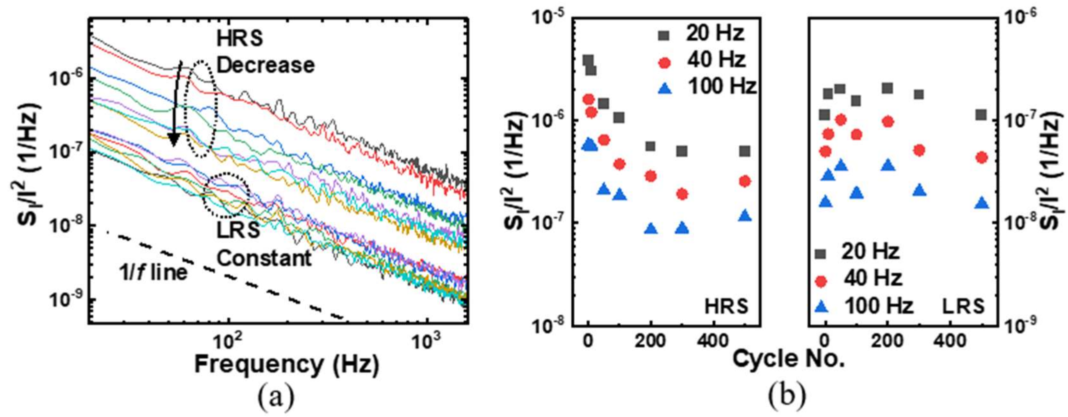


Fig. 3.8. (a) S_i/I^2 according to the switching cycle. (b) Cycle to cycle variation of the S_i/I^2 in HRS (left) and LRS (right) at frequencies 20, 40, and 100 Hz for 500 DC cycles.

Chapter 4

Analysis of conduction mechanism using LFN in RRAMs

4.1 Thermochemical mechanism RRAM (TCM RRAM)

4.1.1 Fabrication

In order to investigate LFN characteristics of TCM RRAM, we fabricate the polycrystalline-TiO_2 based RRAM device. The process flow of the $Pt/TiO_2/Pt$ sample is described as follows (Fig. 4.1(a)). A 40 nm-thick TiO_2 thin film was deposited by plasma-enhanced atomic layer deposition (ALD) at 300 ºC using titanium-tetra-iso-propoxide (TTIP) as a precursor and plasma-activated O_2 as an oxidant on a 100 nm-thick $Pt/SiO_2/Si$ substrate. Then, 50 nm-thick Pt top electrodes with a diameter of 80 μm were formed by an electron-beam evaporation. Subsequently, the lift-off process was performed for patterning the top electrode. Fig. 4.1(b) and (c) show schematic structure and cross-sectional TEM image of the

device used in experiments.

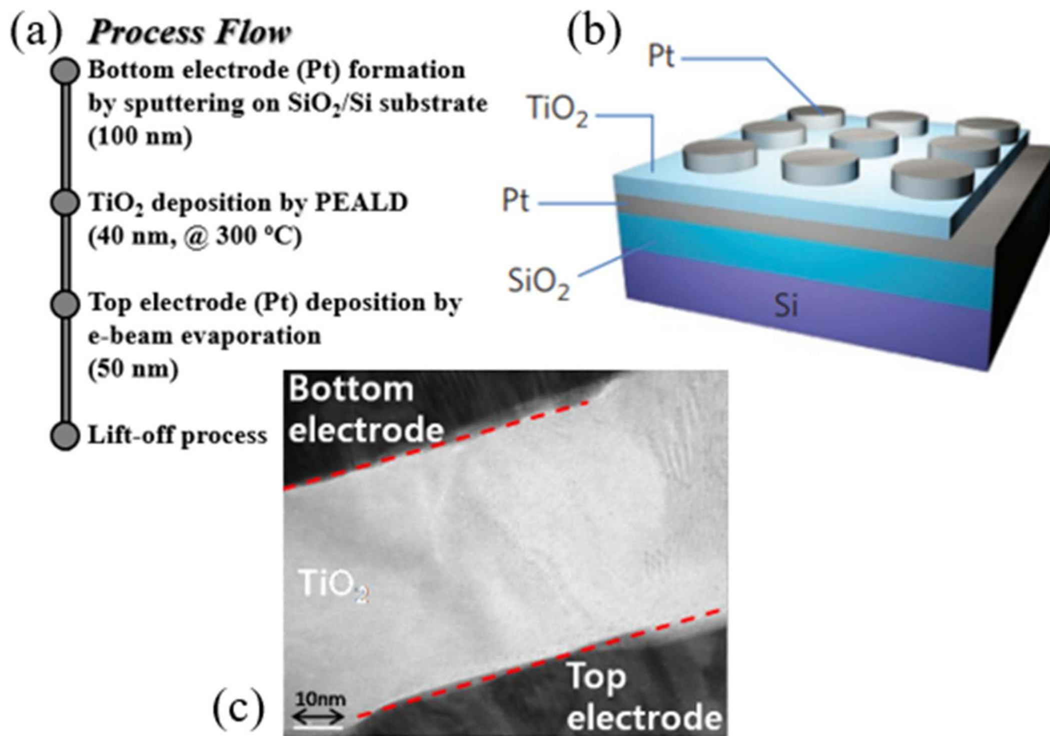


Fig. 4.1. (a) Process flow, (b) schematic structure, and (c) cross-sectional TEM image of the device used in experiments.

4.1.2 Experimental results: RS and *I-V* characteristics

Fig. 4.2(a) shows the current–voltage (*I-V*) curves of the fabricated Pt/TiO_2/Pt device, which exhibit a unipolar RS characteristic showing three typical operations

of Forming, Reset, and Set processes. During Forming and Set processes, a compliance current of 1 mA is applied to protect the device from the dielectric breakdown. To understand the current transport mechanism of the LRS, an *I-V* curve was observed in Fig. 4.2(b), which shows a linear curve with a slope of 1 for the LRS on a logarithmic scale. This shows that the main conduction mechanism of the LRS is Ohmic conduction and that the percolation path was formed during Forming and Set processes. The path is often referred to as the conductive filament (CF). In order to more clearly identify the nature of the CF, we performed the *I-V-T* measurement as shown in Fig. 4.2(c). The decreasing trend of current upon increasing the temperature implies the presence of typical metallic CF. From the resistance data obtained from Fig. 4.2(c), the temperature coefficient of LRS is investigated using the following equation (11):

$$R(T) = R_0[1 + \alpha(T - T_0)], \quad (11)$$

where R_0 is the resistance at temperature T_0 and α is the temperature coefficient of resistance. The fitting lines in Fig. 4.2(d) indicate that α is 3.5 ~ 4.34 $\times$ 10^{-3} K^{-1}, which is similar to the value for metallic nanowires with a diameter of 15 ~ 30 nm

[65].

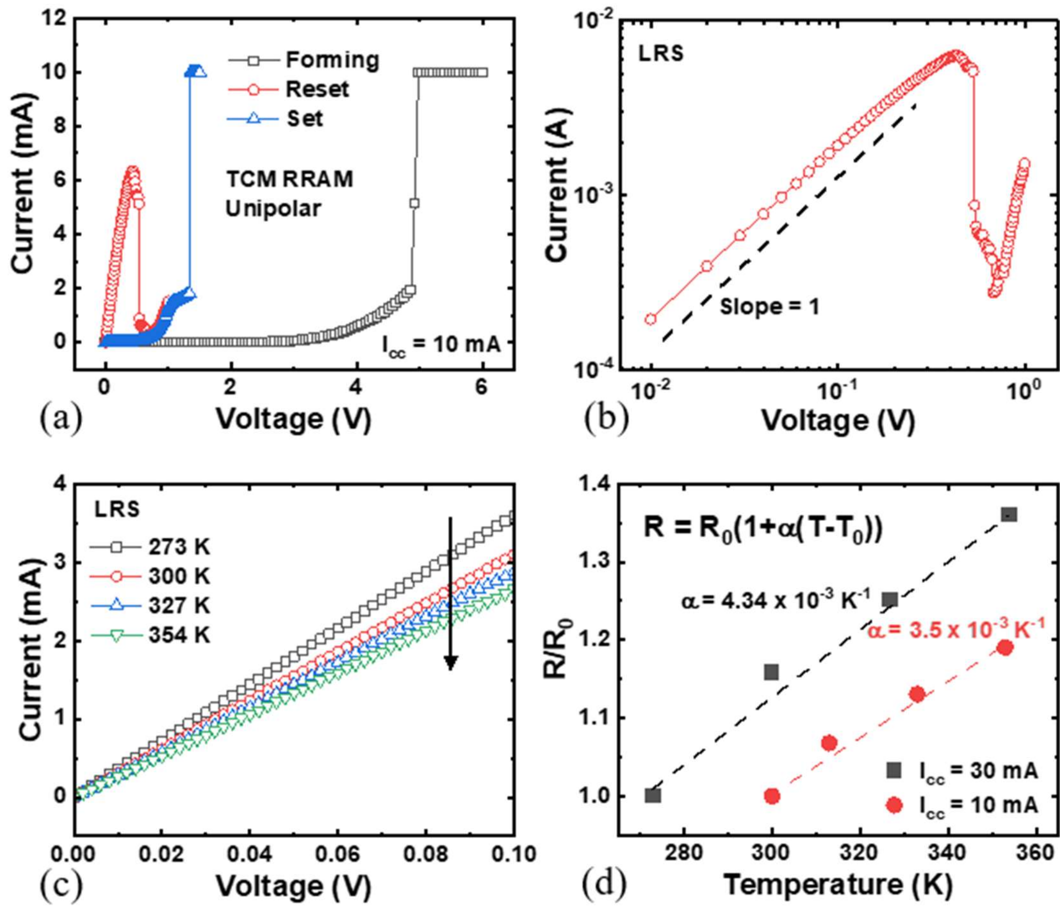


Fig. 4.2. (a) *I-V* curves of the fabricated Pt/TiO_2/Pt device, (b) linear fitting of *I-V* characteristics for LRS on a logarithmic scale, (c) *I-V-T* measurement, and (d) the temperature coefficient of resistance obtained from *I-V-T* data.

Nonlinear curve for HRS in Fig. 4.2(a) shows that the current in HRS flows by a different mechanism from that in LRS. Fig. 4.3(a) shows that ln(I) has a linear relationship with $V^{1/2}$ on a semi-logarithmic scale, representing that the dominant current conduction mechanism in HRS is the Schottky emission. Considering that the TiO_2 is an n-type semiconductor [66] and the work function of the Pt is high (5.12 ~ 5.93 eV) [67], It can be seen that the Schottky contact was formed between the Pt electrode and the TiO_2 after the rupture of the CF in HRS as shown in Fig. 4.3(d). So, the Schottky emission is the most likely conduction mechanism in HRS. The Schottky emission has been repeatedly observed for HRS of RRAMs with TiO_2 and Pt electrodes by several groups [68-70]. Here, P-F emission could be ruled out from a possible current conduction mechanism since the plot of ln(I/V) vs. $V^{1/2}$ is not a straight line (Fig. 4.3(b)). The same also applies to the F-N tunneling (Fig. 4.3(c)). To further clarify the current transport mechanism in HRS, we performed the *I-V-T* measurement as shown in Fig. 4.4(a). From eq. (1), and Fig. 4.4(a), the equivalent Schottky barrier height (SBH, ϕ_B^0) can be extracted by the slope of ln(J/T^2) vs. 1000/T plots as shown in Fig. 4.4(b). Fig. 4.4(c) shows the ϕ_B vs. $E^{1/2}$

plot and the intercept on the x-axis is the ϕ_B^0. By extrapolating to E = 0, the extracted ϕ_B^0 is ~0.77 eV. This is somewhat lower than the expected value of ~1.2 eV. It may be the result of the fermi-level pinning or Schottky barrier lowering. Reportedly, the SBH at the defect-free interface of TiO_2/Pt is 1.2 eV [71], but the measured SBH from 0.55 eV [70] to 1.14 eV [72] have been often reported in RRAM.

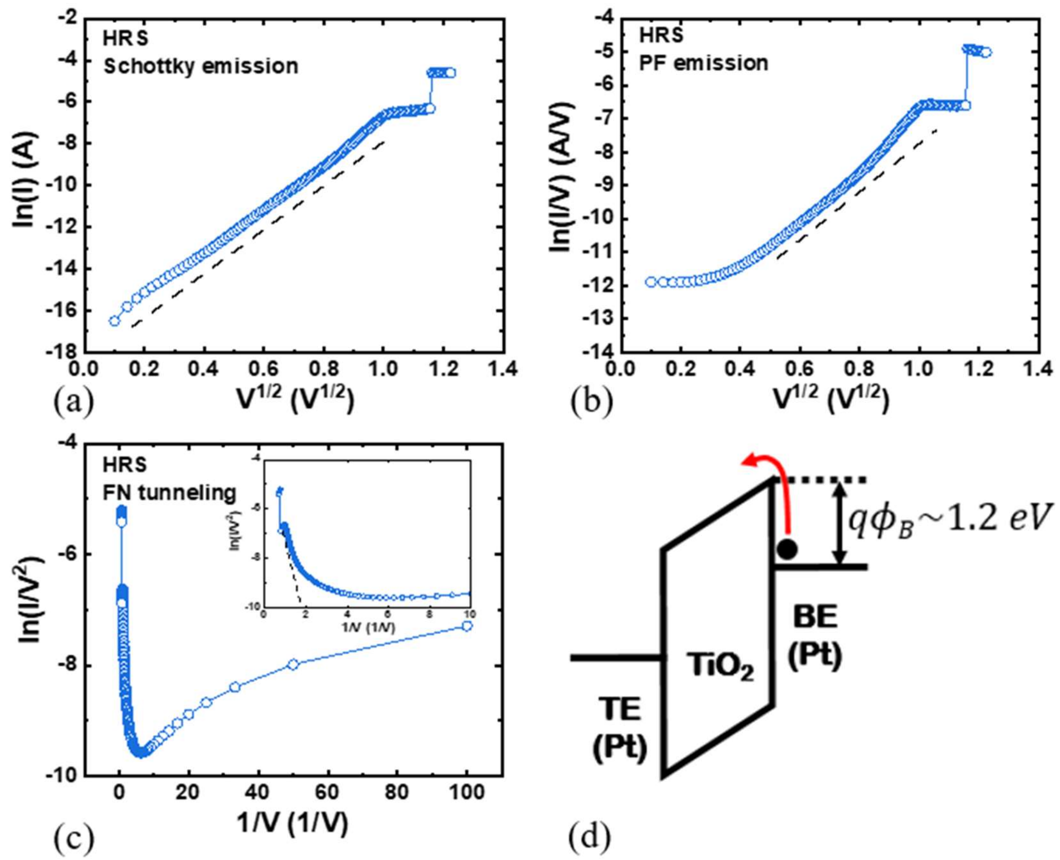


Fig. 4.3. Fitting results for (a) Schottky emission, (b) PF emission, and (c) F-N tunneling. (d) the schematic energy band diagram of the Pt/TiO_2/Pt structure.

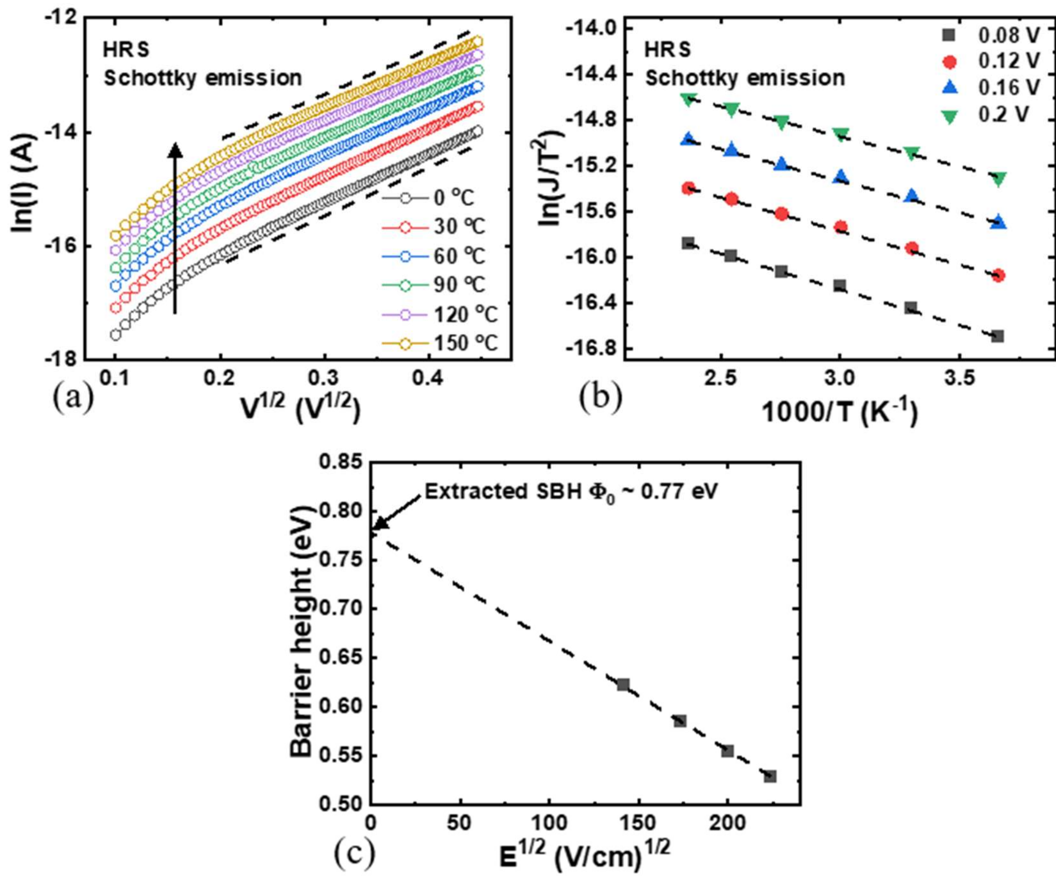


Fig. 4.4. (a) Fitting results for (a) Schottky emission at different temperatures. (b) $\ln(J/T^2)$ vs. $1000/T$ curves for extraction of SBH. (c) The variation in SBH as a function of E.

4.1.3 Experimental results: LFN characteristics

To verify the correlation between current conduction mechanism and LFN

characteristic, we measured the normalized noise power spectral density (S_i/I^2). Fig. 4.5(a) shows the S_i/I^2 measured at 0.04 V to 0.18 V in LRS. The S_i/I^2 is proportional to $1/f^{\gamma}$, with $\gamma \sim 1$ for all voltage regions (see dotted-line in Fig. 4.5(a)), which means that the LFN characteristic in Pt/TiO_2/Pt RRAM devices also follows the classical $1/f$ noise theory. The bias dependence of the S_i/I^2 can be used to confirm the current conduction mechanism in LRS. Fig. 4.5(b) shows the double-logarithmic plot of the bias dependence of the S_i/I^2 at frequencies 20, 40, and 100 Hz in LRS. As shown in Fig. 4.5(b), the measured S_i/I^2 is nearly constant according to the bias, which follows eq. (7) and is compatible with the $1/f$ noise theory for the Ohmic conduction. So, the conduction mechanism verified from the LFN measurement is consistent with expected result by *I-V-T* measurements, which means that LFN can be a diagnostic tool to investigate the conduction mechanism (Ohmic conduction) in TCM RRAM.

To confirm the correlation between current conduction mechanism and LFN properties also in HRS, we measured the noise power spectral density (S_i). Fig. 4.6(a) shows the S_i measured at 0.01 V to 0.8 V in HRS. Like the LRS, the S_i is

proportional to $1/f^{\gamma}$, with $\gamma \sim 1$ for all voltage regions (see dotted-line in Fig. 4.6(a)). The bias dependence of the LFN can be used to confirm the current conduction mechanism. Fig. 4.6(b) shows the double-logarithmic plot of the current dependence of the S_i at frequencies 20, 40, and 100 Hz in HRS. As shown in Fig. 4.6(b), the S_i is proportional to I^2 in all current ranges, which agrees with the $1/f$ noise model for Schottky emission in eq. (9). Therefore, in both states of TCM RRAM, we can conclude the LFN measurement can be a useful tool as electrical characterization technique to investigate the conduction mechanism (Schottky emission) in TCM RRAM

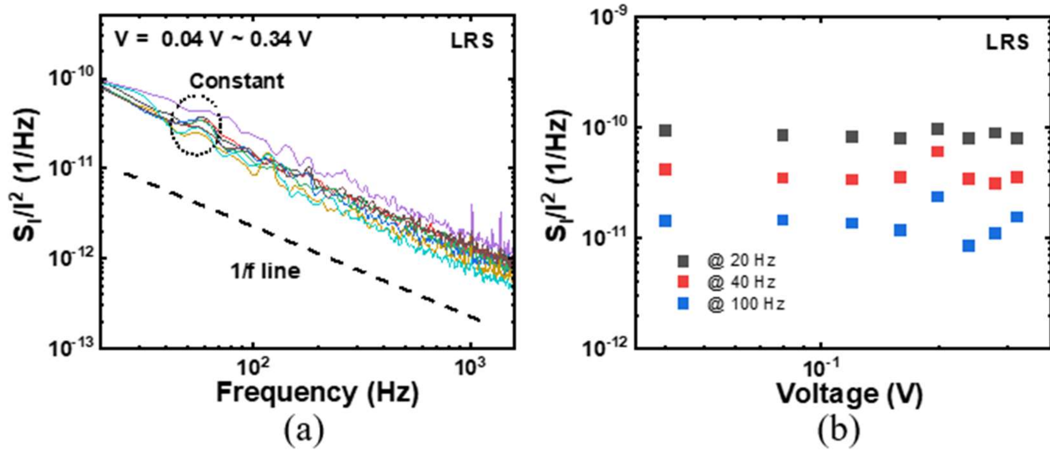


Fig. 4.5. (a) S_i/I^2 according to the voltage in LRS. (b) The logarithmic plot of the voltage dependence of the S_i/I^2 at frequencies 20, 40, and 100 Hz in LRS.

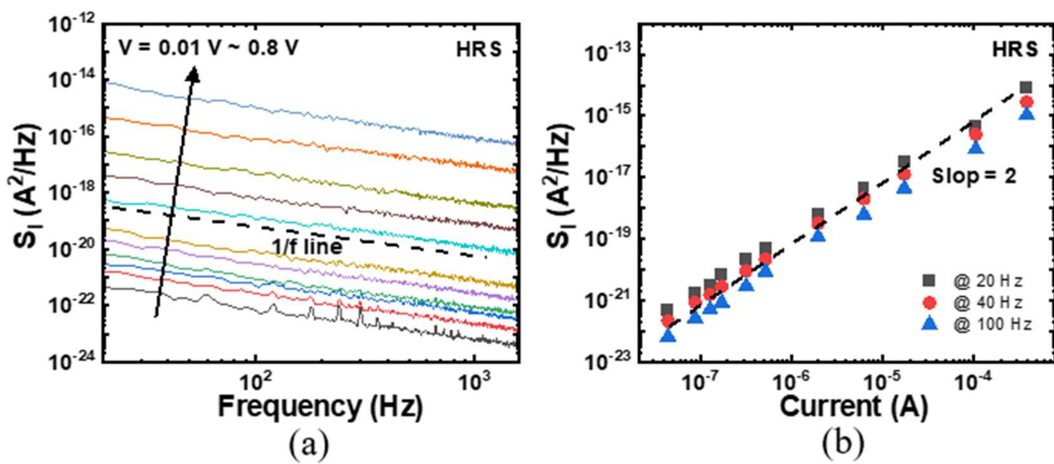


Fig. 4.6. (a) S_i according to the voltage in HRS. (b) The logarithmic plot of the current dependence of the S_i at frequencies 20, 40, and 100 Hz in HRS.

4.2 Valence change mechanism RRAM (VCM RRAM)

4.2.1 Fabrication

In order to investigate LFN characteristics of VCM RRAM, we fabricate the amorphous TiO_2 based RRAM device. The process flow of the Al/αTiO_2/Al sample is described as follows (Fig. 4.7(a)). The TiO_2 oxide film with a thickness of ~8 nm was deposited on a 50-nm-thick Al/SiO2/Si substrate by the PEALD at a substrate temperature of 180 °C. The TTIP precursor was used with an oxygen plasma, which is oxidizing agent. The 50 nm-thick aluminum bottom and top electrode were deposited by thermal evaporation method, forming the cross-bar type structures using a shadow mask with a line width of 60 μm, as shown in Fig. 4.7(b). Fig. 4.7(c) shows the cross-sectional TEM image of the fabricated RRAM device.

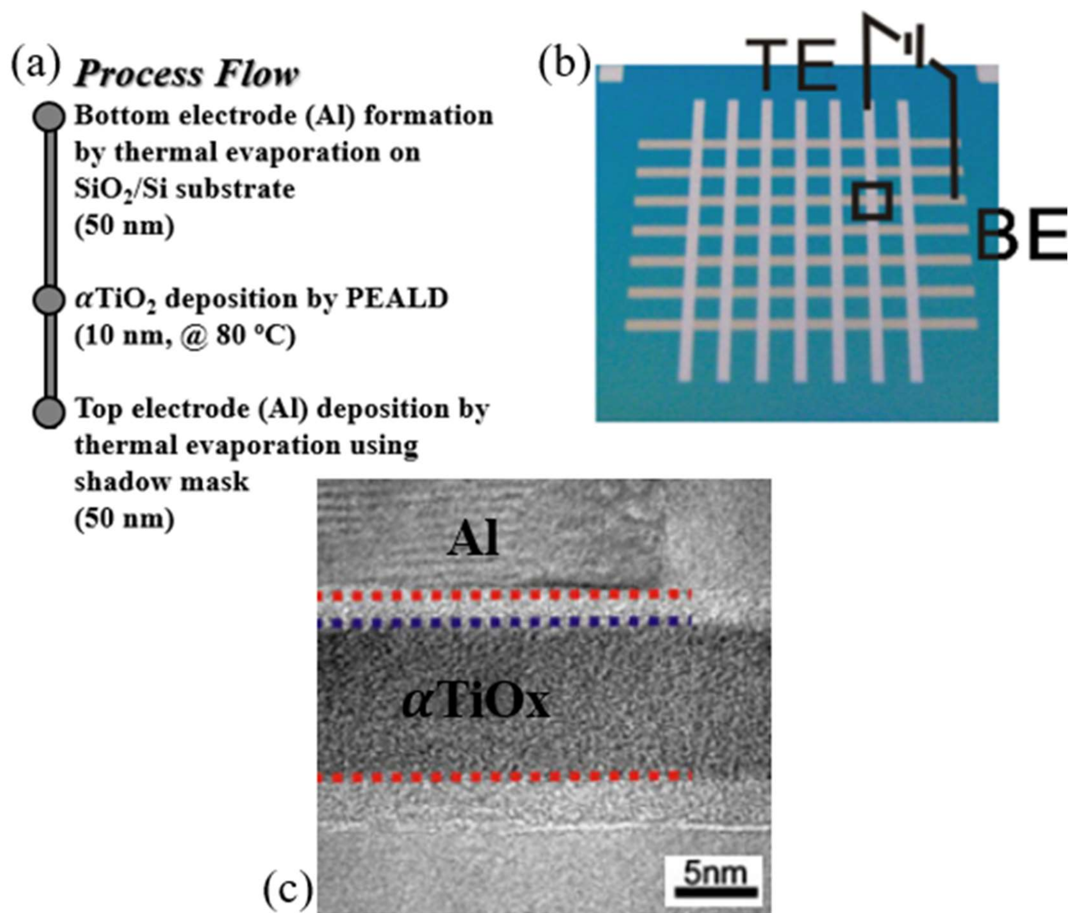


Fig. 4.7. (a) Process flow, (b) schematic structure, and (c) cross-sectional TEM image of the device used in experiments.

4.2.2 Experimental results: RS and *I-V* characteristics

Fig. 4.8(a) shows the current-voltage (*I-V*) characteristics of the fabricated Al/αTiO_2/Al RRAM device for the 10 cycles. The bias sweep sequence is indicated by the arrows. When the voltage is swept from 0 V to the negative voltage direction, the device transitions from the HRS to the LRS above the set voltage (SET process). The LRS is held up to about 2 V during the positive voltage sweep and then switches back to the HRS above the reset voltage (RESET process). A compliance current of 5 mA is applied to protect the device from dielectric breakdown. Our device represents asymmetric bipolar resistance switching, which is no need for an additional electroforming process. To clarify the current transport mechanism in both the HRS and LRS, the I–V curve at the 30th cycle has been replotted on a double-logarithmic scale in Figure 2b. Referring to the linear guidelines in Figure 2b, the conduction mechanism of the device can be understood using the space-charge limited conduction (SCLC) model [33,43]. Trap-controlled SCLC can be divided into two regions. In the low field region, the conduction mechanism is

dominated by the thermally generated free electrons in the dielectric film (Ohmic conduction, $I \propto V$). If the applied field intensity exceeds the critical value, the density of free electrons injected from the electrode gradually exceeds the equilibrium concentration, and excess electrons accumulate in the space between two electrodes. Consequently, the space charge starts to limit the total current flow (SCLC, $I \propto V^m, m > 2$). The trap-controlled SCLC has been reported to be one of the dominant mechanisms causing the resistive switching in various RRAM devices [73-75], and the oxygen vacancies, which is formed from the reaction of the deposited Al with αTiO_2 at the interface of the top Al electrode and αTiO_2, are known to act as the electron traps in Al/αTiO_2/Al devices [75]. So, we can conclude that the trap-controlled SCLC is the most likely conduction mechanism in both LRS and HRS. Here, Schottky emission could be ruled out from a possible current conduction mechanism since the plot of ln(I) vs. $V^{1/2}$ is not a straight line (Fig. 4.9(a)). The same also applies to P-F emission (ln(I/V) vs. $V^{1/2}$ should be fitted by a straight line) and F-N tunneling (ln(I/V^2) vs. $1/V$ should be fitted by a straight line), as shown in Fig. 4.9(b), (c), and (d).

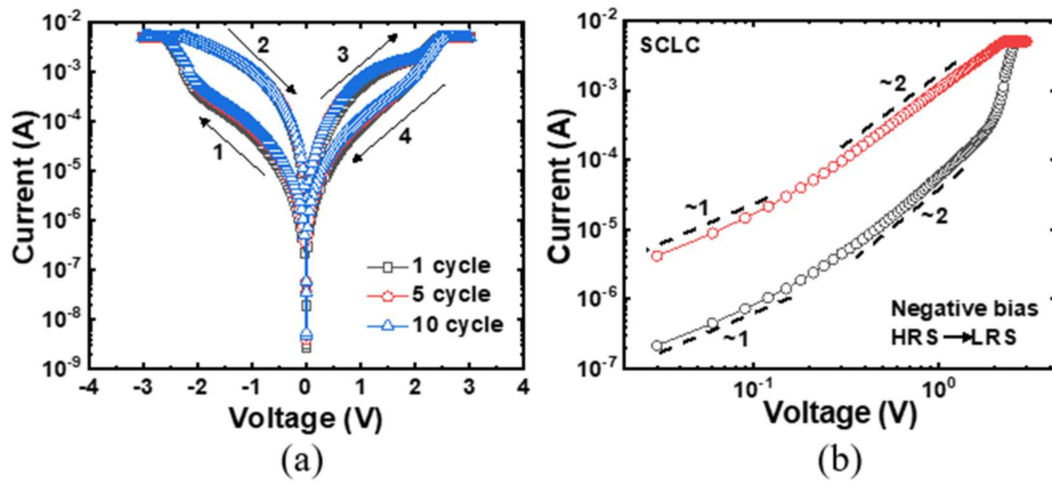


Fig. 4.8. (a) *I-V* curves of the fabricated Al/αTiO_2/Al device. The arrows indicate the direction of the voltage sweep. (b) *I-V* characteristics for both LRS and HRS on a logarithmic scale.

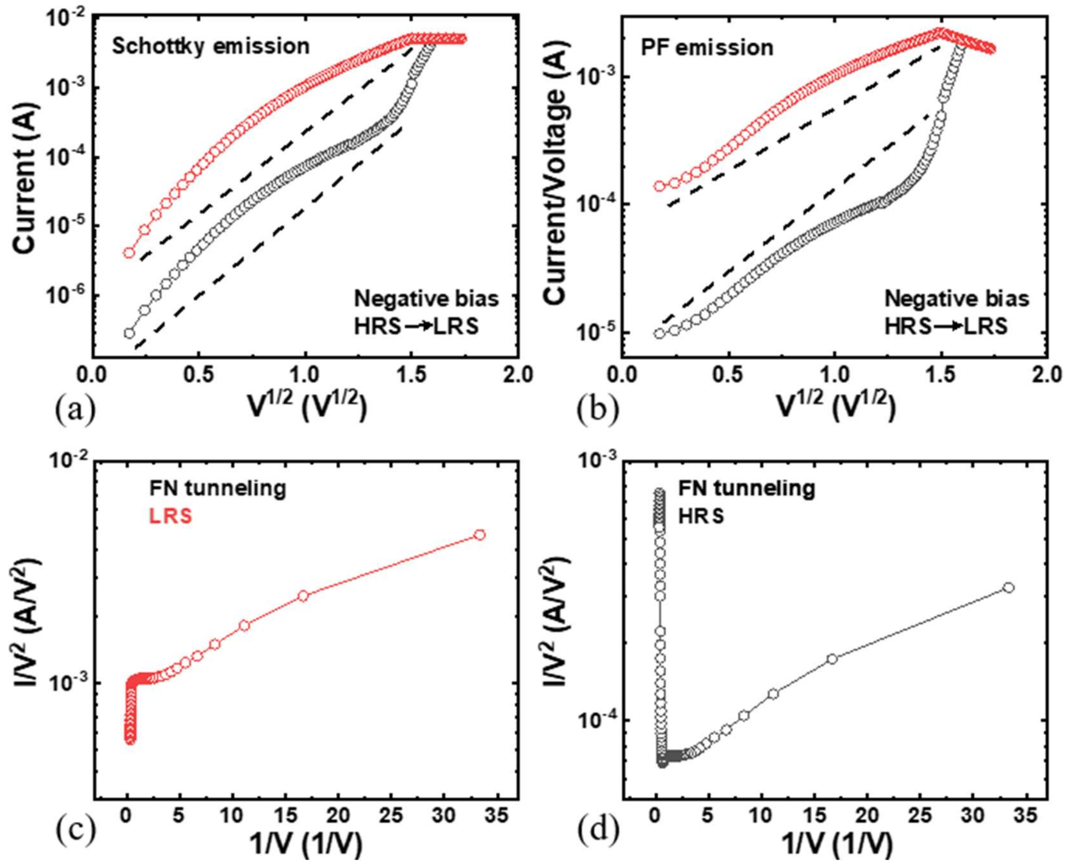


Fig. 4.9. Fitting results for (a) Schottky emission, (b) PF emission, and F-N tunneling ((c) LRS and (d) HRS).

4.2.3 Experimental results: LFN characteristics

To verify the correlation between current conduction mechanism and LFN characteristic, we measured the normalized noise power spectral density (S_i/I^2) in VCM RRAM. Fig. 4.10(a) and (b) show the S_i/I^2 as the voltage increases in LRS

and HRS, respectively. The S_i/I^2 is proportional to $1/f^{\gamma}$, with $\gamma \sim 1$ for all voltage regions and both resistance states (see dotted-lines in Fig. 4.10(a) and (b)), which means that the LFN characteristic in $Al/\alpha TiO_2/Al$ RRAM devices also follows the classical $1/f$ noise theory. From eq. (7) and (8), the bias dependence of the S_i/I^2 can be used to confirm the current conduction mechanism. Fig. 4.10(c) and (d) show the double-logarithmic plots of the bias dependence of the S_i/I^2 at frequencies of 20, 40 and 80 Hz for LRS and HRS, respectively. In both resistance states, the S_i/I^2 has no bias dependence until approximately 0.1 V, but then decreases with a slope of 1 as the voltage increases. These results are consistent with the noise theories that the S_i/I^2 does not change with a voltage for resistance fluctuations in Ohmic conditions, but inversely proportional to the voltage according to a noise suppression mechanism under SCLC conditions [56,76]. The conduction mechanism of VCM RRAM predicted in the subchapter 4.2.2 is double checked from the LFN measurement. Therefore, we can conclude the LFN measurement can be a useful tool as electrical characterization technique to investigate the conduction mechanism (SCLC) in also VCM RRAM.

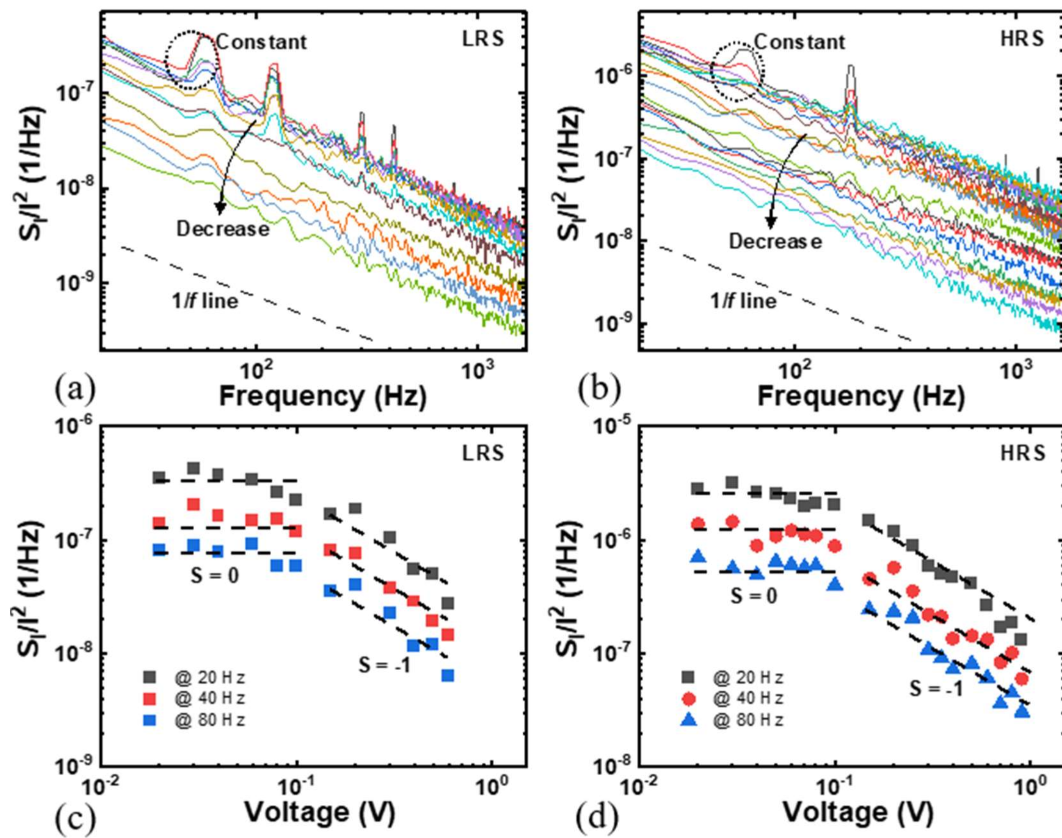


Fig. 4.10. S_i/I^2 as the voltage increases in (a) LRS and (b) HRS. Logarithmic plots of the voltage dependence of the S_i/I^2 at frequencies of 20, 40 and 80 Hz for (c) LRS and (d) HRS.

4.3 Comparative analysis of conduction mechanism (VCM vs. EEM)

4.3.1 Fabrication

For comparative study, RRAMs with MIM structures of TiN/Ti/TiO_2/TiN (VCM) and TiN/Ti/TiO_2/HfO_2/TiN (EEM) were fabricated using the sub-50 nm process technology on 300 mm wafer. From here on, for convenience, TiN/Ti/TiO_2/TiN and TiN/Ti/TiO_2/HfO_2/TiN will be named SLRRAM and DLRRAM, respectively. The process flows of (a) SL- and (b) DLRRAM are described as shown in Fig. 4.11(a) and (b), respectively. TiO_2 (20 nm) or TiO_2 (20 nm)/HfO_2 (2 nm) were deposited on TiN bottom electrode (BE) by the ALD at 280 ºC. The Ti buffer layer was then formed by a sputtering process. Finally, the TiN top electrode (TE) was deposited perpendicularly to the BE by metal-organic ALD. Sequentially, a metal alloy annealing process was conducted in a N_2 ambient at 400 ºC for 10 minutes. Fig. 4.11(c) and (d) show the cross-sectional TEM images of SL- and DLRRAM used in our experiments, respectively. Here, The Ti buffer layer induces local oxygen vacancies such as V_O^+ and V_O^{2+}, which act as traps to capture

electrons in the upper region of TiO_2, and consequently improve the switching characteristics (decrease of switching voltage). Also, in DLRRAM, thin HfO_2 layer was introduced to reduce the high reset current. All the measurements were conducted in samples of the same area (90×90 nm^2).

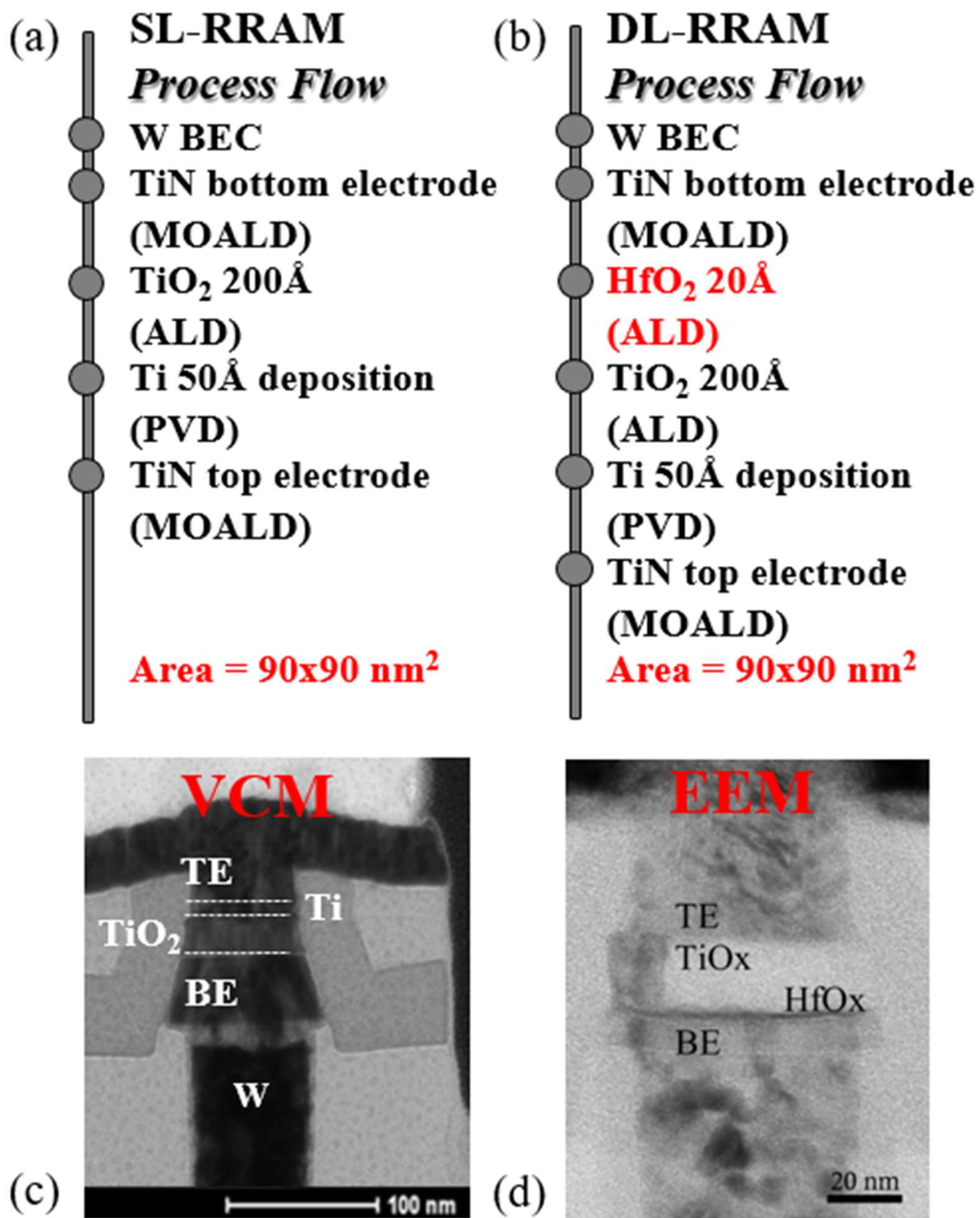


Fig. 4.11. Process flows of (a) SL- and (b) DLRRAM. Cross-sectional TEM images of (c) SL- and (d) DLRRAM.

4.3.2 Experimental results: RS and *I-V* characteristics

Fig. 4.12(a) and (b) show the fitting results for SCLC and Schottky emission in SLRRAM, respectively. As can be seen from Fig. 4.12(a), the Ohmic conduction fits best in LRS and the trap-controlled SCLC seems to fit well in HRS. However, as shown in Fig. 4.12(b), in HRS, the linear fitting seems possible in plot of log(*I*) vs. $V^{1/2}$. So, the *I-V* fitting result alone is insufficient to completely exclude the Schottky emission in HRS. Fig. 4.12(c) and (d) show the fitting results for SCLC and Schottky emission in DLRRAM, respectively. Unlike SLRRAM, the SCLC mechanism (Fig. 4.12(c)) as well as the Schottky emission (Fig. 4.12(d)) appears to be a possible conduction mechanism. Therefore, additional analytical procedures such as physical characterization techniques (STM, AFM, and TEM) or the temperature measurement are required for accurate mechanism analysis. In chapter 4 so far, we have verified the correlation between conduction mechanism and LFN characteristics in various RRAM devices. In the next subchapter 4.3.3, based on the research results so far, we will investigate more accurate conduction mechanism of

SLRRAM and DLRRAM using the LFN measurement method.

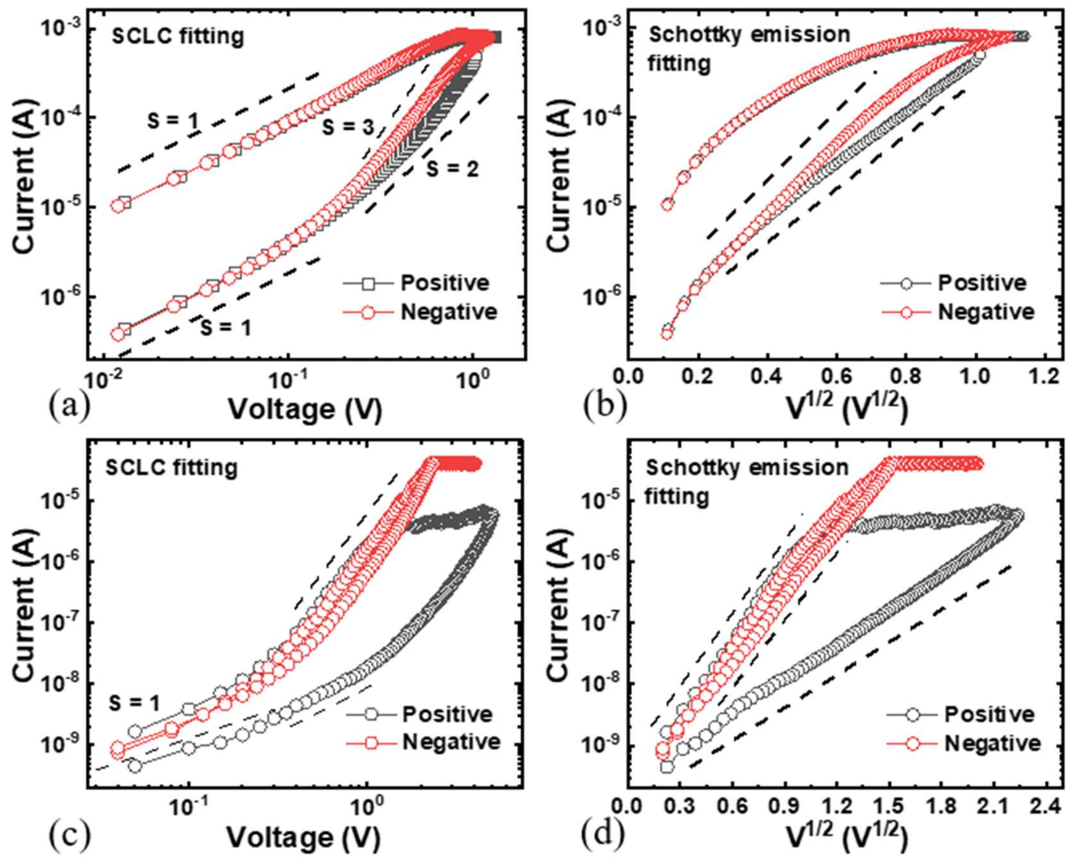


Fig. 4.12. Fitting results for (a) SCLC and (b) Schottky emission in SLRRAM. Fitting results for (c) SCLC and (d) Schottky emission in DLRRAM.

4.3.3 Experimental results: LFN characteristics

Fig. 4.13(a) and (b) show the S_i/I^2 of SLRRAM as the voltage increases in LRS and HRS, respectively. The S_i/I^2 is proportional to $1/f^{\gamma}$, with $\gamma \sim 1$ for all voltage regions and both resistance states. Fig. 4.13(c) shows the double-logarithmic plot of the bias dependence of the S_i/I^2 at 20 Hz for LRS (circle symbol) and HRS (square symbol). The measured S_i/I^2 in LRS is nearly constant according to the bias, which follows eq. (7) and is compatible with the $1/f$ noise theory for the Ohmic conduction. So, in common with the results of *I-V* fitting, it can be clearly seen that the conduction mechanism is the Ohmic. The measured S_i/I^2 in the HRS has no bias dependence until approximately 0.1 V, but then decreases with a slope of 1 as the voltage increases. These results correspond to the noise theories that the S_i/I^2 does not change with a voltage for resistance fluctuations under Ohmic conditions, but inversely proportional to the voltage according to a noise suppression mechanism under SCLC conditions. Therefore, *I-V* fitting alone could not clearly determine the dominant conduction mechanism, but with the help of LFN measurements, the conduction mechanism can be determined more precisely.

Fig. 4.14(a) and (b) show the S_i/I^2 of DLRRAM as the bias in LRS and HRS, respectively. Fig. 4.14(c) shows the double-logarithmic plot of the bias dependence of the S_i at 20 Hz for all voltage regions and both resistance states. The S_i is proportional to I^2 in all current ranges, which agrees with the $1/f$ noise model for Schottky emission in eq. (9). So, it was not possible to accurately distinguish whether the conduction mechanism of DLRRAM was Schottky or SCLC only by *I-V* fitting, but from LFN measurements, it can be concluded that the Schottky emission is the conduction mechanism of DLRRAM. Summarizing the contents of chapter 4, the LFN measurement can be used as an effective tool to analyze the conduction mechanism of RRAM devices together with *I-V* fitting and temperature measurement or physical characterization techniques.

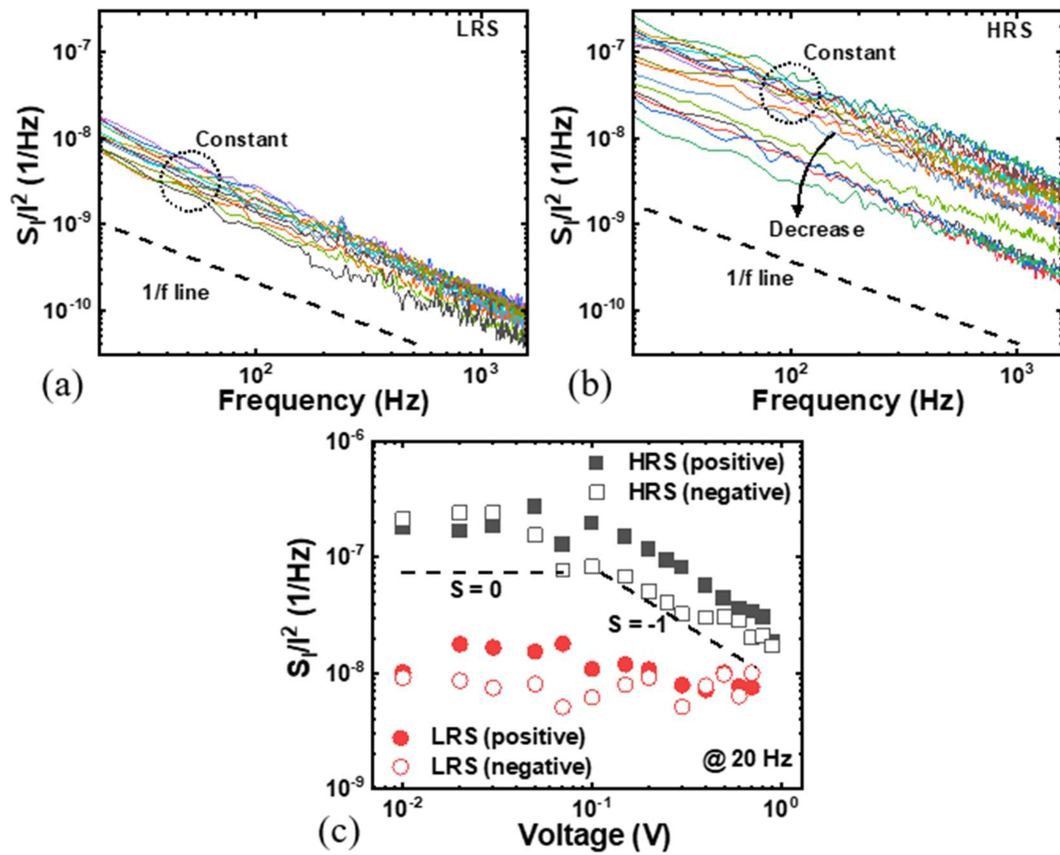


Fig. 4.13. S_i/I^2 according to the voltage in (a) LRS and (b) HRS. (c) The logarithmic plot of the voltage dependence of the S_i/I^2 at 20 Hz in LRS (circle) and HRS (square).

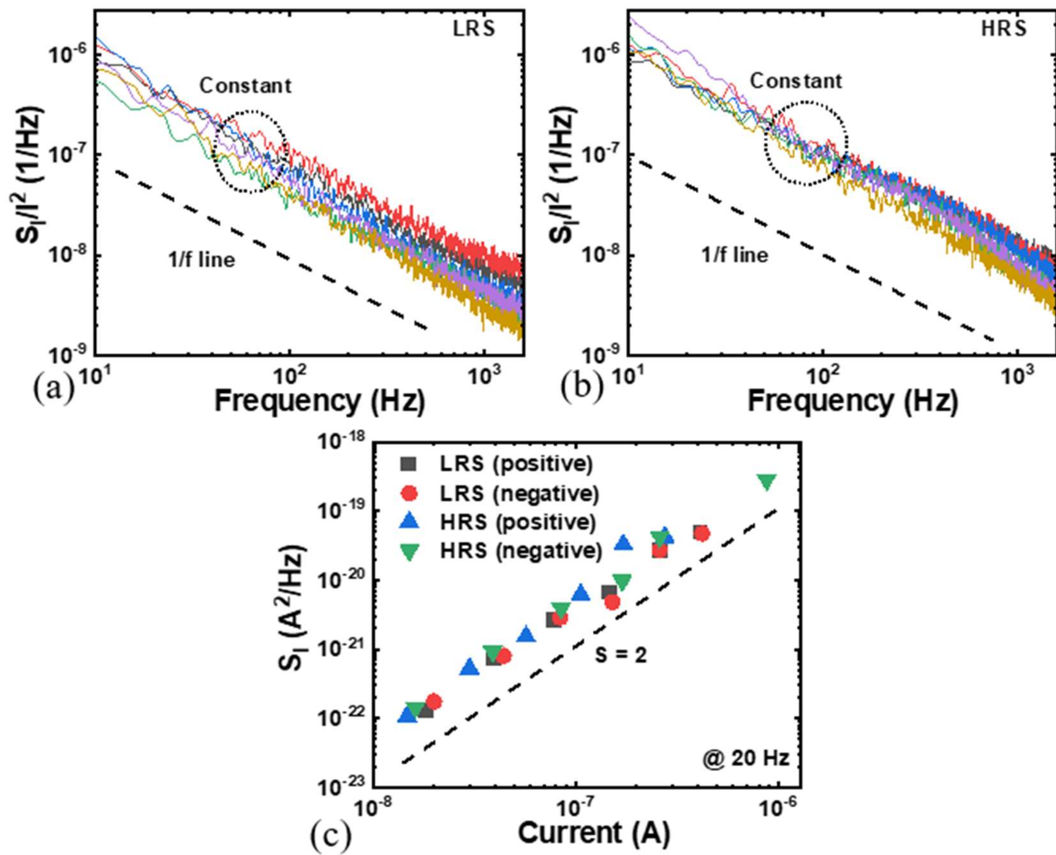


Fig. 4.14. S_i/I^2 according to the voltage in (a) LRS and (b) HRS. (c) The logarithmic plot of the current dependence of the S_i at 20 Hz in LRS and HRS.

Chapter 5

Random telegraph noise (RTN) in RRAM

5.1 Introduction to RTN

The random telegraph noise (RTN) is characterized by a random switching of an observable quantity, (e.g., voltage, current) between two or more levels along time [77]. It has been recognized as a significant variability source since it is responsible for device parameter variation, such as the ΔV_{th} at normal operation conditions. The first observation of RTN in MOSFETs was reported in 1984 [78]. Since then, RTN has been found in many different semiconductor devices including MOSFETs, LEDs, Flash memories, FinFET, and emerging memories such as RRAM devices [79-82]. The RTN is caused by the capture and emission of charge carriers by oxide and interface defects in semiconductor devices. As the device size shrinks, RTNs become much more prominent, resulting in functional or permanent failures in digital logic circuits and memories [77]. Fig. 5.1 shows the schematic

RTN signal. Two-level RTN signal is characterized by three parameters: the fluctuation amplitude (ΔI), the mean elapsed time (τ_c) before the trap captures a charge carrier, and mean elapsed time (τ_e) before the trap emits a charge carrier [78]. In generally, τ_c/τ_e is called capture/emission time constant.

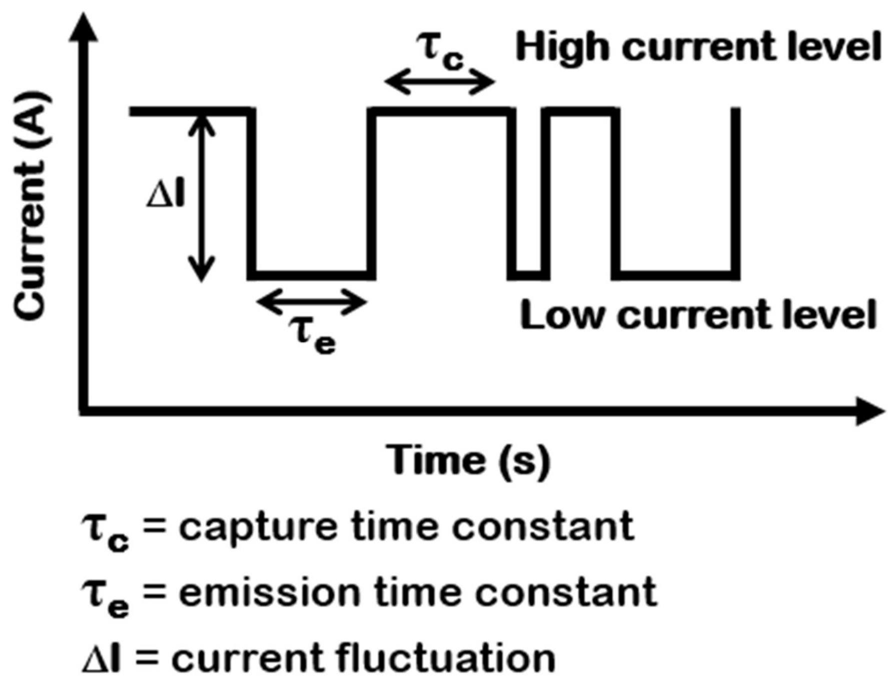


Fig. 5.1. Schematic tow-level RTN signal showing its parameters (ΔI,τ_c, and τ_e).

5.2 RTN in RRAM

5.2.1 Methodology for extracting trap information in RRAM

Fig. 5.2(a) shows simple schematic model elucidating the generation of the RTN in RRAM devices. During the stochastic formation and rupture processes of percolation pathways (CFs) in the oxide, Discrete level switching can be observed due to trapping (capture) and de-trapping (emission) of an electron from a trap when only one dominant pathway is formed and the trap exists near the pathway. Basic model for extracting trap information (trap energy level and depth) can be easily derived because the fundamental RRAM structure is the MIM. Fig. 5.2(b) shows the energy band diagram of the MIM structure, from which we can see the relationship between the energy level (E_T) and the depth (x_T) of the trap. The fractional occupancy of the trap is governed by equation (12) [83]:

$$\frac{\tau_c}{\tau_e} = exp\left(\frac{E_T - E_F}{k_B T}\right), \quad (12)$$

where k_B is the Boltzmann constant, T is the absolute temperature, τ_c and τ_e are the mean capture and emission time constants, respectively, E_T is the trap energy level, and E_F is the Fermi level. From the energy band diagram of the Fig. 5.2(b),

the expression for the capture and emission times in terms of the position of the trap can be derived as equation (13):

$$k_B T ln \frac{\tau_c}{\tau_e} = \Phi_0 - [(E_{Cox} - E_T) + E_x], \quad (13a)$$

$$E_x = q \frac{x_T}{T_{ox}} V_{ox}, \quad (13b)$$

where Φ_0 is the difference between the work function of metal electrode and electron affinity of the oxide, E_{Cox} is the conduction band edge of the oxide, q is the elementary charge, T_{ox} is the oxide thickness, x_T is the position of the trap in the oxide from BE, and V_{ox} is the oxide voltage drop which is the same as the applied bias. Eqs. (13a) and (13b) can be used to find the trap energy ($E_{Cox} - E_T$). Also, by differentiating eq. (13a) according to the voltage, the x_T is derived as equation (14):

$$x_T = -\frac{k_B}{q} T_{ox} \frac{\partial}{\partial V} \left(ln \frac{\tau_c}{\tau_e} \right). \quad (14)$$

From Eq. (14), it can be seen that by examining the bias dependence of τ_c and τ_e, the location information of the trap causing the RTN can be obtained. Trapping and de-trapping of charge carriers through traps in the oxide exhibits a variety of processes. Fig. 5.3 shows four types of capture/emission processes of charge carriers via traps [84]. The process① shows the case that the electron is captured

from the electrode and then emitted to the opposite electrode in which case τ_c and τ_e show the same polarity of the bias dependence. The process② shows the case that the electron is captured from the electrode and then thermally emitted to the conduction band of the oxide in which cases the τ_e is independent on the bias (since $E_{Cox} - E_T$ is constant). The process③ and ④ show the cases that the electron is captured from the electrode and then emitted back to the same electrode in which cases τ_c and τ_e show the opposite polarity of the bias dependence. Meanwhile, the distinction between processes 1 and 2 can be understood through the energy band diagram in Fig. 5.2(b) and the increase/decrease of the time constants according to the bias. For example, if the trap interacts with the BE, E_T becomes close to E_F as the voltage increases. Consequently, the capture probability of the electron at the BE increases due to the decrease in the $E_T - E_F$, resulting in the decrease in τ_c. Conversely, τ_e increases. If the trap interacts with the TE, as the voltage increases, τ_e decreases and τ_c increases. Since eqs. (12) to (14) apply only to processes③ and ④, our experiments to analyze the trap information focus only on those.

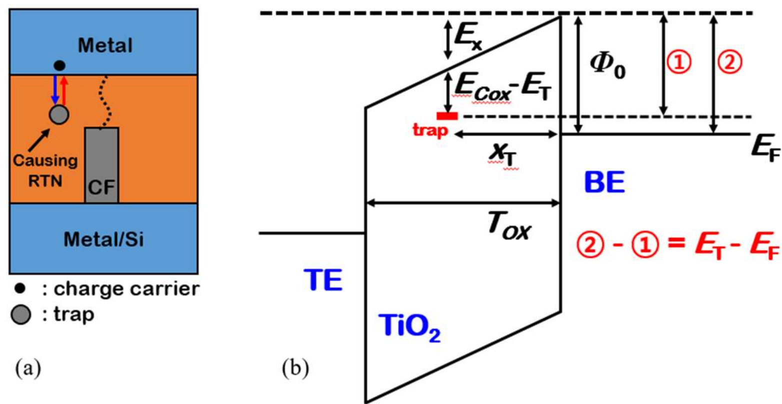


Fig. 5.2. (a) Illustration of two-level RTN mechanism in RRAM device. (b) Energy band diagram of the MIM structure considering the trap energy level (E_T) and depth (x_T).

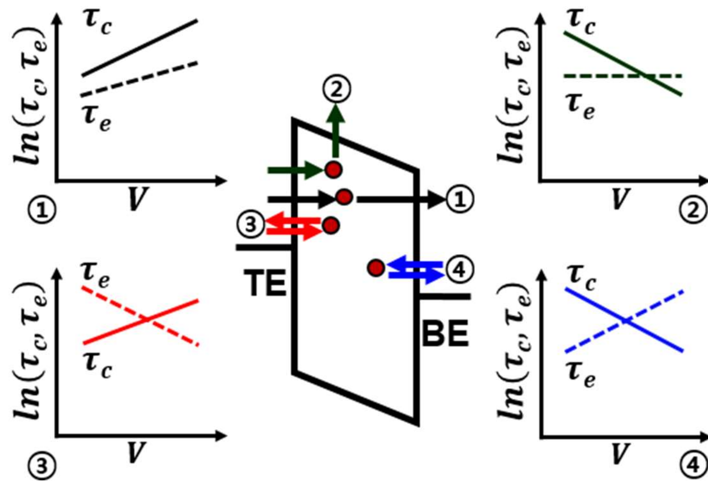


Fig. 5.3. Energy band diagram illustrating various capture/emission processes and

their corresponding bias dependences of τ_c and τ_e [84].

5.2.2 Experimental results

To observe a clear two-level RTN, we chose the SLRRAM with a cell size of < 100 × 100 nm^2 as the experimental devices (Fig. 4.11(c)). Figure 5.4 shows measured read current fluctuations (ΔI) for the SLRRAM in HRS. In the HRS, various levels of RTN were observed because two or more traps are activated under applied energy. Unlike the HRS, discrete current fluctuations were rarely observed in the LRS. This is because most of the traps in the TiO2 are filled with mobile ions such as O^{2-} during the resistive switching process (HRS to LRS), so the probability of the RTN being observed is low [85]. Fig. 5.5 shows time records of the ΔI_{read} according to the voltage. As can be seen in Fig. 5.5(b), clear two-level RTN characteristics are observed. To extract trap information, τ_c and τ_e can be obtained from the data of Fig. 5.5. As shown in Fig. 5.6(a), the trap interacts with the BE because τ_c decrease and τ_e increases. Also, Fig. 5.5(b) shows the dependence of $\ln(\tau_c/\tau_e)$ on the voltage. The dotted line represents linear fitting

result for extracting the x_T, which can be obtained by using the eq. (14). Extracted x_T is 5.7 nm from the BE. Additionally, from eq. (13) and the extracted x_T, we can find the trap energy. The extracted $E_{Cox} - E_T$ is 0.23 eV, and this value is similar to the theoretically calculated point defects of rutile TiO_{2-x} [86]. In the same way as above, we additionally extracted information about traps showing various capture/emission processes. Fig. 5.7(a) shows the result of extracting trap information that interacts with the BE. Fig. 5.7(b) is the result of extracting trap information that interacts with the TE. Finally, Fig. 5.7(c) is the experimental result of the trap corresponding to the process② of Fig.5.3. The location and energy of all extracted traps are summarized in Fig. 5.7(d).

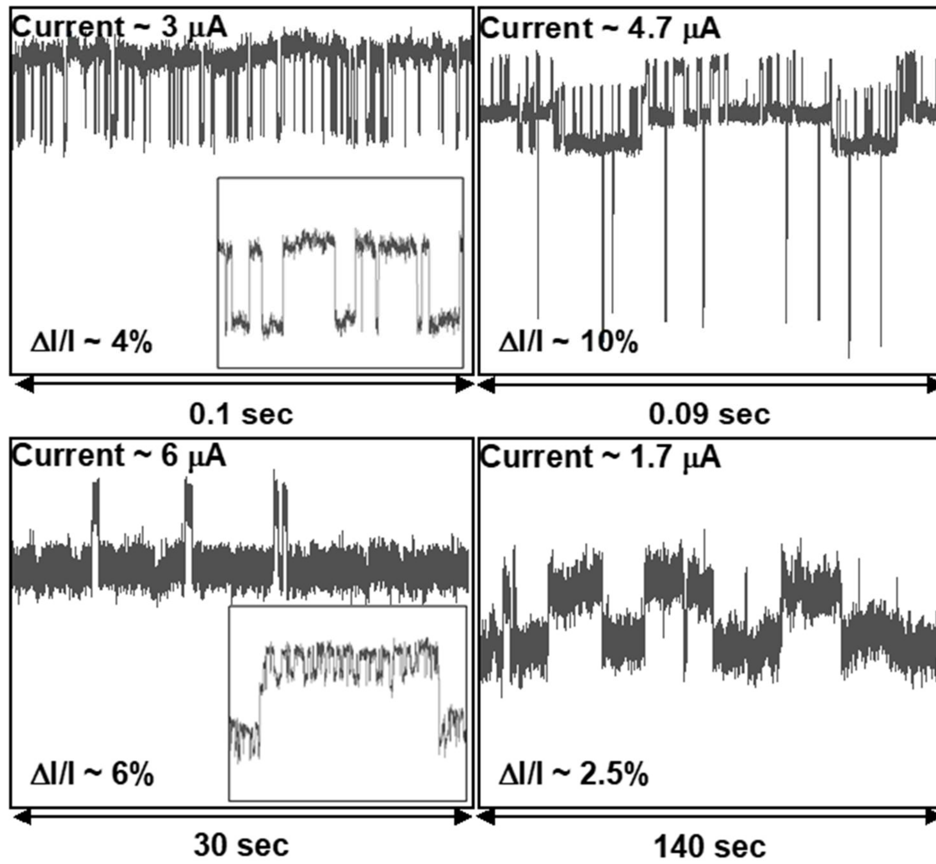


Fig. 5.4. Read current fluctuations (ΔI) for SLRRAMs with a cell size of < 100 × 100 nm^2 in HRS.

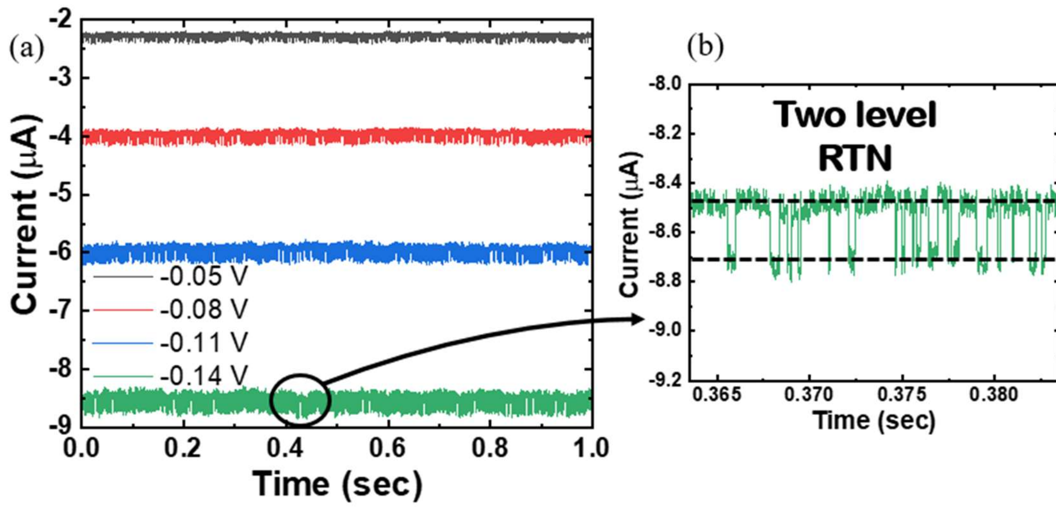


Fig. 5.5. (a) ΔI_{read} according to the voltage in the time domain. (b) Enlarged graph of ΔI_{read} at -0.14 V showing the clear two-level RTN.

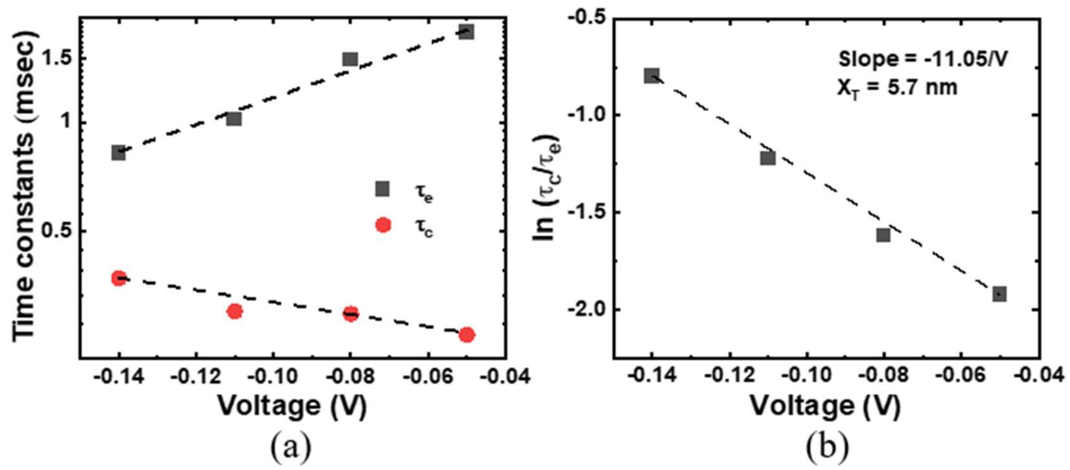


Fig. 5.6. (a) τ_c and τ_e on the voltage. (b) Dependence of $\ln(\tau_c/\tau_e)$ on the voltage.

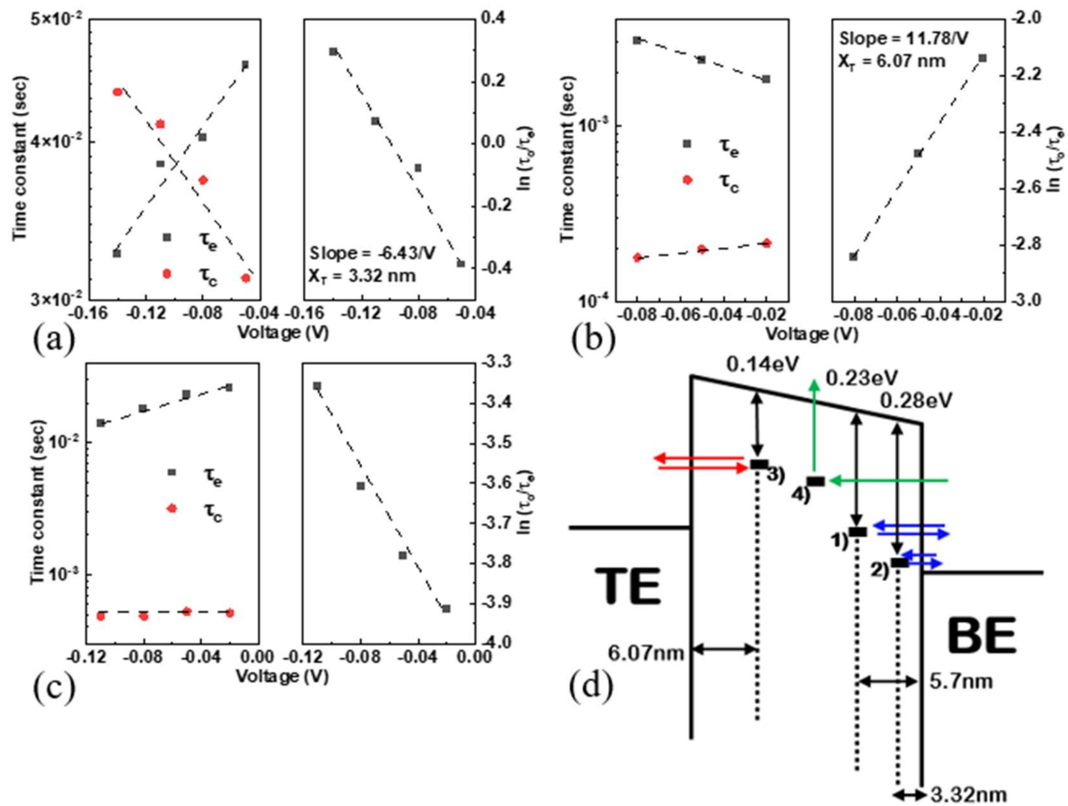


Fig. 5.7. Dependence of $\ln(\tau_c/\tau_e)$ about the trap corresponding the process (a) ④, (b) ③, and (c) ② on the voltage. (d) Energy band diagram showing the location and energy level for 4 traps.

Chapter 6

Conclusions

In this dissertation, LFN characteristics of metal oxide-based RRAM devices were experimented and analyzed. A total of 4 types of devices were fabricated for the experiment, and each device operates as a mechanism of TCM, interface-type VCM, CF-type VCM, and EEM. After the verification process for various devices, we suggested that the LFN measurement can be used as an effective tool to analyze resistive switching mechanism, MLC operation, degradation mechanism, and conduction mechanism of RRAM devices together with *I-V* fitting and temperature measurement or physical characterization techniques. For TCM and VCM RRAMs, the normalized PSD in the HRS is higher than that in the LRS, but there is no significant difference in the noise PSD level according to the states in the EEM RRAM. It has to do with the RS mechanism of the RRAM. In the CF-type RRAM, localized oxygen vacancy is a dominant noise source in the LRS, and the noise

characteristic of the HRS state is the bulk effect. Also, in the interface-type RRAM, the noise characteristics of both resistance states are the bulk effect. In terms of the noise, the I_{cc} mode is more advantageous than the V_{reset} mode during the MLC operation of the RRAM. When analyzing the degradation mechanism of RRAM devices having a conduction mechanism with trap-controlled SCLC, the LFN measurement result is a good basis to support the analysis results because the amount of change in the trap during resistive switching cycles can be indirectly confirmed through noise measurement. In RRAM devices, Vo traps give rise to the RTN, which can be an obstacle to device scaling and MLC operation, so it should be continuously studied. Basic model for extracting trap information (trap energy level and depth) can be easily derived because the fundamental RRAM structure is the MIM. From the derived equation, we proposed a methodology for RTN analysis in RRAM and applied it to an CF-type VCM RRAM to extract trap positions and energies. The results of this study are expected to be widely used in related research fields for RRAM analysis as a new electrical characterization technique.

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초 록

현재의 메모리 계층도를 보면 CPU는 고속 동작을 요구하고, 외부메모리는 고용량을 필요로 하기 때문에, 현재의 주요 메모리 기술인 DRAM과 NAND Flash 메모리의 성능 격차는 지속적으로 늘어나고 있다. 하지만 데이터 양의 폭발적인 증가로 인한 데이터 처리 속도 문제, 그리고 오래전부터 제기 되어왔던 기존 메모리의 물리적 한계를 해결하기 위해서 새로운 메모리 기술에 대한 필요성이 증가하고 있다. 또한 기존 폰노이만방식의 컴퓨터 시스템 구조의 문제점을 해결하기 위한 방법인 In-Memory Process를 실현하기 위한 방법으로 DRAM의 high speed, 그리고 NAND Flash의 high density 모두를 만족하는 SCM (storage class memory) 기술에 대한 관심이 증가하고 있다.

SCM 후보군 중에서, 저항 변화 메모리 소자인 RRAM (Resistive Random Access Memory)은 MIM, cross-point 형태의 간단한 구조를 가지며, 공정 상 집적도 향상에 유리하고, 사용되는 물질이 CMOS공정과 호환 가능하다. 이러한 장점들로 인해 기존 Flash 메모리 소자의 대안으로 학계에서 많은 연구가 진행 되어 왔지만, 한 단계 앞서 연구가 진행되었던 PCM (Phase change RAM)이 겪고 있는 신뢰성 문제가 RRAM에서도 재현되고 있다. RRAM의 신뢰성 문제는 RRAM의 저항 스위칭 메커니즘 자체가 근본적으로 확률적이기 때문에 본질적 변동성에서 기인하는 것이다.

본 논문의 주요 내용은 RRAM의 신뢰성 향상을 위해서 새로운 전기

적 분석기법을 개발하는 것이다.

우선 다양한 메커니즘으로 동작하는 RRAM소자의 기본적인 저주파 잡음 특성을 분석하고, 이를 소자의 전도 메커니즘 및 저항 변화 메커니즘과의 연관성을 검증하였다. 측정결과를 기존 저주파 잡음 이론을 통해 해석하고, 다양한 소자에 이를 적용시켜 저주파 잡음 분석 기법이 RRAM의 동작 메커니즘 분석에 이용할 수 있음을 증명하였다.

또한, 소자의 열화 메커니즘 및 MLC (Multi-Level Cell) 분석에 있어서도 저주파 잡음 측정이 추가적인 분석기법이될 수 있음을 제시하였다.

마지막으로, 소자의 저주파 잡음 특성 중 하나인 RTN (Random Telegraph Noise)특성 분석을 통해 셀의 fail 을 일으킬 수 있는 trap의 위치 및 에너지를 추출하는 연구를 진행하였다. RRAM의 trap정보 추출에 관한 측정 및 분석은 본 연구에서 최초로 진행되었던 것이고, 이후 RRAM의 RTN분석에 가이드라인을 제시하였다.

주요어: 저항 변화 메모리, 전도 메커니즘, 신뢰성, 저주파 잡음, RTN,

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List of Publications

Journals

1. **Jung-Kyu Lee**, Hu Young Jeong, In-Tak Cho, Jeong Yong Lee, Sung-Yool Choi, Hyuck-In Kwon, and Jong-Ho Lee, "Conduction and Low-Frequency Noise Analysis in Al/α-TiO_X/Al Bipolar Switching Resistance Random Access Memory Devices," *IEEE Electron Device Letters*, vol. 31, vo. 6, p. 603, Jun. 2010.
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