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Double-Hybrid Spread-Spectrum Technique for Conducted-EMI Reduction in DC-DC Switching Regulators with FPGA-Based Controller

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Abstract — The purpose of this paper is to present a novel technique for conducted-noise reduction in dc-dc switching regulators. In order to effectively spread the conducted-noise frequency spectrum and, at the same time, attain a satisfactory voltage regulation, two parameters (carrier frequency and pulse position) have been randomized, and the third parameter (duty ratio) has been controlled by a digital compensator. Furthermore, the effect of using the proposed controller on common-mode, differential-mode, and total conducted-noise characteristics of the converter has been experimentally investigated. The converter's performance with using the proposed technique has been experimentally investigated. It is assumed that the implementation technology is a field programmable gate array (FPGA) which is becoming increasingly adopted in industrial electronic applications.

Index Terms—DC-DC power conversion, Electromagnetic interference, Electromagnetic compatibility, Spread-Spectrum, Field programmable gate arrays.

I. INTRODUCTION

Telecommunication central offices, industrial automation, energy-efficient consumer appliances, photovoltaic installations, and mobile phones do not appear to have much in common, but all rely on electronic power converters for operation [1].

The large markets for mobile phone handsets, laptop computers and PDAs are becoming commodity oriented; it is one of the major forces driving demand for the high growth of dc-dc converters.

Switching power converters (SPCs) generate considerable electromagnetic interference (EMI) noise on account of the high dv/dt and di/dt during the switching instant of the power devices. Several international standards (e.g., CISPR, FCC, and VDE) impose limits on the amount of EMI noise that a converter can inject into the utility supply [2]-[3].

Several methods have been reported in literature to mitigate the EMI problem. These techniques include common tools such as passive filters and shields [3]. However, that will put increased pricing pressures on dc-dc converters.

In general, although the various EMI mitigation techniques reduce the EMI noise injected by the SMPS into the supply mains, often an input passive filter is still required to meet the standards [4].

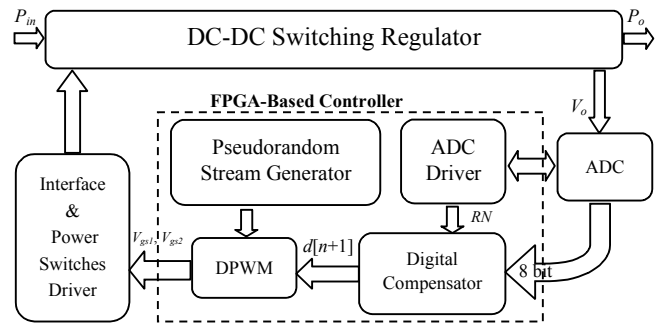


Fig. 1. Block diagram of the DC-DC switching regulator with FPGA-based controller.

The main source of EMI emissions in power converters comes from switching of dc voltages following a constant scheme. Waveforms of interest are typically periodic functions of time. The peaks of EMI are mainly concentrated on multiples of switching frequency. However, in the case of spread-spectrum techniques, even though the energy of harmonics is spread over a frequency belt, the peak of harmonics drastically decreases [5]. This paper proposes a spread-spectrum technique for conducted EMI reduction in dc-dc switching regulators.

In the last few years, the trend to use concurrent hardware for control purposes is increasing, and field-programmable gate arrays (FPGAs) are becoming more popular since they provide higher performances in repetitive and massive computations [6]-[7]. The implementation of proposed spread-spectrum technique has been accomplished by using an FPGA-based controller as shown in Fig. 1.

The paper is organized as follows: Section II presents the idea of the double-hybrid spread-spectrum technique and the digital compensator design. The design and implementation of the proposed FPGA-based controller are addressed in section III. Section IV describes the details of the experimental work. The results and discussion are provided in section V. Finally, conclusions are presented in section VI.

II. DOUBLE-HYBRID SPREAD-SPECTRUM TECHNIQUE

A. Basic Idea

According to Fig. 2, T_k is the duration of the k th cycle, α_k is the duration of the on-state within this cycle, and ε_k is the delay from the starting of the switching cycle to the turn-on within the cycle. Note that the duty ratio is $d_k = \alpha_k / T_k$ and the switching frequency $F_k = 1/T_k$. The switching function $q(t)$ consists of a series of such switching cycles.

In order to spread the frequency spectrum of the switching noise and, at the same time, attain a satisfactory voltage regulation, two parameters; $\{F_k, \varepsilon_k\}$ have been randomized, and the third parameter; $\{d_k\}$ has been controlled by the digital compensator.

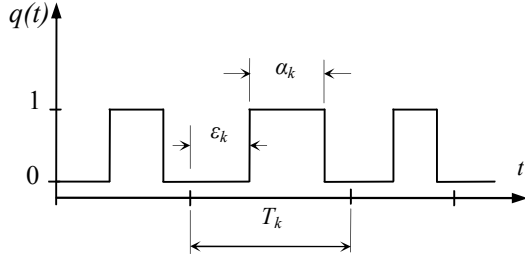


Fig.2. Characteristic parameters in the switching signal.

B. Digital Compensator Design

The digital controller has been designed by emulation approach. This allows the controller to be designed in the s -domain and then converted into a discrete/digital controller [8]. Different types of compensators have been studied. The Proportional-Integral-Derivative (PID) improved compensator attains a good voltage regulation performance which suits the case study. The PID continuous time equivalent, $G_c(s)$ is:

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{s}{\omega_z}\right) \left(1 + \frac{\omega_L}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \quad (1)$$

where;

- the parameter $G_{cm} = 0.3044$,
- the zero frequency; $f_z = \omega_z / 2\pi = 3.0518$ kHz,
- the pole frequency; $f_p = \omega_p / 2\pi = 73.727$ kHz,
- the inverted zero frequency; $f_L = \omega_L / 2\pi = 1.5$ kHz.

As shown in Fig. 3, the Pole-Zero match transformation method was applied on the analog controller $G_c(s)$, using MATLAB [9]–[11], to obtain the discrete one; $G_c(z)$ as follows:

$$G_c(z) = \frac{U}{E} = \frac{(3.973Z^2 - 7.578Z + 3.612)}{(Z^2 - 1.213Z + 0.2135)} \quad (2)$$

Where, U is the control output, E is the error voltage, and the sampling time is $T_s = 1/f_s$. In discrete form, the control law is written as:

$$U[n] = 1.213U[n-1] - 0.2135U[n-2] + 3.973E[n] - 7.578E[n-1] + 3.612E[n-2] \quad (3)$$

The quantities with (n) denote the sampled values for the current sampling cycle, the quantities with $(n-1)$ denote one sample old values and so on.

As clear in Fig. 3, the sampling and hold process introduced an additional phase delay of more than 10 degrees compared to the equivalent analog controlled power supply.

However, for the case study, a 3.3 V computer processor power supply, the voltage must not be allowed to overshoot to 5 or 6 volts when the supply is turned on. This may destroy the integrated circuits in the computer motherboard. Thus the Q -factor must be sufficiently low, 0.5 or less, corresponding to a phase margin of at least 76° [8].

To fulfill the above condition, the controller has been redesigned again [11]. Coefficients are determined based on the poles-zeros cancellation approach: the controller zeroes are selected to cancel the poles of the discrete transfer function.

The control law described by (3) is rewritten in the following form:

$$U[n] = U[n-1] + 2E[n] - 3.968E[n-1] + 1.9786E[n-2] \quad (4)$$

Figure 4 shows the digital control loop bode plot at different loading conditions.

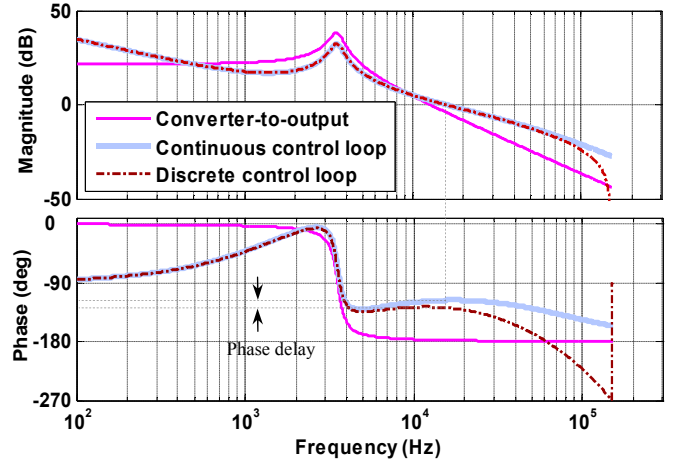


Fig. 3. Continuous and discrete control loop bode plots; (sampling and hold introduces phase delay of more than 10°).

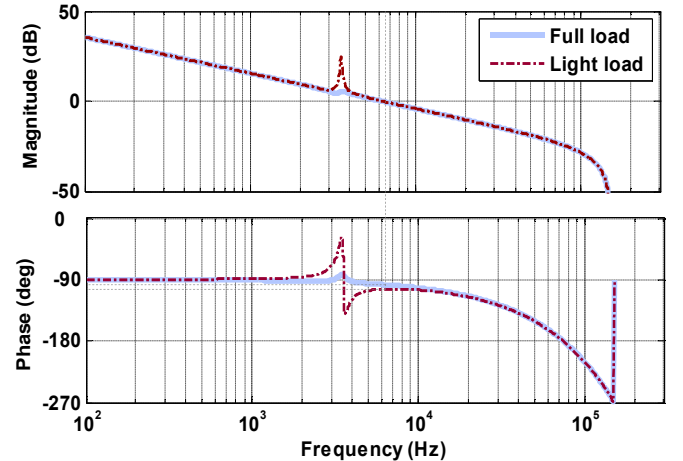


Fig. 4. Digital control loop bode plot at different loading conditions; (Full load: $I_o = 5$ A, Light load: $I_o = 0.5$ A, Phase margin always $> 76^\circ$).

III. FPGA-BASED IMPLEMENTATION

A. Pseudorandom Stream Generator

In order to spread the noise spectrum, both F_k and ε_k are randomized. Thus, two random number generators are required to realize the proposed technique.

As shown in Fig. 5, a pseudorandom stream generator has been constructed for this purpose. The proposed construction uses several maximum length linear feedback shift registers (m-LFSRs) in parallel. For different m-LFSR output bits, different initial contents of m-LFSRs (seeds) are used [12]. It delivers two different random streams: 16-bit and 11-bit streams. The streams are composed of the output bits of the m-LFSRs with different arrangements. For detailed description of the generator, the reader is referred to [13]-[14].

Only at the beginning of every switching cycle, the random output bits are converted into an integer numbers and used in the digital pulse-width modulator (DPWM). However, the other generated random output bits are discarded.

B. Digital Pulse Width Modulator

At the beginning of every switching cycle, the DPWM achieves the following assignments:

1. Converting the pseudorandom streams into integer numbers.
2. Calculating randomization parameters for the started switching cycle and the needed number of steps to fulfill switching frequency, duty-ratio, and pulse position (TN , WN , and EN respectively as shown in Fig. 6.

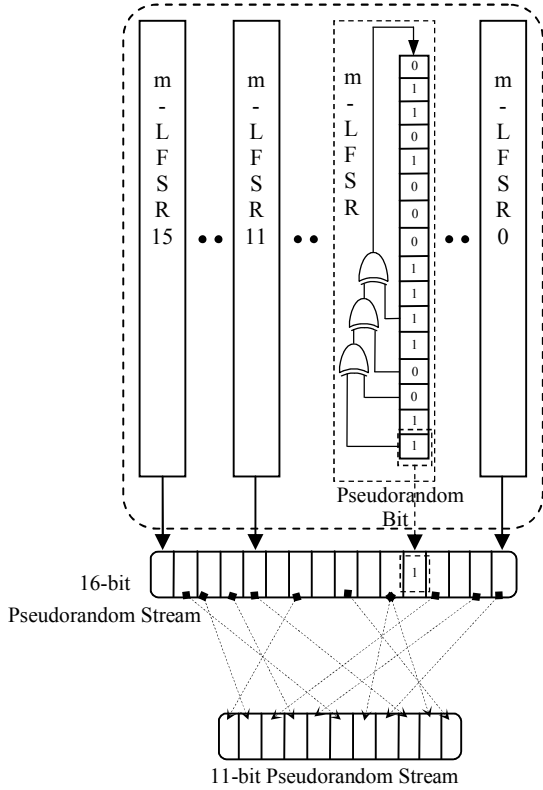


Fig. 5. The proposed pseudorandom stream generator.

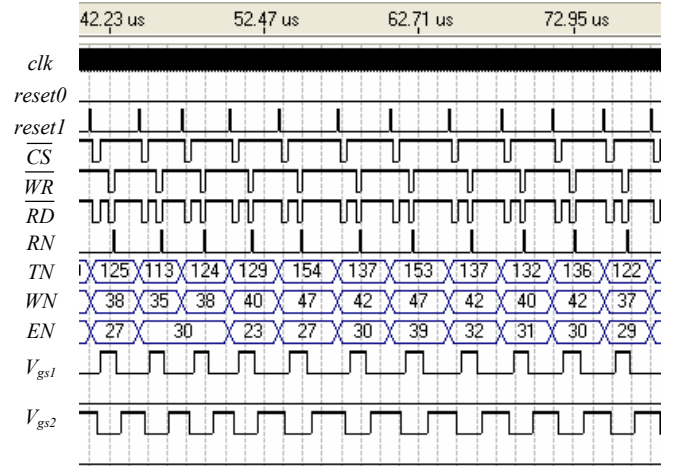


Fig. 6. VHDL simulation of the proposed FPGA-based controller with the double-hybrid technique.

3. Generating the digital pulse width modulated waveforms ($V_{gs1,2}$) with the identified randomization parameters. As shown in Fig. 6, the designed DPWM uses a clocked counter with increments up to TN that resets at the end of every switching cycle of the PWM (see $reset1$ signal). The gate signals ($V_{gs1,2}$) are generated in the following way:

- To generate V_{gs1} : When the counter value lies between the reference values $\{EN, EN+WN\}$, the controller keeps the PWM output state high, otherwise it remains low.
- To generate V_{gs2} : DT denotes the required number of clock steps to fulfill the dead time. When the counter value lies between the reference values $\{EN-DT, EN+WN+DT\}$, the controller keeps the PWM output state low, otherwise it remains high.

IV. EXPERIMENTAL VERIFICATION

As described in Fig. 7 and 8, the line impedance stabilization network (LISN) is used to standardize the input impedance seen from the converter input and sense the conducted-noise. A high-frequency current probe (C-Probe) is used to sense both the common-mode and differential-mode noise currents that are measured by an EMI receiver [3].

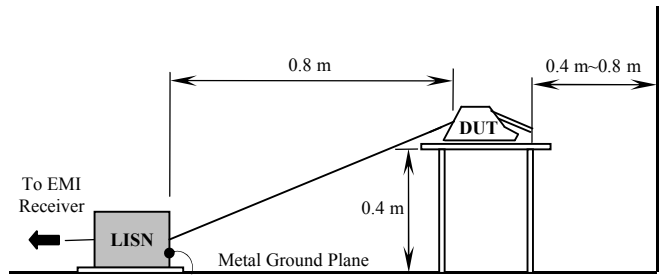


Fig. 7. Conducted-noise measurement system.

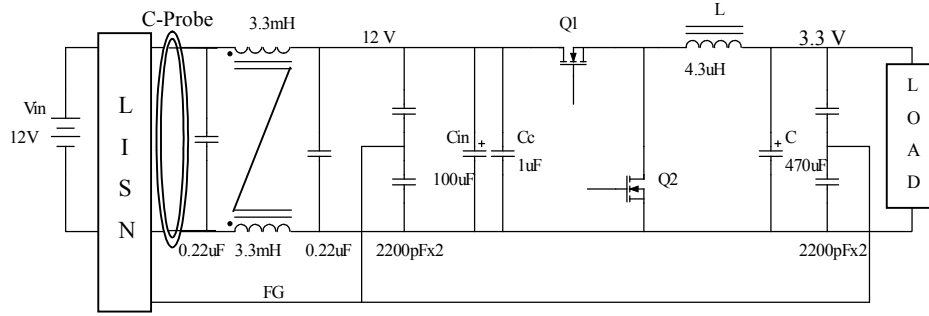


Fig. 8. Experimental converter circuit configuration.

TABLE I
RANDOMIZATION PARAMETERS FOR VARIOUS STUDIED CASES

Case	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
$\pm\Delta F_k$, % of f_{csw}	0				10.92				21.85				32.77			
$\Delta\epsilon_k$, % of T_k	0	6.25	12.5	25	0	6.25	12.5	25	0	6.25	12.5	25	0	6.25	12.5	25

The randomly switched dc-dc converter was designed and implemented using an Altera FPGA. A synchronous buck converter topology was selected to improve efficiency and reduce heat loss. The output inductor and capacitor were sized such that the converter operates in a continuous conduction mode (CCM).

Noise measurements were taken at: $V_{in} = 12$ V, $V_o = 3.3$ V, and $I_o = 5$ A with a center switching frequency $f_{csw} = 300$ kHz and resolution band width of the spectrum analyzer $RBW = 9$ kHz.

The two randomization parameters were swept to identify the values that achieve the best conducted-noise spectrum spreading as follows:

1. The switching frequency randomization ratio (ΔF_k), (0, ± 10.92 , ± 21.85 , and $\pm 32.77\%$ of f_{csw} were used).
2. The pulse position randomization ratio ($\Delta\epsilon_k$), (0, 6.25, 12.5, and 25% of T_k were used).

All the sixteen studied cases were designed, implemented, and experimentally investigated. Then the conducted-noise spectra were compared.

V. RESULTS AND DISCUSSION

A comparison was carried out between all the studied cases to identify the case that achieves the best conducted-noise spectrum spreading. It is clear from Figs. 9–11 that the noise peaks are concentrated in two regions: the first region in the low-frequency range (0.15–1 MHz) around the center switching frequency and the other region in the high-frequency range (1–30 MHz).

As presented in Figs. 9 and 10, with randomizing one parameter only (i.e. random pulse position (RPP) or random switching frequency (RSF)) the conducted-noise spectrum hasn't been significantly improved in the high-frequency range. Moreover, it increases the conducted-noise peak in the low-frequency range.

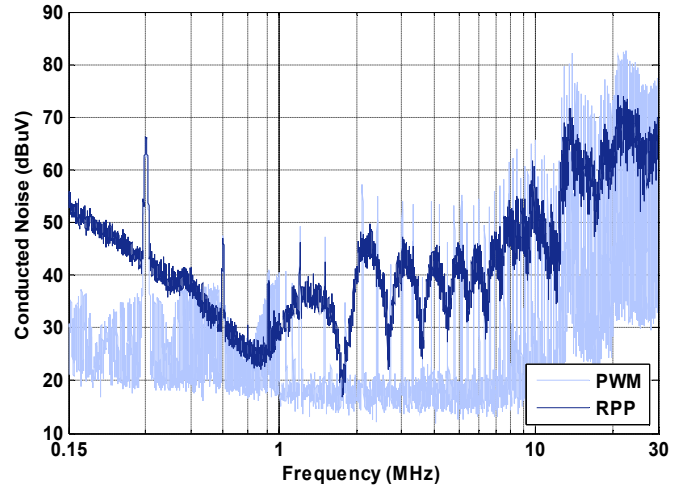


Fig. 9. Comparison between the conducted-noise spectrum with the basic pulse width modulation (PWM) and that with randomized parameters (random pulse position (RPP), $\Delta\epsilon_k = 12.5\%$ of T_k).

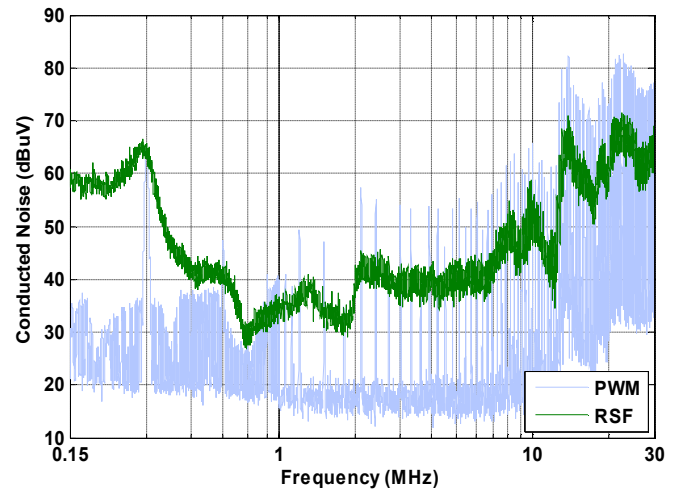


Fig. 10. Comparison between the conducted-noise spectrum with the basic pulse width modulation (PWM) and that with randomized parameters (random switching frequency (RSF), $\Delta F_k = \pm 21.85\%$ of f_{csw}).

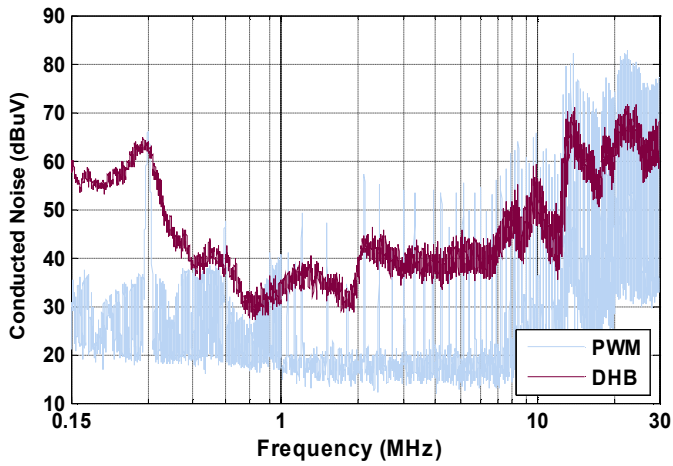


Fig. 11. Comparison between the conducted-noise spectrum with the basic pulse width modulation (PWM) and that with randomized parameters (DHB, $\Delta F_k = \pm 21.85\%$ of f_{csw} and $\Delta \epsilon_k = 12.5\%$ of T_k).

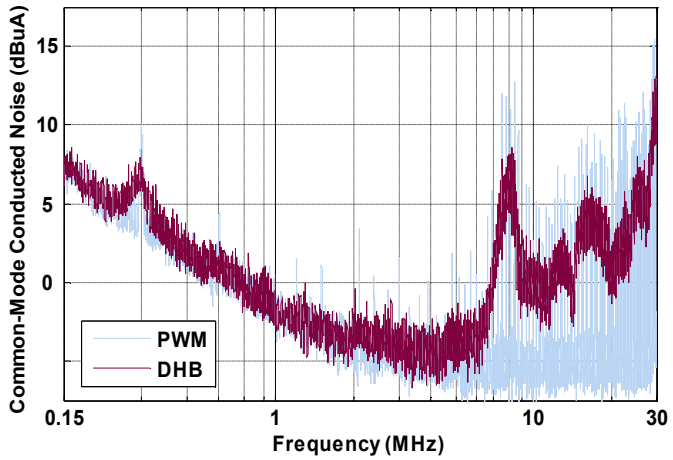


Fig. 12. Comparison between common-mode noise current spectrum with the basic pulse width modulation (PWM) and that with randomized parameters (DHB, $\Delta F_k = \pm 21.85\%$ of f_{csw} and $\Delta \epsilon_k = 12.5\%$ of T_k).

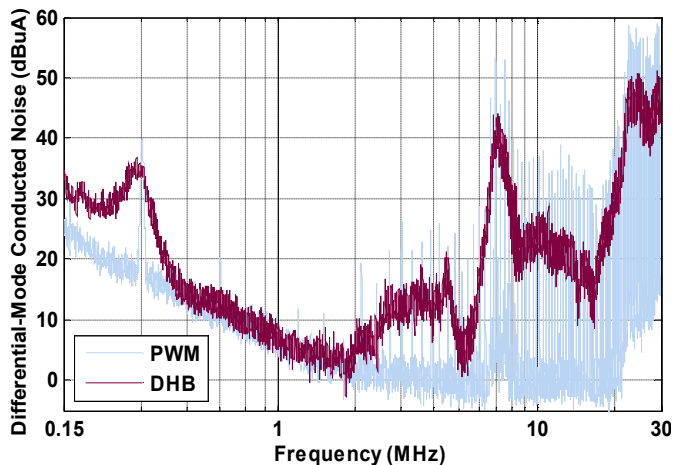


Fig. 13. Comparison between differential-mode noise current spectrum with the basic pulse width modulation (PWM) and that with randomized parameters (DHB, $\Delta F_k = \pm 21.85\%$ of f_{csw} and $\Delta \epsilon_k = 12.5\%$ of T_k).

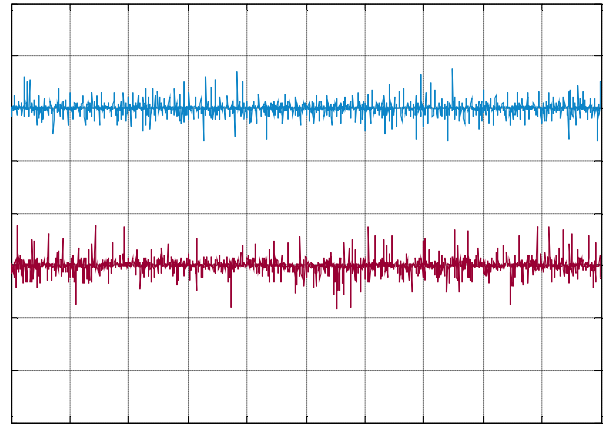


Fig. 14. The effect of using the proposed technique on the measured converter output voltage ripple: upper waveform with using the basic pulse width modulation (PWM) and lower waveform with using randomized parameters (DHB, $\Delta F_k = \pm 21.85\%$ of f_{csw} and $\Delta \epsilon_k = 12.5\%$ of T_k) at vertical: 2.5 V/div, horizontal: 250 μ s/div.

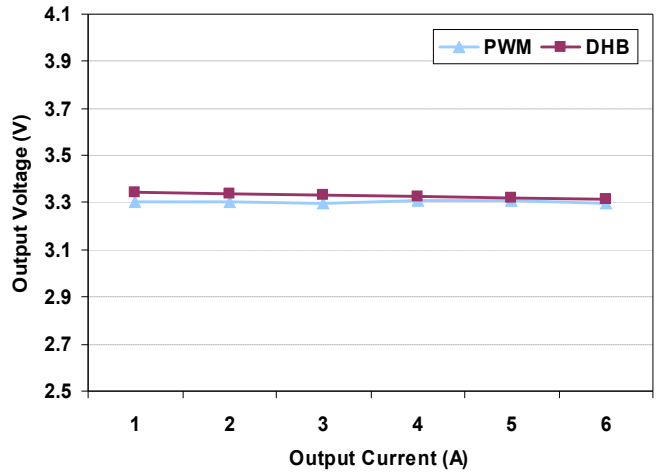


Fig. 15. The effect of using the proposed technique (DHB) on the converter measured output characteristics of the converter.

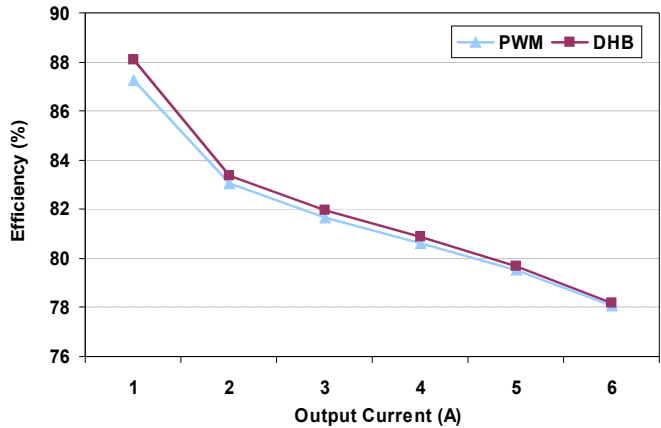


Fig. 16. The effect of using the proposed technique (DHB) on the measured efficiency of the converter.

However, using the proposed technique, case 11 with the randomized parameters ($\Delta F_k = \pm 21.85\%$ of f_{csw} and $\Delta \varepsilon_k = 12.5\%$ of T_k) attains the best performance. As shown in Fig. 11, the conducted-noise spectrum reduced by 1.1 dB at low-frequency range and 11 dB at high-frequency range.

Furthermore, the common-mode noise reduced by 2.8 dB at low-frequency range and 4.7 dB at high-frequency range, as presented in Fig. 12. In addition, the differential-mode noise reduced by 3.1 dB at low-frequency range and 7.9 dB at high-frequency range, as illustrated in Fig. 13.

In order to investigate the influence of using the proposed randomized technique of the converter's normal operation (i.e. dc-dc conversion at an acceptable output voltage quality), different experimental measurements were achieved. The effect of using the proposed technique on the measured converter output voltage ripple is presented in Fig. 14. Furthermore, the effect of using the proposed controller on the converter output characteristics is illustrated in Fig. 15. It is clear that the output voltage has been well-regulated using the proposed controller. Moreover, the measured efficiency of the converter hasn't been deteriorated by using the proposed technique, as shown in Fig. 16.

VI. CONCLUSIONS

A novel technique has been designed and implemented for conducted-noise reduction in dc-dc converters. Furthermore, the effect of using the proposed controller on common-mode, differential-mode, and total conducted-noise characteristics of the converter has been experimentally investigated. To investigate the influence of using the proposed randomized technique of the converter's normal operation (i.e. dc-dc conversion at an acceptable output voltage quality), different experimental measurements were achieved. Finally, experimental results show that using the proposed technique, the conducted-noise spectrum has been significantly improved and the noise level has been effectively reduced at both high- and low-frequency ranges. Moreover, using the proposed randomized technique didn't deteriorate the converter's normal operation.

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