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6-channel CMOS-based instrument for optical absorption spectroscopy and chemical identification

Francesco Zanetto[1], Katherine Stoll[2], Samuel Serna[3], Anuradha Agarwal[2], Marco Sampietro[1] and Giorgio Ferrari[4]
[1] *Department of Electronics, Information and Bioengineering, Politecnico di Milano, Italy*
[2] *Department of Materials Science & Engineering, Massachusetts Institute of Technology, USA*
[3] *Department of Physics, Photonics and Optical Engineering, Bridgewater State University, USA*
[4] *Department of Physics, Politecnico di Milano, Italy*
Email: francesco.zanetto@polimi.it

***Abstract*—A multichannel portable instrument for on-chip optical absorption spectroscopy is presented. The system can house photonic chips having up to 6 sensing sites operating in parallel, allowing real-time simultaneous detection of multiple chemicals. A 6-channel CMOS lock-in front-end performs the amplification and demodulation of the signals from the integrated light detectors, while an FPGA is chosen for signal acquisition and analysis. A digital real-time ratiometric processing cancels out the effect of laser power fluctuations to achieve high sensitivity in monitoring the presence of the analytes, as demonstrated with the detection of an acetone sample. Compact size for portability, real-time parallel detection and flexible FPGA processing make this system suitable for environmental investigations on many different pollutants, both in the near- and mid-infrared wavelength range.**

***Index Terms*—CMOS lock-in amplifier, FPGA, optical absorption spectroscopy, integrated optics, ratiometric measurement.**

I. Introduction

The ability to detect the presence of specific chemicals in liquid and gaseous mixtures and determine their composition is essential for many fields, such as environmental monitoring, medicine and biology. A well-known method to perform chemical analyses is optical absorption spectroscopy (OAS), typically carried out in the infrared wavelength range where many chemicals have distinctive absorption features [1]. The equipment to perform OAS usually relies on bulky and expensive free-space optics, but integrated photonics promises to perform the same analysis with significantly smaller and cheaper chips. These chips can be generally broken down into three main parts: the light source, the sensing element and the light detector. While research work to integrate light sources is still ongoing, photonic chips including both sensing elements and light detectors have been demonstrated [2].

A typical approach to perform OAS with integrated chips is to use uncladded waveguides as sensing elements [3]. The absence of an upper cladding allows the interaction between the evanescent field of the propagating light and the analytes present in the environment. If the wavelength matches one of the absorption peaks of the species of interest, light gets absorbed while traveling through the chip, with an attenuation that depends on the analyte concentration. By monitoring the optical power at the output with a photodetector, the presence of a target chemical can thus be detected in real-time.

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The compact size of the sensing system allows to integrate several waveguides on the same chip, to simultaneously detect multiple chemicals or monitor several absorption lines of a single analyte. This possibility translates into the need for a dedicated electronic readout instrument, capable of acquiring and processing multiple measurements. Similar systems exist for the visible and near-infrared spectral range [4], [5], but they lack for longer wavelengths. In this paper, we present a novel multichannel electronic system specifically designed for mid-infrared on-chip OAS measurements. The circuit comprises a CMOS front-end ASIC for the readout of 6 photodetectors in parallel and a mixed-signal motherboard, managed by an FPGA, for signal acquisition and processing. The system enables reliable spectroscopic measurements, as demonstrated in the final section with the detection of acetone samples.

II. Architecture of the sensing system

Fig. 1 shows the scheme of the photonic chip fabricated to perform OAS. Chalcogenide glass ($Ge_{23}Sb_7S_{70}$) was patterned on a silicon dioxide substrate to define the waveguides. This chalcogenide composition is transparent to wavelengths from $1\,\mu\mathrm{m}$ to $10\,\mu\mathrm{m}$ and is therefore suitable to perform OAS in the near- and mid-infrared range. To increase the sensitivity of the measurement, the waveguide was designed with a spiral shape, obtaining a long interaction length in a small chip area. In addition, a ratiometric structure was conceived to make the measurement insensitive to fluctuations of the optical power coupled to the chip, that cause variations of the output signal indistinguishable from those related to the analytes. Light is therefore split before the spiral and sent to a reference arm, not in contact with the chemical mixture, that provides a measurement of the input light. By computing the ratio of the reference and sensing measurements, all the common mode effects can be rejected. Three sensing structures were integrated on the same die for multichannel detection.

PbTe photoresistors of around $15\,\mathrm{k}\Omega$ were thermally evaporated at the waveguides end to measure the output optical power. The $0.2\,\mathrm{eV}$ energy gap of this material makes it well suited to detect radiations up to $4.3\,\mu\mathrm{m}$ [6]. Previous characterizations of the sensors demonstrated their good sensitivity in the mid-infrared range but also highlighted the presence of a bias-dependent 1/f noise [7]. The lock-in technique has

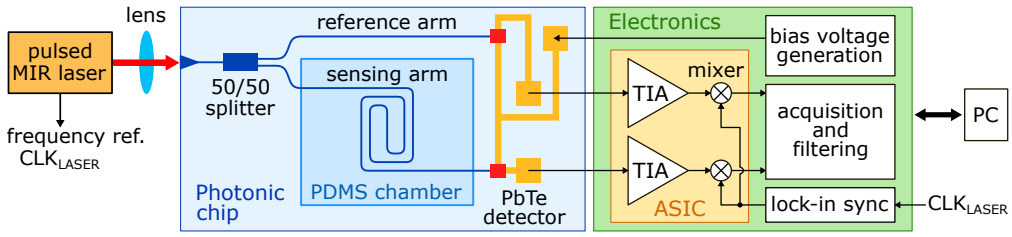

Fig. 1. Schematic view of the on-chip optical absorption spectroscopy sensing system: a laser is coupled to the photonic chip and the resulting signals at the chip output are measured with integrated PbTe photodetectors and acquired with a custom electronic instrument.

thus been chosen as readout scheme in order not to degrade the system performance, taking advantage of the shift in signal frequency that it requires. A pulsed laser with 150 kHz repetition rate was employed to directly generate a modulated signal at the chip input, without an external chopper.

The photonic chip is mounted on a compact holder, shaped to facilitate the coupling of light and the wire-bonding of the integrated detectors. The holder is connected to a custom electronic readout system. The preamplification and lock-in demodulation are performed with a CMOS ASIC, pivotal in enabling multichannel operations in a very compact form factor. The other electronic functionalities are instead managed by discrete-component electronics mounted on a motherboard. An FPGA, on a commercial module, handles the digital signal processing and the communication with a personal computer.

III. 6-Channel CMOS Front-End ASIC

Fig. 2 shows the schematic of the front-end ASIC, fabricated in TSMC 180 nm CMOS technology. A current-sensing architecture based on a transimpedance amplifier (TIA) has been chosen to simultaneously bias the PbTe detectors and read their signal. The light-induced current variations are in the order of few nA, modulated at 150 kHz and superimposed to a large DC bias of around 100 µA. In order not to limit the amplifier gain, an enhanced TIA has been designed [8]. An auxiliary DC handling loop has been added to steer the bias current away from the gain stage, allowing to correctly amplify the signal of interest without saturating the circuit.

The TIA has been designed with digitally selectable feedback resistor and capacitor (15 kΩ, 45 kΩ, 135 kΩ, 405 kΩ and 2.7 pF, 900 fF, 300 fF, 100 fF respectively), always ensuring a bandwidth of at least 4 MHz. A second amplifier, with a gain of 20, has been included at the TIA output to achieve a maximum overall amplification of 8 MΩ. The DC handling network has been made with a cascade of two integrators, that filter out the high-frequency oscillations of the TIA output and amplify its DC component, and a resistor R_{DC} that generates the reaction current to compensate the detector bias. The value of R_{DC} can be digitally selected (5 kΩ, 15 kΩ, 45 kΩ, 135 kΩ) to adapt to different bias conditions of the PbTe detectors, while the capacitor C_Z stabilizes the loop. Since the signal of interest is modulated at 150 kHz, the DC handling network has been designed with a maximum closed-loop bandwidth of around 1 kHz. The very large equivalent resistors needed to satisfy this requirement were obtained with two physical components of 1 MΩ and a cascade of two active current reducers, each with a reduction factor of around 100 [9].

Each TIA is followed by two on-chip demodulators, based on a square-wave double-balanced passive architecture, to perform the lock-in processing and extract the in-phase and quadrature components of the sensor impedance. An analog demodulation is here preferred to simplify the design of the acquisition chains of the motherboard, while not degrading the detection accuracy. The noise of the PbTe detectors ($30\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 150 kHz) is in fact the dominant term.

IV. Ratiometric Readout System

The ASIC is mounted on a printed circuit motherboard designed to: i) further amplify, filter and digitize the ASIC

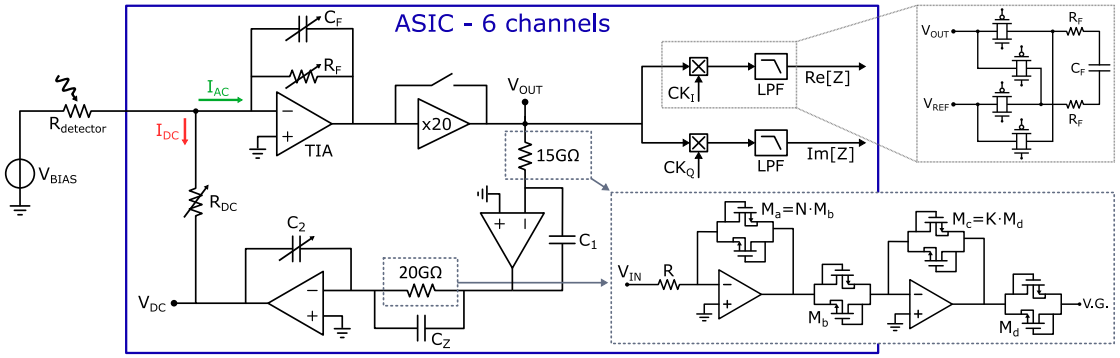

Fig. 2. Schematic of the proposed CMOS lock-in front-end. An active network removes the DC current from the virtual ground of the transimpedance amplifier, allowing larger amplification of the useful modulated signal. A square-wave mixer performs the lock-in demodulation at the chip output.

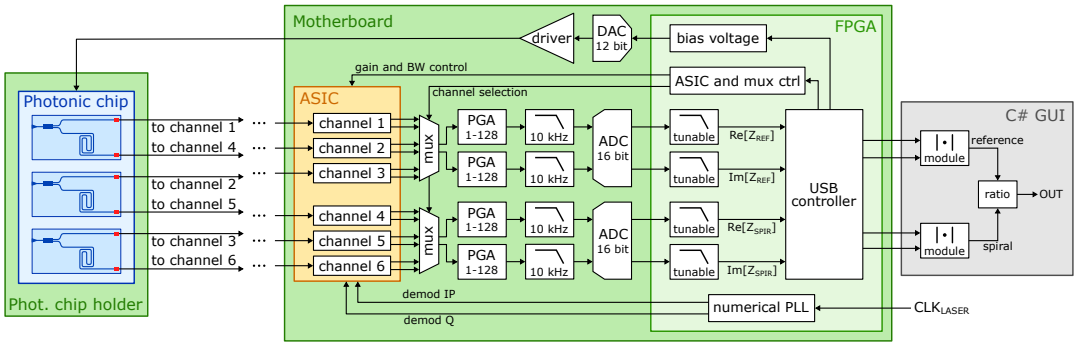

Fig. 3. Schematic view of the complete electronic system, showing the motherboard, the digital signal processing in the FPGA and the ratio operation.

output; ii) provide the voltage bias to the PbTe detectors; iii) generate the demodulation signals required for the lock-in processing; iv) communicate with a personal computer for visualization and storage of the measurement results. Fig. 3 shows the architecture of the board.

The outputs of the 6 ASIC channels are connected to two analog multiplexers, to select and read just one of the 3 sensors on the photonic chip at a time. Since the signals to be measured have a slow evolution with timescale of few seconds, the readout of the 3 structures can be time-multiplexed without penalties. Four acquisition chains are needed to acquire the real and imaginary parts of the spiral and reference detectors. The acquisition chains comprise a low-1/f noise programmable gain amplifier (PGA281, Texas Instruments), a third-order passive antialias filter with $10\,\mathrm{kHz}$ cut-off frequency and a 16-bit ADC (AD7903, Analog Devices), operated at $62.5\,\mathrm{kSps}$. The digitized signals are further low-pass filtered in the FPGA to define the lock-in readout bandwidth and then sent to a PC through a USB controller. A custom C# GUI computes the absolute value of the reference and spiral detectors impedance and then performs the ratio between the measurements. These operations were not performed in the FPGA because of the higher arithmetic precision of a 64-bit computer. The GUI also visualizes and stores the measurement results.

The voltage bias for the PbTe detectors is defined in the FPGA and then generated with a 12-bit DAC (AD5687R, Analog Devices) and buffered (AD8513, Analog Devices). The buffer allows to generate voltages between $\pm 5\,\mathrm{V}$, enough to bias the detectors in different operating conditions if needed.

The motherboard also generates the demodulation signals for the lock-in processing in the ASIC. The laser clock is acquired by the FPGA and fed to a fully-digital phase-locked loop (PLL). The PLL is based on a 12-bit time-to-digital converter and a numerical oscillator implemented by extracting the most significant bit of a free-running counter. By changing the counter increment, the oscillation frequency can be arbitrarily tuned. The use of a $200\,\mathrm{MHz}$ clock and a counter width of 32 bits translates into a frequency resolution of $0.05\,\mathrm{Hz}$. The PLL is used to generate a square wave at twice the laser clock frequency and its inverted version. By halving the frequency of these signals, the two in-phase and quadrature clocks needed for the lock-in demodulation are created.

V. Electrical Characterization

Fig. 4 shows the realized prototype, highlighting its size and building blocks. The system has an overall current consumption of $400\,\mathrm{mA}$ ($200\,\mathrm{mA}$ for the FPGA, $150\,\mathrm{mA}$ for the PCB and $50\,\mathrm{mA}$ for the ASIC) with a supply of $\pm 6.5\,\mathrm{V}$.

The transfer function of the TIA has been measured by applying a voltage signal to a $15\,\mathrm{k\Omega}$ resistor, connected to the virtual ground to simulate the presence of a PbTe detector. A DC current of $100\,\mu\mathrm{A}$ has been injected into the chip by biasing the resistor at $1.5\,\mathrm{V}$. The R_{DC} of the TIA has been set to $5\,\mathrm{k\Omega}$ to achieve the highest possible DC loop bandwidth and verify that, even in these conditions, the TIA can still process the signal of interest correctly. Fig. 5 shows the measurement result. The TIA gain has been varied between the maximum and minimum values, while adapting the value of C_F and C_2 accordingly. In all conditions, the circuit correctly amplifies the signals between $1\,\mathrm{kHz}$ and $1\,\mathrm{MHz}$, perfectly satisfying the requirement of the application. As expected, the DC current is always rejected, certifying the correct operation of the chip.

The digital PLL has also been tested, by connecting the laser reference signal at $150\,\mathrm{kHz}$ to the FPGA to generate the demodulation signals. Fig. 6 shows the obtained results. As expected, the PLL output square wave at twice the laser repetition rate is perfectly synchronized to the input clock. The demodulation square waves, aligned with the rising and falling edge of the PLL output, are in a precise phase quadrature relation and they can thus be used for the lock-in processing.

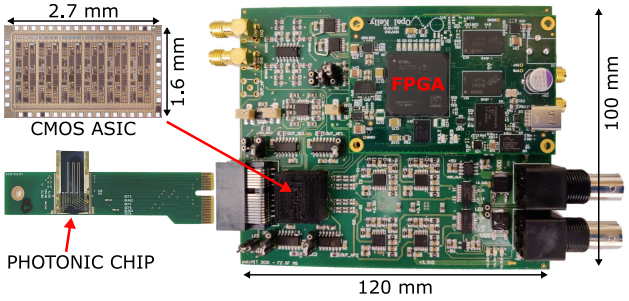

Fig. 4. Photograph of the complete instrument, composed of the photonic chip holder plugged into the main motherboard that contains the CMOS ASIC, the readout electronics and the FPGA.

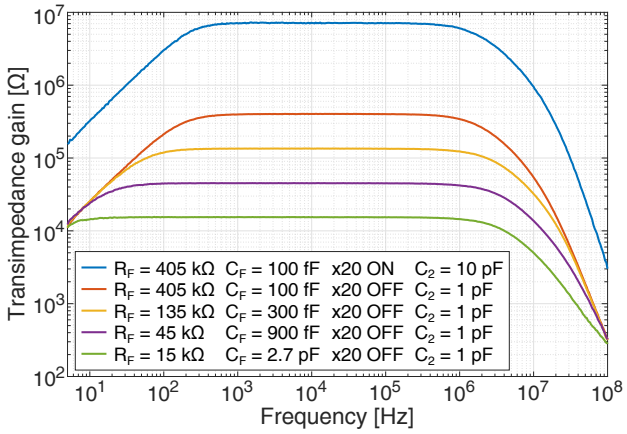

Fig. 5. Transfer function of the integrated TIA, measured for different gain settings. The DC current is correctly rejected, while large amplification is maintained on a frequency range between 1 kHz and 1 MHz.

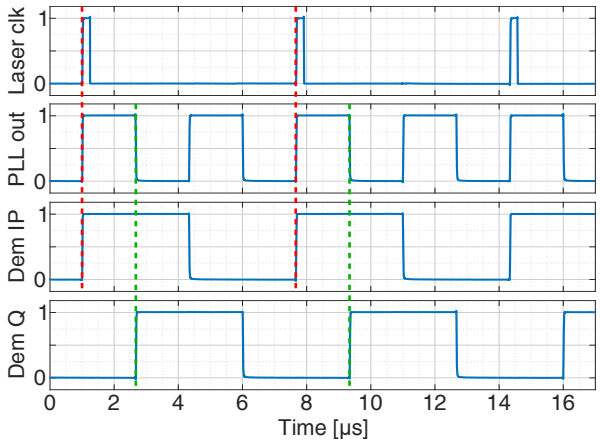

Fig. 6. Measured normalized lock-in demodulation signals, correctly generated by the numerical PLL starting from the laser clock reference.

VI. Detection of an Acetone Sample

The electronic system has been validated in a real ratiometric spectroscopic measurement. Acetone has been chosen as the target analyte, because droplets of this chemical can be easily released on the sensing spiral. The laser wavelength has been set to 3.3 µm, where acetone has an absorption peak. The input power coupled to the chip was about 1 mW. The electronic platform has been used to simultaneously monitor the signals of the sensing and of the reference detectors on the photonic chip, with a lock-in bandwidth of 1 Hz.

Fig. 7 shows the magnitude of the modulated detectors currents during the experiment. Before the arrival of the acetone sample, the laser alignment has been voluntarily disturbed to cause small variations of the optical power coupled to the chip. These variations are correctly measured by both arms of the photonic chip, as highlighted by the similar evolution of the reference and spiral currents. The computation of the ratio between the two signals, shown in the figure, is therefore effective in canceling out these oscillations, demonstrating the validity of the ratiometric approach. After 26 seconds,

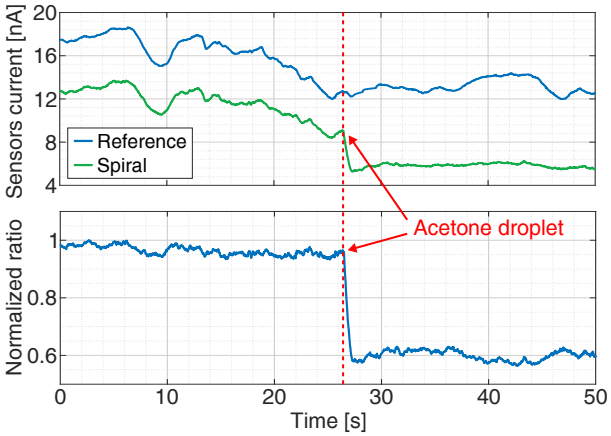

Fig. 7. Detection of an acetone sample, performed at 3.3 µm wavelength: after 26 s a droplet is released on the sensor and correctly detected. The ratiometric measurement successfully cancels out the effect of input power fluctuations.

an acetone droplet has been released on the spiral arm. The presence of the analyte attenuates the light reaching the corresponding photodetector, while the reference signal correctly stays constant. The computation of the ratio thus clearly reveals the moment of the acetone release.

The measurement certifies the correct design and operation of the whole detection system. The electronics, being independent of laser wavelength, optical chip technology and detector material, can also adapt to other environmental monitoring applications, not necessarily limited to the near-infrared region.

References

[1] A. Vasiliev, M. Muneeb, J. Allaert, J. Van Campenhout, R. Baets, and G. Roelkens, "Integrated silicon-on-insulator spectrometer with single pixel readout for mid-infrared spectroscopy," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 6, pp. 1–7, 2018.

[2] L. Tombez, E. J. Zhang, J. S. Orcutt, S. Kamlapurkar, and W. M. J. Green, "Methane absorption spectroscopy on a silicon photonic chip," *Optica*, vol. 4, no. 11, pp. 1322–1325, 2017.

[3] P. Su, Z. Han, D. Kita, P. Becla, H. Lin, S. Deckoff-Jones, K. Richardson, L. C. Kimerling, J. Hu, and A. Agarwal, "Monolithic on-chip mid-IR methane gas sensor with waveguide-integrated detector," *Applied Physics Letters*, vol. 114, no. 5, p. 051103, 2019.

[4] L. Hong and K. Sengupta, "Fully integrated optical spectrometer in visible and near-IR in CMOS," *IEEE transactions on biomedical circuits and systems*, vol. 11, no. 6, pp. 1176–1191, 2017.

[5] J. H. Correia, G. De Graaf, M. Bartek, and R. F. Wolffenbuttel, "A CMOS optical microspectrometer with light-to-frequency converter, bus interface, and stray-light compensation," *IEEE Transactions on Instrumentation and Measurement*, vol. 50, no. 6, pp. 1530–1537, 2001.

[6] A. Bafekry, C. Stampfl, and F. M. Peeters, "The electronic, optical, and thermoelectric properties of monolayer PbTe and the tunability of the electronic structure by external fields and defects," *Physica Status Solidi (b)*, vol. 257, no. 6, p. 2000182, 2020.

[7] E. Guglielmi, P. Su, F. Zanetto, K. Stoll, S. Serna, G. Ferrari, M. Sampietro, K. Wada, L. C. Kimerling, and A. Agarwal, "1/f noise characteristics of waveguide-integrated PbTe MIR detectors and impact on limit of detection," *Journal of Lightwave Technology*, vol. 39, no. 22, pp. 7326–7333, 2021.

[8] F. Zanetto, E. Guglielmi, F. Toso, R. Gaudiano, F. Caruso, M. Sampietro, and G. Ferrari, "Wide dynamic range multichannel lock-in amplifier for contactless optical sensors with sub-pS resolution," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 246–249, 2020.

[9] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance amplifier for high sensitivity current measurements on nanodevices," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1609–1616, 2009.