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NON-LINEAR SHUNT REGULATOR BASED ON A PWM RF POWER DETECTOR FOR RFID APPLICATIONS

Thesis presented in partial fulfillment
of the requirements for the degree of
Master of Microeletronics

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“I would love to change the world.”
— Alvin Lee, 31 August, 1971

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ABSTRACT

Radio Frequency Identification (RFID) is utilized in a variety of applications, including tagging animals and objects to make their identification (ID) easier to read and manage, similar to a bar code or QR code. In this regard, the goal of this research is to improve RFID transponder power regulation in order to increase reader distance. This thesis describes a non-linear shunt regulator that employs a Radio Frequency (RF) power detector based on the Pulse Width Modulation (PWM) technique to aim magnetically coupled RFID transponders. A quick voltage-clamp loop and a slow-accurate power detector loop are used in the proposed regulator architecture. The first loop ensures over-voltage protection, while the second loop gradually corrects the first loop's imprecision based on the measured input power.

To contextualize the issues and improvements of the new design, the state-of-the-art in RFID power management and RF power detector are covered first. The new architecture is specified after theoretical development, electrical simulations, and the design of the new architecture is implemented. The entire regulator design was prototyped as part of a commercial low-frequency (134 kHz) RFID transponder in a 180 nm CMOS process.

The regulator deal with a sinusoidal voltage at its input generated by the LC tank that extracts energy from the reader to supply its circuitry. The use of a 3.3V standard process for the analog circuitry in order to decrease the fabrication cost by not using the high voltage module (5 V for example) complicates the system design. Even though the proposed solution aims to regulate the input voltage precisely at 3.6 V maximum, the maximum voltage supported by 3.3 V standard module using two feedback is achieved.

The total RFID transponder area of 870x870 μm² was obtained, with 130x230 μm² related to the regulator circuit area only. Both resonant and supply capacitors are implemented on the chip. The complete system consumes a maximum current of 4.5 μA, over a wide RF input power range that is modulated by the distance between the reader and the transponder. As the power detector corrects the imprecision of the shunt regulator composed by simple diodes due to its process, voltage and temperature (PVT), the transponder performance was measured with and without the shunt regulator enabled. Results show an improvement of 16.7 % in the communication distance between the transponder and the reader.

Keywords: Shunt Regulator, RF Power Detector, PWM Power Detector, RFID.

RESUMO

Identificação por Rádio Frequência (RFID) é usada em muitas aplicações, colocando etiquetas eletrônicas em animais e objetos para facilitar a leitura a fim de melhorar o gerenciamento destes. Nesse contexto, essa dissertação tem como objetivo melhorar a regulação de potência em chips de RFID a fim de aumentar a distância de leitura. Essa dissertação apresenta um nova arquitetura de regulador paralelo, não linear, que usa um detector de potência de Rádio Frequência (RF) baseado em uma técnica de modulação de pulso (PWM) para aplicação de RFID que usam o princípio de comunicação por acoplamento magnético. A arquitetura de regulador proposto é composta de duas realimentações: uma realimentação usa um limitador de tensão rápido e a outra usa um detector de potência lento porém preciso. O primeiro garante a proteção contra sobre tensão e o segundo corrige a imprecisão do primeiro de acordo com a potência do sinal de entrada.

Primeiramente, o estado da arte em regulação de sitemas de RFID bem como em detectores de potência RF são feitos para contextualizar os problemas e melhorias da nova arquitetura. Um desenvolvimento teórico seguido por simulações elétricas e o projeto do circuito da nova arquitetura de regulador paralelo são abordadas em detalhes. A circuito foi implementado em um processo CMOS de 180 *n*m como parte de um Chip de RFID de baixa frequência (134 kHz). O regulador lida com uma tensão senoidal (134 kHz) na sua entrada, gerada por um tanque LC que extrai energia provinda do leitor e que é usada alimentar todo o chip. Devido ao uso de um processo padrão 3.3 V CMOS para implementação do circuitos analógicos a fim de diminuir o custo de fabricação com o não uso do modulo de alta tensão (Ex. 5 V), impondo dificuldades no projeto do sistema, mesmo assim a solução proposta regula a tensão de entrada do chip em 3.6 V, máxima suportada pela tecnologia, com o uso das duas malhas de realimentação.

A área total do Chip de RFID é de 870x870 μm², com 130x230 μm² para apenas o circuito de regulação. Os capacitores de ressonância e de alimentação foram integrados no Chip. O sistema completo consome 4.5 μA, sobre uma ampla gama de potência de entrada que é modulada pela distância entre o leitor e a tag. Como o detector de potência corrige a imprecisão do limitador de tensão composto de diodos devido a variação em processo, tensão e temperatura (PVT), a distância de leitura foi medida com e sem o detector de potência habilitado. Os resultados mostraram uma melhoria de 16.7 % na distância de comunicação.

Palavras-chave: Regulador paralelo, Detector de potência RF, Detector de potência PWM, RFID.

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LIST OF ABBREVIATIONS AND ACRONYMS

RFID	Radio Frequency Identification
ID	Identification
RF	Radio Frequency
PWM	Pulse Width Modulation
CMOS	Complementary metal-oxide-semiconductor
PVT	Process-Voltage-Temperature
IoT	Internet of Things
MIT	Massachusetts Institute of Technology
WAN	Wide Area Network
WSN	Wireless Sensor Network
LoRa	Long Range
NBIoT	Narrow Band IoT
AI	Artificial Intelligence
LF	Low Frequency (30 - 300 kHz)
HF	High Frequency (3 - 30 MHz)
UHF	Ultra High Frequency (300 MHz - 3 MHz)
VT	Voltage Threshold
DC	Direct Current
AC	Alternate Current
dB	Decibel
dBm	decibel-milliwatts
AFE	Analog Front-End
PMU	Power Managment Unit
ASK	Amplitude Shift keying
ESD	Electrostatic Discharge
RSSI	Received Signal Strength Indicator

SNR	Signal to Noise Ratio
ADC	Analog to Digital Converter
RMS	Root-Mean-Square
VGA	Variable Gain Amplifier
NMOS	N-channel MOS
PMOS	P-channel MOS
DBP	Differential Bi-Phase
OTA	Operational Transconductance Amplifier
GBW	Gain-bandwidth Product
PN	p-type and n-type
KHz	KiloHertz
MHz	MegaHertz
GHz	GigaHertz
IEEE	Institute of Electrical and Electronics Engineers

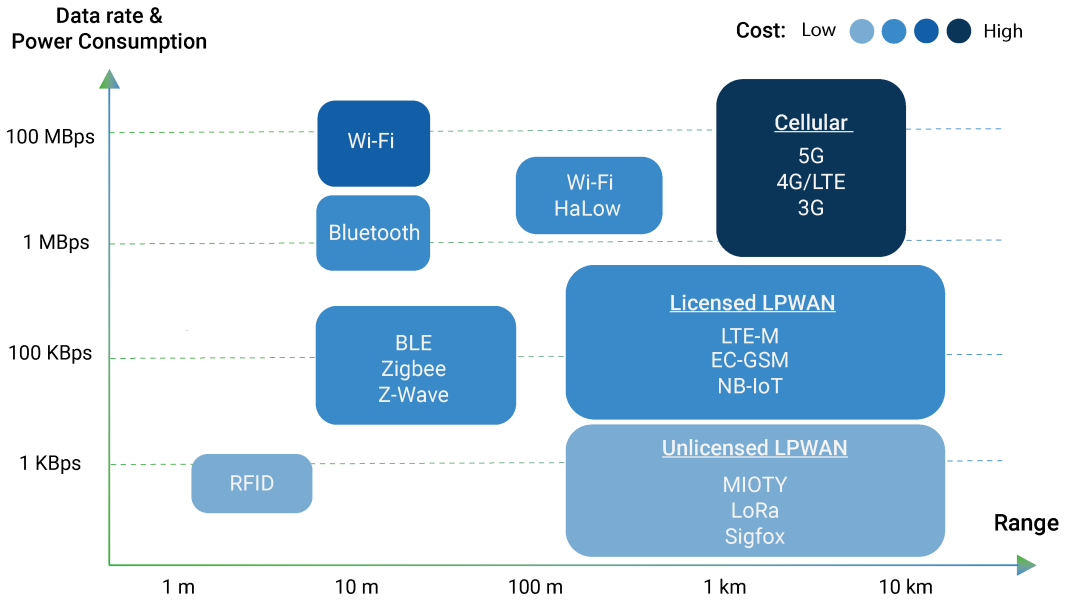
CONTENTS

1 INTRODUCTION

1.1 IoT Technologies

Wireless communication is being used on a variety of devices and gadgets. The growing need for linked devices and the interchange of data among them over the network is a big research field, where the potential to develop smart things abound. The name "Internet of Things" (IoT) was used to describe this phenomenon. Kevin Ashton coined the term IoT in 1999, and it was first used at the Massachusetts Institute of Technology (MIT), when the word was described in terms of a vision in which all of our personal and working devices, including inanimate objects, have not only a digital identity but also the potential to process data, allowing a central computer system to organize and manage it (ZHANG et al., 2020).

Figure 1.1: IoT technologies by the Range versus Power Consumption.



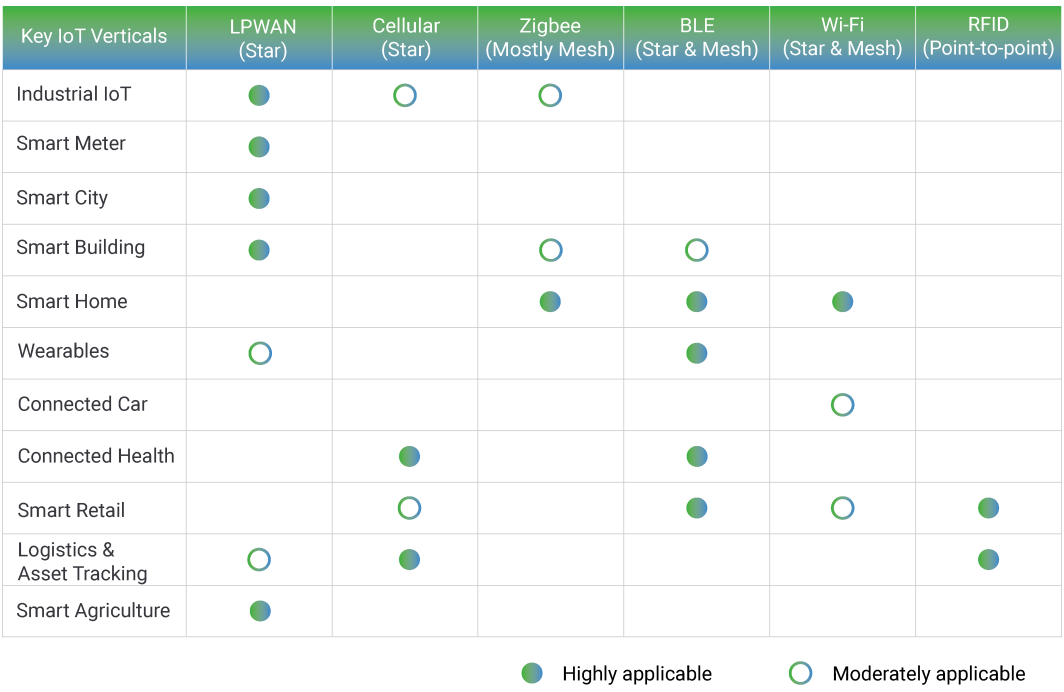
Source: (NOBEHRTECH, 2020).

In the year 2000, a researcher from the RFID Development Committee proposed the concept of the IoT. He suggested that looking for a specific Internet address in a database's contents could provide information about a tagged object (NGAI et al., 2008). Since then, the IoT has been associated with ordinary things that can be detected, identified, addressed, and controlled through the use of radio frequency identification (RFID), wireless networks, wide area networks (WAN), and other tools. Objects include not only elec-

trical equipment, but also non-electrical items including food, clothing, materials, and parts (ALANSARI et al., 2018). This viewpoint promotes the development of wireless technologies for a variety of remote applications, ranging from short ranges like RFID and Bluetooth to long ranges like SigFox, LoRa, and NBIoT. The IoT technologies are summarized in Figure 1.1 by their application range and power consumption.

Each wireless technology enables applications based on its communication range and data communication. Examples of applications could be seen from payments by proximity to industrial applications, smart cities, connected cars, and also smart agriculture. The marketing trends and IoT technology usage is outlined in Figure 1.2.

Figure 1.2: Applications for different IoT technologies

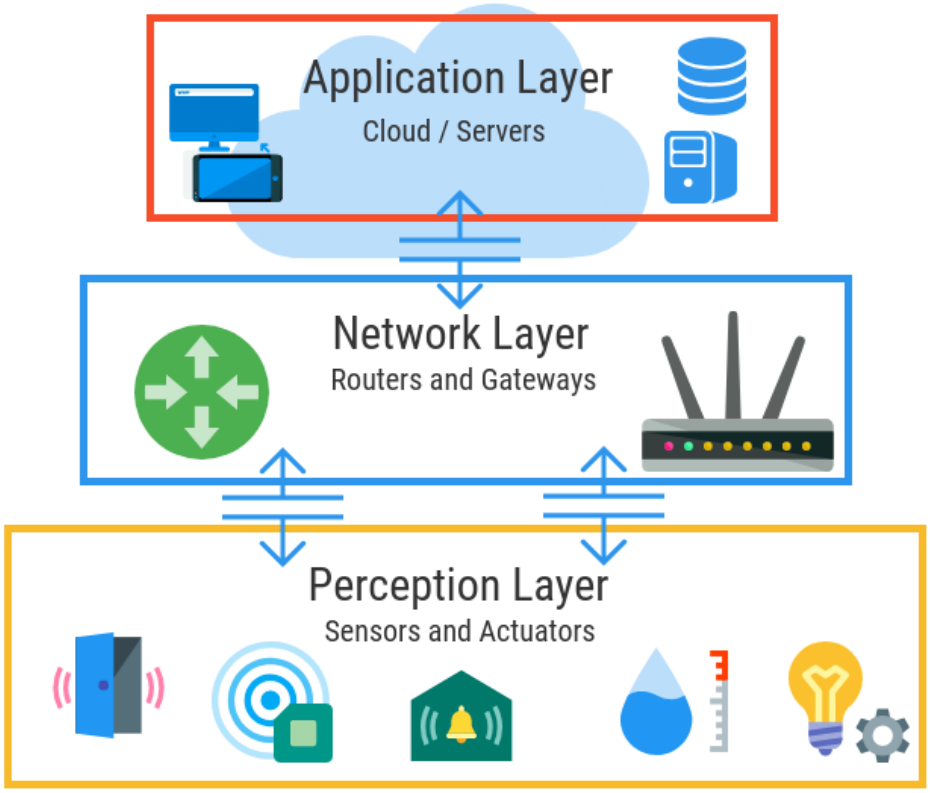


Source: (NOBEHRTECH, 2020).

The IoT ecosystem addresses a variety of issues, including data collecting and processing, solution scalability, security, modularization, open standards, interoperability, and device administration. The concerns are addressed in one of the three functional blocks that make up its design, as indicated in 1.3.

- **Perception Layer**: This layer includes the hardware that collects data and controls the application (sensors and actuators), as well as the hardware that connects the object to the network so that it may be used in a specific application.
- **Network Layer**: This is the intermediary layer that acts as a messenger and translator between the cloud and smart device clusters. They're either physical gadgets or software programs that run from the field near sensors and other equipment. They can perform a variety of tasks, but the most significant are data normalization, connection, and transfer between the physical device layer and the cloud.
- **Application Layer**: It communicates with the gateway using a wired or cellular internet connection. The Cloud could be anything from Amazon Web Services (AWS) to Google Cloud. It offers strong servers and databases that enable IoT applications to run smoothly and combine services like data storage, big data processing, filtering, analytics, business logic, alarms, monitoring, and user interfaces.

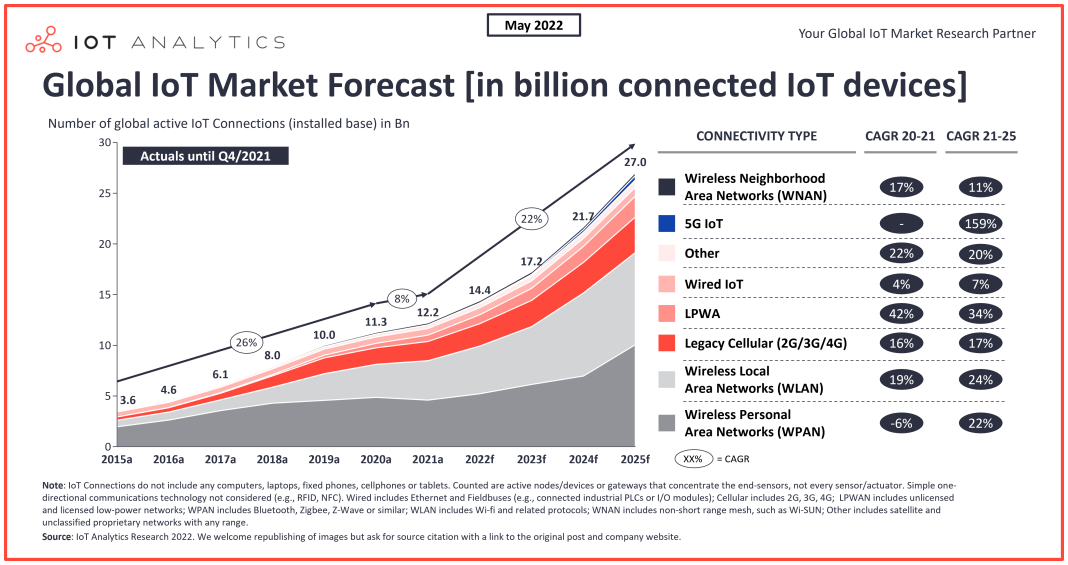
Figure 1.3: IoT Architecture



Source: (CALIHMAN, 2021).

The IoT ecosystem is still in development, from hardware to software and infrastructure to allow this revolution on data communication. The big trends in IoT ecosystem today are Big Data, Cloud Computing, Analytics, Artificial Intelligence (AI) and Security, to enable decisions based on the data collected by the IoT technology in a secure way. Figure 1.4 shows the IoT market forecast made by IoT analytics in 2022 (HASAN, 2022). The number of connected devices was almost 15 Billion in 2021 and its forecast is expected to double in 2025. The connected devices do not consider any computer, cell phone, laptop, and tablet, because those could be also considered IoT devices. Neither one-directional communication technology like RFID. This technology is already spread on the market and many of the applications work standalone, not connected to the Internet. RFID needs a reader connected to the internet to put all RFID data on the network.

Figure 1.4: IoT Market Forecast



Source: (HASAN, 2022).

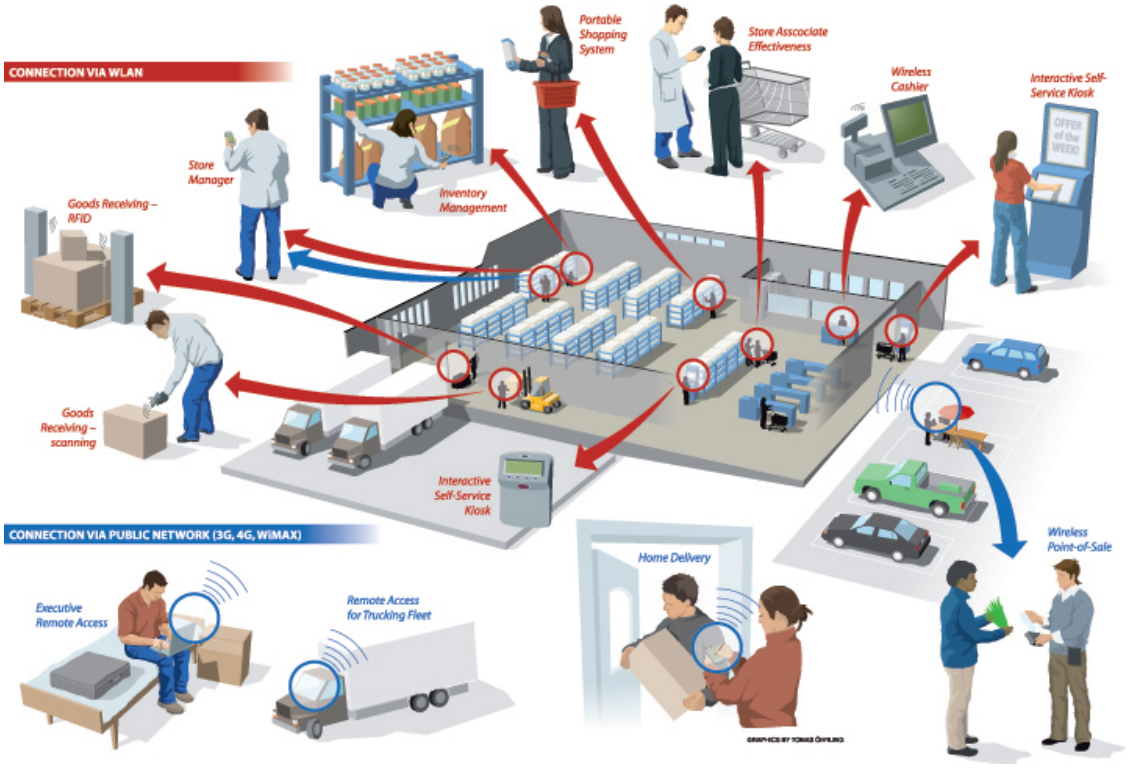
1.2 RFID Technology

As demonstrated in Figure 1.1, RFID is thoroughly investigated and thus employed in the context of IoT technology to link things to the Internet in a narrow range while exchanging a modest amount of data. RFID uses radio waves to identify things, record metadata, and control particular targets. First debuted in 1945, Léon Theremin invented the "Thing", a listening device for the Soviet Union which retransmitted incident radio waves with the added audio information. Sound waves vibrated a diaphragm which slightly altered the shape of the resonator, which modulated the reflected radio frequency (HATCH; KURTZ; SHAH, 2001). RFID is one of the most significant information technology opportunities that will profoundly alter the globe. When the RFID readers abided by appropriate communication protocols are connected to the Internet, the readers distributed across the globe can identify, track and monitor the objects attached with tags globally, automatically, and in real-time (JIA et al., 2012).

RFID is widely used in a variety of applications, such as supply chain management, access control, department stores, luggage tracing, and tracking (CORTES et al., 2014). Figure 1.5 illustrates how RFID technology can be used in supply chain management. Low-Frequency (LF) band, High-Frequency (HF) band, and Ultra-High Frequency (UHF) band are the three main categories. Based on the communication distance and other criteria provided in Table 1.1, the application defines a specific frequency band. Short-range communication enables the LF to be used for animal tracking and security keys, while the HF is used for payment and access control. UHF is commonly used in supply chain management because it allows the reading of numerous tags in less than one second across a 15-meter range (FINKENZELLER, 2003).

Figure 1.6 presents an RFID market forecast made by IDTechEx in 2020. Despite a 5% decline in the global RFID market in 2020 compared to 2019, due to COVID-19's influence, the market rebounded well in 2021. The global RFID market was expected to be worth $11.6 billion in 2021, and it has been raised to $12.2 billion in 2022, according to IDTechEx. The forecast comprises RFID tags, cards, readers, software, and services for both passive and active RFID.

Figure 1.5: RFID Applications



Source: (COLUMBITECH, 2020).

Table 1.1: RFID Technologies

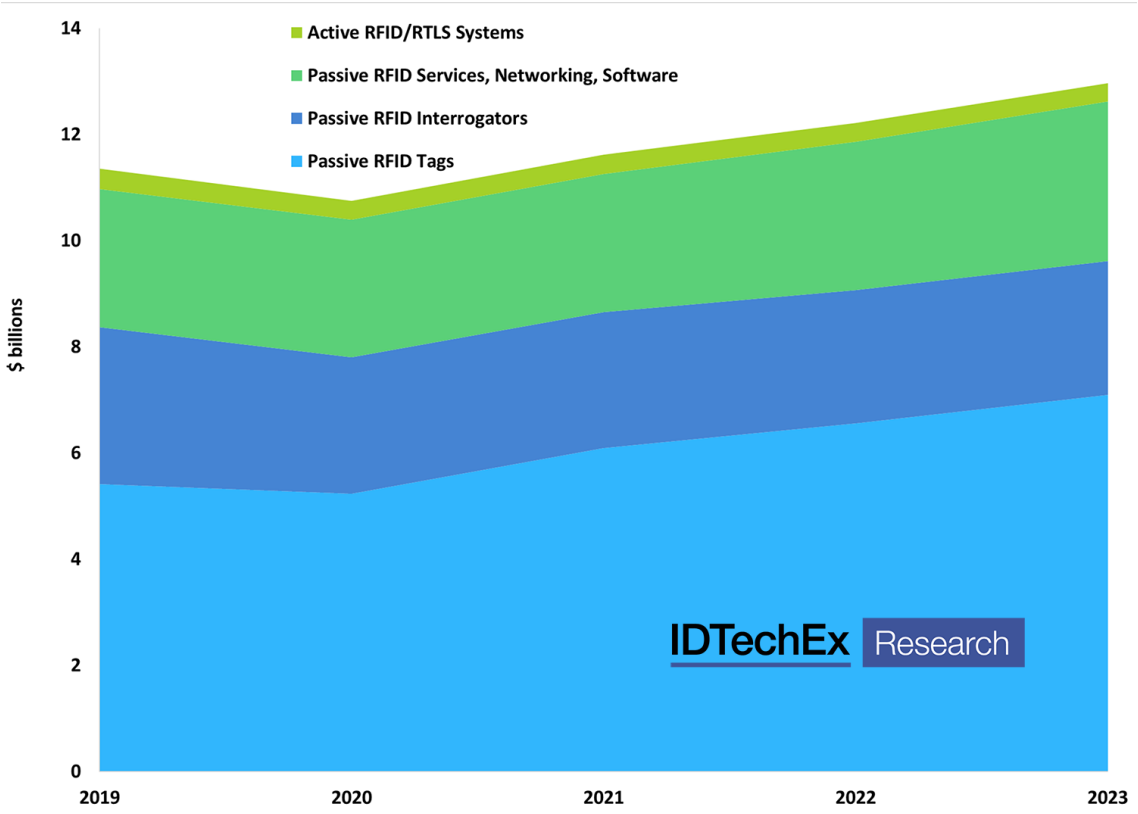
	LF	**HF**	**UHF**
Frequency	125 - 134 K Hz	13.56 M Hz	850 - 960 M Hz
Range	35 cm	1 m	15 m
Data Rate	less than 1 Kbit/s	25 Kbit/s	110 kbits/s
Read Multiple Tags	Poor	Good	Excellent
Penetration of Materials	Excellent	Good	Poor

1.2.1 Power in RFID

The power to supply the RFID system can be provided by two different input sources. The most used is the energy harvesting from the RF signal sent by the reader and the second source of supply an RFID system is a battery. The RFID is classified in passive, semi-passive, and active depending on the supply source. Active tags have the battery as the primary source of energy, semi-passive tags embed the battery to assist in providing power and passive tags do not have a battery and rely only on the reader signal for power supply.

The energy collected by passive RFID is used to provide itself with the RF signal sent by the reader. It is the most popular since it does not require a charge and it could be attached to a variety of objects owing to its tiny size. The battery is used to power the circuit in semi-passive RFID, but it does not help with communication. The RFID is said to be active when the battery also helps with communication. These forms of RFID are

Figure 1.6: RFID Market Forecast



Source: (IDTECHEX, 2020).

employed in specific applications where their cost is justified, such as data loggers that can monitor and work for a long length of time, and communication ranges that can be increased, allowing applications such as Wireless Sensor Networks to be implemented (WSN).

Inductive coupling systems are used in LF and HF RFID. The RF energy is collected and stored in the LC tank used as an antenna. The energy is then changed from an Alternate Current (AC) to a Direct Current (DC) and used to power the circuit. A functional component on RFID called Rectifier converts the energy from the RF signal to DC. When the RF signal is large, the Rectifier can be built using diodes in well-known half-wave and full-wave topologies (from 2 to 6V in HF and LF RFID). The Schottky diode may be utilized or a MOS transistor using a Voltage Threshold (VT) cancellation approach to improve the conversion efficiency of the Rectifer (CANTALICE et al., 2018).

However, UHF RFID collects the RF signal by the planar wave using an antenna tuned in the work frequency. In this scenario, the RF signal is weak (from 100 mV to 1V in UHF RFID) and the Charge Pump architecture is preferable in order to achieve high energy conversion efficiency (VALENTA; DURGIN, 2014).

1.2.2 Communication in RFID

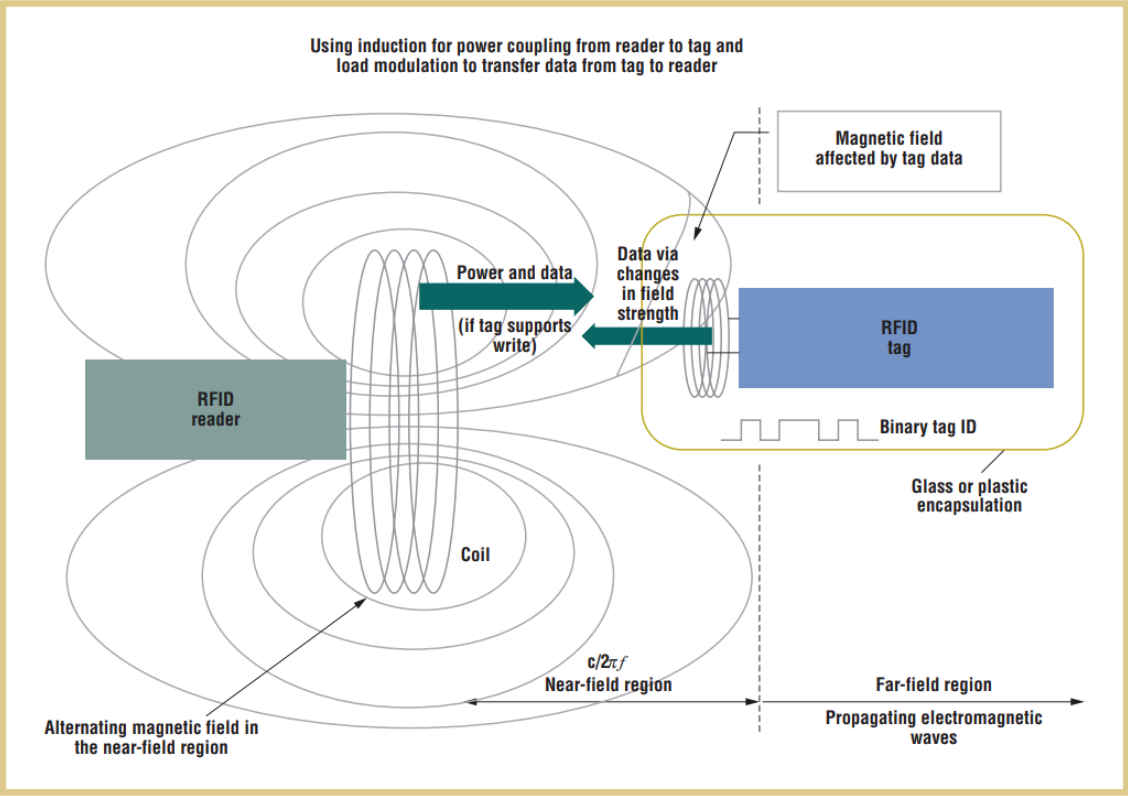
The communication principles between the RFID technologies are different. Magnetic coupling allows the LF and HF bands to exchange data and power. The data is modulated by varying the amount of power provided by the reader to the transponder. The mechanism of communication in the reverse link, from the transponder to the reader,

is to exchange the load linked to the transponder's LC tank, altering the tank's quality factor (Q) that is perceived by the transponder, which is known as the load modulation principle. The quality factor is defined as the ratio of the energy saved to the energy wasted during each cycle in the transponder, or in terms of the electrical parameters, as in Equation 1.1, where R is the load (FINKENZELLER, 2003).

$$Q = R\sqrt{\frac{C}{L}} \tag{1.1}$$

Figure 1.7 explains graphically the communication in LF and HF RFID technology. The near-field region defines the magnetic coupling boundary.

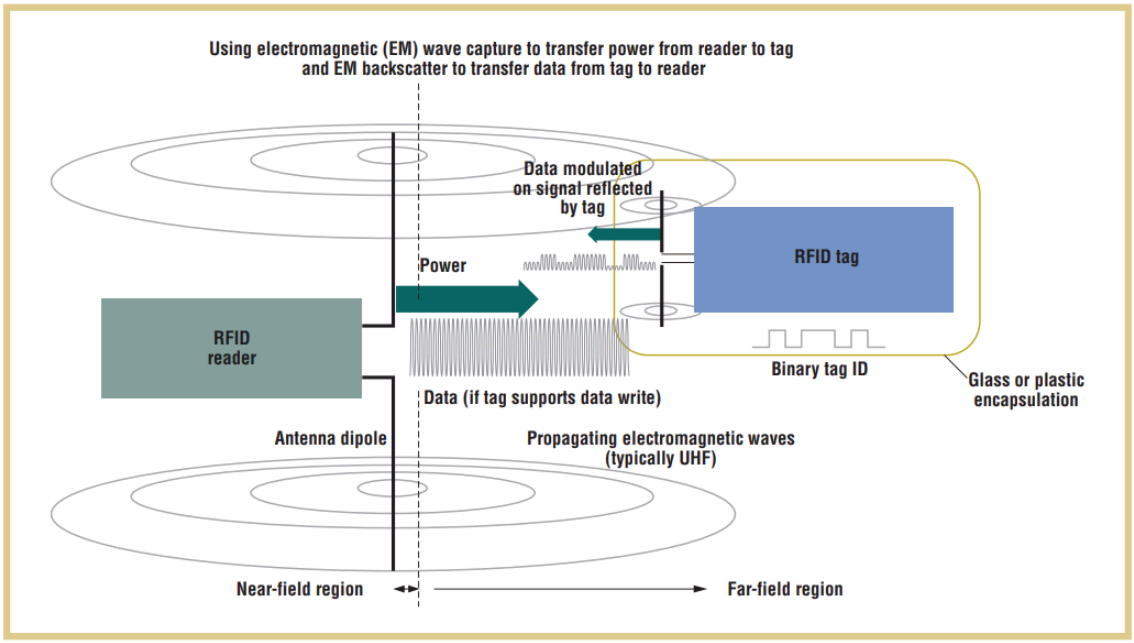
Figure 1.7: LF and HF RFID communication principles



Source: (WANT, 2006).

In the UHF RFID communication, the reader sends data to the transponder modulating the amount of power. In the reverse link, the communication is established by reflecting the power of the planar electromagnetic wave incident over the transponder, this is the backscattering principle explained in a graphic way in Figure 1.8. The power reflected by the transponder is weak, however, the reader sensitivity is high (-70 dBm), enabling read distances in the order of 15 m for a passive UHF RFID. The far-field region defines the UHF work region, the read distance mainly depends on the matching network between the transponder and the antenna, the transponder power consumption, and the reader sensitivity.

Figure 1.8: UHF RFID communication principle

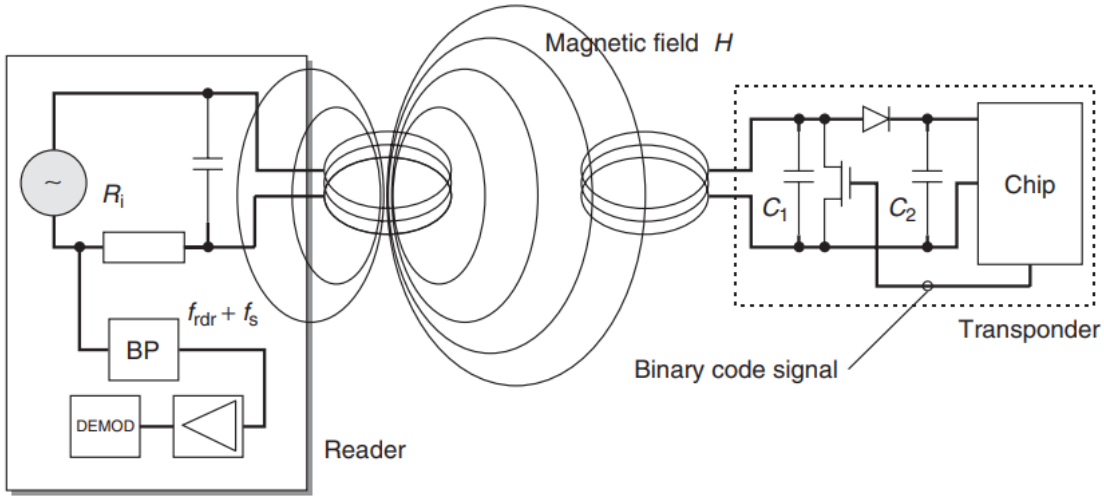


Source: (WANT, 2006).

1.3 Inductive Coupling Passive RFID

Figure 1.9 illustrates a simplified block diagram of the essential components of the inductive coupling systems' communication and power transmission. The magnetic field is created by the reader and is connected to the transponder's inductance. The tuning capacitor C_1 composes the transponder's tank. The MOS switch is the modulator block that alters the transponder's load during communication, while the diode symbolizes the rectifier and the C_2 supply capacitor. In this diagram, the chip represents the whole analog and digital circuitry, including voltage and current references, voltage regulators and protection, signal processing, digital finite state machines, and memory.

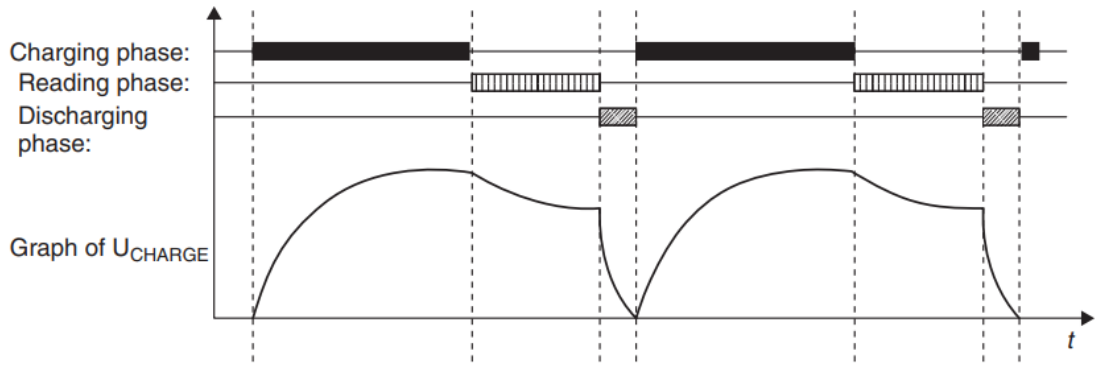
Figure 1.9: RFID inductive coupling block diagram



Source: (FINKENZELLER, 2003).

The communication phases are demonstrated in Figure 1.10, together with the voltage created on the supply capacitor during each phase. During the charge phase, the transponder gets a continuous wave from the rectifier, which charges the supply capacitor (U_{CHARGE}) with energy stored in the transponder's tank. The transponder and reader exchange data during communication, and the transponder gets less energy during this period. The energy accumulated in the preceding phase is supplied to the entire circuitry via the supply capacitor. If the transponder runs out of power during that time, the supply voltage drops until the system is reset to its lowest operational voltage. This procedure reduces the transponder's reading range. It's possible that the discharge phase will kick off a new cycle.

Figure 1.10: RFID inductive coupling power-up sequence



Source: (FINKENZELLER, 2003).

Depending on the reader distance, inductive systems cope with a wide dynamic range of power levels at their input. When the transponder is far away from the reader, the magnetic coupling and energy transfer between the reader and the transponder are poor, resulting in a low voltage signal at the LC tank. The coupling factor is high, the energy transfer is high, and the voltage is likewise high when the reader is close to the transponder. When this occurs, the voltage must be adjusted in order to avoid damage to the internal circuitry. Intending to ensure protection at high power levels, the transponder regulation architecture must manage the RF power entering. On the other hand, it must not run at low power levels, i.e., it must not have the required energy. High-performance transponders must have a better control strategy for transponder design and lower power consumption.

1.4 Motivation

The main idea of this Master's thesis is to improve the efficiency of LF RFID transponders. A more precise voltage management mechanism is employed to improve the energy transmission between the transponder and the reader and hence enhance the reader distance.

1.5 Contribution

In such RFID applications, this thesis provides a non-linear RF shunt regulator with an RF power detector in a feedback loop for managing the incoming RF power. The regu-

lator is composed of a two-feedback loop system that includes an RF power detector and overvoltage protection (voltage clamp or RF clamp). One is provided by the overvoltage protection, which is not precise but fast enough to provide protection against large RF field variations. The other feedback loop is accurate due to the inclusion of the RF power detector block through a more precise voltage reference, which allows for careful adjustment of the RF clamp in low-power settings to maximize energy storage on the LC tank while also boosting transponder sensitivity.

In transceivers, RF detectors are used to measure the amount of incoming RF power. This data may be utilized for various purposes, including reducing system power consumption, adjusting signal route gain, improving circuit characteristics, enhancing efficiency, and so on (COWLES, 2011). The conventional way of determining RF power is to measure the peak voltage of the RF signal. A novel method of measuring incoming power is devised in this study. The power detector block calculates the available RF input power by analyzing the RF voltage peak's rise and fall time. This information is then converted into a PWM signal that is filtered to have an analog voltage proportionate to the RF input voltage. This approach is highly useful for monitoring RF power in systems with high voltage levels, but it must be limited to safeguarding the internal electronics in LF and HF RFID transponders.

Finally, the circuit implementation to improve the efficiency of the regulation system using only 3.3 V CMOS standard transistor, instead of using a higher voltage module (5.5 V), in order to reduce the fabrication cost of the final solution.

1.6 Thesis Organization

The following chapters are how this thesis is structured: The second chapter discusses the state-of-the-art in power regulation in inductive coupling passive RFID, as well as the state-of-the-art in RF power detectors. The third chapter discusses the non-linear shunt regulator solution in-depth, including theoretical analysis, modeling, and design. The fourth chapter contains simulations and measurement findings. Finally, in Chapter 5, the conclusions and future works are presented.

2 RFID POWER DETECTION AND REGULATION

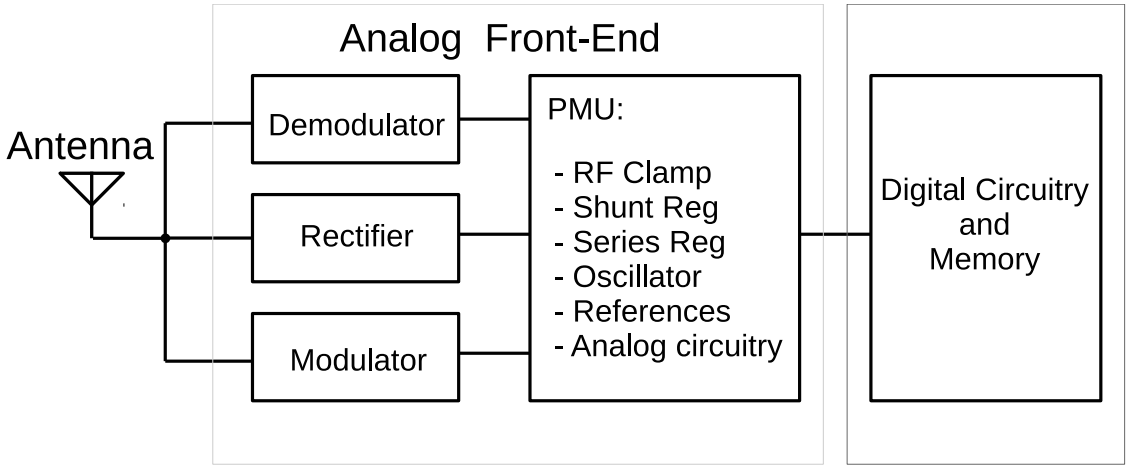
Depending on the distance between the transmitter and the receiver, RF systems deal with varying power levels. RFID systems deal with the same paradigm. However, the power levels are high, owing to the system's closeness and the harvesting nature to supply the transponder. This chapter aims to address the state-of-the-art of inductively linked passive RFID, as well as the RF power detector, to provide a solid understanding of the RFID power regulation system and its trade-offs, and to better introduce the suggested solution presented in this thesis.

2.1 Power Regulation State-of-Art in Inductive Coupling Passive RFID

A passive RFID transponder is primarily a low-power device due to the energy gathering component of its operation. RFID input sensitivity is affected by a number of factors, including the device's maximum distance, the efficiency of RF-to-DC conversion, and the power consumption of its internal circuits.

Figure 2.1 presents the usual building blocks of a typical RFID system.

Figure 2.1: RFID architecture



The Analog Front-End (AFE) is composed of an RF section including a demodulator, modulator, and rectifier blocks, as well as a Power Management Unity (PMU). The rectifier is in charge of converting RF to DC, whereas the demodulator and modulator are communication blocks. The PMU is made up of voltage and current references, an oscillator, regulators, and other analog circuitry necessary to supply and stimulate the

digital circuits in order for them to perform their functions, such as supply capacitors and voltage detectors. When the reader is near the transponder, RFID systems should run at full power. As a result, over-voltage prevention is essential to prevent internal circuit damage; in this case, the protection limits the antenna voltage to a safe level. Different PMU topologies are designed to ensure chip operation depending on the Complementary Metal-Oxide-Semiconductor (CMOS) manufacturing technology utilized in the circuit. The leading-edge shunt regulators for RFID applications were presented in (BROOKS, 1991) and (GAY, 2004). The input voltage is controlled by the shunt regulator, while the output voltage is controlled by the series regulator. The name of this regulator refers to how the controlling element is linked to its load. The structure of these two regulators is seen in Figure 2.2. The control element in the series regulator (Figure 2.2 a) is connected in series to the load, whereas the control element in the shunt regulator (Figure 2.2 b) is linked in parallel to the load. These topologies are constituted of a control element, also known as a pass device or power device, and a sensing or sampling element that senses the output voltage and compares it to a voltage reference. The comparator (or amplifier) amplifies the error difference between both signals, producing an analog signal that modifies the control element. In low power applications, the shunt regulator is frequently favored over the series regulator since it consumes less power when the device is switched off (BROOKS, 1991).

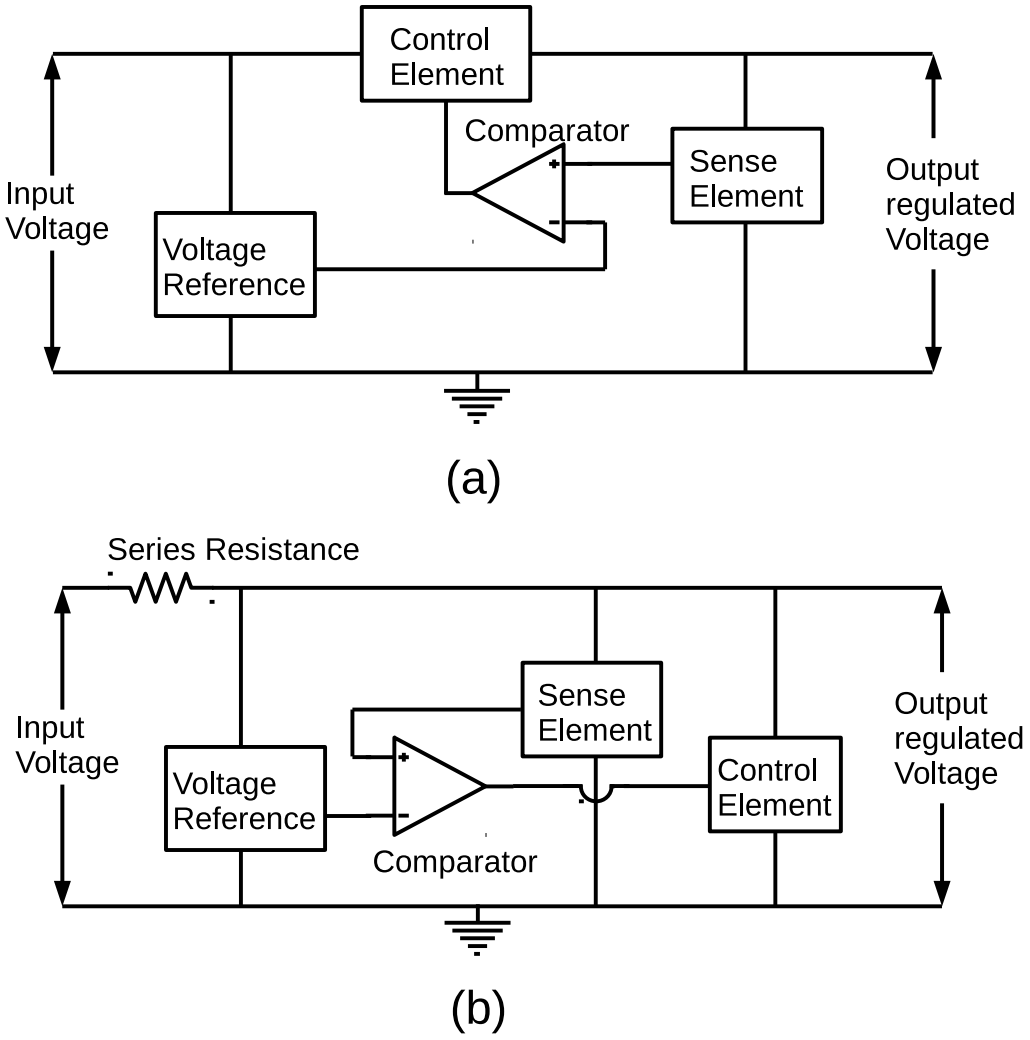
Some aspects of the RFID system operation impose additional requirements on regulator design, as discussed in (BROOKS, 1991; GAY, 2004):

- the transponder operates within a variable range of input power depending on its distance to the reader,
- the regulator must drain the additional power obtained by the input antenna in high power condition,
- the regulator must consume the least possible power in low power conditions,
- during the power-up phase, the shunt regulator must safeguard the internal circuits, acting as quickly as possible,
- the precision of the voltage regulation is determined by the voltage reference's accuracy and the loop gain,
- data communication is often based on Amplitude Shift Keying (ASK) modulation, and as a result, the received RF strength varies with the baseband data. The bandwidth of the regulator is defined by the signal spectrum.

The power condition is defined by the distance between the reader and the transponder. When the reader is distant from the transponder, there is not much power coupled by the transponder's antenna, and the transponder is in a low power (field) state. When the reader is close to the transponder, there is a lot of power (field) coupled by the transponder's antenna, and the transponder is in a high power (field) state.

The I-V characteristic of a power regulator circuit is shown in Figure 2.3. In the ideal curve, no current is drawn until the threshold is reached, and the circuit behaves as a short after that point (GUERIN et al., 2014). The Vtrip is the trip-point voltage where the regulator starts to drain the current excess (FERNANDEZ et al., 2011). The real curve presents a smoother transition between the operation regions depending on its implementation. In the worst scenario, the Vtrip is affected by process variability, supply voltage, and temperature (PVT) conditions. In one way, the protection circuit is specified to prevent damage to the internal circuits according to the chosen CMOS technology. In another way, the PVT variation of Vtrip affects circuit performance in the low field

Figure 2.2: Series (a) and Shunt (b) Regulator



condition, consuming even more power (I(wasted) in Figure 2.3)).

The first shunt regulator utilized with the resonant input source is shown in Figure 2.4. This method consists of an amplifier providing linear feedback, a MOS transistor acting as a shunt element or power transistor, and a voltage reference. The bandwidth of this solution is restricted by the amplifier output resistance and the power transistor (M) capacitance. The operational amplifier power consumption limits the bandwidth of the regulator in low-power systems. Some implementation showed in (GAY, 2004) purposefully includes a low pass filter at their output to drain an average current from the input source. Due to the low dynamic conductance, it creates more ripple in the regulated output line by the modulation signal. This issue is exacerbated when the system is near the reader and receives a strong signal. As the modulation signal is converted to a proportion of the power received, the ripple increases, requiring the use of a large capacitor to suppress the ripple in the line (GAY, 2004).

In (GAY, 2004) a shunt regulator is presented to work around the excessive ripple produced by the modulation signal. Figure 2.5 depicts an alternative shunt regulator implementation composed of two feedback loops. The first loop, which is made up of the resistor divider (R6 and R7), the amplifier (G), and the voltage reference (Vref) drains the excess current through the power switches (M5 and M6). The power switches in the

Figure 2.3: Ideal and Real regulation I vs V

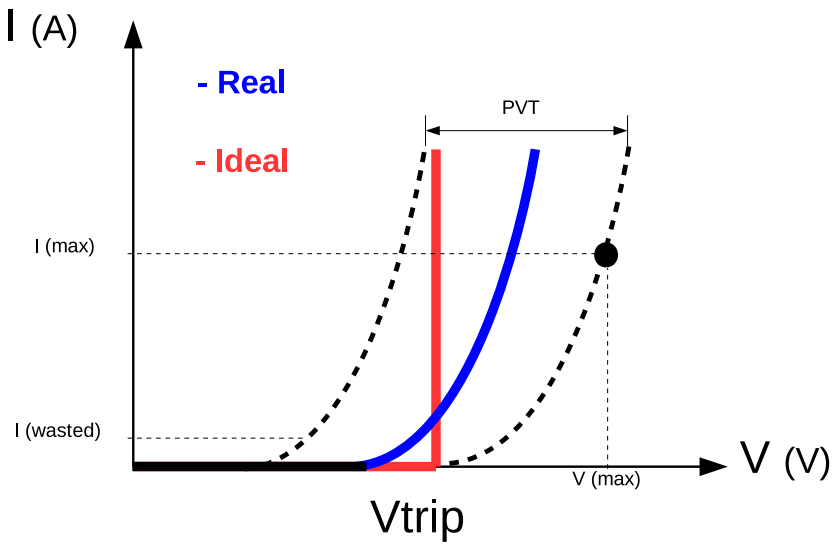
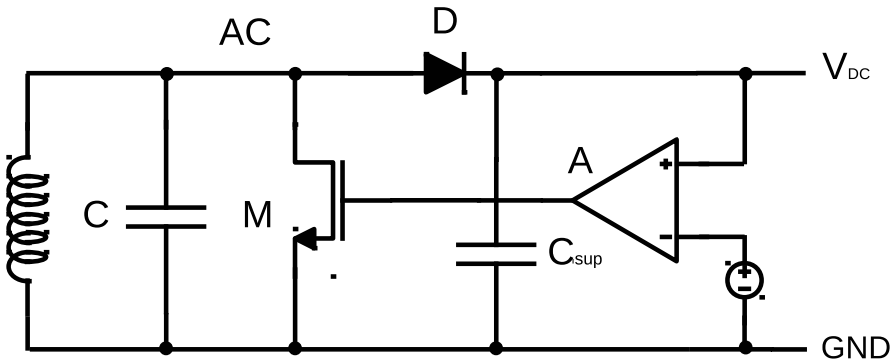


Figure 2.4: Shunt regulator for inductive couple

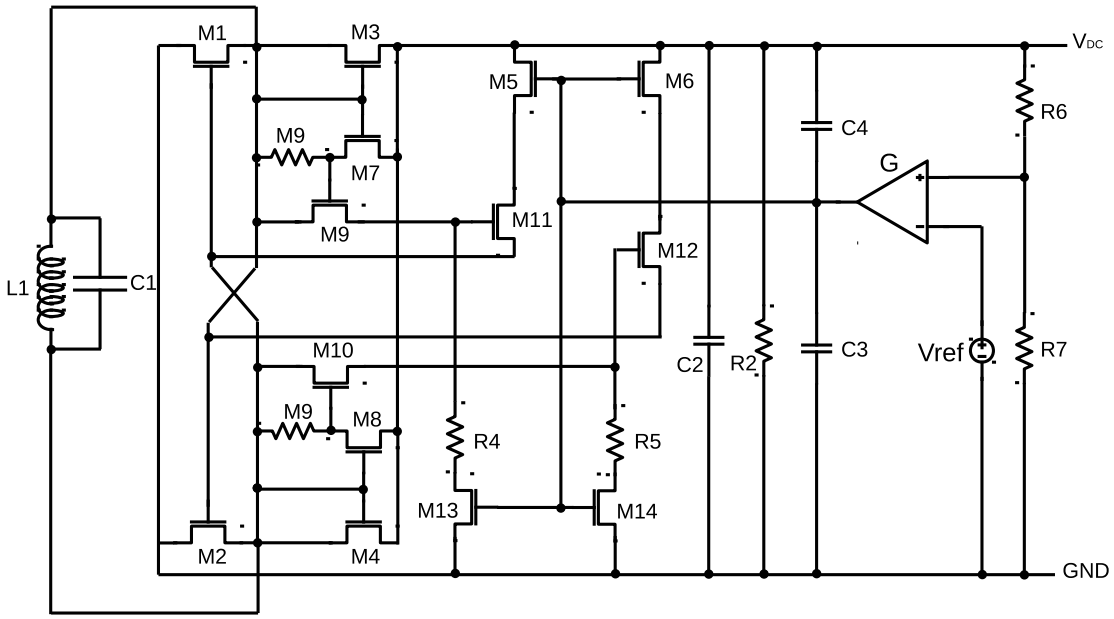


Source: (BROOKS, 1991).

circuit drain the average excess current from the rectifier (M1-M4) output. To achieve a low voltage drop, the rectifier resistance must be reduced, which increases the chip area due to the high current pass (GAY, 2004). A worst-case scenario in RFID regulation happens as the system moves closer to the reader and receives a larger input power. Since the modulated signal is proportional to the received power, a large capacitor C2 reduces the residual ripple (GAY, 2004), resulting in an increase in the chip area. Because this feedback is immediately perceived at the amplifier output, the capacitor dividers C3-C4 offer an extra loop to decrease voltage ripple. It sends a portion of the modulation frequency through M7-M14 and R2-R5 to control the power switches.

Figure 2.6 illustrates the schematic implementation of a rectifier and a shunt regulator (LU; LI; LIN, 2016). The shunt regulator composed of the three diodes and the resistor R1 connected in series, makes the sense circuit connected to the rectifier's output. The power transistors connected to the antenna (M5 and M6) close the regulation loop, draining the excess of the current from the antenna. This architecture has a large bandwidth that does not cause a strong ripple owing to modulation in the regulation line under high field situations due to the low impedance of the diodes series resistance. This type of

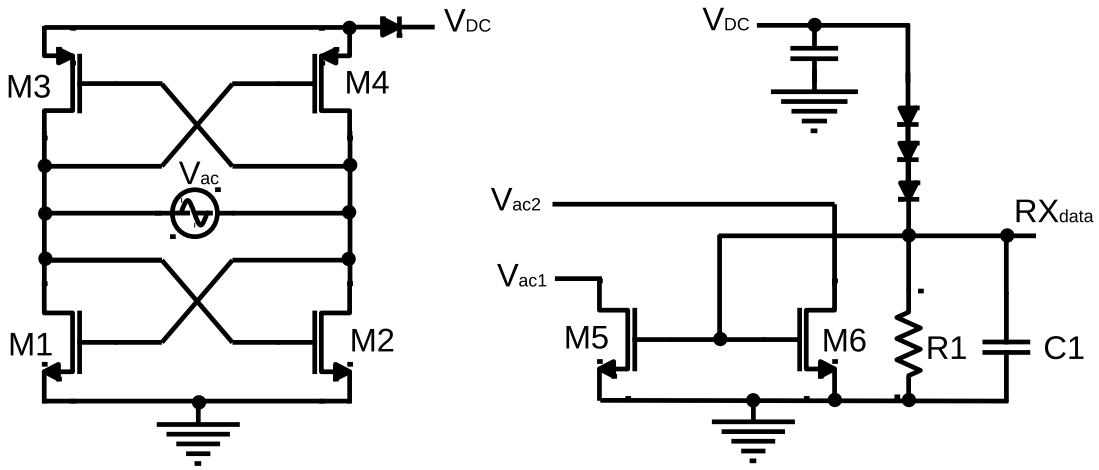
Figure 2.5: Interface for shunt voltage regulator in a contactless smart card



Source: (GAY, 2004).

shunt regulator has many implementations that change some components or the way they are connected (BALACHANDRAN; BARNETT, 2006; GERVACIO et al., 2013; DONG-SHENG et al., 2015; JIA et al., 2012; BHATTACHARYYA et al., 2018). It is used in almost every transponder architecture to guarantee overvoltage protection due to its high bandwidth. The disadvantage is the lack of precision in regulation due to the use of diodes as voltage references, which changes with temperature and process, and its low open-loop gain provided by the power transistor transconductance, which affects transponder power consumption, resulting in reduced performance or read distance in low power conditions.

Figure 2.6: Rectifier and RF over-voltage protection



Source: (LU; LI; LIN, 2016).

The trade-off between precision and high bandwidth becomes clear in transponders' power regulation with the previous implementations cited. In (BALACHANDRAN; BARNETT, 2006), a UHF transponder with regulator dynamic bandwidth boosting is imple-

mented to decrease the voltage ripple due to the modulation signal cited before. It can also be used as a strategy in LF and HF transponders to reduce the ripple in the regulation line due to the energy variation. Still, the clamp circuit connected to the antenna in UHF transponder does not affect the performance of the transponder due to the low antenna voltage (100 - 200m V). As LF and HF work by coupling the magnetic field from the reader and storing it in the resonant tank (LC tank), the input voltage achieves high levels even with low power.

In consideration of work around the initial voltage regulator's imprecision, one method is to employ a high voltage procedure to boost the antenna voltage, for example, 5.5 V in LF and HF RFID applications. In this case, the RF Clamp trip point is set to 5.5 V maximum in the worst corner and the LC tank has the ability to store more energy to be used to supply the transponder in low power conditions. The regulation architecture must be energy efficient, step down the internal voltage at the rectifier output in order to reduce transponder power consumption despite increasing fabrication costs due to the usage of a high voltage process module.

In this work, the RF Clamp trip point is adjusted to 3.6 V maximum in the worst corner to be competitive in the market and use only a 3.3 V process module. The imprecision of the regulation starts to waste power in the lower power condition due to PVT variation. The architecture described in this thesis employs an RF power detector to optimize the RF clamp imprecision based on the incoming RF power due to its high open loop gain, and the use of a voltage reference circuit, more stable on PVT, which defines the new trip point value of the regulation.

2.2 RF Power Detector State-of-Art

Due to the general widespread usage of wireless technologies, communication systems are now present in many devices. The design of a typical super-heterodyne transceiver is seen in Figure 2.7. RF power detectors are widely used in many points of the RF system, with the objective of measuring and controlling the level of the RF power signals transmitted and also to handle with the signal variation in the receive path working together with Variable Gain Control (VGA) as Received Signal Strength Indicator (RSSI in the Figure 2.7) to set the gain in a signal chain to deliver a full-scale signal to the Analog-to-Digital Converter (ADC) at the best Signal to Noise Ratio (SNR) (COWLES, 2011).

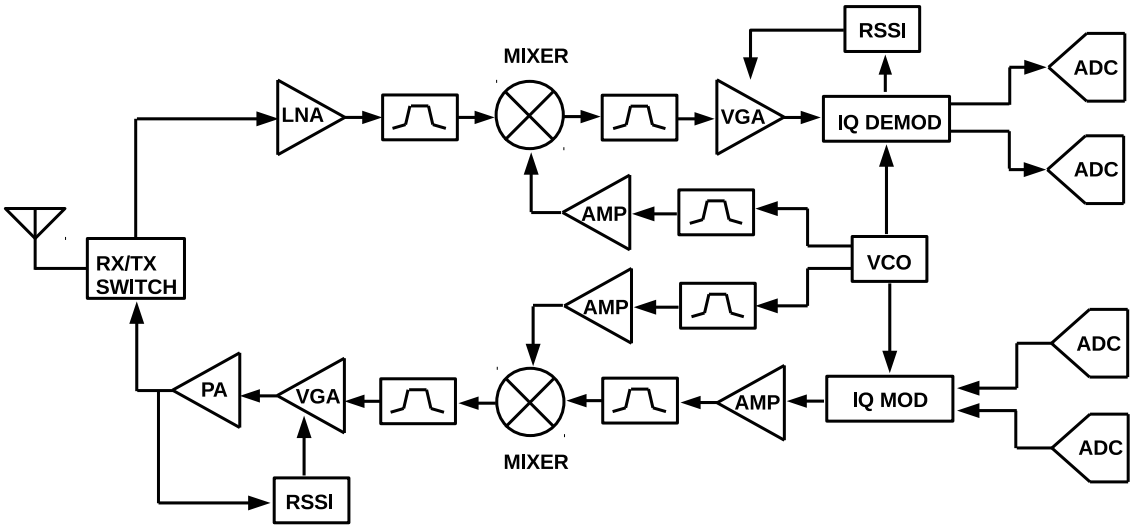
The RF power detectors convert input RF power signals to representative DC voltages. In the state of the art of RF power detectors, there are three types found: peak detectors (or envelop detectors), logarithmic detectors (or log detectors), and Root-Mean-Square (RMS) detectors. Each one of those meets some requirements and they are needed at different points of the RF systems.

2.2.1 Peak Detector

Figure 2.8(a) shows a classic peak detector that uses a diode and a capacitor that converts or stores the peak value of the RF signal as information of the input power. The input signal charges the capacitor through the diode, and the diode retains the charge in an opposite way. In that sense, the power information is acquired through the peak of the input signal. The resistor is a way of discharging the capacitor so that the detector always follows the input signal's peak on its average.

This type of detector has a sensitivity limited by the diode voltage barrier. The Schot-

Figure 2.7: Transceiver architecture



Source: (COWLES, 2011).

tky diode is extensively used to increase the sensitivity of this type of detector. The VT cancellation technique is used to cancel the threshold voltage and the MOS transistor operates in the border of its threshold voltage, increasing the sensitivity of the RF power detectors (CANTALICE et al., 2018). Despite the simple architecture and low power consumption, one of the main limitations is the linearity over PVT variation. In (WIGHT; BRAZEAU; GRANT, 1998), (KURTZMAN; HOGGARTH, 2005) and (PRESTI et al., 2006) many circuits implementation to improve the envelope detector sensitivity and linearity can be found.

2.2.2 Logarithmic Detector

RF logarithmic detectors are commonly utilized in receivers when input power regulation is required due to their quick transient reaction. It also has a high dynamic range and excellent temperature stability over the operation range. There are three ways to achieve logarithmic conversion. Figure 2.8(b) depicts a classic implementation of a log detector which consists of an operational amplifier with a diode in a negative feedback path that uses the diode's log response to generate an output proportional to the input signal, and producing an output signal related in decibels (BARRIE, 1989). The second method is to use an Analog-Digital converter to logarithmically process the digital signal. This method has limited resolution and bandwidth in low voltage amplitudes. The third and most common method is to sequence multi-stage analog amplifiers and detector cells, as shown in Figure 2.8(c). Each step adds a little portion of the entire dynamic range to the output. The advantage of the latter technique is that the power increase required to accomplish operations at low signal levels is dispersed over numerous stages. As a result, the total bandwidth can be rather large and generally independent of signal amplitude (BARRIE, 1989).

2.2.3 RMS Detector

The RMS detector is the third type of detector. As mentioned in 2.1, the power of a waveform may be represented in terms of the RMS voltage and the resistance across

which it dissipates.

$$Power(W) = \frac{V_{RMS}^2}{R} \tag{2.1}$$

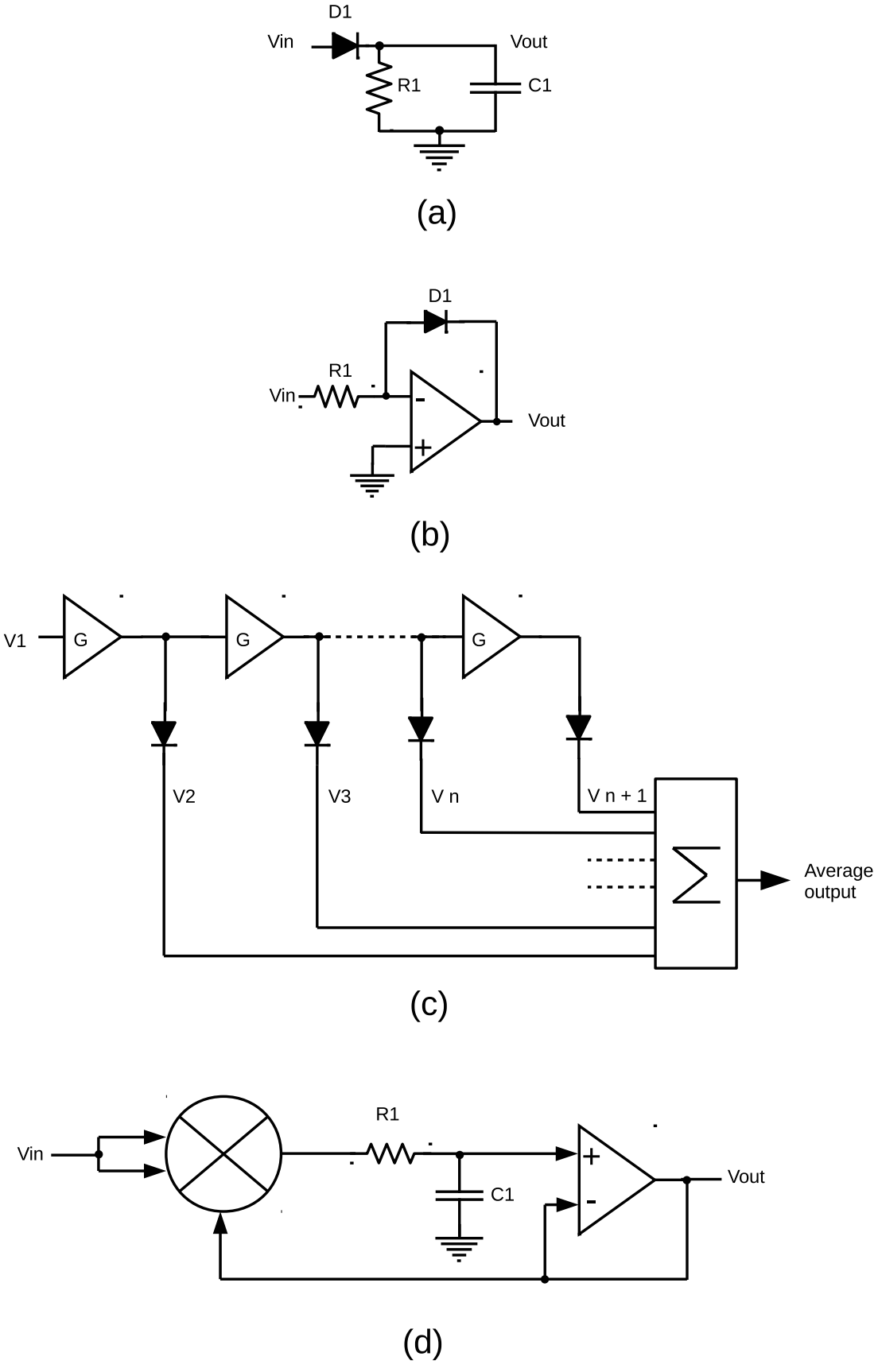
The extraction of RMS power can be accomplished by observing the temperature rise of a thermistor or bolometer when excited by a waveform relative to a reference. While strictly correct, this method is not easy to integrate, since it is susceptible to thermal leakage and limited by slow time constants of heat diffusion (COWLES, 2011). Figure 2.8(d) displays a traditional application of RMS detectors. The RMS detector translates a signal's RMS value into a DC value that represents the signal's power level. As long as the squaring cells can cope with the peak's signal, the topology will generate the RMS voltage with an averaging time related to the filter capacitor. The detectors must be squaring cells rather than the arbitrary envelope detectors cells used in the log-amps to preserve the mathematical assumptions involved in the RMS function (COWLES, 2011). These detectors are capable of measuring the RMS power of a signal independent of the signal waveform and its crest factor, which defines as the ratio of the peak to rms value of the signal, such as high-order quadrature amplitude modulation signals. It also has a high dynamic range and temperature stability over the range used.

Despite the benefits mentioned before for Log and RMS detectors, they are sophisticated structures with power consumption ranging from 1 to 10 mA.

Some essential characteristics for the optimum selection of a suitable detector are highlighted in the context RF detection used in RFID systems. To begin with, the frequency range employed (UHF 915 MHz, HF 13.56 MHz, and LF 135 KHz) is not a constraint for those detectors intended to perform in a wider frequency range than RFID. The majority of RFID modulation is ASK, which does not have a high enough crest factor to warrant an RMS detector. Considering RFID is a low-power device, the ideal candidate is the envelop detector.

In terms of input signal levels and linearity, the UHF has low input signal levels, such as 20mV to 1 V. Except at high power, when the protection circuit begins to work to restrict the input voltage, linearity is rather consistent over the power range. The signal created at the tank is compressed by the circuit protection even in low power settings in LF and HF transponders that function with high signal levels due to magnetic coupling, which stores the energy transfer through the magnetic connection. In this scenario, the power information based on the peak of the input signal may not provide precise information about the power received. The power information is taken from the current produced at the antenna or from any signal at internal circuits via indirect measurement.

Figure 2.8: Peak Detector (a and b), Log Detector (c) and RMS detector (d)

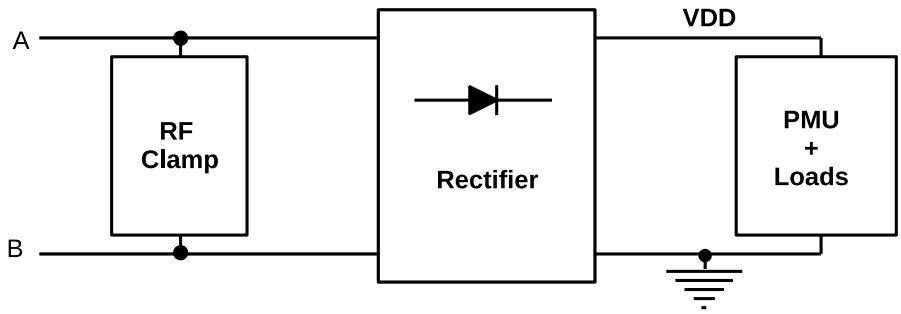


3 A NON-LINEAR SHUNT REGULATOR BASED ON A PWM RF POWER DETECTOR

This chapter presents the proposed shunt regulator architecture which is composed by two feedback loops that enhance the performance of the traditional regulator.

Figure 3.1 shows a simplified block diagram of an LF RFID transponder. It is composed by a shunt regulator called RF clamp, and a Rectifier to converter RF voltage to DC voltage (VDD) in order to supply the analog and digital circuitry (PMU + Loads) including the communication and regulation subblocks necessary to the transponder works.

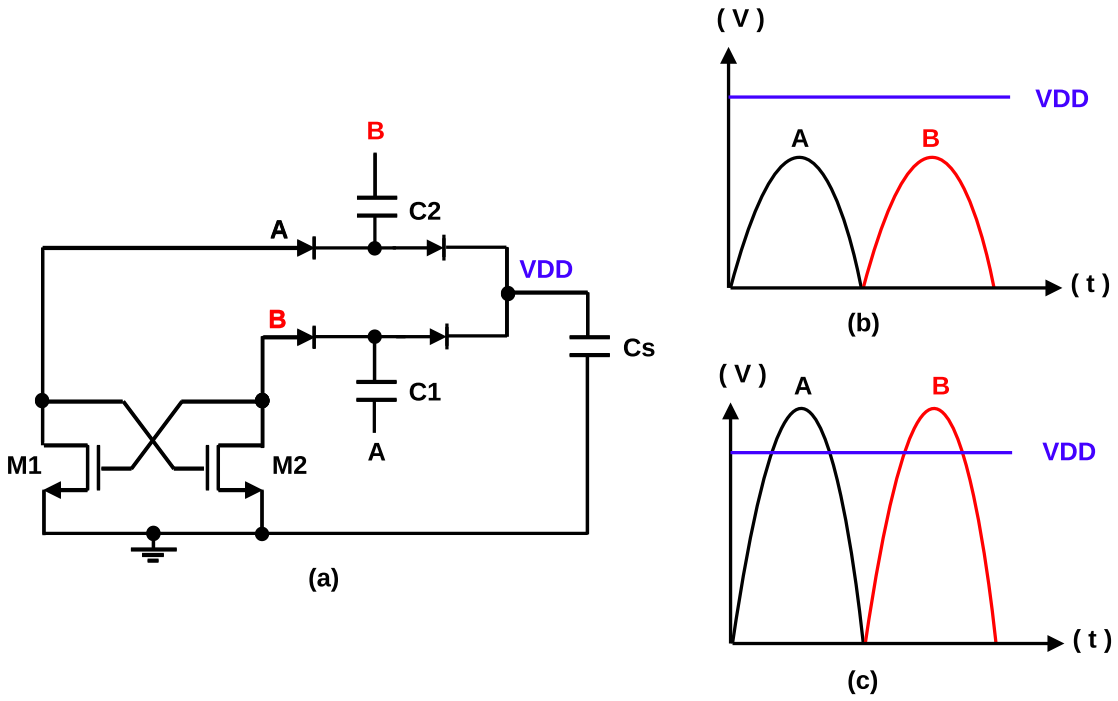
Figure 3.1: Classic LF/HF RFID transponder block diagram



The Rectifier efficiency plays an important role in the low power RFIDs in order to increase the read distance. Figure 3.2 (a) shows a combination of the Dickson Cell or Voltage Multiplier (DICKSON, 1976). The Voltage Multiplier is preferable in order to increase transponder efficiency in low power RFID transponders. The transistors M1 and M2 in Figure 3.2 (a) are used to generate the circuit ground reference in each antenna (A/B) semi-cycle. The C1 and C2 are the Pump capacitors and Cs is the supply capacitor. The diodes can be implemented by any diode junction, bipolar, or MOS transistor. Figure 3.2 (b) shows the antenna terminals (A/B) and the VDD voltage for a low power condition. The VDD voltage generated is higher than the antenna voltage as expected for a Voltage Double cell. In high power conditions in 3.2 (c), the VDD voltage is regulated by another Shunt Regulator at the Rectifier output, making the VDD voltage lower than the antenna voltages (A/B). The VDD voltage is used to distinguish power conditions on the system in this work as will be clear in this section.

To overcome the trade-off between precision and speed on classic RF clamp architectures, as explained before on the State-of-the-Art. The proposed solution is composed of two feedback loops, the inner loop which is fast but not precise, is implemented with diodes at the RF clamp. The external loop is composed by an RF power detector removing the imprecision of the first loop using a voltage reference (V_{REF}) and a high open loop

Figure 3.2: Rectifier architecture (a), antenna voltage (A/B) and VDD signals for low power condition (b), antenna voltage (A/B) and VDD signals for high power condition (c).



gain of the RF power detector. Figure 3.3 shows the block diagram of the proposed solution. The voltage reference used in the RF power detector is the supply voltage (VDD) which is defined by the shunt regulator at the rectifier output through a precise voltage reference.

The RF clamp architecture chosen for the inner is detailed in Figure 3.4. The loop is designed to have a fast response that guarantees protection during the power-up phase, or during abrupt variations of the RF field. It is composed of 3 diodes for each antenna terminal (A/B), in series with a resistor (R), and a NMOS power transistor (M1). When the antenna (A/B) voltage is higher than the three-diode forward voltage, the diodes start to conduct current, generating a control voltage over the resistor. This voltage modulates the NMOS transconductance, draining current, and regulating the antenna voltage. The diodes are used as a voltage reference on the first loop. The resistor and the MOS transconductance together with the diodes define the RF Clamp trip-point, which is the voltage that triggers the current drained by the RF clamp, and the regulator gain (I vs V). The diode forward voltage, the resistor value, and the MOS transconductance are process and temperature dependent. Those variations are responsible for the imprecision of this architecture, changing its trip-point and its gain. The transistor M1 work symmetrically in each carrier semi-cycle, its bulk is tied to the ground reference generated by the Rectifier in each cycle.

In low power conditions, the imprecision of the RF clamp impacts the transponder's performance wasting power that can be used by the transponder. In order to improve the precision of this architecture, extending the range of the RFID link, an RF power detector controls a variable resistor that is put in parallel with the resistor of the RF clamp as

Figure 3.3: Proposed LF/HF RFID transponder block diagram

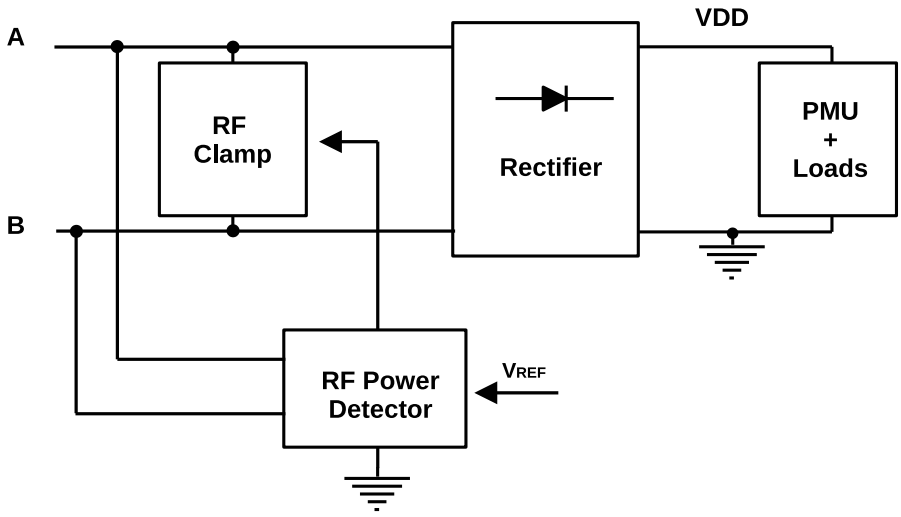
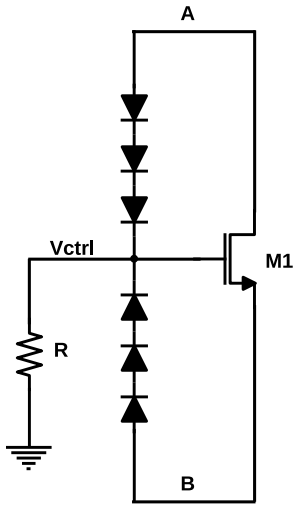


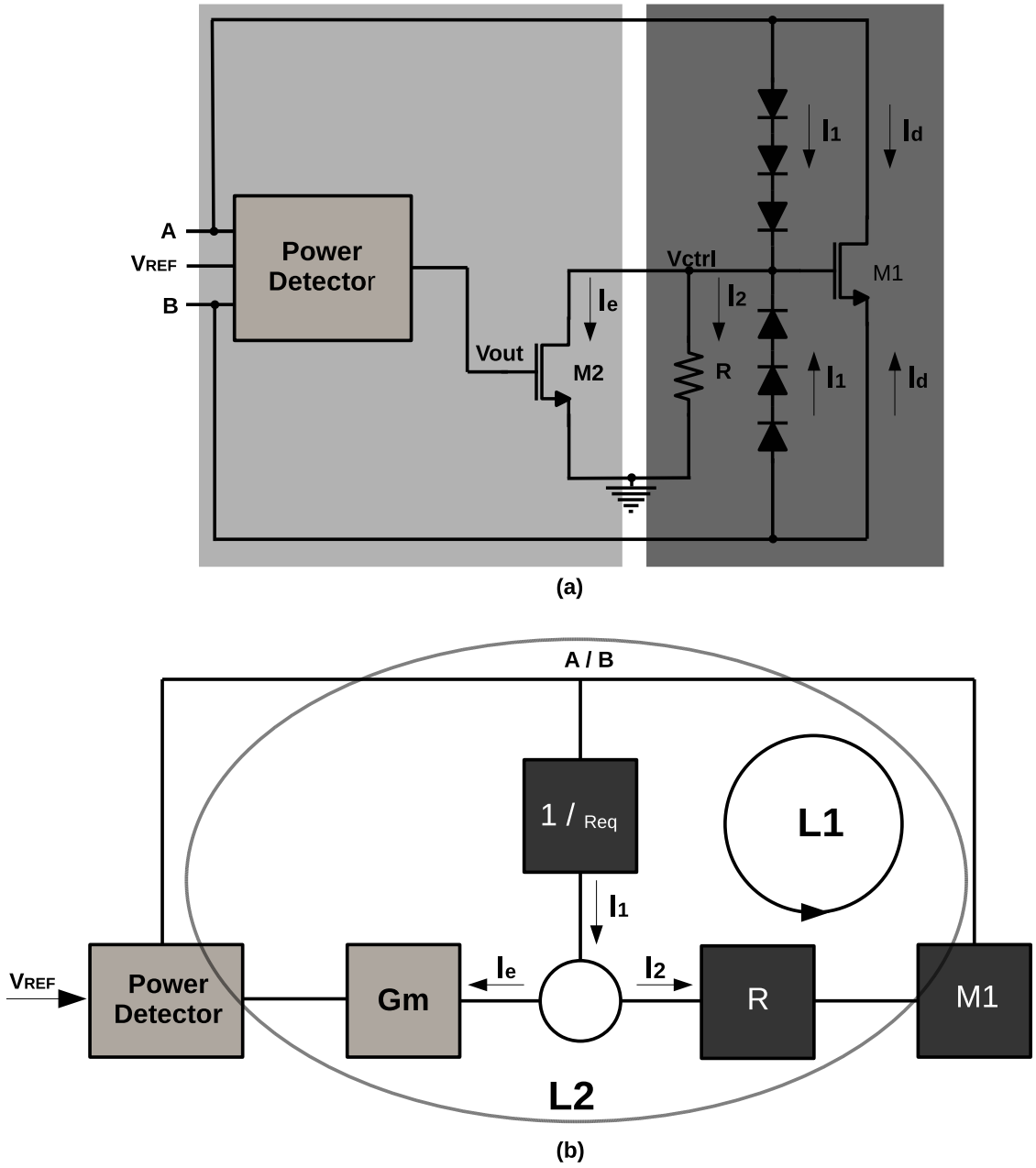
Figure 3.4: RF Clamp architecture



shown in Figure 3.5(a) for the external loop (L2). The variable resistor was implemented using a MOS transistor (M2) operating in the linear region. In this condition, the shunt regulator trip-point is defined by the precise voltage reference and the high gain of the RF power detector that overcome the variation of the inner loop (L1) due to process and temperature, changing the variable resistor.

The control diagram in Figure 3.5(b) describes the function of each element. The antenna voltage over the diodes (rd_{eq}) and the resistance R result in the currents I_1 and I_2. When RF input power is high, the power detector keeps M2 off, and I_2 approximates I_1. When RF input power decreases, M2 becomes active and adjusts the output voltage through the external loop (L2). In this situation, I_e is subtracted from I_1, reducing I_2. In consequence, the gate voltage of M1 decreases, and the antenna voltage is stabilized.

Figure 3.5: Proposed shunt regulator (a) and its control diagram (b)



The RF power detector is shown in Figure 3.5(a) will be explained in detail in the next section.

Before going into detail and explaining some parameters used in this work. The

3.1 PWM RF power detector

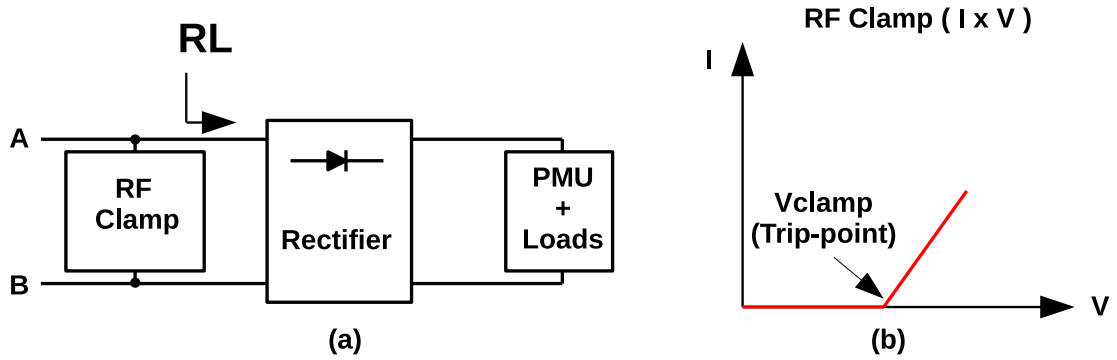
A new approach was developed to produce a low-power RF detector for LF and HF RFID that pulls power information from the antenna signal by inferring the peak signal by its transition time before the signal accomplished circuit protection when clamped. It is implemented by generating a PWM signal by comparing the antenna voltage to a voltage reference. In a range where the protection circuit does not even clip the signal, the PWM

signal can be connected to the signal generated at the antenna. The fundamental advantage of this method is that it provides information regarding RF power in systems that deal with high signal levels, such as LF and HF RFID transponders. Another advantage is the use of a voltage reference to perform the conversion, which adds accuracy for temperature and process. Finally, in comparison to the envelop detector, the circuit has the same time constant for charge and discharge.

To explain the mechanism and establish an analytic formula that connects RF input power to DC voltage output, several assumptions concerning its implementation in a clamped RFID system are required:

- a simplified LF/HF RFID transponder is considered (Figure 3.6 (a)),
- the input power (P_{in}) comes from a sinusoidal voltage with a peak value equals to $V_p = \sqrt{2P_{in}R_{in}}$,
- the equivalent input resistance (R_{in}) of the system is approximated by the parallel association between the RF clamp resistance and the equivalent load resistance R_L,
- R_L is assumed constant,
- the induced sinusoidal input voltage is rectified, and its peak is limited to Vclamp by the RF clamp stage,
- the RF clamp stage IxV behavior is approximated as depicted in Figure 3.6 (b),
- below Vclamp, the RF clamp resistance is much higher than the other equivalent resistances, thus not affecting the system,
- above Vclamp, the RF clamp resistance is much lower than the other equivalent resistances, and the voltage signal is clamped.

Figure 3.6: Simplified LF/HF RFID transponder block diagram (a), RF Clamp stage (I x V) simplified curve (b)



The proposed detection strategy works in the region below Vclamp, where the RF clamp circuit presents high resistance. It estimates the available RF input power by inferring the input voltage peak through its rise time before the clamping stage becomes active. This information is translated into a PWM signal and filtered to generate an analog output voltage. Figure 3.7 shows the proposed architecture composed of the voltage comparator, control logic, and filter. Figure 3.8 depicts the timing diagram of the main signals.

Figure 3.7: High-level block diagram

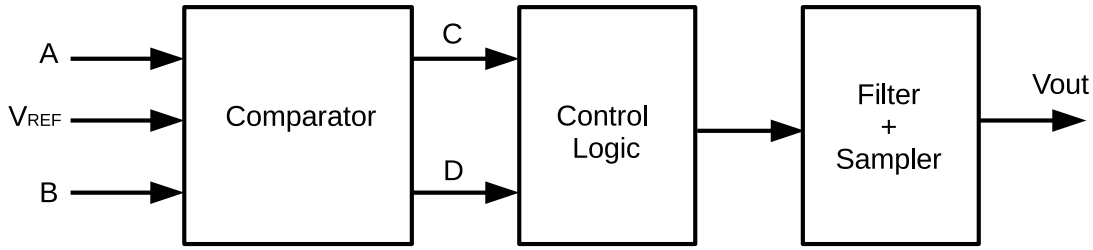
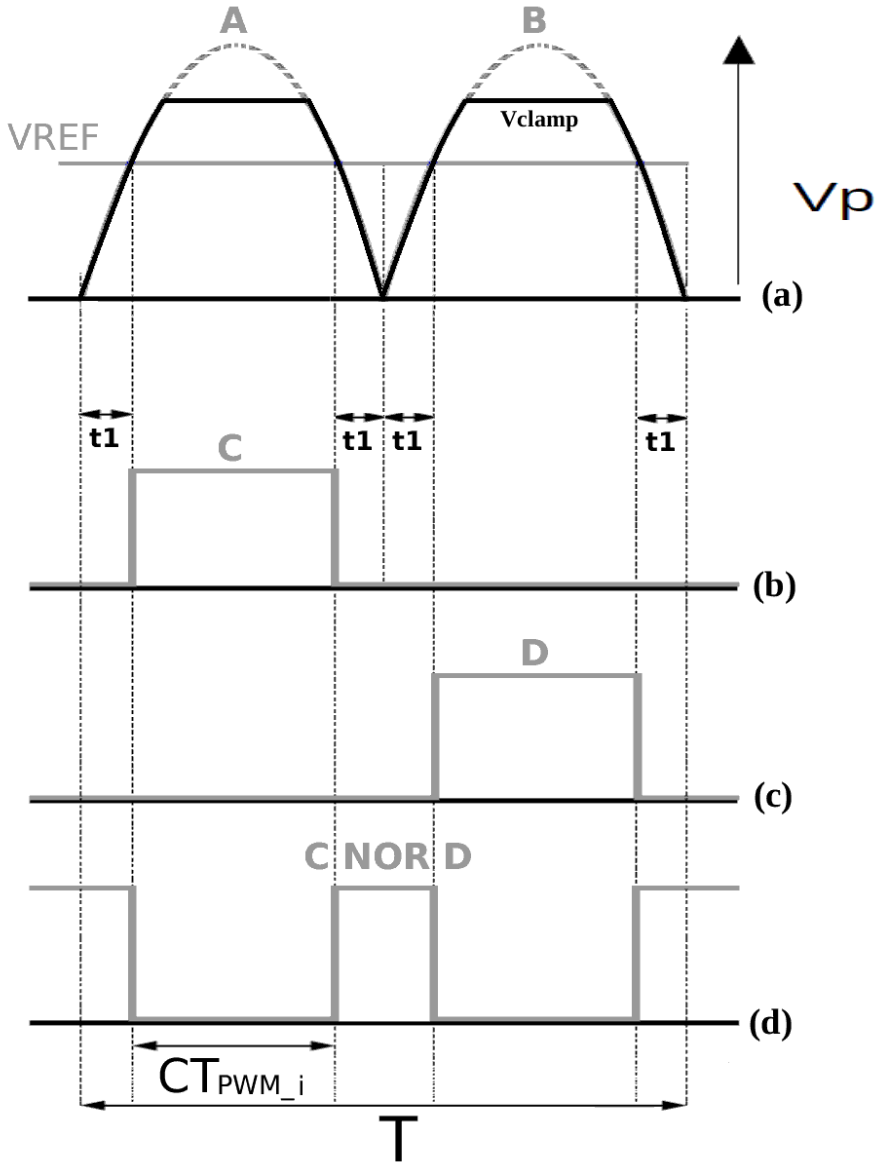


Figure 3.8: Method implementation time diagram



The clamped input voltage signals (A and B) are compared with a voltage reference (V_{REF}) resulting in signals C and D. For a given input amplitude V_p and frequency ($f =$

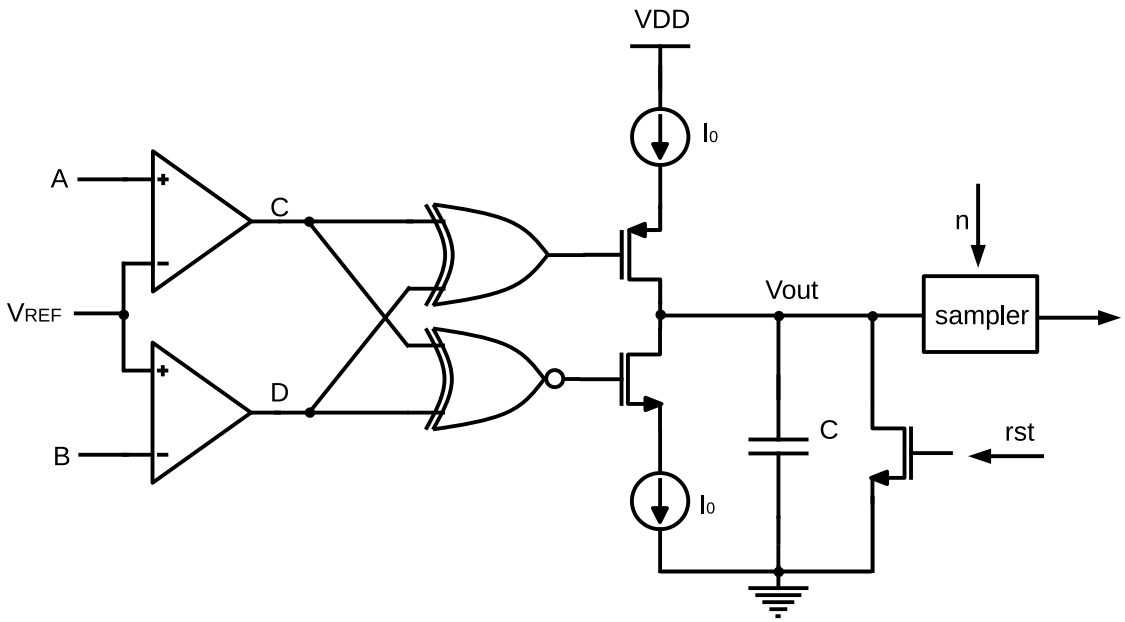
$\frac{1}{T}$), the time $t1$ required to go from 0 to V_{REF} is given by Eq. 3.1.

$$t1 = \frac{T}{2\pi}\sin^{-1}(\frac{V_{REF}}{V_p}) \tag{3.1}$$

It should be noted that the pulse width of C and D depends on the value of V_p. Both signals are fed into the control logic that makes a logical sum of them. After that, a filter returns a DC output voltage (V_{out}) that is inversely related to the input voltage peak.

A high-level implementation of the PWM RF power detector is depicted in Figure 3.9. This implementation helps to understand how the PWM RF power detector works and its formulation in terms of circuits. The implementation is composed of two voltage comparators, it receives the signals A and B that are clamped and shifted by 180 degrees. The control logic is composed of the XOR and XNOR gates that implement a logical sum of C and D. The filter consists of two switched current sources and a capacitor. The signals C and D control the switches, represented in Figure 3.9 by the NMOS and PMOS in series with the current sources, that charge and discharge the capacitor generating the DC output voltage in a certain time window. The sampler circuit, illustrated in Figure 3.9 serves to define the window time to capture the analog voltage. It can be understood as the oscilloscope measurement after a trigger signal or the sampling time taken by an ADC converter to process the measurement.

Figure 3.9: PWM detector block implementation



During a period T of the input signal, there are four occurrences of $t1$ (Figure 3.8). The pulse width (CT_{PWM_i}) used to charge the output capacitor is given by Eq. 3.2.

$$2CT_{PWM\_i} = T(1 - \frac{2}{\pi}\sin^{-1}\frac{V_{REF}}{V_p}) \tag{3.2}$$

A factor n can be defined as the number of samples of period T required to charge the capacitor C from 0 V to the supply voltage (V_{DD}) with a constant current I_0 (3.3). This

factor defines the maximum sampling time window in which the circuit still respects its linearity.

$$n = \frac{CV_{DD}}{TI_0} \tag{3.3}$$

The integration of the output voltage during the period n results in V_{out_i}, given by Eq. 3.4, which defines the DC output voltage as a function of the peak of the RF input voltage.

$$V_{out\_i} = V_{DD} - \frac{2}{\pi} \sin^{-1} \frac{V_{REF}}{V_p} \tag{3.4}$$

After the sampling process concluded, the filter capacitor must be discharged by a reset switch and the cycle restarts. This process can be implemented multiple times, and it takes the average of the measurements to reduce the error by a single measurement. The voltage reference defines the input signal's level to be detected or the power detector sensitivity (low to high amplitude signals). The detection range can be increased using different voltage references and a search selection method in order to track the signal amplitude from a low to a high level.

3.1.1 Power detector High-Level Simulation

A high-level simulation was performed and compared to the theoretical equation (Eq. 3.4) to validate the method. The high-level implementation of the PWM RF power detector depicted in Figure 3.9 uses the comparators and the XOR and XNOR gates described in verilogA models in order to have a precise PMM signal. The current sources and the switches are implemented using real transistors due to their simplicity. The sampler and the reset circuit are not used in this simulation. The sampler concept in Figure 3.9 is the time taken to get the filter's output voltage (Vout) on the simulation.

The design parameters are presented in Table 3.1.

Table 3.1: Design Parameters

	Value	Unit
V_{REF}	2.5	V
V_{DD}	3.3	V
C	1	pF
I_0	40	nA

The voltage reference is defined as 2.5 V, below the RF clamp trip point. A 135 kHz sinusoidal voltage simulates the antenna signal and is increased from 2.4 to 3.8 V. The chosen frequency is used in LF RFID systems. The 3.3 V supply is the nominal voltage for the standard 180 nm CMOS process. A load capacitor is estimated to be in a range of 0.5 pF to 1 pF, considering the parasitic. It was used for the first guess 1 pF. The load capacitor and 40 nA current source was used to implement the output filter. The sample time factor n is calculated by Eq. 3.4, resulting in 82.5 μs of integrating time. Figure 3.10 depicts the integration of the output voltage (Vout_i) during the 82.5 μs period for different input voltages (Vp). It results in a "DC output voltage" inversely proportional to the input peak voltage.

Figure 3.10: Integration of the output voltage during n periods for different input peak voltages

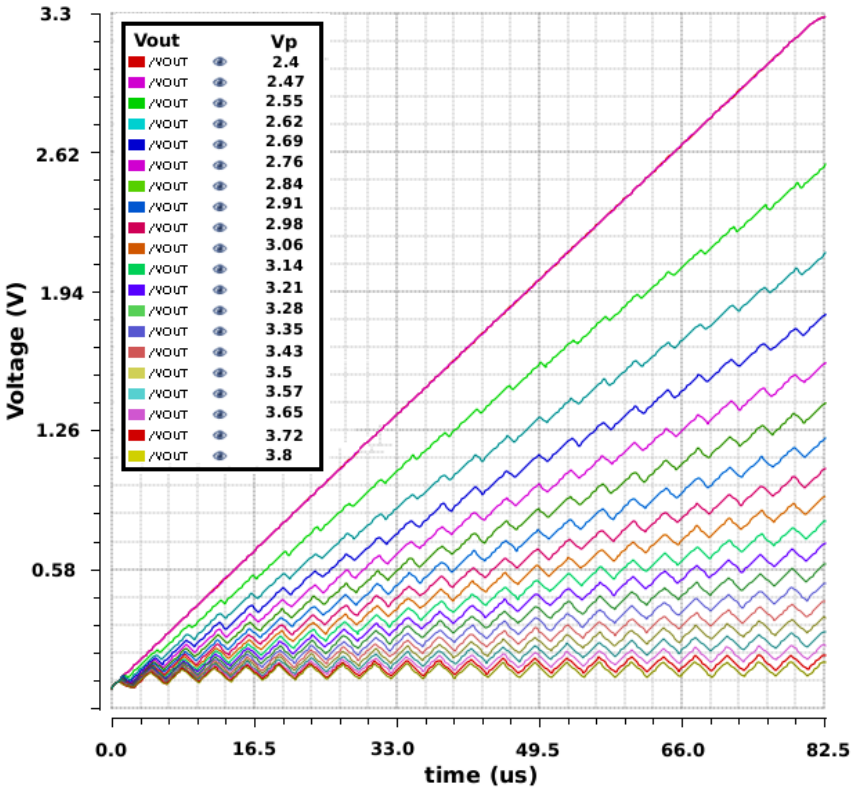
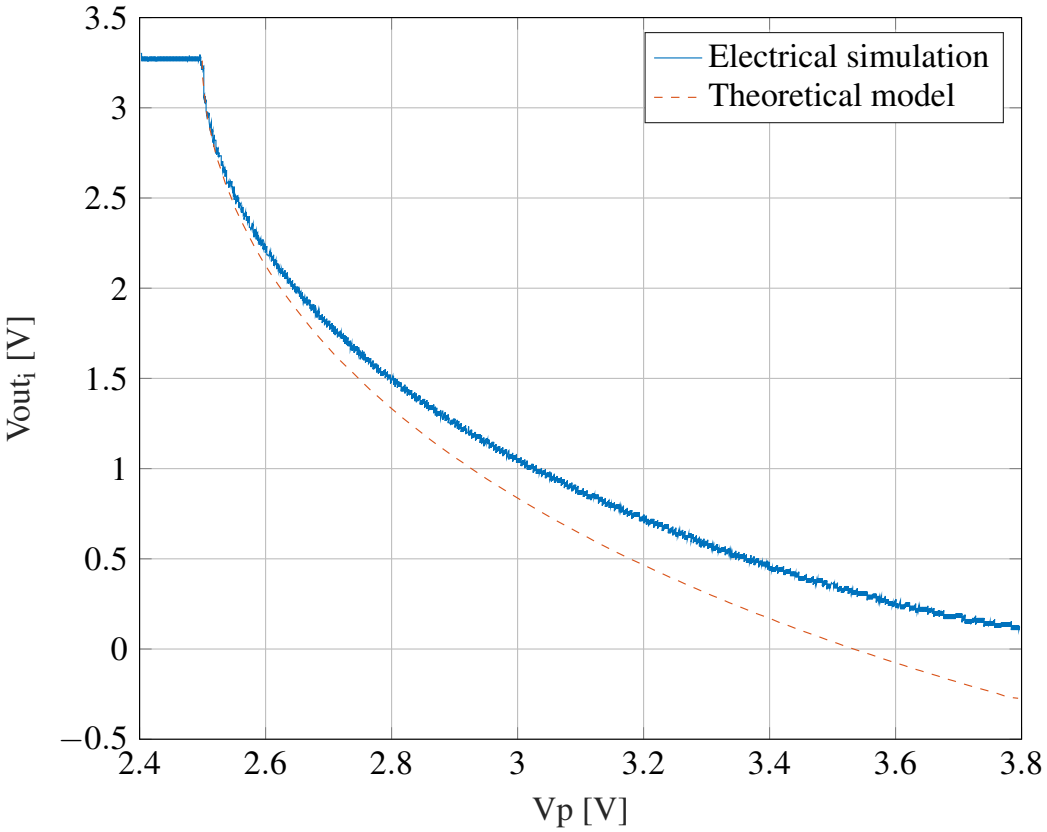


Figure 3.11 depicts the PWM RF power detector characteristic (DC output voltage vs. RF input peak) for both the theoretical model (Eq. 3.4) and the high-level electrical simulation of Figure 3.9. The main difference between both occur because the current source in Eq. 3.4 is ideal and does not saturate, also being able to define a negative voltage over the capacitor. The high-level implementation does not include delays from the comparator, and logic. However, in the real circuit implementation, these non-linearities will result in distortions on PWM signal producing errors in the DC output voltage.

Figure 3.11: Sampled Vout vs. input peak voltage for both theoretical and high-level electrical models



3.2 Shunt Regulator Small-Signal Analysis

This section presents the small-signal model of the shunt regulator. It is divided into two blocks: the power detector and the RF clamp.

3.2.1 Power detector

The power detector is a non-linear block and needs to be first linearized to result in a small-signal model. Figure 3.12 shows the power detector building blocks.

Eq. 3.5 gives the power detector transfer function $G(s)$ as the product of the transfer functions of the PWM modulator $G1(s)$ and the charge pump filter $G2(s)$.

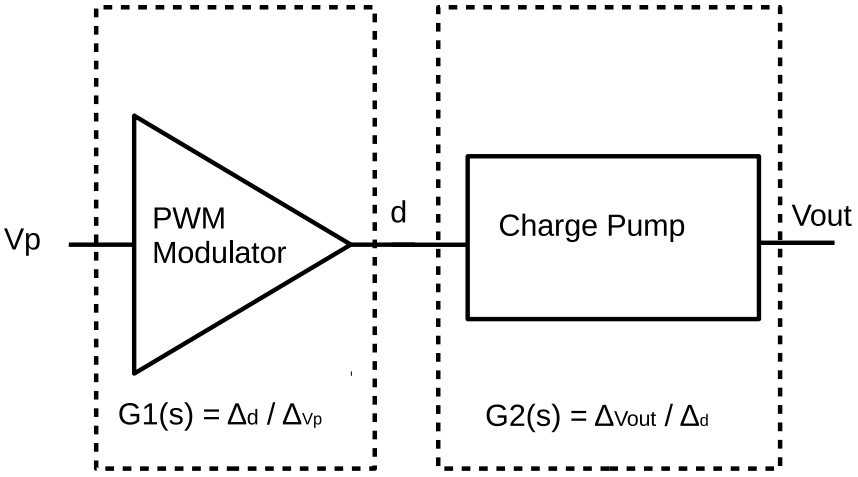
$$G(s) = G_1(s)G_2(s) = \frac{\Delta V_{out}}{\Delta V_p} \tag{3.5}$$

$G1(s)$ can be defined by Eq. 3.6 as the small-signal variation of the duty cycle (Δd) over the antenna voltage (ΔV_p).

$$G_1(s) = \frac{\Delta d}{\Delta V_p} \tag{3.6}$$

The duty cycle defined by Eq. 3.7 as the ratio between the time in which the output signal from the power detector stays in a low state ($2CT_{PWM}$), as presented in Figure 3.8,

Figure 3.12: Power detector building blocks



and the total period (T).

$$d = \frac{2CT_{PWM}}{T} \tag{3.7}$$

Eq. 3.7 can be re-written as Eq. 3.8 using Eq. 3.2.

$$d = 1 - \frac{2}{\pi}\sin^{-1}\frac{V_{REF}}{V_p} \tag{3.8}$$

The derivative of the duty cycle d by the antenna voltage V_p gives the $G_1(s)$ transfer function Eq. 3.9, which in this case is constant in the s domain.

$$G_1(s) = \frac{-\frac{2}{\pi}}{\sqrt{1-(\frac{V_{REF}}{V_p})^2}} \tag{3.9}$$

The charge pump transfer function can also be defined by the small variation of the output voltage over the duty cycle, as presented in Eq. 3.10.

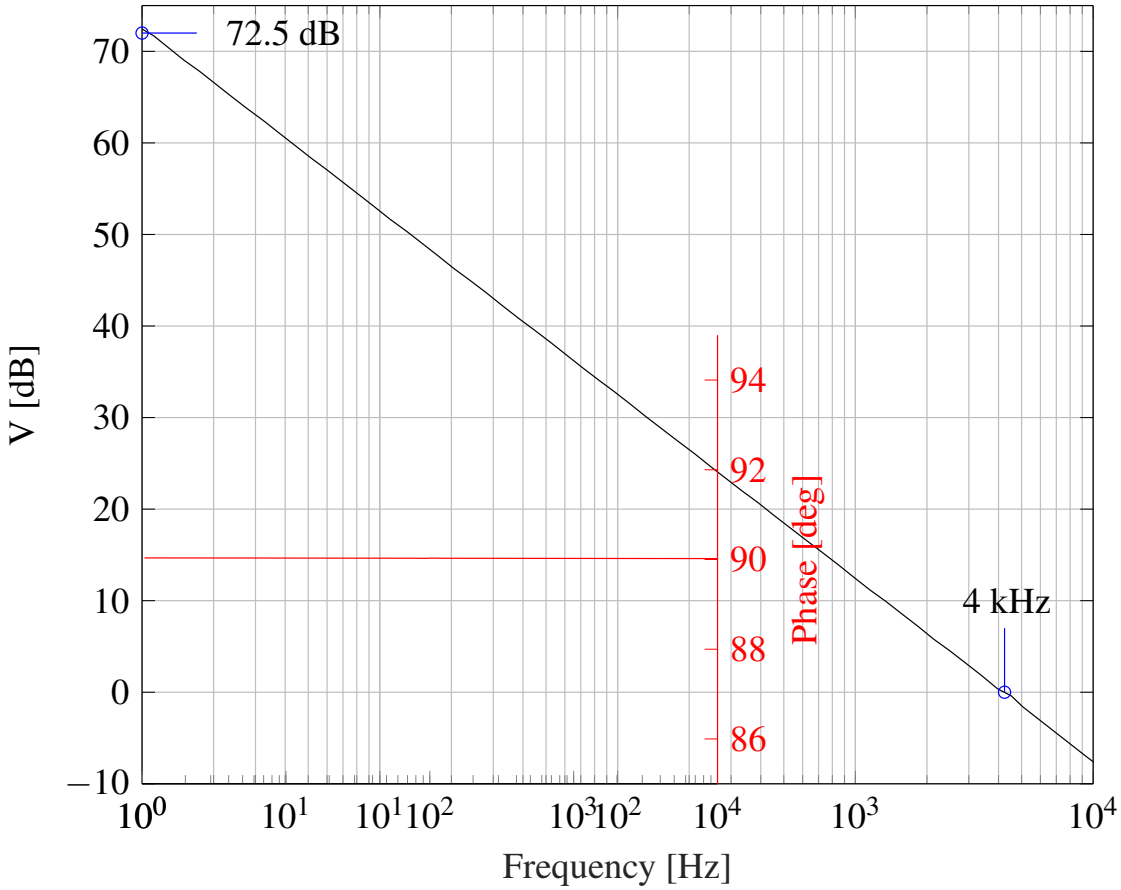
$$G_2(s) = \frac{\Delta V_{out}}{\Delta d} = \frac{I_0}{2\pi sC} \tag{3.10}$$

The power detector transfer function $G(s)$ is then written as follows.

$$G(s) = \frac{-I_0}{\pi^2 sC}\frac{1}{\sqrt{1-(\frac{V_{REF}}{V_p})^2}} \tag{3.11}$$

As observed in Eq. 3.10, the charge pump is an integrator providing minimal error for the steady-state regulation due to the high DC gain. This integrator pole defines the power detector response. Considering the design parameters as V_p = 3.5 V, V_{REF} = 2.9 V, C = 600 fF, and I_0 = 40 nA, chosen to be more realistic based on the project design in order to get the real response of the regulator, and also to optimize the regulator design regarding power consumption, area, and output ripple, Figure 3.13 is obtained. It shows the bode plot of the power detector linearized model, implemented in Verilog A, with the real loads connected to its output to implement the regulator.

Figure 3.13: Power Detector Bode Plot



3.2.2 RF clamp

Figure 3.14 shows a simplified small-signal model of the RF clamp. Its transfer function $H(s)$ can be defined as the small variation ΔV_p over ΔI_d, using Eq. 3.12.

$$H(s) = \frac{\Delta V_p}{\Delta I_d} \tag{3.12}$$

The RF clamp defines the inner loop transfer function. rd_{eq} is the series diodes equivalent resistance, R is the resistance, C_{gs} is the $M1$ gate to source capacitance, gm_1 is the $M1$ transconductance, and rds is the $M1$ drain to source resistance. For this model, Eqs. 3.13 to 3.15 define the feedback loop gain β.

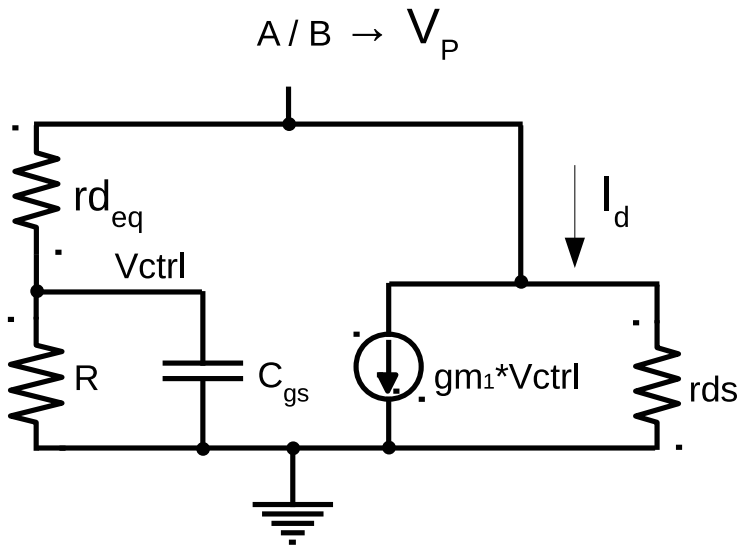
$$Z_2 = R \parallel C_{gs} \tag{3.13}$$

$$\beta = \frac{Z_2}{Z_2 + rd_{eq}} = \frac{R}{R + rd_{eq}} \frac{1}{1 + sC_{gs}rd_{eq}} \tag{3.14}$$

For $rd_{eq} << R$,

$$\beta = \frac{1}{1 + sC_{gs}rd_{eq}}. \tag{3.15}$$

Figure 3.14: RF Clamp small-signal representation



The closed-loop transfer function $H(s)$ is defined in Eq. 3.16 for $gm_1 rds >> 1$ and $rd_{eq} << R$.

$$H(s) = \frac{gm_1 rds}{1 + gm_1 rds\beta} \approx \frac{1 + sC_{gs} rds}{1 + sC_{gs}\frac{rd_{eq}}{gm_1 rds}} \tag{3.16}$$

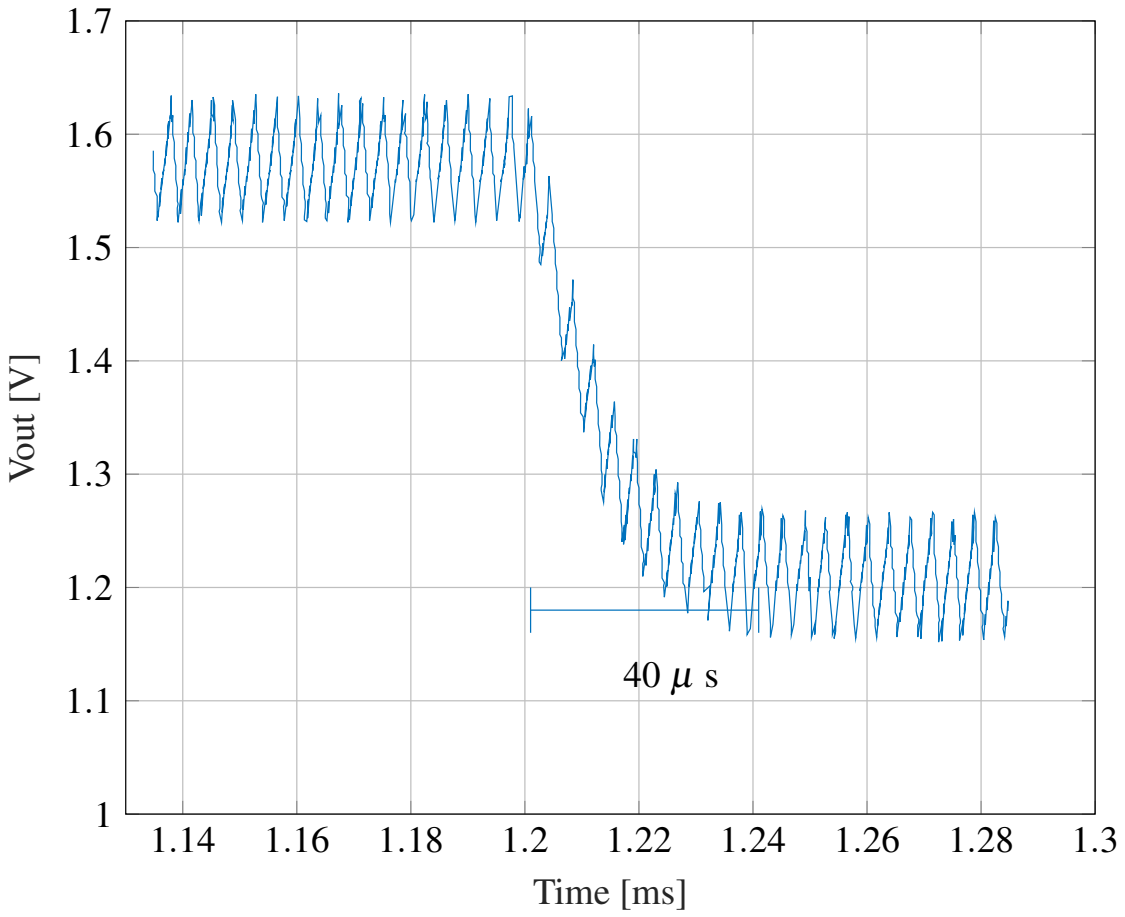
The RF clamp has a unitary gain and high-frequency pole, which guarantees the overvoltage protection.

3.3 Regulator step response

The power detector dominates the shunt regulator step response since the shunt regulator transfer function is equal to $G(s)H(s)$, and the RF clamp $H(s)$ has the highest frequency pole. Figure 3.15 shows the step response of the shunt regulator for a small variation on the input. The change in the field magnitude produces changing in the coupling factor of the link made by the reader and the transponder, from 2 m to 5 m, this range represents the low power condition or a faraway reader condition.

In this simulation, the power detector circuit uses the comparator implemented in a high-level description language (Verilog A) to remove the block's delay and compare the linearized model response with the shunt regulator response. The unitary gain bandwidth of the linearized model shown in Figure 3.13 and is equal to 4 kHz, which results in the shunt regulator step response of 40 μs, as shown in Figure 3.15.

Figure 3.15: Shunt regulator step response



3.4 Regulator CMOS implementation

Before going into details on schematic implementation of the proposed shunt regulator, Figure 3.16 shows the shunt regulator shown in Figure 3.5 with the block diagram of the PWM power detector.

3.4.1 Power detector schematic implementation

Figure 3.17 shows the schematic of the comparator block. This circuit uses a common-gate architecture to minimize the area and power consumption. The circuit is composed NMOS current mirrors (M1, M2, M3, M4, and M5), PMOS transistors M6 and M8 that generates bias voltages Vb1 and Vb2, and PMOS transistors M7 and M9 that compare V_{REF} to the antenna voltages A and B. Note the bulk selector circuit must be used to maintain both pairs M7 and M9 bulks at the highest voltage potential. The bias voltages Vb1 and Vb2 are adjusted by a mirror ratio N. If N=1 and the PMOS transistors are matched, a useful comparison can be achieved directly between the antenna voltages A and B and the voltage reference V_{REF}. Signals C and D are generated by comparing the V_{REF} and the antenna voltage (A and B). The mirrors M1-M5 must be biased in strong inversion to guarantee a proper matching of the current mirror.

Figure 3.18 shows the schematic of the bulk selector circuit cell. It implemented by two PMOS cross-coupled M1 and M2. Two cells are needed in order to compare A with

Figure 3.16: Proposed shunt regulator

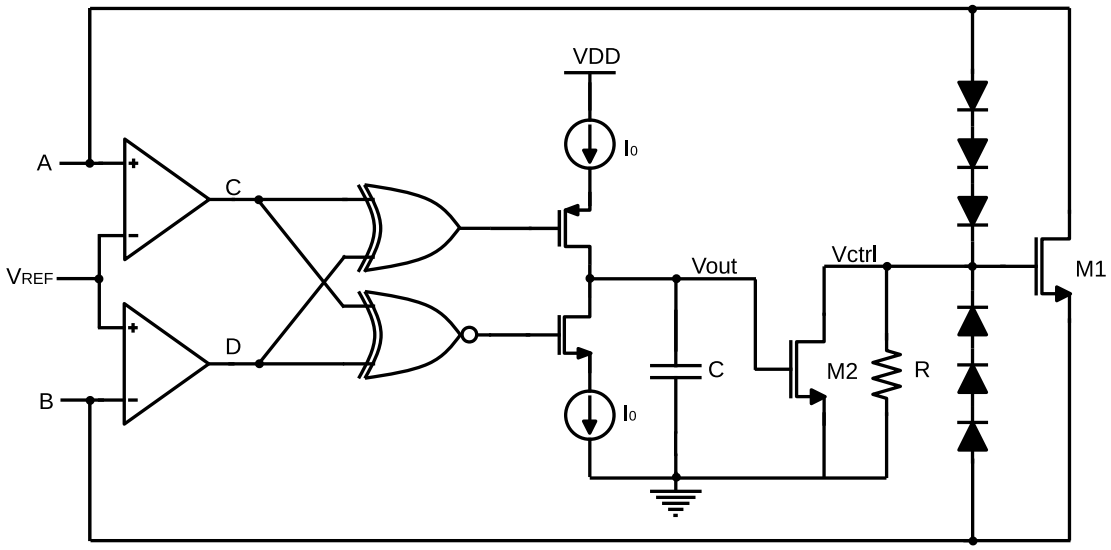
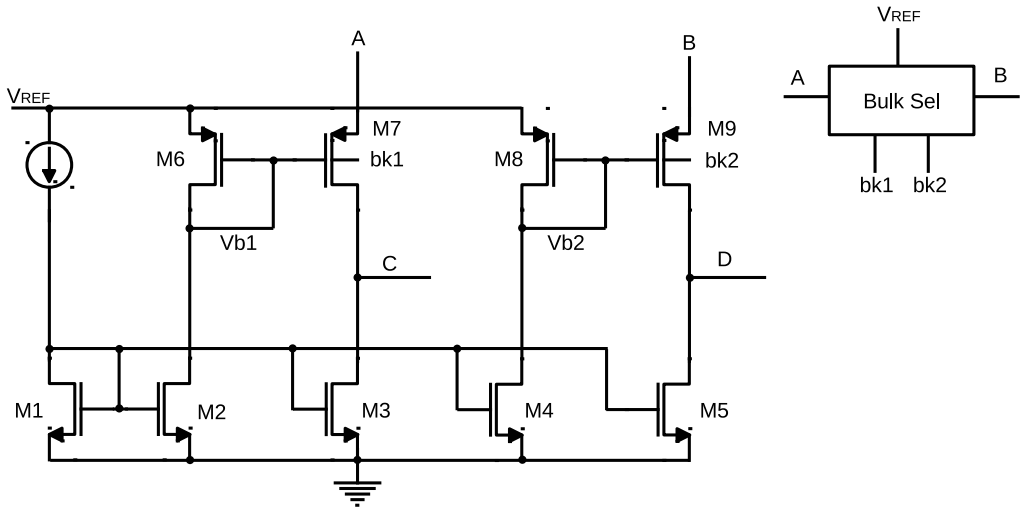


Figure 3.17: CMOS comparator implementation



RVDD, and B with RVDD in order to bias each comparators, M7 and M9 respectively in Figure 3.17.

Figure 3.19 shows the schematic implementation of the Control Logic and the Charge Pump circuit. The logical sum combined with the switches optimizing the number of components. The load capacitor (C1) must be chosen to keep the ripple of the average output voltage below 20%. The current sources are simple, matched current mirrors.

There are different ways to implement the control logic, where various logic gates can be used. Depending on the logic used, the generated signal at its output will be directly or inversely proportional to the incoming input power.

Figure 3.18: Bulk selector implementation

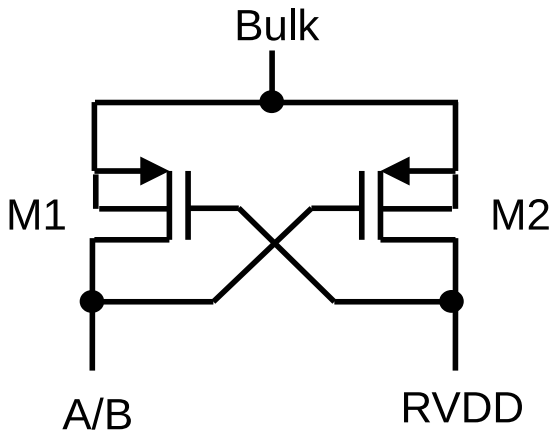
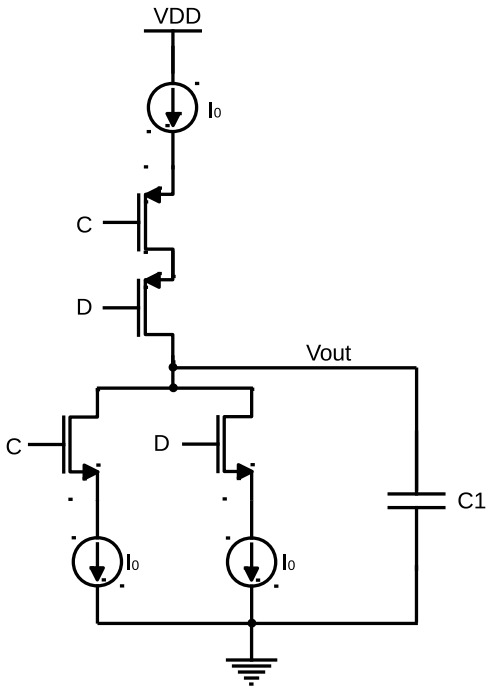


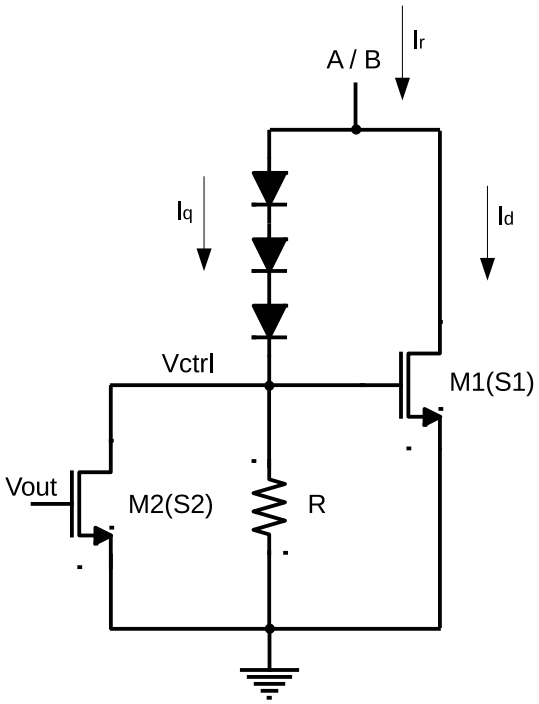
Figure 3.19: Proposed Control Logic with Charge Pump circuit



3.4.2 RF clamp optimization

The RF clamp schematic and the switch (M1) that is controlled by the power detector is show in 3.20. To simplify the analysis, the circuit is not shown in a differential form.

Figure 3.20: RF Clamp circuit



The current drained by the RF Clamp is I_r, which is composed of the current I_q and by the current I_d. I_q passes through the diodes and the resistance R, increasing the voltage $Vctrl$ that triggers I_d when $Vctrl$ voltage is higher than the transistor voltage threshold.

$M1$ is a power device designed to drive enough current so that the overvoltage protection is guaranteed in the high power condition. However, in low power conditions, this transistor operates in the sub-threshold region, and the amount of current drained by $M1$ is significant. On the other way, to decrease I_d changing the impedance made by the parallel between R and $M2$, the transistor size can not be too small since I_q becomes significant when compared to I_d, increasing the total current drained by the RF Clamp. Consequently, $M2$ transistor has an optimum size.

In the low power condition, the antenna voltage does not cross the voltage reference, and the supply voltage saturates the power detector output. The transistor $M2$ is operating in the triode region and its resistance given by Eq. 3.17.

$$R(_{M2})^{-1} = \frac{1}{S_2}\mu_0 C_{OX}(V_{GS_2} - V_t - V_{DS_2}) \tag{3.17}$$

Where V_{GS_2} is the gate to source voltage, V_t is the threshold voltage, μ_0 is the electron mobility for NMOS transistors, C_{ox} is the oxide capacitance, and $S2$ is the transistor size (W/L). The Eq. 3.18 defines R_{eq} which is the equivalent resistance defined by the parallel resistor R and the M2 output resistance.

$$R_{eq} = R||R(_{M2}) \tag{3.18}$$

M1 gate to bulk voltage V_{GB_1} can be defined in two different ways by Eq. 3.19 and Eq. 3.20.

$$V_{GB_1} = V_p - 3V_D = V_p - \frac{3KT}{q} ln \frac{I_q}{Is} \tag{3.19}$$

$$V_{GB_1} = R_{eq} I_q \tag{3.20}$$

Where V_p is the antenna voltage, V_D is the diode barrier voltage, K is the Boltzmann constant, T is the temperature, q is the electron charge, and I_s is the saturation current. Eq. 3.21 is obtained substituting Eq. 3.20 in Eq. 3.19. Assuming constant antenna voltage in a steady-state and a scenario of low field condition, the relation between I_q and the M2 transistor size can be found, by R_{eq} in the Eq. 3.17 and Eq. 3.21.

$$R_{eq} I_q - \frac{3KT}{q} ln \frac{I_q}{Is} - V_p = 0 \tag{3.21}$$

Transistor M1 is operating in sub-threshold region and the current I_d is defined as Eq. 3.22 and Eq. 3.23, according to SCHNEIDER; GALUP-MONTORO (2010).

$$I_d = I_0 \varepsilon^{\frac{V_{GB} - V_t}{n\phi_t}} \tag{3.22}$$

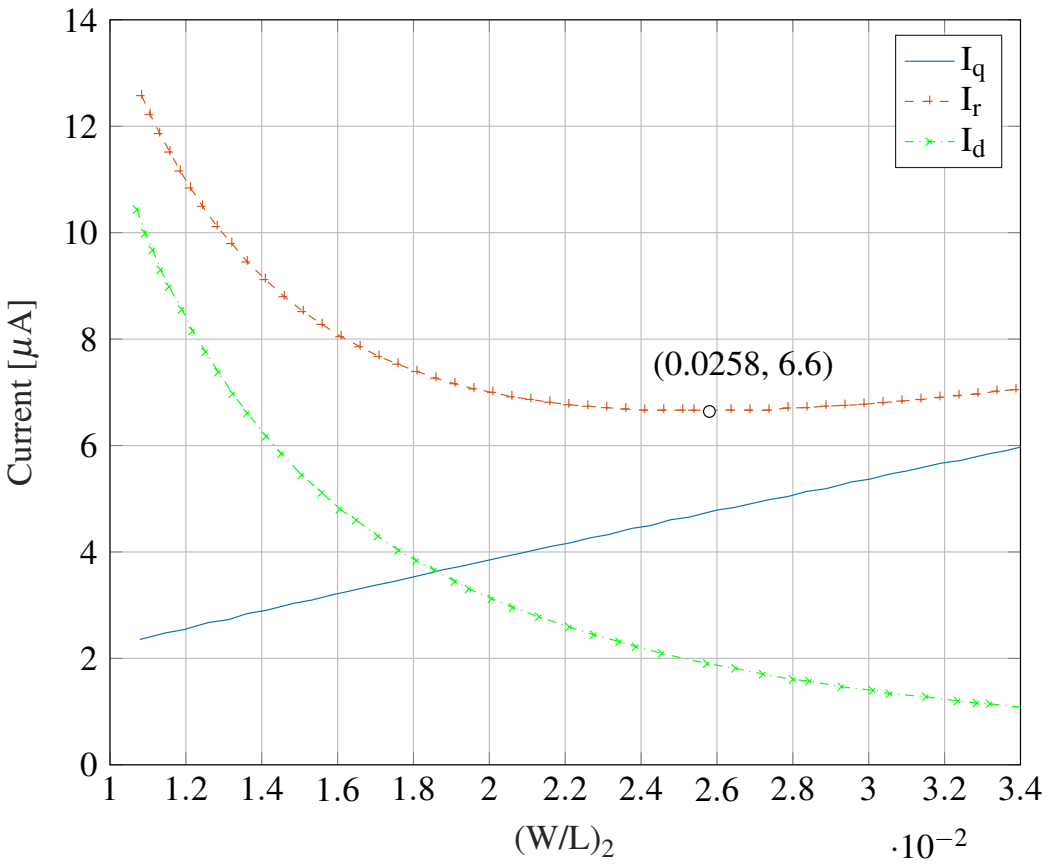
$$I_0 = \mu_0 C_{0X} S_1 \phi_t \varepsilon^1 \tag{3.23}$$

where V_{GB} is the gate to bulk voltage, V_t is the threshold voltage, n is the slope factor, ϕ_t is the thermal voltage and $S1$ is the M1 transistor size (W/L). Substituting Eq. 3.22 in Eq. 3.21, it can be found the current I_d in terms of M2 transistor size Eq. 3.24.

$$I_d = I_0 \varepsilon^{\frac{I_q R_{eq} - V_t}{n\phi_t}} \tag{3.24}$$

Figure 3.21 shows the three currents I_r, I_q and I_d as a function of the $M2$ transistor size. It can be observed that the diode current I_q increases and the transistor current I_d decreases with the transistor size $M2$. The $M2$ optimum size is defined by I_r minimum.

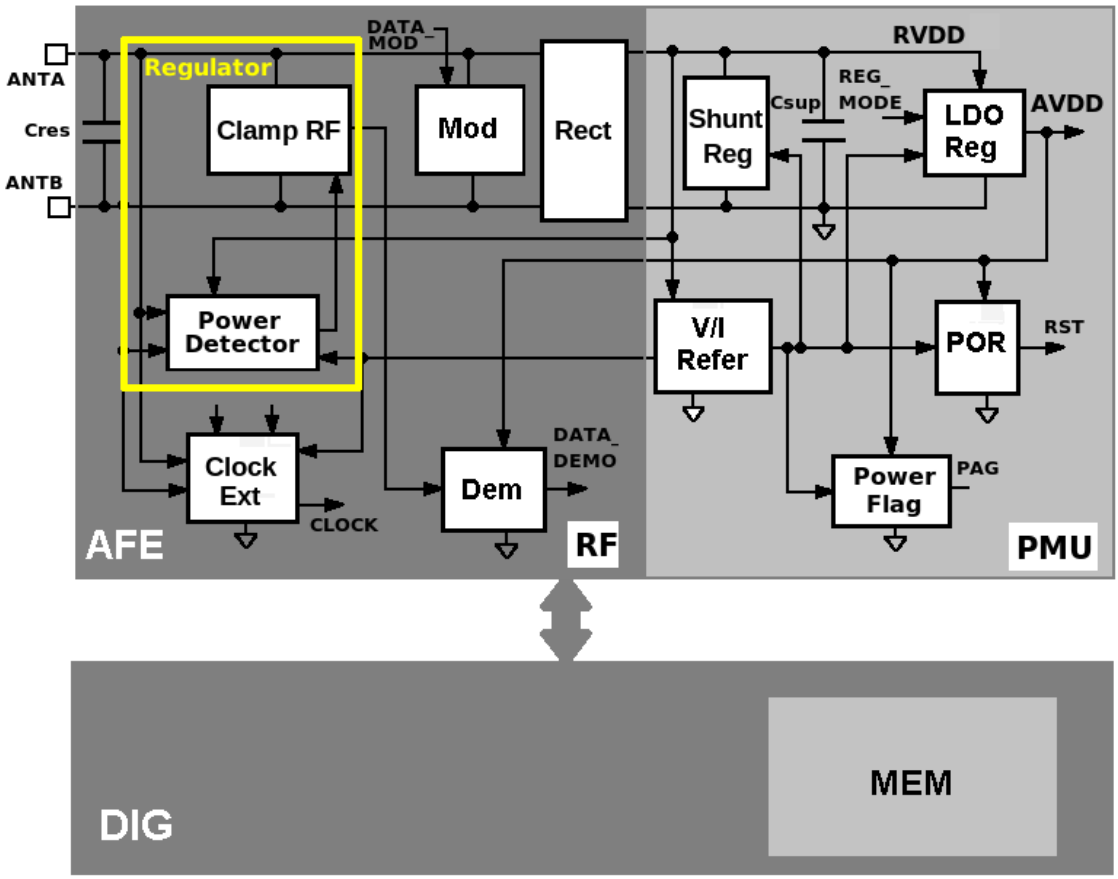
Figure 3.21: RF Clamp currents vs M2 size



4 THE NON-LINEAR SHUNT REGULATOR APPLIED TO LF RFID TRANSPONDER

The non-linear shunt regulator is part of the LF RFID transponder system implemented in (CORTES et al., 2014). The regulator highlighted in Figure 4.1, composed by the RF clamp and the power detector, is connected to the antenna pins, where the power detector stage monitors the available power, providing a feedback signal that adjusts the RF clamp stage accordingly, as depicted in Figure 4.1.

Figure 4.1: Analog front-end architecture of the LF RFID transponder



Source: (CORTES et al., 2014).

Figure 4.1 also shows the whole AFE, the rectifier converters the energy stored in the LC tank in a DC voltage supplying the circuitry. The voltage regulation is provided by the RF Clamp connected to the antenna, which defines the antenna voltage, the shunt regulator

connected to the rectifier output sets the analog supply domain RVDD and the series regulator sets digital supply domain AVDD. The objective of having two supply domains, RVDD for analog and AVDD for digital circuits, is to reduce the power consumption of the system by connecting the digital circuitry in a lower supply domain since their power consumption is proportional to the power supply value (CV^2). A voltage reference is used for the regulators to define RVDD, AVDD and also to be used in voltage detectors as the POR which reset the circuitry when the AVDD supply voltage goes below to the minimum acceptable voltage by the digital standard cells. The clock extractor extracts the system clock signal from the carrier frequency 134 KHz. Finally, the modulator and the demodulator are responsible for communication, and exchanging data between the reader and the transponder.

The RVDD is the voltage reference used by the power detector to track the highest value of the system's antenna voltage, adjusting the RF clamp via the power detector feedback loop. The rectifier transfers the power spent in the RF clamp to RVDD, boosting transponder sensitivity.

The rectifier employed is a voltage doubler, also known as a charge pump, in order to extract as much power as possible under low power conditions when the antenna voltage is the lowest and less than the RVDD. In high power conditions, however, the RF clamp and shunt regulator maintains the antenna voltage and RVDD at the same level, dissipating extra energy in the system.

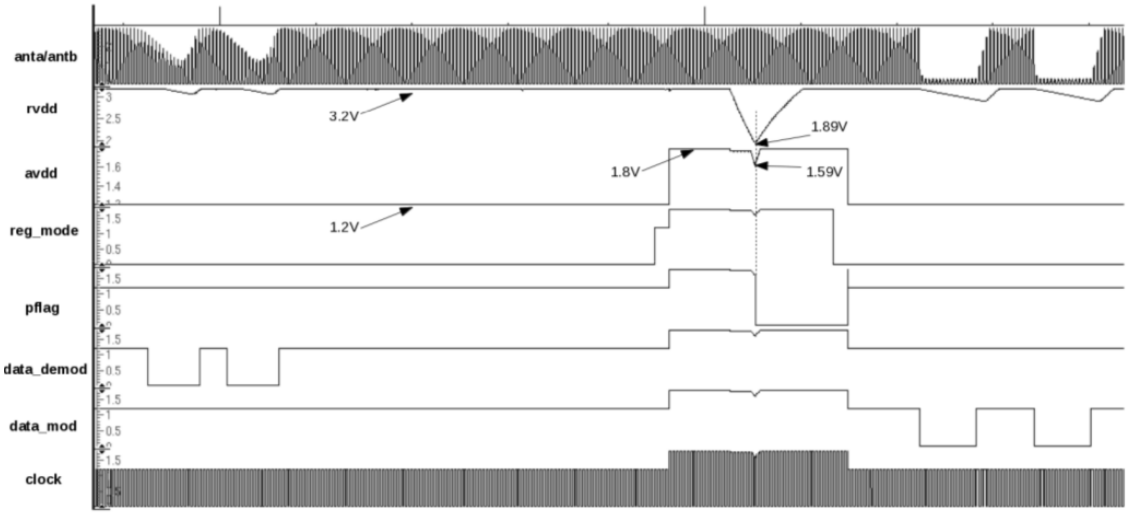
4.1 Simulation Results

System-level simulations were performed using verilogA and VerilogAMS models to validate and characterize the proposed AFE architecture. All building blocks, together with the RF air link and antenna interface modeled using digital and electrical signals with a high abstraction level. Figure 4.2 shows the simulation of the main functionalities of the AFE system. After power-up, the charge pump starts to generate the voltage (RVDD) that will supply the system while the voltage/current reference block provides the signals for both regulators (VREF = 400 mV): the shunt regulator keeps the rectified voltage at 3.2 V, and the series regulator that provides the analog stable low supply (AVDD) at 1.2 V. Then, an ASK modulated signal is received by the AFE system and demodulated into a digital signal (DATA_DEMOD).

The communication process starts with a "write event", the regulated supply AVDD is set to 1.8 V (REG_MODE) intentionally due to the memory specification. A high load is connected to the system, emulating a memory power consumption due to the writing process. Since the available power is low (set in the model), both analog regulated voltages drop until the pflag circuit flags (PFLAG) when AVDD reaches the 1.6 V trip-point, the minimum voltage required to maintain the write event. As soon as this occurs, the high load is removed, and the system set to regular regulation mode (AVDD = 1.2 V). Finally, a "read event" is emulated, where digital data of 4 kHz is applied in the modulator input (DATA_MOD). It results in a perturbation of the magnetic field that supplies energy to the system, which translates into a drop in the RVDD voltage. The integrated supply capacitor of 1.5 nF maintains the RVDD voltage above the minimum supply required of the system to work under low field conditions.

The complete system was validated through electrical simulations and a test prototype. High and low field conditions were applied, where a "read event" is emulated. In order to show the effect of the feedback loop in the system, the complete system was sim-

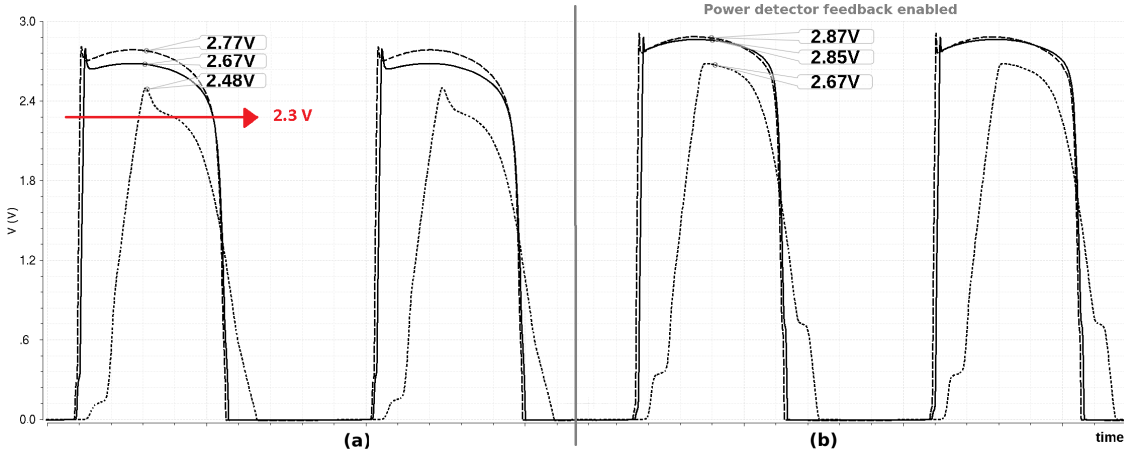
Figure 4.2: Proposed AFE high level system simulation



Source: (CORTES et al., 2014).

ulated with and without the control loop. Figure 4.3 shows the antenna voltage at three different power levels before (a) and after (b) the RF power sensing system is enabled. The antenna voltage variation is decreased in part (b) due to the high gain of the feedback loop composed by the power detector (2.67 V to 2.87 V). It is not only the peak voltage but also the shape of the sinusoidal waveform changes compared (parts a and b). The low peak voltage of 2.48 V can even be considered as 2.3 V to be fair compared to the two states. The small peak of 2.48 V is due to the delay of the RF clamp loop that does not happen in part (b) because the resistance connected to the gate is lower in this scenario.

Figure 4.3: Analog front-end architecture of the LF RFID transponder

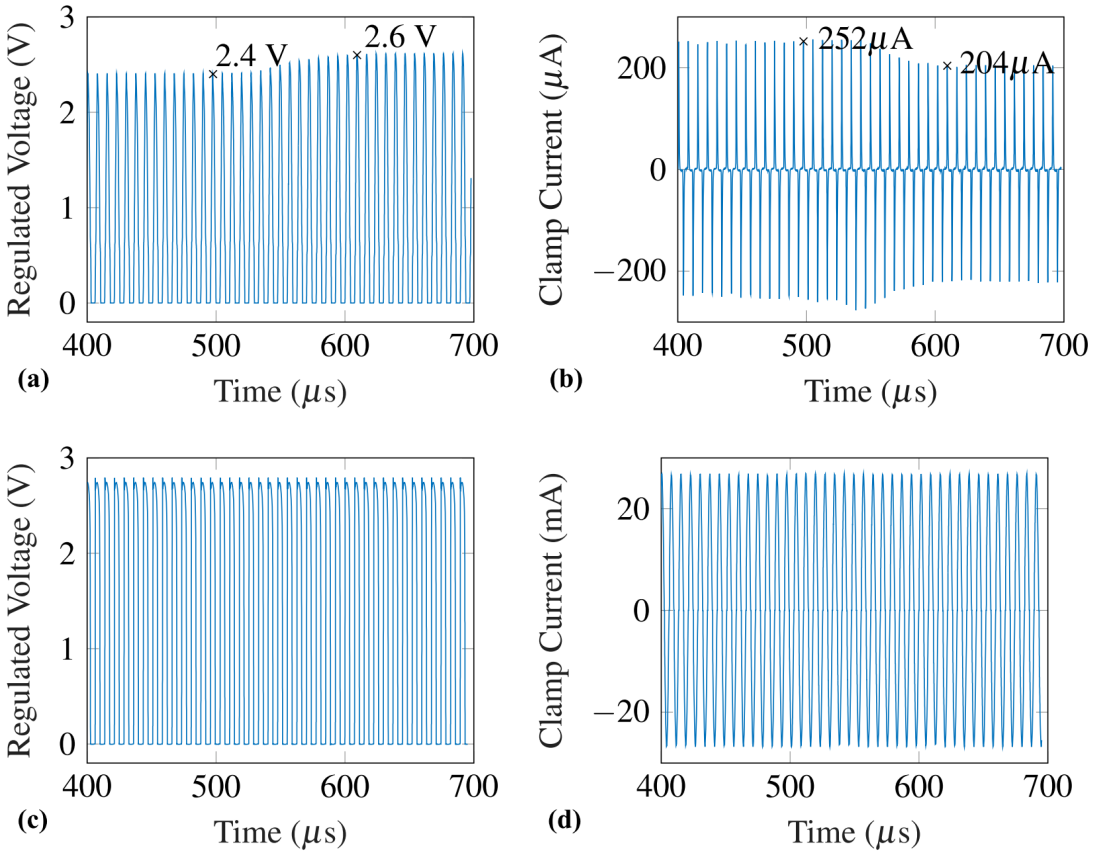


Source: (CORTES et al., 2014).

To verify the impact of the two-loop strategy on the voltage regulation, the transponder was simulated under low-power (k=400x10^{-6}) and high-power (k=100x10^{-3}) conditions. During the simulations, the power detector was activated at 500 μs. Figure 4.4(a) and 4.4(b) illustrate when the power detector is activated, the regulation improves, and less current is dissipated in the clamp. This stored power is utilized by the transponder's internal circuits and contributes to its reading distance.

In the high power condition, Figures 4.4(c) and 4.4(d), the voltage regulation and the clamp operation are not affected

Figure 4.4: Effect of regulation strategy in low power condition with k=400x10^{-6}: antenna voltage regulation (a), current dissipated in the clamp (b); The effect of regulation strategy in high power condition with k=100x10^{-3}: antenna voltage regulation (c), current dissipated in the clamp (d).



4.2 Measurements Results

The prototyped transponder was tested in a laboratory using the previously described ear tag and reader conditions. Two test settings were created: functional and performance evaluation.

4.2.0.1 Functional test

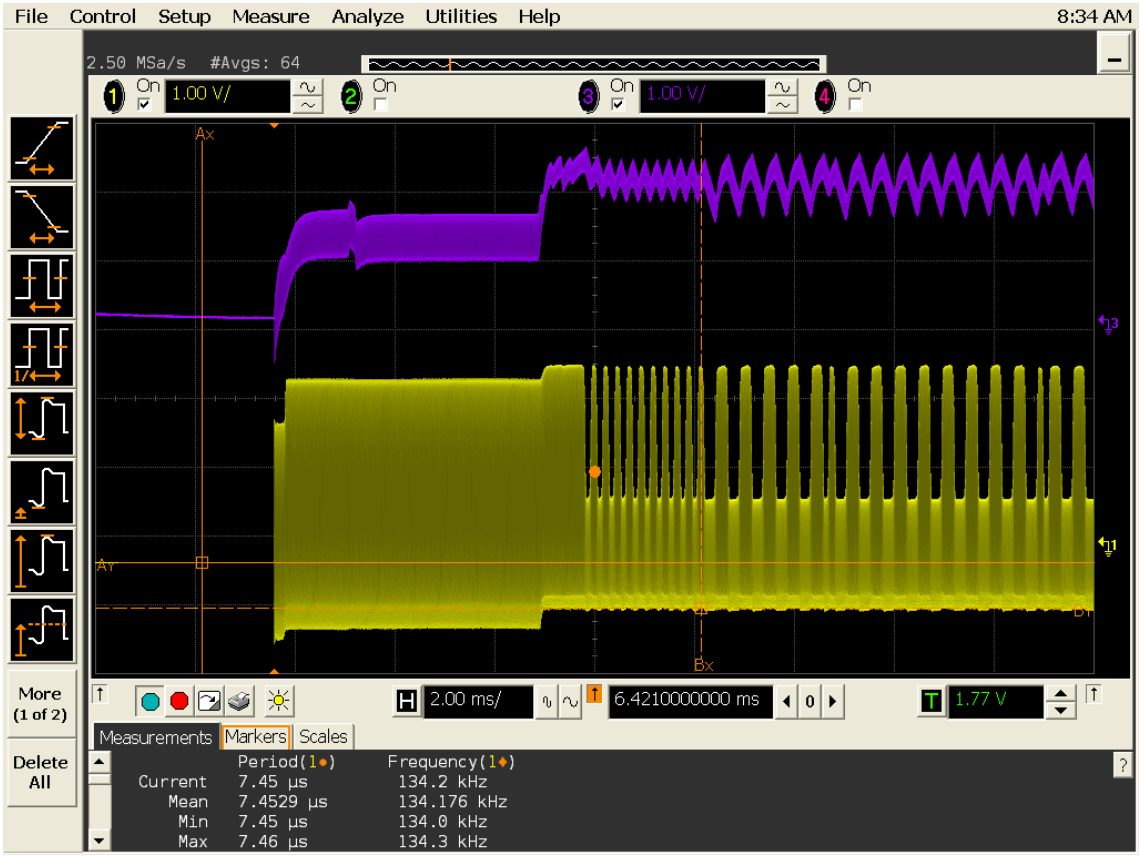
In the functional test setup, a bare die sample was placed in a probe station and connected to the inductor (at the antenna pins via DC probes). Inductor tuning is not required in this case, since the goal is to analyze the functionality of the system.

The portable reader is then moved close to the inductor to activate the transponder, and the antenna and supply voltages are measured using DC probes and an oscilloscope. Figure 4.5 shows the waveforms of the antenna (ANTA/ANTB) and the generated high supply voltage (RVDD). When the “reading event” (TX) occurs, the transponder sends data using ASK 100% modulation, resulting in a magnetic field perturbation. The energy stored in the LC tank is transferred to the supply capacitor, which powers the circuits

while keeping the RVDD voltage over the minimum necessary for the system under low field conditions.

When the regulator begins to work, the antenna voltage increases (the available power at the antenna increases), resulting in a larger RVDD. The rise in supply voltage determines the reading distance increasing. During a "reading event," more energy is stored in the supply capacitor to keep the RVDD above its minimum voltage in the absence of an RF field.

Figure 4.5: Measured signals (ANTA/ANTB and RVDD) during transmission mode performance optimization with new shunt regulator.



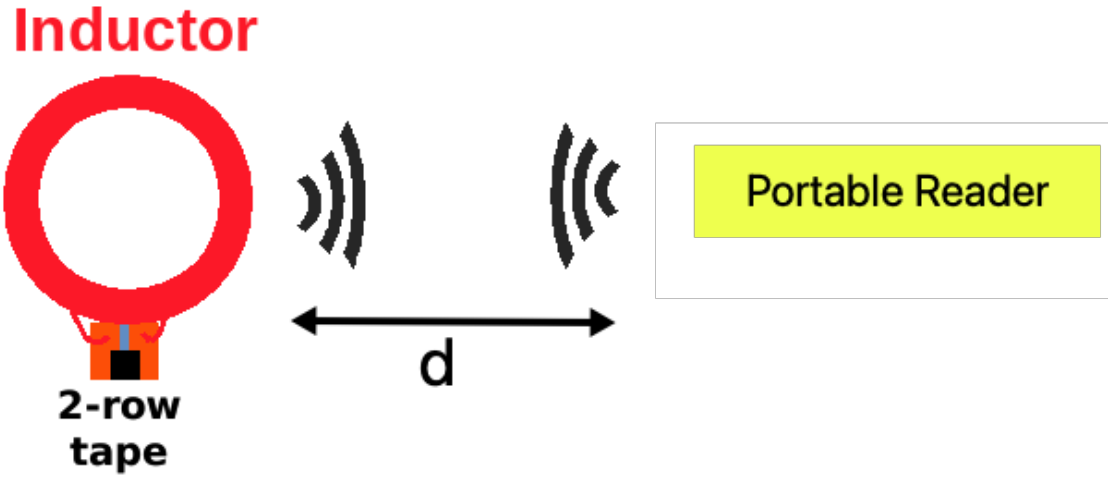
4.2.0.2 *Performance test*

In the performance test setup, the packaged die (2-row tape) was mounted with an inductor tuned to the resonating frequency (around 134 kHz) and placed near the portable reader, as shown in Figure 4.6. When the reader is enabled, it must "read" data already saved at the prototype. The technique is repeated for different distances until it stops "reading", reaching the best read performance.

Manual tuning is used to reach the greatest reading distance by adjusting the number of rotations on the antenna. The sensitivity curve of one sample tested in the antenna tuning procedure is represented in Figure 4.7. Five antenna units were tuned to be used with 50 packaged die samples.

The maximum reading distance was then measured for two different transponder configurations (50 samples): with and without the two-loop regulator activated. The power detector is disabled in the last configuration and corresponds to the traditional strategy, using only the Clamp circuit. The measured maximum reading distance increased from

Figure 4.6: Test setup for measuring the transponder performance.



30 cm to 35 cm with the use of the proposed two-loop regulator, resulting in 16.7 % improvement in the reading distance.

Table 4.1 compares the fully implemented chip with similar commercial applications from different manufacturers identified from A to D, and a published work (ZURIARRAIN et al., 2018). Manufacturer A was also measured as a benchmark and reaches same distance as this work, though with a special fabrication process to achieve 6 V (peak) at the input, enabling the IC to store more power for the read process. Besides, A, B, and C implement a low tolerance resonance capacitor for proper transponder tuning. The whole Chip functionality was characterized in a low temperature range compared to the competitor due to the market destination.

Figure 4.7: Sensitivity vs frequency of one antenna - tuning process.

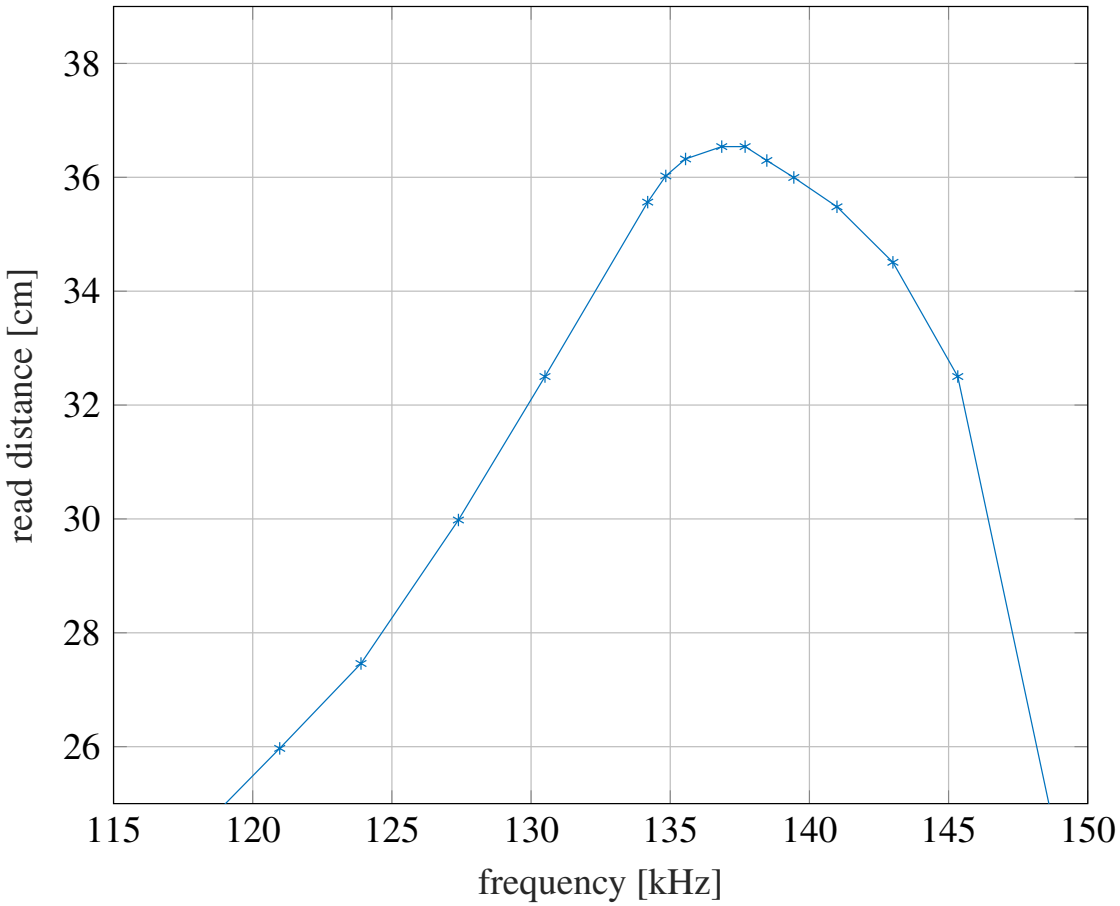


Table 4.1: Comparison of Commercial and Published Transponder Applications.

Manufacturer	This Work	A[1]	B	C	D	(ZURIARRAIN et al., 2018)
Op. freq. (KHz)	100 - 150	100 - 150	100 - 150	100 - 150	100 - 150	124 - 134
Res. Cap. (pF)	210 / 280	210 / 280	210 / 250	250 / 330	75	External cap.
Cap. tol. error	10 %	3% / 5%	3%	3%	-	-
Memory (EEPROM)	256-bit MTP	128-bit 512-bit 1760-bit	512-bit	128-bit	1056-bit	-
Standards	ISO 11784/85 ISO 14223 (RTF)	ISO 11784/85 ISO 14223	ISO 11784/85 ISO 14223	ISO 11784/85	ISO 11784/85	ISO 11784/85 ISO 14223
Communication scheme	FDX-B	FDX-B	FDX-B	FDX-B	FDX-B	HDX
Protocol	TTF/RTF, CRC, 48-bit UID	TTF/RTF, CRC, 48-bit UID	RTF, CRC, 32-bit UID	ITF/TTF, CRC, 32-bit UID	64-bit UID	-
Dist. max. (cm)	35 (2)	35 (2)	-	-	-	-
Electrical characteristics at antenna	2 – 3.6 V ±30 mA (max)	4 – 6 V ±10 mA (max)	9.1 V (max) ±10 mA (max)	8.5 V (max) ±20 mA (max)	-	3 – 6 V
I_{disp} (μA)	4.5	-	-	2	5	< 5 (3)
Temp. range (°C)	-20 to +85	-40 to +85	-40 to +85	-40 to +85	-40 to +85	-20 to +80
Die area (μm x μm)	870 x 870	550 x 550	866 x 818	946 x 966	910 x 1250	900 x 900
Technology	CMOS 0.18 μm	CMOS 0.14 μm	-	-	-	CMOS 90 nm

[1] Requires customized fabrication process to enable low tolerance error capacitors and high input voltage.
[2] Reference reader (ALLFLEX, 2006) was used to measure the performance of the chips.
[3] Includes only the analog part of the circuit.

4.3 Power detector characterization

The power detector block can be used to estimate the RF power incoming in an open-loop measurement, as explained in Chapter 4 through the equations and simulation results. The power detector block, on the other hand, was built as part of the shunt regulator solution, into the feedback loop as indicated. Unfortunately, any isolated sample of the circuit in a standalone test structure was envisioned. However, special routing and metal tweak techniques were applied in the chip to increase test covering. In the case of the power detector block, it is possible to disable it, change its performance, or even open the regulator loop. These modifications are feasible using a laser cut, as illustrated in the setup measurement in Figure 4.8. The cut was made at the power detector output net in order to probe and measure it.

Figure 4.8: Measurement setup in the probe station

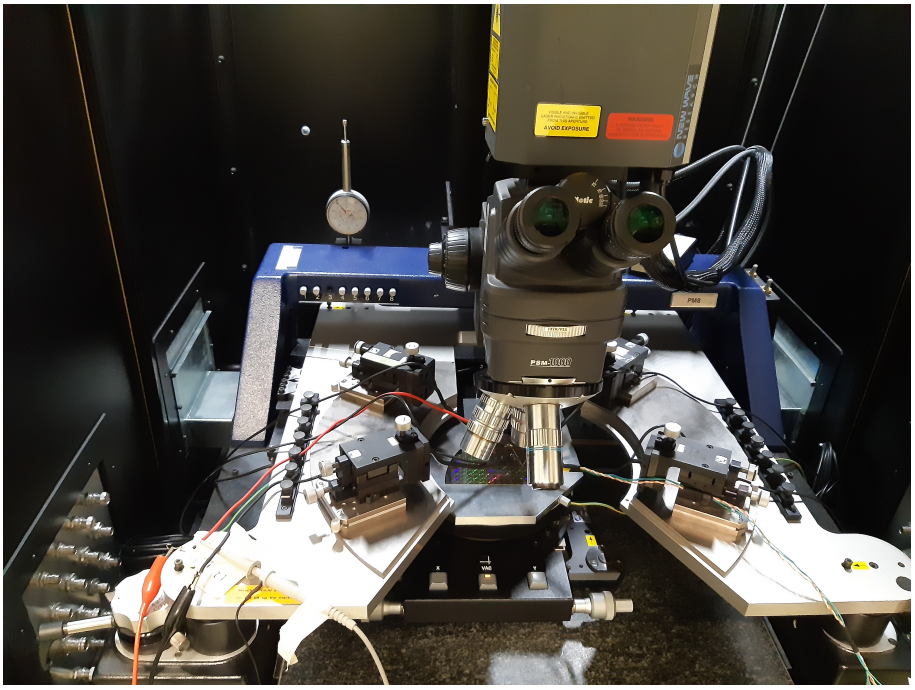
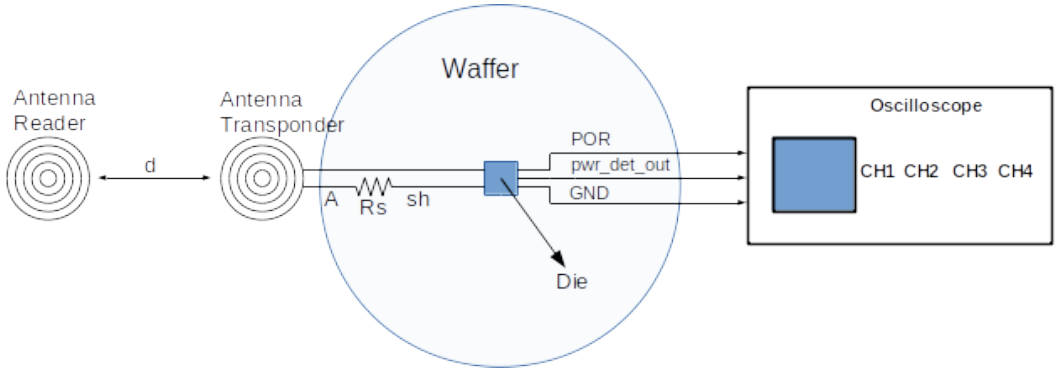


Figure 4.9 shows an illustration of the setup measurement for better understanding. It is composed of the reader and transponder's antennas separated by a distance (d) that modulates the level of power incoming in the transponder. The Die is a sample of the transponder circuit in a whole Waffer. The signals to be measured are the power detector output (pwr_det_out) and the power incoming made by a differential measure in the small resistor Rs, measuring the current in the antenna's transponder. The POR signal enables the systems and it is used to trigger the measurement of the power detector output defined in 3.4. The ground signal (GND) is the reference of the measurements.

Figure 4.10 shows the picture of the entire Chip. The bright parts on the Chip are the top metal. Some digital signals are buffered by digital buffers and observable in the digital PADs on the right side of the Chip. Some analog signals are visible by micro pads, which spread on the Chip located close to analog blocks. A green box highlights the shunt regulator area which is $130 \times 230\,\mu m^2$. A micro pad inside the green box is intended to measure the power detector output.

Figure 4.11 shows the microscope image of the place where the cut is made on the chip to open the loop and make the measurements. Figure 4.12 shows the antenna voltage

Figure 4.9: Measurement setup



after the loop was opened. The antenna voltage stays at the same level after the power detector is enable validating the cut.

Figure 4.13 shows the timing diagram of the transponder response with two signals, the antenna voltage (A) and the power detector output. The maximum power-up time (T1) of the system is 1.2 ms. The POR signal enables the internal blocks during this period, then the transponder waits for the reader to send commands in advance mode during T2 equal to 1.73 ms, and then the transponder enables the power detector block and begins to send a command to the reader after T3 with its maximum value defined by 0.7 ms. Transponder responses are made up of symbols (’0’s and ’1’s) encoded by Differential Bi-Phase (DBP) during the T4.

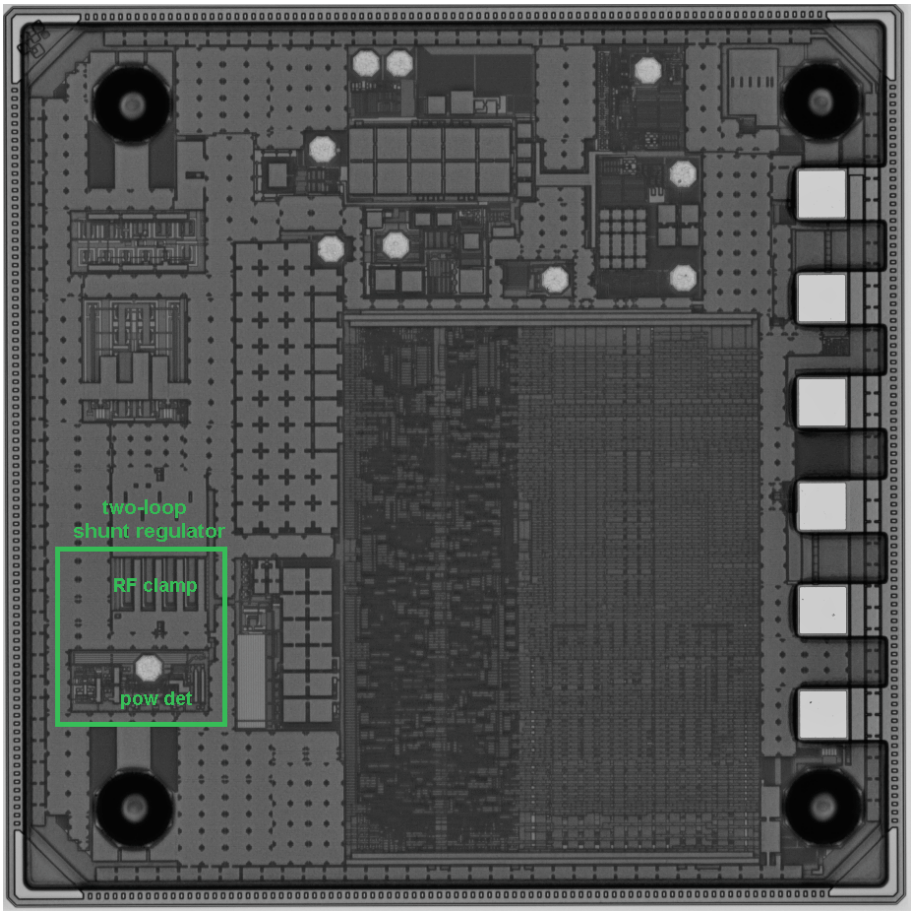
In the disabled state, the power detector signal is set to ground. After enabling, it begins the integration, with its output relying on the antenna voltage value, and the power detector output assuming a value between ground and RVDD after n defined in Eq. 3.3 and previously shown in Figure 3.10. It planned to sample the power detector output before T3. Due to the general oscilloscope’s low input impedance when compared to the power detector output, a buffer was planned to allow the measurement.

The power characterization is affected by the comparator’s architecture. When it compares the measurement results to the simulation results using verilogA model, shown in 3.10. The schematic implementation is based on a common gate, which results in reduced power consumption as compared to the traditional Operational Transconductance Amplifier (OTA). However, it generates different values of rising and falling time, distorting the PWM signal and introducing non-linearity when switching the current sources. As a result, the power detector discharges its output faster than it charges, opening the feedback loop faster for a high field fluctuation, which is ideal from a protection standpoint. Another interesting finding during the experiments was that the lowest input capacitance buffer available has 10 pF (TL081), which is ten times larger than the charge pump’s filter capacitor, resulting in a sampling time of 907.5 us, which is longer than the maximum T3 time.

In light of these concerns, a qualitative evaluation of the power detector was chosen over its characterization. In Figures 4.14, 4.15 and 4.16 show the power detector output in an open loop measurement for three different distances from the reader to the transponder or field condition: low field (4.14), medium field (4.15) and high field (4.16). Because the power detector output is inversely proportional to the antenna voltage, the integration time is better visible under low field conditions during T3.

As predicted, the power detector signal decreases as the field increases. The ripple in the power detector output is caused by the modulator altering the chip impedance after T3

Figure 4.10: Chip picture



time, modulating the baseband signal, and changing the antenna voltage state at a lower frequency due to the symbol characteristic. Even with the modulation signal presented in T4 period, the power detector still works as expected, its output produces information of the average power incoming into the chip if it compares Figure 4.14 and Figure 4.16, due to the PWM signal produces by the antenna voltage has a higher duty cycle in low field condition.

Figure 4.11: Laser cut picture

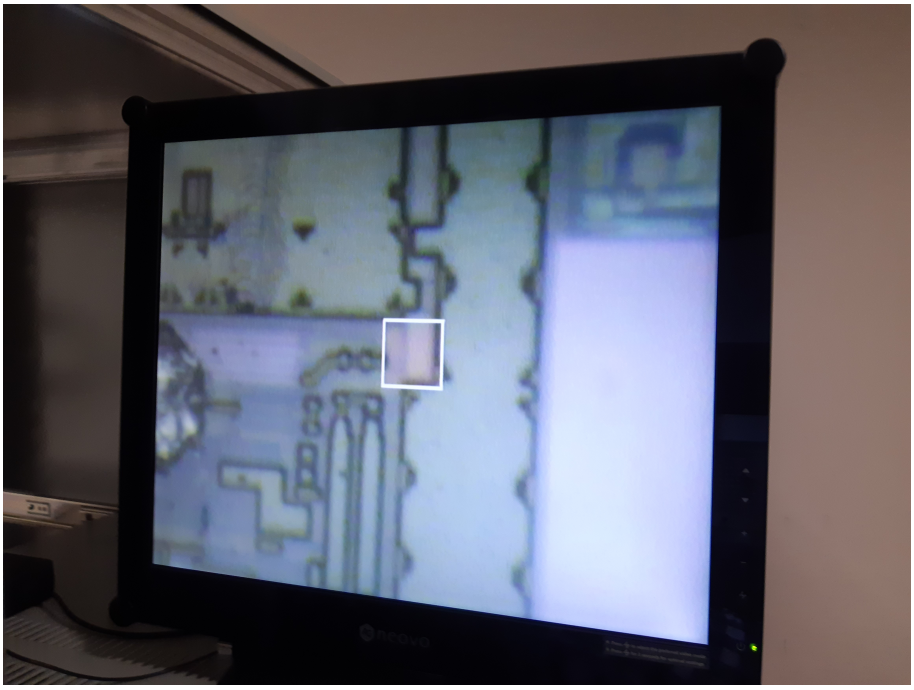


Figure 4.12: Antenna voltage after the loop was broken

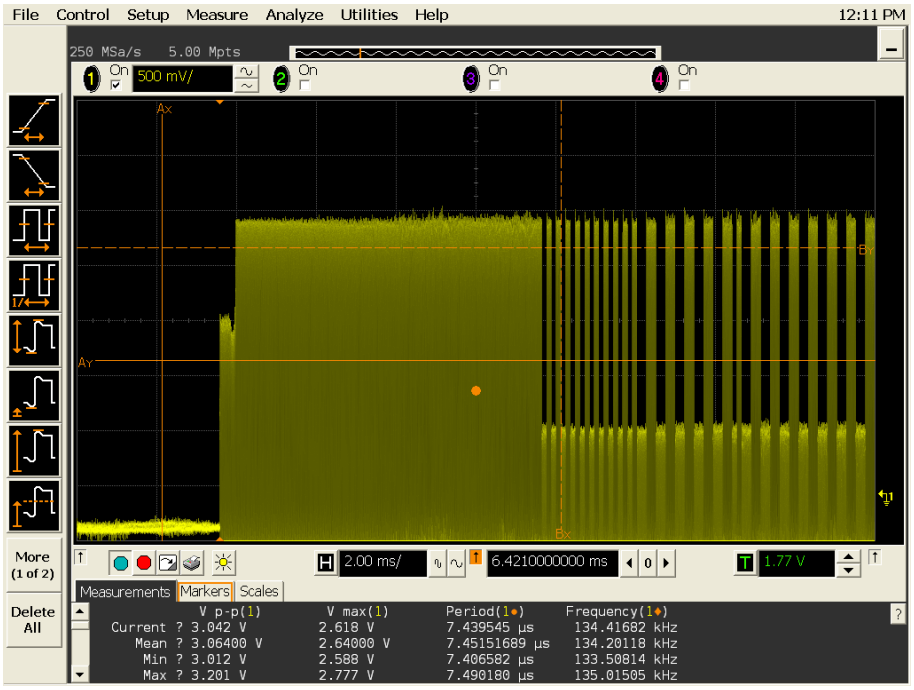


Figure 4.13: Antenna voltage and power detector time diagram

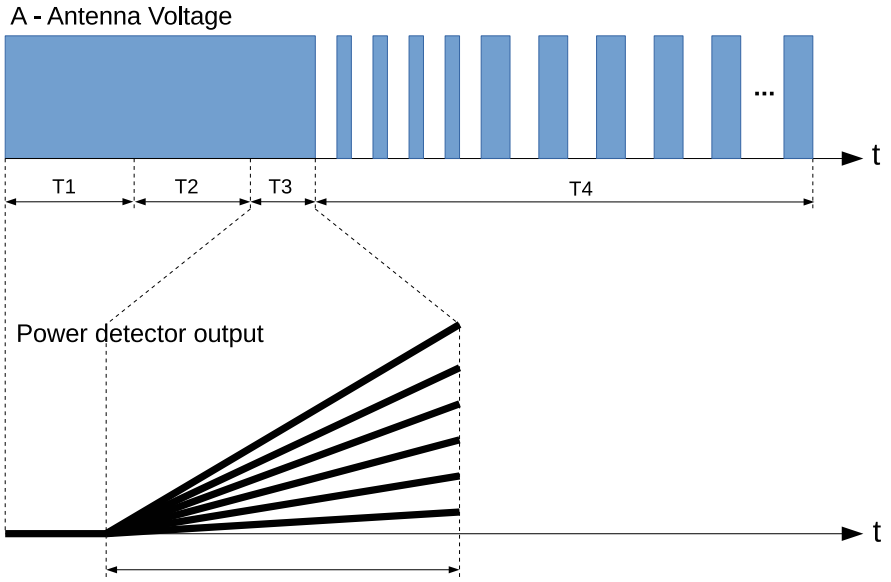


Figure 4.14: Power detector's output measurement (low field condition)

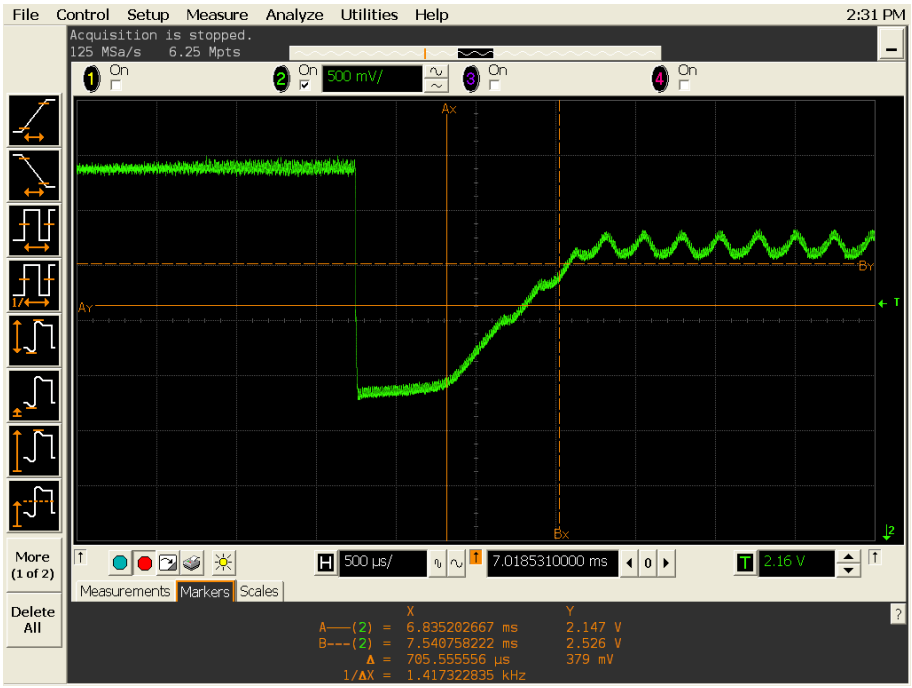


Figure 4.15: Power detector's output measurement (medium field condition)

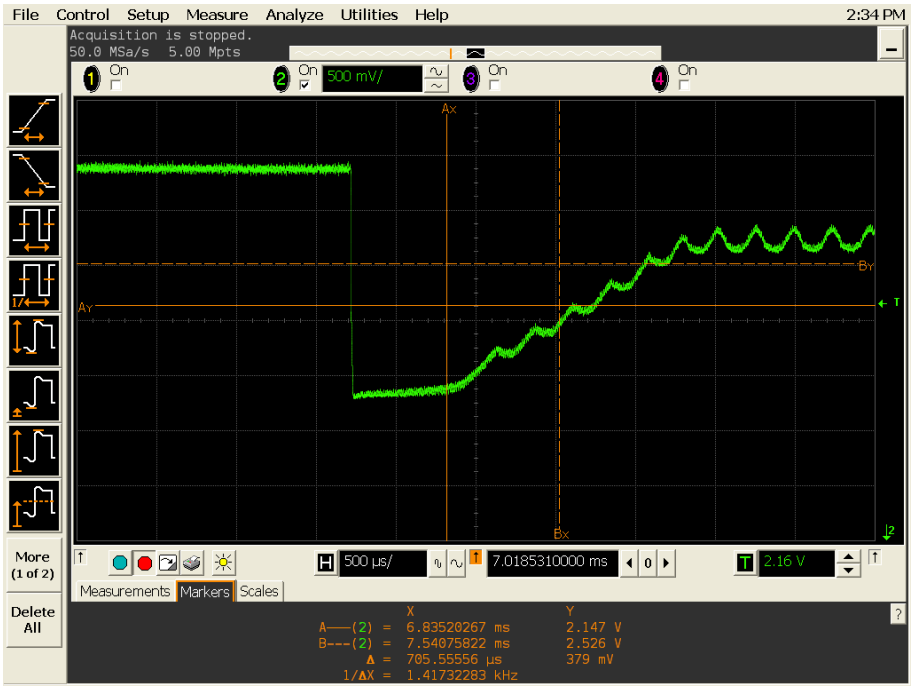
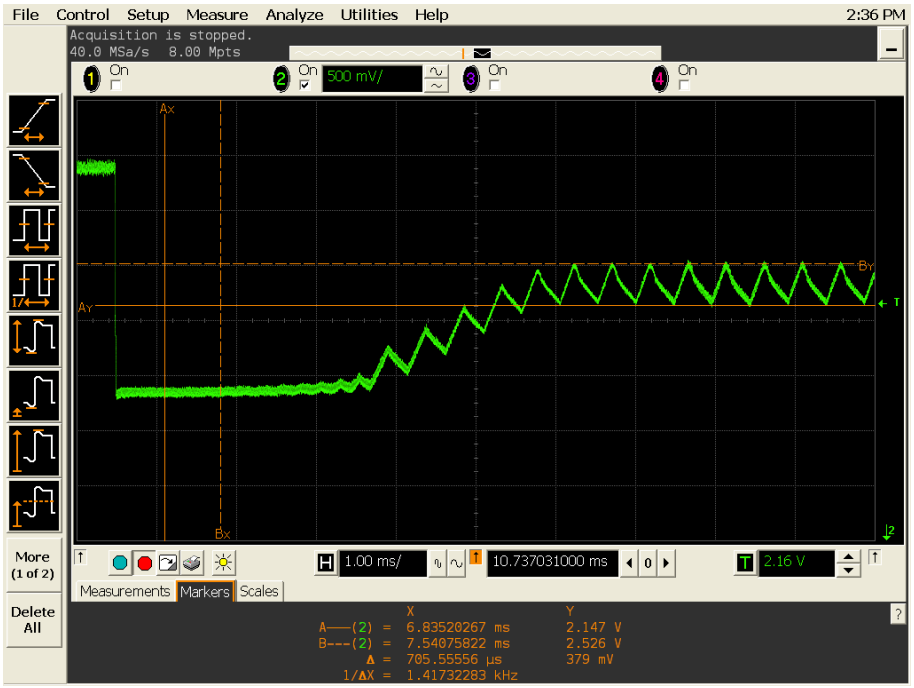


Figure 4.16: Power detector's output measurement (high field condition)



5 CONCLUSION

This work presented the development of a two-loop shunt regulator designed to optimize the distance/power performance of an RFID tag system. In the proposed architecture, the performance is improved by reducing unnecessary power dissipation in the clamping circuit when the RFID transponder is in low RF input power condition, at the maximum distance from the reader. It also preserves its clamping effectiveness when the transponder is in high input power condition (short distance). A PWM power detector composes the second loop, which measures the input power condition and modulates the clamping circuit action, improving efficiency when in low RF power. The complete regulator design was detailed and validated through behavioral and electrical simulations. Implemented in a 180 nm standard CMOS process, the proposed regulator architecture was used in a commercial LF (134 kHz) RFID transponder system. The transponder was prototyped over $870 \times 870\,\mu m^2$ of silicon area, including the resonant and supply capacitors, and $130 \times 230\,\mu m^2$ is the regulator circuit area. The analog and digital functional blocks of the RFID system, including the PWM power detector, consume around $4.5\,\mu W$. An improvement of 16.7 % in the measured reading distance was observed with the proposed shunt regulator enabled.

Measurement results validate the functionality of the two feedback loop shunt regulator on LF RFID transponder and also the isolated power detector block in open loop. The strategy presented to measure RF input power can be extended to other types of communication systems that require power estimation. However, higher operating frequencies will demand faster analog processing and increased power consumption.

6 FUTURE WORK

The analysis from the presented version of the shunt regulator and power detector provided information for future versions:

- To characterize the power detector block, a low input capacitance buffer must be use to measure the power detector output within the T3 interval. Also, new simulation results using the comparator schematic implemented instead of VerilogA model to be fair on the analysis of the measurement results.
- A standalone implementation of the power detector using a comparator with identical rise and fall time in order to remove the non-linearities presented on the present implementation.
- A new version of the shunt regulator using comparators with identical rise and fall time in order to measure the new regulator step response and compare it with the simulation results.

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LIST OF PUBLICATIONS

- IEEE RFID 2020: Non-Linear Shunt Regulator With RF Power Detector for RFID Applications.
- IEEE Journal of Radio Frequency Identification: Two-Feedback Loop Shunt Regulator Based on PWM RF Power Detector Aiming RFID Applications.

APPENDIX

6.1 Magnetic link

The magnetic link between two inductors is defined by the mutual inductance M defined in 6.1.

$$M = \sqrt{L1L2} \tag{6.1}$$

In equation 6.2, the coupling factor k is defined as the ratio of total magnetic flux between the coils to flux leakage.

The equation 6.1 assumes no flux leakage and total magnetic coupling between the two coils, L1 and L2. In fact, there will always be some loss due to leakage and position. The magnetic coupling between the two coils will never be 100%. Still, it can approach this number for some special inductive coils or it can be extremely small when they are weakly coupled, as in RFID systems, where the coupling factor drops with distance.

The ratio between the total magnetic flux between the coils and the flux leakage defines the coupling factor k in the equation 6.2.

$$k = \frac{M}{\sqrt{L1L2}} \tag{6.2}$$

The coupling factor can be calculated after measurements with the setup shown in Figure 6.1. The antenna voltage over the coil inductors is measured with an oscilloscope with coils inductances known. Figure 6.2 shows the coupling factor's measurement results in terms of the distance between the reader and the transponder.

Figure 6.1: k measurements setup PARET (2005)

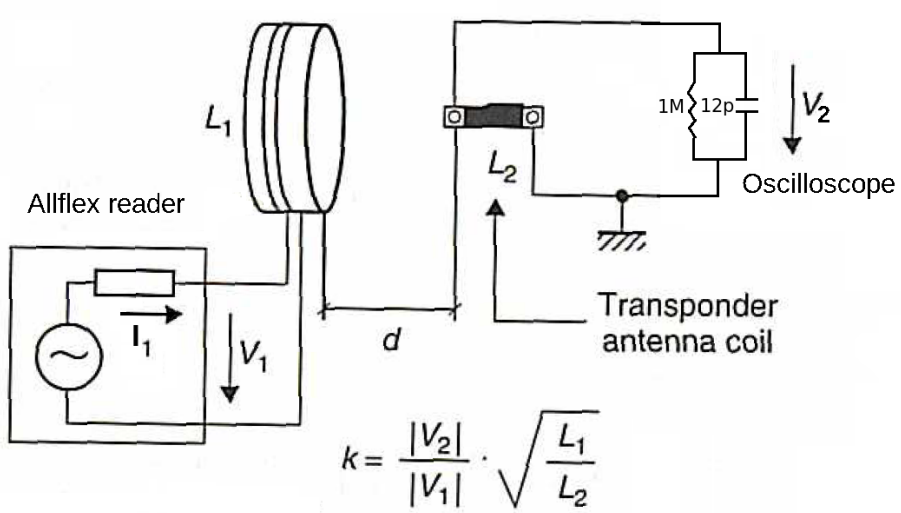

Figure 6.2: k measurements results