Space Shuttle: A Test Vehicle for the Reliability of the SkyWater 130nm PDK for Future Space Processors

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***Abstract*—Recently the ASIC industry experiences a massive change with more and more small and medium businesses entering the custom ASIC development. This trend is fueled by the recent open hardware movement and relevant government and privately funded initiatives. These new developments can open new opportunities in the space sector – which is traditionally characterised by very low volumes and very high non-recurrent (NRE) costs – if we can show that the produced chips have favourable radiation properties. In this paper, we describe the design and tape-out of Space Shuttle, the first test chip for the evaluation of the suitability of the SkyWater 130nm PDK and the OpenLane EDA toolchain using the Google/E-fabless shuttle run for future space processors.**

I. Introduction

Until very recently, custom ASICs were very rare for small and medium companies due to the overall prohibitive cost of their production, which could only be afforded by few large companies. This high cost comes mainly from the very expensive commercial EDA tools used for chip designs. However, recently there have been government initiatives such as DARPA's OpenLane/OpenROAD which supported the production of a fully open source EDA toolchain from hardware description languages down to GDSII.

This has been followed by private initiatives such as Google's support for an open source PDK in collaboration with SkyWater for their 130nm technology, as well as with e-fabless for the sponsored production of multi-project wafers (MPW) of open source designs to test and further mature the status of these open source EDA elements.

The impact of this completely open source option for hardware designs can reduce the hardware production cost many orders of magnitude, lowering the barriers to entry and enabling the production of innovative designs and prototypes, which was not possible before.

One of the sectors that can benefit the most is aerospace due to its different needs than other domains. Aerospace frequently relies on older technology nodes for fabrication of its processors which are normally reused for decades. When the performance of these processors is not sufficient for a mission requirements, the system is normally supplemented with FPGAs. This drives up the cost of missions due to the inability to apply economy of scale, unlike other safety-critical domains with high volumes such as the automotive.

However, this low volume production creates a perfect match for a new revolution in the space silicon. Therefore, the objective of our work is to validate for the first time this process and its open source tool-chain for space use.

II. Background and Related Work

Space electronics are susceptible to radiation effects such as single event upsets (SEUs) and single event latch-ups (SELs). These radiation effects are well known as well as solutions about how to mitigate them [1][2][3][4]. An example of such mitigation techniques for radiation hardening are the ones applied to the widely used in space LEON3 processor [5] over an FPGA. Such mitigations are focused around single error bit flips. Other techniques [6] focus in time delays in redundant structures in order to prevent the same error to impact them in an identical way. Moreover, these methods use checkpoints in order to restore the correct state when these transient errors are detected but not corrected. A collection of several radiation mitigation methods has been performed as part of the standardization activity of the ECSS space standard and published as part of [7].

III. Space Shuttle

The main goal of our work is to assess the reliability of the SkyWater 130nm manufacturing process and evaluate different reliability mitigation techniques.

In order to do so, we have designed an open source prototype chip called Space Shuttle [8] which has been submitted for tape-out during the second MPW run (MPW2), which is the first shuttle of the program that had working chips.

In order to assess the reliability of the chip we require methods to be able to observe in a detailed way its internal state, so that not only we can identify whether errors (e.g. bitflips) have occurred, but also to know which part of the design has been affected. For this reason, the initial reliability assessment has to be performed in a design with relatively low complexity and therefore, high level of control, with appropriate facilities to collect the required information.

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The most vulnerable parts of a hardware design are its memory structures because they retain their previous values. This is achieved through charge retaining, which makes the circuit more susceptible to a bitflip due to charge that can build up due to radiation [9].

For this reason, in our test chip we have decided to focus on error detection and error correction specifically on flip-flops and registers which are the primary memory storage primitives of any circuit. Therefore, our design is centred around a register file with 32 registers of 32-bit width implemented with flip-flops, since MPW2 lacked a memory compiler, due to the fact that the OpenRAM compiler [10] was considered experimental. However, this allowed us to have more control over the memory structures in order to implement our detection and correction methods.

We have implemented multiple reliability solutions at logic level according to [7], such as different degrees of replication and ECC around this register file, which can be selectively configured and combined with few limitations, in order to reliably detect whether errors occur, and in case they do, whether they can be corrected. Moreover, we designed a redundant Reliability Monitoring Unit consisting of detailed event counters for each of the registers. In this way, we can also assess the protection level offered by these different reliability methods under irradiation and study their trade-offs to guide future space developments on this process.

In particular, our design has implemented the following characteristics:

- A register file with 32 registers, each 32-bit wide, implemented with flip-flops, organised in 8 banks which can be used in parallel. Each register value can be individually set or inspected.
- 4 different protection mechanisms and one non-protected storage mechanism each of which can be enabled selectively and combined with others:
  - Error Correction Code (ECC): ECC with 1 bit correction and 2 bit detection.
  - Triple Redundancy: The input value is triplicated in the register file.
  - Shadow Register: The input value has a copy in the register file similar to [11].
  - ECC Shadow Register: The input value has a copy in the register file with ECC protection of 1 bit correction and 2 bit detection [12].
  - no-protection: The word is stored without protection.
- Duplicated Reliability Monitoring Unit: Individual 32-bit counters per register, reporting the number of write and read operations performed, as well as the number of detected and corrected errors.
- The output of the memory and the result of the verification is sent to the GPIO pins of the chip.

IV. Implementation and Verification Results

The final GDSII uses an area of 2.22 mm^2 with a total of 75841 SkyWater cells targetting a frequency of 100 MHz.

We taped out the design as part of the second e-fabless Google-sponsored shuttle in May 2021 and the chips arrived in February 2023 from Efabless. We got 8 chips pre-mounted in a breakout board, 350 BGA chips, plus a development board.

After the MPW2 submission and early during the manufacturing process, it was discovered that hierarchical timing analysis in OpenLane did not work properly, meaning that most of the parts of the chips have *hold violations*. Because of the late discovery of the issue during manufacturing, only the harness was issued a fix in the mask and the rest of the chip remained unchanged.

Even with this change, when the first chip arrived, it was found that the GPIO configuration shift register still had hold violations. After basic tests performed by Efabless, they recommended the use of 1.60V for the chip, instead of the 1.80V nominal voltage, in order to reduce the effects of hold violation by reducing the response time of the gates.

Knowing these issues, our first step was to classify the 8 chips based on the GPIO working status.

From the eight chips three have issues in basic communication (chips with ID 3,4,8), two have issues with the GPIO in the lower part (IO bits 0 to 18), another two have issues in GPIO in the high part, and the remaining ones have a fully functional GPIO. It is worth noting that our chip has the highest success rate in the GPIO functionality among all MPW2 submissions.

Based on this classification, we selected chips 1, 6 and 7 for testing. Using the IO we run the la-test 1 to 7 testing the basic functionality of storing a value without any protection, storing with ECC, a value stored in a shadow register and in triple redundant mode. All of the tests we performed were successful. Values can be stored and retrieved properly, as well as manual error injections (overwriting protected records in specific patterns) and their corrections.

To our knowledge this is the first attempt to assess the reliability of these open source EDA technologies, as well as among the first academic tape-outs performed within this program. We plan to participate in each MPW with designs of increasing complexity and we believe that our developments will be beneficial not only for the space industry but also to other critical domains like automotive and avionics. The next step will be to perform radiation testing to assess the effectiveness of the methodologies apply in the tapeout.

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