MASTER

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# Optimization of a DAB DC-DC Converter for 50kW DC Charging with a Wide Output Voltage Range

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***Abstract*—The need for fast charging of electric vehicles, combined with the increased battery pack voltage, leads to the need for a high-power DC charger with wide output-voltage range. This paper examines the effect of different design choices on the performance of the isolated DC-DC conversion stage of such charger. Particularly, a comparison is made between a SiC based DAB converter that is optimized for soft-switching and one that is optimized for hard-switching, taking into account a large set of circuit and component parameters. The optimization results reveal that the hard-switching DAB variant resembles the simplest circuit implementation and has the highest overall efficiency. This shows that soft switching does not have to be guaranteed anymore with the use of SiC MOSFETs, and higher efficiencies can be achieved with a reduced number of components.**

## 1. Introduction

With the ever expanding fleet of Electric Vehicles (EV) [1] comes the need for more EV chargers. DC fast charging is an important technology that enables users to charge their vehicles faster than AC charging, making EVs more suitable for longer trips. Extensive research was performed [2] to determine the most meaningful and interesting direction to study. A set of target vehicles was investigated and insight can be gained when looking at the EV battery pack configurations shown in Figure 1. It has been found that most EVs can fast charge with a 500V charger and can utilize over 50kW of DC charging power. Some newer vehicles already use 800V battery systems that need 1000V capable DC chargers. This imposes a challenge, as isolated DC charging is hard to design efficiently over a large output voltage range.

A DC charger for electric vehicles that is connected to the AC grid can consist of two main stages: AC to DC conversion and an isolation stage that controls the DC output voltage or current. A visualisation of these stages is shown in Figure 2. The focus of this project is on the isolated DC-DC stage. A compressed table of the most important operating conditions from preliminary research [2] is shown in Table 1. The input voltage of the DC-DC stage was fixed for all operating conditions in order to make a fair comparison between the design methods. For the DC-DC stage the DAB was chosen because this is a well known topology and can be used for bidirectional power flow, allowing for grid-to-vehicle and vehicle-to-grid energy transfer.

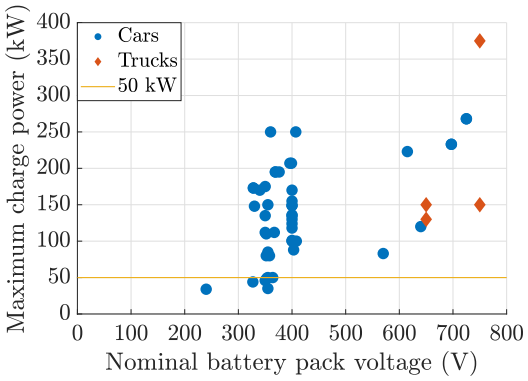


Figure 1. Battery pack maximum charge power in a set of EVs

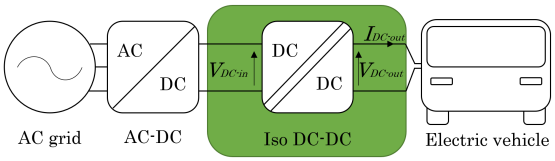


Figure 2. DC charger power conversion stages

A possible solution to achieve a large output voltage range is a modular, dynamically reconfigurable solution that can change between 200-500V and 400-1000V depending on the requested output voltage. A module with an output voltage range of 200-500V can be used in series with another such module to boost the maximum output voltage to 1000V. The configuration will generally not change during a charge cycle because of the clear cut between 400V and 800V battery systems as seen in Figure 1. Relays can be used to set the configuration at the beginning of a charge cycle with minimal losses. The output current characteristics of a six module configuration is shown in Figure 3.

TABLE 1. MAIN OPERATIONAL REQUIREMENTS OF THE DC-DC MODULE

| Parameter | Min | Max | Unit | Remarks |
|---|---|---|---|---|
| $V_{DC-in}$ | 800 | 1000 | $V$ | Fixed input voltage determined by optimization |
| $V_{DC-out}$ | 200 | 500 | $V$ | Half of the system output voltage range |
| $I_{DC-out}$ | 0 | $\frac{150}{n}$ | $A$ | Output current to achieve 50kW at 333V. Divided over n modules |

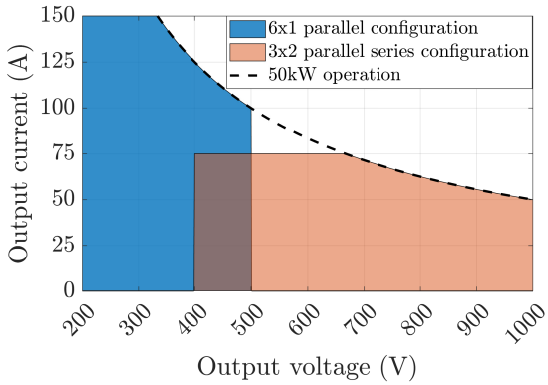


Figure 3. DC charger maximum output current using 6 modules of 25A maximum current each

Since limited time was available, this project focuses on the optimization of a fixed input voltage and wide output voltage range DC-DC (200-500V) DAB design and optimization of a single module, that can be used in parallel and series with another such module. An analytical approach was taken to both get a better understanding of the system, as well as the vastly faster simulation time compared to a circuit simulation in e.g. PLECS. This allowed for more parameters to be considered and optimized.

Improvements in semiconductor technologies enable more efficient power conversion and allow for hard-switching, leading to this research where the optimal Dual Active Bridge (DAB) implementation, configuration and design choices for bi-directional DC charging are determined. A comparison is made between a circuit optimised for only soft-switching and a simpler configuration while allowing hard-switching using analytical models. This provides insight in the possibility of removing the soft-switching constraint in a DAB. Furthermore, a method to increase the efficiency in the low power range of a multi-module configuration is proposed.

## 2. DAB optimization method

To have a fair comparison between the soft-switching and hard-switching optimized circuits, an optimization was used for both circuits. A full-bridge DAB, shown in Figure 4, is used in both circuits, with the only difference being an additional commutation inductor $L_{c1}$ for the soft-switching optimized implementation that is not present in the hard-switching optimized implementation. $V_{DC-in}$ and $V_{DC-out}$ are the primary and secondary side voltages respectively. The inductors and transformer, the AC link, are discussed in more detail in subsection 3.3.

The design and optimization is split into different parts that are integrated with each other to create one integrated model. This model contains all the component models, the optimizations and result processing. The goal of the optimizer is to find a DAB configuration that is most optimal for a typical charge cycle of a battery electric vehicle. The optimization consists of a few stages, being: transformer optimization, inductor(s) optimization, and modulation optimization for a range of operating points.

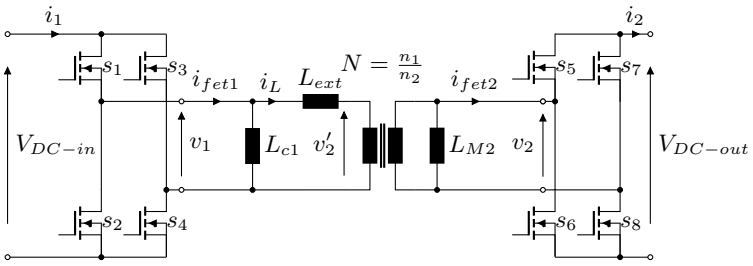


Figure 4. DAB structure including commutation inductors

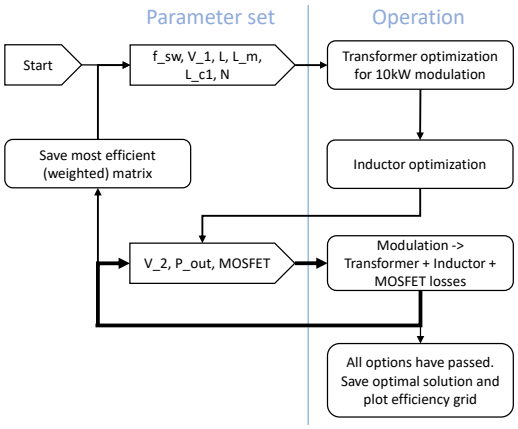


Figure 5. Workflow of the optimization

The input voltage of the DAB is fixed, but can be chosen between 800V and 1000V since this is the design area of a three-phase AC-DC converter. The voltage and current levels are different between the primary and secondary side. To make use of this fact, the optimizer can select different MOSFETs on the primary side and the secondary side to allow for an optimal MOSFETs selection per side. A grid search is used to find the component sizes and configurations of the best solution for the soft-switching circuit and the hard-switching circuit. The high level optimization process is shown in Figure 5.

The efficiency map, which is generated by evaluating operation points of different output voltages and powers (the bottom loop in Figure 5), is weighted by a weights map in order to achieve a single efficiency value. This value is then used to determine which configuration is the best. The weights are chosen such that the operating region where most power transfer happens over a charge cycle is targeted the most by the optimizer. The weight map that is used to determine the performance of a configuration is shown in Figure 6, where the charge cycle of a 400V and 800V battery are shown which are approximated according to [3] and the knowledge of the typical nominal battery pack voltage from Figure 1. Depending on the initial voltage of the battery, the module might be current limited, indicated by the diagonal line at low voltages. Once the voltage is increased enough, full power can be provided by the module, indicated by the vertical line at 10kW. The connected car will communicate [4] when the charging current, and thus charging power, will be decreased below the maximum power of the charger, resulting in the almost horizontal line at the end of a charging cycle. The weighted module efficiency is determined with

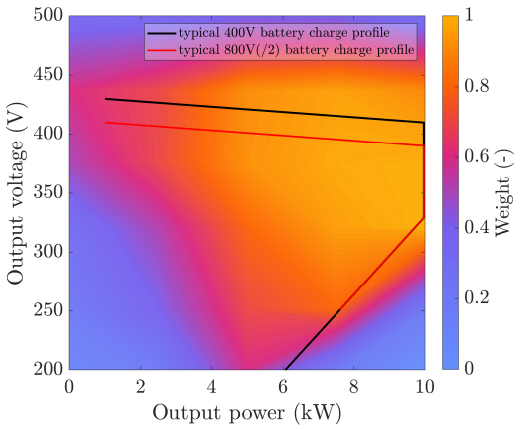


Figure 6. Weight map to optimize for important operating regions

$$\eta_{weight} = \frac{\sum_{n=1}^{n_{max}} \eta(n)w(n)}{\sum_{n=1}^{n_{max}} w(n)}, \tag{1}$$

where $n$ is an operation point, $\eta(n)$ is the efficiency at the selected operation point and $w(n)$ is the weight of the operation point. This method also penalises failing operating points.

## 3. DAB design methods

Component models are used to determine the losses in the DAB which in turn are used to determine the system efficiency. At first the core model is described which integrates the different parts of the simulation. This model serves as a connecting layer between the modulation and the component simulations. After that the semiconductor models are discussed. Then the magnetic components were integrated. Lastly the efficiency calculation is described.

### 3.1. Core model

The core model, referring to the main simulation setup, contains the main behaviour of the DAB in Figure 4. This core part of the simulation generates and handles the voltage and current waveforms depending on parameters such as the primary and secondary side voltage levels, inductances and modulation parameters. Triple phase-shift modulation is implemented in the core model since this provides large benefits over single phase-shift [5]. With triple phase shift there are twelve different switching modes when considering bi-directional power flow [6]. Each mode has a different order in which the rising and falling edges of the primary and secondary side voltages occur. Out of the twelve possible switching modes, it appeared that only two different modes were preferred in forward power transfer under zero voltage switching according to [7]. The other modes generate more losses for the same power transfer. These modes are selected by changing the three modulation parameters $\phi$, $\tau_1$ and $\tau_2$ (visualised in Figure 13), where $\phi$ is the phase shift angle between the primary and secondary side and $\tau_1$ and $\tau_2$ the pulse width modulation angles of the primary and secondary side respectively. The core model uses all the system parameters and modulation parameters to generate the voltage and current waveforms that are used as input for the loss models. The current waveform can be derived from the modulation parameters that determine the voltage waveforms of the primary and secondary side of the transformer and external inductor. The next time point current in any conductor component in the AC link can be calculated with

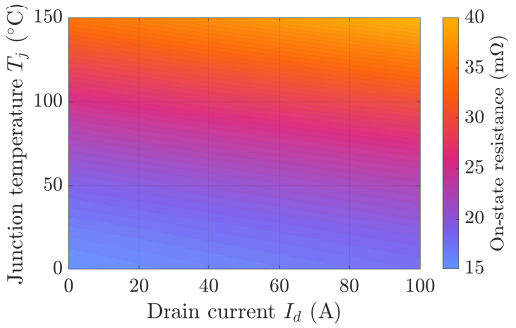


Figure 7. On-state resistance of SCT4018KW7 with respect to junction temperature and drain current for $V_{gs}$ = 18V

$$i_L(t_{n+1}) = i_L(t_n) + \frac{1}{L}\int_{t_n}^{t_{n+1}} V_L dt, \tag{2}$$

where $i_L(t_n)$ is the starting current, $L$ is the inductance, $t_n$ is the starting time, $t_{n+1}$ is the end time and $V_L$ is the voltage over the inductor. This calculation is performed for each time step for both the transformer + external inductor combination $L_{leak}$ + $L_{ext}$, as well as the commutation inductors $L_{c1}$ and $L_{M2}$. The modulation, which determines the voltage waveforms, is described in more detail in section 4.

### 3.2. Semiconductors

To determine the most optimal input and output semiconductors, accurate models were created of different Silicon Carbide (SiC) MOSFETs. Gallium Nitride (GaN) FETs are not considered as these are not available for breakdown voltages above 650V and often have too little datasheet information for accurate models. Silicon (Si) MOSFETs are also not used because of the lower efficiency compared to SiC MOSFETs. A 30% derating on the breakdown voltage is used as a safety margin to avoid complications during hard switchin. The semiconductor losses can be separated into conduction losses and switching losses, which will be explained in more detail in the following paragraphs.

#### 3.2.1. Conduction losses

The on-state resistance models are created with datasheet polynomial fits that determine the on-state resistance as a function of temperature and drain current. The gate voltage was taken as a constant at the nominal gate voltage according to the datasheet. A selection of 18 different MOSFETs with a breakdown voltage in the range of 650-1700V was made. The results of the datasheet fit of one of the MOSFETs can be seen in Figure 7. A variety of MOSFETs with different on-state resistances are evaluated. Generally MOSFETs with a lower on-state resistance (and thus less conduction losses) have more switching losses, where MOSFETs with less switching losses have more conduction losses. Hence, a trade-off must be made. The wide selection of MOSFETs will allow the optimization algorithm, discussed in section 2, to choose the optimal MOSFETs.

The conduction losses of the MOSFETs are calculated with

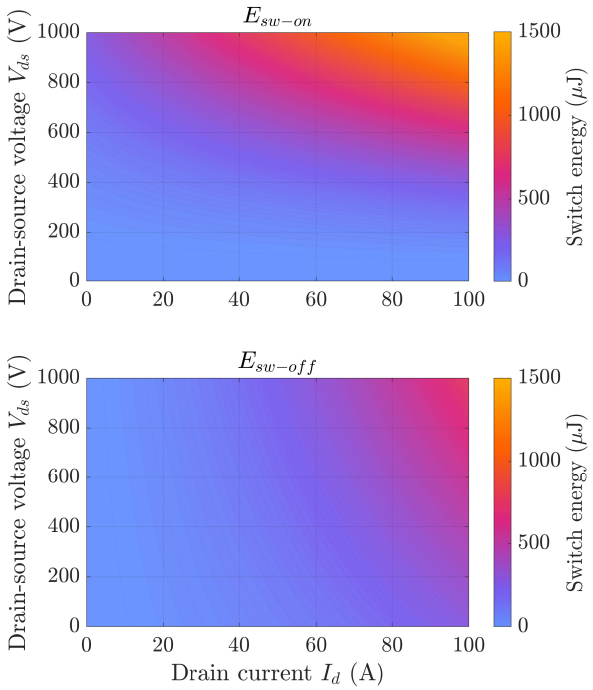


Figure 8. Turn on and off energy of SCT4018KW7 with respect to drain-source voltage and drain current for a gate resistance of 3.3Ω

$$P_{cond} = R_{ds} I_{d-RMS}^2, \tag{3}$$

where $I_{d-RMS}$ is the Root Mean Square (RMS) drain current and $R_{ds}$ is the on-state resistance which depends on the junction temperature and current. Since the current is not constant during a on cycle, a method must be chosen to determine the current that is taken to determine the on-state resistance. The mean current during the on time of each MOSFET is taken as this will result in the mean on-state resistance during the on time.

### 3.2.2. Switching losses

The switching losses are modeled in the same manner, where the losses were fitted from datasheet curves. These losses mostly depend on the drain-source voltage and current. Temperature is not considered, as this generally has little effect on the switching losses, or no data is available. It is assumed that the gate resistance is the lowest that is described in the data sheet since this is always the most efficient. This choice was made to be compatible with as many MOSFETs as possible, as well as the limitation that this value is not known until a PCB is developed. The result of one of the MOSFETs can be seen in Figure 8. The switching losses are calculated with

$$P_{sw} = (E_{sw-on} + E_{sw-off}) f_{sw}, \tag{4}$$

where $E_{sw-on}$ and $E_{sw-off}$ are the switching loss energies during a single switch on or off event respectively and $f_{sw}$ is the switching frequency.

Partial commutation during switching conditions is taken into account to more accurately model the losses in the edge case between soft switching and hard switching. To determine if commutation is partial or has completed, the

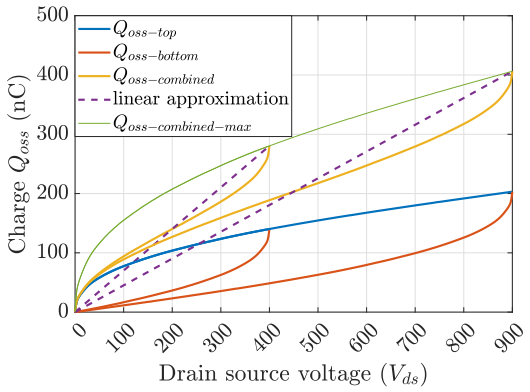


Figure 9. Parasitic charge $Q_{oss}$ of SCT4018KW7 with respect to $V_{ds}$, for a bus voltage of 400 and 900V

displaced charge during the dead time is compared with the initial parasitic charge present on the MOSFETs in a half-bridge. The parasitic charge of a MOSFET that needs to be displaced when turning on or off is equal to [8]

$$Q_{oss} = \int_0^{V_{bus}} C_{oss}(v) dv, \tag{5}$$

where $C_{oss}$ is the output capacitance of a single MOSFET and $V_{bus}$ is the DC bus voltage. The moved charge during the dead time of the half bridge is calculated with

$$Q_{deplete} = -i_d t_{deadtime}, \tag{6}$$

where $i_d$ is the drain current and must be negative (otherwise it is hard-switching) and $t_{deadtime}$ is the dead time. If more charge can be depleted than there is present in the two MOSFETs, full commutation happened and soft-switching conditions apply, where no turn-on losses are assumed based in the knowledge that zero-voltage switching results in up to 95% less losses than hard switching [9]. If not all the charge has been depleted, because of too short dead time and too little current, partial commutation occurs. The parasitic charge curves for two arbitrary 'bus' voltages are shown in Figure 9 and have a similar shape to previous research in GaN parasitic charge [10].

It can be seen that the total charge that needs to be moved is the addition of $Q_{oss-top}$ and $Q_{oss-bottom}$. It is then easy to see that the total charge that needs to be moved is directly related to $Q_{oss-top}$ with

$$Q_{oss-combined-max}(V_{bus}) = 2Q_{oss-top}(V_{bus}), \tag{7}$$

where $Q_{oss-top}(V_{bus})$ refers to the $Q_{oss}$ charge on the top MOSFET when the bus voltage $V_{bus}$ is across the drain and source. The combined charge of the two MOSFETs with respect to bus voltage is not quite linear when charging/discharging them, but a linear assumption speeds up the simulation significantly while still capturing the essence of the phenomena. With linear interpolation of $V_{ds}$ with respect to $Q_{oss}$, the voltage across the MOSFET can be approximated during partial commutation. This can then be used to approximate the losses of the MOSFETs. A fixed dead-time of 200 $n$s is used for all simulations to give both solutions the same amount of effort to achieve soft switching. The primary side MOSFETs show a maximum overestimation of 0.48W and a maximum underestimation of 1.17W. On the secondary side this is 0.30W and 1.16W respectively.

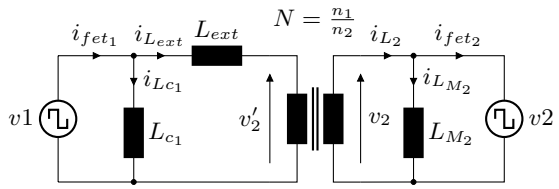


Figure 10. Simplified (lossless) electrical model of the AC link of the DAB based on [13]

This corresponds to a maximum operating point efficiency error of 0.23% from 1kW output power, to 0.02% error for 10kW. The calculations are shown in Appendix B.

#### 3.2.3. Thermal model

The temperature of the semiconductor is determined by a thermal model suitable for steady state operation that includes the thermal resistance from junction to case $R_{jc}$ (in the datasheet of each MOSFET) and from case to ambient $R_{ca}$ with the relation

$$T_j = (R_{jc} + R_{ca})P_{cond}P_{sw} + T_a, \tag{8}$$

where $T_a$ is the ambient temperature. The $R_{ca}$ thermal equivalent resistance is assumed to be $3\frac{K}{W}$ based on the knowledge that steady state operation with appropriate cooling can achieve this according to [11]. Since the junction temperature and on-state resistance have a cyclic dependency, a method is needed to determine these states. An iterative approach is used where the temperature and on-state resistance are updated in sequence, until they do not change more than 0.5% for three cycles in a row to avoid accidental completion. An initial temperature guess is used at 50°C with which equilibrium is often reached after 4 iterations. Since the operations are simple, there is no significant simulation time increase to this method. For the thermal model, an ambient temperature of $40°C$ is assumed. The junction temperature is not allowed to come within $50°C$ of the maximum junction temperature. This is done to extend the system life time by reducing the temperature swing of the semiconductors that causes thermal cycling [12]. If a semiconductor becomes too hot, it will not be considered a viable option.

### 3.3. Magnetic components

Another important and complex component in the optimization is the transformer. A lossless model, used to determine the currents in the transformer, is shown in Figure 10. The commutation inductor current $i_{Lc_1}$ is directly related to the voltage waveform of $v_1$. The inductor $L_{ext}$ current $i_{L_{ext}}$ is related to the primary side voltage $v_1$ and the primary side referenced secondary voltage $v_2'$. This inductor is in series with the leakage inductance $L_{leak}$ inside the transformer which was taken into account when the simulations were made. The magnetizing inductance $L_{M_2}$ of the transformer can be used to create the commutation inductor on the secondary side. The commutation inductors can easily be included or excluded in the optimization to allow for a comparison between the more complex circuit that increases the soft switching range and the simple circuit without commutation inductors for the case where hard switching is allowed.

#### 3.3.1. Magnetics optimization

An optimization is performed to determine the most optimal transformer core and configuration. A transformer model that was created in [14] was used as a basis for the transformer model. The model already calculates the core losses with the improved Generalized Steinmetz Equation (iGSE), described in e.g. [15]. It also calculates the conduction losses in the primary and secondary side wires considering the proximity losses as well as DC losses, where Skin-effect is taken into account. Furthermore, the air gap length is calculated such that the requested magnetizing inductance is achieved and the leakage inductance is calculated. The optimization parameters that are used in the optimization are:

- core material
- E core dimensions
- primary side number of turns
- secondary side number of turns
- Litz strand wire diameter
- number of Litz wires in a bundle
- switching frequency
- turns ratio
- magnetizing inductance
- number of parallel cores
- number of paralleled wires at primary side
- number of paralleled wires at secondary side
- window area ratio between primary and secondary
- airgap legs (center or all).

An optimization was created where, not only the losses were minimized, but also the leakage inductance to avoid manufacturing difficulties or inconsistencies. In this research the transformer can not change during operation so it is only optimized once per DAB configuration and not per operating point. Generating and evaluating a transformer takes a long time; hence, a grid search for many parameters will take too long. Therefore, a surrogate optimization is utilized to find a good solution for the mixed-integer problem with a non-linear objective function. This implementation quickly comes to a good solution, but does not settle or converge because it keeps trying new options. The surrogate optimization function is discussed and evaluated further in Appendix A.

The output of an optimization is shown in Figure 11, where the optimization was performed for a 10kW power transfer at 80kHz for a magnetizing inductance of $250\mu H$. A more detailed explanation of the used transformer model is given in [14].

A similar model is used to create the inductors $L$ and $L_{c1}$, with less parameters available to change. Here the iGSE is used to determine the core losses and again the conduction losses are calculated to determine the wire losses taking into account DC losses and proximity losses with the use of the MATLAB toolbox: "automatic design of inductors for power conversion".

#### 3.3.2. Thermal model

The transformer model from [14] was extended with a thermal model to indicate if the selected core can transfer the peak power without overheating. An R network is used to determine the steady state operating temperature of different parts of the transformer. The transients of the temperature in the core are not considered since the core will operate under

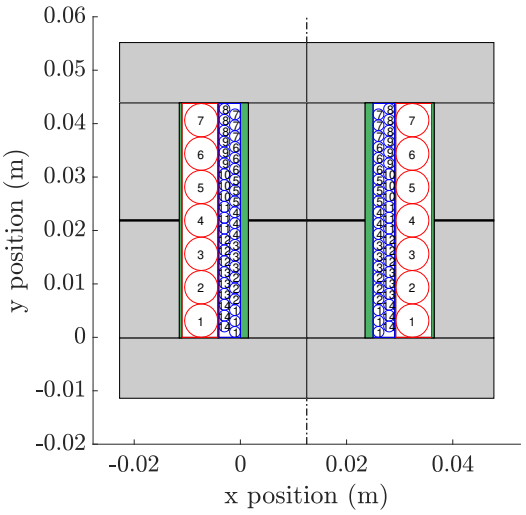


Figure 11. Core optimization output for 10kW power transfer with 820V input, 480V output, turns ratio of 2 and a magnetizing inductance of 230 $\mu H$

TABLE 2. THERMAL CONDUCTIVITY OF TRANSFORMER MATERIALS

| **Material** | **thermal conductivity** $\lambda$ $[\frac{W}{m \cdot K}]$ |
|---|---|
| Ferrite Mn-Zn | 3.9 [16] |
| Ferrite Ni-Zn | 6.3 [16] |
| Copper | 398 |
| Litz-wire | 3.4 [17] |

slowly changing conditions mostly, as DC charging requires the core to transfer a constant power for a long time. The thermal resistances of different parts of the transformer are determined with a few parameters according to the relation

$$R_{th} = \frac{l}{\lambda A}, \tag{9}$$

where $l$ is the length of the thermal path, $\lambda$ is the thermal conductivity of the material and $A$ is the area of the heat transfer. The thermal conductivity coefficient of the materials in the transformer are shown in Table 2. It can be seen that, although copper is thermally very conductive, Litz-wire is less conductive due to the insulation layer between each wire.

The thermal resistance of the exposed parts of the transformer, being the primary winding and a part of the transformer core, can be calculated with a formula for forced convection, dependent on the transformer dimensions, cooling medium and cooling medium speed. The formula for the thermal resistance due to convection that was used in this thermal model is described in [18].

An equivalent nodal network was created that includes the heat sources and thermal resistances between heat paths in the transformer and from the transformer to the ambient air through convection. The thermal nodal network for the transformer core is shown in Figure 12. The thermal resistances and heat sources are labeled in Table 3.

The core losses are divided into two parts: unexposed core losses and exposed core losses. Part of the transformer core is exposed to the air directly and a part is obstructed by the secondary and primary windings. The losses are divided according to the volume that is exposed directly or not. The unexposed part of the core can conduct heat to both the

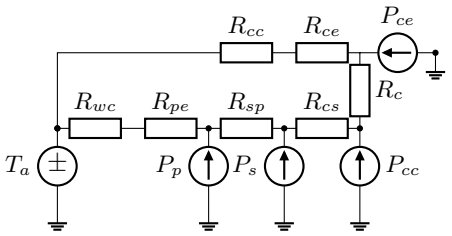


Figure 12. Thermal nodal network inspired by [15]

TABLE 3. THERMAL NETWORK SYMBOL DESCRIPTIONS

| **Symbol** | **description (resistance means thermal resistance)** |
|---|---|
| $R_{wc}$ | Winding convection equivalent resistance |
| $R_{pe}$ | Primary winding to edge of winding resistance |
| $R_{sp}$ | Secondary to primary winding resistance |
| $R_{cs}$ | unexposed core to secondary winding resistance |
| $R_c$ | unexposed core to exposed core resistance |
| $R_{ce}$ | exposed core center to edge resistance |
| $R_{cc}$ | exposed core convection equivalent resistance |
| $P_p$ | Primary winding losses |
| $P_p$ | Secondary winding losses |
| $P_{cc}$ | Unexposed core losses |
| $P_{ce}$ | Exposed core losses |
| $T_a$ | ambient temperature |

secondary side windings and the exposed part of the core. The set of equations resulting from the nodal network can be derived as shown in [15], where the energy balance equation can be adapted to

$$\begin{aligned} 0 &= \frac{T_a - T_{ce}}{R_{cc} + R_{ce}} + \frac{T_{cc} - T_{ce}}{R_c} + P_{ce} \\ 0 &= \frac{T_{ce} - T_{cc}}{R_c} + \frac{T_s - T_{cc}}{R_{cs}} + P_{cc} \\ 0 &= \frac{T_p - T_s}{R_{sp}} + \frac{T_{cc} - T_s}{R_{cs}} + P_s \\ 0 &= \frac{T_a - T_p}{R_{wc} + R_{pe}} + \frac{T_s - T_p}{R_{sp}} + P_p, \end{aligned} \tag{10}$$

where $T_{ce}$ is the temperature of the exposed core, $T_{cc}$ is the temperature of the enclosed core, $T_s$ is the temperature of the secondary side winding and $T_p$ is the temperature of the primary side winding. This set of equations can be solved to determine the temperature in each component. These temperatures can then be evaluated to determine if any part of the transformer gets too hot under the selected operating conditions.

### 3.4. Efficiency

The efficiency of each configuration is calculated for an operation space. This space is defined by output power, in the range 1kW to 10kW, and the output voltage, in the range 200-500V. By comparing the input power with the output power, the efficiency of every operating point is calculated with the following relation

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{MOSFETs} - P_{magnetics}}{P_{in}}, \tag{11}$$

where $P_{out}$ is the usable power on the secondary side, $P_{in}$ is input power, $P_{MOSFETs}$ are the MOSFET losses of the primary and secondary side combined consisting of conduction losses and switching losses, and $P_{magnetics}$ are the losses in the transformer and inductor(s)

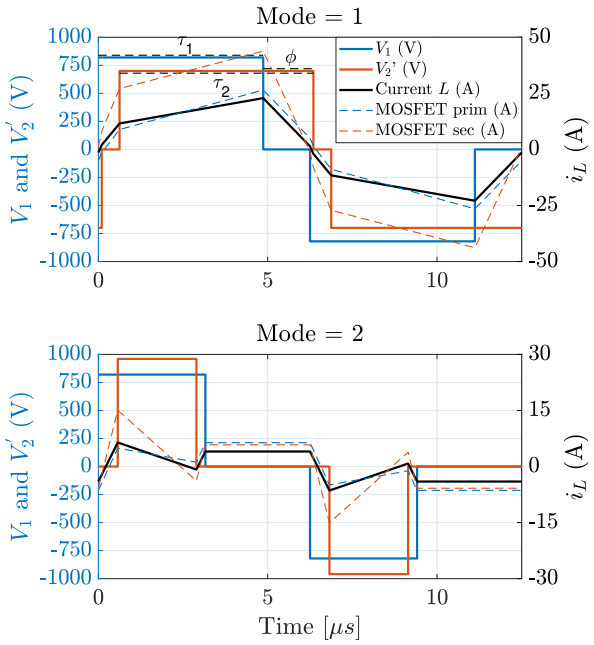


Figure 13. Example of mode 1 and mode 2 optimized waveforms under soft-switching modulation for $L_{ext} + L_{leak}$ = 45 $\mu H$, N = 2, $V_{DC-in}$ = 820, $L_m$ = 250 $\mu H$, $L_{c1}$ = 550 $\mu H$ and $f_{sw}$ = 80 kHz

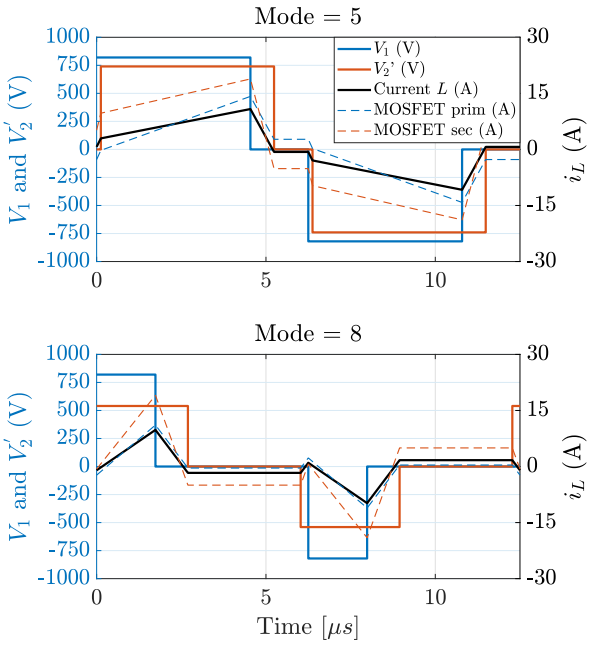


Figure 14. Example of mode 5 and mode 8 optimized waveforms under soft-switching modulation for $L_{ext} + L_{leak}$ = 45 $\mu H$, N = 2, $V_{DC-in}$ = 820, $L_m$ = 250 $\mu H$, $L_{c1}$ = 550 $\mu H$ and $f_{sw}$ = 80 kHz

consisting of core losses and conduction losses taking into account proximity effect. Although auxiliary power for measurements, processing and active cooling decreases system efficiency, it will be similar for both solutions, hence, these losses will not be taken into account. Gate driving losses are also left out of the equation, as these are similar for the two solutions, and small in comparison to the conduction and switching losses [19].

## 4. Modulation method

To give both DAB configurations the best chance to be as efficient as possible, the modulation must be implemented correctly as this can greatly influence the efficiency of the system. Therefore, an optimization is performed for each operating point that is evaluated. Triple-phase-shift provides large benefits over single-phase-shift as was identified in [5], therefore triple-phase-shift modulation is used. To guarantee soft switching operation for the soft switching constraint configuration, the modulation optimization is run for alternated MOSFET loss models that have extremely large turn-on losses during hard switching. The hard switching solutions will then result in overheating and will be disregarded. The system efficiency is not only dependent on the MOSFET losses, but also on the transformer and inductor(s) losses. It was found that taking all these losses into account results in improved system efficiency with respect to only considering the MOSFET losses in the modulation optimization, especially in low power transfer regions where magnetic losses can be dominant. Examples of the two modes identified in [7] are shown in Figure 13.

Two additional modes, mode 5 and 8 according to [7], were implemented as these appeared to be viable options. These modes are shown in Figure 14.

### 4.1. Modulation optimization strategy

The modulation optimization consists of two stages. First a grid search is performed to determine a set of modulation parameters that will generate the requested output power. The initial grid is chosen from 0.1$\pi$ to 1$\pi$ for both $\tau_1$ and $\tau_2$ in 21 steps. The shift between the first falling edge of the primary side voltage and the first falling edge of the secondary side voltage phi is then taken from -0.5$\pi$ and 0.5$\pi$ in 41 steps resulting in 18081 evaluated points. Only solutions close to the requested power are evaluated further to determine the most efficient solution. The losses of the MOSFETs, transformer and inductor(s) are calculated for the potential solutions, after which the most efficient solution is taken. If no solution was found, a finer grid is chosen with 34476 points. This approach saves time since it will often find a solution in the smaller grid search.

The best result of the grid search is used as an initial guess for the minimization operation, which is the second stage of the modulation optimization. The MATLAB built in minimization function ”fminsearch” is used to find the optimum by changing the three input parameters and optimizing for two output parameters: efficiency and power. Power is also taken into account since the requested operating power should be delivered. This will not happen if efficiency is the only optimization parameter because this can cause the optimizer to move to the global optimum at that output voltage, which might have a different power level. The difference between the output power and the requested output power $P_{diff}$ is used in the optimization where

$$P_{diff} = |P_{ref} - P_{out}|, \tag{12}$$

where $P_{ref}$ is the reference output power and $P_{out}$ is the simulated output power. The minimization function is then defined by

$$F_{val} = (1 - \frac{P_{out}}{P_{in}}) + P_{diff} \cdot 10^{-5}. \tag{13}$$

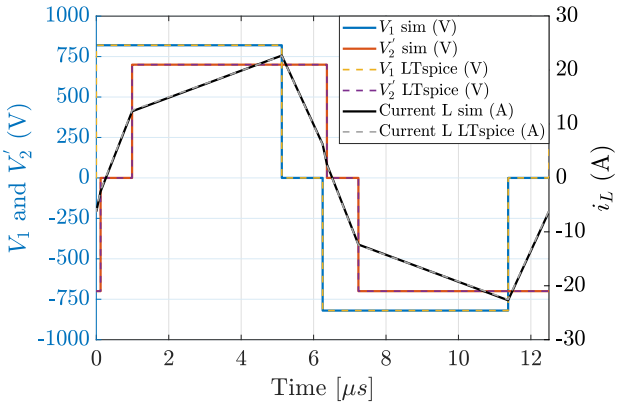


Figure 15. Analytical waveform validation with an LTspice simulation for $L_{ext} + L_{leak}$ = 48 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 230 $\mu H$ and $f_{sw}$ = 80 kHz

A correction factor is used such that not all the focus is on achieving the requested output power, but also the efficiency will be maximized. Although this method could not be used in real time, it does provide the necessary accuracy to do the comparison between the soft-switching constrain and hard-switching allowed solutions, as well as giving insight in the optimal modulation mode selection depending on the operation conditions. A comparison between the optimization result and the implementation of a soft switching guaranteed modulation strategy described in [7] (also triple-phase-shift) showed that the optimization indeed finds a higher efficiency than the analytical solution when used on the loss models described in this paper.

## 5. Results and discussions

The simulation models were used to determine if hard-switching should remain a requirement in a DAB. First the waveform generation, which is handled by the core model, is validated to check if no mistakes were made in the analytical approach. Then the optimal configuration of the two solutions is compared. Then the modulation optimization results are given and discussed. At last the combined module efficiency is determined where an efficiency extending method is proposed.

### 5.1. Waveform validation

#### 5.1.1. Results

To validate if the inductor currents are calculated correctly, an LTspice simulation is performed with the same inductance value and modulation parameters as the analytical implementation. This was done for a 1kW use case and a 10kW use case. The result of the simulations for the 10 kW use case is shown in Figure 15. It can be seen that the current from both simulations overlap. The maximum difference in current in this case is 0.15 A, which is 1.3% for that operating point. For the 1kW use case the maximum difference in current is 0.016 A, which is 1.0% for that operating point.

#### 5.1.2. Discussion

The waveform calculation in the analytical approach is nearly identical to the LTspice simulation. This means that the core model from subsection 3.1 can closely approximate the current behaviour in the inductor(s) and transformer. Therefore, the loss models that use the calculated currents will result in accurate loss calculations.

TABLE 4. OPTIMAL CIRCUIT PARAMETERS FOR A 10KW DC-DC MODULE

| Parameter | unit | Soft-switching | Hard-switching |
|---|---|---|---|
| $f_{sw}$ | kHz | 80 | 80 |
| $V_{in}$ | $V$ | 820 | 820 |
| $L_{ext} + L_{leak}$ | $\mu H$ | 45 | 48 |
| $L_{M_2}$ | $\mu H$ | 250 | 230 |
| $L_{c_1}$ | $\mu H$ | 550 | - |
| transformer ratio N | - | 2 | 2 |
| MOSFET primary | - | SCT4036KW7 | SCT4036KW7 |
| MOSFET secondary | - | SCT4018KW7 | SCT4018KW7 |

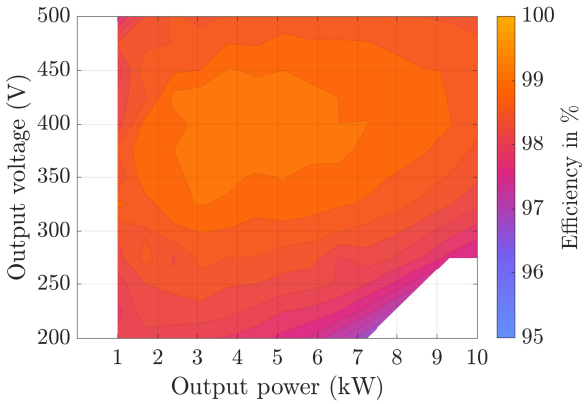


Figure 16. Efficiency map of the hard-switching allowed implementation for the optimised parameters: $L_{ext} + L_{leak}$ = 48 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 230 $\mu H$ and $f_{sw}$ = 80 kHz

### 5.2. Module efficiency comparison

#### 5.2.1. Results

The DAB optimization, described in section 2, is performed for a large set of parameters for both the soft-switching constraint and hard-switching allowed solution. The resulting optimal parameters for both solutions are shown in Table 4. To visualise the performance of both solutions, an efficiency map is created. The efficiency map of the optimized DAB without the commutation inductor and allowing hard-switching is shown in Figure 16. The efficiency map of the soft-switching constraint optimal configuration is shown in Figure 17.

A comparison between the mean and maximum efficiency

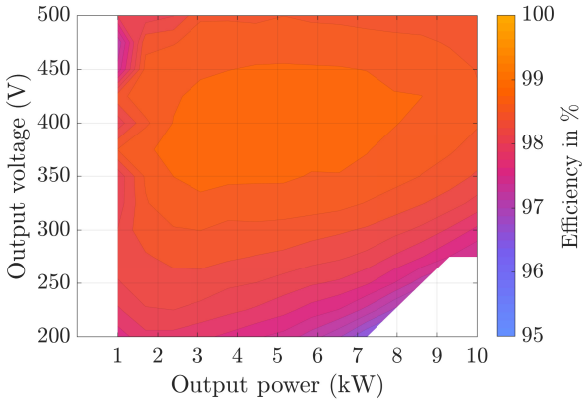


Figure 17. Efficiency map of the soft-switching constraint implementation for the optimised parameters: $L_{ext} + L_{leak}$ = 45 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 250 $\mu H$, $L_{c1}$ = 550 $\mu H$ and $f_{sw}$ = 80 kHz

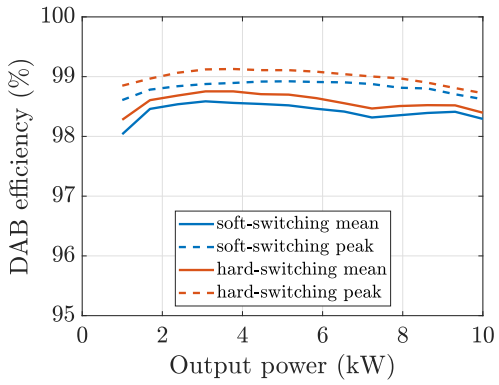


Figure 18. Comparison between the hard-switching allowed and soft-switching constraint module efficiencies for the achievable operating points

TABLE 5. EFFICIENCY COMPARISON BETWEEN SOFT-SWITCHING CONSTRAINT AND HARD-SWITCHING ALLOWED IMPLEMENTATION

| Method | Soft-switching circuit | Hard-switching |
|---|---|---|
| Weighted $\eta$ | 97.21% | 97.36% |
| mean $\eta$ | 98.42% | 98.58% |
| max $\eta$ | 98.92% | 99.13% |

of both solutions can be made for the different power levels as can be seen in Figure 18. A few methods can be used to show the performance of the solutions with a single value: the weighted efficiency described in section 2, the mean (unweighted) of all achievable operating points, and the maximum efficiency. The results of both solutions are shown in Table 5. Another optimization was performed where the hard-switched allowed circuit, meaning no additional commutation inductor, was used under soft-switching constraint modulation. The weighted efficiency of this solution was 96.58% and two important operating conditions were not achieved, showing the necessity of a commutation inductor for the soft-switching constraint solution.

To see where the difference in losses are, a comparison between the losses per component per power level can be seen in Figure 19. This helps with identifying the efficiency gain or loss per component between the implementations. Within the semiconductor the losses can be split in switching losses and conduction losses. These losses are compared between the two implementations in Figure 20. For larger power transfer, the conduction losses in the primary side were lower for the hard switching allowed solution, due to the absence of the commutation inductor.

#### 5.2.2. Discussion

When comparing the efficiency maps of the two implementations, it can be seen that the most optimal region is in the same area and they both manage to operate over the same operation space. There is a small difference in weighted efficiency which shows that the hard-switching allowed implementation is more efficient for a typical EV charge cycle by 0.15%. The mean and max efficiency per power level are higher for the hard-switching allowed implementation as apparent from Figure 18. The increase in mean efficiency for high output power is due to the absence of the low output voltage high output power solutions (the open area in the right bottom of the efficiency maps), because the module can not achieve this operation due to

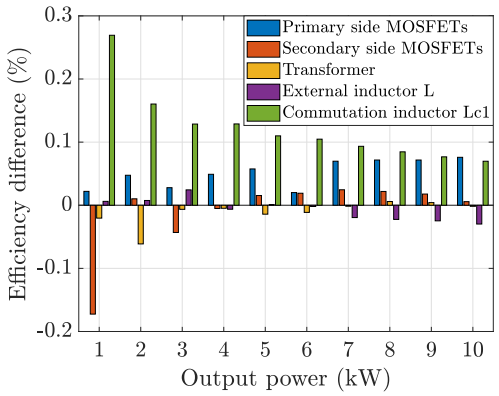


Figure 19. Hard-switching allowed efficiency gain over soft-switching constraint implementation per component

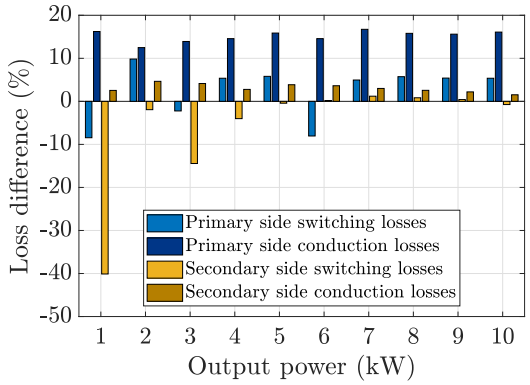


Figure 20. Hard-switching allowed efficiency gain over soft-switching constraint implementation in a semiconductor with respect to the total losses of the semiconductor

overheating of components. More detailed per component losses are discussed in Appendix C.

The largest efficiency gain of the hard-switching allowed implementation during low power transfer is in the removal of the commutation inductor. At higher power levels, the removal of the commutation inductor still helps, but also the primary side reduced conduction losses in the MOSFETs due to the lower currents, and thus conduction losses, become significant.

### 5.3. Modulation results

#### 5.3.1. Results

The modulation optimization manages to optimize the module efficiency as a function of the MOSFETs, inductor(s) and transformer losses as well as the requested output power. A modulation selection map can be created for the operation space of the DAB. The hard-switching allowed and soft-switching constraint modulation mode selection can be seen in Figure 21 and Figure 22 respectively.

The output power error with respect to the requested output power is at most 1.5% for 1kW power transfer. From 2kW and higher, the output power is within 0.3% of the requested output power. This means the optimization method correctly and accurately optimizes for output power.

#### 5.3.2. Discussion

Although only 2 modes were identified to be efficient in [7], the modulation optimization showed the need for mode

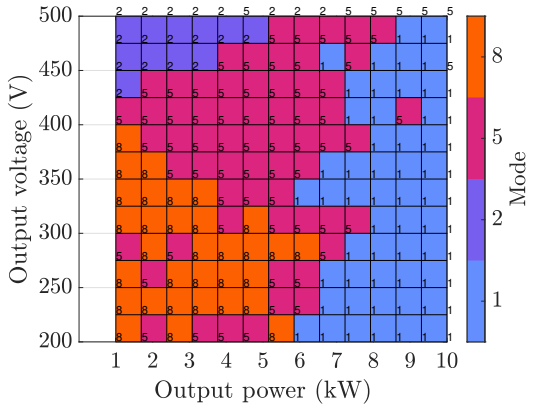


Figure 21. Modulation optimization mode selection over the operation space for hard-switching allowed implementation for $L_{ext} + L_{leak}$ = 48 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 230 $\mu H$ and $f_{sw}$ = 80 kHz

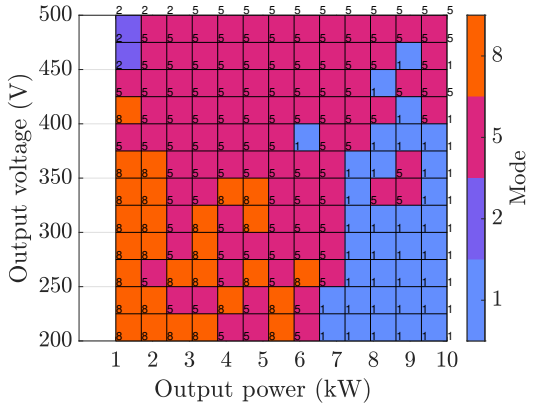


Figure 22. Modulation optimization mode selection over the operation space for soft-switching constraint implementation for $L_{ext} + L_{leak}$ = 45 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 250 $\mu H$, $L_{c1}$ = 550 $\mu H$ and $f_{sw}$ = 80 kHz

5 and 8 to increase the efficiency for a large operation space. The challenge in changing modes during operation of the DAB is the discontinuity if soft-switching must be maintained. When hard switching is allowed, a transition can be more gradual as it can move through the hard switched region instead of jumping over. The benefit of the two extra modes is apparent from the selection of the modulation optimization as visible in the modulation map for the hard-switching allowed implementation in Figure 21. Areas can be distinguished where certain modes give the best efficiency. All four identified modes have their operation space where they are more efficient than the other modes. The mode map is highly dependent on the component dimensions, hence this map cannot be used for any configuration.

Also the soft-switching constraint implementation shows the use of the four identified modulation modes as can be seen in Figure 22. A similar selection of modes in the operation space can be seen with respect to the hard-switching implementation.

When analysing the modulation results, it was found that if the optimiser chooses for a hard-switching solution, the current during a switching instance often was below 10 A. This is likely due to the higher losses during hard-switching with large drain currents as can be seen in Figure 8.

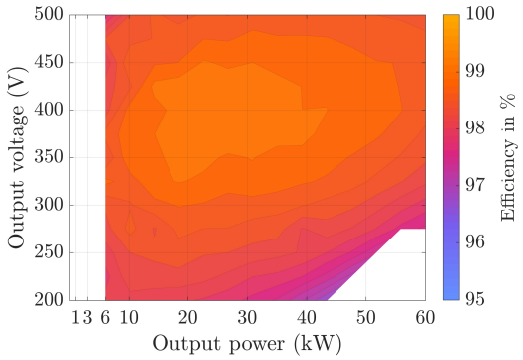


Figure 23. Hard-switch allowed 6 module system efficiency map for $L_{ext}+$ $L_{leak}$ = 48 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 230 $\mu H$ and $f_{sw}$ = 80 kHz

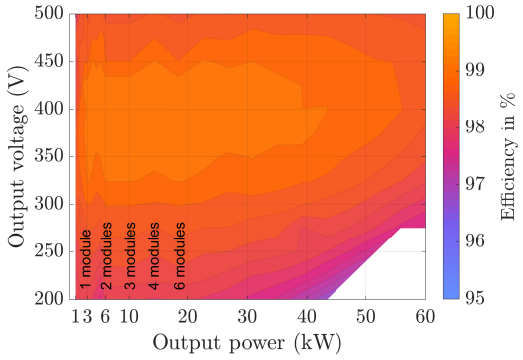


Figure 24. Hard-switch allowed 6 module dynamic turn on and off system efficiency map for $L_{ext} + L_{leak}$ = 48 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 230 $\mu H$ and $f_{sw}$ = 80 kHz

## 5.4. 50kW system efficiency

### 5.4.1. Results

With the use of 6 modules, a 50kW charger can be made. The system efficiency, when allowing hard-switching and using all the modules, is shown in Figure 23. The power rating of a single module is multiplied by six and additional losses in the circuit (of relays for example) are not taken into account. The system efficiency can be improved for low power operation by turning off modules such that the remaining modules operate in a higher efficiency point. The efficiency map for such an approach will be similar to Figure 24. This approach can also be used for the soft-switching constraint implementation.

The mean efficiency gain for low output power is especially apparent when looking at Figure 25. The efficiency below 18kW is boosted with this method.

### 5.4.2. Discussion

The system efficiency at low power operation can be increased by turning off modules to increase the power demand in the remaining modules that will then operate more efficiently. Additionally, the minimum output power of the system can be decreased by a factor of six, because the five other modules can be turned off. A limitation in this approach is in the series parallel configuration, where at least two modules must be operational to provide the higher output voltage. In this case two, four or six modules can be turned on depending on the requested output power.

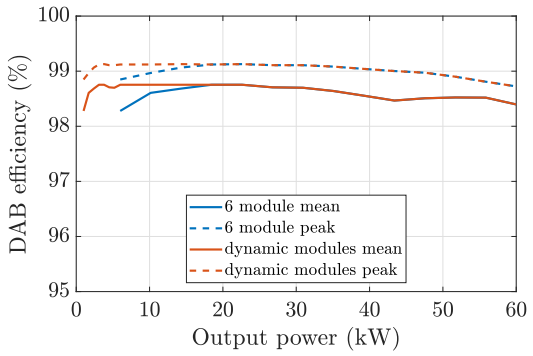


Figure 25. Comparison between mean and maximum efficiency by making use of dynamic module turn on and off for $L_{ext} + L_{leak}$ = 48 $\mu H$, N = 2, $V_{DC-in}$ = 820 $V$, $L_m$ = 230 $\mu H$ and $f_{sw}$ = 80 kHz

## 6. Conclusion

This research shows that the requirement for soft-switching a DAB is no longer needed and actually decreases system efficiency due to the required additional commutation inductor and higher losses in the semiconductors. Analytical models were used based on real products to perform the analysis for two different DAB structures. An optimization was performed for both implementations to perform a fair comparison. The analytical waveform models were validated through simulations and showed only up to a 1.3% current error.

The hard-switching allowed configuration has a 0.15% weighted efficiency gain over the soft-switching implementation, while reducing the number of required components and relaxing the modulation constraints. This means the system costs can go down and the modulation implementation becomes easier. The modulation optimization showed the need of four different modes that can be used to create the optimal modulation parameters per operating condition. With the use of a series parallel reconfigurable module layout, a large output voltage range can be achieved while maintaining acceptable efficiencies. Additional system efficiency can be gained by dynamically turning on and off modules depending on the requested output power.

Additional research can be done by validating the research findings with a prototype. Furthermore, the modulation implementation can not be used real-time, as the optimization is too computationally heavy. Hence, an analytical expression could be derived for the hard-switched allowed implementation that can be implemented in a controller. Another interesting research direction is the implications of hard-switching on electromagnetic compatibility. This would prove the simulation results in practice and make it possible to use the proposed simple, yet efficient, DAB implementation for bi-directional charging.

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## Appendix A

A surrogate optimization can make use of mixed-integer variables. It is a suitable tool for computationally intense non-convex optimizations as it can find a good solution in a few iterations as can be seen in Figure 26. The function uses random searches as well as adaptive searched where it tries to adapt some of the parameters when it finds a good solution with respect to previous solutions. This helps in finding a good solution in as few iterations as possible.

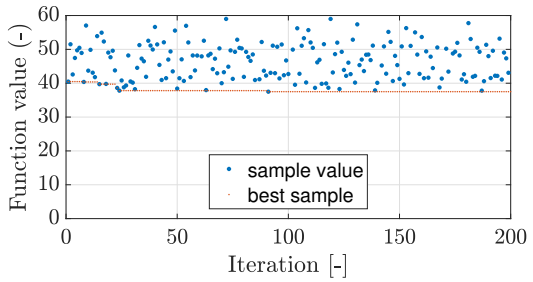


Figure 26. Surrogate optimization of a 10kW transformer with 820V input, 480V output, turns ration of 2 and a magnetizing inductance of 230 $\mu H$

## Appendix B

The partial commutation simplification, by assuming a linear relation between $Q_{oss}$ and the remaining voltage $V_{ds}$ across the MOSFET, results in a small error in loss calculation. The difference in the calculated loss can be determined by comparing the actual losses with the estimated losses. To determine these losses, first the voltage across $V_{ds}$ must be determined for both cases with respect to the residual charge $Q_{oss}$. The charge - voltage relation described in Equation 5 is used for the real case. The linear assumption is used to determine the voltage difference as shown in Figure 27

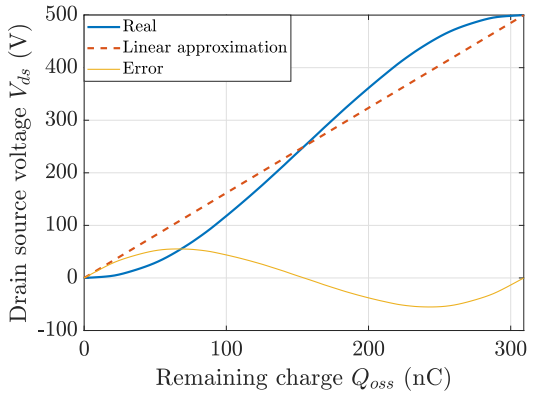


Figure 27. Comparing the drain-source voltage against remaining charge of a SCT4018kW7 half bridge with a bus voltage of 500V for the real case and the linear approximation

The turn-on switching losses during partial commutation can now be determined by using the remaining drain-source voltage after partial commutation and knowing the switching frequency and using the loss map shown in Figure 8. The comparison between the real losses and approximation is shown in Figure 28. The maximum output voltage, where the SCT4018kW7 MOSFETs are used, is 500V. This is where the largest possible error can occur on the secondary side. The same analysis was done for the primary side MOSFETs SCT4036KW7, where the bus voltage is 820V.

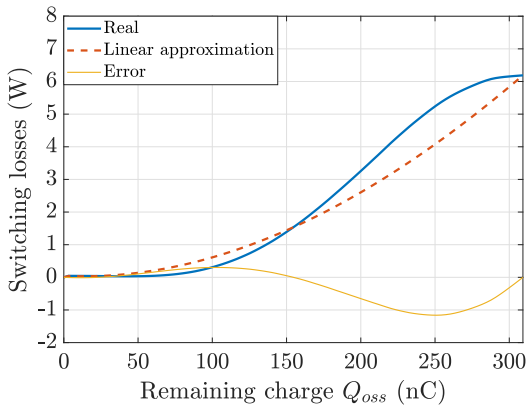


Figure 28. Comparing the switching losses against remaining charge after partial commutation of a SCT4018kW7 half bridge with a bus voltage of 500V and a switching frequency of 80kHz for the real case and the linear approximation

## Appendix C

The losses per component and per configuration provide some additional insight in the losses of the DAB. First the losses in the soft-switched DAB are shown.

### Soft-switching constraint DAB component losses

The soft-switching DAB losses per component are shown in Figure 29-33.

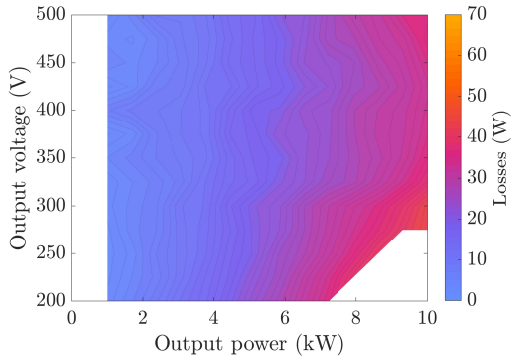


Figure 29. Transformer losses in soft-switching implementation

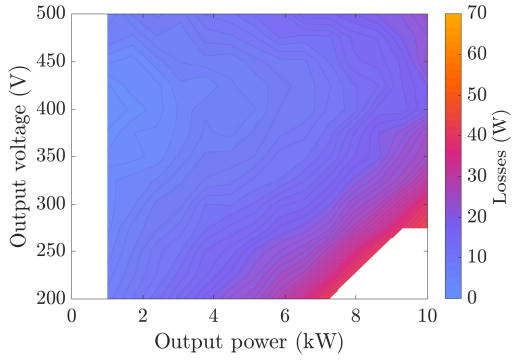


Figure 30. External inductor losses in soft-switching implementation

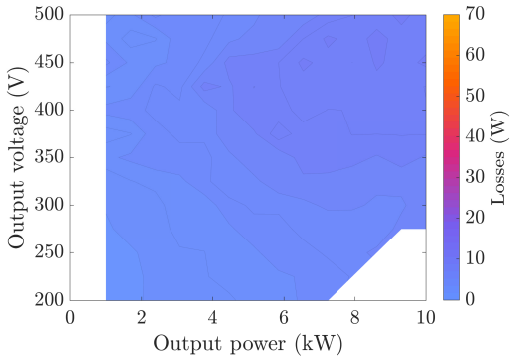


Figure 31. Commutation inductor losses in soft-switching implementation

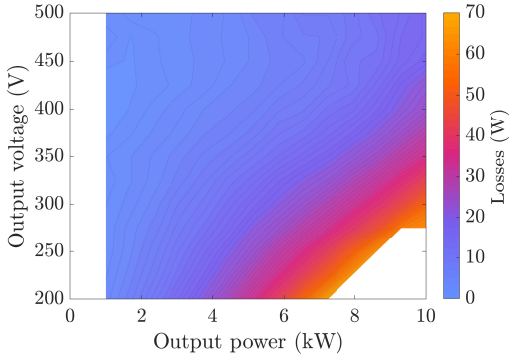


Figure 32. Primary side combined MOSFET losses in soft-switching implementation

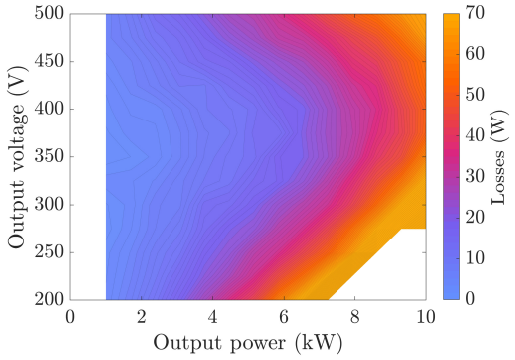


Figure 33. Secondary side combined MOSFET losses in soft-switching implementation

## Hard-switching allowed DAB component losses

The hard-switching allowed DAB losses per component are shown in Figure 34-37. There are no losses in the commutation inductor because this component is not used in the hard-switching allowed implementation.

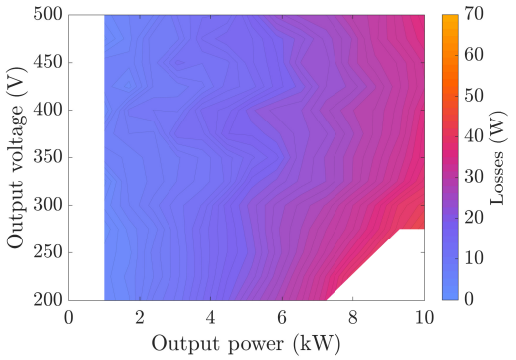


Figure 34. Transformer losses in hard-switching allowed implementation

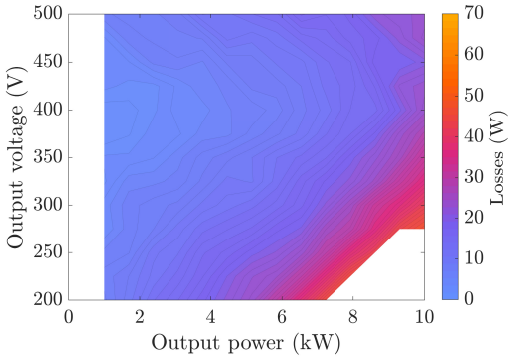


Figure 35. External inductor losses in hard-switching allowed implementation

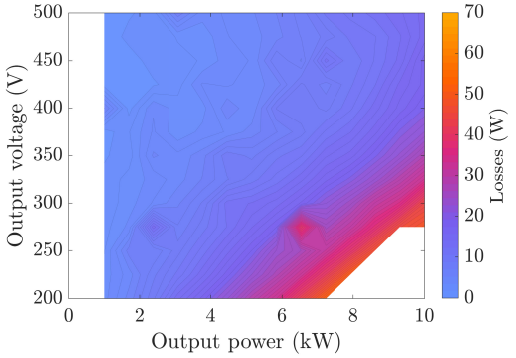


Figure 36. Primary side combined MOSFET losses in hard-switching allowed implementation

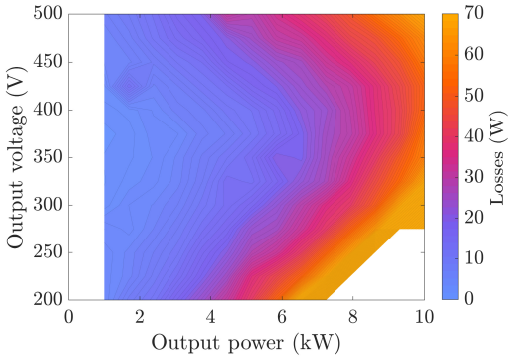


Figure 37. Secondary side combined MOSFET losses in hard-switching allowed implementation