Power Electronics for Plasma Processing

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Power Electronics for Plasma Processing

Enabling Energy-Efficient and Accurate Ion Energy Control for Semiconductor Manufacturing

PROEFSCHRIFT

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door

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geboren te Zhejiang, People's Republic of China

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Summary

Power Electronics for Plasma Processing

PLASMA is an ionized gas consisting of positive ions, electrons, and neutral particles. It is used in essential process steps in semiconductor manufacturing, for both deposition and etching. Deposition is a process of growing thin film layers on the substrate, and etching is a process of selectively removing the material layers of a specific pattern. Plasma is crucial in these processes as it provides additional reaction energy, lowers the process temperature, increases throughput, enhances anisotropy, and so forth.

The ever-growing demand for more powerful computing capability continuously pushes the transistors in the integrated circuits (ICs) to shrink, enabling more circuitry to be laid down in the same space. With the advent of an artificial intelligence (AI) revolution led by ChatGPT, this demand will reach new heights, posing critical challenges to plasma processing in semiconductor manufacturing. One of these challenges is accurately controlling the plasma ion energy to allow more precise process control and improved quality.

Plasma processing occurs within a plasma reactor. In the reactor chamber, plasma is ignited and sustained by applying a power source to a feedstock gas. This power source can be either capacitively or inductively coupled with the feedstock gas. With the substrate wafer placed on the reactor table, the fast-moving electrons in the plasma can get lost in the wafer, forming a region on the substrate surface where the ion density exceeds the electron density, known as the plasma sheath. An electric potential difference is built over the sheath, causing the substrate surface potential to be consistently lower than the plasma potential. Consequently, ions are accelerated in the plasma sheath, bombard the substrate, and enhance material processing reactions on the substrate surface. Different processing recipes require different plasma ion energy. The bombarding ions should carry sufficient energy to be effective in the reactions, but excessive ion energy could degrade the process quality

and damage the substrate. In short, this means that the ion energy distribution (IED) should fall into a narrow window.

The ion energy can be controlled by a bias converter, which is electrically connected to the reactor table and the bottom side of the substrate. The bias converter generates voltage waveforms, typically negative on average, to further increase the voltage difference over the plasma sheath, thus accelerating the ions to the desired energy. Among the various bias waveforms that can be used, the tailored waveform is found particularly promising, since it can achieve a narrow IED for a broad range of applications.

The tailored waveform comprises a negative voltage slope followed by a positive voltage pulse. The negative voltage slope compensates for the charge accumulation effect caused by the bombarding ions in the capacitance of the dielectric substrate. The voltage pulse is applied to discharge and reset all the capacitors in case of overvoltage and restart the process with the desired substrate surface potential.

Traditionally, such tailored waveforms are generated by linear amplifiers, which are of low efficiency. Besides, a matching network is required for the linear amplifier, adding additional energy dissipation. While switched-mode power converters (SMPCs) are well-known energy-efficient alternatives to linear amplifiers, they are not yet widespread in this cutting-edge technology. However, they have recently demonstrated immense potential. Nevertheless, designing an effective SMPC requires a well-established load that reflects the electrical responses of the plasma. Currently, such models are unavailable, which is a significant obstacle to transitioning towards efficient power electronics.

Therefore, this thesis derives an equivalent electric circuit (EEC) of the plasma processing that depicts the electrical behavior for all phases in tailored waveform biasing. It can be simulated in combination with the bias converter on a circuit level. Moreover, the IED can also be reproduced from the circuit simulation, which substantially reduces the computational effort compared to traditional plasma simulations like particle-in-cell (PIC). Furthermore, a parameter identification method is proposed to extract all the parameters of the EEC model. This method only requires the voltage and current measurements on the bias converter side, which is non-intrusive to the process.

The proposed model reveals that the below-zero portion of the falling edge of the voltage pulse determines the ion energy value, while the voltage slope determines the width of IED. The optimal slope should result in the narrowest IED, and it is dependent on the ion current and the substrate capacitance, thus varying under different operating conditions. Conventionally, this optimal slope is manually tuned by measuring the IED in real-time using a retarding field energy analyser (RFEA). Such manual tuning needs to be repeatedly conducted once the operating conditions

change. Meanwhile, the RFEA can introduce errors. This thesis develops an auto-tuning method, which finds the optimal slope based on mathematical relations between voltage and current, thus eliminating the need for an RFEA.

Based on the proposed model, this thesis proposes a multilevel tailored waveform bias converter concept, which is based on efficient switched-mode operation. The original tailored waveform, specifically the voltage slope, is replaced by a sequence of monotonically decreasing voltage levels. Approximating the voltage slope with the multilevel waveform can introduce undesired voltage ripples on the substrate surface, which could broaden the IED. To overcome this, a filter inductor can be added to further reduce the voltage ripple, at the cost of a slower voltage pulse. This compromise is analyzed in this thesis, and the constraints for the multilevel waveform configurations given by the required IED are derived. Based on the analysis, it is found that multilevel voltage converters can be used in this application, offering the benefits of scalability and modularity compared to other existing concepts. Specially, an asymmetrical multilevel converter, formed by a T-type converter and two cascaded H-bridge converters, is proposed in this research.

The plasma reactor is a capacitive load, thus forming an LC circuit with all the inductance in the converter loop. This LC circuit can cause severe resonance triggered by the voltage pulse. To minimize the resonance in a non-dissipative manner, a trajectory control method is developed. This method utilizes multiple intermediate voltage levels and determines a specific switching sequence during the rising and falling edge of the voltage pulse.

A converter prototype is designed to verify the various concepts. The magnitude and frequency of the multilevel waveform are optimized by pushing the switching components to their limits based on a comprehensive switching loss model. Based on the EEC model, a plasma-reactor mockup is designed and built to emulate the electrical responses of the plasma reactor, which is used as the qualification load for the converter prototype. This research provides a systematic solution for accurate ion energy control, from plasma processing modeling to converter design, control, and optimization, paving the way towards more energy-efficient and accurate semiconductor manufacturing.

Contents

Chapter 1 Introduction

PLASMA is widely recognized as the fourth state of matter, along with solid, liquid, and gas [14]. It not only exists in nature, such as within the Sun and during lightning strikes, but can also be artificially generated, as is the case with the plasma in a neon light and nuclear fusion [88].

Essentially, a plasma refers to an ionized gas, whereby at least one electron is stripped off a neutral atom, leaving a free-moving negatively charged electron and a positively charged ion [23]. Similar to how heating a liquid can produce a gas, adequately heating a gas can also create a plasma since gaseous particles, when colliding with one another with sufficient energy, can knock off electrons [63].

Plasma plays a crucial role in semiconductor manufacturing, particularly in plasma-enhanced deposition and etching processes for nanodevice fabrication [72, 149]. Nowadays, the ever-growing demand for the semiconductor industry attaches more and more importance to plasma processing. As the size of ICs continues to shrink, new challenges are brought to plasma processing, which are the central focus of this thesis.

While plasma physics is fascinating, it can be quite complex. This chapter provides a first glimpse into plasma and plasma processing. Necessary plasma physics and the basics of plasma processing are introduced in this chapter. Subsequently, the research scope and the thesis outline are provided.

This chapter is based on [183].

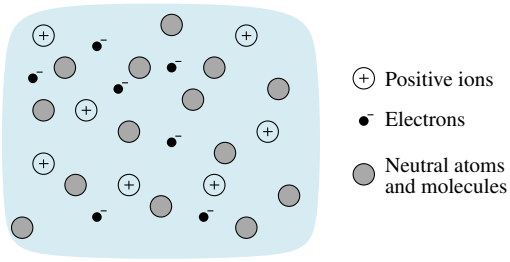


Figure 1.1 The composition of a plasma.

1.1 Plasma physics

1.1.1 Plasma fundamentals

Not all gas atoms need to be ionized to create a plasma. A plasma can be composed of positive ions, electrons, and neutral atoms and molecules, as depicted in Figure 1.1. The quantities of ions, electrons, and neutral particles per unit volume are represented by n_i, n_e, and n_n, respectively. From a macroscopic viewpoint, a plasma is expected to have an approximately neutral net charge, known as quasi-neutrality [2]. It should be stressed that only the singly charged ions are considered in this thesis. Therefore, quasi-neutrality implies that $n_\mathrm{i} = n_\mathrm{e} \equiv n$, where n denotes the charged particle density in the plasma.

The behavior of plasma can vary significantly based on its degree of ionization, which is defined as

$$D_\mathrm{i} = \frac{n_\mathrm{i}}{n_\mathrm{i} + n_\mathrm{n}}. \tag{1.1}$$

A plasma with $D_\mathrm{i} \approx 1$ is considered fully ionized while $D_\mathrm{i} \ll 1$ corresponds to a weakly or partially ionized plasma [2]. As a matter of course, the Sun's core and the nuclear fusion plasmas are fully ionized [84, 118].

In the semiconductor manufacturing industry, weakly ionized plasmas are typically used, making them the main focus of this thesis. The most common method of exciting plasma is by applying an electric field to a neutral gas at low pressure and relatively low temperature. The electric field accelerates free electrons, which then collide with the gas atoms. If the kinetic energy of the electrons is greater than the ionization energy, these collisions can create new charged particles [31]. This ionization process can be represented by

$$\mathrm{e} + \mathrm{A} \longrightarrow 2\,\mathrm{e} + \mathrm{A}^+,$$

where e is the electron, and A represents an atom. The ionization releases additional free electrons, which in turn further the ionization process as an avalanche. In this

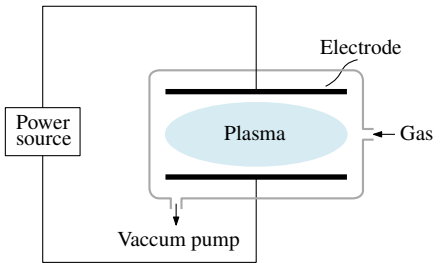


Figure 1.2 The schematic of a gas discharge.

way, a weakly ionized plasma is ignited by the electric field, also known as "gas discharge" [154].

Figure 1.2 provides an example of a gas discharge in which two electrodes are connected to a power source, generating an electric field between them. With the feedstock gas infused, a plasma is excited and sustained. The power source can be of various types, such as direct current (dc) [42], pulsed dc [12], radio-frequency (RF) [95, 162], *etc* [31].

Different types of particles undergo collisions within a plasma. In a weakly ionized plasma, these collisions can be inelastic, meaning that the total kinetic energy changes after the collisions [167]. Inelastic collisions in a plasma include ionization, excitation, dissociation, and electron attachment [30]. For instance, during the excitation process, a colliding electron can provide energy to an atom, causing it to enter its excited state. The electron within the atom jumps from the ground state to a higher energy level. This excitation requires less energy compared to ionization, and it is unstable. Within a short period, the excited atom can return to the ground state, and a photon can be emitted [126]. The photon emission explains the glow we see from a plasma and can be described by

$$\mathrm{e} + \mathrm{A} \longrightarrow \mathrm{e} + \mathrm{A}^* \longrightarrow \mathrm{e} + \mathrm{A} + \text{photon},$$

where A* is the atom in excited state. Dissociation is another vital reaction in plasma processing, which can be expressed as

$$\mathrm{e} + \mathrm{AB} \longrightarrow \mathrm{e} + \mathrm{A} + \mathrm{B},$$

where AB is a molecule, and A and B could be radicals with high chemical reactivity.

Electrons can lose their kinetic energy in these inelastic collisions [181]. Usually, a vacuum pump is adopted to lower the pressure in the chamber, as depicted in Figure 1.2. A lower pressure results in smaller particle densities and larger interparticle distances generally [107], thus sharply reducing the collisions and enabling and sustaining plasma excitation at a low temperature.

When discussing "low temperature" in this context, it is important to clarify what is meant by this term. Temperature is a macroscopic property of a system, so it is not typically discussed in reference to a single particle. Additionally, temperature is normally only defined in systems that are in thermal equilibrium [84]. A gaseous system in thermal equilibrium is one in which particles collide randomly and exchange their energy sufficiently with each other. In this scenario, particles have different velocities that can be described by the Maxwell-Boltzmann distribution. Specifically, in one-dimensional coordinate x, the distribution is

$$f(v_x) = \left(\frac{m}{2\pi k_\mathrm{B} T}\right)^{\frac{1}{2}} \mathrm{e}^{-\frac{mv_x^2}{2k_\mathrm{B}T}}, \tag{1.2}$$

where v_x is the particle velocity in one dimension, $f(v_x)$ is the probability density function, k_B is Boltzmann's constant, T is the system temperature, and m is the mass of the particles [84]. In three-dimensional coordinates, the velocity distribution is given as

$$f(v) = \left(\frac{m}{2\pi k_\mathrm{B} T}\right)^{\frac{3}{2}} 4\pi v^2 \mathrm{e}^{-\frac{mv^2}{2k_\mathrm{B}T}}, \tag{1.3}$$

where v is the particle velocity. It is worth noting that v is a scalar value. The velocity distribution of particles of the same species is solely determined by the temperature. Since particles are of different velocities, a single representative value, such as the average velocity v_avg given by

$$v_\mathrm{avg} = \int_0^\infty v f(v) \mathrm{d}v = \sqrt{\frac{8k_\mathrm{B}T}{\pi m}} \tag{1.4}$$

and the root-mean-square (RMS) velocity v_rms given by

$$v_\mathrm{rms} = \sqrt{\int_0^\infty v^2 f(v) \mathrm{d}v} = \sqrt{\frac{3k_\mathrm{B}T}{m}}, \tag{1.5}$$

can be chosen to describe the temperature [80]. Moreover, the corresponding particle kinetic energy E can be calculated by

$$E = \frac{1}{2} m v_\mathrm{rms}^2 = \frac{3}{2} k_\mathrm{B} T, \tag{1.6}$$

which relates the average energy of gaseous particles with the temperature. Such representative velocity v_rms is also named the thermal velocity.

In a weakly ionized plasma, the inter-particle distance is deliberately increased, and the particle collisions are brought down. Therefore, the energies of electrons, ions, and neutral particles are not equalized. Hence, a weakly ionized plasma is not in thermal equilibrium. Technically, in this case, the Maxwell-Boltzmann distribution is not applied, and the definition of temperature is more complex [19].

Nevertheless, electrons, as a single species, are in near-thermal equilibrium [2], so they are assumed to follow the Maxwell-Boltzmann distribution at electron temperature T_e in this thesis. For simplicity, ions and neutral particles can also be considered in thermal equilibrium at their respective temperature (T_i and T_n) [84], assuming that particles of the same species collide sufficiently with themselves but interact much less with other species [24].

The temperatures T_e and T_i can be significantly different. Simply considering a charged particle with an elementary charge e, it experiences an acceleration $\boldsymbol{a}$ in an electric field $\boldsymbol{E}$, governed by

$$\boldsymbol{a} = \frac{\boldsymbol{F}}{m} = \frac{e\boldsymbol{E}}{m}, \tag{1.7}$$

where $\boldsymbol{F}$ is the force exerted on the particle. The work W done by the electric field on the particle is determined by

$$W = \boldsymbol{F}\boldsymbol{x} = \boldsymbol{F} \cdot \frac{1}{2}\boldsymbol{a}t^2 = \frac{(e\boldsymbol{E}t)^2}{2m}, \tag{1.8}$$

where $\boldsymbol{x}$ is the displacement, and t is the time. As a result of their significantly smaller mass, electrons in the plasma gain substantially more energy from the electric field compared to the ions. In contrast, ions can only obtain a very limited amount of energy from elastic collisions with electrons, which can be easily solved using the laws of conservation of energy and momentum [180]. Consequently, T_e is significantly higher than T_i. In a typical weakly ionized plasma, T_e can be on the order of 10^4 K, while T_i ranges from 300 to 1000 K [126]. Neutral particles, which have dominant quantities, stay at a lower temperature from 300 to 500 K. Therefore, the plasma as a whole is considered low-temperature.

1.1.2 Plasma sheath

Quasi-neutrality, as previously introduced, holds for a bulk plasma. However, it may be locally violated in the region near a solid material surface, such as a wafer, probe [22], or electrode, as shown in Figure 1.2. This special region is called the plasma sheath, where the ion density is greater than the electron density.

To provide an intuitive perception, first consider a plasma surrounded by two solid material surfaces with floating electric potential, as depicted in Figure 1.3(a). Since a weakly ionized plasma is typically contained in a vessel [56], such a parallel plate system can be seen as the elementary construction of the plasma system in one dimension. According to Maxwell's equations [66], the electric field is determined by

$$\nabla \cdot \boldsymbol{D} = \nabla \cdot \epsilon\boldsymbol{E} = \rho_f, \tag{1.9}$$

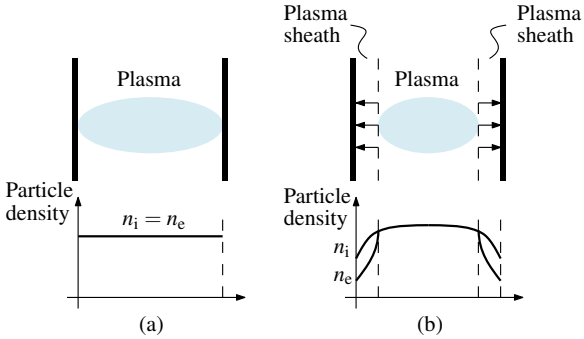


Figure 1.3 The formation of plasma sheaths. (a) Initially, the plasma is surrounded by two solid material surfaces. (b) Shortly, the plasma sheaths are formed on the material surfaces. The arrows indicate the direction of the electric fields.

where $\nabla\cdot$ is the divergence operator, $\boldsymbol{D}$ is the electric displacement field, ϵ is the dielectric constant, and ρ_f is the volume charge density. Quasi-neutrality, as represented by $n_\mathrm{i} = n_\mathrm{e}$, leads to

$$\rho_f = e\left(n_\mathrm{i} - n_\mathrm{e}\right) = 0. \tag{1.10}$$

Therefore, initially, both the electric field $\boldsymbol{E}$ and the electric potential u are zero everywhere in the plasma. In other words, the electrons and ions are not confined and can move freely [2]. As derived in (1.6), the velocity of electrons is much larger than that of ions due to their much higher temperature and lower mass. The electrons immediately flux into the materials, thus negatively charging the material with respect to the plasma. The negatively charged materials form electric fields towards their surfaces, as shown in Figure 1.3 (b). Meanwhile, the electric potential of the bulk plasma increases and becomes higher with respect to the materials. The electric potential continues to rise as long as there is a net flux of negative electrons until the steady state is reached when the ion and electron fluxes get balanced [56]. Consequently, the ion density is larger than the electron density near the material surface, and such a region is called the plasma sheath.

Because the plasma sheath is an essential and unique characteristic of plasma, it is important to derive its basic properties in order to provide a quantitative understanding. The voltage drop over the sheath is of particular interest, as it determines the energy of ions bombarding the surface. For a parallel plate system, as shown in Figure 1.3, one side can be focused on since both material surfaces are symmetrical, as shown in Figure 1.4. Some basic hypotheses should be accepted for simplicity, including:

- The electrons follow a Maxwell-Boltzmann distribution at T_e, including in the

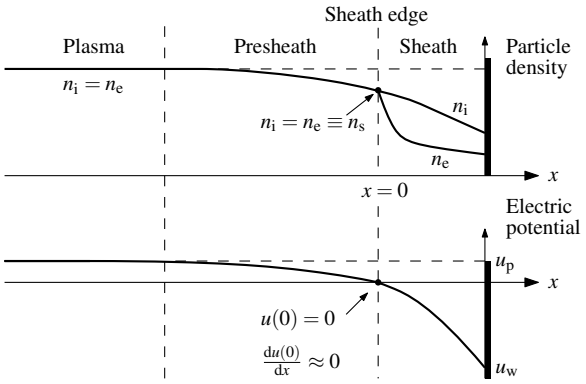


Figure 1.4 The formation of the plasma sheath and presheath [2].

sheath, as elaborated in the previous section.

- Quasi-neutrality holds at the sheath edge, such that $n_i = n_e \equiv n_s$ at $x = 0$, where n_s represents the density of charged particles at the sheath edge.
- The plasma oscillation is neglected so that the plasma is time-independent [62].
- The sheath is collisionless, so there is no ionization happening within it, and the ion flux is equal along with x (known as the fluid model) [58, 62, 137].

By assuming these conditions, a better understanding of the fundamental properties of the plasma sheath can be achieved. First and foremost, the conservation of energy must always be upheld. For ions in the sheath, it follows

$$\frac{1}{2}m_i v_i^2(x) + eu(x) = \frac{1}{2}m_i v_{is}^2, \tag{1.11}$$

where $v_i(x)$ is the ion velocity function with respect to the one-dimensional coordinate x, m_i is the mass of the ion, v_{is} is the ion velocity at the sheath edge, and $u(x)$ is the electric potential defined as zero at $x = 0$, as shown in Figure 1.4. The continuity of the ion flux Γ_i must be guaranteed, leading to

$$\Gamma_i = n_s v_{is} = n_i(x)\, v_i(x). \tag{1.12}$$

The ion density distribution in the sheath can be obtained by solving (1.11) and (1.12), yielding

$$n_i(x) = n_s \left(1 - \frac{2eu(x)}{m_i v_{is}^2}\right)^{-\frac{1}{2}}. \tag{1.13}$$

In an electric field, the electron density is governed by the Boltzmann relation in

thermal equilibrium [2], as described by

$$n_{\mathrm{e}}(x) = n_{\mathrm{e}}(0)\mathrm{e}^{\frac{e(u(x)-u(0))}{k_{\mathrm{B}}T_{\mathrm{e}}}} = n_{\mathrm{s}}\mathrm{e}^{\frac{eu(x)}{k_{\mathrm{B}}T_{\mathrm{e}}}}. \tag{1.14}$$

Poisson's equation in vacuum gives

$$\nabla^2 u = -\frac{\rho_f}{\epsilon_0}, \tag{1.15}$$

where ∇ is the gradient operator, and ϵ_0 is the vacuum permittivity. Based on the assumption that $n_{\mathrm{i}} = n_{\mathrm{e}} \equiv n_{\mathrm{s}}$ at the sheath edge, the electric potential along the coordinate can be derived according to Equation 1.15, as given by

$$\frac{\mathrm{d}^2 u(x)}{\mathrm{d}x^2} = -\frac{e}{\epsilon_0}\left(n_{\mathrm{i}}(x) - n_{\mathrm{e}}(x)\right) = \frac{en_{\mathrm{s}}}{\epsilon_0}\left[\mathrm{e}^{\frac{eu(x)}{k_{\mathrm{B}}T_{\mathrm{e}}}} - \left(1 - \frac{2eu(x)}{m_{\mathrm{i}}v_{\mathrm{is}}^2}\right)^{-\frac{1}{2}}\right]. \tag{1.16}$$

By examining (1.13) and (1.16), it can be deduced that a reasonable value for v_{is} is required in order for n_{i} to decrease along the coordinate x, which is given by

$$v_{\mathrm{is}} \geq v_{\mathrm{B}} = \sqrt{\frac{k_{\mathrm{B}}T_{\mathrm{e}}}{m_{\mathrm{i}}}}, \tag{1.17}$$

where v_{B} is called Bohm velocity. Such a requirement is known as the Bohm sheath criterion, which must be satisfied to form a collisionless sheath [144]. The criterion involves extensive mathematics to deal with (1.16), and it is omitted here. Based on (1.5), the RMS ion velocity is $\left(3k_{\mathrm{B}}T_{\mathrm{i}}/m_{\mathrm{i}}\right)^{-1/2}$, which is negligible compared to v_{B} for $T_{\mathrm{i}} \ll T_{\mathrm{e}}$. Therefore, Bohm velocity can only be obtained by the acceleration in the electric field in the presheath, *i.e.*, the plasma has a positive potential u_{p} with respect to the sheath edge, which is determined by

$$eu_{\mathrm{p}} = \frac{1}{2}m_{\mathrm{i}}v_{\mathrm{B}}^2 = \frac{1}{2}k_{\mathrm{B}}T_{\mathrm{e}}. \tag{1.18}$$

Substituting (1.18) into (1.14) leads to the electron density at the sheath edge as

$$n_{\mathrm{s}} = ne^{-\frac{1}{2}} \approx 0.61n. \tag{1.19}$$

The ion flux Γ_{i} can be calculated by

$$\Gamma_{\mathrm{i}} = n_{\mathrm{s}}v_{\mathrm{is}} = n_{\mathrm{s}}\sqrt{\frac{k_{\mathrm{B}}T_{\mathrm{e}}}{m_{\mathrm{i}}}}. \tag{1.20}$$

To obtain the electron flux on the material surface, the average electron velocity $v_{\mathrm{e,avg}}$ should be calculated, which can be obtained from (1.4) as

$$v_{\mathrm{e,avg}} = \sqrt{\frac{8k_{\mathrm{B}}T_{\mathrm{e}}}{\pi m_{\mathrm{e}}}}, \tag{1.21}$$

where m_e is the mass of electron. Therefore, the electron flux Γ_e onto the material surface can be obtained by [24]

$$\Gamma_e = n \cdot \frac{1}{4} v_{e,avg} = n_s \sqrt{\frac{k_B T_e}{2\pi m_e}} e^{\frac{e u_w}{k_B T_e}}, \tag{1.22}$$

where u_w is the electric potential of the material surface. To balance the net charge flux during the steady state, the electron flux should be equal to the ion flux on the material surface. Consequently, equalizing (1.20) and (1.22) yields

$$u_w = \frac{k_B T_e}{2e} \ln\left(\frac{2\pi m_e}{m_i}\right). \tag{1.23}$$

To conclude, in this plasma system, the plasma maintains a positive floating potential respective to the floating material surface, given by

$$V_p = u_p - u_w = \frac{k_B T_e}{2e} - \frac{k_B T_e}{2e} \ln\left(\frac{2\pi m_e}{m_i}\right). \tag{1.24}$$

This potential difference V_p is determined by the electron temperature T_e, electron mass m_e, and ion mass m_i. For a typical argon (Ar) plasma with $m_i = 40$ atomic mass unit (amu) and $T_e = 56\,000\,\mathrm{K}$, V_p is about 25 V. It implies that the Ar ions are bombarding the material surfaces with an energy $E_i = 25\,\mathrm{eV}$.

The sheath model is derived based on two symmetrical floating surfaces, but it also applies to the case where the two symmetrical surfaces are connected to the same voltage potential (equivalently short-circuited). The voltage potential drop over the sheath should apparently remain the same.

Furthermore, the sheath thickness can be calculated numerically. It is typically thin, in the sub-millimeter to millimeter range [131], and can be approximated by a few Debye lengths λ_D (*e.g.*, $5\lambda_D$ in [21]), which is defined by [165]

$$\lambda_D = \sqrt{\frac{\epsilon_0 k_B T_e}{n e^2}}. \tag{1.25}$$

Therefore, this sheath is also named the Debye sheath.

Readers familiar with semiconductors might experience déjà vu and find an analogy between the plasma sheath and a pn-junction. In a pn-junction, the free-moving electrons in the n-type semiconductor diffuse into the p-type and combine with the holes in the p-type semiconductor. Consequently, in the vicinity of the junction, the p-type has excess electrons and is negatively charged (similar to the material surface). The n-type has excess holes and is positively charged (similar to the bulk plasma). Regions with non-zero net charge form a depletion layer (similar to the

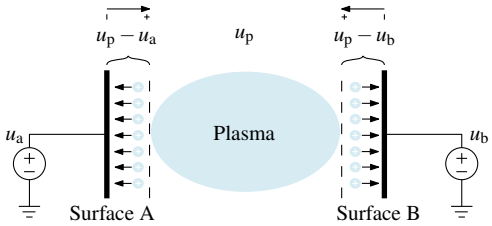


Figure 1.5 The parallel plate system, in which the material surfaces are asymmetrically biased. Here u_a and u_b are the potentials of surface A and B, respectively. The arrow pointing from the minus sign to the plus sign indicates the voltage direction over the sheath.

plasma sheath). An electric field is established towards the p-type, resulting in a built-in potential in the depletion layer (similar to the sheath voltage) [122].

Moreover, both a pn-junction and a plasma sheath have nonlinear capacitances that are voltage-dependent. In fact, a plasma sheath is often modeled by a nonideal diode with a parasitic capacitance in the equivalent circuit model, which will be further elaborated on in the following chapters.

1.1.3 High-voltage sheath

Just like a diode that can be negatively biased, a plasma sheath can also be negatively biased to increase the voltage drop over the sheath. This biasing technique is commonly used in semiconductor manufacturing so that ions can be accelerated by a larger voltage in the sheath and bombard the material surface with higher energy. In a biased parallel plate system, as shown in Figure 1.5, it is equivalent to the case where the material surfaces are asymmetrically biased such that $u_a \neq u_b$.

The voltage drops in each sheath are $u_p - u_a$ and $u_p - u_b$, respectively, resulting in two different sheaths. Under this circumstance, the plasma potential u_p is always determined by the more positive one [24]. For example, if $u_a > u_b$, the Debye sheath, as previously introduced, is formed between the plasma and surface A, and the plasma potential is equal to $u_p = u_a + V_p$ (where V_p is determined by (1.24)).

In practice, surface A can represent the wall of a plasma reactor, which is typically grounded to earth for electrical safety ($u_a = 0$) [146]. Consequently, the voltage drop over the sheath near surface B is determined by $u_p - u_b = V_p - u_b$. Such a high voltage drop cannot be fully taken by the Debye sheath, and an extra sheath smoothly joins the Debye sheath, called the Child law sheath [2], as depicted in Figure 1.6. It must be stressed that these "two sheaths" are imposed artificially for better illustration and easier modeling [24], but in reality, there is only one sheath.

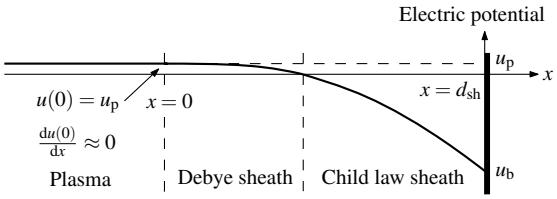


Figure 1.6 The formation of the high-voltage sheath. The presheath still exists, but it is neglected here for simplicity.

Assuming $|u_b| \gg V_p$ when the surface B is negatively biased by a high voltage, V_p can be considered zero for simplicity. Similar to deriving the Debye sheath, the conservation of energy for the ions and the continuity of ion flux give

$$\frac{1}{2} m_i v_i^2(x) + e u(x) = e u_p \approx 0 \tag{1.26}$$

and

$$e\Gamma_i = e n_i(x)\, v_i(x) = e n_s v_B = J_i, \tag{1.27}$$

respectively, where J_i is the constant ion current density. Solving (1.26) and (1.27) for $n_i(x)$ yield

$$n_i(x) = \frac{J_i}{e} \left(-\frac{2eu(x)}{m_i} \right)^{-\frac{1}{2}}. \tag{1.28}$$

According to (1.14), the electron density n_e falls exponentially with $u(x)$. Hence, n_e can be neglected in the Child law sheath, *i.e.*, there exist only ions. Poisson's equation is then written as

$$\frac{d^2 u(x)}{dx^2} = -\frac{e}{\epsilon_0} \left(n_i(x) - n_e(x) \right) = \frac{J_i}{\epsilon_0} \left(-\frac{2eu(x)}{m_i} \right)^{-\frac{1}{2}}. \tag{1.29}$$

Considering the boundary conditions $u(0) = 0$, $\frac{du(0)}{dx} = 0$, and at the surface B $u(d_{sh}) = u_b$, where d_{sh} is the sheath thickness as shown in Figure 1.6, (1.29) can be solved for J_i as [11]

$$J_i = \frac{4}{9} \epsilon_0 \sqrt{\frac{2e}{m_i}} \frac{u_b^{\frac{3}{2}}}{d_{sh}^2}. \tag{1.30}$$

(1.30) is known as the Child-Langmuir law [26, 99], after which the sheath is named. Furthermore, d_{sh} can be determined by

$$d_{sh} = \frac{\sqrt{2}}{3} \lambda_D \left(\frac{2eu_b}{k_B T_e} \right)^{\frac{3}{4}}, \tag{1.31}$$

which can be the order of 100 Debye lengths dependent on the voltage over the sheath [2].

There is a distinct difference between the Debye sheath and the Child law sheath. In the Debye sheath, the ion and electron flux are balanced during the steady state. Thus, there is no net current through the surface. However, in the Child law sheath, the continuous ion flux introduces a net current into the surface because the electron density is almost zero. As a consequence, the bias voltage source u_b is continuously drawing a constant current from the sheath.

Obviously, the ions bombard the surface B with an energy $E_\mathrm{i} = e\left(V_\mathrm{p} - u_\mathrm{b}\right)$. By controlling the value of u_b, the energy of the bombarding ions can be controlled correspondingly for material processing on surface B.

This section provides the necessary fundamentals of plasma for the research. It is also worth noting that the physics model derived in this chapter is based on simplified hypotheses, so it may deviate to some extent from practical scenarios. For further reading, the author suggests referring to the sources cited in the references [2, 23, 24, 161].

1.2 Plasma processing

1.2.1 Semiconductor manufacturing

Semiconductors undoubtedly form the bedrock of nearly all modern industries and technologies. The process of creating a commercial semiconductor device from a polished wafer involves hundreds of sequential steps, of which a repeated cycle of essential steps is depicted in Figure 1.7 [1].

In semiconductor manufacturing, deposition (or thin film technology) is a process of growing thin film layers of atom-scale to micrometer range on a substrate [112]. These thin films can be composed of oxides, metals, or other component materials. Figure 1.7(b) shows a typical deposition process for a silicon dioxide (SiO_2) layer on the most common silicon (Si) wafer. This layer can act as an insulator in various components, such as the gate dielectric in a metal–oxide–semiconductor field-effect transistor (MOSFET) [134].

After necessary post-deposition cleaning, a photoresist is coated onto the wafer surface [38]. The wafer is then exposed to deep or extreme ultraviolet light in a lithography machine, as illustrated in Figure 1.7(c). The ultraviolet light projects the reticle pattern of the mask to the photoresist through the lens. The exposed portion of the photoresist undergoes a structural change. Either the exposed portion (for positive photoresist) or the masked portion (for negative photoresist) of the

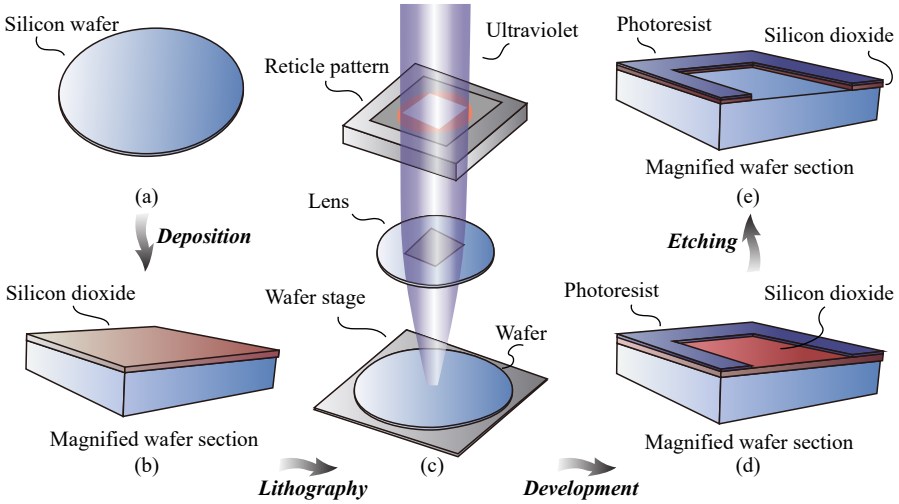


Figure 1.7 The essential processes in semiconductor manufacturing. (a) A silicon wafer. (b) A magnified wafer section after deposition. (c) Lithography process. (d) A magnified wafer section after development. (e) A magnified wafer section after etching. It is worth noting that a photoresist is coated on the wafer surface between (b) and (c), but this process is not drawn here for brevity.

photoresist can be dissolved by a developer, while the other portion remains on the wafer [103]. As a consequence, the reticle pattern is transferred to the photoresist, leaving the exposed portion of the SiO_2 layer ready for removal, and the remaining photoresist acting as an etching mask, as shown in Figure 1.7(d).

Etching is a process to selectively remove the material layers from the substrate surface. In this particular example, we seek to remove the exposed SiO_2 layer as efficiently as possible while retaining the photoresist, the covered SiO_2, and the underlying Si. This requirement is known as etching selectivity. After etching, the reticle pattern is transferred to the SiO_2 layer, as shown in Figure 1.7(e). Afterwards, the photoresist is tripped.

To produce a complex component like a central processing unit (CPU), these processes must be repeated multiple times with various materials, structures, and operating conditions. Deposition, lithography, and etching are the most crucial processes in semiconductor manufacturing [149]. Plasma is deeply involved in both deposition and etching, which are the primary applications of the technology described in this thesis. While there are other plasma processes in semiconductor manufacturing, such as ion implantation, they are not the focus of this thesis.

1.2.2 Plasma deposition

Although the primary focus is on plasma deposition, it is important to clarify that deposition can occur without plasma involvement. Thermal oxidation, for instance, is the simplest method to grow SiO_2 on Si because Si can be directly oxidized by oxygen (O_2) at high temperature (ranging from 800 to 1200 °C) [124], as shown in the reaction

$$\mathrm{Si(s) + O_2(g) \xrightarrow{\text{high temperature}} SiO_2(s).}$$

While thermal oxidation is highly efficient, its application scope is relatively limited. For example, it cannot be applied to the substrates that contain certain metals because the reaction temperature has exceeded the melting points of these metals [75].

Chemical vapor deposition (CVD) is a more versatile method. In CVD, gases or vapor (known as precursors) are decomposed, and solid materials are deposited onto the substrate surface. An example of CVD depositing SiO_2 utilizing silane (SiH_4) and O_2 is given as [124]

$$\mathrm{SiH_4(g) + O_2(g) \xrightarrow{430\,^\circ C,\,40\,Pa} SiO_2(s) + 2\,H_2(g).}$$

In this reaction, hydrogen (H_2) is produced as a by-product. Moreover, CVD could also produce higher-quality materials compared to thermal oxidation [101].

Plasma-enhanced chemical vapor deposition (PECVD) can lower the required temperature of CVD [124] and further extend to more precursors, materials, and structures [68]. Numerous different reactions happen in parallel in PECVD, making it exceedingly complex to describe [98, 116]. The reaction's essence is that the plasma provides high-energy electrons, which collide with precursor atoms and molecules, creating chemically reactive radicles by dissociation (an inelastic collision as introduced in the previous section), and enabling the reactions at a lower temperature [68]. The plasma ions can also increase the reaction rates. For example, the positive oxygen ions in the O_2 plasma can directly participate in the oxidation reactions and also help removing the undesired H atoms from SiH_4 [35].

The plasma ion energy is a critical factor in the PECVD process, as it affects the throughput and film quality [113]. It is intuitive to think that adequately increasing the ion energy can enhance the chemical reaction, thus obtaining a higher deposition rate [136,143]. However, too high energy can conversely lower the deposition rate [4]. Furthermore, the energetic ions can lead to defects and damages to the films [104]. It has been observed that low (10 to 30 eV) or intermediate (about 100 eV) ion energies generally have a positive effect on the film quality [114, 168].

With the shrinkage of IC devices, a more precise deposition method, named atomic layer deposition (ALD), comes into being, which allows growing thin films layer by layer of sub-nm scale [51]. It is advantageous in conformality and suitable

for growing high aspect ratio (HAR) structures [127]. It introduces two or more precursors sequentially to the substrate surface, where each precursor participates in the chemical reaction at a time and saturates itself. In the case of ALD of SiO_2 on Si, silicon tetrachloride ($SiCl_4$) and water (H_2O) can be used as precursors [155]. First, the Si surface is hydroxylated by water, where hydroxyl groups are formed on the surface [87]. Then the precursor $SiCl_4$ introduces the half-reaction A as

$$\text{s-Si}-\text{OH}\,(\text{s}) + \text{SiCl}_4(\text{g}) \longrightarrow \text{s-Si}-\text{O}-\text{Si}-\text{Cl}_3(\text{s}) + \text{HCl}\,(\text{g}),$$

where s-Y indicates the surface with surface groups Y [92]. After the necessary purge, the second precursor H_2O (also named by co-reactant) introduces the half-reaction B as

$$\text{s-Si}-\text{Cl}\,(\text{s}) + \text{H}_2\text{O}\,(\text{g}) \longrightarrow \text{s-Si}-\text{OH}\,(\text{s}) + \text{HCl}\,(\text{g}).$$

Consequently, a monolayer of SiO_2 is grown. With cyclic reactions, SiO_2 can be grown layer by layer. Such reaction requires a temperature of 327 to 407 °C if without a catalyst [155].

It should not be surprising that plasma-enhanced atomic layer deposition (PEALD) can lower the required temperature [140] and expand to more precursors [171]. Apart from enhancing chemical reactions, recent researches have shown that the plasma ion energy can serve as an additional control degree of freedom to tailor the material properties in PEALD [6, 52, 138]. Observations suggest that increasing ion energy below certain thresholds can improve properties, while exceeding them can cause degradation [53]. The optimal ion energy varies significantly depending on the materials and processes.

In this thesis, plasma deposition mainly refers to PECVD and PEALD. While there are other deposition methods, such as sputtering, that also utilize plasma, they are not discussed here due to significant differences in their reactors [59].

1.2.3 Plasma etching

Speaking of etching, electrical engineers might be familiar with etching a printed circuit board (PCB), in which a solution like ferric chloride ($FeCl_3$) is used to remove the unwanted copper. This type of etching with liquid chemicals or etchants is referred to as wet etching. In contrast, plasma etching is considered dry etching, where material is removed by exposing the substrate to plasmas, which generally has better anisotropy than wet etching [126].

The most straightforward plasma etching method is sputtering etching, which uses high-energy ions to bombard the substrate and knock off the surface atoms. This etching method only involves physical reactions. Depending on the applications, the energy of the bombarding ions can range from 50 to 2000 eV [38].

Reactive ion etching (RIE) utilizes both energetic ions and gas phase reactants, resulting in a significantly higher reaction efficiency than sputtering etching or pure chemical reactions [28]. It is now the most widely used etching method in semiconductor manufacturing [38]. The reaction mechanism is complex [81], but similar to PECVD, plasma ions and electrons generate chemically reactive radicles, thus accelerating the chemical reactions. Besides, the normal direction of the ion bombardment enhances anisotropy [39].

Similar to plasma deposition, RIE also critically demands a precise plasma ion energy. Ions with inefficient energy can yield a low etch rate and poorer anisotropy [29, 166]. However, ions with excessively high energy can impair the etching mask [38], degrade etching selectivity [175], and damage the structure [90].

Atomic layer etching (ALE) can be regarded as the reversed process of ALD, which can bring material removal to atomic resolution as well [127]. Although ALE can occur with only spontaneous chemical reactions, it is much more common to have energetic species as assistance [105]. For instance, plasma-enhanced atomic layer etching (PEALE) uses energetic ions for material removal in the second half-reaction.

In PEALE, the substrate surface is first exposed to the precursors to weaken the binding energy between the surface and bulk atoms of the substrate [51]. This step aims to modify the surface so that the surface atoms can be removed without affecting the underlying material [85]. Afterward, energetic plasma ions bombard the modified substrate surface, break the bonds of the surface layer of atoms, and release the volatile by-products [163].

As previously mentioned, the binding energy between the surface and bulk atoms of the substrate is lowered in the first half-reaction. The energy of bombarding ions should at least be higher than the lowered binding energy to effectively and completely remove the modified surface. To achieve high selectivity, the bombarding ions should avoid sputtering the underlying bulk. Therefore, the ion energy should not exceed the binding energy between the bulk atoms. Consequently, the required ion energy is located in a range known as the ALE window [127]. This energy window is dependent on the material and process. Under certain circumstances, this energy window can be as narrow as 10 eV such as the plasma ALE of germanium (Ge) using chlorine (Cl_2) plasma for surface modification [86].

In summary, this section introduces three different plasma etching methods: sputtering etching, RIE, and PEALE. Although other plasma etching methods exist, they are omitted for the sake of brevity.

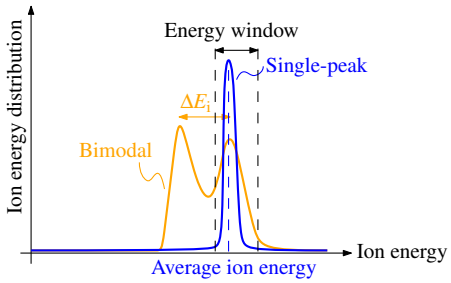


Figure 1.8 Single-peak and bimodal ion energy distribution. Here ΔE_i represents the difference of the ion energy peaks.

1.2.4 Ion energy control

As demonstrated in this section, ion energy plays a predominant role in plasma deposition and etching. It not only affects the reaction rate but also has a crucial impact on the process quality. In most processes, the energetic ions are desired to fall into a specific energy window within a lower and upper bound. This window varies tremendously with different materials, applications, and process recipes and can be very narrow. Additionally, the required ion energy can span a wide range of magnitudes, from typically tens of eV in plasma deposition to thousands of eV in sputtering etching. Such requirements can be translated into a single-peak IED located in an energy window with controllable average ion energy, as shown in Figure 1.8. For comparison, Figure 1.8 also depicts a bimodal IED, which is the most common case in plasma processing.

In a traditional capacitively coupled plasma (CCP), as shown in Figure 1.2, a single power source is used to control the ion density, ion flux, ion energy, and other plasma properties, which can easily lead to plasma nonuniformity [135, 148] and makes it difficult to accurately control the ion energy independently of ion flux [2]. To address this issue, dual-frequency CCPs were invented [64, 65]. They use a high-frequency RF source to mainly control ion flux and an RF source of a lower frequency to control ion energy separately. Dual-frequency CCP offer better plasma uniformity over large surface areas compared to single-frequency CCPs [13]. However, the coupling effect of the two RF sources can cause issues such as substrate damage or reduced etching rate [102].

Compared to CCPs, inductively coupled plasmas (ICPs) further decouple the ion energy and flux. ICPs also enjoy the benefit of higher plasma density. A schematic representation of a typical ICP is depicted in Figure 1.9. In this ICP, the RF power is inductively coupled to the plasma across a dielectric window, which is used to excite and sustain the plasma and mainly determines the plasma density and ion flux. The

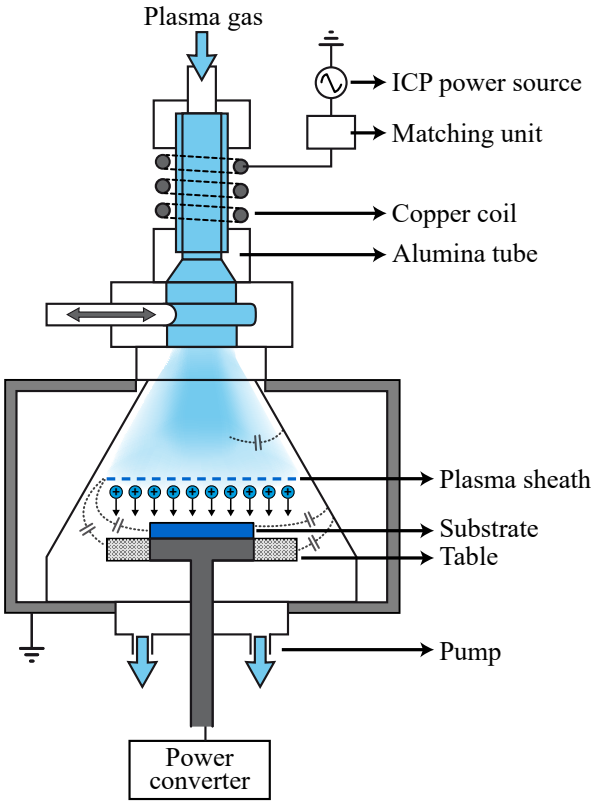


Figure 1.9 A typical setup of an inductively coupled plasma reactor. The solid part of the table is covered by the substrate, while the gridded part is directly exposed to the plasma.

substrate is placed on the conductive table for plasma processing. A power converter is connected to the table, biasing the substrate surface potential with specific voltage waveforms and controlling the ion energy. This power converter is also called bias converter, and the output waveform of the bias converter is referred to as the bias waveform in this thesis.

For a conductive substrate, such as a metal, the bias converter can deliver a negative dc voltage directly. The substrate surface potential is equal to the output voltage of the bias converter, thus building a high-voltage sheath (as modeled in the previous section) and accelerating ions toward the substrate surface. By adjusting the output dc value, the ion energy on the substrate can be controlled as desired. However, for a dielectric substrate, such as the most commonly used Si substrate, the substrate surface potential does not exactly equate to the output voltage of the bias converter due

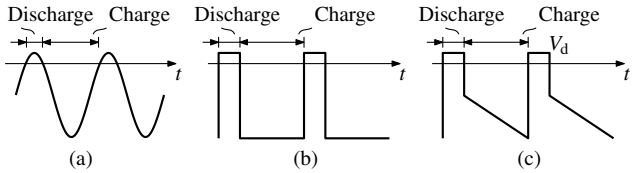


Figure 1.10 (a) RF biasing voltage waveform. (b) Pulse-shaped biasing voltage waveform. (c) Tailored waveform biasing voltage waveform. Here V_d represents a positive discharge voltage.

to the equivalent capacitance of the dielectric substrate [10]. If a negative dc voltage is suddenly applied to the table, the substrate surface potential initially becomes negative. The bombarding ions then continuously charge the equivalent capacitance and increase the substrate surface potential until it reaches zero. Therefore, a simple negative dc bias voltage cannot control the ion energy for dielectric substrates.

Various biasing techniques for dielectric substrates in ICPs have been studied [44, 139,141], the most typical ones including RF biasing [3,138], pulse-shaped biasing [9, 153,166], and tailored waveform biasing [54,55,70,96,108,111,174,176], the voltage waveforms of which are shown in Figure 1.10(a), (b) and (c), respectively. In all three techniques, the negative parts of the bias waveforms are utilized to create a negative voltage potential on the substrate surface to enhance ion energy. The bombarding ions are charging the substrate capacitance during this time. Therefore, to prevent overvoltage on the substrate, a short positive voltage is periodically applied to attract the electrons and reset the voltage potential, *i.e.,* discharging the substrate.

RF biasing generates a sinusoidal voltage potential on the substrate surface, resulting in a broad and bimodal IED as depicted in Figure 1.8 [119,159], which is not desirable in plasma processing. While increasing the RF biasing frequency can narrow the IED, it is limited by the ion mass and less effective for lighter ions, such as hydrogen. Additionally, a sufficiently large biasing frequency makes the RF wavelength comparable to the substrate dimension, which can cause severe nonuniformities [3].

Pulse-shaped biasing can deliver a narrow single-peak IED, as depicted Figure 1.8 under specific conditions, especially for a dielectric substrate with large capacitance. However, if the substrate capacitance is small, the IED can become heavily distorted since a small substrate capacitance leads to a considerable voltage potential rise due to the charging effect, thus resulting in a broad IED [96]. Although increasing pulse-shaped biasing frequency can reduce this charging effect as well, similar drawbacks occur as with increasing the RF biasing frequency.

In contrast to pulse-shaped biasing, tailored waveform biasing uses a negative voltage slope to compensate for the charging effect. The voltage slope rate should

be well-tuned, and its value is determined by the properties of the substrate and the ion flux. Under this circumstance, the voltage potential of the substrate bottom linearly decreases, keeping the substrate surface potential quasi-constant. Tailored waveform biasing requires a significantly reduced repetition frequency compared to RF and pulse-shaped biasing. The capability of accurate ion energy control makes tailored waveform biasing well-suited for highly-selective plasma processing. It has been proven promising in both PECVD [111,176] and PEALE [54]. This thesis focuses on its derivation and generation.

1.3 Research objectives

The primary objective of this research is to develop a power electronics system for plasma processing with tailored waveform biasing. This objective leads to the following major research questions.

• *What is the equivalent electric circuit model of plasma processing?* To build a power electronics system, the load should be primarily defined, and its EEC model is required for circuit simulation and design. In this application, the load is the complex plasma processing, which is divided into multiple phases in a fundamental period, and its electrical response is peculiar during each phase. The EEC model should reproduce its electrical responses and essential plasma properties, such as IED. Moreover, the parameters of the model should be identified.

• *How does the tailored waveform profile influence the ion energy?* The tailored waveform profile contains a negative slope and a positive pulse. Both the slope rate and the pulse magnitude affect the ion energy. It is known that the slope rate determines the width of the IED. For each operating condition, there is an optimal slope rate leading to the narrowest IED. However, finding this optimal slope rate requires repetitive manual tuning. An automatic method to find the optimal slope rate is desired. The pulse magnitude determines ion energy. However, whether the entire pulse or just part of the pulse takes effect is unknown. Furthermore, how the pulse duty cycle influences the process remains unsettled. These issues should be related to the EEC model of plasma processing.

• *What topology and control strategy should be used for the bias converter?* On the one hand, the bias converter should be able to generate various voltage pulses with fast rising and falling edges. On the other hand, it can deliver a linear voltage slope of different slope rates. The uniqueness of the waveform profile calls for a special topology for the bias converter. Moreover, since the load is capacitive, it forms an LC network together with the inductance in the loop. Such an LC network could cause severe resonance, especially during the voltage rising and falling edge of the

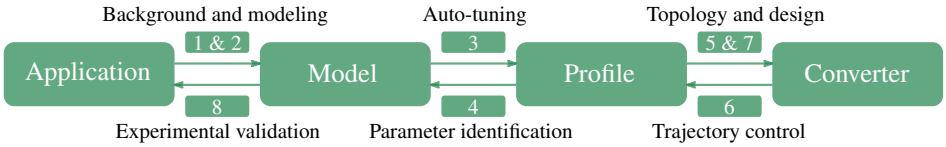


Figure 1.11 The organization of this thesis. The digits in the figure represent the chapter numbers.

voltage pulse. Therefore, it also demands a smart control strategy to damp out or prevent the resonance.

1.4 Organization of this thesis

The organization of this thesis is illustrated in Figure 1.11, which depicts the connections between the various research questions and corresponding chapters.

Chapter 1 provides background information on plasma physics and plasma processing applications. Based on the plasma physics, Chapter 2 examines the limitations of the traditional EEC model of plasma processing and presents an improved model that enables the explicit solution of the tailored waveform profile. The factors that determine the optimal slope rate and the effect of the voltage pulse are analyzed in details in this chapter.

In Chapter 3, an auto-tuning method is developed, which can automatically find the optimal slope rate using only the voltage and current measurements on the bias converter side. Besides, the system influence of the RFEA is also elaborated on.

Based on the proposed EEC model, the magnitude of the voltage pulse and the slope rate of the tailored waveform profile can be derived. In return, by applying different waveform profiles, the parameters of the EEC model can be identified with the help of voltage and current measurements. This parameter identification method is introduced in Chapter 4.

With the EEC model and the waveform profile, the topology of the bias converter can be derived. Chapter 5 analyzes and compares two basic bias converter concepts, the voltage source converter and the hybrid source converter, and introduces a multilevel tailored waveform concept. With a filter inductor, the multilevel tailored waveform can be smoothed into the required tailored waveform. The value of the filter inductance is solved analytically to ensure a qualified ion energy distribution. Based on this concept, a multilevel converter topology is developed to generate the waveform, which consists of a T-type converter and a series of cascaded H-bridge submodules.

Chapter 6 presents a trajectory control method to damp out the resonance that may be triggered during the rising and falling edges of the pulse due to the LC network formed by the capacitive load and the filter inductance. It uses multiple intermediate voltages to damp out the resonance, which is non-dissipative theoretically. The time duration of each voltage level can be solved analytically based on the trajectory control method, and the required waveform profile can be generated.

With the trajectory control method, the operating conditions of the switching devices in each submodule of the bias converter, including the switching frequency, voltage, and current, can be obtained. These operating conditions are determined by the selection of the time step of the multilevel tailored waveform. Chapter 7 introduces a switching transient model that can solve the switching loss and time analytically under different operating conditions based purely on datasheet parameters. By knowing the exact limits of the devices together with an accurate estimation of the device stress, the system can be used up to their full capacities.

Chapter 8 presents the design of a prototype to validate the analysis provided in the previous chapters. Specially, a passive load is built to emulate the electrical responses of plasma processing, as modeled in the previous chapters. The experimental results confirm the analysis on the model, profile, and converter.

Finally, in Chapter 9, conclusions are drawn, recommendations are given for the future research, and the scientific contributions are summarized.

CHAPTER 2

Model of plasma processing

THE tailored waveforms introduced in the previous chapter are delivered by a bias converter. Traditionally, class-A linear amplifiers have been adopted for this purpose [179], but they are typically energy inefficient. In addition, a tuned matching network is necessary to match the impedance of the linear amplifier and the plasma reactor [138].

Recently, variants of switched-mode power converters have been applied to generate the tailored waveform, which are significantly more energy-efficient than linear amplifiers [5, 17, 18, 40, 41, 48, 49, 91, 123, 187]. These converters also advantageously eliminate the need for a matching network, and they can actively and flexibly generate the required bias waveforms with controllable pulse magnitude and voltage slope rate.

The SMPCs offer significant convenience and flexibility in tailored waveform biasing. However, for electrical engineers, an EEC model of plasma processing is required to conduct circuit simulations and optimize electrical design. For plasma physicists, such a model is also desired to combine the simulation of the bias converter and plasma processing to simulate the IED and optimize the bias waveform. A complete EEC model of plasma processing could enable this combined simulation at the circuit level, which would significantly reduce computation time compared to traditional plasma simulation methods like PIC.

This chapter is based on [183, 186].

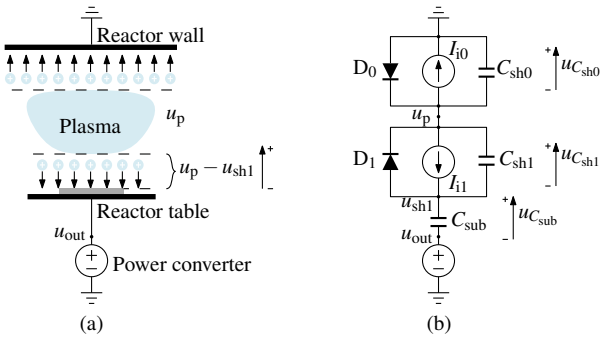


Figure 2.1 (a) An asymmetric parallel plate system representation of the ICP plasma reactor. (b) The traditional EEC model of the ICP plasma reactor. The plasma sheath between the reactor wall and the plasma is modeled by a diode D_0, a current source I_{i0}, and a sheath capacitance C_{sh0} in parallel. The plasma sheath between the substrate and the plasma is modeled by a diode D_1, a current source I_{i1}, and a sheath capacitance C_{sh1} in parallel.

Although some models have been derived in previous researches, most of them are used for RF biasing [2, 34, 60, 108, 138, 147] or a steady-state simplification of tailored waveform biasing [18, 184, 187]. These models cannot be directly used for transient analysis in tailored waveform biasing, as they do not accurately include the discharge process. In [186], a modified model is proposed that emulates the discharge process using a virtual sheath reset circuit. While this modified model can roughly represent the charge and discharge processes and can be used for electric simulation, it significantly increases the complexity of the circuit.

This chapter aims to analyze the limitations of the existing models and propose an improved EEC model that satisfies the requirements of electric waveform and IED simulation at the circuit level.

2.1 Equivalent electric circuit model

2.1.1 Traditional equivalent electric circuit model

As introduced in Section 1.1.2, a parallel plate system is the elementary construction of a plasma system. In a typical ICP reactor, the bulk plasma is confronted with two major surfaces: the grounded reactor wall and the reactor table. The reactor table is electrically connected to the bias converter. The area of the reactor wall is larger than that of the table, so the plasma reactor can be simplified as an asymmetrical parallel

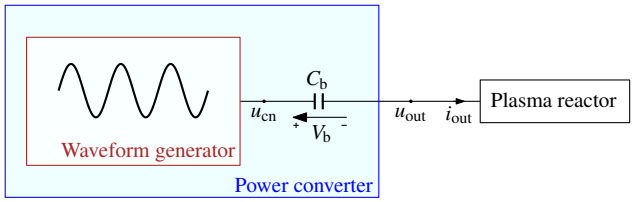


Figure 2.2 A power converter which is coupled with the plasma reactor with a blocking capacitor. i_{out} represents the output current of the power converter.

plate system, as depicted in Figure 2.1(a). In most cases, the substrate is dielectric, as indicated by the gray area in the figure.

The traditional EEC model focuses on RF biasing as described in [2,60,93,94,138,147], which can be generalized by the EEC model shown in Figure 2.1(b). In this model, two sheaths are formed between the plasma and reactor wall, and the plasma and substrate, respectively. It must be stressed that this model is used to describe the waveform biasing, while the plasma generation in ICP is not modeled and regarded as fully decoupled with the waveform biasing. As demonstrated in Section 1.1.2, the plasma sheath is analogous to a nonideal diode with parasitic capacitance. Therefore, each sheath is modeled by a diode, a sheath capacitor, and a constant current source in parallel. The current source accounts for the equivalent current generated by bombarding ions in a high-voltage sheath. The dielectric substrate is modeled by a capacitor C_{sub}, and u_{sh1} represents the substrate surface potential.

In RF biasing, a blocking capacitor is usually used to couple the power converter to the table, as shown in Figure 2.2. Thereby the power converter can be assumed to consist of a waveform generator and a blocking capacitor C_b. The waveform generator delivers the voltage waveforms of desired shapes. In RF biasing, this waveform generator delivers a voltage sinusoidal u_{cn} given by

$$u_{cn} = V_{rf} \sin(2\pi f_{rf} t), \tag{2.1}$$

where V_{rf} is the amplitude of the RF voltage, and f_{rf} is the RF frequency.

A self-biased blocking voltage V_b is formed over C_b, and the output voltage u_{out} is shifted to a more negative value with respect to u_{cn}. The self-biased voltage V_b arises from the initial unbalance between the inflow and outflow currents. Once the steady state is reached, the net current flowing through the blocking capacitor is zero in each fundamental period, and V_b can be considered constant if C_b is sufficiently large [160]. The bias waveform u_{out} is the voltage waveform after the blocking capacitor, and it can be described by

$$u_{out} = V_{rf} \sin(2\pi f_{rf} t) - V_b. \tag{2.2}$$

In the traditional model, the bombarding ions enter the sheath with an initial energy equal to $eu_{\mathrm{p}} = -eu_{C_{\mathrm{sh0}}}$. For simplicity, it can be assumed for now that the sheath thickness is negligible so that the ion transit time in the sheath is much shorter than the RF period. As a result, the extra energy that ions obtained in the sheath due to the acceleration in the electric field is equal to $eu_{C_{\mathrm{sh1}}}$, which is determined by the instantaneous value of $u_{C_{\mathrm{sh1}}}$ at the moment when ions enter the sheath.

During the steady state in RF biasing, C_{sh0}, C_{sh1}, and C_{sub} constitute a capacitive voltage divider. As a result, the voltages over these capacitors are determined by

$$\begin{pmatrix} u_{C_{\mathrm{sh0}}} \\ u_{C_{\mathrm{sh1}}} \\ u_{C_{\mathrm{sub}}} \end{pmatrix} = -\begin{pmatrix} \frac{1}{C_{\mathrm{sh0}}} \\ \frac{1}{C_{\mathrm{sh1}}} \\ \frac{1}{C_{\mathrm{sub}}} \end{pmatrix} \cdot \frac{V_{\mathrm{rf}} \sin\left(2\pi f_{\mathrm{rf}} t\right)}{\frac{1}{C_{\mathrm{sh0}}} + \frac{1}{C_{\mathrm{sh1}}} + \frac{1}{C_{\mathrm{sub}}}} + \begin{pmatrix} V_0 \\ V_1 \\ V_{\mathrm{sub}} \end{pmatrix}, \tag{2.3}$$

where V_0, V_1, and V_{sub} are the dc offset voltages over C_{sh0}, C_{sh1}, and C_{sub}, respectively. The values of V_0, V_1, and V_{sub} are determined by the bias waveform and the capacitance values. According to Kirchhoff's voltage law, they are governed by

$$V_0 + V_1 + V_{\mathrm{sub}} = V_{\mathrm{b}}. \tag{2.4}$$

Since C_{sh0} cannot be positive and C_{sh1} cannot be negative due to the diodes, V_0 and V_1 should satisfy the constraints:

$$\begin{cases} V_0 \le -\frac{\frac{1}{C_{\mathrm{sh0}}}}{\frac{1}{C_{\mathrm{sh0}}} + \frac{1}{C_{\mathrm{sh1}}} + \frac{1}{C_{\mathrm{sub}}}} V_{\mathrm{rf}} \\ V_1 \ge \frac{\frac{1}{C_{\mathrm{sh1}}}}{\frac{1}{C_{\mathrm{sh0}}} + \frac{1}{C_{\mathrm{sh1}}} + \frac{1}{C_{\mathrm{sub}}}} V_{\mathrm{rf}} \end{cases}. \tag{2.5}$$

The ions bombard the substrate surface with an energy equal to

$$E_{\mathrm{i}}(t) = e\left(u_{\mathrm{p}}(t) + u_{C_{\mathrm{sh1}}}(t)\right), \tag{2.6}$$

which can be described by

$$E_{\mathrm{i}}(t) = \frac{\frac{1}{C_{\mathrm{sh0}}} - \frac{1}{C_{\mathrm{sh1}}}}{\frac{1}{C_{\mathrm{sh0}}} + \frac{1}{C_{\mathrm{sh1}}} + \frac{1}{C_{\mathrm{sub}}}} V_{\mathrm{rf}} \sin\left(2\pi f_{\mathrm{rf}} t\right) + V_1 - V_0. \tag{2.7}$$

Since the asymmetrical sheath yields $C_{\mathrm{sh0}} \neq C_{\mathrm{sh1}}$ [147], the bombarding ions have an average energy equal to $e\left(V_1 - V_0\right)$ and an energy variance ΔE_{i} equal to

$$\Delta E_{\mathrm{i}} = eV_{\mathrm{rf}} \left| \frac{\frac{1}{C_{\mathrm{sh0}}} - \frac{1}{C_{\mathrm{sh1}}}}{\frac{1}{C_{\mathrm{sh0}}} + \frac{1}{C_{\mathrm{sh1}}} + \frac{1}{C_{\mathrm{sub}}}} \right|. \tag{2.8}$$

This results in a bimodal IED as shown in Figure 1.8.

In practice, the ion transition in the sheath takes time, since the thickness of the high-voltage sheath is much larger than a Debye length and ions have a finite velocity, as introduced in the previous chapter. Therefore, the extra energy that ions obtain in the sheath is the average of $eu_{C_{\mathrm{sh1}}}(t)$ over the ion transit time. This effect acts as an energy damper and can reduce the width of the IED, leading to a smaller ΔE_{i}. Furthermore, it also explains why higher f_{rf} induces narrower IED, as introduced in Section 1.2.4, as ions can perceive an average voltage over multiple fundamental periods instead of a small portion of the RF waveform. Therefore, f_{rf} is typically in the megahertz magnitude range [158].

The traditional EEC model is effective in explaining RF biasing but is inadequate for tailored waveform biasing. In tailored waveform biasing, bombarding ions are accumulated on the substrate surface and charging C_{sub} when a negative voltage slope is applied to the table, as illustrated in Figure 1.10(c). To prevent overvoltage, C_{sub} needs to be periodically discharged by a positive voltage pulse. During the positive voltage pulse, fast-moving electrons should be attracted to rapidly discharge the capacitors. However, in the traditional EEC model, the capacitors can only be discharged through the current sources I_{i0} and I_{i1}. As the ion current is significantly smaller than the electron current, this results in a slow discharge process. Furthermore, the discharge electron current decays exponentially, as depicted in [96], which can not be realized by the constant current sources.

Besides, in practice, after applying the positive discharge voltage denoted by V_{d} in Figure 1.10(c), and when the circuit reaches a steady state, the voltage of C_{sub} should be fully discharged to zero, resulting in a substrate surface potential of V_{d}. Consequently, the substrate surface has a higher voltage potential than the grounded reactor wall. Since plasma potential u_{p} is always determined by the surface with higher voltage potential as introduced in Section 1.1.3, according to (1.24), it is then determined by the substrate surface as

$$u_{\mathrm{p}} = V_{\mathrm{d}} + V_{\mathrm{p}}. \tag{2.9}$$

The voltage of C_{sh1} should represent the voltage over this sheath, and thus it is nearly zero as V_{p} is typically small [2].

However, due to the capacitive voltage divider formed by C_{sh0}, C_{sh1} and C_{sub} as shown in Figure 2.1(b), the capacitors cannot be entirely discharged when $u_{\mathrm{out}} = V_{\mathrm{d}}$, as per Kirchhoff's voltage law. Instead, the voltage drop over C_{sub} remains positive during discharge, deviating from practical applications.

In summary, the traditional EEC model of the plasma reactor is suitable for RF biasing, but it is not applicable for tailored waveform biasing. Therefore, a different EEC is necessary for this biasing technique.

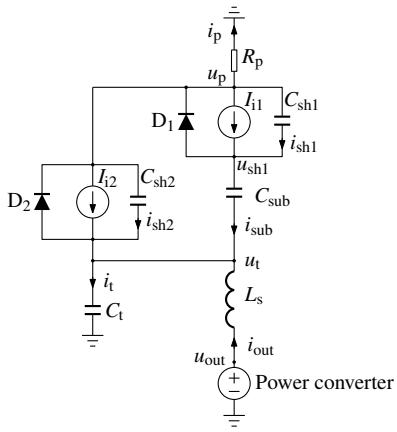


Figure 2.3 The improved EEC model of the plasma reactor for waveform biasing.

2.1.2 Improved equivalent electric circuit model

An improved EEC model, depicted in Figure 2.3, has been proposed. In comparison to the traditional model, the sheath between the plasma and reactor wall is omitted. In fact, during the slope portion of tailored waveform biasing, the substrate surface has a negative voltage potential while the reactor wall is grounded. Under these conditions, a high-voltage sheath is formed between the plasma and the substrate surface, while a Debye sheath is formed between the plasma and the reactor wall. Theoretically, there should be no net current going through or voltage change over the Debye sheath during this time. Therefore, this Debye sheath is not of interest and can be omitted for simplicity. Such a simplification is also frequently used in previous research, such as in [34, 46]. If this sheath is not neglected, the EEC model can be much more complex [186]. Meanwhile, a resistor R_p represents the bulk plasma and provide a fast discharge path that exponentially decays.

Hypothetically, an extra sheath, called the table sheath, is formed between the plasma and the exposed part of the table (as depicted by the gridded part in Figure 1.9), comprising a sheath diode D_2, an ion current I_{i2}, and a sheath capacitor C_{sh2}. This table sheath is rarely discussed in previous research, but it is essential, especially with the existence of diode D_2. Diode D_2 provides an additional discharge path so that C_{sh1} and C_{sub} can be fully discharged when the positive discharge voltage V_d is applied, and D_2 is conducting. The necessity of this table sheath is proven in the following sections.

In addition, parasitic capacitors exist between the table and the reactor wall, as well as between the substrate and the reactor wall, as shown in Figure 1.9. These capacitors are modeled as a lumped table capacitor C_t. L_s represents the stray

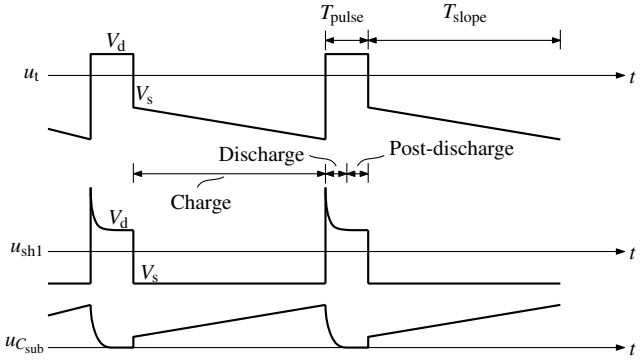


Figure 2.4 The typical waveforms of u_{t}, u_{sh1}, and $u_{C_{\text{sub}}}$. Here T_{pulse} and T_{slope} represent the time duration of the voltage pulse and slope, respectively. V_{s} is the desired start voltage of the voltage slope.

inductance in the power converter and the table connection.

The proposed model aims to replicate the transient electrical behavior in plasma processing. In a fundamental period, tailored waveform biasing can be divided into three individual phases as shown in Figure 2.4, namely the charge phase, the discharge phase, and the post-discharge phase.

The part of the tailored waveform where the table is negatively biased is defined as the charge phase since ions are accumulating on the substrate surface and charging the substrate capacitor during this time. When the discharge voltage V_{d} is applied to the table, the capacitors are discharged within a short time, defined as the discharge phase. As the discharge time is unknown, V_{d} should be held for a little longer after the capacitors are guaranteed to be fully discharged, defined by the post-discharge phase. Each phase is analyzed in detail in this section.

Essentially, in tailored waveform biasing, u_{t} should be the so-called tailored waveform, and the target of the bias converter is to generate a voltage waveform u_{out} to obtain the desired u_{t}. In fact, u_{sh1} is the property we want to control.

Charge phase

To achieve high-selectivity plasma processing, it is necessary to maintain the ion energy within a specific narrow window. Therefore, u_{sh1} is desired to remain at a constant negative value. As ions accumulate and charge the substrate, this phase is designated as the "charge phase". From the EEC model, u_{sh1} is determined by

$$C_{\text{sub}} \frac{\mathrm{d}\left(u_{\text{sh1}} - u_{\text{t}}\right)}{\mathrm{d}t} = I_{\text{i1}} + C_{\text{sh1}} \frac{\mathrm{d}\left(u_{\text{p}} - u_{\text{sh1}}\right)}{\mathrm{d}t}. \tag{2.10}$$

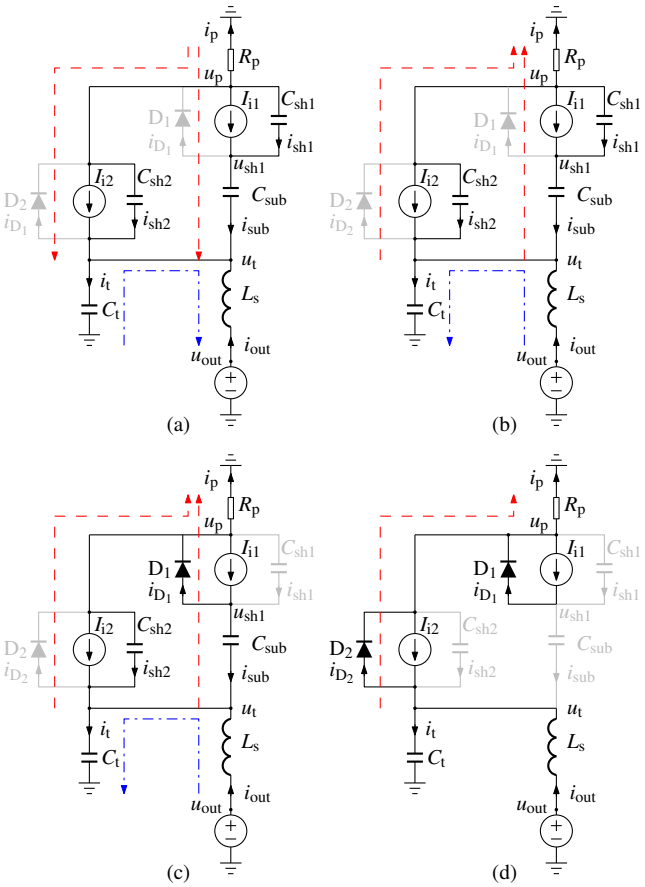


Figure 2.5 The equivalent circuit of plasma processing in tailored waveform biasing during (a) the charge phase, (b) the discharge phase when $u_{C_{sh1}}$ has not been fully discharged, (c) the discharge phase when $u_{C_{sh1}}$ has been fully discharged, and (d) the post-discharge phase when all the capacitors have been fully discharged. The dashed arrows indicate the net current direction through corresponding sheath. The dash doted arrows indicate the current direction through C_t. Here i_{D_1}, i_{D_2}, i_p, i_{sh1}, i_{sh2}, i_{sub}, and i_t represent the current flows through D_1, D_2, R_p, C_{sh1}, C_{sh2}, C_{sub}, and C_t, respectively.

During the charge phase when the reactor table is negatively biased, the grounded reactor wall has a higher voltage potential than the table, which determines the plasma potential. Therefore, in practice, the plasma has a positive potential V_p governed by (1.24). Since this voltage is relatively small compared to the bias voltage, it is temporarily neglected here for simplicity. In the model, the plasma potential u_p is determined by

$$u_\mathrm{p} = R_\mathrm{p} i_\mathrm{p} = -R_\mathrm{p} \left(I_\mathrm{i1} + I_\mathrm{i2} + i_\mathrm{sh1} + i_\mathrm{sh2} \right), \tag{2.11}$$

which yields a negative value during the charge phase. Therefore, R_p should be sufficiently small during this phase to ensure that $u_\mathrm{p} \approx 0$ to avoid a negative plasma potential.

I_i1 is causing charge accumulation on C_sub, which needs to be compensated for. Therefore, according to (2.10), maintaining a constant u_sh1 requires a voltage slope on u_t, as defined by

$$\frac{\mathrm{d}u_\mathrm{t}}{\mathrm{d}t} = -\frac{I_\mathrm{i1}}{C_\mathrm{sub}}. \tag{2.12}$$

In other words, to achieve a constant current I_i1, u_t should linearly decrease with a slope rate of $-I_\mathrm{i1} C_\mathrm{sub}^{-1}$ to precisely compensate for the ion charge effect, resulting in a constant u_t and ion energy [9]. During the charge phase, a more negative voltage slope leads to a falling u_t (over-compensation), whereas a less negative slope causes a rising u_t (under-compensation).

Assuming the duration of the voltage slope is T_slope (as labeled in Figure 2.4), the magnitude of the voltage change ΔV during the charge phase can be determined by

$$\Delta V = \frac{\mathrm{d}u_\mathrm{t}}{\mathrm{d}t} T_\mathrm{slope} = -\frac{I_\mathrm{i1}}{C_\mathrm{sub}} T_\mathrm{slope}. \tag{2.13}$$

In contrast, in pulse-shaped biasing, as depicted in Figure 1.10, the charge effect is not compensated for, so the substrate surface potential rises by $|\Delta V|$ during the charge phase. A small C_sub or a large charge time (low repetition frequency) could lead to a significant voltage rise and a broad IED.

In this thesis, the condition that (2.12) is achieved is defined as the optimal operating point. At the optimal operating point, the output current can be derived as

$$i_\mathrm{out} = -\frac{C_\mathrm{sub} + C_\mathrm{t} + C_\mathrm{sh2}}{C_\mathrm{sub}} I_\mathrm{i1} - I_\mathrm{i2}. \tag{2.14}$$

The EEC model in Figure 2.3 can be simplified during the charge phase as shown in Figure 2.5(a).

Discharge phase

Because I_{i1} is continuously charging C_{sub} during the charge phase, it becomes necessary to periodically discharge C_{sub} to prevent overvoltage on the substrate. To achieve this, a positive voltage pulse is applied to the table, causing a restructuring and reformation of both the substrate and table sheath. The capacitors C_{sh1}, C_{sh2}, and C_{sub} are discharged by attracting the electrons, which is realized by an RC discharge through resistor R_p in the circuit model.

Initially, $u_{C_{sh1}}$ is positive, thus D_1 is blocking. C_{sub} is discharged through C_{sh1}. The equivalent circuit representing the moment when C_{sh1} is not fully discharged is shown in Figure 2.5(b).

Once C_{sh1} is fully discharged, $u_{C_{sh1}}$ becomes zero, and D_1 starts conducting. C_{sub} is then discharged through D_1. The ion current I_{i1} entirely flows through D_1. The equivalent circuit representing the moment after C_{sh1} is fully discharged is shown in Figure 2.5(c). Since C_{sub} and C_{sh2} are in parallel, both capacitors should be fully discharged simultaneously.

The RC discharge process represents the sheath collapsing. The discharge current in the loop decays exponentially. Typically, this process occurs within a short time, up to hundreds of nanoseconds [96].

Post-discharge phase

Once C_{sh2} and C_{sub} are fully discharged, the voltages across C_{sh1}, C_{sh2}, and C_{sub} are all zero, and D_2 is conducting. In this case, the plasma potential u_p is then clamped to the discharge voltage V_d, and the ion current I_{i2} is entirely flowing through D_2. The equivalent circuit for this moment is presented in Figure 2.5(d).

The post-discharge phase is preferably short to ensure that the ion energy is well-defined during most of the duration of the waveform. On the other hand, the post-discharge phase is a degree of freedom to adjust the fundamental period of the bias waveform. The duration of the charge phase T_{slope} is rather fixed because ΔV is limited by the voltage rating of the power converter. The duration of the discharge phase is determined by the plasma properties and the operating condition and is typically very short, so it is uncontrollable. By manipulating the duration of the post-discharge phase, the fundamental period of the bias waveform (and its frequency) can be flexibly regulated. The total time duration of the discharge and the post-discharge phases is denoted by T_{pulse}, as shown in Figure 2.4.

Moreover, the duty cycle of the post-discharge phase can be utilized as a degree of freedom to regulate the discharge voltage V_d if the power converter is coupled to the reactor table via a blocking capacitor as depicted in Figure 2.2. In steady-state

conditions, the output current is determined by

$$\langle i_{\text{out}} \rangle = \langle i_{\text{t}} \rangle - \langle i_{\text{sub}} \rangle - \langle i_{\text{sh2}} \rangle - \langle I_{\text{i2}} \rangle + \langle i_{\text{D}_2} \rangle, \tag{2.15}$$

where $\langle \cdot \rangle$ represents the average value in a fundamental period. The net currents through all the capacitors are zero during the steady state due to periodic voltages. Therefore, $\langle i_{\text{t}} \rangle$, $\langle i_{\text{sub}} \rangle$, and $\langle i_{\text{sh2}} \rangle$ are all equal to zero. During the charge and discharge phases, $\langle i_{\text{D}_2} \rangle$ is zero. During the post-discharge phase, it is described by

$$i_{\text{D}_2} = \frac{V_{\text{d}}}{R_{\text{p}}} + I_{\text{i2}}. \tag{2.16}$$

During the steady state, the net output current should also be balanced due to the blocking capacitor, meaning that $\langle i_{\text{out}} \rangle$ should be equal to zero. This leads to

$$\langle i_{\text{D}_2} \rangle = I_{\text{i2}} \approx \left(\frac{V_{\text{d}}}{R_{\text{p}}} + I_{\text{i2}} \right) \frac{T_{\text{pulse}}}{T_{\text{pulse}} + T_{\text{slope}}}. \tag{2.17}$$

Solving (2.17) for V_{d} gives

$$V_{\text{d}} \approx \frac{T_{\text{slope}} I_{\text{i2}} R_{\text{p}}}{T_{\text{pulse}}}, \tag{2.18}$$

where V_{d} is the output voltage u_{out} after the blocking capacitor, as shown in Figure 2.2. V_{d} results from the actively controlled voltage u_{cn} from the waveform generator subtracting the self-biased blocking voltage V_{b}. As indicated by (2.18), V_{d} can be modulated by changing its duty cycle, defined as

$$D_{\text{pulse}} = \frac{T_{\text{pulse}}}{T_{\text{pulse}} + T_{\text{slope}}}. \tag{2.19}$$

This also means that, for a specific magnitude of u_{cn}, the voltage over the blocking capacitor can be regulated by changing the pulse duty cycle.

It should be clarified that the ions are bombarding the substrate surface throughout the fundamental period. Since ions have much larger inertia than electrons due to their mass, it is assumed that the ion energy does not change much if the post-discharge phase is relatively short. However, if the post-discharge phase is too long, the distribution at lower ion energy, approximating to eV_{p}, can be increased in the IED.

Restart charge phase

When the post-discharge phase is finished, a negative voltage should be applied to the table to restart the charge phase. The value of this negative voltage determines the ion energy. Assuming u_{t} changes from the positive discharge voltage V_{d} to a

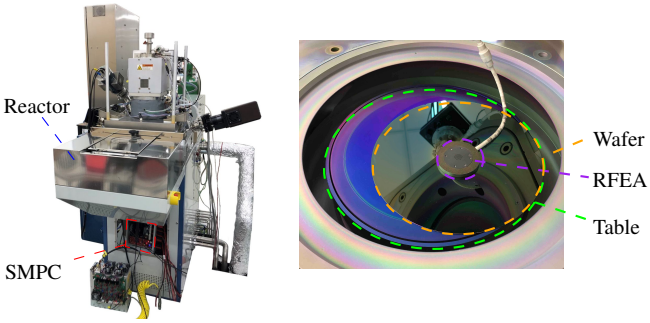


Figure 2.6 (a) The FlexAL system. (b) The reactor table, substrate wafer, and an RFEA.

negative start voltage V_s, it is essential to note that before u_t turns negative, D_2 remains conducting, and voltages over C_{sh1}, C_{sh2}, and C_{sub} are clamped to zero. Only after u_t falls below zero, D_2 starts blocking, and the equivalent circuit turns from Figure 2.5(d) to (a) again by rapidly recharging C_{sh1}, C_{sh2} and C_{sub} through R_p.

It should be stressed that this recharge process also takes a time comparable to the discharge phase. However, since its equivalent circuit is identical to the charge phase, it is not classified separately for conciseness. During this short recharge time, the voltage u_{sh1} acquires an initial value at the start of the charge phase due to the capacitive voltage divider formed by C_{sh1} and C_{sub}. Neglecting the effect of ion current, this initial value of u_{sh1} is governed by

$$u_{sh1} = \frac{C_{sub}}{C_{sub} + C_{sh1}} V_s. \tag{2.20}$$

If C_{sub} is much larger than C_{sh1} (which is generally the case), u_{sh1} can be approximate by V_s. This reveals that the below-zero part of the falling edge of the voltage pulse, rather than the entire part, determines the sheath surface potential. Together with the plasma potential, the sheath surface potential determines the ion energy.

2.2 Experimental verification

2.2.1 Experimental setup

To verify the proposed EEC model, experiments were conducted using an Oxford Instruments FlexAL system, as shown in Figure 2.6(a), which is a plasma reactor designed for ALD, but can also be used for ALE. The standard RF bias converter

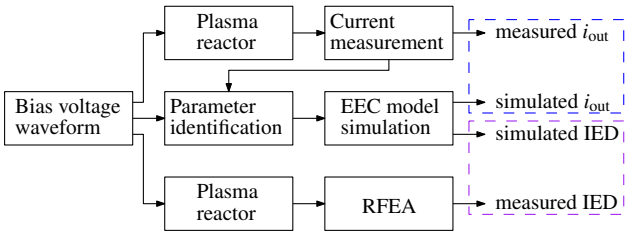


Figure 2.7 The process of the experimental verification.

was uninstalled, and a custom SMPC was used to deliver the required tailored waveforms. The SMPC was coupled with the reactor table via a blocking capacitor of 2 µF. The details of the SMPC are provided in [187,189] and Appendix A, and it is patented in [40].

An Ar plasma was created with an ICP source through an automatic matching network. The plasma source can deliver up to 600 W power at 13.56 MHz. It contains a three-turn water-cooled copper coil around a cylindrical 65-mm aluminium oxide (Al_2O_3) ceramic plasma tube. The distance between the substrate and the plasma source is in the order of 25 cm. The pressure inside the reactor was maintained at 2.2 mTorr. More details of the plasma reactor can be found in [71].

For the experiments, four-inch and eight-inch Si wafers with 400-nm SiO_2 were used as the dielectric substrates. In the cases of measuring the IEDs, a commercial gridded RFEA from Impedance Ltd. with a resolution of $\Delta E = 1$ eV was used and placed on the top of the substrate, as shown in Figure 2.6(b).

The process of the experimental verification is depicted in Figure 2.7. First, bias voltage waveforms u_{out} with different voltage slopes were applied to the plasma reactor with a wafer on the table. Waveforms of u_{out} were measured using a differential voltage probe, while waveforms of i_{out} were measured using a current probe. As explained in Appendix A, i_{out} entirely goes through an inductor during the charge phase, and the average inductor current is equal to the average value of i_{out} during the charge phase, which was measured using a high-accuracy multimeter. It must be pointed out that RFEA measurement is intrusive and can disturb the EEC model, which is further explained in Chapter 3. Therefore, the RFEA was removed in these measurements.

Second, the applied u_{out} and the measured i_{out} were used for parameter identification as explained in Chapter 4, but it is skipped in this chapter. The identified parameters were then substituted into the EEC model for circuit simulation. The simulation was conducted in MATLAB/Simulink with the Simscape toolbox.

Figure 2.8 shows the measured electric waveforms, including the output voltage

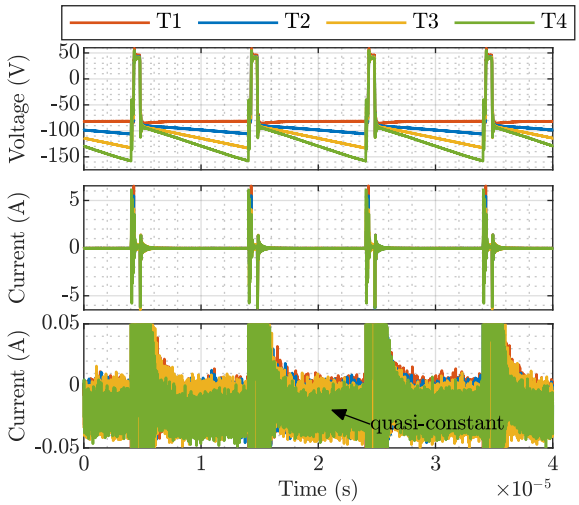


Figure 2.8 The measured electric waveforms, being from top to bottom: u_{out}, i_{out} and a zoomed-in view of i_{out}, respectively. T1, T2, T3 and T4 represent different voltage slope rates.

and output current waveforms for the four-inch wafer with 200 W ICP power. The applied bias waveforms have a repetition frequency of 100 kHz. The duty cycle of the charge phase is 90%, and the duty cycle of the discharge phase and post-discharge phase add up to 10%. The discharge voltage V_{d} is fixed at 50 V, and the negative voltage applied to restart the charge phase V_{s} is fixed at -100 V. Therefore, at the optimal operating point, the average ion energy is expected to be approximately 100 eV.

The voltage slope rate is controllable and ranges from approximately 0 to $-16.7 \cdot 10^6\,\text{V}\,\text{s}^{-1}$ in this experiment. Consequently, the peak-to-peak voltage of the bias waveforms is determined by the slope rate and ranges from 150 to 200 V. As can be seen, the output current is quasi-constant in the charge phase. When applying output voltages u_{out} with different slope rates, different dc values of the output current i_{out} are obtained.

2.2.2 Simulation setup

The circuit model used for simulation is illustrated in Figure 2.9. Compared to the EEC model depicted in Figure 2.3, I_{i2} and C_{sh2} are neglected for simplicity, as explained in Section 4.1.

An ideal switch S and a resistor R_{pd} are added. Here R_{pd} is an extra plasma

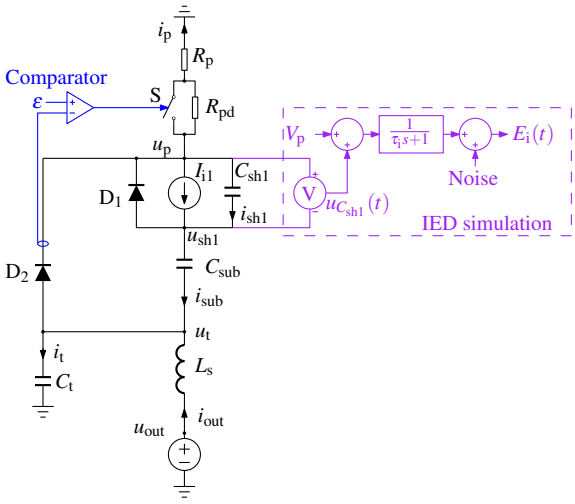


Figure 2.9 The circuit model used for simulation.

resistance added during the post-discharge phase, which leads to a virtually zero output current, and its value is derived in Chapter 4. The switch is controlled by the current of D_2 and the current comparator. When the current of D_2 is smaller than a small positive quantity ε, which effectively means D_2 is not conducting, the comparator outputs logic "1" and turns on the switch S. As a result, only R_p is connected in the circuit, which should be a small value according to (2.11). When the current of D_2 is larger than ε, which only occurs during the post-discharge phase depicted in Figure 2.5(d), the comparator outputs logic "0" and turns off the switch S. In this case, R_{pd} is connected in the circuit. The total resistance in the loop is $R_p + R_{pd}$, which determines the current during the post-discharge phase.

It must be stressed that the waveforms of u_{out} used for simulation were directly taken from the measurements and were measured after the blocking capacitor for simplicity. In other words, the simulation does not guarantee self-balancing of the output current i_{out}. The electric waveforms of all the components can be simulated by circuit simulation and compared to the measured ones. In this experimental setup, only i_{out} can be measured non-intrusively and was thus used for comparison.

Additionally, the IED can also be simulated as using the circuit model depicted in Figure 2.9. As described in Section 2.1, ions enter the sheath with an initial energy eV_p, where the floating potential V_p for a typical Ar plasma is 25 V as calculated by (1.24) in Section 1.1.2. The ions obtain extra energy in the sheath, determined by the instantaneous voltage of $u_{C_{sh1}}$. In practice, since the ions have a finite transit time τ_i in the sheath, they do not respond to instantaneous $u_{C_{sh1}}$. Instead, the ions

respond to the averaged $u_{C_{sh1}}$ within the transit time τ_i [36], which results in an inertial effect. This effect can be represented by a transfer function H_{damp} in the s (complex frequency) domain as

$$H_{damp}(s) = \frac{1}{\tau_i s + 1}. \tag{2.21}$$

The transit time τ_i can be approximated by the inverse of the ion plasma frequency ω_i at the sheath edge as [36, 45, 132, 180]

$$\omega_i = \sqrt{\frac{e^2 n_s}{\epsilon_0 m_i}}. \tag{2.22}$$

In this work, an estimated ion density $n_s = 1 \cdot 10^9\,\mathrm{cm}^{-3}$ is used [138].

Furthermore, the ion energy can be affected by collisions in the sheath, which broadens the IED [15, 96]. In practice, the measurement with RFEA can also broaden the IED due to the scattering of ions on the RFEA's grids [36, 96]. These broadening effects are equivalent to a normally distributed noise defined by

$$f(E_i) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{E_i-\mu}{\sigma}\right)^2}, \tag{2.23}$$

where μ is the mean of the noise, and σ is the standard deviation of the noise. In this thesis, μ is assumed to be zero, and a typical standard deviation $\sigma^2 = 5\,(\mathrm{eV})^2$ is adopted based on the measurement results. The standard deviation of a normal distribution determines its full width at half maximum (FWHM) as

$$\mathrm{FWHM} = 2\sqrt{\ln 2}\sigma \approx 2.35\sigma. \tag{2.24}$$

This means that the narrowest IED that can be obtained has a FWHM of 5.3 eV even with an ideal tailored waveform. Further derivations are provided in Appendix C.

The software simulation generates a discrete time series $\{t[1], t[2], ...t[m]\}$ and the corresponding energy series $\{E_i[1], E_i[2], ..., E_i[m]\}$, where m is the total number of simulated moments within one fundamental period, and $E_i[j]$ $(j = 1, 2, 3, ..., m)$ is the energy of the ions arriving at the substrate surface at time $t[j]$. If the ion flux is assumed to be constant over the period, then the normalized ion flux $P(E)$ can be approximated by

$$P(E) = \frac{1}{T_{pulse} + T_{slope}} \sum_{1 \le j < m, E \le E_i[j] < E + \Delta E} t[j+1] - t[j]. \tag{2.25}$$

Consequently, the IED can be simulated based on this circuit simulation. To verify the accuracy of the simulation, the simulated IEDs were compared to the RFEA measurements.

Table 2.1 The parameters of the EEC model

Parameter	Value	Unit	Parameter	Value	Unit
I_{i1}	12.65	mA	V_p	25	V
I_{i2}	0	mA	L_s	25	nH
C_t	2.22	nF	C_{sub}	3.09	nF
C_{sh1}	0.435	nF	R_p	16.2	Ω
C_{sh2}	0	nF	R_{pd}	6000	Ω

2.2.3 Electric waveform and ion energy distribution simulation

The electric waveforms can be simulated by applying the same bias voltage waveforms used in experimental measurements. The simulation parameters are obtained through a parameter identification method, which is further explained in the following chapters. However, for brevity, the details of how these parameters are derived are omitted here, but their values are provided in Table 2.1.

Figure 2.10 displays the simulated waveforms at the optimal operating point, obtained from the circuit simulation based on the EEC model. During the charge phase, both the substrate surface potential u_{sh1} and the ion energy E_i are quasi-constant. Although the experimental setup doesn't allow measuring the waveforms of $u_{C_{sh1}}$ and $u_{C_{sub}}$, the simulated results agree with the measured ones presented in [96]. Zooming in around the discharge phase of the waveforms in Figure 2.10, Figure 2.11 shows the simulated i_{out} generally matches the measured i_{out}, considering the transient behavior, magnitude, and resonant frequency.

Additionally, the IED can be simulated based on the simulated waveform of E_i according to (2.25), as shown in Figure 2.12. Similarly, by applying the same bias voltage waveform to both the simulation model and the plasma reactor with an RFEA presented, the simulated and measured normalized IED can be compared. Figure 2.13 illustrates a comparison between the simulated and measured results for different voltage slopes. The simulated results generally follow the trend of the measured ones.

Furthermore, Figure 2.14 compares the FWHM and the average energy at different voltage slope rates from both the simulations and measurements. The simulated IEDs accurately identify the optimal slope rate, leading to the minimum FWHM. Compared to the measurements, the simulated average ion energy is generally within 10 eV difference. It should be noted that the IED can only be measured with an RFEA, which interacts with the plasma processing and IED. In the case without RFEA, the IED inherently differs from that with RFEA. Such a difference may contribute to the deviation of the comparison as well.

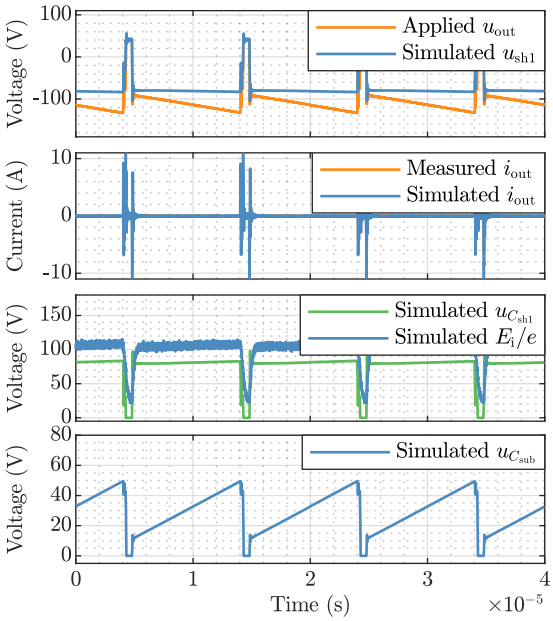


Figure 2.10 The simulated electric waveforms from the circuit simulation based on the EEC model. The measured and simulated i_{out} are almost overlapping and are distinguished in the following figure.

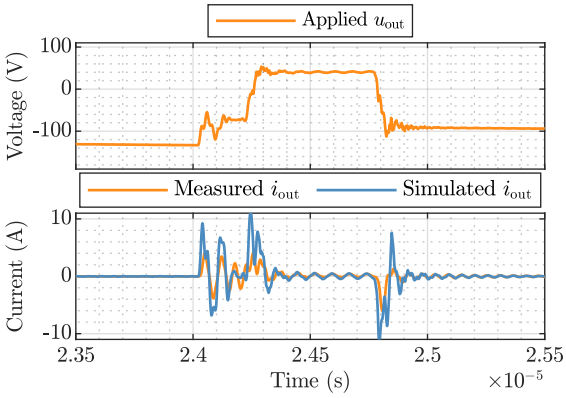


Figure 2.11 A zoomed-in view around the discharge phase of the simulated electric waveforms from the circuit simulation based on the EEC model.

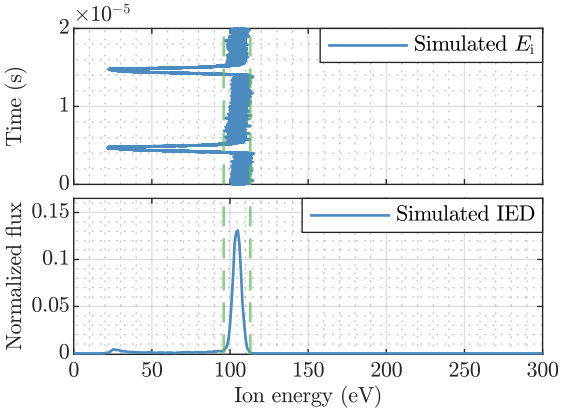


Figure 2.12 The IED simulation from the waveform of E_i.

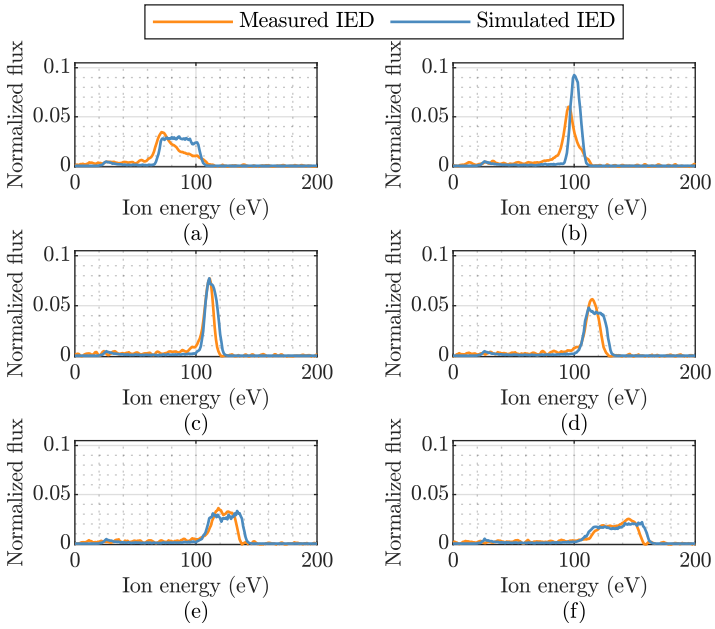


Figure 2.13 Comparison of the simulated and measured normalized IED for the four-inch wafer with 200 W ICP power at voltage slope rate of (a) $0.056 \cdot 10^6\,\mathrm{V\,s^{-1}}$, (b) $-3.023 \cdot 10^6\,\mathrm{V\,s^{-1}}$, (c) $-5.722 \cdot 10^6\,\mathrm{V\,s^{-1}}$, (d) $-6.753 \cdot 10^6\,\mathrm{V\,s^{-1}}$, (e) $-7.983 \cdot 10^6\,\mathrm{V\,s^{-1}}$, and (f) $-9.982 \cdot 10^6\,\mathrm{V\,s^{-1}}$.

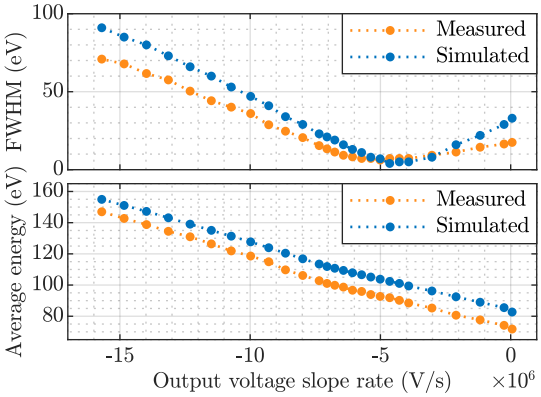


Figure 2.14 Comparison of the simulated and measured full width at half maximum and average energy for the eight-inch wafer at different voltage slope rates.

2.2.4 Case study of variant pulse duty cycles

In the previous sections, a study on variant slope rates with a fixed pulse duty cycle is presented. Figure 2.15 illustrates the measured waveforms of u_{cn} from the waveform generator and u_{out} after the blocking capacitor. It is observed that the magnitudes of the negative voltage pulse delivered by the waveform generator are the same and equal to $-100\,\mathrm{V}$. Meanwhile, the slope rates are kept approximately equal. The pulse duty cycles for T1, T2, T3, and T4 are about 2.5 %, 5 %, 10 %, and 20 %, respectively. According to (2.18), these different pulse duty cycles should lead to different V_{d}, which approximates to $39I_{\mathrm{i2}}R_{\mathrm{p}}$, $19I_{\mathrm{i2}}R_{\mathrm{p}}$, $9I_{\mathrm{i2}}R_{\mathrm{p}}$, and $4I_{\mathrm{i2}}R_{\mathrm{p}}$, respectively. As seen from Figure 2.15, these variant duty cycles apparently cause differences to the discharge voltage V_{d} in u_{out}. The measured values of V_{d} are 70, 50, 25, and 15 for T1, T2, T3, and T4, respectively. Although this correlation generally follows (2.18), their ratios are deviated with the equation. This deviation originates from several factors, including the inaccuracy of duty cycle due to resonance, I_{i2} not being constant but voltage-dependent, and so on. However, the results prove that V_{d} (and V_{b}) can be controlled by the pulse duty cycle.

Moreover, the IEDs corresponding to the waveforms of u_{out} were both simulated and measured, and the results are plotted in Figure 2.16. It should be noted that since this series of experiments was not conducted in a continuous run with the previous ones, the plasma potential can be variable due to the inconsistent feedstock gas, vacuum pressure, temperature, *etc.* Therefore, V_{p} was recalibrated to 35 V, and the variance $\sigma^2 = 10\,(\mathrm{eV})^2$. Apart from these two, other parameters used in the simulations are equal to the ones in Table 2.1. As seen from Figure 2.16, the

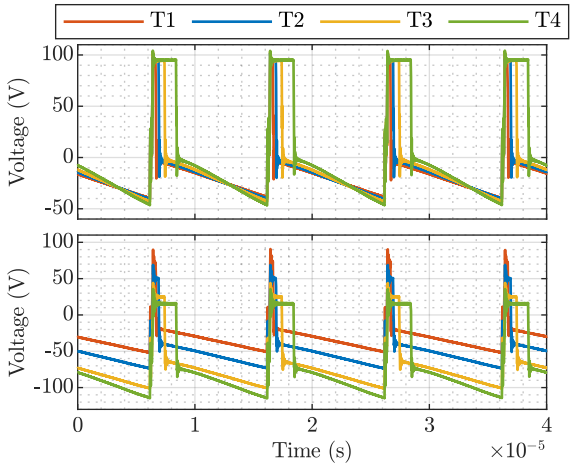


Figure 2.15 The measured electric waveforms, being from top to bottom: u_{cn} from the waveform generator and u_{out} after the blocking capacitor, respectively. T1, T2, T3 and T4 represent different duty cycles.

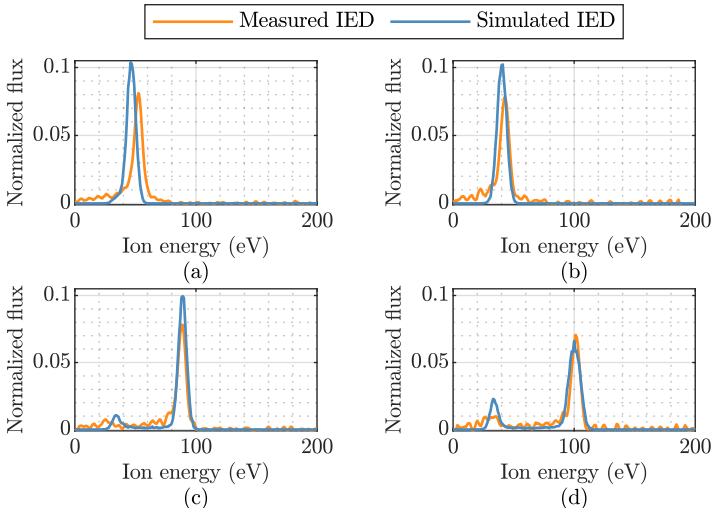


Figure 2.16 Comparison of the simulated and measured normalized IED for the four-inch wafer with 200 W ICP power. (a), (b), (c), and (d) correspond to T1, T2, T3, and T4, respectively.

simulated and measured IEDs match well.

Both the simulated and measured IEDs manifest that the ion energy is determined by the below-zero part of the falling edge of the voltage pulse, *i.e.*, V_s, instead of its entire part. Therefore, it underscores the correctness of (2.20). Meanwhile, it provides strong evidence of the existence of the table sheath and D_2. Otherwise, without D_2, C_{sh2} or C_{sub} cannot be fully discharged to zero voltage with a positive V_d, neither can (2.20) hold.

Additionally, this case study suggests that if a blocking capacitor is used, to make the most use of the falling edge of the voltage pulse, the pulse duty cycle is preferred to be large to obtain a small V_d and large V_s. On the other hand, an excessive pulse duty cycle causes an inadequate charge phase duty cycle (which is the effective phase for ion energy control). Thus, more ions fall into a lower energy spectrum, as reflected by Figure 2.16(d).

2.3 Conclusion

The EEC model is essential for circuit simulation and bias waveform optimization for tailored waveform biasing in plasma processing. Traditional EEC models were developed for RF biasing. They are unsuitable for tailored waveform biasing, mainly because the capacitors in the EEC are not rapidly and completely discharged during the discharge phase.

To address this issue, this chapter proposes an improved EEC model, which is especially suitable for tailored waveform biasing. The improved EEC model simplifies the plasma by a resistor, thus providing a fast discharge path for the capacitors. Meanwhile, it introduces another sheath, known as the table sheath, between the bulk plasma and the exposed part of the reactor table, allowing all capacitors to discharge to zero voltage. It should be clarified that the existence of the table sheath depends on the configuration of the plasma reactor. In some cases, such as when the wafer area is larger than the table area, the table sheath might not exist. In tailored waveform biasing, the plasma processing can be divided into three phases: the charge phase, the discharge phase, and the post-discharge phase. The proposed model is thoroughly analyzed during all of these phases.

Using the proposed EEC model, along with the parameter identification method presented in the following chapters, plasma processing can be simulated in ordinary circuit simulation software, such as the simulation program with integrated circuit emphasis (SPICE) or MATLAB/Simulink. Electric waveforms and IEDs are simulated by circuit simulation, and experiments have been conducted for verification. The alignment between the simulation and measurement under different conditions

underlines the correctness of the proposed EEC model. This model can be a supplement and substitute for traditional plasma simulation methods like PIC, enjoying the advantage of considerably reduced computation time.

This chapter bridges the gap between plasma processing and bias converter design by providing an electrically equivalent description of plasma processing, offering insights into the process from an electrical engineering perspective. As such, the EEC can be used to design and optimize the SMPC for electrical engineers, thereby significantly improving the process efficiency. Meanwhile, a well-designed bias converter can improve tailored waveform biasing performance by allowing more flexible bias waveforms.

The proposed model might also be used for bias waveform optimization and IED tailoring. It is expected to be compatible with other bias waveforms like RF biasing and pulse-shaped biasing but requires further experimental validation.

Chapter 3

Auto-tuning

The previous chapter has demonstrated the principles of tailored waveform biasing. It has been found that the negative part of the falling edge of the discharge voltage pulse determines the ion energy, while the voltage slope rate during the charge phase determines the width of the IED. There exists an optimal slope rate to precisely compensate for the ion charge effect and retain the narrowest IED, governed by the ion current I_{i1} and the substrate capacitance C_{sub}, as derived by (2.12). It is defined as the optimal operating point in this thesis if such a slope rate is reached.

Usually, I_{i1} is unknown and challenging to measure directly, so the optimal slope rate cannot be obtained in a straightforward way. A widely adopted method in both industrial and academic applications is to use an RFEA placed on the top of the substrate to help find the optimal slope rate. This involves applying different voltage slope rates to the reactor table to measure IEDs of varying widths by the RFEA. The slope rate corresponding to the narrowest IED is considered optimal. Afterward, the RFEA is removed in standard production, and the same slope rate is used for plasma processing. This method is referred to as manual tuning in this thesis.

However, the manual-tuning method makes an implicit assumption that the RFEA does not affect the electrical properties, meaning that the optimal slope rate remains the same when the RFEA is removed, and the substrate surface potential remains the

This chapter is based on [184, 188].

same as when the RFEA is placed. Whether this assumption holds or not is seldom investigated in published literature. The previous chapter has briefly mentioned that the RFEA could interfere with the process and the IED. In this chapter, its effect is further demonstrated. It is also proven that the implicit assumption is unreliable and could lead to inaccuracy.

Furthermore, the manual-tuning method suffers from another drawback. The ion current I_{i1}, which affects the optimal slope rate, is dependent on various plasma conditions, including the plasma power, species, pressure, ionization degree, and so forth. The substrate capacitance C_{sub} is mostly dominated by the wafer. Therefore, this optimal slope rate can vary from plasma to plasma, wafer to wafer, reactor to reactor, and process to process. Any change in the numerous operating condition parameters necessitates repetitive RFEA measurements to obtain the new optimal slope rate, which can be time-consuming.

The previous chapter proposes an equivalent electrical circuit model, which provides more insight into the electrical properties of plasma processing. Based on this model, an auto-tuning method is developed in this chapter that can automatically find the optimal slope rate under different operating conditions by utilizing the unique electrical properties at the optimal operating point. This auto-tuning method is elaborated on in the following sections.

3.1 Auto-tuning concept

During the charge phase, as depicted in Figure 2.5(a), plasma processing can be generalized by

$$i_{out} = \left(\frac{C_{sh1} C_{sub}}{C_{sh1} + C_{sub}} + C_{sh2} + C_t \right) \dot{u}_t - \frac{C_{sub}}{C_{sub} + C_{sh1}} I_{i1} - I_{i2}, \tag{3.1}$$

where $\dot{u}_t$ represents the derivative of u_t with respect to time (*i.e.*, $\frac{\mathrm{d}u_t}{\mathrm{d}t}$). By varying the voltage slope $\dot{u}_t$, the output current i_{out} changes accordingly, as observed in the experimental measurements shown in Figure 2.8. In the case where $\dot{u}_t$ is fixed, i_{out} can be considered constant during the charge phase, and $\dot{u}_t = \dot{u}_{out}$, disregarding L_s.

Typically, the values of C_{sh2} and I_{i2} are not of interest and are relatively small, so they are assumed to be zero for simplicity. As such, the simplified description of the system is then given by

$$i_{out} = \left(\frac{C_{sh1} C_{sub}}{C_{sh1} + C_{sub}} + C_t \right) \dot{u}_{out} - \frac{C_{sub}}{C_{sub} + C_{sh1}} I_{i1}. \tag{3.2}$$

Assuming u_{out} is an independent variable and i_{out} is a dependent variable, (3.2) can be considered a linear equation with two coefficients, one in Coulomb and the

other in Ampere. Two effective parameters, capacitance C_{eff} and current I_{eff}, can be defined to represent these two coefficients as

$$C_{\text{eff}} = \frac{C_{\text{sh1}} C_{\text{sub}}}{C_{\text{sh1}} + C_{\text{sub}}} + C_{\text{t}}, \tag{3.3}$$

and

$$I_{\text{eff}} = -\frac{C_{\text{sub}}}{C_{\text{sub}} + C_{\text{sh1}}} I_{\text{i1}} = \left(\frac{C_{\text{sh1}}}{C_{\text{sh1}} + C_{\text{sub}}} - 1 \right) I_{\text{i1}}. \tag{3.4}$$

Note that both C_{eff} and I_{eff} are varying with different operating points and dependent on $\dot{u}_{\text{out}}$.

If a set of different output voltage slopes $\dot{u}_{\text{out},x}$ $(x \in 1, 2, 3, ..., n)$ with sufficiently small gradients is applied, the resultant output current $i_{\text{out},x}$ $(x \in 1, 2, 3, ..., n)$ during the charge phase can be measured. This allows the value of C_{eff} and I_{eff} at the corresponding $\dot{u}_{\text{out}}$ to be approximated using two adjacent points using forward difference, as given by

$$C_{\text{eff},x} = \frac{\dot{i}_{\text{out},x} - \dot{i}_{\text{out},x-1}}{\dot{u}_{\text{out},x} - \dot{u}_{\text{out},x-1}} \tag{3.5}$$

and

$$I_{\text{eff},x} = \frac{\dot{u}_{\text{out},x-1} \dot{i}_{\text{out},x} - \dot{u}_{\text{out},x} \dot{i}_{\text{out},x-1}}{\dot{u}_{\text{out},x} - \dot{u}_{\text{out},x-1}}. \tag{3.6}$$

The values of $\dot{u}_{\text{out},x}$ $(x \in 1, 2, 3, ..., n)$ should cover a sufficiently large range with the optimal operating point included. Assuming the optimal operating point is found at $x = k$, $\dot{u}_{\text{out},k}$ should be equal to $-I_{\text{i1}} C_{\text{sub}}^{-1}$ according to (2.12). Under this circumstance, u_{sh1} remains constant during the charge phase, and there is no current flowing through the sheath capacitor C_{sh1}. Therefore, C_{sh1} can be omitted from the circuit depicted in Figure 2.5(a). Consequently, the system can be equivalently simplified by

$$\dot{i}_{\text{out}} = C_{\text{t}} \dot{u}_{\text{out}} - I_{\text{i1}}. \tag{3.7}$$

This simplification can also be derived by substituting $\dot{u}_{\text{out}} = -I_{\text{i1}} C_{\text{sub}}^{-1}$ into the generalized system equation (3.2) since (3.7) is essentially a special case of the general equation. It's worth noting that

$$C_{\text{t}} \leq C_{\text{eff}} = \frac{C_{\text{sh1}} C_{\text{sub}}}{C_{\text{sh1}} + C_{\text{sub}}} + C_{\text{t}} \tag{3.8}$$

and

$$-I_{\text{i1}} \leq I_{\text{eff}} = -\frac{C_{\text{sub}}}{C_{\text{sub}} + C_{\text{sh1}}} I_{\text{i1}} \tag{3.9}$$

always hold true. Therefore, finding the optimal operating point is equivalent to finding the minimum value of C_{eff} or I_{eff}, which can be easily obtained from (3.5) and (3.6).

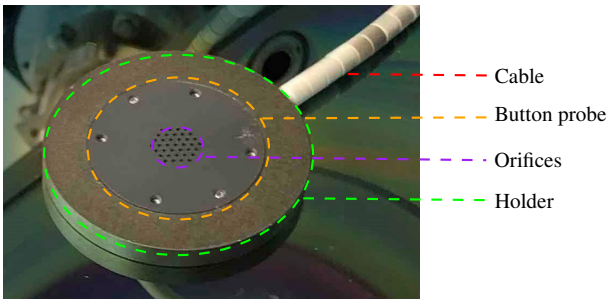


Figure 3.1 The composition of a typical RFEA (Semion Single manufactured by Impedans Ltd).

Theoretically, the minimum value of C_{eff} and I_{eff} should be reached at the same value of $\dot{u}_{\text{out},x}$. However, in practice, the ion current increases as the voltage becomes more negative [156, 157]. Therefore, it turns out to be more reliable to find minimum value of C_{eff}. Essentially, the search for the minimum value of C_{eff} is equivalent to the search for C_{t}, which is relatively constant at different voltages. This is due to the fact that the surface area of both the table and the reactor wall, as well as their distance, remain unchanged.

3.2 System influence of retarding field energy analyser

It has been proven that the RFEA measurements can distort and deviate from the actual IED [69, 164, 169] due to multiple factors, including the space charge effect, misalignment of the grids, and so on. However, the influence of these factors on the electrical characteristics of plasma processing has not received sufficient attention. Therefore, further exploration of the influence of the RFEA is necessary.

To understand how the RFEA affects the EEC, it is important to briefly introduce its basic principles. As depicted in Figure 3.1, a typical RFEA consists of a holder, a button probe (the effective sensing element) with multiple orifices of millimeter diameter, and a high-voltage cable for voltage supply. The cable connects to a feed-through unit outside of the reactor chamber, serving as a connection between the vacuum chamber and its supply and measurement electronics in the atmospheric environment, transmitting electrical signals. The holder and button probe bodies are both made of metal, such as aluminum or stainless steel. The orifices receive the plasma ions (and possible electrons) and measure the ion flux and energy.

The operating principle of a typical four-gridded RFEA is illustrated in Figure 3.2.

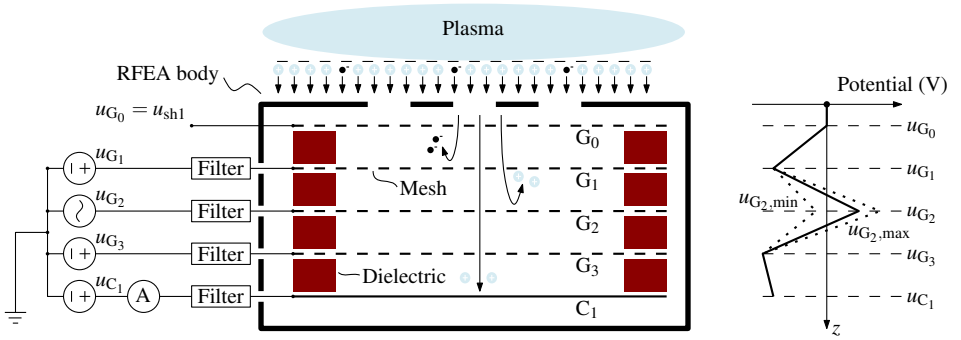


Figure 3.2 The schematic of a typical fourth-gridded RFEA and its working principle.

This type of RFEA is composed of four grids (G_0, G_1, G_2, and G_3), typically made of metal (like nickel), with numerous square meshes of micrometer size on each grid. A metal collector C_1 is situated beneath the four grids to receive the ions. The gap between each grid and the collector is filled with a dielectric layer, such as mica [8].

The grid G_0 is electrically connected to the RFEA body. When measuring the IED on the substrate surface, the RFEA should be positioned on the top of the substrate. Therefore, its metal body should have the same voltage potential as the substrate surface, such that the potential of the first grid $u_{G_0} = u_{sh1}$. The plasma ions enter the orifices with an initial energy determined by the substrate surface potential and plasma potential.

Other grids and the collector are connected to voltage sources through low-pass filters, and their electric potentials are displayed in Figure 3.2. The grid G_1 is negatively biased with respect to G_0 ($u_{G_1} < u_{G_0}$), creating a retarding field against electrons and repelling the possible electrons from the plasma sheath. Therefore, this grid is also known as the plasma electron repellor.

The grid G_2 is biased by a voltage source delivering a sweeping voltage with respect to G_0. Its voltage potential u_{G_2} sweeps between its minimum $u_{G_2,min}$ and maximum $u_{G_2,max}$. Any ion with an energy lower than the instant voltage difference $u_{G_2} - u_{G_0}$ is repelled, whereas ions with higher energy can enter the next grid and be collected. Consequently, this grid is also referred to as the discriminator. Its voltage swinging range $u_{G_2,max} - u_{G_2,min}$ is the measurement range of the RFEA.

The grid G_3 is also negatively biased with respect to G_0 ($u_{G_3} < u_{G_0}$), serving as a second electron suppressor. Its purpose is to repel the secondary electrons that may be emitted from the collector surface due to ion bombardment. In a simpler three-gridded RFEA, this grid is eliminated.

The collector C_1 is also negatively biased with respect to G_0 ($u_{C_1} < u_{G_0}$) to attract all the ions passing through G_3. The ion current is measured using a current meter. By recording the voltage difference $u_{G_2} - u_{G_0}$ and the resultant ion current at each sweep step, a current-voltage curve can be plotted, and the IED can be derived.

The low-pass filters in the RFEA have a high impedance at high frequencies. There is capacitive coupling between the RFEA body and the protective earth (PE) through the dielectric between each grid. The filters have a high attenuation for the possible high-frequency current introduced by the variable u_{sh1} through the capacitive coupling. Since RF biasing is still the most popular technique, RFEAs are designed for the typical RF frequency, such as 0.5 to 60 MHz, as specified in [61]. However, as explained in the previous chapter, tailored waveform biasing advantageously reduces the repetition frequency, which may degrade the effectiveness of the low-pass filters, thus increasing the capacitive coupling between the RFEA body and the ground.

Therefore, the electrical effects of the RFEA can be summarized as follows. On the one hand, it sinks the ion current to the ground, which reduces the current going to the substrate. It is worth noting that the total area of orifices can be considerable, for example, in the case of a Semion Multi RFEA, which can cover the entire wafer surface. On the other hand, the RFEA increases the capacitive coupling between its body (which has a potential of u_{sh1}) and the ground, thus equivalently increasing C_{sh1}.

The equation (2.10) implies that if u_p is considered constant during the charge phase, then the voltage u_{sh1} is governed by

$$(C_{sub} + C_{sh1}) \frac{\mathrm{d}u_{sh1}}{\mathrm{d}t} = I_{i1} + C_{sub} \frac{\mathrm{d}u_t}{\mathrm{d}t}. \tag{3.10}$$

Consequently, with an RFEA on the top of the substrate, a less negative voltage slope is required to maintain a constant u_{sh1}. Therefore, theoretically, the optimal slope rate found by the auto-tuning method should be more negative compared to the manual-tuning with an RFEA. Besides, the extra capacitance added by the RFEA results in a smaller u_{sh1} variance and a narrower IED than the scenario without the RFEA at the same voltage slope rate.

3.3 Experimental verification

Experiments were conducted to validate the auto-tuning methods using the same experimental setup as described in Section 2.2. The experimental verification process is shown in Figure 3.3. Initially, the optimal operating slope rate was determined by the manual-tuning method with the RFEA measurements. Subsequently, the RFEA was removed, and voltage slopes within the similar range were applied

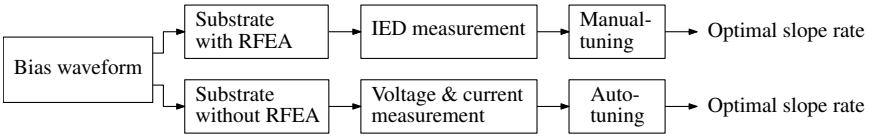


Figure 3.3 The experimental verification process.

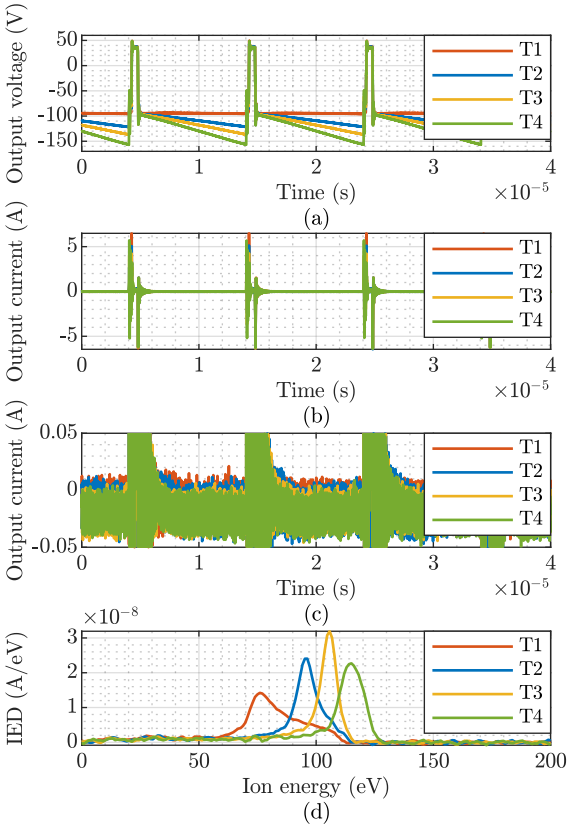


Figure 3.4 The measured waveforms of (a) the output voltage, (b) output current, (c) a zoom-in view of the output current, and (d) the corresponding IED measured with the RFEA. T1, T2, T3 and T4 indicate different voltage slope rates.

Table 3.1 Comparisons between the optimal slope rate found by manual-tuning and auto-tuning under different conditions

Wafer	Four-inch		Eight-inch	
ICP power (W)	200	600	200	600
Manual-tuning ($\mathrm{V\,s^{-1}}$)	$-5.01 \cdot 10^6$	$-6.39 \cdot 10^6$	$-5.96 \cdot 10^6$	$-7.03 \cdot 10^6$
Auto-tuning ($\mathrm{V\,s^{-1}}$)	$-5.59 \cdot 10^6$	$-2.80 \cdot 10^6$	$-5.64 \cdot 10^6$	$-6.50 \cdot 10^6$

while measuring the resultant electrical waveforms. The optimal slope rate could then be derived based on the proposed auto-tuning method and compared to the manual-tuning result for validation.

The measurement results of a typical manual-tuning for the four-inch wafer under 200 W plasma power are depicted in Figure 3.4. As presented, during the charge phase, the output current is negative and quasi-constant, which yields very similar electrical behavior to the case without RFEA presented in Figure 2.8.

Varying the voltage slope also results in changes in the width of IED. Among the cases shown in Figure 3.4, the voltage slope of T3 produces the narrowest IED and is considered optimal. In comparison, the under-compensation slope rates (T1 and T2) shift the IED to the left as the substrate surface potential u_{sh1} rises during the charge phase, while the over-compensation slope rate (T4) has the opposite effect. Additionally, a narrower IED corresponds to a higher IED peak, which can be used as a quantitative merit for further comparison, denoted as A_{IED}.

From the comparison between Figure 3.4 and Figure 2.8, it is hard to see the electrical effect of the RFEA. To further investigate into this effect, the effective capacitance C_{eff} and effective current I_{eff}, as defined in (3.3) and (3.4), can be similarly defined and measured with the RFEA placed on the substrate. The comparison of C_{eff} and I_{eff} with and without the RFEA under different conditions is demonstrated in Figure 3.5. As observed in the figure, placing an RFEA on the top of the substrate generally increases the effective capacitance while decreasing the magnitude of the effective current (note that it is negative), which supports the analysis provided in Section 3.2. In the presented measurements, the added capacitance is approximately 0.1 nF, and the reduced current is approximately 1 mA. Since I_{i1} is more than 10 mA (as further discussed in the following chapter), this reduced current leads to less than a 10% error when finding the optimal slope rate in manual-tuning according to (2.12).

Furthermore, Figure 3.6 shows comparisons between the optimal slope rate found by manual-tuning and auto-tuning under different conditions, and Table 3.1 summarizes the corresponding values.

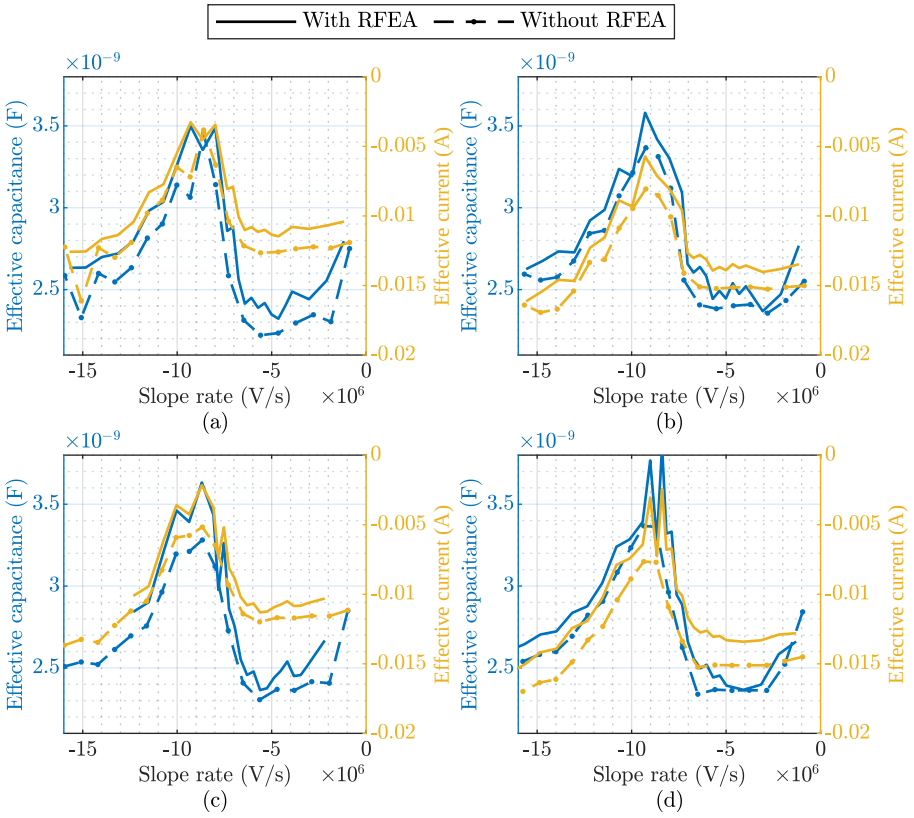


Figure 3.5 The effective capacitance C_{eff} and effective current I_{eff} in the case with and without RFEA for (a) four-inch wafer and 200 W plasma power, (b) four-inch wafer and 600 W plasma power, (c) eight-inch wafer and 200 W plasma power, and (d) eight-inch wafer and 600 W plasma power.

To evaluate IED width for an aligned direction with C_{eff} and for better visualization, the reciprocal of the peak IED, $1/A_{\text{IED}}$, is used. Therefore, for manual-tuning, the smallest value of $1/A_{\text{IED}}$ corresponds to the optimal slope rate, as indicted by the green squares in Figure 3.6. In the vicinity of the optimal slope rate in manual-tuning, the peak IED is approximately the same, so their IED widths should be comparable. Therefore, despite the less than 10% error caused by the reduced current, manual-tuning can still find a slope rate with comparable performance to the optimum.

On the other hand, the optimal slope rates found by auto-tuning are generally comparable to those found by manual-tuning, except for the case in Figure 3.6(b).

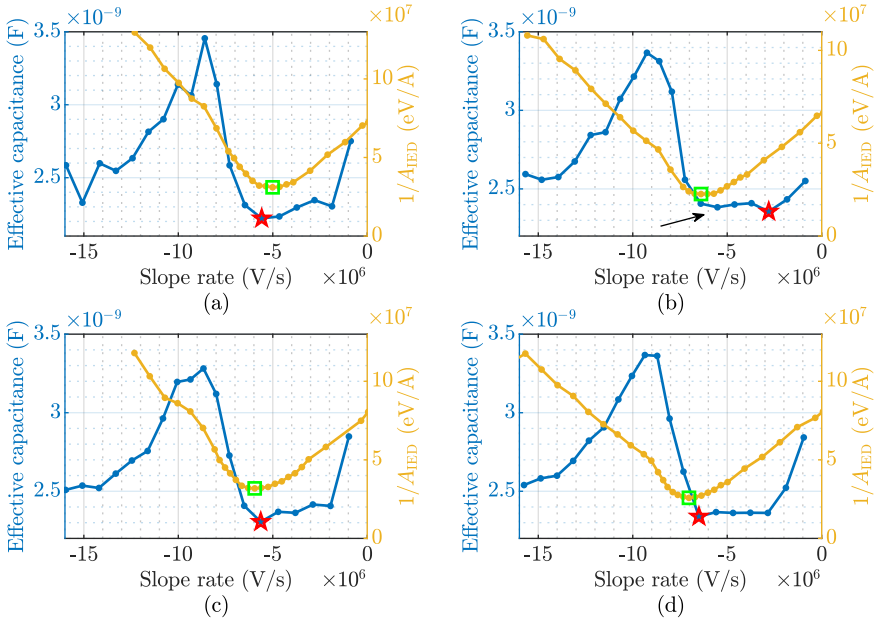


Figure 3.6 Comparisons between the optimal slope rate found by manual-tuning and auto-tuning for (a) four-inch wafer and 200 W plasma power, (b) four-inch wafer and 600 W plasma power, (c) eight-inch wafer and 200 W plasma power, and (d) eight-inch wafer and 600 W plasma power. The green squares indicate the manual-tuning results, and the red pentagons indicate the auto-tuning results.

However, upon zooming in on Figure 3.6(b), a local minimum of C_{eff} can be found at the slope rate of $-5.52 \cdot 10^6\,\text{V}\,\text{s}^{-1}$, as annotated by the arrow, which is much closer to the manual-tuning optimum. There is a possibility that a real minimum value of C_{eff} is around this point, but it is skipped due to the low gradient resolution of the applied slope rates.

Additionally, since the current going through the substrate is reduced by the RFEA, the optimal slope rate found by auto-tuning should be theoretically more negative than that found by manual-tuning. However, this is only observed in Figure 3.6(a). The low gradient resolution of the slope rates could lead this deviation since there is still a possibility of finding a smaller C_{eff} to the left of the manual-tuning results in Figure 3.6(c) and (d). Neglecting C_{sh2} and I_{i2} may also contribute to the deviation, but further validation is required.

3.4 Conclusion

The tailored waveform introduced in this study determines the IED in two aspects. The negative part of the falling edge of the voltage pulse determines the ion energy, and the voltage slope rate determines the width of the IED. The optimal slope rate should be found to obtain the narrowest IED.

The manual-tuning method, which is widely used to determine the optimal slope rate in tailored waveform biasing, employs an RFEA. However, such an RFEA can affect the electrical characteristics of plasma processing by adding equivalent sheath capacitance and reducing the ion current going to the substrate. This electrical effect has been validated by the experiments by extracting C_{eff} and I_{eff}. Consequently, the optimal slope rate found by the RFEA should be less negative than the actual optimal value when the RFEA is removed. Although this effect is minor in this experimental setup, it could degrade the accuracy under other conditions, particularly when using an RFEA of a larger size and a smaller repetition frequency for the bias waveforms. Besides, when a plasma parameter is altered, the optimal slope rate should be redetermined for manual-tuning, requiring repetitive adjustments of the slope rates and IED measurements.

This chapter proposes an auto-tuning method that solves these issues. By delivering different slope rates and measuring the electrical waveforms, C_{eff} can be derived at different slope rates. Finding the optimal slope rate is then equivalent to finding the minimum value of C_{eff}. This method only requires electrical measurements on the bias converter side, which is nonintrusive to the process and advantageously removes the need for an RFEA, while still obtaining optimal slope rates that are generally similar to those found with manual-tuning. Although the optimal slope rate found by auto-tuning may not result in the absolute narrowest IED, the difference is minor based on the experimental results, and it is far superior than what is achievable with RF biasing.

Approaching the proposed auto-tuning method with a critical mindset, it is important to note that the proposed auto-tuning method has not been evaluated to deliver correct results universally. Although various wafers with different plasma powers have been tested, the results are limited to a specific plasma reactor. Thus, the possibility of having obtained a lucky shot cannot be conclusively excluded. It is important to recognize that experimental setups, including the reactor, wafer, and plasma, may differ significantly across various industrial applications. More experiments under different experimental setups can certainly evidence (instead of confirming) or falsify its versatility.

Furthermore, measuring the substrate surface potential can provide more valuable insight into the process. Essentially, the optimal slope rate should lead to a quasi-

constant substrate surface potential and the narrowest IED. Considering the electrical effect of the RFEA, direct measurement of the substrate surface potential with a voltage probe would be more accurate. Unfortunately, such a measurement cannot be easily realized with the setup used in this research, but it is strongly recommend for further validation.

Aside from the critical perspective, it is important to acknowledge the success of the proposed auto-tuning method in finding satisfactory slope rates in our experiments, with only electrical measurements on the bias converter side and without looking into the plasma processing inside the chamber, which can be appreciated as the initial evidence of its effectiveness. It is also found that using a smaller slope rate gradient could help increasing accuracy. Besides, neglecting C_{sh2} and I_{i2} might also contribute to the error. In future research, it would be beneficial to reduce the capacitive coupling of C_{sh2}. What's more, the auto-tuning method has the potential to be effective in real-time during an actual process, but this feature needs further experimental verification.

Chapter 4

Parameter identification

In Chapter 2, an EEC model of plasma processing is developed, which can accurately replicate both the electrical behaviors and IEDs in circuit simulation. To fulfill simulation, parameters of the EEC model, including the capacitances and currents, are required. Typically, these parameters are derived from plasma physics theory, as introduced in Section 1.1. However, the derived parameters can often be highly nonlinear, which can significantly increase the complexity of the model. Furthermore, determining some parameters requires intrusive measurements of plasma properties, such as the ion density, which can only be measured using a Langmuir probe [36].

Therefore, as a supplement to the EEC model, a parameter identification method is introduced in this chapter, which linearizes the electric parameters in the model within a reasonable operating range. The method is entirely based on nonintrusive electric measurements, which includes the voltage and current waveforms on the converter side.

4.1 Parameter identification procedure

In practice, the sheath capacitance C_{sh1} and C_{sh2} are voltage-dependent and nonlinear. If and only if the optimal operating point is reached, u_{sh1} and C_{sh1} can remain

This chapter is based on [183].

constant during the charge phase [138]. Moreover, the ion current I_{i1} and I_{i2} are theoretically constant and voltage-independent in a high-voltage sheath, as can be derived from (1.28) and (1.31). However, in practice, the ion currents have been found voltage-dependent, and they generally increase with the voltage over the sheath [156, 157].

In this parameter identification method, all of these parameters are assumed to be constant around the optimal operating point. Specially, C_{sh2} and I_{i2} are assumed to be zero for simplicity. In addition, C_{sub} is considered constant since the processing depth of the substrate is negligible compared to its height. C_t is also assumed to be constant, as each surface area and distance remain unchanged.

In the previous chapter, an auto-tuning method has been introduced to determine the optimal voltage slope rate. This method involves applying different voltage slope rates $\dot{u}_{out,x}$ $(x \in 1, 2, 3, ..., n)$ spanning over an adequate range with sufficiently small gradients and measuring the resultant currents $i_{out,x}$ $(x \in 1, 2, 3, ..., n)$. An effective capacitance C_{eff} and effective current I_{eff} can be approximated at different $\dot{u}_{out,x}$ based on (3.5) and (3.6). The auto-tuning method reveals that at the optimal operating point, both C_{eff} and I_{eff} reach their minimum values, which equivalently leads to

$$C_t = \min\left(C_{eff,x}\right) = C_{eff,k} \tag{4.1}$$

and

$$I_{i1} = -\min\left(I_{eff,x}\right) = -I_{eff,k}. \tag{4.2}$$

Consequently, following the same procedure as auto-tuning, the value of C_t and I_{i1} can be obtained.

It should be pointed out that I_{i1} can also be calculated from (3.7) after obtaining C_t. Theoretically, the minimum values of C_{eff} and I_{eff} should be achieved at the same $\dot{u}_{out}$, thus both methods should yield the same result.

The above analysis utilizes a special case of the proposed circuit model at the optimal operating point to calculate the exact value of C_t and I_{i1}. The benefit of this method is that the values of C_{sh1} and C_{sub} are not required, making the method immune to the nonlinear C_{sh1} effect. Therefore, the identification of C_t and I_{i1} is expected to be highly accurate.

Nonetheless, the value of C_{sh1} has to be linearized and assumed to be constant within the covered range of $\dot{u}_{out,x}$ $(x \in 1, 2, 3, ..., n)$. Defining a constant equivalent capacitance C_{eq} and current I_{eq} by

$$C_{eq} = \frac{C_{sh1}C_{sub}}{C_{sh1} + C_{sub}} + C_t \tag{4.3}$$

and

$$I_{eq} = \frac{C_{sub}}{C_{sub} + C_{sh1}} I_{i1}, \tag{4.4}$$

(3.2) can be rewritten as

$$i_{out} = C_{eq}\dot{u}_{out} - I_{eq}. \tag{4.5}$$

A linear regression can be determined within the operating range to estimate the values of C_{eq} and I_{eq} with the least squares method by minimizing the function

$$f(C_{eq}, I_{eq}) = \sum_{x=1}^{n} \left(C_{eq}\dot{u}_{out,x} - I_{eq} - i_{out,x}\right)^2. \tag{4.6}$$

Both C_{eq} and I_{eq} are extracted from the linear regression. In other words, both values are equivalent to the averaged values over the applied $\dot{u}_{out}$ range. It is important to note that the identified values of C_{eq} and I_{eq} are dependent on $\dot{u}_{out}$. Thus, applying a different range of $\dot{u}_{out}$ may lead to different C_{eq} and I_{eq}.

Based on the practical measurements, C_{sub} (typically in nanofarad magnitude) is usually much larger than the sheath capacitance (typically in sub-nanofarad magnitude). Therefore, (4.3) can be further simplified by

$$C_{eq} \approx C_{sh1} + C_t. \tag{4.7}$$

As a result, C_{sh1} can be approximated by

$$C_{sh1} = C_{eq} - C_t. \tag{4.8}$$

Moreover, C_{sub} can be further solved from (4.4), yielding

$$C_{sub} = \frac{C_{sh1} I_{eq}}{I_{i1} - I_{eq}}. \tag{4.9}$$

At this stage, the parameters essential for the charge phase have been fully identified. However, during the discharge phase, there is a resonance in the transient response with a frequency of f_r in the loop. This resonance arises from the LC network formed by the plasma reactor and the stray inductance L_s. The value of L_s can be determined by

$$L_s = \frac{1}{4\pi^2 f_r^2 \left(C_t + C_{sub}\right)}, \tag{4.10}$$

once the optimal operating point is reached.

During the discharge phase, capacitors C_{sh1}, C_{sh2} and C_{sub} should be discharged through resistor R_p within hundreds of nanoseconds. Therefore, during this phase, R_p can be approximated by

$$R_p = \frac{\tau}{C_{sub}}, \tag{4.11}$$

where τ is the time constant of the RC circuit. Based on the RC discharge circuit, it takes about 2.3τ to discharge the capacitor voltage to 10% of the initial value. Given that the sheath collapsing and reforming can take hundreds of nanoseconds, a typical value of τ can be tens of nanoseconds.

If the power converter is coupled with the reactor table via a blocking capacitor, as depicted in Figure 2.2, the net output current should be balanced during the steady state due to the blocking capacitor. This mechanism has been analyzed in Section 2.1.2. According to (2.18), during the post-discharge phase, R_p can be calculated by

$$R_\mathrm{p} \approx \frac{T_\mathrm{pulse} V_\mathrm{d}}{T_\mathrm{slope} I_\mathrm{i2}}. \tag{4.12}$$

It is important to note that a Debye sheath is built up on the reactor table during the post-discharge phase. Therefore, ideally, there should be no net current through the sheath. However, in practice, due to various parasitic components and resonance, a current could be observed.

It should be clarified that a different value of R_p should be used during the post-discharge phase compared to the discharge phase. In the simulation model shown in Figure 2.9, two different resistors are used for distinction, of which R_p is obtained from (4.11), while the total value of R_pd and R_p is determined by (4.12). Specially, if I_i2 is neglected, R_p becomes infinite during the post-discharge phase, as derived from (4.12). In practice, a sufficiently large resistance can be used for R_p during the post-discharge phase. With the value of R_p, all circuit parameters have been extracted.

4.2 Experimental verification

4.2.1 Example implementation

This section provides an illustrative example of the experimental implementation of the proposed parameter identification method. The experimental setup was the same as that introduced in Section 2.2.1. Specifically, the operating condition with a four-inch wafer at 200 W ICP power was utilized as an example.

As analyzed in Section 4.1, the dataset of the output voltage with different slope rates $\dot{u}_{\mathrm{out},x}$ and the output current $i_{\mathrm{out},x}$ can be employed to identify the effective capacitance C_eff and current I_eff, as per (3.5) and (3.6). The waveforms of $\dot{u}_{\mathrm{out},x}$ and $i_{\mathrm{out},x}$ are illustrated in Figure 3.4. The identified values of C_eff and I_eff are depicted in Figure 4.1(a).

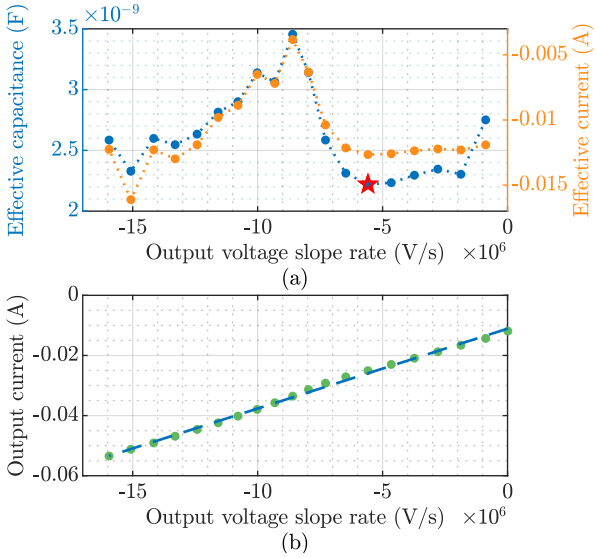


Figure 4.1 The measured dataset of (a) the effective capacitance C_{eff} and effective current I_{eff}, and (b) the output current and its linear regression at different voltage slope rates. The red pentagon in (a) indicates the optimal slope rate, at which $C_{\text{t}} = C_{\text{eff}}$.

It can be observed that C_{eff} and I_{eff} exhibit a similar trend with the varying $\dot{u}_{\text{out}}$. This is due to the fact that they share the same coefficient of $C_{\text{sh1}} \left(C_{\text{sh1}} + C_{\text{sub}}\right)^{-1}$ according to (3.3) and (3.4). In theory, C_{eff} and I_{eff} should reach their minimum values at the same $\dot{u}_{\text{out}}$. However, it can be observed that C_{eff} reaches its minimum value when $\dot{u}_{\text{out}} = -5.586 \cdot 10^6\,\text{V}\,\text{s}^{-1}$, as denoted by the red pentagon in Figure 4.1(a), while I_{eff} only reaches its local minimum. As $\dot{u}_{\text{out}}$ becomes more negative, I_{eff} exhibits a trend towards a more negative value than the local minimum. This deviation occurs because the ion current I_{i1} is not voltage-independent, as assumed in the previous analysis. Instead, I_{i1} increases when $\dot{u}_{\text{out}}$ becomes more negative, *i.e.*, the voltage drop on the substrate sheath increases. To keep the model simple and functional within a reasonable slope rate range, the effective current is chosen at the same operating point where the minimum effective capacitance is obtained. Consequently, $C_{\text{t}} = \min(C_{\text{eff},x}) = 2.22\,\text{nF}$, and $I_{\text{i1}} = -\min(I_{\text{eff},x}) \approx 0.012\,65\,\text{A}$.

Figure 4.1(b) shows the measured output currents at different voltage slopes and their linear regression. The resultant linearized equivalent capacitance and current are $C_{\text{eq}} = 2.66\,\text{nF}$ and $I_{\text{eq}} = 0.0111\,\text{A}$, respectively. C_{sh1} and C_{sub} can be solved by applying (4.8) and (4.9), which yield $C_{\text{sh1}} = 0.435\,\text{nF}$ and $C_{\text{sub}} = 3.09\,\text{nF}$.

The resonance in the waveform has been measured to have a frequency of $f_{\text{r}} =$

Table 4.1 The identified parameters for different wafers at different ICP powers.

Wafer	Four-inch		Eight-inch	
ICP power (W)	200	600	200	600
C_t (nF)	2.22	2.36	2.31	2.34
C_{sub} (nF)	3.09	4.35	2.84	3.65
C_{sh1} (nF)	0.435	0.386	0.409	0.402
I_{i1} (mA)	12.65	15.26	11.99	15.24

14 MHz. The stray inductance L_s can then be determined by (4.10) and is 25 nH. In addition, an equivalent series resistance R_s is present in the loop, with a value of 1.5 Ω. Apart from these, selecting $\tau = 50$ ns, as introduced in Section 4.1, R_p can be calculated using (4.11) and is found to be 16.2 Ω. The value of R_{pd} should be sufficiently large since I_{i2} is neglected, as explained in Section 4.1. In this case, R_{pd} is selected to be 6000 Ω to ensure that the output current during the post-discharge phase is close to the measured value.

In summary, all the parameters have been identified and are summarized in Table 2.1. These parameters have been substituted back into the circuit simulation, and the simulation results match well with the experiments, as illustrated in Chapter 2. This underscores the effectiveness and accuracy of the parameter identification method.

4.2.2 Discussion

The same parameter identification procedure, and electric waveform and IED simulations were carried out for an eight-inch wafer and at different ICP powers. The resultant identified parameters are listed in Table 4.1. As shown in the table, C_t is consistent and around 2.3 nF for different wafers with different ICP powers, which is logical as the area of and the distance between the table and the reactor wall remain constant. The extracted C_{sub} is of several nanofarads for both applied wafers.

However, the extracted C_{sub} of the same wafer is expected to be the same with different ICP powers, yet the results show deviation. The reason is that C_{sub} is calculated based on multiple extracted parameters, including C_{sh1}, I_{eq}, and I_{i1}, according to (4.9). As inaccuracy occurs when identifying each parameter, it accumulates on C_{sub}. Therefore, the identification of C_{sub} is more sensitive.

The values of C_{sh1} that were identified for different wafers with varying ICP powers are around 0.4 nF. Furthermore, the current I_{i1} shows a positive correlation with the ICP power. An intriguing observation is that despite the eight-inch wafer being four times larger than the four-inch wafer, their values of C_{sh1} and I_{i1} are still similar

when subjected to the same ICP powers. This similarity can be attributed to the neglect of C_{sh2} and I_{i2}. In (4.3), the equivalent capacitance C_{eq} is defined, and in (4.6), its value is obtained through linear regression, as shown in Figure 4.1(b). This value is derived based on the simplified system outlined in (3.7), which disregards C_{sh2} and I_{i2} in the actual system as described by (3.2). In other words, the actual definition of C_{eq} is given by

$$C_{eq} = \frac{C_{sh1}C_{sub}}{C_{sh1} + C_{sub}} + C_{sh2} + C_t \approx C_{sh1} + C_{sh2} + C_t. \tag{4.13}$$

As a result, the previously identified C_{sh1} actually represents the sum of real values of C_{sh1} and C_{sh2}. Similarly, the previously identified I_{i1} is the sum of real I_{i1} and I_{i2} as stated in (3.9). Since the total exposed area (equivalent to the combined area of the solid and tilled parts of the table, as depicted in Figure 1.9) remains constant, the sum of sheath capacitances and ion currents should roughly maintain similar values even if different wafers are used. This effect also suggests that an additional sheath exists between the plasma and the exposed part of the table.

In summary, this section identifies the parameters of the EEC model based on experimental measurements. The identified parameters are then used to simulate the EEC model, which is used to validate the accuracy of the parameter identification method. These experiments were conducted on two wafers of different sizes and with different ICP powers, resulting in similar outcomes, demonstrating the broad applicability of the method.

4.3 Conclusion

A parameter identification method is proposed to fulfill the simulation of the EEC model at the circuit level. The method relies entirely on electric measurements and requires only the output voltage and current waveforms. Both waveforms can be easily measured, and the measurements are nonintrusive to the process. The identification process linearizes all the components, including the sheath capacitances and currents, and obtains all the parameters through simple mathematical manipulation of the electrical waveforms. Once obtained, the parameters can be substituted back into the model for circuit simulation. The simulation and experimental results validate the effectiveness and accuracy of the proposed method.

Essentially, the proposed parameter identification method aims to reproduce the electrical responses and the IED of the plasma processing in circuit simulation. Therefore, non-linearity of the parameters is not taken into account, which might induce errors compared to the actual values. In future research, plasma diagnostic

techniques with ultra-high accuracy can be implemented for comparison. Furthermore, it is recommended to improve the accuracy of the parameter identification by taking non-zero values of C_{sh2} and I_{i2} into consideration.

CHAPTER 5

Bias converter

PREVIOUS chapters have introduced the EEC model of plasma processing and have demonstrated that tailored waveform biasing is advantageous for obtaining the narrowest IED. This tailored waveform is composed of a negative voltage slope followed by a voltage pulse, and both the magnitude and time duration of these components should be controllable to accommodate varying operating conditions. However, this irregular profile is scarcely used in the electronics world, and only a few prior studies and commercial products have set foot in this field.

Previously, the unavailability of a complete EEC was a significant obstacle to properly designing a bias converter capable of generating such a tailored waveform. Practically, it is impossible to generate a perfect tailored waveform with either an ideal linear voltage slope or an infinitely fast voltage pulse, due to the presence of various parasitic components in electronics. Therefore, compromises must be made when designing the bias converter. With the proposed EEC model in Chapter 2, the effects of any nonideal tailored waveform on the IED can be analyzed, and reasonable design choices can be made.

In this chapter, basic topology variants for generating the tailored waveform are derived and compared, and their limitations are analyzed. A novel bias converter concept is proposed, which approximates the tailored waveform by a multilevel waveform, thus enabling the multilevel converters to be used in this application. The multilevel waveform adds extra voltage ripples on the substrate surface, and

This chapter is based on [185, 187].

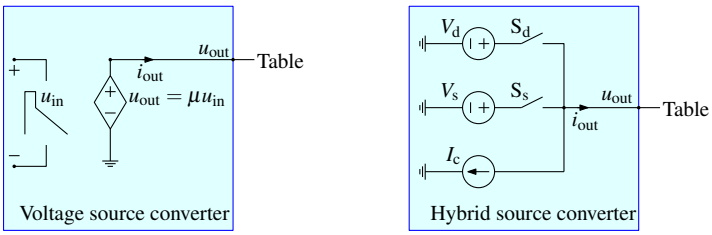


Figure 5.1 The basic topology variants: (a) a voltage source converter and (b) a hybrid source converter.

this effect is analyzed. Adding an extra filter inductor can reduce the voltage ripple, thus narrowing the IED. Based on the analysis, a specific multilevel topology is proposed in this application, and its operating principle is provided.

5.1 Existing bias converter concept

5.1.1 Voltage source converter

The most straightforward concept for a bias converter is a voltage source converter that directly amplifies the input signals, as depicted in Figure 5.1(a). The repetition frequency of the tailored can be in the hundreds of kilohertz range. Due to the voltage pulse with a fast rising and falling edge, the tailored waveform contains much higher-order harmonics. Therefore, the bandwidth requirement on the bias converter is very challenging.

In the earliest applications of tailored waveform biasing, linear amplifiers were used to generate the waveform. For example, a class-A amplifier (ENI A-500 manufactured by Electronic Navigation Industries) was adopted in [179], and a linear amplifier (150A250 manufactured by Amplifier Research) with a push-pull MOSFET (class-B or class-AB) was used in [176]. These linear amplifiers have the benefit of a high output bandwidth up to hundreds of megahertz, making them capable of delivering the tailored waveforms with a high repetition frequency. However, linear amplifiers are not energy-efficient, and their typical input/output impedance of 50 Ω requires an impedance matching network to maximize output power, which adds additional loss to the system.

SMPCs are known as an energy-efficient alternatives to linear amplifiers. Theoretically, switched-mode voltage sources can also generate the tailored waveform. For the most common buck converter with pulse-width modulation (PWM), an LC

filter is required to eliminate the high-frequency output components, which limits its bandwidth to roughly one-tenth of its switching frequency. Therefore, the high bandwidth requirement is very challenging, as the switching frequency of power semiconductors is limited, especially at high voltage.

In [41], half-bridge converters are interleaved to increase the effective switching frequency and bandwidth. However, to obtain the required bandwidth, a large number of interleaved half-bridge converters are required, which tremendously increases the components used. Additionally, interleaving may lead to severe issues, such as high circulating current.

5.1.2 Hybrid source converter

Other than a voltage source converter, a new concept for a hybrid source converter (also an SMPC) has emerged in recent years, as depicted in Figure 5.1(b). This hybrid source converter consists of at least two voltage sources (including the ground connection), a current source, and multiple power switches.

As Chapter 2 has shown, a discharge voltage V_d is necessary to discharge all substrate and sheath capacitors, and a negative voltage V_s is required to restart the process with the correct initial substrate surface potential. Therefore, to generate the voltage pulse, at least two voltage sources are required. Power switch $\mathrm{S_d}$ and $\mathrm{S_s}$ are used to select the source that connects to the output and cannot be on at the same time.

In these SMPCs, the voltage slope is generated by the current source, which sinks a constant current from the output. Since the load is capacitive, a negative voltage slope can be obtained by a negative dc current, and *vice versa*. Therefore, after disconnecting all the voltage sources once u_out reaches V_s, a linearly decreasing voltage slope results from the current source. Note that at the optimal operating point, the current source I_c should deliver a negative output current as indicated in (2.14).

This hybrid source converter has the advantage of significantly reduced switching frequency when compared to the switched-mode voltage source converter. This is because power switch $\mathrm{S_d}$ and $\mathrm{S_s}$ are switched on and off only once in each fundamental period. With the help of wide-bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) transistors, a high repetition frequency of megahertz can be reached. Furthermore, all the voltage sources and the current source are dc, requiring only minimal bandwidth.

These benefits have made the hybrid source converter concept a popular choice in tailored waveform biasing applications. Most of the existing designs are variants of this concept [18, 33, 40, 48–50, 74, 91, 121, 123, 170, 187, 189]. A notable difference is

that some of them also use more than two voltage sources to achieve more flexibility in waveform generation [40, 48–50, 170].

The current source is typically realized by an inductor in series with a controllable voltage source. This voltage source is used to maintain the voltage-second balance of the inductor at an average of zero and can be either dc or alternating current (ac). Any voltage over the inductor creates an inductor current error. To maintain a constant substrate surface potential and a narrow IED, the inductor current should be as constant as possible, which requires a very small inductor current error. This can be realized by ensuring a low inductor voltage or by using a sufficiently large inductance.

One straightforward method to reduce the inductor current error is to increase the repetition frequency of the bias waveform, since the integral has less time to accumulate. Nevertheless, this frequency is inherently limited by the capability of the power semiconductors, as a higher switching frequency significantly increases their switching losses. Meanwhile, an inductor has a self-resonant frequency due to its parasitic capacitance, which also limits the maximum repetition frequency in practice.

In [48, 49], a half-bridge converter is used to generate a high-frequency rectangular waveform, which helps balance the inductor voltage and reduce the inductor current ripple, unlike in [18, 40, 74, 91], where a dc voltage source is used. To minimize the inductor current error, this half-bridge should push its switching frequency to much higher than the repetition frequency. However, this is also inherently limited by the capability of the power semiconductors.

In some designs [40, 91, 187, 189], the current source (inductor) is disconnected from the output node during the discharge and post-discharge phase. This helps reduce the inductor current error since the voltage pulse is not applied to the inductor. However, since the inductor current is continuous, a freewheeling path should be provided for the inductor, which requires specific switching sequence control, as explained in [187, 189].

Apart from these, increasing the inductance can also be effective in reducing the inductor current error. Nonetheless, a larger inductance typically leads to a larger parasitic capacitance and hence a lower self-resonant frequency. This effect in turn limits the repetition frequency of the tailored waveforms.

In summary, the inductor current error should be minimized in the hybrid source converter concept to obtain the narrowest IED. Various solutions have been proposed to achieve this goal, including increasing the repetition frequency, disconnecting the inductor during the discharge and post-discharge phase, and increasing inductance value. However, these solutions are limited by the switching frequency of the power

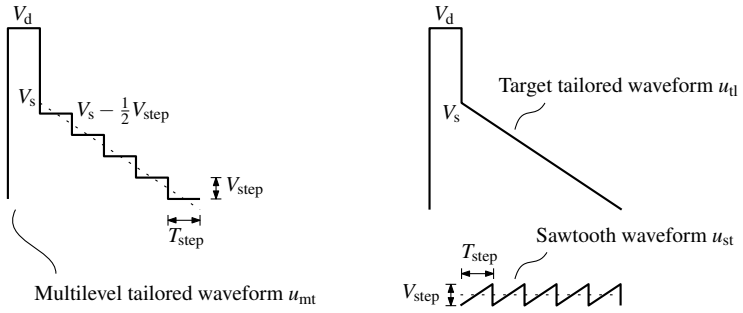


Figure 5.2 A multilevel tailored waveform can be seen as a superposition of the target tailored waveform and a sawtooth waveform.

semiconductors or inductor parasitic capacitance, making it difficult to scale to a higher voltage rating or repetition frequency. Therefore, a more scalable converter concept is required.

5.2 Multilevel bias converter concept

5.2.1 Multilevel tailored waveform

In power electronics, the term "scalability" is often associated with multilevel converters due to their primary advantage. It naturally raises the question of whether multilevel converters can be effectively utilized in this application. Figure 5.2 illustrates a multilevel tailored waveform u_{mt}, which can be generated by multilevel converters. In comparison to a tailored waveform, it employs monotonically decreasing voltage levels with a voltage step size V_{step} and a time step T_{step} to approximate the voltage slope during the charge phase. It can be viewed as a superposition of the tailored waveform u_{tl} and a sawtooth waveform u_{st}, as shown in Figure 5.2 and expressed as

$$u_{mt} = u_{tl} + u_{st}. \tag{5.1}$$

The slope rate of the tailored waveform is determined by $V_{step}T_{step}^{-1}$. The sawtooth waveform has a peak-to-peak amplitude V_{step} and a repetition period T_{step}.

The tailored waveform is the target output voltage, while the sawtooth waveform represents a disturbance in the output voltage, which affects the substrate surface potential and broadens the IED. To quantitatively investigate its effect, first consider the equivalent circuit of the load during the charge phase, as depicted in Figure 2.5(a). As explained in Chapter 2, for simplicity, parameters R_p, I_{i2}, and C_{sh2} can be neglected during the charge phase, and D_1 and D_2 are blocking. Consequently, the

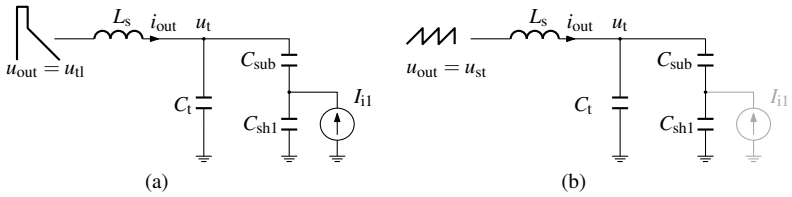


Figure 5.3 The equivalent circuit during the charge phase, which can be seen as a superposition of two separate input source as (a) a tailored waveform u_{tl} and current source I_{i1}, and (b) a sawtooth waveform u_{st}.

remaining components C_t, C_{sub}, C_{sh1}, and L_s form an LC circuit, and I_{i1} and u_{out} can be seen as the external sources applied to the circuit. If we assume these parameters to be constant, it becomes a linear time-invariant (LTI) system during the charge phase, as derived in Appendix B.

One of the fundamental properties of an LTI system is its superposition principle [73]. Therefore, for a given input vector

$$\boldsymbol{u}(t) = \begin{pmatrix} u_{out} \\ I_{i1} \\ 0 \end{pmatrix} = \begin{pmatrix} u_{mt} \\ I_{i1} \\ 0 \end{pmatrix}, \tag{5.2}$$

the state variable $\boldsymbol{x}(t)$ and the output $\boldsymbol{y}(t)$ can be calculated as the sum of the results from two separate inputs as shown in Figure 5.3(a) and (b), respectively, where

$$\boldsymbol{u}(t) = \begin{pmatrix} u_{tl} \\ I_{i1} \\ 0 \end{pmatrix} + \begin{pmatrix} u_{st} \\ 0 \\ 0 \end{pmatrix}. \tag{5.3}$$

The result from the tailored waveform u_{tl} in Figure 5.3(a) has already been analyzed in Chapter 2. To maintain $u_{C_{sh1}}$ constant, the slope rate is dominated by

$$\frac{V_{step}}{T_{step}} = \frac{I_{i1}}{C_{sub}}. \tag{5.4}$$

On the other hand, in Figure 5.3(b), the stray inductance L_s and the capacitors form a low-pass filter, while C_{sub} and C_{sh1} form a capacitive voltage divider. As a result, the sawtooth waveform u_{st} generates a filtered and divided voltage ripple on the substrate surface potential. Assuming a periodical sawtooth signal $u_{st}(t) = u_{st}(t + T_{step})$ and

$$u_{st}(t) = \frac{V_{step}}{T_{step}} t - \frac{1}{2} V_{step}, t \in \left[0, T_{step}\right), \tag{5.5}$$

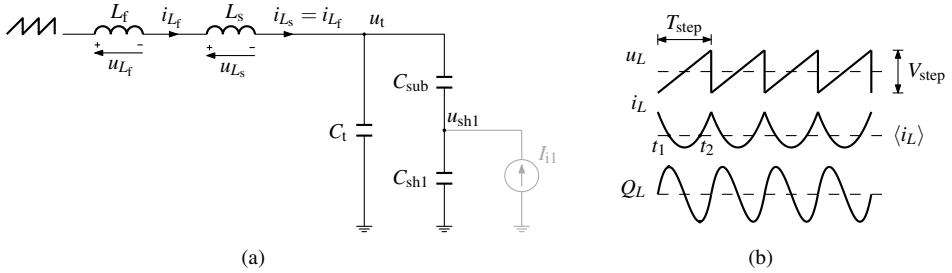


Figure 5.4 (a) The equivalent circuit during the charge phase with an extra filter inductor. Here u_{L_f} and u_{L_s} are the voltage over L_f and L_s, and i_{L_f} and i_{L_s} are the current through L_f and L_s, respectively. (b) The inductor voltage, current, and charge accumulation caused by the current error.

which can be represented by a Fourier series as

$$u_{st}(t) = \sum_{n=1}^{\infty} -\frac{V_{step}}{n\pi} \sin\left(\frac{2\pi n}{T_{step}} \cdot t\right). \tag{5.6}$$

The transfer function of the low-pass filter be expressed as

$$H_{lp}(s) = \frac{1}{s^2 L_s \left(C_t + \frac{C_{sh1} C_{sub}}{C_{sub}+C_{sh1}}\right) + 1}. \tag{5.7}$$

Therefore, the harmonic components of the substrate surface potential are found to be

$$A_{sh1}(n) = \frac{C_{sub}}{C_{sub} + C_{sh1}} \frac{V_{step}}{n\pi} H_{LC}(j\frac{2\pi n}{T_{step}}). \tag{5.8}$$

5.2.2 Extra filter inductor

The previous analysis has demonstrated that the sawtooth waveform creates voltage ripples on the substrate surface, which broadens the IED. The low-pass filter formed by the stray inductance L_s and the capacitive load reduces the amplitude of the voltage ripple on the substrate surface, making it smaller than that of the the sawtooth waveform u_{st}. However, in practice, the stray inductance in the loop is relatively small, and the cut-off frequency of the low-pass filter can be much higher than the sawtooth frequency, making the filter less effective.

To achieve the narrowest IED, it is essential to minimize the voltage ripple. This can be accomplished by reducing V_{step}, which decreases the amplitude of the sawtooth waveform. However, V_{step} and T_{step} jointly determine the slope rate, a smaller V_{step} also calls for a smaller T_{step} for a given operating condition. Consequently,

this leads to a higher switching frequency that is limited by the capability of the power semiconductors. Besides, a smaller V_{step} necessitates more voltage levels and components in a multilevel topology for a fixed output voltage requirement. Therefore, there is a limit to reducing V_{step}.

On the flipside, an extra filter inductor L_{f} can be added in series with L_{s} to further filter and reduce the voltage ripple on the substrate surface, as shown in Figure 5.4(a). Given a required voltage ripple Δu_{sh1}, the minimum required L_{f} can be calculated for a fixed V_{step} and T_{step}.

Assuming that L_{f} is sufficiently large and denoting $L = L_{\text{f}} + L_{\text{s}}$, it can be obtained that $u_L = u_{L_{\text{f}}} + u_{L_{\text{s}}}$ and $i_L = i_{L_{\text{f}}} = i_{L_{\text{s}}}$. As shown in Figure 5.4, i_L can be represented by

$$i_L = \langle i_L \rangle + \hat{i}_L, \tag{5.9}$$

where $\langle i_L \rangle$ is the dc value of the inductor current, which equals to $-I_{\text{c}}$, and $\hat{i}_L$ is the inductor current error. For the sawtooth waveform u_{st}, it has $u_{\text{t}} = 0$ and $u_L = u_{\text{st}}$, and thus, $\hat{i}_L$ can be calculated as

$$\hat{i}_L(t) = \int_0^t \frac{u_L(\tau)}{L} \mathrm{d}\tau = \frac{V_{\text{step}}}{2LT_{\text{step}}} t^2 - \frac{V_{\text{step}}}{2L} t + i_L(0), \tag{5.10}$$

The charge accumulation by the current error is governed by

$$Q_L(t) = \int_0^t \hat{i}_L(\tau) \mathrm{d}\tau = \frac{V_{\text{step}}}{6LT_{\text{step}}} t^3 - \frac{V_{\text{step}}}{4L} t^2 + i_L(0)t. \tag{5.11}$$

During the steady state, this charge accumulation in one cycle should be zero, which leads to

$$Q_L(T_{\text{step}}) = \frac{V_{\text{step}}}{6LT_{\text{step}}} T_{\text{step}}^3 - \frac{V_{\text{step}}}{4L} T_{\text{step}}^2 + \hat{i}_L(0) T_{\text{step}} = 0. \tag{5.12}$$

Therefore, $\hat{i}_L(0)$ can be given by

$$\hat{i}_L(0) = \frac{V_{\text{step}} T_{\text{step}}}{12L}. \tag{5.13}$$

Consequently, the inductor current error can be written as

$$\hat{i}_L(t) = \frac{V_{\text{step}}}{2LT_{\text{step}}} t^2 - \frac{V_{\text{step}}}{2L} t + \frac{V_{\text{step}} T_{\text{step}}}{12L}. \tag{5.14}$$

At time t_1 when $\hat{i}_L(t) = 0$, as shown in Figure 5.4(b), the charge accumulation of the current error reaches its maximum, and at t_2 its minimum, which is governed by

$$\hat{i}_L(t_1) = \hat{i}_L(t_2) = \frac{V_{\text{step}}}{2LT_{\text{step}}} t^2 - \frac{V_{\text{step}}}{2L} t + \frac{V_{\text{step}} T_{\text{step}}}{12L} = 0. \tag{5.15}$$

Consequently, $t_1 = \frac{3-\sqrt{3}}{6} T_{\text{step}}$ and $t_2 = \frac{3+\sqrt{3}}{6} T_{\text{step}}$. The charge accumulation ΔQ at t_1 and t_2 is determined by

$$Q_L(t_1) = -Q_L(t_2) = \frac{\sqrt{3} V_{\text{step}} T_{\text{step}}^2}{216L}. \tag{5.16}$$

Due to the capacitive current divider formed by C_{t}, C_{sub}, and C_{sh1}, the maximum charge difference going through C_{sh} is given by

$$\begin{aligned} \Delta Q_{C_{\text{sh1}}} &= (Q_L(t_1) - Q_L(t_2)) \cdot \frac{\frac{C_{\text{sh1}} C_{\text{sub}}}{C_{\text{sh1}} + C_{\text{sub}}}}{\frac{C_{\text{sh1}} C_{\text{sub}}}{C_{\text{sh1}} + C_{\text{sub}}} + C_{\text{t}}} \\ &= \frac{\sqrt{3} V_{\text{step}} T_{\text{step}}^2}{108L} \cdot \frac{C_{\text{sh1}} C_{\text{sub}}}{C_{\text{sh1}} C_{\text{sub}} + C_{\text{t}} C_{\text{sh1}} + C_{\text{t}} C_{\text{sub}}}. \end{aligned} \tag{5.17}$$

This maximum charge difference translates to the peak-to-peak voltage ripple on the substrate surface, which can be calculated as

$$\Delta u_{\text{sh1}} = \frac{\Delta Q_{\text{sh1}}}{C_{\text{sh1}}} = \frac{\sqrt{3}}{108} \cdot \frac{1}{L} \cdot \frac{C_{\text{sub}} V_{\text{step}} T_{\text{step}}^2}{C_{\text{sh1}} C_{\text{sub}} + C_{\text{t}} C_{\text{sh1}} + C_{\text{t}} C_{\text{sub}}} \tag{5.18}$$

Substituting (5.4) into (5.18) leads to

$$\Delta u_{\text{sh1}} = \frac{\Delta Q_{\text{sh1}}}{C_{\text{sh1}}} = \frac{\sqrt{3}}{108} \cdot \frac{1}{L} \cdot \frac{I_{\text{i1}} T_{\text{step}}^3}{C_{\text{sh1}} C_{\text{sub}} + C_{\text{t}} C_{\text{sh1}} + C_{\text{t}} C_{\text{sub}}}. \tag{5.19}$$

For a given maximum allowed Δu_{sh1}, the minimum filter inductance is then calculated by

$$L_{\text{f}} = \frac{\sqrt{3}}{108} \cdot \frac{1}{\Delta u_{\text{sh1}}} \cdot \frac{I_{\text{i1}} T_{\text{step}}^3}{C_{\text{sh1}} C_{\text{sub}} + C_{\text{t}} C_{\text{sh1}} + C_{\text{t}} C_{\text{sub}}} - L_{\text{s}}. \tag{5.20}$$

Therefore, for a fixed operating condition, it follows that L_{f} is proportional to T_{step}^3. Although increasing L_{f} can further reduce the voltage ripple on the substrate surface, it does come with a price. Specifically, a larger L_{f} causes a slower voltage rising and falling edges, leading to a higher pulse duty cycle. As explained in Section 2.2, this can cause more ions to fall into a lower energy spectrum, which is not desirable. Hence, to obtain a higher slope duty cycle without a large L_{f}, a larger number of voltage levels are required to reduce T_{step} and obtain an acceptable slope duty cycle. Typically, more than 10 voltage levels are needed to achieve a slope duty cycle higher than 80 %, as elaborated in the following sections.

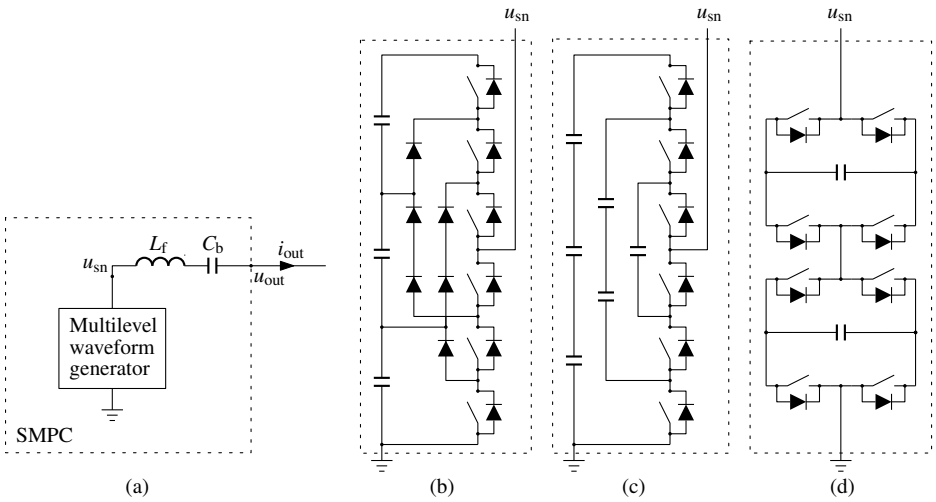


Figure 5.5 (a) A basic configuration for the multilevel bias converter. Here u_{sn} represents the switched-node voltage. (b) Flying capacitor converter. (c) Neutral-point-clamped converter. (d) Cascaded H-bridge converter converter.

5.3 Multilevel bias converter topology

5.3.1 Topology evaluation

Based on the analysis presented above, a basic configuration for the multilevel bias converter can be derived, as shown in Figure 5.5(a). It comprises a multilevel waveform generator, a filter inductor L_f, and a blocking capacitor C_b.

Technically, the multilevel waveform generator can be of various multilevel topologies [89], including the most common ones such as the neutral-point-clamped converter (NPC) [120], the flying capacitor converter (FCC) [117], and the cascaded H-bridge converter (CHB) [32], as illustrated in Figure 5.5(b), (c), and (d), respectively. However, as explained in the previous section, a higher number of voltage levels is beneficial for both a smaller voltage ripple on the substrate surface and a higher slope duty cycle. Thereby, the scalability of each topology is the main goal.

Unfortunately, the NPC or FCC can hardly be scaled to a higher number of voltage levels due to the drastic increase in the number of components required. Denoting the number of voltage levels by n and assuming the same components are used, the required number of diodes for the NPC is $(n-1)(n-2)$, and the required number of the flying capacitors for FCC is $\frac{1}{2}(n-1)(n-2)$ (not counting $n-1$ dc-link capacitors), as listed in Table 5.1. Both of these figures are quadratic in relation

Table 5.1 The comparison of various multilevel topologies.

Topology	Number		
	Diodes	Capacitors	Active switches
NPC	$(n-1)(n-2)$	$n-1$	$2(n-1)$
FCC	-	$\frac{1}{2}(n-1)(n-2)$	$2(n-1)$
CHB	-	$\frac{1}{2}(n-1)$	$2(n-1)$

to the number of voltage levels, making them unsuitable in this application.

For the CHB, the number of components increases linearly with the number of voltage level. Each H-bridge submodule has three different output states. For the most typical symmetrical CHB, assuming m submodules, the number of available voltage levels is $n = 2m + 1$. The numbers of components for the CHB are shown in Table 5.1. Therefore, compared to NPC and FCC, it is more suitable for a higher number of voltage levels.

As shown in Figure 5.5(d), each submodule of the CHB is supplied by a dc-link capacitor. Therefore, the voltage over each capacitor should be balanced during the steady state by utilizing the redundant states of the CHB converter. However, due to the complexity of the load, voltage balancing might not be guaranteed for all submodules.

Isolated dc supplies can serve as alternatives to these dc-link capacitors. In practice, a capacitive coupling path between the output of the isolated supply and PE is inevitable, typically caused by the parasitic capacitance of the isolating transformer. Such a capacitive coupling path induces high common-mode (CM) current during the switching transients of the power semiconductors. This CM current increases the switching current, reduces the switching time, and leads to higher switching losses. Besides, with more submodules stacked up, the switches experience more capacitive coupling to PE, thus suffering from more severe electromagnetic interference (EMI) issues. Therefore, if CHB with isolated dc supplies is used, the number of submodules should be minimized to reduce the EMI effect.

The asymmetrical CHB is a technique used to decrease the number of submodules required. In this topology, the voltage of each submodule differs. Specially, they can be in a binary or trinary ratio [37, 172]. In a binary asymmetrical CHB, the number of voltage levels n grows exponentially with the number of submodules m, as $n = 2^{m+1} - 1$. In a trinary one, $n = 3^m$. Although the trinary asymmetrical CHB provides the highest number of voltage levels, it does not have a single redundant state, making the use of isolated dc supplies a must due to the inability to balance voltage. Conversely, the binary asymmetrical CHB has $3^m - 2^{m+1} + 1$ redundant

states.

Besides, the higher number of voltage levels for the asymmetrical CHB comes at a cost of higher switching frequency, since the switching frequency of the submodules is proportional to its dc-link voltage, meaning that submodules with lower dc-link voltage have a higher switching frequency than those with higher dc-link voltage. Therefore, if the asymmetrical CHB is employed, the trade-off between a higher number of voltage levels and an acceptable switching frequency should be taken into account.

Apart from the topologies depicted in Figure 5.5, another option is the modular multilevel converter (MMC), which is attracting more and more attention as a multilevel topology with excellent scalability. The most typical building submodule of the MMC is a half-bridge with dc-link capacitor. Like the CHB, voltage balancing is also required for the MMC, thus making it inapplicable without isolated supplies. Recently, a new family of multilevel converters named the extended commutation cell (ECC) has been proposed [106]. The number of voltage levels of ECC exponentially increases with the number of switches. To deliver monotonically decreasing voltage levels with a fixed step size, the capacitor voltage of each submodule must be asymmetrical and equal to a portion of the dc-link supply voltage. This constraint limits its output voltage range to three times of the dc-link voltage. Consequently, it can hardly be scaled to a higher voltage.

In summary, compared to other topologies, the asymmetrical CHB is the most suitable one for this application due to its scalability and the demand for a high number of voltage levels. Specially, the binary asymmetrical CHB maintains a balance between voltage levels and redundant states for future voltage balancing research. Therefore, it is adopted as the basis of the bias converter topology.

5.3.2 Bias converter topology

Figure 5.6 depicts an enhanced topology of the multilevel bias converter. The multilevel waveform generator is comprised of a T-type submodule (M1) and a series of cascaded H-bridge submodules (M2 and M3). At the bottom, a T-type submodule M1 is used instead of another H-bridge submodule, because the dc supplies for the T-type submodule are grounded. This saves another isolated dc supply while maintaining the same number of output voltage states as compared to the H-bridge.

As shown in Figure 5.6, M1 is supplied by two dc voltages: V_{dsn} and $4V_{\text{step}}$. M2 and M3 are two binary cascaded H-bridge submodules, with a dc-link voltage equal to $2V_{\text{step}}$ and V_{step}, respectively. Each submodule has three output voltage states. The output voltage for M1 can be V_{dsn}, 0, and $-4V_{\text{step}}$, while the output voltage for

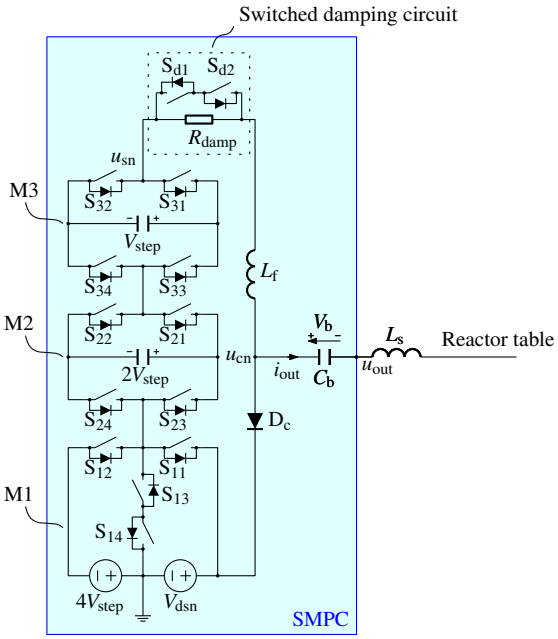


Figure 5.6 An improved topology of the multilevel bias converter.

M2 can be $2V_{step}$, 0, and $-2V_{step}$, and the output voltage for M3 can be V_{step}, 0, and $-V_{step}$. Thus, a combination of different states of each submodule yields 18 different voltage levels.

Each submodule can be represented by a state vector, denoted by 1, 0, and -1, depending on whether it delivers positive, zero, or negative voltage, respectively. For instance, $[1, -1, 0]$ indicates that M1, M2, and M3 deliver positive, negative, and zero voltage, respectively. Table 5.2 has listed all voltage levels and their corresponding submodule state vectors. It should be noted that an implicit assumption has been made, which is that $V_{dsn} - 3V_{step} > 3V_{step}$, implying that $V_{dsn} > 6V_{step}$. As can be seen, redundant states are available, allowing the use of dc-link capacitors with voltage balancing. However, this topic is beyond the scope of this thesis.

As seen from the table, there are 11 voltage levels ranging from $3V_{step}$ to $-7V_{step}$, which decrease monotonically with a fixed step size of V_{step}. Therefore, they can be used to construct the voltage slope in tailored waveform. As discussed earlier, the below-zero part of the falling edge of the voltage pulse in tailored waveform determines the ion energy. As a result, having a flexible V_{dsn}, rather than an integer multiple of V_{step}, is beneficial for more accurate ion energy.

Between the multilevel waveform generator and the filter inductor L_f, there exists

Table 5.2 The available voltage levels and corresponding submodule state vectors.

Voltage level	Submodule state vector
$V_{\text{dsn}} + 3V_{\text{step}}$	$[1, 1, 1]$
$V_{\text{dsn}} + 2V_{\text{step}}$	$[1, 1, 0]$
$V_{\text{dsn}} + V_{\text{step}}$	$[1, 1, -1]$, $[1, 0, 1]$
V_{dsn}	$[1, 0, 0]$
$V_{\text{dsn}} - V_{\text{step}}$	$[1, 0, -1]$, $[1, -1, 1]$
$V_{\text{dsn}} - 2V_{\text{step}}$	$[1, -1, 0]$
$V_{\text{dsn}} - 3V_{\text{step}}$	$[1, -1, -1]$
$3V_{\text{step}}$	$[0, 1, 1]$
$2V_{\text{step}}$	$[0, 1, 0]$
V_{step}	$[0, 1, -1]$, $[0, 0, 1]$
0	$[0, 0, 0]$
$-V_{\text{step}}$	$[0, 0, -1]$, $[0, -1, 1]$, $[-1, 1, 1]$
$-2V_{\text{step}}$	$[0, -1, 0]$, $[-1, 1, 0]$
$-3V_{\text{step}}$	$[0, -1, -1]$, $[-1, 1, -1]$, $[-1, 0, 1]$
$-4V_{\text{step}}$	$[-1, 0, 0]$
$-5V_{\text{step}}$	$[-1, 0, -1]$, $[-1, -1, 1]$
$-6V_{\text{step}}$	$[-1, -1, 0]$
$-7V_{\text{step}}$	$[-1, -1, -1]$

a switched damping circuit, comprising of a damping resistor R_{damp} and a four-quadrant switch made up of S_{d1} and S_{d2}. The damping circuit is employed to mitigate the potential LC resonance during the charge phase, and can be bypassed by turning on S_{d1} and S_{d2} during other phases.

A clamping diode D_{c} is placed between the common node of L_{f}, C_{b} and V_{dsn} to limit the maximum value of u_{cn} to V_{dsn} and advantageously prevents overvoltage during the discharge phase. This is elaborated on in the following chapter. The voltage levels of u_{sn} above V_{dsn} can be skipped, rendering $V_{\text{dsn}} + 3V_{\text{step}}$, $V_{\text{dsn}} + 2V_{\text{step}}$, and $V_{\text{dsn}} + V_{\text{step}}$ ineffective. Moreover, $V_{\text{dsn}} - V_{\text{step}}$, $V_{\text{dsn}} - 2V_{\text{step}}$, and $V_{\text{dsn}} - 3V_{\text{step}}$ are between V_{dsn} and the voltage levels used for the charge phase, and can be used as intermediate voltage levels to actively dampen the resonance during the voltage rising and falling edge. This is also further elaborated on in the following chapter.

It should be clarified that Figure 5.6 only depicts a specific implementation of the topology with three submodules, and it can be scaled by stacking up more H-bridge submodules. Assuming there are m submodules, the T-type submodule (M1) should be supplied with V_{dsn} and $2^{m-1}V_{\text{step}}$, while the other H-bridge submodules

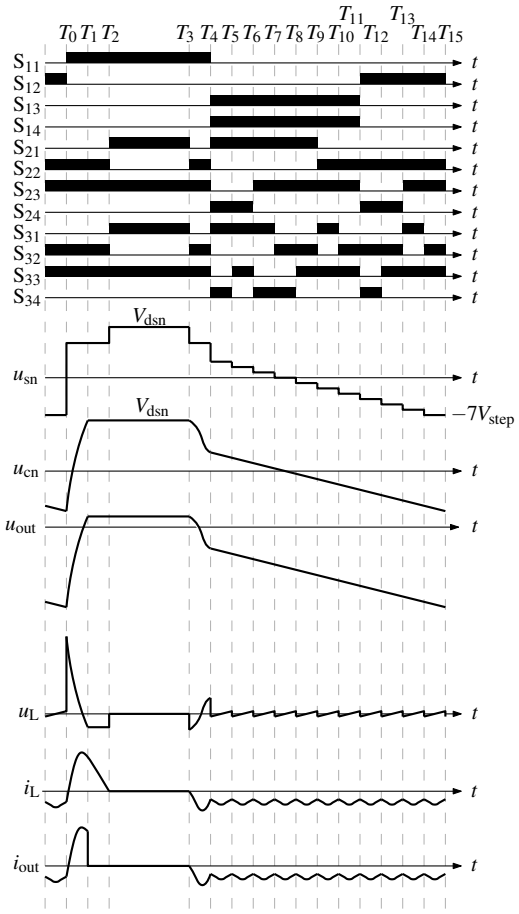


Figure 5.7 An implementation example of the operating principle.

(M2, M3,..., Mm) should be supplied by $2^{m-2}V_{\text{step}}$, $2^{m-3}V_{\text{step}}$,..., V_{step}, respectively. Moreover, the voltage levels used for the charge phase are from $\left(2^{m-1}-1\right)V_{\text{step}}$ to $-\left(2^{m}-1\right)V_{\text{step}}$, totaling $2^{m}+2^{m-1}-1$ voltage levels.

5.3.3 Operating principle

To further explain the bias converter, Figure 5.7 shows an example of its operating principle. To balance the switching loss in each submodule, over one fundamental period, the power switches in each submodule can be switched once, twice, and four times, respectively. In the example shown in Figure 5.7, all the switches of M1 are switched on and off once in a fundamental period, M2 twice, and M3 four times,

except S_{34}, since some voltage levels are skipped as analyzed above. The operation during each time interval is explained below.

• $T_0 \sim T_1$: At time T_0, the charge phase is completed, and the capacitor should be discharged. A positive voltage is applied at the switched-node. In Figure 5.7, this positive voltage is $V_{\text{dsn}} - 3V_{\text{step}}$, but it can be other values such as $V_{\text{dsn}} - 2V_{\text{step}}$, $V_{\text{dsn}} - V_{\text{step}}$, and $-V_{\text{step}}$, which won't increase the switching frequency of each submodule. The LC circuit starts resonating, and the common-node voltage u_{cn} is rising until it is clamped at V_{dsn} at T_1 by the clamping diode.

• $T_1 \sim T_2$: During this interval, u_{cn} is clamped at u_{cn}, and u_{sn} holds a lower voltage. As a result, a negative voltage is applied to the filter inductor, allowing the inductor current to fall to zero, reducing the power loss. By the end of this interval, the sheath capacitors and the substrate capacitor have been fully discharged, and the output current is approximately zero.

• $T_2 \sim T_3$: This interval allows for adjusting the duration of the post-discharge phase, providing another degree of freedom for regulation. During this time, u_{sn} is maintained at V_{dsn}. The time duration of $T_3 - T_2$ can be adjusted to control the blocking voltage.

• $T_3 \sim T_4$: After completing the post-discharge phase, the charge phase must be restarted. A lower voltage level should be applied at this stage. In Figure 5.7, this voltage is $V_{\text{dsn}} - 3V_{\text{step}}$, but is can also be $V_{\text{dsn}} - 2V_{\text{step}}$ and $V_{\text{dsn}} - V_{\text{step}}$, depending on the desired V_{s}. This change won't increase the switching frequency of each submodule. The LC circuit starts resonating again, and the common-node voltage u_{cn} falls to the correct value, making $u_{\text{out}} = V_{\text{s}}$ at T_4. Meanwhile, the inductor current should be equal to $-I_{\text{c}}$. Afterward, the plasma processing enters the charge phase.

• $T_5 \sim T_{15}$: The voltage at u_{sn} should be sequentially decreased with the same duration of T_{step}. After being filtered by the inductor L_{f}, u_{cn} and u_{out} are linearly decreasing, as shown in Figure 5.7.

To obtain a smooth waveform with the required voltage slope and prevent undesired resonance, each time interval should be accurately regulated. In this thesis, a trajectory control method has been developed to calculate each time interval, which is illustrated in the following chapter.

5.4 Conclusion

In this chapter, two existing bias converter concepts are introduced: the voltage source converter and the hybrid source converter. The former can be a linear ampli-

fier or an SMPC. The linear amplifier has a low energy efficiency, and the SMPC has a shortcoming of limited frequency. In contrast, the hybrid source converter uses a dc current source to generate the voltage slope, which significantly reduces bandwidth requirements and is thus more popular in industries. However, it can hardly be scaled to higher voltages or repetition frequencies due to inherent limitations in the switching devices.

Based on the analysis, a multilevel bias converter concept is derived, which enjoys a better scalability. It approximates the linear voltage slope by monotonically decreasing voltage levels. While such an approximation could cause voltage ripple on the substrate surface and broaden the IED, an extra filter inductor can reduce the voltage ripple. For a given requirement on the voltage ripple, the minimum filter inductance has been derived in this chapter. Consequently, a basic configuration for the multilevel bias converter is derived, which includes a multilevel waveform generator, a filter inductor, and a blocking capacitor.

Various multilevel topologies are evaluated, and it is concluded that the asymmetrical CHB is the most suitable one as a basis for the multilevel waveform generator. An enhanced topology is introduced, which is formed by a T-type converter and a series of cascaded H-bridges. Besides, a switched damping circuit and a clamping diode is added for better damping and protection in practice. The basic operating principle of this bias converter has been demonstrated and is further explained in the following chapter.

CHAPTER 6

Trajectory control

THE previous chapter introduces a multilevel bias converter to generate the tailored waveform. During the charge phase, the multilevel waveform generator delivers monotonically decreasing voltage levels at the switched-node. These voltage levels are smoothened and become the required voltage slope at the output during the charge phase after being filtered by the low-pass filter formed by the inductances and the load capacitances. The voltage slope is one of the two essential parts of the tailored waveform, and its steady state has been explained in the previous chapter. However, the generation of the positive voltage pulse that realizes the discharge and post-discharge phase requires further exploration.

The inductances, including the stray inductance in the loop and the extra filter inductance, together with the load capacitances, form an LC circuit. If a voltage step with a sufficiently fast rising or falling edge is applied to the LC circuit at the switched-node, a resonance is triggered, creating an oscillation on the inductance and capacitance. The amplitude of this oscillation depends on the magnitude of the voltage pulse, and its frequency is equal to the natural frequency of the LC circuit.

In tailored waveform biasing, such a voltage step exists in the discharge phase (rising edge) and after the post-discharge (falling edge), which can trigger two resonances in one fundamental period. If actions are not taken to dampen these resonances, voltage oscillations could be seen over the table and sheath, which could significantly broaden the IED.

This chapter is based on [189].

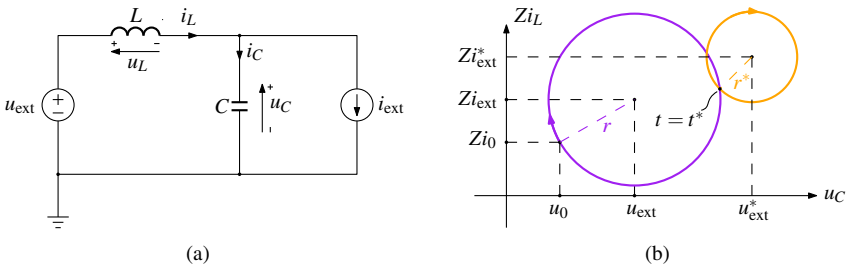


Figure 6.1 (a) A basic LC circuit. Here u_C and i_C are the voltage and current of capacitor C. (b) State-plane diagram of the LC circuit.

Different damping methods can be adopted to diminish the resonance, and the most straight-forward one is resistive damping. By adding a damping resistor in the loop, the resonance can be passively damped out, at the cost of extra power dissipation on the resistor and a lower efficiency. Since efficiency is always the pursuit of power electronics, this chapter introduces a trajectory control method, which uses extra intermediate voltage levels to mitigate the resonance while tremendously reducing the power dissipation compared to resistive damping.

6.1 Fundamentals of trajectory control

The trajectory control is often studied through state-plane analysis. To comprehend this technique, a basic LC circuit can be considered, as shown in Figure 6.1(a) [47]. The LC circuit is supplied with a dc voltage source u_{ext} and a dc current source i_{ext}. The inductor current i_L and the capacitor voltage u_C are governed by

$$L\frac{\mathrm{d}i_L}{\mathrm{d}t} = -u_C + u_{ext} \tag{6.1}$$

and

$$C\frac{\mathrm{d}u_C}{\mathrm{d}t} = i_L - i_{ext}. \tag{6.2}$$

Solving these equations for u_C and i_L leads to

$$u_C = u_{ext} + (u_0 - u_{ext})\cos(\omega t) + Z(i_0 - i_{ext})\sin(\omega t) \tag{6.3}$$

and

$$i_L = i_{ext} - \frac{1}{Z}(u_0 - u_{ext})\sin(\omega t) + (i_0 - i_{ext})\cos(\omega t), \tag{6.4}$$

where u_0 is the initial voltage of the capacitor, i_0 is the initial current of the inductor, Z is the impedance of the LC circuit defined by

$$Z = \sqrt{\frac{L}{C}}, \tag{6.5}$$

and ω is the natural frequency calculated as

$$\omega = \frac{1}{\sqrt{LC}}. \tag{6.6}$$

Both u_C and i_L are sinusoidal functions of time with an angular frequency of ω. Manipulating (6.3) and (6.4) yields

$$(u_C - u_{\text{ext}})^2 + (Zi_L - Zi_{\text{ext}})^2 = (u_0 - u_{\text{ext}})^2 + (Zi_0 - Zi_{\text{ext}})^2. \tag{6.7}$$

Therefore, by selecting u_C and Zi_L as the two state variables, the trajectory of their values over time in the state-plane forms a circle centered at $(u_{\text{ext}}, Zi_{\text{ext}})$ and passing through the initial state (u_0, Zi_0), as depicted in Figure 6.1(b). Based on (6.1) and (6.2), it can be concluded that the direction of the trajectory is always clockwise. The radius r of the circle is determined by

$$r = \sqrt{(u_0 - u_{\text{ext}})^2 + (Zi_0 - Zi_{\text{ext}})^2}, \tag{6.8}$$

which indicates the oscillation amplitude of both u_C and Zi_L. Although time is not visible in this state-plane diagram, it is proportional to the arc (or the angle) of the circle traversed.

Furthermore, if at time $t = t^*$, the dc voltage and current source turn into u^*_{ext} and i^*_{ext}, respectively, it is apparent that the new trajectory will be a circle with a center of $(u^*_{\text{ext}}, Zi^*_{\text{ext}})$ and passing through the its initial state $(u_C(T), Zi_L(T))$, as shown in Figure 6.1(b). Obviously, by changing the voltage or current source at the appropriate time, variant trajectories in the state-plane can be obtained, which will construct the desired waveforms in the time domain.

The trajectory control is popular in power electronics, especially in resonant converters [16, 25, 83, 128, 129]. In the following sections, the trajectory control is applied to the bias converter to generate the tailored waveform.

6.2 Trajectory control of the bias converter

6.2.1 Preparation

To implement the trajectory control on the proposed bias converter, certain simplifications need to be made since the system is not a straight-forward LC circuit. In this chapter, C_{sh2} and I_{i2} are assumed to be zero for simplicity. The switched damping circuit is assumed to be shorted. As a result, the equivalent circuit of the system can be simplified as shown in Figure 6.2(a). The switched-node voltage u_{sn} is the voltage generated by the multilevel waveform generator, as depicted in Figure 5.6. The

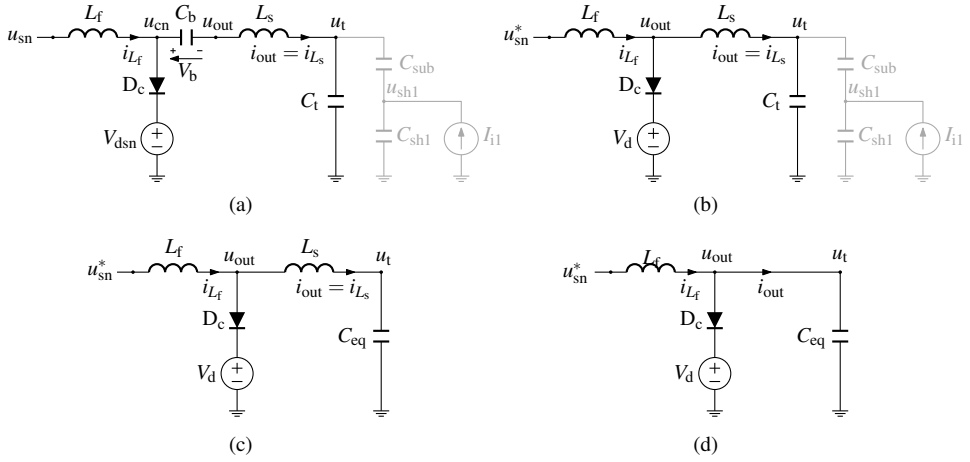


Figure 6.2 (a) The equivalent circuit of the bias converter and its load. (b) Simplifying the equivalent circuit by removing the blocking capacitor C_b. (c) Simplifying the equivalent circuit by approximating the load by an equivalent capacitor C_{eq}. (d) Simplifying the equivalent circuit by neglecting L_s.

maximum value of the common-node voltage u_{cn} is clamped to V_{dsn}. Depending on the load status during each phase, as introduced in Figure 2.5, C_{sub}, C_{sh1}, and I_{i1} can be connected or disconnected from the bias converter (represented by the gray components in Figure 2.5), while C_t is always connected.

As described in Section 2.1, a self-biased voltage V_b is formed across the blocking capacitor C_b. If the blocking capacitance is sufficiently large, V_b can be regarded as constant. In this case, subtracting V_b from u_{sn} directly and removing C_b will not affect the voltage and current of other components. Denoting $u^*_{sn} = u_{sn} - V_b$, the simplified equivalent circuit can be described by Figure 6.2(b). Applying any voltage level to u_{sn}, as enumerated in Table 5.2, is equivalent to applying $u_{sn} - V_b$ to u^*_{sn}. It should be noted that the maximum output voltage u_{out} is then clamped to $V_d = V_{dsn} - V_b$.

I_{i1} is disconnected from the converter during the post-discharge phase. Besides, its effect on the capacitor voltages is trivial during the voltage rising and falling edge since these times are relatively short. Therefore, I_{i1} can be neglected when analyzing the transient behavior of the circuit. C_{sh1} and C_{sub} are disconnected from the converter one after another during the discharge phase, as explained in Figure 2.5(b) and (c), leading to different load capacitances at different moments. For simplification, a constant equivalent capacitance C_{eq} defined by (4.3) is used to represent the load capacitance throughout the fundamental period. This simplification can lead to

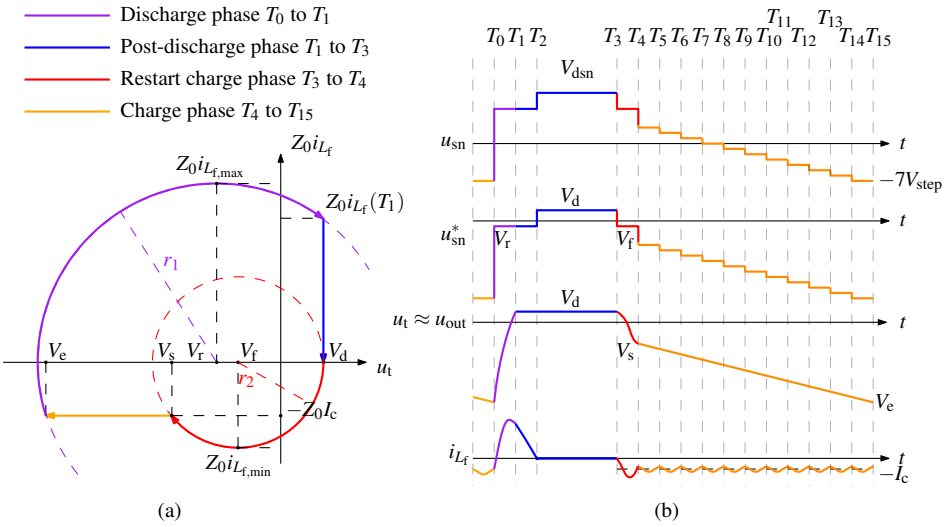


Figure 6.3 (a) The state-plane analysis of the whole repetition period. (b) The waveforms of u_{sn}, u^*_{sn}, u_t, and i_{L_f} in time domain.

inaccuracy, especially during the discharge phase, which will be discussed in the following sections. After that, the equivalent circuit can be further simplified as shown in Figure 6.2(c).

Finally, because the filter inductance L_f is usually much larger than the stray inductance L_s (in order to minimize the output voltage ripple), L_s can be safely neglected and u_{out} can be considered approximately equal to u_t. The simplified equivalent circuit of the system is shown in Figure 6.2(d), which is similar to the LC circuit introduced in the previous section and prepared for trajectory control. The impedance and the natural frequency of this circuit are given by

$$Z_0 = \sqrt{\frac{L_f}{C_{eq}}} = \sqrt{\frac{L_f\,(C_{sh1} + C_{sub})}{C_{sh1}C_{sub} + C_{sh1}C_t + C_{sub}C_t}} \tag{6.9}$$

and

$$\omega_0 = \frac{1}{\sqrt{L_f C_{eq}}} = \sqrt{\frac{C_{sh1} + C_{sub}}{L_f\,(C_{sh1}C_{sub} + C_{sh1}C_t + C_{sub}C_t)}}, \tag{6.10}$$

respectively. As previously demonstrated, u_t and $Z_0 i_{L_s}$ can be used as two state variables for state-plane analysis.

6.2.2 General principles

The desired trajectory in the state-plane diagram for one fundamental period is depicted in Figure 6.3(a), and its corresponding waveforms in the time domain are displayed in Figure 6.3(b).

The objective of the trajectory control is to acquire precise values for V_s and the slope rate of u_t. The slope rate is determined by $V_{step}T_{step}^{-1}$, which is realized by the monotonically decreasing voltage levels from $3V_{step}$ to $-7V_{step}$. To ensure a smooth transition to V_s, two intermediate voltages, V_r and V_f, are employed during the voltage rising and falling edge, respectively. These intermediate voltages at the switched-node are denoted as $V_{rsn} = V_r + V_b$ and $V_{fsn} = V_f + V_b$. As explained in Chapter 5, during the voltage rising and falling edge, three different voltage levels: $V_{dsn} - V_{step}$, $V_{dsn} - 2V_{step}$, and $V_{dsn} - 3V_{step}$, can be used for both V_{rsn} and V_{fsn} without increasing the switching frequency. Therefore, the possible values of V_r and V_f include $V_{dsn} - V_{step} - V_b$, $V_{dsn} - 2V_{step} - V_b$, and $V_{dsn} - 3V_{step} - V_b$.

The desired trajectory and waveform are accomplished by carefully selecting the appropriate values of V_r, V_f, V_d, and their respective durations for u_{sn}^*, which is essentially achieved by controlling u_{sn}. It should be noted that u_{sn}^* is a virtual voltage, obtained by shifting u_{sn} by the blocking voltage V_b, and does not exist physically. The specific voltage levels and their durations are explicitly determined in the subsequent sections.

6.2.3 Discharge phase

At the end of the charge phase, a voltage level of $-7V_{step}$ is applied to u_{sn}, which represents the lowest voltage level. Denoting the voltage at this moment as $u_t = V_e$, it can be derived that

$$V_e = u_{sn} - V_b \approx -7V_{step} - V_b. \tag{6.11}$$

Moreover, the inductor current should be

$$i_{L_f} = -I_{i1}\left(1 + \frac{C_t}{C_{sub}}\right) \tag{6.12}$$

to precisely compensate for the ion charge effect on the substrate. Denoting this current by $-I_c$, the state at the end of the charge phase (also the initial state of the discharge phase) becomes $(V_e, -Z_0 I_c)$. After the discharge phase, u_t should be $u_t = V_d = V_{dsn} - V_b$, which implies the target for trajectory control during the transition to this phase. Therefore, an intermediate voltage level V_r, which is between V_d and V_e, can be applied to u_{sn}^* until u_t rises to V_d. During this time, the clamping diode D_c is blocking.

The radius of the trajectory is calculated by

$$r_1 = \sqrt{(V_\mathrm{r} - V_\mathrm{e})^2 + Z_0^2 I_\mathrm{c}^2}. \tag{6.13}$$

During this trajectory, the voltage u_t is generally rising, as illustrated by Figure 6.3(a). The time duration of this trajectory corresponds to the time interval of T_0 to T_1 depicted in Figure 6.3(b) and is proportional to the angle of the arc. The duration is given by

$$T_\mathrm{r} = T_1 - T_0 = \frac{\arcsin\left(\frac{Z_0 I_\mathrm{c}}{r_1}\right) + \pi - \arccos\left(\frac{V_\mathrm{d} - V_\mathrm{r}}{r_1}\right)}{\omega_0}. \tag{6.14}$$

At the end of this trajectory ($t = T_1$), the inductor current can be calculated from the state-plane diagram as

$$i_{L_\mathrm{f}}(T_1) = \frac{\sqrt{r_1^2 - (V_\mathrm{d} - V_\mathrm{r})^2}}{Z_0}. \tag{6.15}$$

The maximum inductor current can also be derived as

$$i_{L_\mathrm{f,max}} = \frac{r_1}{Z_0}. \tag{6.16}$$

There are certain requirements for the value of V_r. It must be sufficiently large to allow the capacitor voltage to resonate to V_d. This requirement can be expressed in terms of a geometric language in the state-plane diagram. The circle in the diagram must intersect with line $u_\mathrm{t} = V_\mathrm{d}$ at least once, as described by

$$V_\mathrm{r} + r_1 = V_\mathrm{r} + \sqrt{(V_\mathrm{r} - V_\mathrm{e})^2 + Z_0^2 I_\mathrm{c}^2} \geq V_\mathrm{d}. \tag{6.17}$$

Additionally, V_r must be smaller than V_d to allow the inductor current to decrease during the post-discharge time. Based on experimental experience, it is usually true that $Z_0 I_\mathrm{c} \ll V_\mathrm{r} - V_\mathrm{e}$. Consequently, the requirement for V_r can be simplified to $V_\mathrm{d} > V_\mathrm{r} > \frac{1}{2}(V_\mathrm{d} + V_\mathrm{e})$. For this bias converter, depending on the specific values of V_dsn and V_step, V_r can take on multiple values.

Specially, because

$$\frac{1}{2}(V_\mathrm{dsn} - 7V_\mathrm{step}) < V_\mathrm{dsn} - 3V_\mathrm{step} < V_\mathrm{dsn} \tag{6.18}$$

always holds for u_sn, the voltage level

$$V_\mathrm{r} = V_\mathrm{d} - 3V_\mathrm{step} = V_\mathrm{dsn} - V_\mathrm{b} - 3V_\mathrm{step} \tag{6.19}$$

is always suitable to use for this trajectory (so are $V_\mathrm{r} = V_\mathrm{dsn} - 2V_\mathrm{step} - V_\mathrm{b}$ and $V_\mathrm{r} = V_\mathrm{dsn} - V_\mathrm{step} - V_\mathrm{b}$). Moreover, it is preferable to use a smaller value for V_r, since a larger value will result in a larger radius and therefore higher current and loss. Besides, a smaller V_r also makes the inductor current drop to zero faster in the following post-discharge phase.

6.2.4 Post-discharge phase

After u_t reaches V_d, the clamping diode D_c starts conducting, forcing u_{out} to be V_d. $u^*_{sn} = V_r$ can be held for an additional period, so that the inductor current can decrease to zero, as depicted by the time interval from T_1 to T_2 in Figure 6.3(b). The benefit of this action is to reduce the inductor current and loss, while maintaining the discharge voltage V_d during the post-discharge phase. The duration of this interval can be calculated as

$$T_{p1} = T_2 - T_1 = \frac{L_f i_{L_f}(T_1)}{V_d - V_r}. \tag{6.20}$$

After i_{L_f} drops to zero, the circuit state becomes $(V_e, 0)$. During the time interval from T_2 to T_3, denoted by T_{p2}, as shown in Figure 5.7, u_{sn} should be switched to V_{dsn} ($u^*_{sn} = V_d$). As discussed in previous chapters and verified by experiments in Section 2.2, the pulse duty cycle is an additional degree of freedom to regulate V_d and V_b. Therefore, the time duration of interval T_{p2} is a control variable. The time duration of this trajectory during the post-discharge phase is $T_p = T_{p1} + T_{p2}$. In the state-plane diagram, this phase is a vertical line, as illustrated in Figure 6.3(a).

6.2.5 Restart charge phase

After the post-discharge phase is completed, the circuit should be restarted into the charge phase. As specified in Section 2.1, u_t should be recharged to the correct start voltage V_s, which determines the ion energy according to (2.20). Meanwhile, the inductor current should reach the correct value $-I_c$ to compensate for the ion charge effect. In other words, at the start of the charge phase, the state of the LC circuit should be $(V_s, -Z_0 I_c)$.

Similar to the discharge phase, an intermediate voltage level V_f between V_d and V_s can be used during voltage falling. At this time, the clamping diode D_c is again blocking.

The radius of the trajectory is calculated by

$$r_2 = V_d - V_f. \tag{6.21}$$

In this trajectory, the voltage u_t is falling. This voltage falling trajectory is illustrated by Figure 6.3(a), the time duration of which is corresponding to the time interval from T_3 to T_4 depicted in Figure 5.7, given by

$$T_f = T_4 - T_3 = \frac{\pi - \arcsin\left(\frac{Z_0 I_c}{r_2}\right)}{\omega_0}. \tag{6.22}$$

The minimum inductor current during this time can be easily obtained as

$$i_{L_{\mathrm{f,min}}} = -\frac{r_2}{Z_0}. \tag{6.23}$$

As previously demonstrated, for this bias converter, three different intermediate voltage levels can be used for V_f, represented by $V_\mathrm{f} = V_\mathrm{dsn} - kV_\mathrm{step} - V_\mathrm{b} (k = 1,\ 2, \mathrm{or}\ 3)$, which are always between $V_\mathrm{dsn} - V_\mathrm{b}$ and $3V_\mathrm{step} - V_\mathrm{b}$. For a fixed k, the radius of the trajectory is equal to $r_2 = kV_\mathrm{step}$. V_s can then be represented by

$$V_\mathrm{s} = V_\mathrm{d} - kV_\mathrm{step} - \sqrt{(r_1^2 - Z_0^2 I_\mathrm{c}^2)}. \tag{6.24}$$

It means that for a required state $(V_\mathrm{s}, -Z_0 I_\mathrm{c})$, two control variables, V_d and k, should be regulated together to reach the target. V_d should be positive, leading to $V_\mathrm{d} = V_\mathrm{s} + kV_\mathrm{step} + \sqrt{(r_1^2 - Z_0^2 I_\mathrm{c}^2)} > 0$. Consequently, for a specific k, the feasible V_s has a minimum value of approximately $-kV_\mathrm{step} - \sqrt{(r_1^2 - Z_0^2 I_\mathrm{c}^2)}$.

Furthermore, if the required V_s is lower than $-3V_\mathrm{step} - \sqrt{(r_1^2 - Z_0^2 I_\mathrm{c}^2)}$, then none of the k values could achieve the goal. Under this circumstance, voltage levels lower than $V_\mathrm{dsn} - 3V_\mathrm{step} - V_\mathrm{b}$, such as $3V_\mathrm{step} - V_\mathrm{b}$, should be applied to u_sn^*. As a result, the resonance cannot be fully regulated by trajectory control, and extra passive damping is required. Besides, it also reduces the available number of voltage levels for the charge phase. The mathematical derivation of this scenario is out of the scope of this thesis and skipped for brevity.

6.2.6 Charge phase

After obtaining the correct state $(V_\mathrm{s}, -Z_0 I_\mathrm{c})$, the charge phase restarts. The voltage levels applied to u_sn monotonically decrease from $3V_\mathrm{step}$ to $-7V_\mathrm{step}$. Neglecting the voltage ripple of u_t, u_t linearly decreases, while i_{L_f} remains constant. In the state-plane diagram, this phase is a vertical line, as represented by Figure 6.3(a).

Suppose $V_\mathrm{f} = V_\mathrm{d} - kV_\mathrm{step}$, then the first voltage level during the charge phase should be $u_\mathrm{sn}^* = 3V_\mathrm{step} - V_\mathrm{b}$. By definition, the time duration of the charge phase is $11T_\mathrm{step}$. The end voltage V_e can be calculated by

$$V_\mathrm{e} = V_\mathrm{s} - 11V_\mathrm{step}. \tag{6.25}$$

If V_f is lower than $V_\mathrm{d} - 3V_\mathrm{step}$, the available number of voltage levels for the charge phase is less than eleven. Under such circumstances, the operation becomes more complex, which is beyond the scope of this discussion.

Table 6.1 The parameters of the plasma processing model

Parameter	Value	Unit	Parameter	Value	Unit
I_{i1}	100	mA	V_p	25	V
I_{i2}	0	mA	L_s	25	nH
C_t	2.3	nF	R_s	1.5	Ω
C_{sub}	2	nF	R_p	17	Ω
C_{sh1}	0.1	nF	R_{pd}	6000	Ω
C_{sh2}	0	nF	σ^2	5	$(eV)^2$

Table 6.2 The configuration of the bias converter

Parameter	Value	Unit	Parameter	Value	Unit
L_f	5.22	μH	C_b	1	μF
R_{damp}	20	Ω	V_{dsn}	190	V
V_{step}	20	V	T_{step}	400	ns

Table 6.3 The control variables for the trajectory control

Parameter	Value	Unit	Parameter	Value	Unit
V_d	41	V	V_b	149	V
V_r	-19	V	V_f	-19	V
T_r	200	ns	T_f	350	ns
T_{p1}	600	ns	T_{p2}	40	ns

6.3 Simulation

A simulation was conducted in MATLAB/Simulink with the SimScape toolbox to verify the trajectory control method. The simulation circuit for plasma processing was the same with the one depicted in Figure 2.8, and the related parameters are listed in Table 6.1. The proposed bias converter shown in Figure 5.6 was used in the simulation. The power semiconductors were regarded as ideal for simplicity, so the switching speed was infinitely fast, and dead-time was not required. The configurations of the bias converter are shown in Table 6.2.

Moreover, the voltage and time resolution of the bias converter were assumed to be 1 V and 10 ns, which are also reasonable values achievable in reality. Therefore, any calculated voltage and time values were rounded to 1 V and 10 ns. After re-starting the charge phase, the switched damping circuit was enabled to dampen the

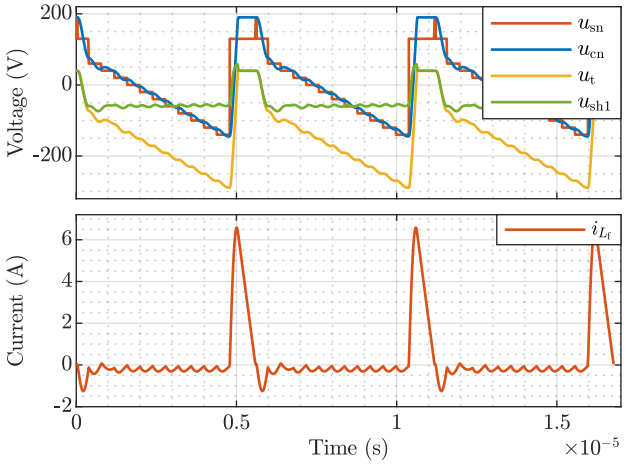


Figure 6.4 The simulated waveforms of u_{sn}, u_{cn}, u_t, u_{sh1}, and i_{L_f}.

undesired resonance caused by the rounding errors and the mismatch between the real capacitance and estimated C_{eq}.

The operating principle of the bias converter is described in Figure 5.7. As analyzed in (5.4), the slope rate during the charge phase is determined by

$$-\frac{V_{step}}{T_{step}} = -\frac{I_{i1}}{C_{sub}} = -5 \cdot 10^7 \,\mathrm{V\,s^{-1}}. \tag{6.26}$$

Selecting either value of V_{step} or T_{step} determines the other one simultaneously. In this simulation, T_{step} is set to 400 ns, and V_{step} is 20 V. Assuming that the desired ion energy is 100 eV, according to (2.9) and (2.20), V_s should be approximately -75 V. Based on the aforementioned analysis in the previous sections, the control variables for the trajectory control can be calculated and rounded to their resolutions, as listed in Table 6.3. It must be clarified that T_{p1} in Table 6.3 is 90 ns longer than the calculated value to compensate for the modeling errors, such that i_{L_f} falls to approximately zero at T_2. This effect is further illustrated in the following paragraphs.

The waveforms obtained from the simulation are plotted in Figure 6.4. It can be observed that the waveforms of u_{cn} and u_t are smoothed out after filtering u_{sn}. During the charge phase, the voltage u_{sh1} remains generally constant with only minor voltage ripples. By utilizing the IED simulation method introduced in Section 2.2, the resulting IED can be obtained as shown in Figure 6.5. The FWHM of the simulated IED is smaller than 6 eV, confirming the feasibility of the multilevel bias converter concept.

The desired ion energy is 100 eV, while the peak of the obtained IED is located at

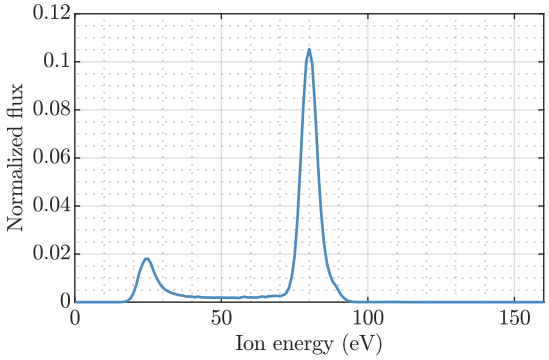


Figure 6.5 The simulated IED.

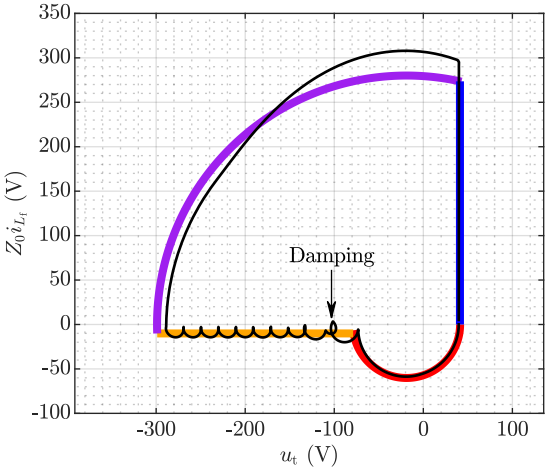


Figure 6.6 The comparison between the theoretical and simulated trajectory. Thick and colorful curve represents the theoretical trajectory, and the thin and black curve represents the simulated one.

80 eV. This deviation originates from the neglect of I_{i1}. During the voltage falling edge, I_{i1} can charge C_{sub} and C_{sh1}, thereby raising the voltage potential of u_{sh1} and reducing the ion energy. This effect is positively correlated with the duration of the voltage falling edge T_f. Therefore, a large T_f should be avoided. On the other hand, V_d can be further decreased, for instance, by increasing V_b, to achieve a larger voltage drop to compensate for the effect of I_{i1}.

To further validate the trajectory control, Figure 6.6 demonstrates a comparison between the theoretical and simulated trajectory in the state-plane diagram. The

simulated trajectory match well with the theoretical one, except for the discharge phase where the radius of the trajectory varies, indicating changing impedance of the LC circuit. As explained in the previous section, C_{sh1} and C_{sub} are disconnected from the converter one after another during the discharge phase, leading to a changing impedance and distorted trajectory. This effect also increases the inductor current, as the simulated value of $i_{L_{\mathrm{f}}}(T_1)$ is higher than the calculated one. Therefore, T_{p1} should be increased so that $i_{L_{\mathrm{f}}}(T_1)$ can fall down to zero during the post-discharge phase.

Moreover, since restarting the charge phase is equivalent to the reverse process of the discharge phase, the mismatch between the real capacitance and the estimated C_{eq} also affects the trajectory during the voltage falling edge. This mismatch could cause undesired resonance during the charge phase. Therefore, the switched damping circuit is enabled during the charge phase to reach steady-state earlier. The effect of the switched damping can be seen at the unnatural turning point, as annotated by the arrow in Figure 6.6.

The simulation underlines the effectiveness of the trajectory control, but also reveals its drawback in terms of accuracy. In general, given a specific ion energy goal, the trajectory control method can deliver satisfactory waveforms close to the target with low computation effort. It can serve as an initial point, and with further tuning, the results can be further refined. In the future, closed-loop trajectory control can be implemented to avoid manual tuning and reject disturbances.

6.4 Conclusion

When driving the plasma reactor with the proposed tailored waveform, the LC circuit formed by the inductances and load capacitances can cause resonance when applied with a voltage pulse. In this chapter, a trajectory control method is developed to dampen this resonance using intermediate voltage levels during the voltage rising and falling edge. With the help of state-plane analysis, the time of applying each voltage level can be intuitively and accurately determined. A simulation was conducted to verify the method, and the results were found to be generally consistent with the analysis.

It must be noted that this trajectory control method is developed based on a simplified model. In reality, there are various factors that can affect its operation. For instance, the load capacitance can have different values during different phases, which is simplified by a constant C_{eq} in this chapter. Additionally, resistance is inevitably present in the loop, introducing passive damping to the LC circuit. Moreover, the ion current can charge the load capacitance during voltage rising and falling,

which is neglected in this study. Furthermore, time delays exist in all kinds of ICs and power semiconductors, and processors have finite time resolutions, which may cause inaccuracies in the desired time duration. Similarly, all voltage sources are limited by their voltage resolutions, which may disturb the trajectories and cause inaccuracies. All these factors can disturb the trajectories and cause inaccuracy.

As a result, in practice, manual fine tuning of voltages and times based on the calculation discussed in this chapter can help to improve the delivered waveforms. Furthermore, these nonideal factors may also cause additional resonance to the LC circuit, and therefore, the switched damping circuit can be enabled at a proper time to passively dampen these parasitic effects. In the future, closed-loop trajectory control can be developed to improve the accuracy of the method.

Chapter 7

Top-down design

In previous chapters, a bias converter and its trajectory control method to generate the tailored waveform have been proposed. The goal of this bias converter is to obtain a narrow IED, which poses two crucial requirements for the generated tailored waveform. First, the voltage ripple that is in superpositioned with the output voltage during the charge phase should be as low as possible to keep the ion energy constant. Second, the discharge pulse duty cycle, including the rising and falling edge, should be as small as possible so that the ion energy is well-defined for most of the time, and the fewest ions fall into the low energy range during the post-discharge phase.

Both requirements are related to the filter inductance. The lower voltage ripple calls for a large filter inductance, as demonstrated by (5.18), which, in turn, slows the transient and increases the time duration of the rising and falling edge.

Reducing T_{step} can help achieve both goals simultaneously. A smaller T_{step} corresponds to a higher frequency of the voltage ripple, thus a smaller filter inductance and faster transient. Nevertheless, this method is not a panacea. On the one hand, the lowest value of T_{step} is inherently limited by the capability of the power semiconductors. Since the turn-on and off delays always exist, T_{step} cannot be infinitely small. Meanwhile, a smaller T_{step} requires a higher switching frequency, and a smaller filter inductance could also lead to higher current during transients. Both of these factors could tremendously increase the switching loss of the power semiconductors. On the other hand, since $V_{\text{step}} T_{\text{step}}^{-1}$ is governed by the required slope rate, given a specification of operating conditions, a smaller T_{step} yields a smaller V_{step}, which

Table 7.1 The parameters for plasma processing

Parameter	Minimum	Typical	Maximum	Unit
I_{i1}	0.001	0.1	0.7	A
C_t	2	3	5	nF
C_{sub}	2	2	10	nF
C_{sh1}	0.1	0.3	0.5	nF
L_s	10	20	50	nH
E_i	25	100	250	eV
Δu_{sh1}	-	-	10	V
$\frac{du_t}{dt}$	$-1.2 \cdot 10^8$	$-0.5 \cdot 10^6$	0	$V\,s^{-1}$

helps reduce voltage stress over the power semiconductors but limits the output voltage and ion energy range. Therefore, selecting the appropriate value of T_{step} is crucial in designing the bias converter.

Anyhow, electrical engineering is the art of making trade-offs. There can hardly exist an optimal design for all goals simultaneously. The primary goal is to make a proper design that satisfies the requirements for a given specification. In this chapter, a top-down design method is developed to make appropriate design selections for a given specification.

7.1 Specification

In order to illustrate the top-down design method, a typical case is used as an example in this chapter. The parameters for plasma processing are provided in Table 7.1. These parameters vary in different plasma processing scenarios and range from their minimum to maximum values in the typical processes, as listed in Table 7.1.

According to (2.12), the slope rate $\frac{du_t}{dt}$ is determined by $-I_{i1}C_{sub}^{-1}$, which could lead to a minimum $\frac{du_t}{dt} = -3.5 \cdot 10^8\,V\,s^{-1}$ (given $I_{i1} = 0.7\,A$ and $C_{sub} = 2\,nF$). However, such a slope rate is not realistic, as larger I_{i1} corresponds to a larger C_{sub} in practice. Therefore, the most negative value of the desired $\frac{du_t}{dt}$ is set to $-1.2 \cdot 10^8\,V\,s^{-1}$, which is about 20 times the typical optimal value obtained in Section 2.2.

The bias converter is required to reach an ion energy E_i of up to 250 eV under various operating conditions. To achieve a narrow IED, the voltage ripple on the substrate surface Δu_{sh1} during the charge phase should not exceed 10 V. This constraint can ensure the FWHM of the IED is lower than 10 eV in most cases, as demonstrated in

Appendix C.

7.2 Converter dimensioning

After establishing the specifications and requirements, the essential parameters of the bias converter can be determined. Primarily, the combination of V_{step} and T_{step} must be capable of generating the most negative slope rate, which can be described by

$$\min\left(-\frac{V_{\text{step}}}{T_{\text{step}}}\right) = \min\left(\frac{\mathrm{d}u_{\text{t}}}{\mathrm{d}t}\right) = \min\left(-\frac{I_{\text{i1}}}{C_{\text{sub}}}\right) < 0. \tag{7.1}$$

For a specific operating point (for example, a smaller I_{i1} or a larger C_{sub}), the desired slope rate may be less negative than the value used for dimensioning. In such cases, theoretically, adjusting the slope rate is possible by either reducing V_{step} or increasing T_{step}. However, increasing T_{step} may reduce the frequency of the voltage ripple, rendering the LC filter ineffective. Therefore, reducing V_{step} while keeping T_{step} constant is usually the better approach, unless V_{step} is small enough, *e.g.*, smaller than Δu_{sh1}, in which case the LC filter is not required anymore. Consequently, given a specific T_{step}, the bias converter should be capable of delivering V_{step} up to the value governed by

$$V_{\text{step}} = \max\left(\frac{\mathrm{d}u_{\text{t}}}{\mathrm{d}t}\right) T_{\text{step}}, \tag{7.2}$$

which can be regarded as a function of T_{step}. As illustrated by (5.18), given a required Δu_{sh1} and a specific T_{step}, the minimum filter inductance can be obtained as

$$L_{\text{f}} \geq \frac{\sqrt{3}}{108} \cdot \frac{1}{\Delta u_{\text{sh1}}} \cdot \max\left(\frac{C_{\text{sub}} V_{\text{step}}}{C_{\text{sh1}} C_{\text{sub}} + C_{\text{t}} C_{\text{sh}} + C_{\text{t}} C_{\text{sub}}}\right) T_{\text{step}}^2 - \min\left(L_{\text{s}}\right). \tag{7.3}$$

Its boundary should be determined at the maximum value of C_{sub} and V_{step} (given by (7.2)) and the minimum value of C_{sh1} and C_{t}. With T_{step} fixed, any filter inductance satisfying (7.3) can guarantee a satisfactory Δu_{sh1} under any operating point within the required range.

Moreover, a larger L_{f} leads to a smaller Δu_{sh1}, resulting in a narrower IED and reduced inductor current, but causing a slower voltage rising and falling edge. Therefore, a trade-off must be made while selecting L_{f}.

Combining (6.14) and (6.22) gives the total transition time for the voltage rising and falling edge, as given by

$$T_{\text{tr}} = T_{\text{r}} + T_{\text{f}} = \frac{2\pi + \arcsin\left(\frac{Z_0 I_{\text{c}}}{r_1}\right) - \arccos\left(\frac{V_{\text{d}} - V_{\text{r}}}{r_1}\right) - \arcsin\left(\frac{Z_0 I_{\text{c}}}{r_2}\right)}{\omega_0}. \tag{7.4}$$

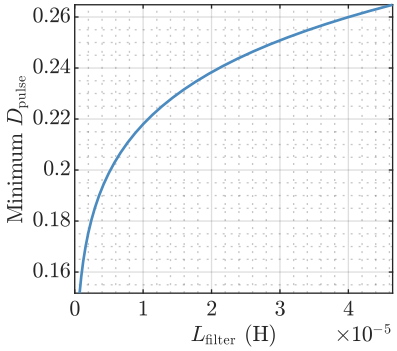


Figure 7.1 The relationship between the guaranteed D_{pulse} and the filter inductance L_{f}.

In practice, $Z_0 I_{\text{c}} \ll r_1$ and $Z_0 I_{\text{c}} \ll r_2$ typically hold. Besides, it can be assumed that $V_{\text{d}} - V_{\text{r}} \approx r_1$ for simplicity. This assumption leads to the largest T_{r}, and thus the total transition time can be approximated by

$$T_{\text{tr}} \approx \frac{2\pi}{\omega_0} = 2\pi\sqrt{L_{\text{f}} C_{\text{eq}}} = 2\pi\sqrt{L_{\text{f}}\left(C_{\text{t}} + \frac{C_{\text{sh1}} C_{\text{sub}}}{C_{\text{sub}} + C_{\text{sh1}}}\right)}. \tag{7.5}$$

The maximum T_{tr} occurs when the maximum values of C_{sh1}, C_{t}, and C_{sub} are used, which leads to the largest pulse duty cycle. In other words, under other conditions, the pulse duty cycle can be guaranteed smaller than this value. Neglecting the time of the post-discharge phase T_{p}, the guaranteed pulse duty cycle can be represented by

$$D_{\text{pulse}} = \frac{T_{\text{tr}}}{T_{\text{tr}} + T_{\text{slope}}} = \frac{T_{\text{tr}}}{T_{\text{tr}} + 11 T_{\text{step}}}. \tag{7.6}$$

It can be derived that for a fixed T_{step}, a larger L_{f} results in a larger guaranteed D_{pulse}. Figure 7.1 shows an example of the relationship between the guaranteed D_{pulse} and the filter inductance L_{f}. Here, T_{step} is selected as 300 ns, and C_{sh1}, C_{t}, and C_{sub} are at their maximum values. As validated in Section 2.2, it is preferable to have a small D_{pulse} to prevent ions from shifting to the low-energy spectrum. Thus, once the worst-case Δu_{sh1} has been qualified, it is undesired to increase L_{f} beyond the critical value given by (7.3).

Now that the values of V_{step} and L_{f} have been determined for a given T_{step}, other dimensions of the bias converter can be calculated. For converter design, these dimensions should also be calculated for the worst-case scenario, which corresponds to the highest switching frequency, the highest currents and voltages, and maximum switching loss.

Firstly, the repetition frequency of the bias waveform can be calculated as

$$f_{\mathrm{rep}} = \frac{1}{T_{\mathrm{tr}} + 11T_{\mathrm{step}}} = \frac{1}{2\pi\sqrt{L_{\mathrm{f}}\left(C_{\mathrm{t}} + \frac{C_{\mathrm{sh1}}C_{\mathrm{sub}}}{C_{\mathrm{sub}}+C_{\mathrm{sh1}}}\right)} + 11T_{\mathrm{step}}}. \tag{7.7}$$

Apparently, the maximum repetition frequency is reached at the minimum values of C_{t}, C_{sh1}, and C_{sub}. Moreover, as introduced in Chapter 5, the switching frequency of the submodule M1, M2, and M3 is f_{rep}, $2f_{\mathrm{rep}}$, and $4f_{\mathrm{rep}}$, respectively.

According to (6.12), during the charge phase, the inductor current can be calculated by

$$i_{L_{\mathrm{f}}} = -I_{\mathrm{c}} = -\frac{\mathrm{d}u_{\mathrm{t}}}{\mathrm{d}t}\left(C_{\mathrm{sub}} + C_{\mathrm{t}}\right). \tag{7.8}$$

The maximum I_{c} is obtained at the most negative voltage slope rate and the maximum values of C_{sub} and C_{t}. Combining (6.13) and (6.16) yields

$$i_{L_{\mathrm{f,max}}} = \frac{\sqrt{\left(V_{\mathrm{r}} - V_{\mathrm{e}}\right)^2 + Z_0^2 I_{\mathrm{c}}^2}}{Z_0} = \sqrt{\frac{\left(V_{\mathrm{r}} - V_{\mathrm{e}}\right)^2}{Z_0^2} + I_{\mathrm{c}}^2}. \tag{7.9}$$

As analyzed in Section 6.2.3, V_{r} can always be $V_{\mathrm{d}} - 3V_{\mathrm{step}}$. To obtain a maximum ion energy E_{i}, $V_{\mathrm{d}} - V_{\mathrm{s}}$ should be approximately equal to E_{i} in the worst case. Meanwhile, V_{s} and V_{e} are governed by (6.25). Therefore, the maximum inductor current $i_{L_{\mathrm{f,max}}}$ is determined by

$$\begin{aligned} i_{L_{\mathrm{f,max}}} &= \sqrt{\frac{\left(V_{\mathrm{s}} + E_{\mathrm{i}}/e - 3V_{\mathrm{step}} - V_{\mathrm{s}} + 11V_{\mathrm{step}}\right)^2}{Z_0^2} + I_{\mathrm{c}}^2} \\ &= \sqrt{\frac{\left(E_{\mathrm{i}}/e + 8V_{\mathrm{step}}\right)^2}{Z_0^2} + I_{\mathrm{c}}^2}. \end{aligned} \tag{7.10}$$

Based on (6.9), the worst-case value of $i_{L_{\mathrm{f,max}}}$ is achieved at the maximum values of C_{sh1}, C_{t}, and C_{sub}. Similarly, its minimum current (the most negative current) when restarting the charge phase can be calculated by

$$i_{L_{\mathrm{f,min}}} = -\frac{3V_{\mathrm{step}}}{Z_0}. \tag{7.11}$$

Consequently, all the essential parameters introduced in this section can be represented by functions of T_{step}, as depicted in Figure 7.2. As illustrated in the figure, the voltage step V_{step} is directly proportional to T_{step}, and the critical filter inductance L_{f} increases with an increase in T_{step}. A larger T_{step} leads to longer transition times for the voltage rising and falling edges, resulting in an increase in the guaranteed pulse duty cycle. Furthermore, an increase in T_{step} can decrease the switching frequency of all the submodules and reduce the inductor current simultaneously.

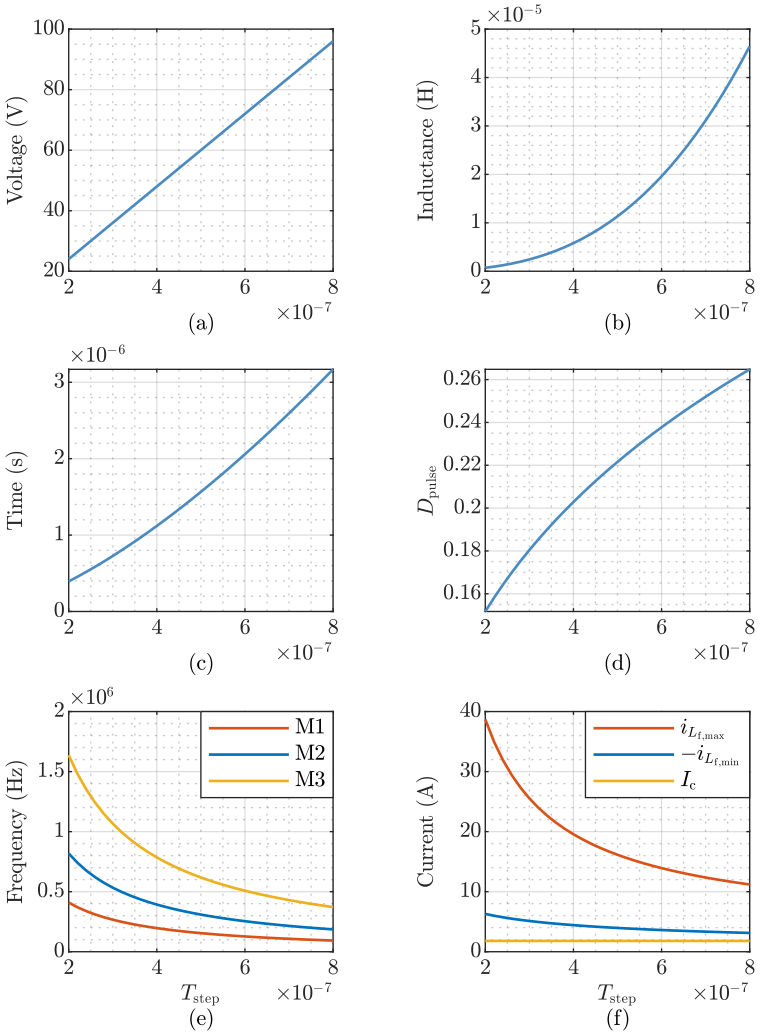


Figure 7.2 The relation of the essential parameters to T_{step}. (a) V_{step}. (b) Filter inductance L_{f}. (c) The total transition time of the voltage rising and falling edge. (d) The guaranteed pulse duty cycle. (e) Switching frequency of each submodule. (f) Variant inductor currents.

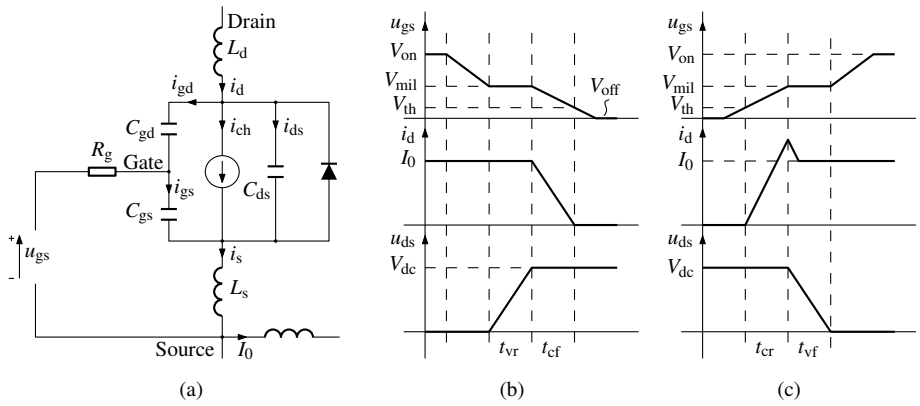


Figure 7.3 (a) The equivalent electric circuit model of a typical MOSFET. Here i_{gs}, i_{gd}, and i_{ds} are the current flowing through C_{gs}, C_{gd}, and C_{ds}, respectively. Simplified waveforms of the gate-source voltage u_{gs}, the drain current i_d, and the drain-source voltage u_{ds} during (b) the turn-off transient and (c) the turn-on transient.

7.3 Switching transient

7.3.1 Simplified analysis

When it comes to the performance of the bias converter, it is preferred for T_{step} to be as small as possible, but this is limited by the capacity of the switching power semiconductors. As T_{step} decreases, the switching frequency and current increase. As seen in Figure 7.2(e), the switching frequency of all the submodules can reach megahertz levels within the considered range. However, such a high switching frequency could introduce significant switching loss to the power semiconductors, which can result in excessively high junction temperature. Although V_{step} decreases at a smaller T_{step}, indicating that the dc-link voltage of each submodule decreases as well, it may still lead to a higher switching loss due to the effect of increasing current and switching frequency.

The switching loss originates from the finite turn-on and turn-off speed during the switching transient. Meanwhile, the finite switching time also sets a minimum for T_{step} to ensure that all the switching cells can completely commutate within each T_{step} and a well-defined waveform can be achieved. Consequently, an accurate model of the switching transient that includes both the switching energy and switching time is critical for pushing the switches to their limits and determining the appropriate value of T_{step}.

In Figure 7.3 (a), an equivalent circuit of a MOSFET with an inductor is depicted,

which represents a part of a basic half-bridge circuit, while the bottom MOSFET is not shown here. It is assumed that the inductor current I_0 is constant during the switching transient. The MOSFET channel is modeled as a current source i_{ch}, controlled by the gate-source voltage u_{gs} with the transconductance. The MOSFETs have internal parasitic capacitances, including the gate-source capacitance C_{gs}, the gate-drain capacitance C_{gd}, and the drain-source capacitance C_{ds}, which affect their switching speed. Stray inductances L_d and L_s also exist in the drain and source terminal, respectively, due to packaging and PCB design. The internal gate resistance R_g restricts the current through the gate and can be supplemented by additional external resistance during turn-on and turn-off to adjust the switching performance.

In Figure 7.3 (b) and (c), simplified waveforms of the gate-source voltage u_{gs}, the drain current i_d, and the drain-source voltage u_{ds} are shown during the turn-off and turn-on transients, respectively. For simplification, all waveforms have been linearized, but they can be more intricate in practice due to the non-linearity of the parasitic capacitances. Furthermore, the parasitic capacitances and the stray inductances can trigger resonance.

During turn-off, first, the gate-source voltage u_{gs} should decrease from the turn-on voltage V_{on} to the Miller voltage V_{mil}. During this time interval, both the drain current i_d and the drain-source voltage u_{ds} remain unchanged. After u_{gs} reaches V_{mil}, u_{ds} starts increasing. During this time interval t_{vr}, a portion of the drain current i_d is charging C_{ds} until u_{ds} reaches the dc-link voltage V_{dc}. Then i_d begins to decrease until it reaches zero in the time interval t_{cf}. Meanwhile, the gate-source voltage u_{gs} drops below the threshold voltage V_{th}, and the MOSFET has been turned-off. Subsequently, u_{gs} continues to decrease to the turn-off voltage V_{off}. As can be observed, u_{ds} and i_d overlap in the time intervals t_{vr} and t_{cf}, causing the turn-off loss, the energy of which can be approximated by

$$E_{off} \approx \frac{1}{2} V_{dc} I_0 \left(t_{vr} + t_{cf} \right). \tag{7.12}$$

Similarly, during turn-on, u_{gs} first rises to its threshold voltage V_{th}. Then, the MOSFET is turned on and starts conducting current. i_d rises during the time interval t_{cr} until u_{gs} reaches the Miller voltage V_{mil}. Note that the Miller voltage can be different during turn-on and turn-off. During the time interval t_{vf}, u_{ds} starts falling until it reaches zero. Afterward, u_{gs} continues to rise until it reaches its turn-on voltage V_{on}. However, a current spike might occur during the transient, caused by the reverse recovery of the body diode of the bottom MOSFET, which can increase both switching loss and time. The mechanism of the reverse recovery is complex to model [97, 100, 109]. However, if a Schottky diode is placed in parallel with one MOSFET in a half-bridge, the reverse recovery effect on its complementary MOSFET can be significantly reduced [110, 130, 152]. Under this circumstance, the reverse

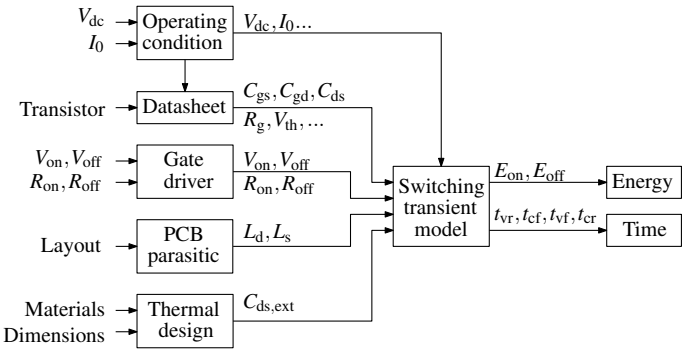


Figure 7.4 Parameters that influence the switching transient, which can be characterized into five categories, including the operation conditions, the MOSFET body parameters, gate driver design, PCB parasitics, and thermal design.

recovery loss becomes negligible. The turn-on energy E_{on} can then be simplified as

$$E_{on} \approx \frac{1}{2} V_{dc} I_0 \left(t_{cr} + t_{vf}\right). \tag{7.13}$$

7.3.2 Switching transient model

The switching transient is influenced by numerous factors, including its operating conditions, body parameters, gate driver, PCB parasitics, thermal design, *etc* [173]. Generally, higher values of V_{dc} and I_0 lead to higher switching energy and longer switching time. Additionally, these two operating conditions affect certain parameters of the MOSFET, such as C_{gs}, C_{gd}, and C_{ds}. In general, these capacitances decrease as the drain-source voltage increases. The gate driver design is also crucial in determining the switching transient. Within a permissible range, a higher V_{on} and a lower V_{off} result in faster turn-on and turn-off transients, thus reducing the switching energy. Furthermore, smaller turn-on and turn-off resistors, denoted by R_{on} and R_{off}, respectively, also lead to a faster switching transient.

In practical designs, parasitics, such as the stray inductances, affect the switching performance, mainly originating from the PCB layout and thermal design. The traces on the PCB inevitably introduce stray inductance to the switch on both the drain and source terminals. These stray inductances, especially the common source inductance L_s, can slow down the switching transient, thus increasing the switching loss. Moreover, it may trigger resonances with the parasitic capacitances during the switching transient.

The thermal design adds an external drain-source capacitance $C_{ds,ext}$ to the switch

due to the isolation material used. Most heatsinks are grounded to PE. Therefore, they cannot be mounted directly to the thermal pads of the MOSFETs, and a dielectric thermal interface material (TIM) must be used for thermal conductivity and electrical isolation. Consequently, an extra capacitance $C_{ds,ext}$ is introduced and added to C_{ds}. The value of $C_{ds,ext}$ is determined by material properties and dimensions.

Figure 7.4 summarizes the parameters that influence the switching transient. An accurate switching transient model that considers all these parameters is required to obtain the switching energy and time.

Endless efforts have been devoted to accurately modeling the switching transient of the MOSFET. The most commonly used model is first proposed in [7], which linearizes the capacitances but neglects other parasitic components, resulting in linear waveforms. The model is very straightforward but can greatly deviate from practice, since the stray inductance can tremendously increase the switching loss. Since then, countless extensive models have been developed by incorporating various parasitic components [20, 43, 76, 78, 142, 145, 182], which generally improve modeling accuracy. However, since model accuracy relies heavily on the accuracy of the MOSFET parameters, experiments are often required to extract certain parameters [115]. For example, an impedance analyzer is used to extract the stray inductance in [182], dedicated experiments are designed to measure the dynamic on-resistance in [76], and a power device analyzer is adopted to obtain the gate charge characteristics in [78].

When designing a power converter, it is desired to know the switching loss in advance instead of measuring it after building the converter. Therefore, to avoid experimental measurements, [27] proposes an analytical switching transient model of SiC MOSFET based entirely on the datasheet. The essence of this method is iteratively solving nonlinear and operating condition dependent parameters, such as Miller voltage and transconductance, to satisfy all crucial equations. Based on its experimental validation and further research evaluations [77, 79], the model strikes a satisfactory balance between accuracy and simplicity.

Hence, this thesis uses the model developed in [27] to calculate switching energy and time. Additionally, SPICE simulations using manufactures' official models are used for comparison and cross-check.

7.3.3 Example implementation

In this section, an example implementation of the switching transient model is introduced for illustration. To clarify, this section only derives the factors that influence the switching transient and the resultant switching energy and time. The model itself is well expatiated in [27], and its derivation is skipped here for brevity.

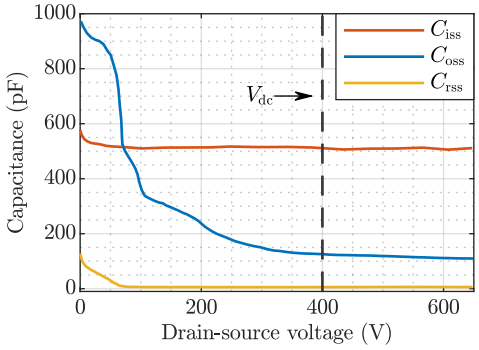


Figure 7.5 The voltage-dependent capacitances of the GaN HEMT GS66516T extracted from the datasheet, being the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse transfer capacitance C_{rss}, respectively.

In other words, the switching transient model is regarded as a known function, and we only deal with its input and output.

As mentioned in the previous section, the cascaded H-bridge submodules require a relatively low dc-link voltage and a high switching frequency, making the GaN high-electron-mobility transistor (HEMT) a suitable choice for this application. While the original switching transient model in [27] is developed for SiC MOSFETs, the similarities between their equivalent electric circuit allow for the migration of the model to GaN HEMTs [76]. In this migration, the dynamic on-resistance effect is omitted [57], as the focus is solely on the switching loss. The GaN HEMT GS66516T manufactured by GaN Systems is used for illustration.

First, the parasitic capacitances of the transistor can be obtained from the device documentation. Figure 7.5 depicts its voltage-dependent capacitances extracted from the datasheet. The charge equivalent capacitances during the switching transient can be determined as

$$C_{\mathrm{gs}} = \int_0^{V_{\mathrm{dc}}} u \cdot \left(C_{\mathrm{iss}}(u) - C_{\mathrm{rss}}(u)\right) \mathrm{d}u, \tag{7.14}$$

$$C_{\mathrm{ds}} = \int_0^{V_{\mathrm{dc}}} u \cdot \left(C_{\mathrm{oss}}(u) - C_{\mathrm{rss}}(u)\right) \mathrm{d}u, \tag{7.15}$$

and

$$C_{\mathrm{gd}} = \int_0^{V_{\mathrm{dc}}} u \cdot C_{\mathrm{rss}}(u) \mathrm{d}u, \tag{7.16}$$

respectively. Taking $V_{\mathrm{dc}} = 400\,\mathrm{V}$ for example, the charge equivalent values of C_{gs}, C_{ds}, and C_{gd} are equal to 503 pF, 324 pF, and 13.7 pF, respectively. Combining C_{ds}

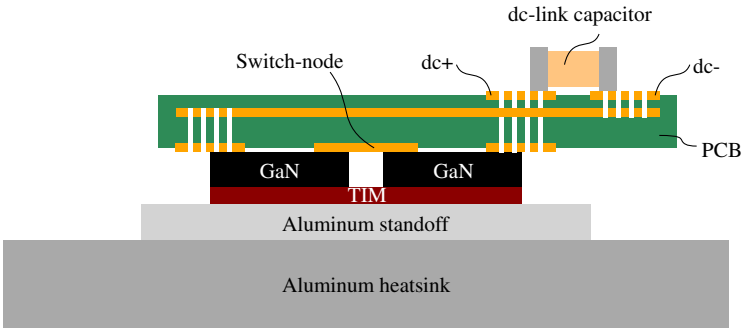


Figure 7.6 The cross-section of the thermal design for the GaN HEMTs (only one of the PCB internal layers is shown here, and others are omitted for simplicity). Between the standoff and the heatsink, there is a layer of conductive thermal paste, which is also omitted.

and C_{gd} leads to a total output capacitance of 337.7 pF, which is very close to the charge equivalent output capacitance given in the datasheet (335 pF) under the same voltage condition.

The internal gate resistance R_g can be obtained directly from the datasheet, which gives $R_g = 0.3\,\Omega$. The threshold voltage V_{th} can be read from the transfer characteristic figure in the datasheet, which is approximately 1.6 V. It must be clarified that its transfer characteristic curves are temperature-dependent, and the one at 25 °C is selected for calculation. It has also been found that using a different curve at higher temperature makes minor difference to the switching energy and time. Furthermore, the datasheet has indicated the typical gate driver design, *i.e.*, $V_{on} = 6\,V$, $V_{off} = 0\,V$, $R_{on} = 10\,\Omega$, and $R_{off} = 1\,\Omega$.

The stray inductance is highly dependent on the package and PCB layout design. It is assumed that the stray inductance introduced by the package of the device is equivalent to the manufacturer's SPICE model, resulting in $L_s = 0.15\,nH$ and $L_d = 0.37\,nH$. When designing the PCB, the trace lengths of the gate-source loop and the power loop should be minimized. It is assumed that the PCB design contributes extra 0.1 nH to L_s and 0.5 nH to L_d, based on a rough estimation of the PCB trace routing.

The external drain-source capacitance is determined by the thermal design. A typical thermal design for this top-cooled GaN transistor is considered as represented in Figure 7.6. The transistors are placed on the bottom of the PCB and mounted to a large aluminum heatsink with a TIM and aluminum standoff in between. Here the TIM is dielectric, and the aluminum standoff is connected to PE. It forms a parasitic capacitance $C_{ds,ext}$, which is electrically connected between the thermal pad of the

transistor and the heatsink (PE). The value of $C_{ds,ext}$ can be determined by

$$C_{ds,ext} = \frac{\epsilon_0 \epsilon_r A_{cu}}{h_{tim}}, \tag{7.17}$$

where ϵ_r is the relative permittivity of the TIM, A_{cu} is the area of the thermal pad of the transistor, and h_{tim} is the thickness of the TIM. For the GS66516T transistor used in this study, A_{cu} is about 69 mm^2 (approximated by its surface area).

It is noteworthy that although both transistors in a half-bridge with a dc supply referenced to PE (like the T-type converter in this bias converter) are capacitively coupled to PE through the TIM, only the $C_{ds,ext}$ of the upper-leg transistor is connected to the switched-node and affecting the switching transient. This is because the thermal pad is electrically connected to the source of the HEMT, and for the bottom transistor (the one connected to dc-), its $C_{ds,ext}$ is eventually shorted [82, 150]. Such an effect is similar for those transistors with thermal pad electrically connected to their drains (the $C_{ds,ext}$ of the top switch adds up to the dc-link capacitance). Therefore, the TIM only adds one $C_{ds,ext}$ to the switched-node, which is equivalent to adding $\frac{1}{2}C_{ds,ext}$ to C_{ds} for each transistor in a half-bridge.

For the half-bridge with an isolated dc supply, like the cascaded H-bridges in this bias converter, the dc-link voltage is not referenced to PE. However, there is still a distributed capacitance between the dc-link and PE. As a result, the extra capacitance added to the switched-node is equal to $C_{ds,ext}$ in series with the distributed capacitance, and this lumped value is always smaller than $C_{ds,ext}$. In the worst case, it can be assumed to be equal to $C_{ds,ext}$. Under these circumstances, it is also equivalent to adding $\frac{1}{2}C_{ds,ext}$ to C_{ds} for each transistor in a half-bridge.

The power dissipation of the transistors is converted into heat, which is thermally conducted to the aluminum heatsink through the TIM. This thermally conductive path has three significant thermal resistances: the junction-to-case thermal resistance of the transistor $R_{th,jc}$, the thermal resistance introduced by the TIM $R_{th,tim}$, and the heatsink-to-ambient thermal resistance $R_{th,hs}$. $R_{th,jc}$ can be obtained from the datasheet, which is equal to 0.27 K W^{-1}. $R_{th,hs}$ is determined by the dimension of the heatsink. According to [178], $R_{th,tim}$ can be approximated by

$$R_{th,tim} = \frac{h_{tim}}{\kappa A_{cu}}, \tag{7.18}$$

where κ is the thermal conductivity of the TIM. Taking the TIM BERGQUIST SIL-PAD 1500 manufactured by Henkel as an example, its thickness is 0.254 mm, the relative permittivity is 4.0, and the thermal conductivity is 2 W m^{-1} K^{-1}. This leads to $C_{ds,ext} = 9.58$ pF and $R_{th,tim} = 1.85$ K W^{-1}.

By now, all the inputs to the switching transient model have been established, and the switching transient can be solved by the model. The switching energy and time

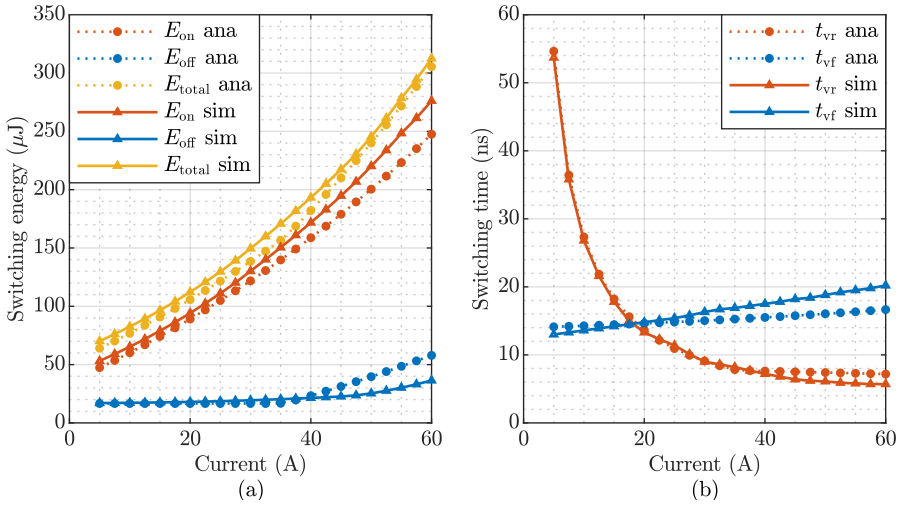


Figure 7.7 The comparison of the results from the analytical switching transient model (abbreviated by 'ana') and SPICE simulations (abbreviated by 'sim'). (a) Switching energy, where $E_{total} = E_{on} + E_{off}$. (b) Switching time.

have been calculated under different currents and are plotted in Figure 7.7(a) and (b), respectively. The voltage rising and falling times are of more interest. Therefore, only t_{vr} and t_{vf} are plotted here. For comparison, SPICE simulations under the same operating conditions are conducted.

As shown in the figure, the results obtained from the model and the simulations generally match well, indicating the effectiveness and accuracy of this model. The turn-on energy E_{on} is rising with the switching current, while the turn-off energy E_{off} remains unchanged when the switching current is lower than 40 A. This is because zero-voltage switching (ZVS) is achieved during turn-off when the switching current is lower than 40 A, meaning all the current is flows through C_{ds} and $i_{ch} = 0$ during turn-off. Therefore, the turn-off energy is the snubber energy of the drain-source capacitance [27, 67]. Although the differences in E_{on} and E_{off} between the analytical model and simulations start to deviate at higher current, the relative errors of E_{total} are always within 10%.

As seen from Figure 7.7(b), in both the analytical model and simulations, the voltage rising time t_{vr} decreases with increasing switching current, while the voltage falling time t_{vf} increases. The values of t_{vr} obtained from the analytical model and the simulations match very well, while the values of t_{vf} have an absolute difference of less than 5 ns.

Since the analytical model is much faster with similar accuracy compared to the SPICE simulation, it is better suited for the proposed design methodology.

7.4 Design selection

As explained in Section 7.2, the properties of the converter are determined by the value of T_{step}, which is limited by the capability of the power semiconductors. Different T_{step} values lead to varying dc-link voltage and switching current for each submodule, resulting in different switching time, power dissipation, and temperature for each switch. The feasibility of different T_{step} values can be verified with the switching transient model introduced in Section 7.3. In this section, each submodule of the bias converter is analyzed based on its operating conditions, and the power dissipation, junction temperature, and switching time of their switches are determined under different T_{step}. Eventually, all feasible design selections can be collected.

For simplicity, all submodules use the same GaN HEMT GS66516T. They are mounted on the same heatsink, which has a large volume and negligible thermal resistance. Therefore, the lumped thermal resistance is determined by

$$R_{\text{th}} = R_{\text{th,jc}} + R_{\text{th,tim}} = 2.13\,\text{K}\,\text{W}^{-1}. \tag{7.19}$$

The gate driver, PCB parasitics, and thermal design are the same as in the previous sections, and they are uniform for different submodules and under different operating conditions, except for $V_{\text{on}} = 5\,\text{V}$ to simplify circuit design. Consequently, E_{on}, E_{off}, t_{vr}, and t_{vf} can be regarded as a function of their dc-link voltage V_{dc} and switching current I_0, which can be defined by four functions, as represented by $E_{\text{on}}(V_{\text{dc}}, I_0)$, $E_{\text{off}}(V_{\text{dc}}, I_0)$, $t_{\text{vr}}(V_{\text{dc}}, I_0)$, and $t_{\text{vf}}(V_{\text{dc}}, I_0)$, respectively.

7.4.1 Worst case estimation

Submodule M1 (T-type converter)

In accordance with Chapter 5, submodule M1 features switches that are turned on and off once in a fundamental period. The dc-link voltage is distributed as follows: $V_{\text{dsn}} + 4V_{\text{step}}$ between S_{11} and S_{12}, V_{dc} between S_{11} and S_{13} and S_{14}, and $4V_{\text{step}}$ between S_{12} and S_{13} and S_{14}.

As shown in Figure 7.8, switch S_{11} is turned on at T_0, when its drain-source voltage commutates from $V_{\text{dsn}} + 4V_{\text{step}}$ to 0. Meanwhile, the inductor current starts rising, the maximum transient inductor current is equal to $i_{L_{\text{f,max}}}$. Due to turn-on delay, in the worst-case scenario, switch S_{11} is assumed to experience a turn-on current of $i_{L_{\text{f,max}}}$.

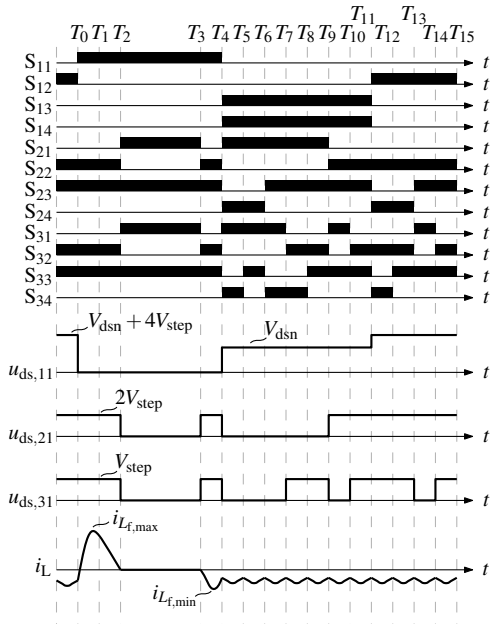


Figure 7.8 The operating principle of the switches, where $u_{ds,11}$, $u_{ds,21}$, and $u_{ds,31}$ represent the drain-source voltage of S_{11}, S_{21}, and S_{31}, respectively.

At T_4, S_{11} is turned off, and its drain-source voltage commutates from 0 to V_{dsn}. Ideally, S_{11} should be turned off when it conducts a negative current, which enables ZVS and significantly reduces the turn-off loss. However, if T_4 is not well regulated by trajectory control, S_{11} can be turned off at a positive current, the maximum value of which is equal to $-i_{L_{f,max}}$, according to the state-diagram depicted in Figure 6.3.

Under these circumstances, S_{11} has the highest switching loss among all the switches in this submodule. This switching loss is calculated by

$$P_{sw,M1} = f_{rep}\left(E_{on}(V_{dsn} + 4V_{step}, i_{L_{f,max}}) + E_{off}(V_{dsn}, -i_{L_{f,min}})\right). \tag{7.20}$$

During the voltage rising and falling edge, the switched-node voltage is not defined. Thus, the total time for the switched-node voltage to commutate to the defined value should be short enough to satisfy the T_{step} constraint. As higher switching currents result in a smaller t_{vr} and a larger t_{vf}, the longest commutation time for submodule M1 occurs at T_0, when S_{12} is turned off with a switching current of I_c and S_{11} is turned on with a switching current of $i_{L_{f,max}}$. This is illustrated in Figure 5.7. The total commutation time can be determined as

$$t_{sw,M1} = t_{vr}(V_{dsn} + 4V_{step}, I_c) + t_{vf}(V_{dsn} + 4V_{step}, i_{L_{f,max}}). \tag{7.21}$$

Submodule M2

The switching behavior of submodule M2 involves each switch being turned on and off twice in a fundamental period, with a corresponding dc-link voltage of $2V_{\text{step}}$, as shown in Figure 7.8.

Similar to submodule M1, in the worst-case scenario, switch S_{21} is turned on and off during the voltage rising and falling edge, resulting in a turn-on current of $i_{L_{\text{f,max}}}$ and a turn-off current of $-i_{L_{\text{f,max}}}$.

During the charge phase, S_{21} is once again turned on and off. Ideally, the switching current for S_{21} during the charge phase is $-I_{\text{c}}$, which enables ZVS. However, due to the possible resonance if the switching time is not well regulated by trajectory control, it can be switched on and off at a positive current, which is estimated by I_{c}. As a result, the total switching loss can be calculated by

$$\begin{aligned} P_{\text{sw,M2}} =& f_{\text{rep}} \left(E_{\text{on}}(2V_{\text{step}}, i_{L_{\text{f,max}}}) + E_{\text{off}}(2V_{\text{step}}, -i_{L_{\text{f,min}}}) \right) \\ &+ f_{\text{rep}} \left(E_{\text{on}}(2V_{\text{step}}, I_{\text{c}}) + E_{\text{off}}(2V_{\text{step}}, I_{\text{c}}) \right). \end{aligned} \tag{7.22}$$

The longest commutation time for submodule M2, similar to that of submodule M1, occurs at the voltage rising edge and can be calculated as

$$t_{\text{sw,M2}} = t_{\text{vr}}(2V_{\text{step}}, I_{\text{c}}) + t_{\text{vf}}(2V_{\text{step}}, i_{L_{\text{f,max}}}). \tag{7.23}$$

Submodule M3

For submodule M3, the switches are turned on and off for four times in a fundamental period, and their dc-link voltage is V_{step}, as shown in Figure 7.8.

Similar to submodule M2, in the worst-case scenario, switch S_{31} is turned on and off once during the voltage rising and falling edge, thus having a turn-on current of $i_{L_{\text{f,max}}}$ and a turn-off current of $-i_{L_{\text{f,max}}}$. During the charge phase, it can be turned on and off three times at a switching current of I_{c}. Therefore, the total switching loss can be calculated by

$$\begin{aligned} P_{\text{sw,M3}} =& f_{\text{rep}} \left(E_{\text{on}}(V_{\text{step}}, i_{L_{\text{f,max}}}) + E_{\text{off}}(V_{\text{step}}, -i_{L_{\text{f,min}}}) \right) \\ &+ 3f_{\text{rep}} \left(E_{\text{on}}(V_{\text{step}}, I_{\text{c}}) + E_{\text{off}}(V_{\text{step}}, I_{\text{c}}) \right). \end{aligned} \tag{7.24}$$

The longest commutation time for submodule M3 also occurs at the voltage rising edge, which is

$$t_{\text{sw,M3}} = t_{\text{vr}}(V_{\text{step}}, I_{\text{c}}) + t_{\text{vf}}(V_{\text{step}}, i_{L_{\text{f,max}}}). \tag{7.25}$$

7.4.2 Design selection

The dc-link voltage for switches S_{11} and S_{12} is equal to $V_{\text{dsn}} + 4V_{\text{step}}$, and the maximum voltage of GS66516T is 650 V. Therefore, when V_{step} increases, V_{dsn} is limited

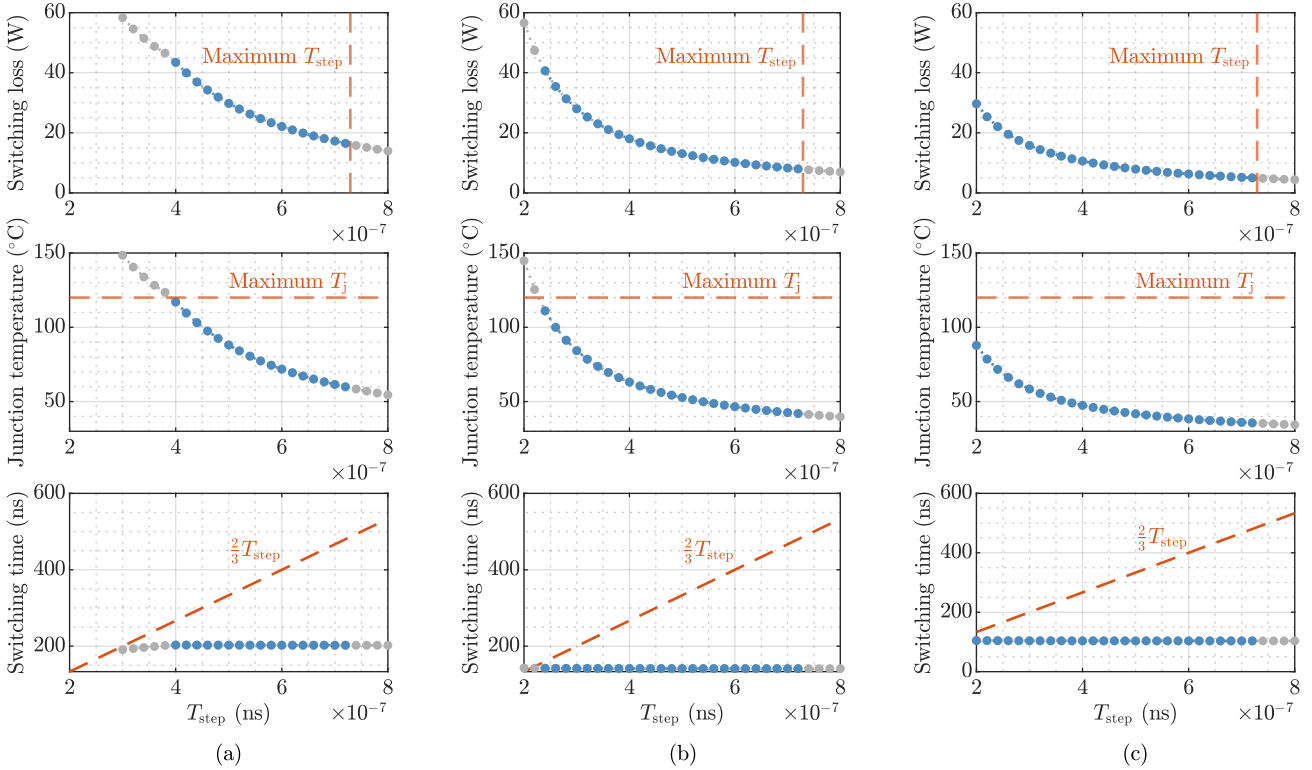


Figure 7.9 The performance of the GaN HEMT GS66516T in submodule (a) M1, (b) M2, and (c) M3, respectively. From the top to bottom, the figures are the switching loss, junction temperature, and switching time, respectively. The red dashed lines indicate the preset constraints of the maximum T_{step}, the maximum junction temperature T_j, and the maximum switching time, respectively. The gray dots represent the operating conditions within the rating of the switch, and the colored dots represent the operating conditions meeting the preset constraints.

by the voltage rating of the switch. As the required E_i can be as high as 250 eV, V_{dsn} must also be able to reach 250 V in any scenario. Consequently, the maximum value of V_{step} that can be used is limited to 87.5 V, if leaving 50 V safety margin for the dc-link voltage (meaning that the maximum value of $V_{dsn} + 4V_{step}$ is target at 600 V). This maximum V_{step} corresponds to a maximum T_{step} equal to 729 ns.

Besides, the maximum junction temperature of the GS66516T transistor is 150 °C. To ensure a safety margin, the maximum junction temperature in this converter is set to 120 °C at an ambient temperature of 25 °C. Moreover, to ensure a well-defined voltage waveform, the maximum commutation time is set to $\frac{2}{3}T_{step}$. With these constraints, feasible design selections can be obtained as plotted in Figure 7.9.

As shown in the figure, higher T_{step} results in lower switching loss and junction temperature. The switching time requirement also becomes less critical in relative to T_{step}. According to Figure 7.2, this is because higher T_{step} leads to a smaller switching current and switching frequency at the cost of a higher D_{pulse}.

If minimizing switching loss is the top priority, then a higher T_{step} should be selected. If the performance of the bias converter is the primary consideration, then D_{pulse} should be minimized to maximize the duty cycle of the charge phase. Therefore, T_{step} should be minimized.

For this design, the minimum value of T_{step} that yields the smallest D_{pulse} is selected, which is 400 ns. By comparing Figure 7.9(a), (b), and (c), it can be concluded that submodule M1 is the bottleneck for further reducing T_{step}, due to its highest switching loss and commutation time. Despite having the lowest switching frequency compared to the other submodules, the effect of a higher dc-link voltage dominates in determining its switching loss.

Once T_{step} is selected as 400 ns, other parameters of the bias converter can be determined using Figure 7.2. V_{step} should be set to 50.4 V, and L_f should be approximately 5.8 µH. The switching frequency for submodule M1, M2, and M3 are approximately 196, 393, 785 kHz, respectively.

7.5 Conclusion

This chapter presents a top-down design methodology that allows for proper design selections to be made for the proposed bias converter in plasma processing applications based on a given specification of the IED and plasma reactor. The method demonstrates that key parameters of the bias converter, such as V_{step}, the filter inductance L_f, and the switching frequency, are dependent on T_{step}. Therefore, determining T_{step} is a crucial step in this design approach.

Notably, the capability of the switching devices restricts the value of T_{step} because a lower T_{step} results in a higher switching current and frequency, leading to higher switching loss. Additionally, a lower T_{step} places a more demanding requirement on the switching time of the power semiconductors. To calculate the switching energy and time accurately, an analytical switching transient model is employed. By using this model, the switching performance under various V_{step} values can be determined, and all the feasible design selections can be collected. Among the feasible design selections, trade-offs can be made to achieve a balance between the pulse duty cycle D_{pulse} and switching loss.

In this chapter, the minimum V_{step} is chosen to target a minimal D_{pulse} for optimal IED, and the corresponding circuit parameters are determined, which enable the prototype design described in the following chapter.

CHAPTER 8

Experimental validation

In this chapter, a bias converter prototype is described for experimental validation. It uses the multilevel topology proposed in Chapter 5, and the design selection is determined based on Chapter 7. The prototype consists of various PCBs, including a converter board, a switched damping board, an interface board connected with the control platform, two isolated dc supply boards, and a plasma mockup board designed to emulate the electrical responses of an actual plasma reactor. The control of the converter is executed by the field programmable gate array (FPGA) of a dSPACE MicroLabBox platform. Experiments have been conducted, and the results underscore the effectiveness of the proposed converter and its trajectory control.

8.1 Experimental setup

8.1.1 Converter board

The majority of the power circuits is located on the converter board, as shown in Figure 8.1. Its topology is shown in Figure 5.6, which contains a T-type submodule and two cascaded H-bridge submodules, which use the same GaN HEMTs GS66516T. High speed gate drivers, namely 1EDN7512GXTMA1 manufactured by Infineon, are employed and positioned on the bottom of the PCB together with all the switching devices, as shown in Figure 8.2.

The switching devices are thermally coupled with a large aluminum heatsink

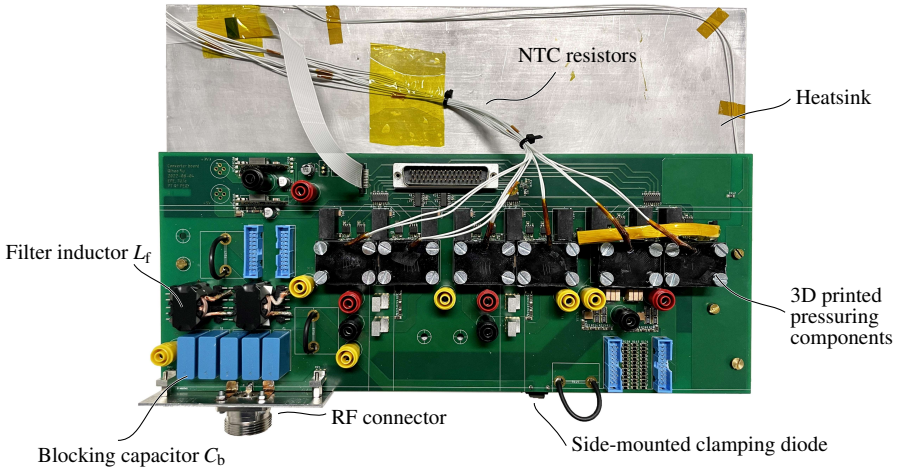


Figure 8.1 A photograph of the converter board.

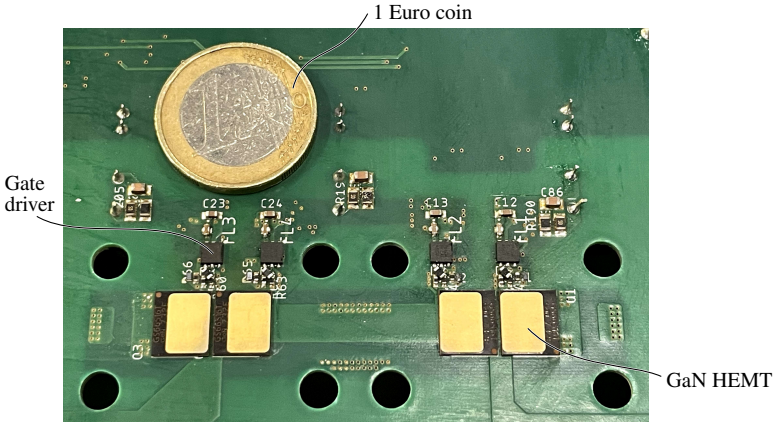


Figure 8.2 A photograph of switches and gate drivers in an H-bridge. A coin is used for size comparison.

through the Bergquist SIL PAD 1500 TIM manufactured by Henkel and an aluminum standoff. The digital isolators and the dc-link capacitors are situated on the top of the PCB. The layout of the power loop has been depicted in Figure 7.6. Besides, six pressuring components are 3D-printed and affixed to the heatsink to provide proper mounting pressure for better thermal coupling. A SiC Schottky diode LSIC2SD170B25 manufactured by Littlefuse is used as the clamping diode, and it is also thermally coupled to the sidewall of the heatsink through a aluminum nitride (AlN) TIM.

As introduced in Chapter 7, T_{step} is selected to be 400 ns. This small T_{step} necessitates a minimal dead-time to ensure a well-defined switched-node voltage for the majority of the time. As detailed in [177], interlock gate drivers can achieve the shortest dead-time. It samples the gate-source voltage of each switch and feeds it back through a digital isolator to the gate driver of its complementary switch. If the gate-source voltage of one switch is high, the gate driver of its complementary switch is consistently disabled. This method ensures the minimum dead-time which is purely caused by the delay variances of the hardware. In this converter, both the T-type and H-bridge submodules utilize the interlock gate drivers. For the T-type converter, additional interlocks are required between S_{11} and S_{13}, as well as between S_{12} and S_{14}. For all the switches, the minimum dead-time is measured to be about 35 ns. In practice, a dead-time of 50 ns is set for a safety margin.

The control signals are received via a Sub-D connector from the interface board. Differential signal transmitters are employed to enhance noise immunity. The switched-node of the bias converter can be connected to the switched damping board through insulation-displacement connector (IDC) cables, but the switched damping circuit can also be bypassed.

The filter inductor is customized in accordance with the design selections outlined in Chapter 7. Two identical inductors are placed in parallel for current sharing, which yield an equivalent inductance of 6.03 µH. Given the high switching frequency of the GaN HEMTs, magnetic cores with N49 material from TDK, designed for high-frequency applications, are utilized to minimize iron loss. Litz wires are adopted to lower ac resistance. For the blocking capacitor, a total of five film capacitors, each rated at 0.22 µF, are connected in parallel. Consequently, the cumulative blocking capacitance significantly surpasses the load capacitance. The output is delivered to the plasma mockup via high-voltage RF coaxial connectors and coaxial cables.

When powered off, the converter exhibits a capacitance of 2.6 nF between its output and PE, which equivalently adds up to C_t. This capacitance mainly originates from the parasitic capacitances of the transistors in each submodule and the clamping diode, as well as the parasitic capacitance across the isolation barriers of the control circuitry, and the capacitive coupling between the PCB and the heatsink. It's

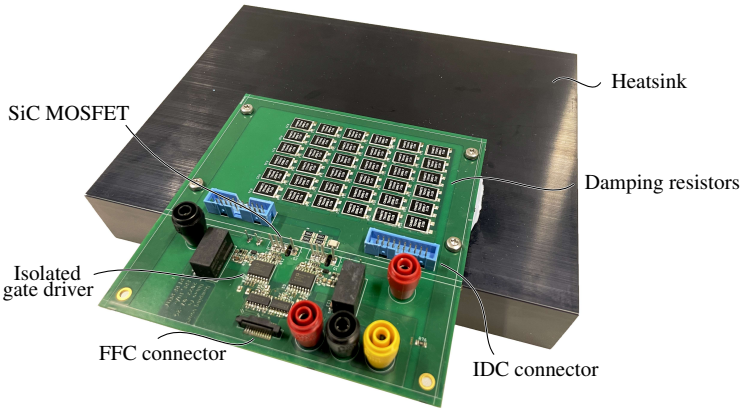


Figure 8.3 A photograph of the switched damping board.

worth noting that this capacitance is nonlinear and tends to diminish at higher voltage, considering the general trend of decreasing parasitic capacitances of power semiconductors with increasing voltages.

8.1.2 Switched damping board

Figure 8.3 shows a photograph of the switched damping board. The four-quadrant switch configuration is constituted by two through-hole SiC MOSFETs C3M0065100K fabricated by Wolfspeed. Each MOSFET is connected to an anti-parallel through-hole SiC Schottky diode E4D20120A from Wolfspeed, designed to curtail reverse recovery losses. Effective thermal coupling of all power semiconductors is achieved through an aluminum heatsink affixed to the side wall, facilitated by the AlN TIM. The control signals for these switches are transmitted from the converter board through a flat flex cable (FFC). Each MOSFET is equipped with an isolated gate driver, specifically the Analog Devices-manufactured ADUM4136. This gate driver has the capability to activate desaturation protection for the MOSFET within a mere 1 µs in instances of saturation.

The damping resistor is constructed using a 6×6 array of thick-film resistors. All these resistors share identical characteristics, collectively yielding a total resistance of 20 Ω. These resistors are cooled from the bottom side through a 2 mm-thick layer of liquid dispense gap filler, while being thermally interconnected with an aluminum heatsink. Each resistor has a typical equivalent series inductance of 14.65 nH. As the damping resistors and the SiC MOSFETs alternately carry the filter inductor current, the presence of parasitic inductance might lead to voltage spikes during current

Figure 8.4 A photograph of the interface board with dSPACE MicroLabBox.

commutation. Therefore, an RC snubber has been incorporated in parallel with the resistor array to absorb energy and mitigate voltage overshoots.

8.1.3 Interface board

The interface board has been meticulously crafted to establish a seamless connection between the dSPACE MicroLabBox platform and the hardware prototype, as visually represented in Figure 8.4. The board is plugged into the box using Sub-D connectors, a strategic approach that ensures the signal traces are maintained at minimal lengths. The control signals are generated by the internal FPGA of the dSPACE platform, transmitted by the differential transmitters, and sent to the converter board through a Sub-D connector and a shielded cable. The time resolution of the FPGA is 10 ns. Therefore, all the time-related control values are rounded to this resolution.

Various voltages and currents are measured by probes and fed to the interface board through coaxial connectors for both hardware and software over-voltage and over-current protection. Multiple negative temperature coefficient (NTC) resistors are placed on various locations on the converter, the switched damping board, and the plasma mockup, and they are connected to the interfaced board for hardware over-temperature protection.

8.1.4 Isolated supply board

The cascaded H-bridges require bidirectional isolated dc supplies to provide dc-link voltages with minimal capacitive coupling with respect to PE, as explained in Chapter 7. At lower voltage levels, the lithium-ion batteries are employed to supply the dc-link voltage, effectively circumventing any substantial capacitive coupling

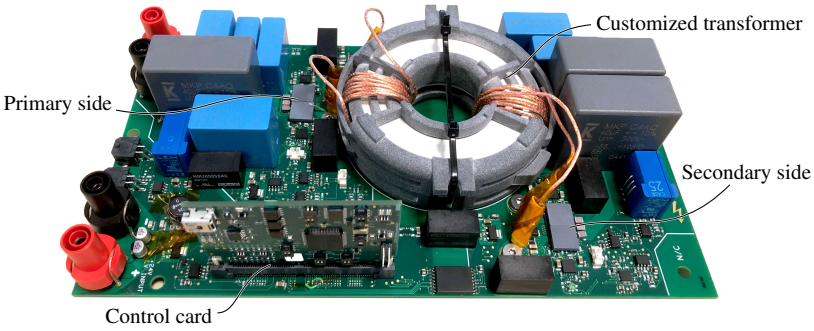


Figure 8.5 A photograph of the isolated dc supply.

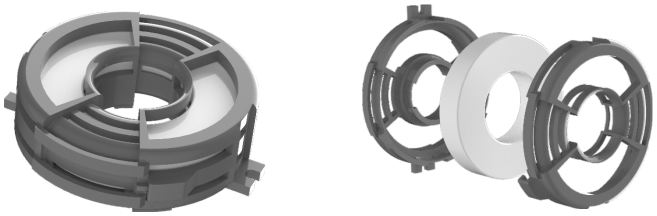


Figure 8.6 (a) An assembled view and (b) an exploded view of the customized transformer bobbin with the magnetic core.

with PE. In this experiment, if the dc-link voltage remains below 16 V, it is supplied with the lithium-ion batteries, with up to four batteries connected in series.

To provide dc-link voltages exceeding 16 V, isolated dc supplies with ultra-low parasitic capacitance have been designed. Figure 8.5 shows a photograph of the isolated supply. The supply is based on the dual-active bridge (DAB) topology with closed-loop controlled phase-shift modulation. The control of the converter is orchestrated by a TMS320F280025 control card from Texas Instruments. Both input and output voltages are capped at 120 V, while the maximum output power is 240 W. GaN HEMTs (GS-065-008-1-L manufactured by GaN Systems) are used as the switching devices in both primary and secondary sides, and their switching frequency is 300 kHz. Digital isolators and isolated supplies with ultra low capacitances for the gate drivers are used for the transistors.

In the context of a typical isolated supply, the principal contributor to parasitic capacitance often lies within the transformer, primarily attributed to capacitive coupling between its primary and secondary windings. As a countermeasure, the present isolated supply employs a relatively sizeable toroid magnetic core, specifically the TX80/40/15-3C94 model from Ferroxcube. This core's dimensions serve to increase the separation between the primary and secondary windings, consequently diminishing capacitive coupling. Further optimization of parameters governing winding geometry, such as turn-core distance, is undertaken to minimize inter-winding capacitance, based on a capacitance model proposed in [125]. For achieving the intended physical configuration, a customized bobbin is crafted to achieve the optimized physical geometry using 3D printing technology, as depicted in Figure 8.6.

The cumulative parasitic capacitance between the converter output and PE approximates 11.4 pF. This aggregate value is attributed to contributions from cables and traces (1.6 pF), control devices (4.8 pF), and the transformer (5.0 pF). For a more comprehensive exploration of this converter's intricacies, additional insights are offered in [133].

8.1.5 Plasma mockup

To facilitate experimentation of the converter prototype within an electrical engineering lab setting, a plasma mockup has been ingeniously devised. This mockup emulates the electrical responses characteristic of an authentic plasma reactor, in accordance with the EEC model introduced in Chapter 2. The schematic outlining the configuration of the plasma mockup is illustrated in Figure 8.7. Notably, this emulation involves pertinent adaptations and simplifications from the original EEC model to enable practical realization.

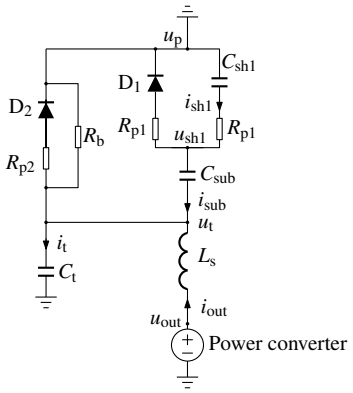


Figure 8.7 The circuit schematic of the plasma mockup.

As introduced in Chapter 2, R_p is subject to variation across distinct phases of the process. During the charge phase and discharge phase, R_p is relatively small, while during the post-discharge phase, R_p is significantly larger. In practice, to avoid using active components for a switched resistor, R_p is split into two different resistors: R_{p1} and R_{p2}. R_{p1} represents the low resistance during the charge and discharge phase, while R_{p2} represents the substantially larger resistance during the post-discharge phase when D_2 is conducting. Therefore, these different resistors should be relocated to each path, instead of being grounded, as shown in Figure 8.7.

Such an arrangement makes the current waveforms of each path similar with the EEC model, but it leads to different voltage waveforms. Specifically, during the post-discharge phase when u_t holds a positive discharge voltage V_d, this voltage V_d almost completely falls over R_{p2}. Under this circumstance, C_{sh1} and C_{sub} cannot be fully discharged. Instead, there is a dc voltage built over C_{sh1} and C_{sub}. When restarting the charge phase, this dc voltage acts as a bias, leading to a different V_s on u_{sh1}, which is deviated with the EEC model.

Besides, the simulation omits consideration of the ion current I_{i1} and I_{i2}. Due to the fast voltage rising and falling at u_t and u_{sh1}, it is challenging to have a dc current source functionally operating at such high voltage slew rate in practice. Compared to the EEC model, neglecting I_{i1} causes a linearly decreasing u_{sh1} during the charge phase, instead of a quasi-constant u_{sh1}. However, the transient response of the plasma mockup remains very similar and representative. Thus, despite these simplifications, the mockup retains its suitability for validating trajectory control approaches.

Figure 8.8 shows a photograph of plasma mockup. For the construction of R_{p1}, a configuration involving a 22×9 array of pulse-proof resistors has been adopted,

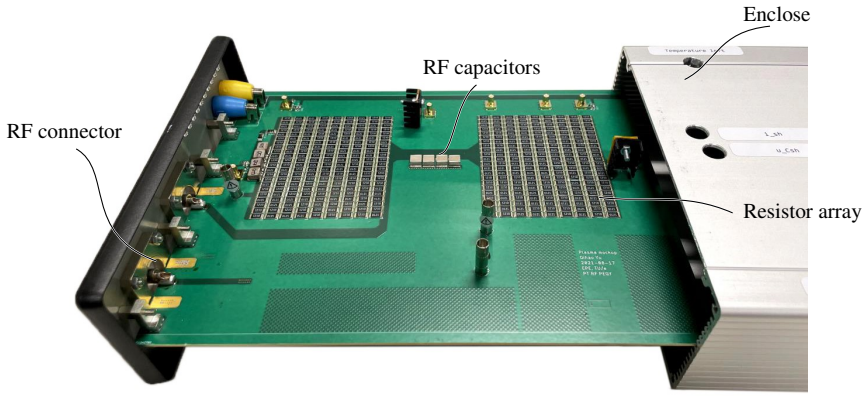


Figure 8.8 A photograph of the plasma mockup.

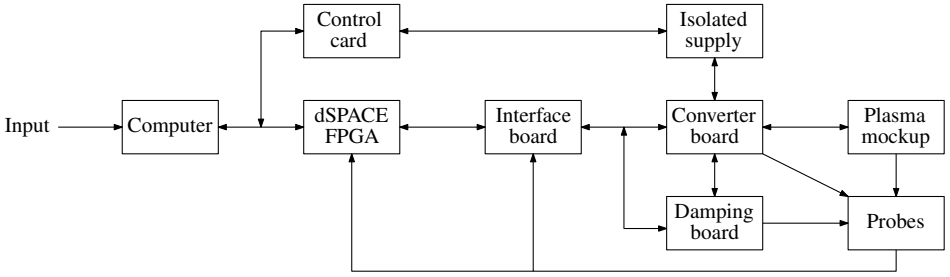


Figure 8.9 The block diagram of the experimental setup.

with each resistor amounting to 121 Ω. Consequently, R_{p1} is calculated to be approximately 50 Ω. The value assigned to R_{p2} is roughly 5 kΩ, whereas the bleeder resistor R_b holds a value of around 300 kΩ. RF capacitors are used for C_t, C_{sub}, and C_{sh1}, which are equal to 2.35 nF, 1.08 nF, and 0.48 nF, respectively. A through-hole SiC Schottky diode E4D20120A manufactured by Wolfspeed is used for both D_1 and D_2. Notably, this diode is characterized by a voltage-dependent parasitic capacitance, contributing to an effective augmentation of C_{sh1}, particularly evident at low voltage levels. To encapsulate the entire arrangement, an aluminum enclosure has been introduced, serving to curtail electromagnetic emissions.

8.1.6 Overview of the experimental setup

An overview of the experimental setup is illustrated in Figure 8.9. The circuit parameters, along with the requisite waveform profiles, serve as inputs to the computer. In response, the corresponding control parameters are computed within the CPU of the computer. The time settings are sent to the FPGA of the dSPACE

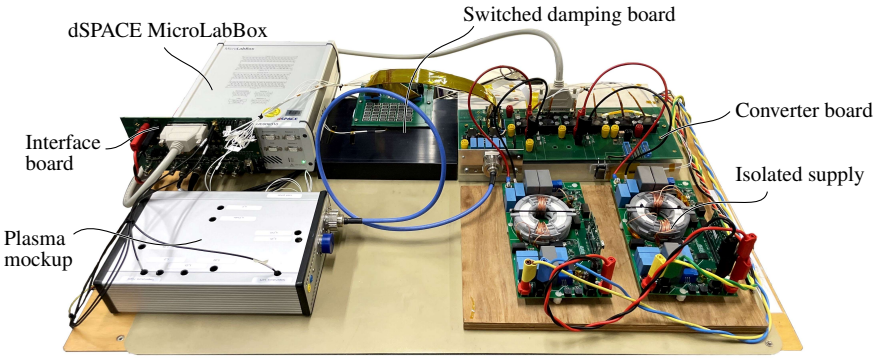


Figure 8.10 A photograph of the experimental setup. Several cables and probes are not shown for better visualization.

platform to control the gate-source voltages of the switches on the converter board and damping board. Additionally, the value of V_{step} is communicated to the control card through a JTAG-USB cable. This input serves to establish the output voltages of the isolated supplies.

The FPGA generates generates control signals for switching operations based on the control parameters, thereafter transmitting these signals through the interface board to both the converter board and the switched damping board. The control card primarily manages the V_{step} value, concurrently exercising phase-shift control to regulate the output voltage of the isolated dc supply.

Multiple probes are used to measure the voltage and current waveforms of the converter board, damping board, and the plasma mockup. The measured results undergo feedback to the interface board for hardware protection, as well as to the dSPACE platform for software protection. Figure 8.10 shows a photograph of the experimental setup.

8.2 Experimental results

8.2.1 Functional test

Trajectory control

As previously introduced, the converter has a voltage-dependent parasitic capacitance between its output and the PE. To validate the trajectory control method on this bias converter, it is desired to operate it under low voltages, since all capacitances remain relatively stable compared to their values measured at zero voltage.

Table 8.1 The converter configuration for functional test

Parameter	Value	Unit	Parameter	Value	Unit
V_{dsn}	76	V	V_{step}	8	V
V_{rsn}	52	V	V_{fsn}	52	V
T_{step}	400	ns	T_{p2}	200	ns
$\dot{u}_{\mathrm{out}}$	$-2 \cdot 10^7$	$\mathrm{V\,s^{-1}}$			

Table 8.2 The key parameters for trajectory control under different conditions

Values	T_{r} (ns)	T_{p1} (ns)	T_{f} (ns)	$i_{L_{\mathrm{f,max}}}$ (A)	$i_{L_{\mathrm{f,min}}}$ (A)
Calculated	325	817	543	3.25	-0.72
Finely tuned	250	640	450	2.76	-0.65
Calibrated	265	654	439	2.60	-0.57

In this low-voltage test, V_{step} was equal to 8 V, and V_{dsn} was equal to 76 V. This makes it appropriate to utilize $V_{\mathrm{dsn}} - 3V_{\mathrm{step}}$ for V_{fsn} during the voltage falling edge, as elaborated in Chapter 6. Besides, $V_{\mathrm{dsn}} - 3V_{\mathrm{step}}$ was also adopted for V_{rsn} at the switched-node during the voltage rising edge. Furthermore, a value of T_{step} amounting to 400 ns was chosen. Consequently, the corresponding theoretical slope rate equals $-2 \cdot 10^7\,\mathrm{V\,s^{-1}}$. The duration of T_{p2} was held at a brief 200 ns. The configuration of the converter is succinctly summarized in Table 8.1.

Moreover, when operating at low voltages, the parasitic capacitance of D_1 can reach the magnitude of hundreds of picofarads, making it comparable to C_{sh1}. Based on its datasheet, this parasitic capacitance is estimated to be 500 pF. Consequently, the total value of C_{sh1} amounts to approximately 0.98 nF. Given that $C_{\mathrm{sub}} = 1.08\,\mathrm{nF}$ and $C_{\mathrm{t}} = 2.35\,\mathrm{nF}$, the overall equivalent capacitance contributed by the plasma mockup totals approximately 2.86 nF. Incorporating the parasitic capacitance of 2.6 nF introduced by the converter board, the combined C_{eq} is approximately 5.46 nF.

Given the known filter inductance of 6.03 µH, the impedance and natural frequency can be obtained, resulting in 33 Ω and 5.5 rad $\mathrm{s^{-1}}$, respectively. Utilizing these values, the trajectory control parameters can be computed according to the guidelines provided in Chapter 6, and these values are presented in Table 8.2. The calculated values for T_{r}, T_{p1}, and T_{f} serve as a initial control settings. These settings are then further refined through online adjustments to achieve the desired waveforms. The optimized time values are also included in Table 8.2, and the resulting waveforms are illustrated in Figure 8.11. Throughout this scenario, the switched damping remains bypassed consistently. All the fine-tuned time settings are smaller than the

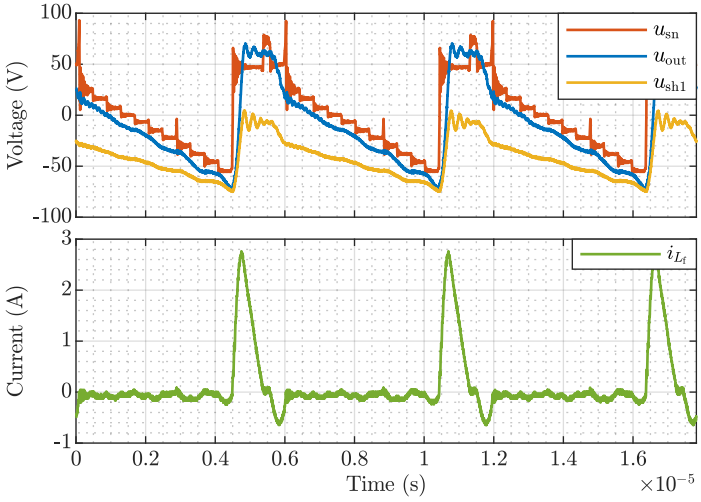


Figure 8.11 Measured waveforms of u_{sn}, u_{out}, u_{sh1}, and $i_{L_{\text{f}}}$ with the switched damping circuit bypassed.

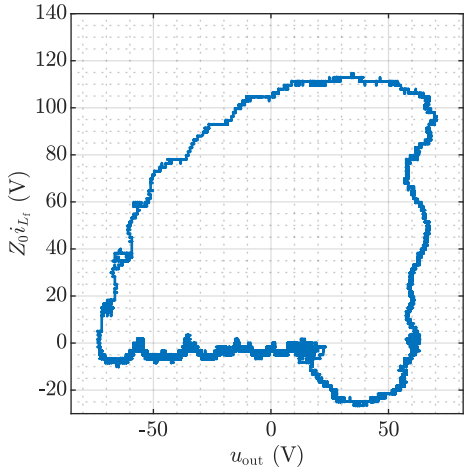


Figure 8.12 The state-plane diagram of u_{out} and i_L with the switched damping circuit bypassed.

calculated values, which implies that C_{eq} has been reduced at this voltage compared to its value recorded at zero voltage.

As seen from Figure 8.11, the measured waveform of u_{sn} generally aligns with expectations when compared to the simulated waveform Figure 6.4, which delivers a series of sequentially decreasing voltage levels during the charge phase, wherein V_{step} and T_{step} remain constant. However, two instances of voltage spikes emerge during the charge phase, coinciding with the dead times at T_4 and T_{11}. These spikes occur as the T-type submodule transitions to a lower output voltage, as depicted in Figure 5.7. The reason is that all H-bridge submodules are commutating to a higher output voltage at the same time. Since the switches in the H-bridge submodule are faster, a high voltage spike can be obtained until the T-type converter commutates to a lower output voltage. The effect of these two voltage spikes on the output is minor due to the filter inductor.

During the charge phase, the voltage slope of u_{out} is smoothed by the filter inductor. The measured slope rate approximates $-1.92 \cdot 10^7\,\mathrm{V\,s^{-1}}$, which is about 4 % higher than the theoretical value. This deviation is caused by the blocking capacitor C_{b}, which acts as a capacitive voltage divider together with other load capacitors and shares a small portion of the voltage slope. Since C_{b} is much larger than other capacitances, this effect is minor. As there is no active current source in the plasma mockup, the "substrate surface potential" C_{sh1} also decreases linearly during the charge phase, instead of keeping quasi-constant. The measured slope rate of u_{sh1} is about $-9.7 \cdot 10^6\,\mathrm{V\,s^{-1}}$, approximately half of the output voltage slope. It confirms that D_1 adds a parasitic capacitance and forms an equivalent sheath capacitance of approximately 1 nF, thus being equal to C_{sub} and attaining only half of the output voltage slope.

Regarding the measured waveform of $i_{L_{\mathrm{f}}}$, it conforms to anticipated patterns. It rises to its maximum value $i_{L_{\mathrm{f,max}}}$ during the discharge phase, and subsequently falls to zero during the post-discharge phase. When restarting the charge phase, it reaches its minimum value $i_{L_{\mathrm{f,min}}}$ and then resonates to the correct dc value after entering the charge phase. However, both $i_{L_{\mathrm{f,max}}}$ and $-i_{L_{\mathrm{f,min}}}$ are smaller than the calculated values, as shown in Table 8.2. It is because the real impedance is higher due to a decreased value of C_{eq}.

The reduction in the value of C_{eq} can be effectively calibrated within this process. During the charge phase, the measured average value of $i_{L_{\mathrm{f}}}$ is about $-0.067\,\mathrm{A}$, which is equal to i_{out} since the clamping diode $\mathrm{D_c}$ is blocking. Therefore, the C_{eq} during the charge phase can be approximated by

$$C_{\mathrm{eq}} = \frac{i_{\mathrm{out}}}{\frac{\mathrm{d}u_{\mathrm{out}}}{\mathrm{d}t}} \approx 3.5\,\mathrm{nF}, \tag{8.1}$$

which has been observably reduced compared to the value measured at zero voltage. If this calibrated capacitance value is reused for trajectory control, the calculated control times can offer heightened accuracy and a closer alignment with the fine-tuned values, as shown in Table 8.2. This outcome forms a solid foundation for potential closed-loop control endeavors in future research. If real-time monitoring of nonlinear capacitances becomes feasible, trajectory control stands to achieve even higher accuracy.

If the stray inductance L_s in the output loop is neglected, u_t can be approximated by u_out. Therefore, a state-plane diagram can be constructed by using the measured waveform of u_out and i_{L_f}, in conjunction with the calibrated impedance. This construction is depicted in Figure 8.12, which notably aligns well with the introduced calculated and simulated diagram in Chapter 6.

Switched damping

To further underscore the efficacy of the switched damping circuit, the identical fine-tuned time settings were used while the switched damping was enabled since the beginning of the charge phase. Therefore, the damping resistor was connected in the loop throughout the entire charge phase. The resulting waveforms and state-plane diagram are illustrated in Figure 8.13 and Figure 8.14, respectively.

As evident from the figures, during the charge phase, with the switched damping, the circuit enters the steady state faster, and the magnitude of the resonance has been successfully reduced. Since both the magnitude of resonance and output current during the charge phase are much lower compared to their values during the discharge phase, the power dissipation on the damping resistor is low as well.

This example implementation shows a well-defined trajectory control that can almost completely dampen the resonance by adjusting the values and time durations of V_r and V_f. However, as introduced in Chapter 6, if the required V_s is lower than $-3V_\mathrm{step} - \sqrt{\left(r_1^2 - Z_0^2 I_\mathrm{c}^2\right)}$, complete damping of resonance via trajectory control becomes unattainable. Under such circumstances, the voltage levels below $V_\mathrm{dsn} - 3V_\mathrm{step}$ should be used to obtain a larger voltage drop during the voltage falling edge, and the switched damping circuit should be enabled since the beginning of the charge phase. This operation reduces the available number of voltage levels for the charge phase and increases the power dissipation on the damping resistor.

An example implementation was conducted using the converter configurations and control parameters listed in Table 8.3. The measured waveforms are depicted in Figure 8.15. As can be seen, the voltage drop of the voltage falling edge becomes larger, while a large resonance is introduced during the charge phase, which is slowly and passively dampened by the switched damping circuit.

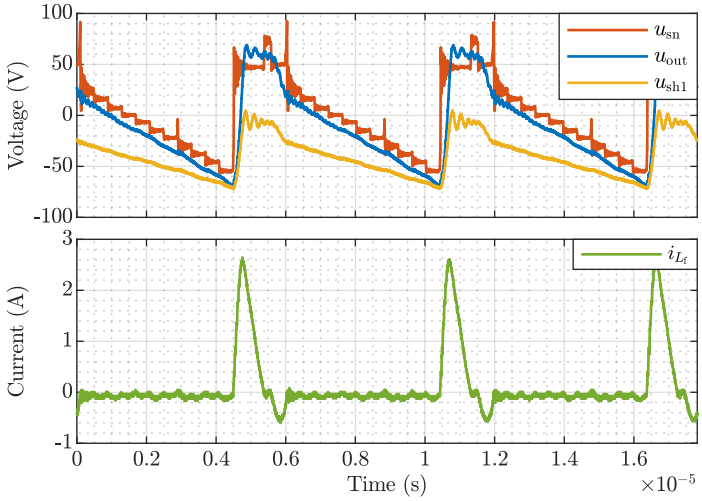


Figure 8.13 Measured waveforms with the switched damping enabled since the beginning of the charge phase.

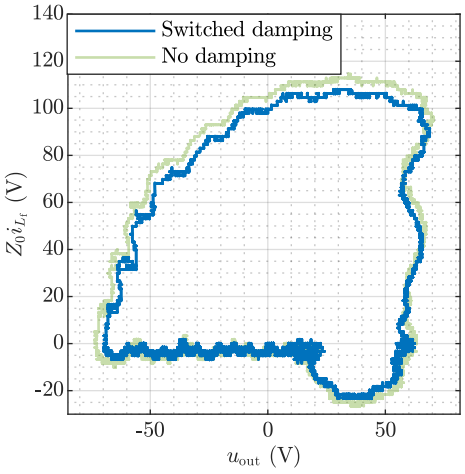


Figure 8.14 The state-plane diagram of u_{out} and i_L with the switched damping enabled since the beginning of the charge phase. The case with no damping is shown as a comparison.

Table 8.3 The converter configuration and control parameters for functional test with the switched damping circuit.

Parameter	Value	Unit	Parameter	Value	Unit
V_{dsn}	130	V	V_{step}	8	V
V_{rsn}	106	V	V_{fsn}	106	V
T_{step}	400	ns	$\dot{u}_{\mathrm{out}}$	$-2 \cdot 10^7$	$\mathrm{V\,s^{-1}}$
T_{r}	280	ns	T_{p1}	720	ns
T_{p2}	400	ns	T_{f}	390	ns

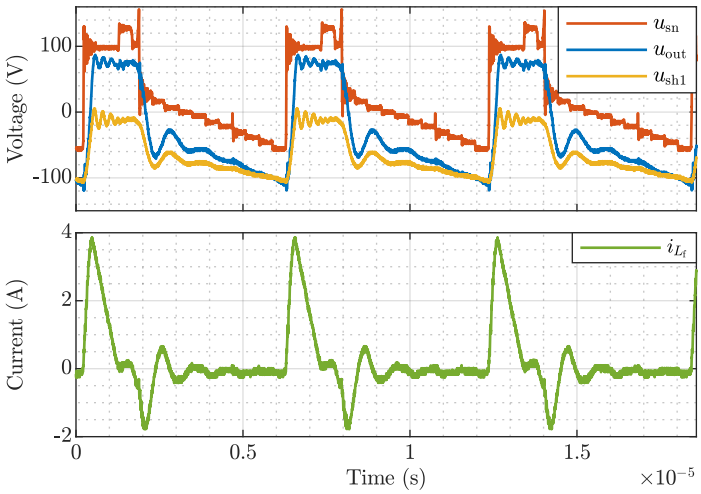


Figure 8.15 Measured waveforms with the switched damping enabled since the beginning of the charge phase.

Besides, during the charge phase, the voltage slope rate of u_{sh1} becomes closer to that of u_{out}, since the operating voltage in this case is increased, and the parasitic capacitance introduced by D_1 is significantly reduced.

8.2.2 Stress test

High voltage

In this section, a stress test was conducted to assess the maximum output voltage of the bias converter using the converter configuration and control parameters listed in Table 8.4. Notably, for this test, $V_{\mathrm{fsn}} = V_{\mathrm{dsn}} - 3V_{\mathrm{step}}$. The measured waveforms and the state-plane diagram are illustrated in Figure 8.16 and Figure 8.17, respectively.

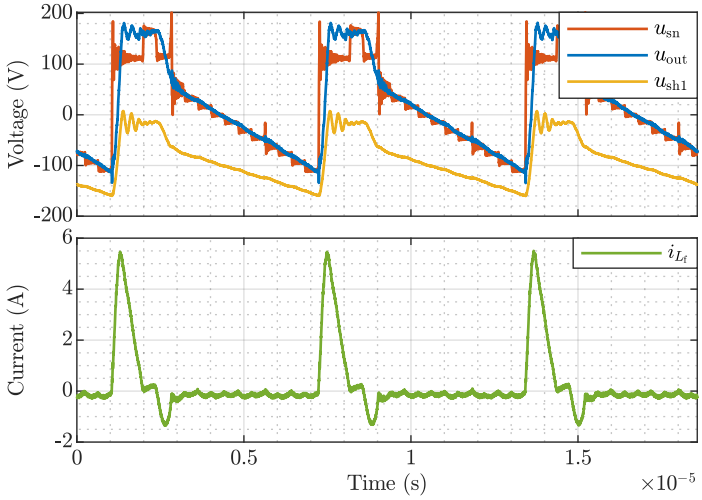


Figure 8.16 Measured waveforms with the switched damping enabled since the beginning of the charge phase.

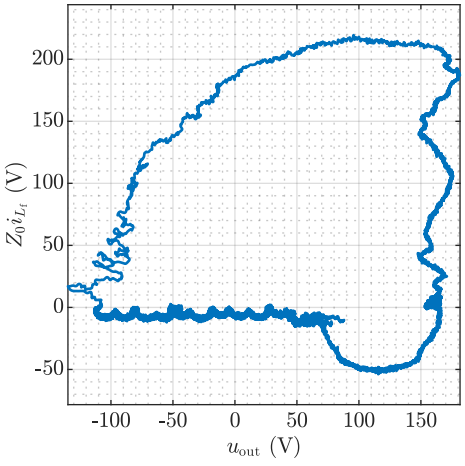


Figure 8.17 The state-plane diagram of u_{out} and i_L with the switched damping enabled since the beginning of the charge phase.

Table 8.4 The converter configuration and control parameters for high-voltage stress test

Parameter	Value	Unit	Parameter	Value	Unit
V_{dsn}	168	V	V_{step}	16	V
V_{rsn}	120	V	V_{fsn}	120	V
T_{step}	400	ns	$\dot{u}_{\mathrm{out}}$	$-4 \cdot 10^7$	$\mathrm{V\,s^{-1}}$
T_{r}	250	ns	T_{p1}	690	ns
T_{p2}	400	ns	T_{f}	450	ns

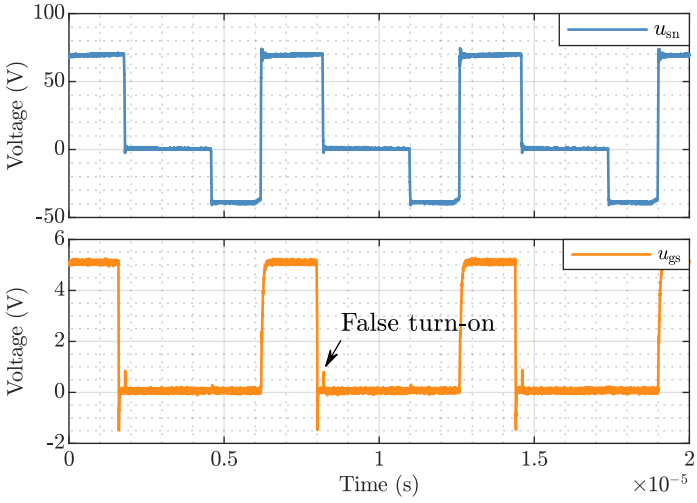


Figure 8.18 Measured switched-node voltage u_{sn} and the gate-source voltage u_{gs} of the top switch in the T-type submodule.

As can be seen, the trajectory control was implemented, resulting in the attainment of a peak-to-peak voltage of roughly 320 V.

The dc-link voltage of the T-type submodule is 232 V in this case. Further increasing this voltage causes breakdown to the switches in this submodule. The possible reasons for switch failures have also been investigated.

Figure 8.18 depicts the measured switched-node voltage and the gate-source voltage of the top switch in the T-type submodule. In this case, the T-type converter was supplied with 70 V and -40 V. The plasma mockup was disconnected with the converter, so there was no current. Therefore, the influence of the stray inductances on the switching transients was negligible. Measurement of the switched-node

voltage was facilitated using a LeCroy-manufactured high-voltage passive probe, specifically the PPE4kV model. In parallel, the gate-source voltage was measured utilizing an IsoVu isolated probe from Tektronix.

The waveform of u_{gs} exposes a positive voltage spike induced by the high-voltage falling slew rate when the switch should remain off. In the GaN transistor, the gate-source voltage interacts with the switched-node voltage via the reverse transfer capacitance. A high voltage slew rate can generate a large current in the reverse transfer capacitance, which flows into the gate driver and causes a positive voltage due to the impedance of the turn-off path. In this measurement, the falling slew rate was quantified at $5.65\,\mathrm{V\,ns^{-1}}$, leading to a voltage spike of 0.95 V on u_{gs}. Increasing the supply voltages can further increase the slew rate and subsequently yield a higher voltage spike. Given that the turn-on threshold voltage of the GaN transistor is remarkably low ($V_{\mathrm{th}} \approx 1.6\,\mathrm{V}$), increasing supply voltage can trigger false turn-on. This, in turn, prompts shoot-through events and break down the switching components. Regrettably, this issue extends to other switches and submodules, and the incorporation of increased dead-time fails to provide a remedy.

Efforts have been made to address this problem. A snubber capacitance of 1 nF has been added to the gate-source of the switches, and a turn-off path with smaller R_{off} and better turn-off diode has been established. However, the improvement was very limited. Therefore, the issue is attributed to the gate driver, which, according to its datasheet, can exhibit an internal turn-off impedance as high as $0.64\,\Omega$. As such, future resolutions could involve the adoption of an enhanced gate driver or the implementation of a negative turn-off voltage to effectively grapple with this challenge.

The slope rate of u_{sh1} during the charge phase is about $-2.03 \cdot 10^7\,\mathrm{V\,s^{-1}}$. In superposition with the linear slope, it has a voltage ripple below 4 V. This outcome aligns with the predefined design goal that stipulates $\Delta u_{\mathrm{sh1}} \leq 10\,\mathrm{V}$.

High frequency

As introduced in Chapter 7, $T_{\mathrm{step}} = 400\,\mathrm{ns}$ was selected based on the worst-case estimation. However, if the voltage or current is lower than the worst case, there exists a potential opportunity to further reduce T_{step}. In this section, a stress test was conducted to examine the minimal attainable T_{step} for this bias converter using the converter configuration and control parameters listed in Table 8.5. The configuration is almost the same with the one depicted in Table 8.5, except that T_{step} is merely 25 % of the previous value. Consequently, the repetition frequency corresponding to this configuration approximates 400 kHz, implying that the switches within submodule M3 undergo switching at a frequency of approximately 1.6 MHz.

The measured waveforms and the state-plane diagram are illustrated in Figure 8.19

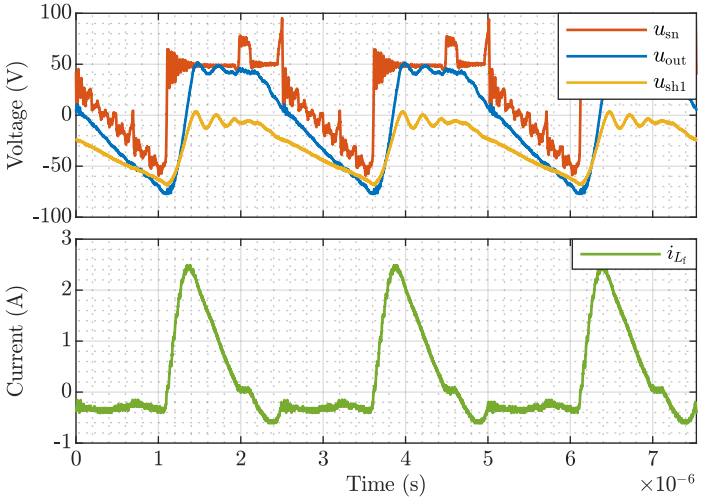


Figure 8.19 Measured waveforms with the switched damping enabled since the beginning of the charge phase.

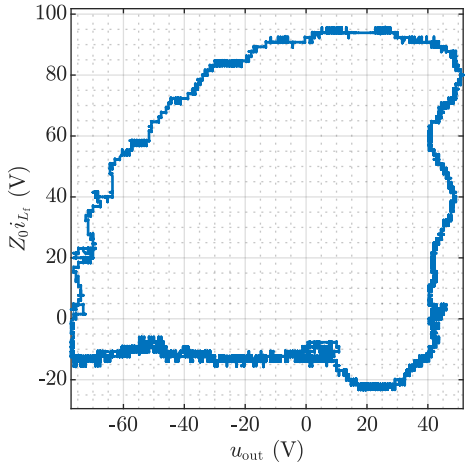


Figure 8.20 The state-plane diagram of u_{out} and i_L with the switched damping enabled since the beginning of the charge phase.

Table 8.5 The converter configuration and control parameters for high-frequency stress test

Parameter	Value	Unit	Parameter	Value	Unit
V_{dsn}	76	V	V_{step}	8	V
V_{rsn}	52	V	V_{fsn}	52	V
T_{step}	100	ns	$\dot{u}_{\mathrm{out}}$	$-8 \cdot 10^7$	$\mathrm{V\,s^{-1}}$
T_{r}	250	ns	T_{p1}	640	ns
T_{p2}	140	ns	T_{f}	100	ns

and Figure 8.20, respectively. The bias converter continues to function in alignment with expectations. As T_{step} becomes smaller, the frequency of the voltage ripple of u_{sh1} gets higher, thereby augmenting the efficacy of the LC filter. Therefore, the voltage ripple is mitigated at the same V_{step}. Notably, T_{step} lower than 100 ns is hard to achieve, since it becomes comparable to the dead-time.

8.3 Conclusion

Experiments have been conducted and demonstrated in this chapter to validate the converter concept and proposed trajectory control. In the experimental setup, a converter board based on the proposed bias converter topology was designed following the top-down design methodology. A switched damping board was developed and incorporated in the loop for waveform improvement. The converter system was controlled by an FPGA in a dSPACE MicroLabBox connected with an interface board. Isolated supplies with ultra-low parasitic capacitance were used to power the cascaded H-bridge submodules. The entire system was implemented on a plasma mockup designed to emulate the electrical response in plasma processing.

The measurement results have confirmed that the proposed bias converter topology can generate the multilevel tailored waveform, which can be further filtered to the tailored waveform by an extra filter inductor. The trajectory control works as intended, and the switched damping circuit can be used to passively dampen the undesired resonance during the charge phase with very little power dissipation. Moreover, same experimental studies should be repeated on a real plasma reactor in future research.

The converter demonstrated robust performance at low voltages. However, the switching components experience breakdown at high voltages. It is caused by the false turn-on introduced by the high voltage falling slew rate. It is suggested to solve this problem in the future by using a gate driver with smaller turn-off impedance or

adopting a negative turn-off voltage for higher safety margin.

In practice, the equivalent load capacitances can be variant under different operating conditions. Therefore, real-time measurements of the capacitances are recommended to enable closed-loop trajectory control in the future. During the charge phase, the equivalent capacitance can be derived by measuring the current and output voltage slope rate. During the voltage rising and falling edge, the load capacitance might be deduced by measuring the resonant frequency or period of the electrical waveforms.

Chapter 9 Closing

This chapter presents the conclusions of the thesis, provides recommendations for the future research, and summarizes the scientific contributions. Moreover, publications and patent applications are listed in this chapter.

9.1 Conclusions

In this thesis, the fundamentals of plasma physics and plasma processing are introduced. A mathematical description of the plasma sheath is derived, revealing similarities between the plasma sheath and a diode and providing a basis for its equivalent electric circuit modeling. Furthermore, it is shown that like a diode, the plasma sheath can be further negatively biased to increase the voltage across the sheath to accelerate the ions to higher energies. This biasing technique is commonly used in plasma processing for semiconductor manufacturing, where accurate and uniform ion energy is required for atomic-scale material processing.

Tailored waveform biasing has shown promising results for achieving a narrow and single-peak ion energy distribution in a wide range of applications involving the most common dielectric wafers. Traditionally, linear amplifiers are used to deliver tailored waveforms, but they prove to be energy-inefficient and require matching networks. Energy-efficient alternatives, known as switched-mode power converters, have been identified, but their design, simulation, and optimization necessitate an equivalent electric circuit model of plasma processing.

This thesis introduces an equivalent electric circuit model suitable for tailored waveform biasing. The model represents the plasma with a resistor of switched values and introduces an additional sheath compared to the traditional models, known as the table sheath, to enable the discharge of all capacitors to zero voltage. The tailored waveform biasing is divided into three distinct phases within a fundamental period: the charge phase, the discharge phase, and the post-discharge phase. Each phase is analyzed individually. Moreover, this model indicates that the negative portion of the falling edge of the discharge voltage pulse determines the ion energy, while the voltage slope rate during the charge phase determines the width of the ion energy distribution. By employing this model, plasma processing can be simulated using standard circuit simulation software, accurately reproducing both electrical responses and ion energy distributions.

Based on the EEC model, an auto-tuning method is developed to automatically determine the optimal slope rate. This method relies solely on voltage and current measurements on the converter side, making it nonintrusive to the plasma processing. It calculates effective capacitances at different voltage slopes and identifies the minimum effective capacitance corresponding to the optimal slope rate. Experimental results demonstrate the effectiveness and accuracy of the auto-tuning method. Additionally, the thesis explores the impact of the retarding field energy analyser, which introduces an equivalent sheath capacitance and reduces the ion current to the substrate. Consequently, a reduced negative slope rate is required compared to the actual optimal value.

A parameter identification method is introduced to extract the parameters of the equivalent electric circuit model. By applying bias waveforms with various slope rates and measuring resultant current waveforms, all the components, including the capacitances and currents, can be linearized within a reasonable operating range. Their parameters can be obtained through simple mathematical manipulation of the electrical waveforms. Once obtained, these parameters can be used to simulate plasma processing in the circuit model. The alignment between circuit simulations and experimental measurements validates the effectiveness and accuracy of the identification method.

This thesis evaluates and compares two existing bias converter concepts: the voltage source converter and the hybrid source converter. Neither of these concepts is suitable for scaling to higher voltages. Consequently, a multilevel tailored waveform concept is proposed as a solution. This concept approximates the desired tailored waveform while adding minor voltage ripples to the substrate surface. By incorporating an extra filter inductor, the voltage ripples can be reduced, enabling the achievement of the desired ion energy distribution. The thesis derives the minimum filter inductance required for a given specification on the voltage ripple and ion energy distribution. It presents a generic multilevel bias converter topology based

on asymmetrical cascaded H-bridge converters.

The LC circuit formed by the inductances and load capacitances can cause undesired resonance when applied with a voltage pulse. To address this issue, the thesis proposes a trajectory control method to actively dampen the resonances. Intermediate voltage levels are applied to the switched-node, and their time durations can be accurately determined through state-plane analysis. This trajectory control enables the generation of smooth tailored waveforms. Additionally, a switched damping circuit can be activated at the appropriate time to further passively dampen undesired resonances caused by parasitic effects and modeling errors.

Furthermore, this thesis presents a top-down design methodology for selecting the appropriate design parameters for the proposed bias converter in plasma processing applications, based on a given specification of the ion energy distribution and plasma reactor parameters. Determining T_{step} is critical in this design approach, as the key parameters of the bias converter depend on it. By using the introduced switching transient model, the switching performance under various V_{step} values can be assessed, and all feasible design selections can be collected. Among the viable design selections, trade-offs can be made to achieve a balance between the pulse duty cycle and switching loss.

A bias converter prototype is built based on the proposed multilevel topology and the top-down design methodology. The prototype incorporates the proposed trajectory control for experimental verification. The converter is validated using a plasma mockup designed to emulate the electrical response of a plasma reactor. The hardware and software design of the experimental setup are discussed, and comprehensive measurements are conducted. The results demonstrate that the proposed trajectory control functions as intended, enabling the bias converter to deliver smooth tailored waveforms. However, it should be noted that the achieved output voltage falls short of the target value, which could be attributed to a false turn-on in the T-type converter. Furthermore, it is worth considering that in practice, the value of T_{step} can be further reduced, as the top-down design methodology employs a conservative constraint.

9.2 Recommendations

A systematic research effort has been conducted in this thesis, covering various aspects such as physics theory, circuit modeling, waveform optimization, converter topology derivation, control strategy, and converter design and implementation. The analysis and methodologies presented in this thesis provide a solid foundation for designing, implementing, and controlling power electronics systems for similar

applications, with an expectation of achieving high performance. However, since this study is still in its early stages within this cutting-edge technology, further research is recommended in several additional areas:

• The proposed equivalent electric circuit model reveals the existence of a table sheath formed between the plasma and the exposed part of the reactor table. However, the values of its sheath capacitance and current are neglected in both circuit simulation and parameter identification. Furthermore, in order to capture the nonlinear behavior of the components more accurately, it is necessary to consider all component parameters in the model and employ nonlinear values for certain parameters.

• The EEC model developed for tailored waveform biasing is also expected to be compatible with other biasing techniques, which requires experimental validations in the future. Furthermore, with the model, the plasma ion energy distribution can be simulated at the circuit level, enabling bias waveform optimization to tailor specific ion energy distribution for various applications.

• The auto-tuning method developed in this thesis is currently implemented offline. In future research, it is recommended to implement it in real-time control, which necessitates high-accuracy and high-bandwidth voltage and current measurements. Moreover, achieving a finer gradient of the voltage slope is desirable to enhance accuracy, which calls for higher resolution in the bias converter. Furthermore, additional experimental validations using various plasma processing setups are demanded, and direct measurement of the substrate surface potential can provide further insights into the process.

• The proposed bias converter topology includes a T-type converter and a series of cascaded H-bridges with a binary configuration. The redundant switching states in this configuration can potentially be utilized for voltage balancing. In this special application, considering the highly complex load, further investigation is required to determine the feasibility of voltage balancing using these redundant states. In cases where voltage balancing is not achievable, the trinary configuration should be explored as it allows for the highest number of voltage levels with the same number of submodules. Additionally, other topologies, such as asymmetrical neutral-point-clamped converter, can serve as alternatives, eliminating the need for isolated supplies.

• The use of isolated dc supplies for the cascaded H-bridges in the proposed bias converter topology may pose challenges when scaling the topology to include more submodules and higher voltage levels, since the parasitic capacitances of the isolated supplies can increase the switching losses and times. Therefore, in future research, accurate determination of the output power of these isolated supplies is necessary to optimize their hardware design and minimize parasitic capacitances.

• The proposed bias converter topology features a flexible voltage level V_{dsn} used for the discharge voltage pulse, which does not necessarily need to be a multiple of V_{step}. This flexibility in voltage levels allows for greater control over ion energy. Future research can explore the addition of more flexible voltage levels, particularly during the rising and falling edges of the voltage, which can expedite the transient response and achieve a smaller pulse duty cycle. These flexible levels can be implemented using additional cascaded H-bridges.

• The trajectory control developed in this thesis has been implemented in an open-loop manner. It relies on accurate values of inductance and capacitance to determine switching sequences and their durations. However, modeling errors and parasitic factors in practical designs can lead to variations and nonlinearities in circuit parameters, particularly capacitances, thereby introducing disturbances to the control system and generating undesired resonances. Future research can focus on developing closed-loop trajectory control to reject disturbances and further enhance the accuracy of the method. Closed-loop control necessitates real-time measurement of all capacitances. Since the filter inductance is typically known and relatively constant, the capacitances can be extracted by measuring the resonant frequency.

• This thesis presents a top-down design methodology for making proper design selections for the bias converter. In the given example, all the submodules use the same transistors. The calculated results indicate that the T-type converter is the bottleneck of reducing T_{step} further. Further research can explore the use of different transistors for each submodule to optimize the design and improve performance.

• The converter prototype and its trajectory control have been validated through experiments using a plasma mockup. However, the plasma mockup does not have an active current source, making it unable to maintain a quasi-dc substrate surface potential during the charge phase. It is highly recommended to validate the prototype and trajectory control on a real plasma reactor. Additionally, improving the plasma mockup by incorporating a dc current source capable of handling fast voltage changes over it can further enhance its accuracy and effectiveness.

9.3 Scientific contributions

The main contributions of this thesis can be summarized as follows:

• An EEC model that bridges the gap between plasma processing and bias converter design.
The limitations of the traditional EEC models have been analyzed, and these traditional models have been proven unsuitable for tailored waveform biasing. The improved EEC model proposed in this thesis enables plasma simulation at the circuit

level with significantly reduced computational effort. Both the electrical waveforms and IEDs can be simulated using circuit simulation. It also provides an electrically equivalent description of plasma processing and offers insights into the process from an electrical engineering perspective.

• A proprietary auto-tuning method that automatically detects the optimal slope rate.
The traditional manual-tuning method utilizes an RFEA to find the optimal slope rate, which necessitates repetitive measurements to reach the target once any of the operating conditions is changed. Additionally, the RFEA measurement is interactive with the plasma and can cause inaccuracies. The proposed auto-tuning method utilizes the voltage and current measurements on the converter side to derive the minimum value of the effective capacitance, which equivalently leads to the optimal slope rate. It is advantageously nonintrusive to the plasma process. This method has been patented in multiple countries.

• A parameter identification method to extract the EEC model parameters in plasma processing.
The plasma parameters can be highly nonlinear, which can significantly increase the complexity of the model. The proposed identification method linearizes all the parameters within a reasonable range of operating conditions. The method is entirely based on nonintrusive electrical measurements, which includes the voltage and current waveforms on the converter side. Substituting the identified parameters into the EEC model enables simulating the electrical waveforms and IEDs through circuit simulation, which well aligns with the experiments.

• A generic multilevel bias converter topology to generate the multilevel tailored waveform.
The existing bias converters can be categorized into two classes: the voltage source converter and the hybrid source converter, neither of which is suitable for scaling to higher voltages. The proposed multilevel tailored waveform concept allows the multilevel converters to be used in this application. It uses monotonically decreasing voltage levels to approximate the negative voltage slope in the tailored waveform. Adding an extra filter inductor can smooth the voltage waveforms, reduce the voltage ripple on the substrate surface to a value smaller than the voltage step, and obtain a narrower IED. The mathematical relation between the filter inductance and the voltage ripple has also been derived. This generic topology has been patented.

• A trajectory control method to smoothly generate the tailored waveform.
The LC circuit formed by the inductances and load capacitances can trigger severe resonances during the voltage rising and falling edge. The proposed trajectory control method uses the intermediate voltage levels that are provided by the proposed multilevel converter during the voltage rising and falling to actively dampen the

undesired resonances. With the state-plane analysis, the time durations for each voltage levels can be accurately determined.

• **A top-down design methodology to make proper design selections for a given specification.**
The top-down design methodology for the multilevel bias converter indicates that the converter dimensions are highly determined by the selection of T_{step}, which is limited by the capability of the switching devices. It builds the mathematical relations of the crucial converter parameters with T_{step}. A switching transient model is used to evaluate the semiconductor performance under various operating conditions, with which and all the feasible designs can be collected.

• **Experimental verification of the introduced modeling, control strategy, topology, and design methodology.**
A multilevel bias converter prototype type is built according to the top-down design methodology and implemented with the proposed trajectory control for experimental verification. Various measurements are conducted under different operating conditions, and the results confirm the proposed concepts.

9.4 Publications

9.4.1 Journal publications

• **Q. Yu**, E. Lemmen, C. G. E. Wijnands, and B. J. D. Vermulst, "Output Spectrum Modeling of an H-Bridge Inverter With Dead-Time Based on Switching Mode Analysis," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11344–11356, Oct. 2021.

• **Q. Yu**, E. Lemmen, B. Vermulst, A. J. M. Mackus, W. M. M. (Erwin) Kessels, and K. Wijnands, "Equivalent electric circuit model of accurate ion energy control with tailored waveform biasing," *Plasma Sources Science and Technology*, vol. 31, no. 3, p. 035012, Mar. 2022.

9.4.2 Conference publications

• **Q. Yu**, R. Baeten, E. Lemmen, B. Vermulst, and K. Wijnands, "A 1 MHz Wide Bandgap Power Amplifier for High-Precision Applications," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*. IEEE, Sep. 2019, pp. P.1-P.7.

• **Q. Yu**, E. Lemmen, and B. Vermulst, "A Numerical Method for Calculating the Output Spectrum of an H-Bridge Inverter with Dead-time Based on Switching Mode

Analysis," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE).* IEEE, Sep. 2019, pp. 2245-2251.

• **Q. Yu**, E. Lemmen, K. Wijnands, and B. Vermulst, "Exploring the Boundaries and Effects of the Discontinuous Conduction Mode in H-Bridge Inverter with Dead-time," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe).* IEEE, Sep. 2020, pp. P.1-P.8.

• **Q. Yu**, E. Lemmen, K. Wijnands, and B. Vermulst, "A Switched-Mode Power Amplifier for Ion Energy Control In Plasma Etching," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe).* IEEE, Sep. 2020, pp. P.1-P.8.

• **Q. Yu**, E. Lemmen, C. G. E. Wijnands, and B. Vermulst, "Model and Verification of a Plasma Etching Reactor with a Switched-Mode Power Converter," in *12th International Conference on Electrical and Electromechanical Energy Conversion (ECCE Asia 2021).* IEEE, May 2021, pp. 578-573.

• **Q. Yu**, E. Lemmen, K. Wijnands, and B. Vermulst, "Auto-Tuning Control of a Switched-Mode Power Converter for Tailored Pulse-Shape Biased Plasma Etching Applications," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE).* IEEE, Oct. 2021, pp. 5949-5954.

• **Q. Yu**, E. Lemmen, K. Wijnands, and B. Vermulst, "Accurate Ion Energy Control in Plasma Processing by Switched-Mode Power Converter," in *2022 International Power Electronics Conference (IPEC-Himeji 2022-ECCE Asia).* IEEE, May 2022, pp. 498-505.

9.4.3 Patents

• **Q. Yu**, E. Lemmen, and B. J. D. Vermulst, "Determining an optimal ion energy for plasma processing of a dielectric substrate," WO Patent WO2 021 064 110A1, Apr., 2021.

• **Q. Yu**, E. Lemmen, and B. J. D. Vermulst, "Voltage waveform generator for ion energy control in plasma processing," Patent, submitted.

APPENDIX A

Custom switched-mode power converter

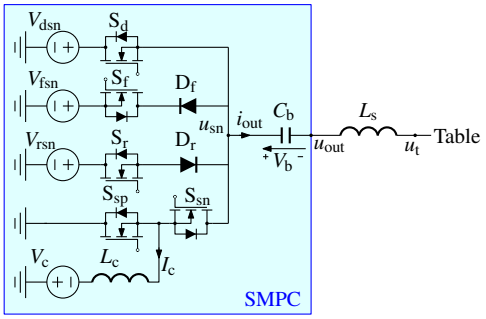


Figure A.1 The topology of the custom SMPC.

In Section 2.2 and Section 3.3, a custom SMPC was utilized for the experiments. The topology of this SMPC is illustrated in Figure A.1. The converter comprises four controllable dc voltage supplies V_{dsn}, V_{fsn}, V_{rsn}, and V_c. V_{dsn} generates the discharge voltage V_d at the output.

L_s represents the stray inductance in the converter connection loop. As shown in Figure 2.5, the plasma reactor is a capacitive load and forms an LC resonant circuit with L_s, which can cause severe resonances when the pulse voltage rises and falls rapidly. V_{rsn} and V_{fsn} are two intermediate voltage levels at the switched-node utilized for trajectory control during the rising and falling edge of the voltage pulse. By properly adjusting the value and the conduction time of V_{rsn} and V_{fsn},

the resonance caused by the LC circuit can be suppressed, and a smooth and well-defined output voltage waveform can be obtained.

The voltage source V_c is connected with a large inductor L_c, forming an equivalent current source I_c if the inductor current ripple is neglected. The current source I_c sinks the current from the table and generates a linearly decreasing output voltage during the charge phase. By adjusting V_c, the steady-state value of I_c can be modulated accordingly. During the charge phase, I_c should be equal to $-i_{out}$.

A blocking capacitor C_b is used to couple the switched-node and the reactor table. The value of C_b should be much larger than C_t and C_{sub} so that the voltage ripple over C_b can be neglected, and the voltage over C_b is kept at V_b during the steady state. Consequently, different voltage levels at the switched-node can lead to different values at the output, given by

$$\begin{pmatrix} V_d \\ V_r \\ V_f \\ V_s \end{pmatrix} = \begin{pmatrix} V_{dsn} \\ V_{rsn} \\ V_{fsn} \\ 0 \end{pmatrix} - \begin{pmatrix} V_b \\ V_b \\ V_b \\ V_b \end{pmatrix}. \tag{A.1}$$

Based on the analysis given in Chapter 2, it is V_s that determines the ion energy. In this converter, V_s can be controlled by adjusting the blocking voltage V_b, which can be realized by adjusting the value of V_{dsn} or the pulse duty cycle.

The benefit of the blocking capacitor is not only to maintain a balanced net output charge, thus obtaining a well-defined output current, but also to enable a bipolar output voltage by using only positive dc voltage supplies, increasing the flexibility of tailoring the output voltage waveforms.

The operating principle of the converter is depicted in Figure A.2. The switching sequences of all switches should be well regulated so that the output waveform can be optimized. Due to the stray inductance L_s and the capacitances in the plasma reactor, the load of the converter can be simplified as an LC circuit with necessary simplifications. Consequently, trajectory control is used to accurately determine the switching sequences, as explained in [183] and also analyzed in Chapter 6. During different time intervals, the equivalent circuit of the converter is shown in Figure A.3.

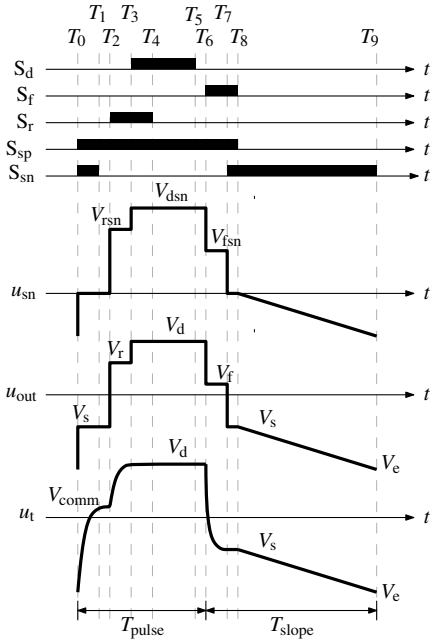
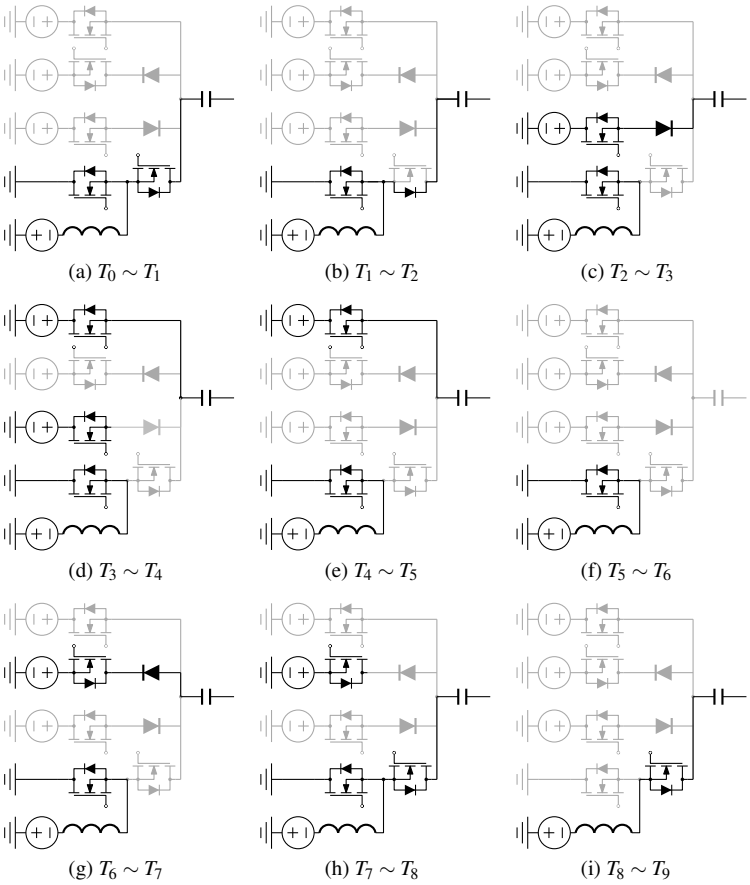


Figure A.2 The operation of the switched-mode power converter. The time duration of $T_0 \sim T_3$ and $T_5 \sim T_8$ are very short but exaggerated here for better visualization.



(a) $T_0 \sim T_1$ (b) $T_1 \sim T_2$ (c) $T_2 \sim T_3$

(d) $T_3 \sim T_4$ (e) $T_4 \sim T_5$ (f) $T_5 \sim T_6$

(g) $T_6 \sim T_7$ (h) $T_7 \sim T_8$ (i) $T_8 \sim T_9$

Figure A.3 The equivalent circuit of the switched-mode power converter during different intervals.

APPENDIX B

Linear time-invariant system during the charge phase

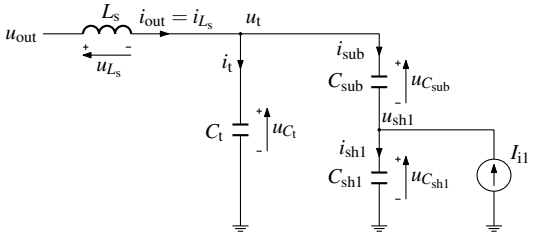


Figure B.1 The simplified equivalent circuit of the load during the charge phase.

DURING the charge phase, the equivalent circuit of the load can be simplified by neglecting R_p, I_{i2}, and C_{sh2}, as depicted in Figure B.1. If all the parameters in the equivalent circuit are considered constant, it becomes an LTI system. To derive its state-space representation, the inductor current i_{L_s} and the capacitor voltages C_t and $u_{C_{sub}}$ are chosen as the state variables, while u_{out} and I_{i1} are taken as inputs, and $u_{C_{sh1}}$ is designated as the output, since the target is to obtain a constant $u_{C_{sh1}}$. The voltage and current and their directions of all the components are depicted in Figure B.1. The state variables are determined by

$$L_s \dot{i}_{L_s} = u_{out} - u_{C_t}, \tag{B.1}$$

$$C_t \dot{u}_{C_t} = i_t, \tag{B.2}$$

and

$$C_{sub} \dot{u}_{C_{sub}} = i_{sub}, \tag{B.3}$$

respectively. Meanwhile, Kirchhoff's current law yields

$$i_{L_s} = i_t + i_{sub} \tag{B.4}$$

and

$$i_{sub} = i_{sh1} - I_{i1}. \tag{B.5}$$

Kirchhoff's voltage law gives

$$u_{C_t} = u_{C_{sub}} + u_{C_{sh1}}. \tag{B.6}$$

Combining (B.2) to (B.6) leads to

$$\dot{u}_{C_t} = \frac{C_{sh1} + C_{sub}}{C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}} i_{L_s} + \frac{C_{sub}}{C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}} I_{i1} \tag{B.7}$$

and

$$\dot{u}_{C_{sub}} = \frac{C_{sh1}}{C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}} i_{L_s} - \frac{C_t}{C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}} I_{i1}. \tag{B.8}$$

The output $\dot{u}_{C_{sh1}}$ is calculated as

$$\dot{u}_{C_{sh1}} = \frac{C_{sub}}{C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}} i_{L_s} + \frac{C_{sub} + C_t}{C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}} I_{i1}. \tag{B.9}$$

Therefore, denoting $\nu = C_{sh1}C_t + C_{sub}C_t + C_{sh1}C_{sub}$, the LTI system can be described by

$$\begin{pmatrix} \dot{i}_{L_s} \\ \dot{u}_{C_t} \\ \dot{u}_{C_{sub}} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L_s} & 0 \\ \frac{C_{sh1}+C_{sub}}{\nu} & 0 & 0 \\ \frac{C_{sh1}}{\nu} & 0 & 0 \end{pmatrix} \begin{pmatrix} i_{L_s} \\ u_{C_t} \\ u_{C_{sub}} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_s} & 0 & 0 \\ 0 & \frac{C_{sub}}{\nu} & 0 \\ 0 & -\frac{C_t}{\nu} & 0 \end{pmatrix} \begin{pmatrix} u_{out} \\ I_{i1} \\ 0 \end{pmatrix}. \tag{B.10}$$

The output can be represented by

$$\begin{pmatrix} u_{C_{sh1}} \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 \end{pmatrix} \begin{pmatrix} i_{L_s} \\ u_{C_t} \\ u_{C_{sub}} \end{pmatrix}. \tag{B.11}$$

A standard state-space representation can be described by

$$\begin{aligned} \dot{\boldsymbol{x}}(t) &= \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t) \\ \boldsymbol{y}(t) &= \boldsymbol{C}\boldsymbol{x}(t) + \boldsymbol{D}\boldsymbol{u}(t), \end{aligned} \tag{B.12}$$

where $\boldsymbol{x}(\cdot)$ is the state vector, $\boldsymbol{y}(\cdot)$ is the output vector, $\boldsymbol{u}(\cdot)$ is the input vector, and $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ are the state matrix, input matrix, output matrix, and feedthrough

matrix, respectively. Therefore, in this system, $\boldsymbol{x}(t)$, $\boldsymbol{y}(t)$, $\boldsymbol{u}(t)$, $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$, and $\boldsymbol{D}$ are equal to

$$\boldsymbol{x}(t) = \begin{pmatrix} i_{L_\mathrm{s}} \\ u_{C_\mathrm{t}} \\ u_{C_\mathrm{sub}} \end{pmatrix}, \tag{B.13}$$

$$\boldsymbol{y}(t) = \begin{pmatrix} u_{C_\mathrm{sh1}} \end{pmatrix}, \tag{B.14}$$

$$\boldsymbol{u}(t) = \begin{pmatrix} u_\mathrm{out} \\ I_\mathrm{i1} \\ 0 \end{pmatrix}, \tag{B.15}$$

$$\boldsymbol{A} = \begin{pmatrix} 0 & -\frac{1}{L_\mathrm{s}} & 0 \\ \frac{C_\mathrm{sh1}+C_\mathrm{sub}}{\nu} & 0 & 0 \\ \frac{C_\mathrm{sh1}}{\nu} & 0 & 0 \end{pmatrix}, \tag{B.16}$$

$$\boldsymbol{B} = \begin{pmatrix} \frac{1}{L_\mathrm{s}} & 0 & 0 \\ 0 & \frac{C_\mathrm{sub}}{\nu} & 0 \\ 0 & -\frac{C_\mathrm{t}}{\nu} & 0 \end{pmatrix}, \tag{B.17}$$

$$\boldsymbol{C} = \begin{pmatrix} 0 & 1 & -1 \end{pmatrix}, \tag{B.18}$$

and

$$\boldsymbol{D} = \begin{pmatrix} 0 & 0 & 0 \end{pmatrix}, \tag{B.19}$$

respectively. It is worth noting that this state-space representation is not the minimal realization, and its order might be further reduced but not necessary here [151].

APPENDIX C

Ion energy distribution

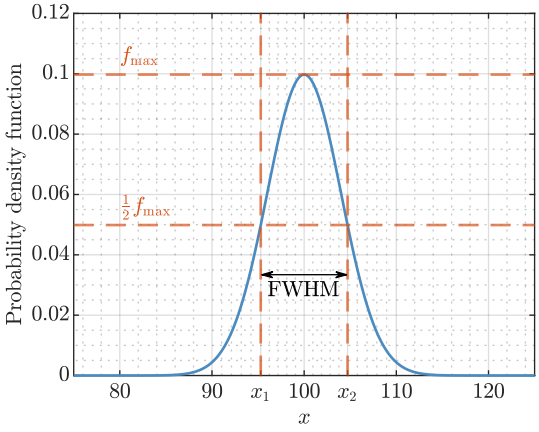


Figure C.1 Probability density function of a normal distribution, of which $\mu = 100$, and $\sigma = 4$.

In this appendix, a mathematical description of the ion energy distribution is provided, and the effect of the voltage ripple of the substrate surface on the ion energy distribution is analyzed.

If x is a random variable following a normal distribution, its can be described by

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2}, \tag{C.1}$$

where f is the probability density function, σ is the standard deviation, and μ is the mean value. An example of the probability density function of a normal distribution is shown in Figure C.1. The peak value of the probability is denoted by $f_{\max}$, and the width of the curve at $\frac{1}{2}f_{\max}$ is defined as the FWHM.

It is easy to derive that when $x = \mu$, its probability density function reaches its maximum as

$$f_{\max} = f(\mu) = \frac{1}{\sigma\sqrt{2\pi}}. \tag{C.2}$$

To calculate its FWHM, solving

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} = \frac{1}{2} f_{\max} \tag{C.3}$$

leads to $x_1 = \mu - \sqrt{2\ln 2}\sigma$ or $x_2 = \mu + \sqrt{2\ln 2}\sigma$. Therefore, the FWHM is equal to $x_2 - x_1 = 2\sqrt{2\ln 2}\sigma \approx 2.3548\sigma$. For instance, the FWHM of $f(x)$ with $\sigma = 4$ is equal to 9.42, as depicted in Figure C.1.

For a plasma confronted with floating surfaces, its ion energy E_i can be considered normally distributed. Its mean value μ is eV_p according to (1.24), and σ is depending on the plasma parameters. This is equivalent to a constant ion energy eV_p superimposed with normally distributed noise with the same σ and $\mu = 0$. This relation has been used in the simulations introduced in Section 2.2.

Apparently, if the material surface is biased with a constant voltage, such as a constant substrate surface potential V_s obtained in the plasma reactor, the mean value of the ion energy is shifted by V_s, but the FWHM remains unchanged. However, if the substrate surface has a sawtooth voltage ripple introduced by the multilevel tailored waveform, as shown in Figure 5.2, it can enlarge the FWHM. This effect is unfolded in detail in this appendix.

Consider a random variable y, which is independent of x and follows a uniform distribution described by the probability density function $g(y)$ as

$$g(y) = \begin{cases} \frac{1}{b-a}, & \text{for } a \le y \le b, \\ 0, & \text{for } y < a \text{ or } y > b, \end{cases} \tag{C.4}$$

where a and b are the lower and upper boundary of y. Interestingly, this probability density function can represent the sawtooth voltage ripple, as explained in the following context.

The sum of x and y follows a new distribution. Denoting $z = x + y$, the probability

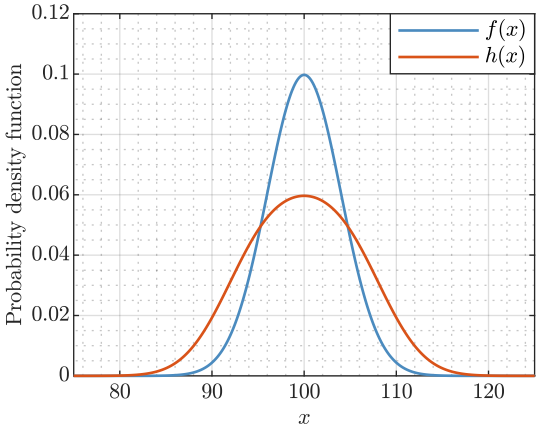


Figure C.2 Probability density function of the normal distribution and the new distribution. $\mu = 100$, $\sigma = 4$, $a = -8$, and $b = 8$.

density function of the new distribution is determined by

$$\begin{aligned} h(z) &= \int_{-\infty}^{\infty} f(z-t)g(z)\mathrm{d}t \\ &= \frac{1}{b-a}\int_{a}^{b} f(z-t)\mathrm{d}t \\ &= \frac{1}{2\,(b-a)}\left[\operatorname{erf}\left(\frac{b+\mu-z}{\sqrt{2}\sigma}\right) - \operatorname{erf}\left(\frac{a+\mu-z}{\sqrt{2}\sigma}\right)\right], \end{aligned} \tag{C.5}$$

where erf is known as the error function, as defined by

$$\operatorname{erf}(z) = \frac{2}{\sqrt{\pi}}\int_{0}^{z} \mathrm{e}^{-t^2}\mathrm{d}t. \tag{C.6}$$

Figure C.2 compares the probability density function of the new distribution with that of the original normal distribution. The parameters used for this plot are $\mu = 100$, $\sigma = 4$, $a = -8$, and $b = 8$. The FWHM of the new distribution $h(z)$ is equal to 16.46, which is an increase of 7.04 from the original normal distribution. The extent of this expansion is jointly determined by the values of σ and $b - a$.

Assuming $a = -b$, Figure C.3 shows the FWHM under different σ and $b - a$. When $b - a$ is smaller than $2\sqrt{2\ln 2}\sigma$ (the FWHM of the corresponding normal distribution), FWHM slightly increases, and it is dominated by σ. However, when $b - a$ is larger than $2\sqrt{2\ln 2}\sigma$, its effect becomes dominant. If $b - a$ is sufficiently large, then the FWHM is almost equal to $b - a$.

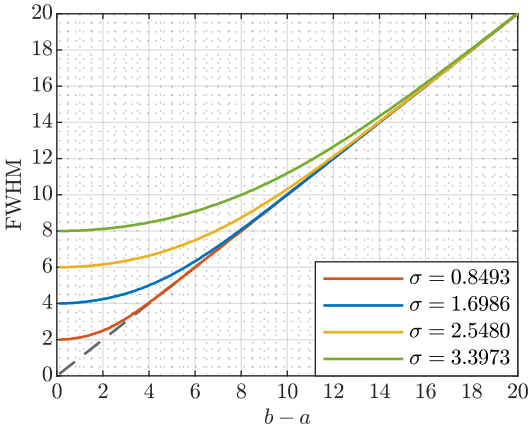


Figure C.3 FWHM of the $h(z)$ under different σ and $b-a$. $\sigma = 0.8493$, $\sigma = 1.6986$, $\sigma = 2.5480$, and $\sigma = 3.3973$ correspond to the FWHM of 2, 4, 6, and 8 for the normal distributions, respectively.

For the sawtooth voltage ripple $\hat{u}_{\mathrm{sh1}}$ on u_{sh1}, it is a periodic waveform in the time domain, which can be described as

$$\hat{u}_{\mathrm{sh1}}(t) = \hat{u}_{\mathrm{sh1}}(t - T_{\mathrm{step}}) = \frac{\Delta u_{\mathrm{sh1}}}{T_{\mathrm{step}}} t - \frac{1}{2}\Delta u_{\mathrm{sh1}}. \tag{C.7}$$

Since at any moment t, the value of the voltage ripple seen by the ions arriving at the substrate surface is equally distributed between $-\frac{1}{2}\Delta u_{\mathrm{sh1}}$ and $\frac{1}{2}\Delta u_{\mathrm{sh1}}$, this voltage ripple can be seen as a uniformly distributed noise, which is independent of other parameters. This leads to

$$g(\hat{u}_{\mathrm{sh1}}) = \begin{cases} \frac{1}{\Delta u_{\mathrm{sh1}}}, \text{ for } -\frac{1}{2}\Delta u_{\mathrm{sh1}} \leq \hat{u}_{\mathrm{sh1}} \leq \frac{1}{2}\Delta u_{\mathrm{sh1}}, \\ 0, \text{ for } -\frac{1}{2}\Delta u_{\mathrm{sh1}} < \hat{u}_{\mathrm{sh1}} \text{ or } u_{\mathrm{st}} > \frac{1}{2}\Delta u_{\mathrm{sh1}}. \end{cases} \tag{C.8}$$

Consequently, (C.5) can be used to describe the IED obtained by the multilevel tailored waveform. In Chapter 7, the maximum Δu_{sh1} is set to 10 V. According to Figure C.3, it can ensure an FWHM under 10 eV under most of the cases.

Interestingly, the influence of the sawtooth waveform on the IED is exclusively determined by the voltage magnitude, irrespective of its frequency. Furthermore, as the triangle waveform shares the same probability density function as the sawtooth waveform, it exerts an equivalent effect on the IED.

APPENDIX D

Symbols and notation

D.1 Conventions

Symbol	Description	First use
d	Differential operator	4
$f(x)$	Function f of variable x	4
$\boldsymbol{x}$	Vector variable or matrix	4
$\dot{x}$	Derivative of variable x with respect to time	48
$\hat{x}$	Ac component of periodical variable x	74
x^*	A new value of variable x	87
$x_{\max}$	Maximum value of variable x	51
$x_{\min}$	Minimum value of variable x	51
Δ	Difference	17
∇	Gradient operator	8
$\nabla\cdot$	Divergence operator	6
$\equiv$	Identical to	2
$\langle\cdot\rangle$	Average value in a period	33

D.2 Global Symbols (Latin)

Symbol	Unit	Description	First use
$\boldsymbol{a}$	$\mathrm{m\,s^{-2}}$	Acceleration	5
A	-	Atom A	2
A^*	-	Atom in excited state	3
AB	-	Molecule	3
A_{cu}	$\mathrm{m^2}$	Copper area	111
A_{IED}	$\mathrm{A\,eV^{-1}}$	Peak of the IED	54
A_{sh1}	V	Harmonic component of u_{sh1}	73
B	-	Atom B	3
C	F	Capacitance	86
C_{b}	F	Blocking capacitance	25
C_{ds}	F	Switch drain-source capacitance	106
$C_{\mathrm{ds,ext}}$	F	External drain-source capacitance	107
C_{eff}	F	Effective capacitance	49
C_{eq}	F	Equivalent capacitance	60
C_{gd}	F	Switch gate-drain capacitance	106
C_{gs}	F	Switch gate-source capacitance	106
C_{iss}	F	Switch input capacitance	109
C_{oss}	F	Switch output capacitance	109
C_{rss}	F	Switch reverse transfer capacitance	109
C_{sh0}	F	Wall sheath capacitance	24
C_{sh1}	F	Substrate sheath capacitance	24
C_{sh2}	F	Table sheath capacitance	28
C_{sub}	F	Substrate capacitance	25
C_{t}	F	Table capacitance	28
d_{sh}	m	Sheath thickness	11
$\boldsymbol{D}$	$\mathrm{C\,m^{-2}}$	Electric displacement field	5
D_{i}	-	Degree of ionization	2
D_{pulse}	-	Pulse duty cycle	33
e	-	Electron	2
E	J	Kinetic energy	4
$\boldsymbol{E}$	$\mathrm{V\,m^{-1}}$	Electric field	5
E_{i}	J or eV	Ion energy	12
E_{on}	J	Switch turn-on energy	107
E_{off}	J	Switch turn-off energy	106
E_{total}	J	Total switch energy	112
$\boldsymbol{F}$	N	Force	5

Continued on next page

Symbol	Unit	Description	First use
f_r	Hz	Resonant frequency	61
f_rep	Hz	Repetition frequency	103
f_rf	Hz	RF frequency	25
H_damp	-	Damping effect transfer function	38
H_lp	-	Low-pass filter transfer function	73
h_tim	m	Thickness of the TIM	111
i_0	A	Initial inductor current	86
I_0	A	Inductor current	106
i_C	A	Current through C	86
I_c	A	Constant current	69
i_ch	A	Channel current	106
i_d	A	Drain current	105
i_{D_1}	A	Current through D_1	30
i_{D_2}	A	Current through D_2	30
i_ds	A	Drain-source capacitor current	105
I_eff	A	Effective current	49
I_eq	A	Equivalent current	60
i_ext	A	Excitation current	86
i_gd	A	Gate-drain capacitor current	105
i_gs	A	Gate-source capacitor current	105
I_i0	A	Wall sheath current	24
I_i1	A	Substrate sheath current	24
I_i2	A	Table sheath current	28
i_L	A	Current through L	74
i_{L_f}	A	Current through L_f	73
i_{L_s}	A	Current through L_s	73
i_out	A	Output current	25
i_p	A	Current through plasmas	30
i_sh1	A	Current through C_sh1	30
i_sh2	A	Current through C_sh2	30
i_sub	A	Current through C_sub	30
i_t	A	Current through C_t	30
J_i	$\mathrm{A\,m^{-2}}$	Ion current density	11
L	H	Inductance	74
L_c	H	Current source inductor	150
L_d	H	Drain inductance	106
L_f	H	Filter inductance	74
L_s	H	Stray (source) inductance	28

Continued on next page

Symbol	Unit	Description	First use
m	kg	Mass	4
m_e	kg	Mass of electron	9
m_i	kg	Mass of the ion	7
n	m^{-3}	Charged particle density in plasma	2
n_e	m^{-3}	Electron density	2
n_i	m^{-3}	Ion density	2
n_n	m^{-3}	Neutral particle density	2
n_s	m^{-3}	Charged particle density at sheath edge	7
P	-	Normalized ion flux	38
P_{sw}	W	Total switching loss	114
Q_L	C	Charge accumulation through L	74
$Q_{C_{sh1}}$	C	Charge accumulation over C_{sh1}	75
r	V	Radius in state-plane diagram	87
r_1	V	Radius of the voltage rising edge	91
r_2	V	Radius of the voltage falling edge	92
R_b	Ω	Bleeder resistance	**??**
R_{damp}	Ω	Damping resistance	80
R_g	Ω	Gate resistance	106
R_{off}	Ω	Turn-off resistance	107
R_{on}	Ω	Turn-on resistance	107
R_p	Ω	Plasma resistance	28
R_{p1}	Ω	Plasma resistance during charge phase	126
R_{p2}	Ω	Plasma resistance during post-discharge phase	126
R_{pd}	Ω	Extra plasma resistance	36
R_{th}	KW^{-1}	Total thermal resistance	113
$R_{th,hs}$	KW^{-1}	Heatsink-to-ambient thermal resistance	111
$R_{th,jc}$	KW^{-1}	Junction-to-case thermal resistance	111
$R_{th,tim}$	KW^{-1}	Thermal resistance of the TIM	111
s	$rad\,s^{-1}$	Complex frequency	38
t	s	Time	5
T	K	Temperature	4
t_{cf}	s	Switch current fall time	106
t_{cr}	s	Switch current rise time	106
T_e	K	Electron temperature	5
T_f	s	Voltage falling time	92
T_i	K	Ion temperature	5
T_j	K	Junction temperature	116

Continued on next page

Symbol	Unit	Description	First use
T_n	K	Neutral gas temperature	5
T_p	s	Post-discharge phase duration	92
T_p1	s	Current falling time	92
T_p2	s	Flexible time during post-discharge phase	92
T_pulse	s	Voltage pulse duration	29
T_r	s	Voltage rising time	91
T_slope	s	Voltage slope duration	29
T_step	s	Time step	71
t_sw	s	Total commutation time	114
T_tr	s	Total transient time	101
t_vf	s	Switch voltage fall time	106
t_vr	s	Switch voltage rise time	106
u	V	Electric potential	6
u_0	V	Initial capacitor voltage	86
u_a	V	Potential of surface A	10
u_b	V	Potential of surface B	10
u_C	V	Voltage across C	86
u_{C_1}	V	Potential of RFEA collector	52
u_cn	V	Common-node voltage	25
u_{C_sh0}	V	Voltage across C_sh0	26
u_{C_sh1}	V	Voltage across C_sh1	26
u_{C_sub}	V	Voltage across C_sub	26
u_ds	V	Drain-source voltage	105
u_ext	V	Excitation voltage	86
u_{G_0}	V	Potential of RFEA grid G_0	51
u_{G_1}	V	Potential of RFEA grid G_1	51
u_{G_2}	V	Potential of RFEA grid G_2	51
u_{G_3}	V	Potential of RFEA grid G_3	51
u_gs	V	Gate-source voltage	105
u_L	V	Voltage over L	74
u_{L_f}	V	Voltage over L_f	73
u_{L_s}	V	Voltage over L_s	73
u_mt	V	Multilevel tailored waveform	71
u_out	V	Output voltage	25
u_p	V	Plasma potential	8
u_sh1	V	Substrate surface potential	25
u_sn	V	Switched-node voltage	76
u_st	V	Sawtooth waveform	71

Continued on next page

Symbol	Unit	Description	First use
u_t	V	Table potential	29
u_tl	V	Tailored waveform	71
u_w	V	Material surface potential	9
v	$\mathrm{m\,s^{-1}}$	Velocity	4
V_0	V	Voltage offset over C_sh0	26
V_1	V	Voltage offset over C_sh1	26
v_avg	$\mathrm{m\,s^{-1}}$	Average velocity	4
v_B	$\mathrm{m\,s^{-1}}$	Bohm velocity	8
V_b	V	Blocking voltage	25
V_c	V	Voltage used to generate constant current	149
V_d	V	Discharge voltage	19
V_dc	V	Dc-link voltage	106
V_dsn	V	Discharge voltage at switched-node	78
V_e	V	Voltage at the end of charge phase	90
$v_\mathrm{e,avg}$	$\mathrm{m\,s^{-1}}$	Average electron velocity	8
V_f	V	Intermediate voltage level for falling edge	90
V_fsn	V	Intermediate voltage level at switched-node for falling edge	90
v_i	$\mathrm{m\,s^{-1}}$	Ion velocity	7
v_is	$\mathrm{m\,s^{-1}}$	Ion velocity at sheath boundary	7
V_mil	V	Miller voltage	106
V_p	V	Potential difference	9
V_off	V	Turn-off voltage	106
V_on	V	Turn-on voltage	106
V_r	V	Intermediate voltage level for rising edge	90
V_rf	V	RF voltage magnitude	25
V_rsn	V	Intermediate voltage level at switched-node for rising edge	90
v_rms	$\mathrm{m\,s^{-1}}$	RMS thermal velocity	4
V_s	V	Start voltage of the voltage slope	29
V_step	V	Voltage step	71
V_sub	V	Voltage offset over C_sub	26
V_th	V	Switch turn-on threshold	106
v_x	$\mathrm{m\,s^{-1}}$	Velocity along coordinate x	4
W	J	Work	5
$\boldsymbol{x}$	m	Displacement	5
Z	Ω	Impedance of LC circuit	86
Z_0	Ω	Impedance of plasma reactor	89

D.3 Global Symbols (Greek)

Symbol	Unit	Description	First use
Γ_e	$m^{-2}\,s^{-1}$	Electron flux	9
ϵ	$F\,m^{-1}$	Dielectric constant	6
ϵ_r	-	Relative permittivity	111
ε	A	A small positive current	37
κ	$W\,m^{-1}\,K^{-1}$	Thermal conductivity	111
λ_D	m	Debye length	9
μ	-	Mean	38
ν	F^2	Product of capacitances	154
ρ_f	$C\,m^{-3}$	Volume charge density	6
σ	-	Standard deviation	38
τ	s	RC time constant	62
τ_i	s	Ion transit time	37
ω	$rad\,s^{-1}$	Natural frequency of LC circuit	86
ω_0	$rad\,s^{-1}$	Natural frequency of plasma reactor	89
ω_i	$rad\,s^{-1}$	Ion plasma frequency	38

D.4 Physical constants and conversion factors

Quantity	Value	Unit	Description	First use
amu	$1.6606 \cdot 10^{-27}$	kg	Atomic mass unit	9
e	$1.6022 \cdot 10^{-12}$	C	Elementary charge	5
e	2.7182	-	Euler's number	4
k_B	$1.3807 \cdot 10^{-23}$	$J\,K^{-1}$	The Boltzmann constant	4
ϵ_0	$8.8542 \cdot 10^{-12}$	$F\,m^{-1}$	Vacuum permittivity	8

D.5 Acronyms

Acronym	Description	First use
ac	alternating current	70
AI	artificial intelligence	iii

Continued on next page

Acronym	Description	First use
Al_2O_3	aluminium oxide	35
ALD	atomic layer deposition	14
ALE	atomic layer etching	16
AlN	aluminum nitride	121
amu	atomic mass unit	9
Ar	argon	9
CCP	capacitively coupled plasma	17
CHB	cascaded H-bridge converter	76
Cl_2	chlorine	16
CM	common-mode	77
CPU	central processing unit	13
CVD	chemical vapor deposition	14
DAB	dual-active bridge	125
dc	direct current	3
ECC	extended commutation cell	78
EEC	equivalent electric circuit	iv
EMI	electromagnetic interference	77
FCC	flying capacitor converter	76
$FeCl_3$	ferric chloride	15
FFC	flat flex cable	122
FPGA	field programmable gate array	119
FWHM	full width at half maximum	38
GaN	gallium nitride	69
Ge	germanium	16
H_2	hydrogen	14
H_2O	water	15
HAR	high aspect ratio	15
HEMT	high-electron-mobility transistor	109
IC	integrated circuit	iii
ICP	inductively coupled plasma	17
IDC	insulation-displacement connector	121
IED	ion energy distribution	iv
LTI	linear time-invariant	72
MMC	modular multilevel converter	78
MOSFET	metal–oxide–semiconductor field-effect transistor	12
NPC	neutral-point-clamped converter	76
NTC	negative temperature coefficient	123
O_2	oxygen	14

Continued on next page

Acronym	Description	First use
PCB	printed circuit board	15
PE	protective earth	52
PEALD	plasma-enhanced atomic layer deposition	15
PEALE	plasma-enhanced atomic layer etching	16
PECVD	plasma-enhanced chemical vapor deposition	14
PIC	particle-in-cell	iv
PWM	pulse-width modulation	68
RF	radio-frequency	3
RFEA	retarding field energy analyser	iv
RIE	reactive ion etching	16
RMS	root-mean-square	4
Si	silicon	12
SiC	silicon carbide	69
$SiCl_4$	silicon tetrachloride	15
SiH_4	silane	14
SiO_2	silicon dioxide	12
SMPC	switched-mode power converter	iv
SPICE	simulation program with integrated circuit emphasis	44
TIM	thermal interface material	108
ZVS	zero-voltage switching	112

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Curriculum vitae

Qihao Yu was born in Quzhou, China in 1995. He obtained his B.Sc. degree in Electrical Engineering and Automation from Zhejiang University, Hangzhou, China, in 2017. He went on to complete his M.Sc. degree in Electrical Engineering (*cum laude*) at Eindhoven University of Technology (TU/e), Eindhoven, the Netherlands, in 2018.

Starting in November 2018, he embarked on his journey as a Ph.D. candidate in the Power Electronics Lab (PEL/e), part of the Electromechanics and Power Electronics (EPE) group within the Electrical Engineering department at TU/e. Since 2017, he has also been working as a part-time engineer at Prodrive Technologies B.V., Son, the Netherlands. His research endeavors primarily revolve around high-performance power electronics for advanced industrial applications, particularly in semiconductor manufacturing, focusing on areas like plasma etching and deposition.

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