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Abstract—This paper proposes a dual-cell switching power amplifier with ultra-high small-signal bandwidth. A control strategy is introduced to guarantee system stability while two converter cells work together to increase the control bandwidth. Simulation results show that the proposed converter can achieve up to 33 times larger control bandwidths, compared with a conventional single-cell half-bridge converter working with the same switching frequency as the high-voltage cell.

Index Terms—accuracy, productivity, power amplifier, high bandwidth.

I. INTRODUCTION

Accuracy and productivity improvement are two strong performance metrics in many high-precision systems such as lithography machines, 3D printing systems, high-energy particle accelerators, and medical imaging scanners. For example, in a lithography machine, a Lorentz short-stroke actuator exerts a force proportional to the current through the actuator coils that leads to the desired displacement. These actuators cause displacements in the range of micrometers with precision in the range of hundreds of picometers [1], [2]. Fig. 1 (a) illustrates a typical acceleration trajectory of a lithography machine [1]. Considering a simple model of a linear short-stroke actuator and a one-phase power amplifier, the reference digital current waveform is proportional to the acceleration reference, as seen in Fig. 1 (a). The short-stroke power amplifier must convert the digital reference current to a low-noise and low-distortion current through the actuator to prevent the generation of undesired forces that disturb the positioning system movements. Considering the current trajectory, there are some requirements for both the large and small signal bandwidths of the power amplifier. Firstly, the large signal bandwidth should be high enough to follow the general shape of the current reference. Since the whole period of the acceleration reference, $T_{p,a}$, is in the range of a few hundred ms and the large signal rise time, T_r, is in the range of a few ms, there is no necessity to increase the large signal bandwidth to more than a few kHz. However, the digital current reference is dictated by an outer position control loop that works with a sampling frequency, $f_{s,pos} = \frac{1}{T_{s,pos}}$, in the

range of tens of kHz. Thus, after every $T_{s,pos}$, a new current reference is created that has a small change compared with the previous reference signal. Hence, from the small-signal operation viewpoint, the power amplifier should be able to work as close as possible to an ideal Zero Order Hold (ZOH), see i_{ref} in Fig. 1 (a). For achieving this goal, higher small signal bandwidths are preferable. Moreover, a higher small signal bandwidth allows for achieving higher position loop sampling frequencies and more productivity.

Output waveform closed-loop control and feedforward strategy are two main control approaches that are applied to make such low-noise low-distortion currents. To design a feedforward controller, the plant should be well defined; also, most feedforward controllers are specifically designed for one converter and should be changed depending on the type of components. Also, they cannot compensate for ambient and aging effects and need recalibration [3], [4]. The closed-loop control strategy requires a high control bandwidth and open-loop gain to improve disturbance rejection. Commercially, class-D power amplifiers are applied for converters in a short-stroke application. The bus voltage is 400V and the peak output current can reach up to 50A. The switching frequency of a class-D power amplifier is proportional to its control bandwidth. Hence for achieving higher control bandwidths, higher switching frequencies are inevitable. However, the switching losses of relatively high-voltage (e.g., 650-V rating) semiconductors limit the highest achievable switching frequency of the conventional class-D power amplifiers to a few hundred kHz [2], [4].

On the other hand, low-voltage power semiconductors can easily reach switching frequencies up to tens of MHz [5], [6]. Hence, inspired by the hybrid power amplifier idea introduced in [7], a dual-cell power amplifier solution is introduced in this paper with a main Low-Frequency High-Voltage (LF-HV) cell, that provides the bulk output power, and a correction High-Frequency Low-Voltage (HF-LV) cell, that increases the small signal bandwidth and fine control of the output power. Fig. 2 (a) shows a single-phase half-bridge representation of the proposed power amplifier. In comparison with a conventional single-cell Half-Bridge (HB) converter, the correction cell is added in series with the output capacitor, so there is no additional semiconductor device in the main power path. Therefore, the current and voltage stress of the HF-
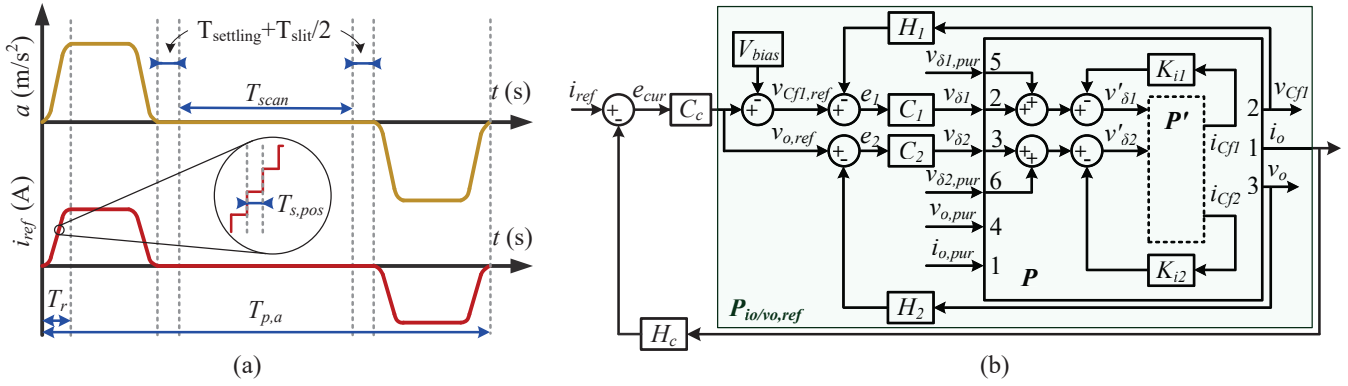
Fig. 1: (a) Acceleration and current reference in a lithography machine, considering a simple model of a short-stroke actuator and a one-phase power amplifier; (b) control diagram of the proposed converter with a high-frequency shunt correction cell.
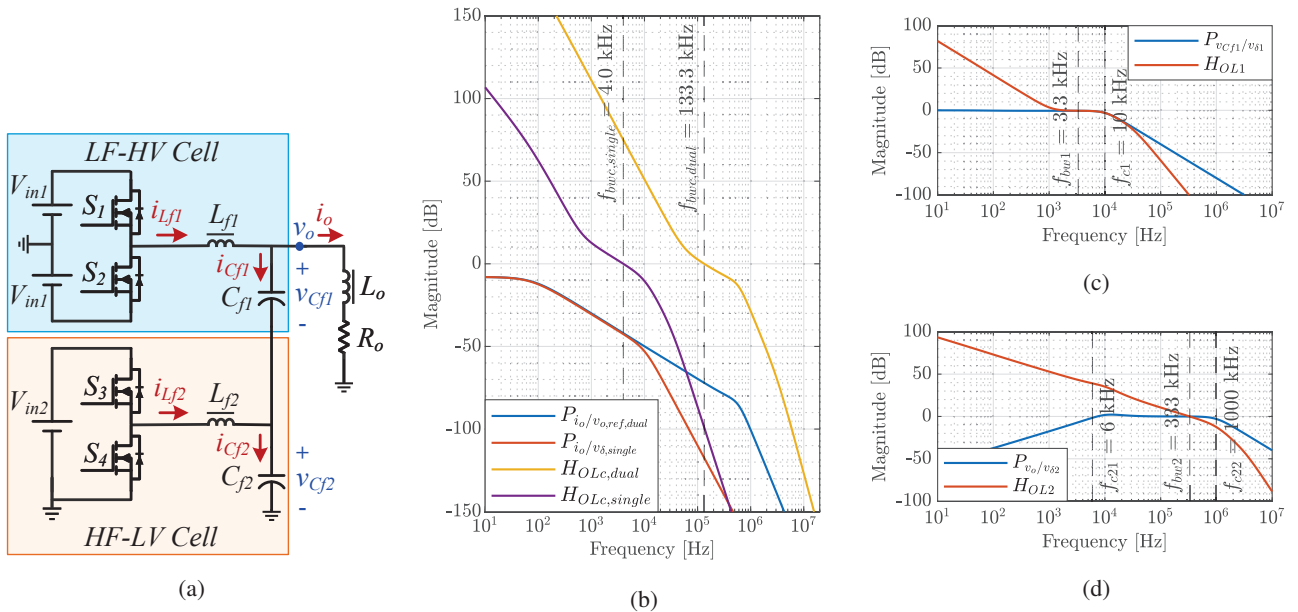

Fig. 2: (a) Single-phase half-bridge representation of the proposed converter; (b) proposed dual-cell converter controller open-loop gain compared with single-cell converter controller open-loop gain; (c) LF-HV cell controller open-loop gain; (d) HF-LV cell controller open-loop gain.

LV cell is minimized, and the whole system efficiency does not degrade considerably. Moreover, a low-voltage unipolar voltage source is used for powering the HF-LV cell. Unlike the converter in [4], no isolated voltage source is used. Hence, there is no need for transformers, EMI filters, nor power-factor-correction converters to make the HF-LV cell voltage source. The main challenge of implementing the proposed converter is to control both LF-HV and HF-LV cells to increase the control bandwidth while the whole system remains stable. Thus, this paper mainly focuses on the control strategy of the proposed converter. As the suggested control strategy delivers higher loop gain compared with the conventional single-cell converter, the unwanted disturbances are rejected faster. Hence, output current errors are damped quickly during the settling time, $T_{settling}$ in Fig. 1 (a), and the wafer position

is set more accurately during the scan time, T_{scan} in Fig. 1 (a).

II. CONVERTER WITH A SHUNT CORRECTION CELL CONTROL STRATEGY

In order to evaluate different control strategies, the State-Space-Average (SSA) model of the proposed converter is determined. Then, for calculating the SSA model, parasitic components are neglected, and active-damping of the output filter is considered. The proposed converter SSA model has seven inputs, including the unwanted perturbations, three outputs and five state variables as
$$u = \begin{bmatrix} i_{o,pur} & v_{\delta 1} & v_{\delta 2} & v_{o,pur} & v_{\delta 1,pur} & v_{\delta 2,pur} \end{bmatrix}^T, \quad y = \begin{bmatrix} i_o & v_{Cf1} & v_o \end{bmatrix}^T, \text{ and } x = \begin{bmatrix} i_{Lf1} & i_{Lf2} & i_o & v_{Cf1} & v_{Cf2} \end{bmatrix}^T.$$
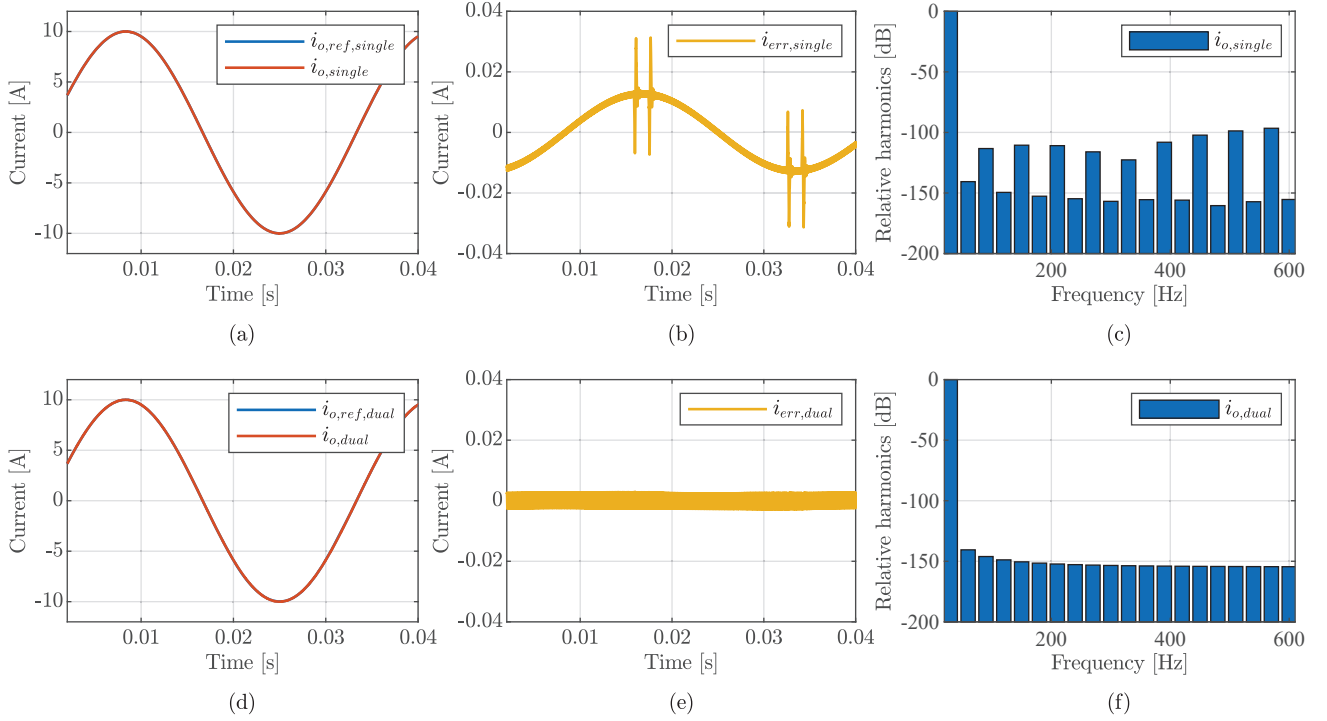
Fig. 3: Simulation results for a sinusoidal sinusoidal reference current 10 A/30 Hz: (a) single-cell converter input reference and output currents, (b) single-cell converter output current error, (c) single-cell converter output current harmonic content, (d) proposed dual-cell converter input reference and output currents, (e) dual-cell converter output current error, (f) dual-cell converter harmonic content.
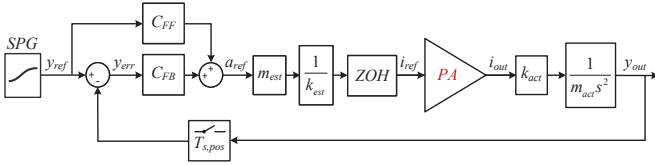

Fig. 4: Generic outline of a motion control system.

The SSA matrices are as follows:

$$A = \begin{bmatrix} \frac{-K_{i1}}{L_{f1}} & 0 & \frac{K_{i1}}{L_{f1}} & \frac{-1}{L_{f1}} & \frac{-1}{L_{f1}} \\ \frac{-K_{i2}}{L_{f2}} & \frac{-K_{i2}}{L_{f2}} & \frac{K_{i2}}{L_{f2}} & 0 & \frac{-1}{L_{f2}} \\ 0 & 0 & \frac{-R_o}{L_o} & \frac{1}{L_o} & \frac{1}{L_o} \\ \frac{1}{C_{f1}} & 0 & \frac{-1}{C_{f1}} & 0 & 0 \\ \frac{1}{C_{f2}} & \frac{1}{C_{f2}} & \frac{-1}{C_{f2}} & 0 & 0 \end{bmatrix},$$

(1)

$$B = \begin{bmatrix} \frac{-K_{i1}}{L_{f1}} & \frac{1}{L_{f1}} & 0 & 0 & \frac{1}{L_{f1}} & 0 \\ \frac{-K_{i2}}{L_{f2}} & 0 & \frac{1}{L_{f2}} & 0 & 0 & \frac{1}{L_{f2}} \\ 0 & 0 & 0 & \frac{-1}{L_o} & 0 & 0 \\ \frac{1}{C_{f1}} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{f2}} & 0 & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$C = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{bmatrix}, D = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\Rightarrow \begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases}$$

Fig. 1 (b) represents the control diagram of the proposed converter. As $v_o = v_{Cf1} + v_{Cf2}$, by controlling two of these three variables, the plant can be shaped so that the control bandwidth is increased. As shown in Fig. 2 (c), $P_{v_{Cf1}/v_{\delta1}}$ is a Low-Pass-Filter (LPF) with a low-pass corner frequency, f_{c1}. Hence, the LF-HV cell controls v_{Cf1} to shape the dc and low-frequency signals. The controller, $C_1 = \frac{s^2 + 2\zeta_{z1}\omega_{z1}s + \omega_{z1}^2}{s^2}$, has two poles at the origin to improve the low-frequency gain and two complex-conjugate zeros around the corner frequency to improve the phase margin. As shown in Fig. 2 (d), $P_{v_o/v_{\delta2}}$ is a Band-Pass-Filter (BPF) whose lower cut-off frequency, f_{c21}, is close to f_{c1}, and its higher cut-off frequency, f_{c22}, is located further away. This provides the possibility of increasing the small signal bandwidth for controlling v_o. The controller $C_2 = \omega_{bw2}\frac{s+\omega_{c1}}{s^2}$ has two poles at the origin and one zero around f_{c21}. When both controllers C_1 and C_2 work together, the corner frequency of the plant $P_{i_o/v_{o,ref}}$ is increased compared with the conventional single-cell converter. Hence, a higher control bandwidth for controlling the output current is achievable. Finally, the current controller, $C_c = \frac{s^2 + 2\zeta_{zc}\omega_{zc}s + \omega_{zc}^2}{s^2}$, is designed based on a loop-shaping strategy to build -3,-1,-3 slopes for the system loop gain. In order to use a unipolar voltage source a constant bias voltage, $V_{bias} = \frac{V_{in2}}{2}$, is subtracted from the LF-HV cell reference voltage; thus, v_{Cf1} always has a negative bias voltage while v_{Cf2} has a positive bias voltage.
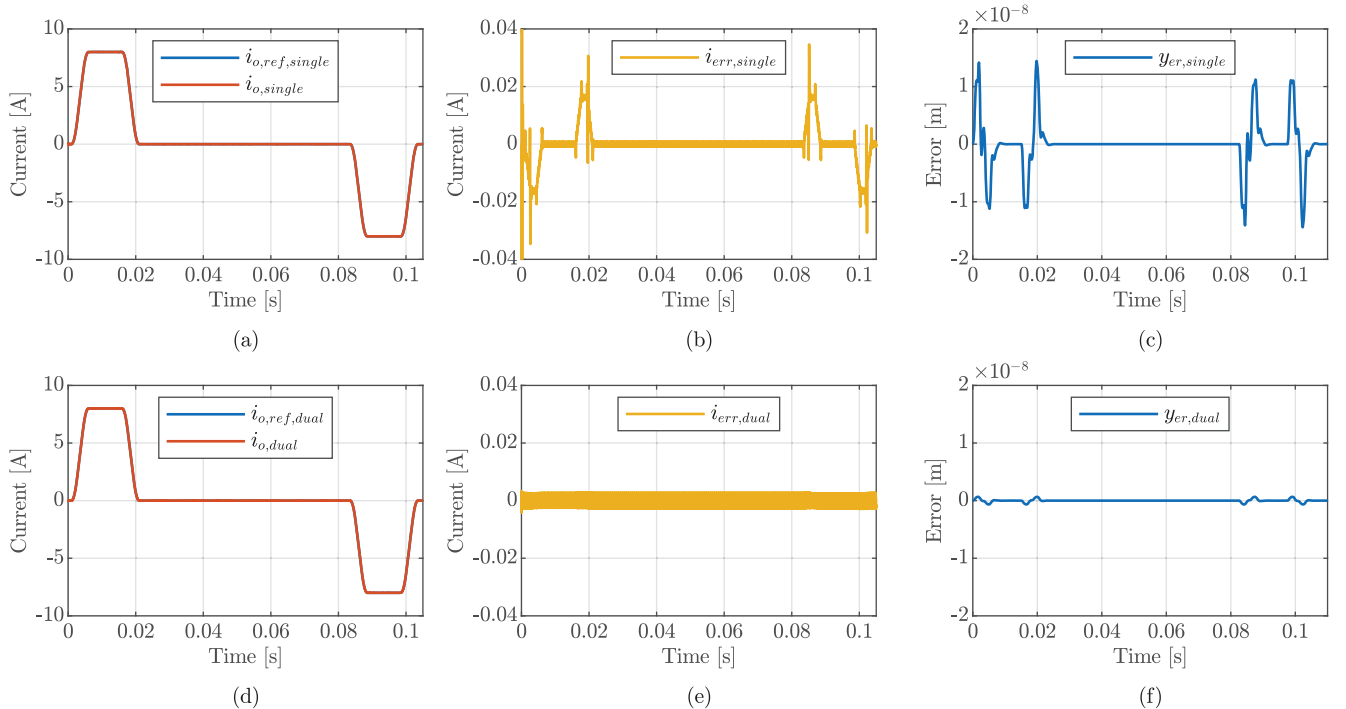
Fig. 5: Simulation results for a trapezoidal reference current: (a) single-cell converter input reference and output currents, (b) single-cell converter output current error, (c) single-cell converter position error, (d) proposed dual-cell converter input reference and output currents, (e) dual-cell converter output current error, (f) dual-cell converter position error.

III. SIMULATION RESULTS

The single-phase half-bridge representation of the proposed dual-cell converter, shown in Fig. 2 (a), is simulated in PLECS to evaluate its performance. The specifications of the simulated converter are as follows: $V_{in1} = 200$ V; $V_{in2} = 50$ V; $R_o = 2.5$ Ω; $L_o = 5$ mH; $f_{sw1} = 100$ kHz; $f_{sw2} = 10$ MHz; $T_{d1} = 50$ ns; $T_{d2} = 20$ ns; $L_{f1} = 333$ µH; $L_{f2} = 312$ nH; $C_{f1} = 760$ nF; $C_{f2} = 81$ nF; S_1, S_2 : GS66508T; S_3, S_4 : GS61004B. The proposed converter is simulated in closed loop with natural sampling for two different current references: 1. sinusoidal reference current 10 A/30 Hz, and 2. trapezoidal reference current with 8 A peak. Fig. 3 illustrates the simulation waveform of $i_{o,ref}$, i_o and i_o harmonics in comparison with the single-cell converter with the same switching frequency as the HV-LF cell. The largest output current harmonic is -140 dB, showing 40 dB improvement in comparison with the conventional solution. This achievement is due to increasing the loop gain of the proposed converter, as seen in Fig. 2 (b). As shown in Fig. 2 (d) and (e), the output current has high frequency errors in the range of hundreds of kHz and a peak amplitude lower than 3 mA. Usually, the position loop has very low sensitivity to errors in this high frequency range. Also, compared with the single-cell converter, the LF-HV cell dead-time errors that occur close to zero-crossing areas are compensated by the high frequency cell.

Fig. 4 represents a simplified schematic of a high-precision

position loop. In high-precision systems, the current reference of the power amplifier is proportional to the acceleration reference of the position loop. As in a lithography machine the acceleration reference has a trapezoidal shape, see Fig. 1 (a), the power converter response to a trapezoidal reference current is investigated. Fig. 5 shows the simulation results of the proposed dual-cell converter compared with its single-cell HB rival considering a trapezoidal reference current. While the peak current error in the single-cell converter reaches 0.04 A, the current error of the dual-cell converter is limited to 0.003A, and only high-frequency harmonics of f_{sw1} are seen in the current error waveform, that have no visible effect on the position error, compare Fig. 5 (f) with Fig. 5 (c). In order to analyze the effect of this converter on a position system, the proposed power amplifier is put in an ideal position loop; then, the position system is simulated in MATLAB Simulink and PLECS Blockset. The position error indices Moving Average (MA), Moving Standard Deviation (MSD), and Moving Root Mean Square (MRMS) that are defined in [1], [8] are applied to evaluate the error contribution of the proposed dual-cell converter in the position loop. For comparison, the position error indices are calculated for a single-cell converter with the same switching frequency as the LF-HV cell as well. For a top-hat window, $w_{th}(t)$, the MA and MSD functions are defined as

$$MA(t) = w_{th}(t) * y_{err}(t) = \frac{1}{T} \int_{t-T/2}^{t+T/2} y_{err}(\tau)d\tau \quad (2)$$

$$MSD(t) = \sqrt{w_{th}(t) * y_{err}^2(t) - MA^2(t)}$$
$$= \sqrt{\frac{1}{T} \int_{t-T/2}^{t+T/2} (y_{err}(\tau) - MA(t))^2 d\tau}. \quad (3)$$

MA, that is related to the overlay error in a high-precision position system, is a low-pass-filter and passes the low-frequency part of the error. MSD shows the high-frequency part of the error and is related to the achievable critical dimensions. MRMS is an inclusive position error index that combines both MA and MSD errors and is defined as $MRMS(t) = \sqrt{MA(t)^2 + MSD(t)^2}$.

Fig. 6 shows the calculated MA, MSD, and MRMS errors. The position errors of the proposed power amplifier are remarkably lower compared with its single-cell HB rival. In a lithography machine, these errors are specially important in the time-limited exposure window, thus the maximum MRMS value in this time window is reported as a valuable decision factor. While the maximum MRMS of the conventional single-cell converter in the exposure window is 189.47 pm, the MRMS error of the proposed dual-cell converter is 7.93 pm, i.e. a 23 times improvement. This improvement is due to the increase of the power amplifier bandwidth and its higher control gain.

IV. LOSS BREAKDOWN ANALYSIS

In this section the switching semiconductors losses are calculated and compared for the proposed dual-cell power amplifier and a quad-phase interleaved HB converter with the same control loop bandwidth and, therefore, the same MRMS error as the proposed converter ($f_{bw,quad} = 133.3$ kHz, $f_{sw,quad,eff} = 3$ MHz). As shown in Fig. 7, the quad-phase interleaved HB converter, appears as a strong competitor for the proposed dual-cell converter because by using interleaved switching legs the converter effective switching frequency increases, in proportion to the number of the interleaved phases. Thus, in order to make a quad-phase converter with an effective switching frequency of 3 MHz, each switching leg has a switching frequency of 3/4 MHz. Hence, the switching losses are decreased in the switching legs. Also, as the power is shared between the interleaved legs, the conduction losses of the switching devices are reduced. In order to compare the converters power dissipation, a pure resistive load, $R_o = 10 \ \Omega$, and a constant reference current $I_{ref} = 10$ A is considered.

In a switching leg, the dissipation in the switching semiconductors can be divided to the conduction and switching losses:

$$P_{cond} = P_{cond,dir} + P_{cond,rev}, \quad (4)$$
$$P_{sw} = P_{on} + P_{off} + P_{drive}. \quad (5)$$

The direct conduction loss, $P_{cond,dir}$, is obtained as $P_{cond,dir} = R_{ds}I_{rms}^2$, where R_{ds} and I_{rms} are the on-resistance and RMS current through the switch, respectively. The conduction losses during the reverse conduction mode can be estimated as

$$P_{cond,rev} = I_{on}t_{d1} \ f_{sw}V_{sd} + I_{off}t_{d2} \ f_{sw}V_{sd}, \quad (6)$$
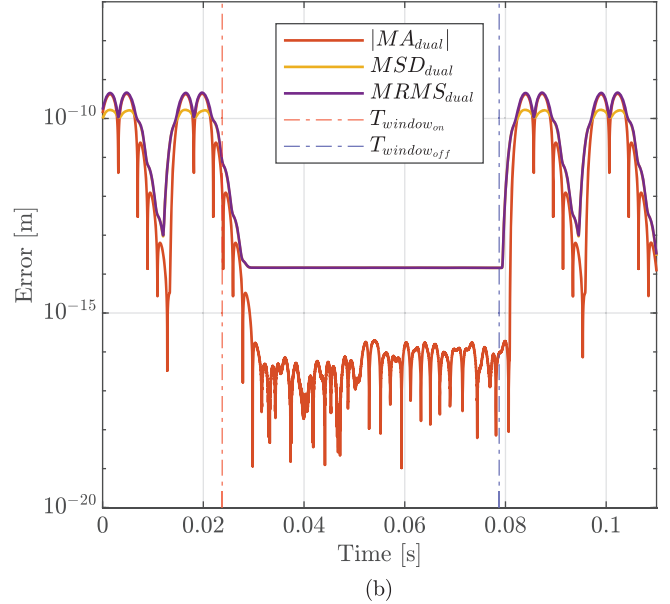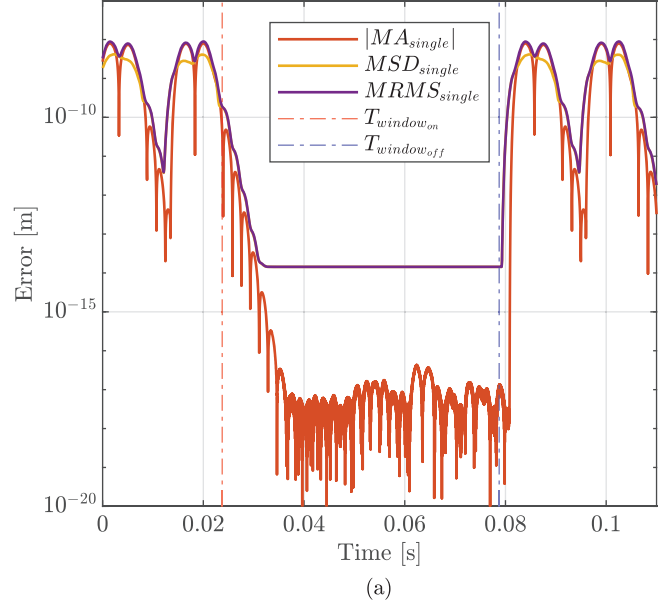

Fig. 6: Position errors of (a) the single-cell converter and (b) the proposed dual-cell converter.

where t_{d1}, t_{d2}, I_{on}, I_{off}, V_{sd}, and f_{sw}, are the turn-on deadtime, turn-off deadtime, current through the switch during the turn-on transient, current through the switch during the turn-off transient, voltage drop over the switch in reverse conduction mode, and the switching frequency, respectively.

The turn-on and turn-off switching losses in GaN transistor are calculated based on the datasheet parameters following the method introduced in [9]. The driver loss of a switching semiconductor device is calculated using $P_{drive} = Q_g V_{gs} f_{sw}$, where Q_g and V_{gs} are the total gate charge and the gate-source voltage, respectively.
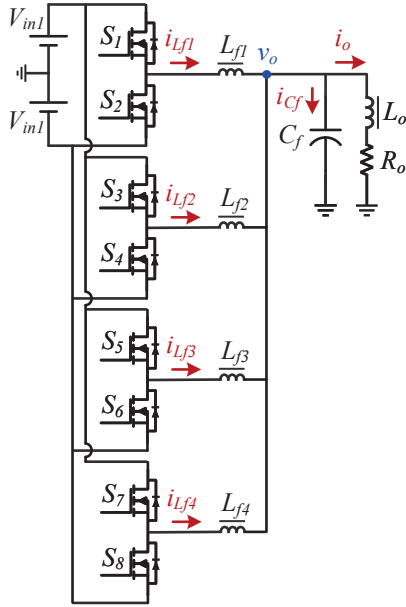
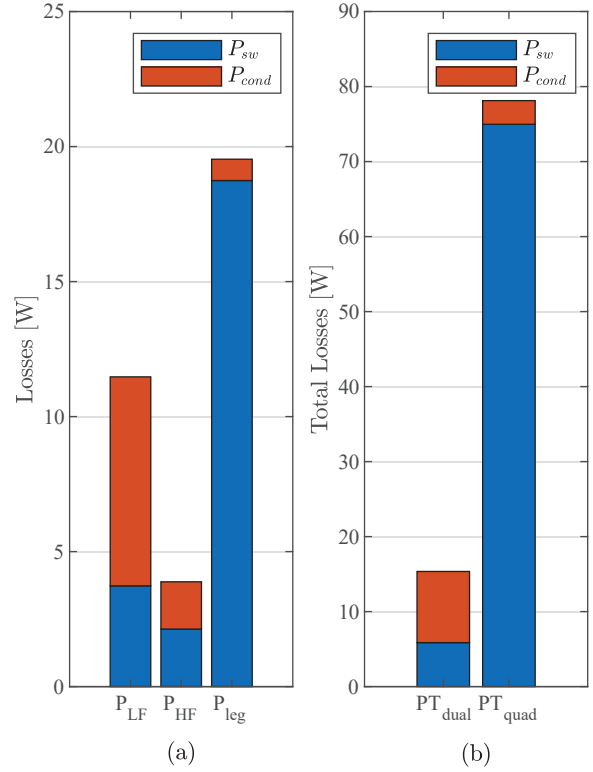Fig. 7: quad-phase interleaved half-bridge converter schematic.

Fig. 8: Dissipation in the switching devices (a) switching and conduction losses of LF-HV cell, HF-LV cell, and one switching leg of the quad-phase interleaved HB converter, (b) total switch losses of the proposed dual-cell converter and the quad-phase interleaved HB converter.

By using the explained relations the power dissipated in LF-HV cell and HF-LV cell is analytically calculated and compared with the power dissipation of the quad-phase interleaved converter. As Fig. 8 (a) illustrates, the HF-LV cell adds minimum additional losses to the system. While the switching frequency of HF-LV cell is high, this cell has a low voltage stress (50 V). Thus, low voltage 100 V GaN transistors that have lower on-resistance and parasitic capacitance can be used for this cell. Moreover, since on average the output current of the HF-LV cell is zero, by selecting its current ripple larger than the LF-HV cell current ripple, both switches of the HF-LV cell are always turned-on under zero voltage switching (ZVS), and hence, the turn-on switching loss of this cell is negligible. Furthermore, the conduction losses in this cell are low because it delivers no net power. Consequently, as Fig. 8 (a) shows, the total loss of HF-LV cell is around 1/3 of LF-HV cell. Having the possibility of reducing the switching frequency in the LF-HV cell, $f_{sw1} = 100$ kHz, leads to a considerable decrease in the switching losses of this cell. Thus, even though in the quad-phase interleaved HB converter the conduction loss of each switching leg is considerably decreased, the reduction of the switching frequency is not comparable with the LF-HV cell in the dual-cell converter, and the switching losses are still considerably high in each switching leg. Furthermore, as seen in Fig. 8 (b), since in the quad-phase HB interleaved converter each switching leg is directly connected to the high-voltage bus and provides a part of power to the output, the total loss of the quad-phase HB interleaved converter is considerably higher than the total loss of the dual-cell HB converter.

V. Conclusion

The proposed dual-cell power amplifier solution combines a main low-frequency high-voltage cell, that provides the bulk

output power, with a correction high-frequency low-voltage cell, which increases the small signal bandwidth and fine control of the output power. In comparison with a conventional single-cell converter, the correction cell is added in series with the output capacitor, so there is no additional semiconductor device in the main power path. Moreover, a low-voltage unipolar voltage source is used for powering the correction cell. Therefore, the current and voltage stress of the HF-LV cell is minimized, and the whole system efficiency does not degrade considerably. The main challenge of implementing the proposed converter is to control both LF-HV and HF-LV cells to increase the control bandwidth while the whole system remains stable. Thus, this paper mainly focuses on the control strategy of the proposed converter. As the suggested control strategy delivers higher loop gain compared with the conventional single-cell converter, the unwanted disturbances are rejected faster. Hence the MRMS error contribution of the converter in a linear actuator position loop is reduced to 8 pm.

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