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Citation for published version (APA):
Ying, K., & Gao, H. (2023). A 25% Tuning Range 7.5-9.4 GHz Oscillator With 194 FoM_and 400 kHz 1/f Corner in 40nm CMOS Technology. IEEE Access, 11, 6351-6356. Article 10018234. https://doi.org/10.1109/ACCESS.2023.3237488

DOI:

10.1109/ACCESS.2023.3237488

Document status and date:

Published: 01/01/2023

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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Download date: 17 Nov. 2023



Received 27 December 2022, accepted 11 January 2023, date of publication 16 January 2023, date of current version 20 January 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3237488



APPLIED RESEARCH

A 25% Tuning Range 7.5–9.4 GHz Oscillator With 194 FoM₇ and 400 kHz 1/f₃ Corner in 40nm CMOS Technology

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This work was supported in part by Cluster for Application and Technology Research in Europe on Nanoelectronics (CATRENE), Coexistence of Radio Frequency Transmission In the Future (CORTIF) Project, and in part by the AutoDrive Project, financed by ECSEL Joint Undertaking within the Scope of the Horizon 2020 Research and Innovation Programme.

ABSTRACT An 8-GHz VCO with class-F₂₃ operation was realized in a 40 nm CMOS technology without ultra-thick metals. The class-F₂₃ operation was enabled in a transformer-based LC tank to allow multiple impedance peaks in the common mode (CM) and the differential mode (DM) excitation. With the additional resonance at 2nd and 3rd harmonic frequency, the circuit noise to phase-noise conversion and 1/f noise up-conversion are reduced significantly. In a 40 nm CMOS technology without ultra-thick metal, a patterned shielding structure was proposed to improve the inductor quality factor. A combined varactor and capacitor array is proposed to provide accurate matching for a desired resonance frequency ratio, reducing AM-FM conversion and it achieves a broad tuning range. With the proposed transformer-based LC bank and class-F₂₃ operation, the oscillator achieves a phase noise of -150.8 dBc/Hz at 10 MHz offset from a 1.85 GHz carrier after an on-chip /4 divider, and the measured 1/f₃ flicker noise corner is around 400 kHz. The oscillator core covers a 7.5-9.4 GHz frequency range for a 25% tuning range.

INDEX TERMS VCO, phase noise, CMOS, transformer, class-F₂₃.

I. INTRODUCTION

Modern wireless transceivers have a stringent requirement for spectral purity. For example, RF receivers working under coexistence scenarios suffer from noise figure degradation due to reciprocal mixing between the LO signal and the interferer at a mixer input [1], [2], [3], [4], [5], [6], [7], [8]. Interferes could be several MHz or tens of MHz away from the wanted signal. In order to reduce the effect of reciprocal mixing, it is desirable to suppress interferes before the mixer and to have an LO with very low phase noise. However, methods are very challenging with the decrease in the offset frequency. For frequency ranges in the order of several or tens of MHz, the LO phase noise is usually dominated by the phase noise from the oscillator [9]. Therefore it is desired to lower the VCO phase noise so that the reciprocal mixing causes negligible impact.

The associate editor coordinating the review of this manuscript and approving it for publication was Harikrishnan Ramiah

In conventional voltage-controlled oscillator design, the close-in phase noise (PN) is usually degraded by 1/f flicker noise up-conversion and varactor's AM to FM conversion [10], [11]. Even though technology scaling improves capacitor density and effective maximum and minimum capacitance ratio, the inductor quality factor is degraded. It is even worse in a digital library due to the lack of ultrathick metal, which further deteriorating the performance. An additional tank with resonance at the second harmonic can significantly reduce the 1/f₃ flicker noise corner [11]. However, it requires extra area and extra tuning on the 2^{nd} resonant frequency to cover a wide tuning range. Other recent works on oscillator [12], [13], [14] achieve low phase noise by using a transformer-based LC tank with additional resonance at the third harmonic frequency (class-F₃). It benefited from accurate capacitor matching for accurate control on resonant frequency ratio and a transformer implemented with ultrathick metal.

In this work, we propose a oscillator with class-F₂₃ operation to achieve low PN and low 1/f3 corner frequency by



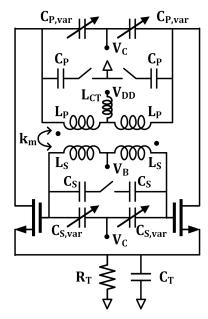


FIGURE 1. The schematic of the proposed class-F₂₃ oscillator core.

enabling additional resonance at the 2^{nd} and 3^{rd} harmonic frequencies with a transformer-based LC tank. The transformer is realized with pattern shielding to improve the quality factor. The capacitor bank is composed of a combination of varactor and binary-weighted MoM capacitor array, minimizing PN degradation due to varactor AM-FM conversion. And this capacitor array combination achieves a 25% tuning range.

This paper is organized as the following. Section II shows the schematic of the proposed transformer-based class-F₂₃ VCO and analyses the condition for the class-F₂₃ operation. Section III describes the detailed realization of a high-*Q* transformer and capacitor bank with large tuning and high linearity. The details of circuit implementation and measurement results are discussed in section IV. Conclusions and a comparison to other state-of-arts are drawn in Section V.

II. PROPOSED VCO SCHEMATIC WITH CLASS- $\mathbf{F}_{\mathbf{23}}$ OPERATION

The schematic of the proposed class- F_{23} oscillator is shown in Fig. 1. In this class- F_{23} oscillator, a 2-wing transformer-based LC tank has multiple impedance peaks in differential-mode (DM) and common-mode (CM) operations [13]. This is explained in Fig. 2.

In the DM operation, the tank has an auxiliary impedance magnitude peak ideally at the third harmonic frequency. A pseudo-square waveform oscillation is created with an extended region of the waveform where its impulse sensitivity function (ISF) is close to zero. The fundamental resonant frequency is $\omega_1^2 = 1/(L_P C_{P,tot} + L_S C_{S,tot})$, where L_P and L_S is the inductance at the transformer's primary and second winding. $C_{P,tot}$ and $C_{S,tot}$ is the total capacitance at each winding. The ratio between two DM resonant frequencies, ω_3/ω_1 , is given in (1), which is controlled by the magnetic

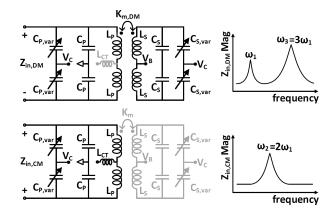


FIGURE 2. Transformer-based resonator under differential-mode (DM) and common-mode (CM) operation, and its magnitude of the input impedance respectively.

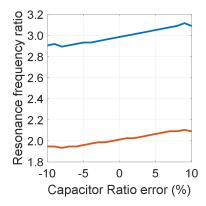


FIGURE 3. The resonant frequency ratio ω_2/ω_1 (red) and ω_3/ω_1 (blue) versus error of capacitor matching between transformer primary and secondary winding.

coupling factor, $k_{m,DM}$ and ratio X. The X is defined as $X = L_S C_{s,tot}/L_P C_{p,tot}$.

In the CM mode, the resonance only sees the CM inductance $L_P + 2L_{CT}$ and CM capacitor $C_{P,tot}$ on the primary winding, due to low magnetic coupling. L_{CT} is the inductance on the center tap connection. The CM resonant frequency is $\omega_2^2 = 1/(L_P + 2L_{CT})C_{P,tot}$. The ratio between CM resonant frequency ω_2 and DM fundamental frequency ω_1 is in (2). In the CM mode, the second harmonic components are forced to flow into the resistive path of the tank by having a tank impedance peak at the second harmonic frequency. In this way, it reduces: (i) flicker noise up-conversion, (ii) the DC value of the effective ISF [15], (iii) the close-in PN degradation by varactor nonidentities.

However, as shown in (1) and (2), class- F_{23} operation depends on the parameters of L_P , L_{CT} , X. Therefore it is very sensitive to mismatch between these parameters. The sensitivity of resonance frequency ratio ω_2/ω_1 and ω_3/ω_1 to capacitance mismatch between the primary and secondary winding is shown in Fig. 3. Therefore, the realization of the

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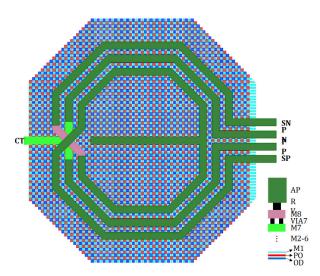


FIGURE 4. The layout of the transformer with proposed patterned shielding using M1, PO and OD layer.

transformer and capacitor bank is highly critical.

$$\left(\frac{\omega_3}{\omega_1}\right)^2 = \frac{1 + X + \sqrt{1 + X^2 + X(4k_{m,DM}^2 - 2)}}{1 + X - \sqrt{1 + X^2 + X(4k_{m,DM}^2 - 2)}} = 9 \quad (1)$$

$$\left(\frac{\omega_2}{\omega_1}\right)^2 = \frac{L_p C_{p,tot} + L_s C_{s,tot}}{(L_p + 2L_{CT})C_{p,tot}} = \frac{(1+X)L_p}{L_p + 2L_{cp}} = 4$$
 (2)

III. REALIZATION OF TRANSFORMER-BASED LC TANK

A. TRANSFORMER REALIZATION

Realization of the transformer with a turn ratio of 1:2 is shown Fig. 4. Due lacking the ultra-thick metal layer, the transformer was constructed by stacking the aluminum layer (AP layer) on top of the top copper layer (M_8 layer) to increase the metal thickness and reduce metal line resistance. The metal width is $10~\mu m$ for the primary and secondary winding, and the gap is kept at $8~\mu m$. A customized pattern shielding with M_1 , OD and PO layers are placed on top of the substrate to terminate the electric field and provide better shielding from the substrate to further improve its Q factor.

The simulated transformer performance is shown in Fig. 5. The performance is compared between using different shielding patterns, one with the proposed shielding pattern on M_1 , OD and PO layers, and the other is using shielding pattern on M_1 layer only. In differential mode, the primary and secondary inductance are around 0.5 nH and 1.2 nH, respectively. The quality factor at 8 GHz of the primary and secondary winding are 11.6 and 15.6, respectively. The coupling factor is 0.64. Compared with shielding using M_1 layer only, the transformer with proposed pattern shielding achieves a higher quality factor over a larger bandwidth, without affecting the inductor value and coupling factor. Under common-mode operation, the inductance on the primary winding center-tap is modelled precisely to the point

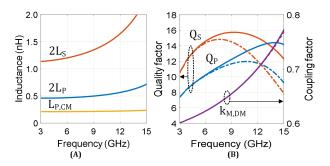


FIGURE 5. Transformer primary and secondary (a) inductance in CM and DM excitation (b) inductance quality factor and coupling factor in DM excitation, solid lines refer to shielding with M1, OD and PO, dashed lines refer to shielding with M1 only.

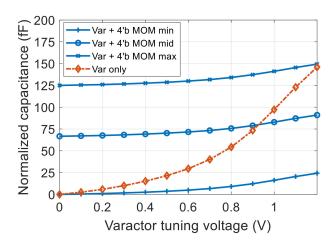


FIGURE 6. Comparison of capacitance tuning range between a capacitor bank of varactor and 4-bit MoM capacitor array, and a varactor bank.

where decoupling capacitors are placed. The common-mode inductance on the primary winding is around 0.2 nH.

B. CAPACITOR BANK REALIZATION

The realization of the capacitor bank should be considered together with the transformer characteristics to meet (1) and (2) for class- F_{23} operation, while at the same time to achieve a wide tuning range of oscillation frequency. The varactor effective capacitance not only depends on the tuning voltage, but also on the oscillation waveform. The varactor nonideality leads to two undesired side affects. Firstly, the matching between the varactor capacitance on different transformer windings is sensitive to the different oscillation waveform on the two windings. Secondly, it also introduces AM-FM conversion. Both side effects degrade the oscillator phase noise.

In order to reduce these side affects, a small varactor with a small tuning range of 25 fF is used on the primary side. A 4-bit binary-weighted MoM capacitors is used in parallel with the varactor to have a large tuning range of oscillation frequency. The LSB MoM capacitor is 18 fF. Fig. 6 shows the comparison of normalized capacitance tuning range between the solution of using capacitor bank of varactor-and-MoM

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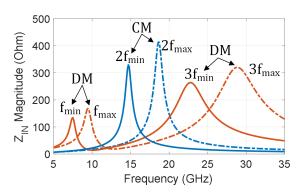


FIGURE 7. Transformer-based tank input impedance magnitude over oscillator tuning range frequency.

capacitors, and using varactor bank only. To achieve the same capacitance tuning range, the varactor bank consists of multiple small varactor units and shows strongly nonlinear capacitance tuning behavior. The capacitor bank however, is more linear as only one small varactor unit is used. Therefore, it is less sensitive to varactor mismatch due to the dependence on oscillation waveform. Furthermore, the phase noise degradation due to varactor AM-FM conversion is much alleviated. With this combination, the quality factor of the capacitor array is kept above 30 at 8 GHz for the whole tuning range. Therefore the quality factor of the LC tank is mostly limited by the quality factor of the transformer.

In order to meet class- F_{23} operation condition, the capacitance ratio between the primary and the secondary winding is kept as 1.8. As the transformer and capacitor bank characteristics have been settled, the simulated tank impedance over the tuning range is given in Fig. 7. The minimum and maximal resonant frequencies are 7.5 GHz and 9.4 GHz, respectively. The accuracy of the ratio between resonance frequencies is limited by the matching of varactor and MoM capacitance between transformer windings, as well as transformer characteristics to meet (1) and (2). Ideally, the varactor on the secondary winding could use a separate tuning voltage for a perfect matching for class- F_{23} operation.

IV. MEASUREMENT

The proposed class- F_{23} VCO is implemented in a 40-nm CMOS technology without an ultra-thick metal layer. The g_m devices are thick-oxide devices to handle the large voltage swing at the gate and drain node of the cross-coupled pair. The current source is implemented with a resistor at the drain to further reduce the flicker noise contribution to phase noise conversion at the close-in region. The center tap of the primary winding is connected to the supply, and the center tap of the secondary winding is connected to the bias voltage. The varactors on the transformer primary and secondary winding are connected to the same tuning voltage for simplicity. The oscillator is followed by a resistor-feedback buffer and a /4 divider. It drives the output 50 Ω load by a differential buffer. The die micrography is shown in Fig. 8 and the core die area is 0.1 mm².

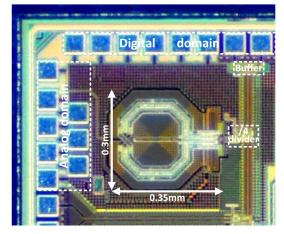


FIGURE 8. Die micrography of the proposed F_{23} oscillator with a on-chip /4 divider.

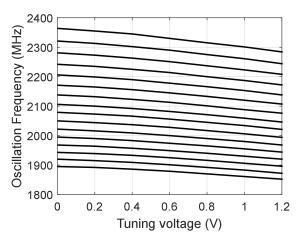


FIGURE 9. Measured oscillator tuning range with a on-chip /4 divider.

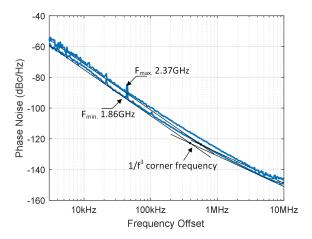


FIGURE 10. Measured phase noise at f_{min} and f_{max} with a on-chip /4 divider.

The results are measured by the Keysight E5052A signal source analyzer after on-chip /4 divider and buffer circuits.

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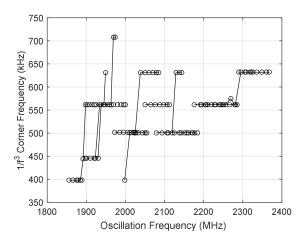


FIGURE 11. Measured 1/f₃ corner frequency over analog and digital tuning range.

The measured tuning range over the 4-bit digital steps and the analog tuning range is shown in Fig. 9. After /4 divider, the measured oscillator tuning range is from 1.85 to 2.37 GHz. The oscillator core is from 7.4 to 9.48 GHz. The current consumption of the core oscillator is 9.8 mA from a 1.2 V supply.

The measured phase noise is shown in Fig. 10 at the minimum and maximum oscillation frequency, after /4. At the minimum oscillation frequency, the measured phase noise at 100 kHz, 1 MHz and 10 MHz offset are -105, -131 and -151 dBc/Hz, achieving a FoM of 180, 185 and 186 dB/Hz, respectively. The 1/f₃ corner frequency is 400 kHz. At the maximum oscillation frequency, the phase noise at 100 kHz, 1 MHz, and 10 MHz offset are -101, -127 and -148 dBc/Hz, achieving a FoM of 178, 184, and 185 dB/Hz, respectively. The 1/f₃ corner frequency is 632 kHz.

The measured $1/f_3$ corner frequency over the entire digital and analog tuning range is shown in Fig. 11. The 1/f₃ corner frequency is mostly between 400 kHz and 632 kHz across the whole tuning range. It is limited by the mismatch between inductance and capacitance characteristics between the primary and secondary windings. This can be caused by the imperfect EM modeling of varactor mismatch, layout matching, or parasitic capacitance. The solid line in Fig. 11 shows some of the 1/f₃ corner frequencies experience abrupt changes during the analog tuning range, while most of them are constant. This result verifies the concept in most conditions that by using the combination of a small varactor unit and MoM capacitor array, the capacitance tuning range is linearized so that capacitance matching is accurate, and varactor AM-FM conversion is much alleviated. Ideally, a separate varactor tuning voltage can be used to fine tune the capacitance ratio to further reduce the 1/f₃ corner frequency.

Table 1 compares the measured performance with other recent works on oscillators. This VCO work achieves good phase noise, low $1/f_3$ corner frequency and a wide tuning

TABLE 1. Comparison of state-of-the-art low phase noise oscillators.

Ref	[12]	[13]	[16]	This work*
Topology	1/f Noise Filtering	Class-F	Class-D	Class-F ₂₃
CMOS Technology(nm)	350	65	65	40
Thick metal	Yes	Yes	Yes	No
Tuning range (%)	13.7	25	45%	25
Core power (mW)	16.2	15	6.8	11.8
Frequency (GHz)	1.64	7.4	4.8	1.85-2.381 (/4)
				7.4-9.48(Core)
PN @100kHz (dBc/Hz)	-109	-98.5	-91	-105/-101
PN @1MHz (dBc/Hz)	-129	-125	-119	-131/-127
PN @10MHz (dBc/Hz)	N.A.	-147	-143.5	-151/-148
FoM @100kHz (dB)	182.5	184.1	178.6	180/178
FoM @1MHz (dB)	182.5	190.6	186.6	185/184
FoM @10MHz (dB)	N.A.	192.6	191.1	186/185
FoM _T † @10MHz (dB)	185.2	200.2	205.3	194/193
1/f ₃ corner (kHz)	21	700	2100	400/632
Core area (mm ²)	N.A.	0.12	0.12	0.1

^{*} Oscillator's frequency and phase noise are measured after on-chip /4 divider.

range. It proves that VCO can benefit from class- F_{23} operation to achieve low phase noise and low $1/f_3$ corner frequency by novel design and implementation of a transformer-based LC tank, even without the ultra-thick metal layer.

V. CONCLUSION

This paper presents an 8 GHz VCO with class-F₂₃ in a 40-nm digital CMOS technology. The class-F₂₃ operation was enabled by having a transformer-based tank with auxiliary resonant frequency at 2rd harmonic in CM mode and at 3rd harmonic in DM mode in order to achieve low phase noise and low 1/f₃ corner frequency. A patterned shielding and stacked metal method are applied to increase the on-chip inductor quality factor. The resonant frequency ratio is accurate controlled by the capacitor matching on the primary and secondary of the transformer. With the mixed capacitor bank architecture, the 1/F₃ is 400 kHz. The VCO with a /4 divider buffer prototype measured a PN of -131 dBc/Hz at 1 MHz offset and -151 dBc/Hz at 10 MHz offset. The measured frequency is from 1.85 to 2.37 GHz with on-chip /4 divider, while the oscillator core covers from 7.4 to 9.48 GHz. With on-chip /4 divider, its FoM_T reach a 194, which kept a stateof-art performance.

ACKNOWLEDGMENT

(Kuangyuan Ying and Hao Gao are co-first authors.)

REFERENCES

- [1] A. Nejdel, M. Abdulaziz, M. Tormanen, and H. Sjoland, "A positive feedback passive mixer-first receiver front-end," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2015, pp. 79–82.
- [2] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1348–1360, May 2018.

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[†] $FoM_T = |PN| + 20\log_{10}(f_0/\Delta f)(TR/10) - 10\log_{10}(P_{DC,mw})$



- [3] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M.-C. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Jun. 2015.
- [4] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M.-C. F. Chang, "A blocker-tolerant inductor-less wideband receiver with phase and thermal noise cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2948–2964, Dec. 2015.
- [5] T. Zhang, Y. Chen, C. Huang, and J. C. Rudell, "A low-noise reconfigurable full-duplex front-end with self-interference cancellation and harmonic-rejection power amplifier for low power radio applications," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf.*, Sep. 2017, pp. 336–339.
- [6] E. J. G. Janssen, D. Milosevic, and P. G. M. Baltus, "A 1.8 GHz amplifier with 39 dB frequency-independent smart self-interference blocker suppression," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 97–100
- [7] K. Ying, H. Gao, D. Milosevic, and P. Baltus, "A nonlinear transfer function based receiver for wideband interference suppression," *J. Sensors*, vol. 2017, pp. 1–15, Jan. 2017.
- [8] K. Ying, C. A. M. C. Junio, B. Wang, D. Milosevic, H. Gao, and P. Baltus, "A reconfigurable receiver with 38 dB frequency-independent blocker suppression and enhanced in-band and linearity and power efficiency," in Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC), Sep. 2018, pp. 74–77.
- [9] H. Darabi, H. Jensen, and A. Zolfaghari, "Analysis and design of small-signal polar transmitters for cellular applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1237–1249, Jun. 2011.
- [10] B. Soltanian and P. Kinget, "AM-FM conversion by the active devices in MOS LC-VCOS and its effect on the optimal amplitude," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2006, pp. 108–112.
- [11] E. Hegazi and A. A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.
- [12] A. Ismail and A. A. Abidi, "CMOS differential LC oscillator with suppressed up-converted flicker noise," in *IEEE Int. Solid-State Circuits Conf.* (ISSCC) Dig. Tech. Papers, vol. 1, Feb. 2003, pp. 98–99.
- [13] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.
- [14] C. C. Lim, H. Ramiah, J. Yin, P.-I. Mak, and R. P. Martins, "An inverseclass-F CMOS oscillator with intrinsic-high-Q first harmonic and second harmonic resonances," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3528–3539, Dec. 2018.
- [15] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [16] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.



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