

A 2-D-Material FET Verilog-A Model for Analog Neuromorphic Circuit Design

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Abstract—We present a charge-based Verilog-A model for 2-D-material (2DM)-based field-effect transistors (FETs) with application in neuromorphic circuit design. The model combines the explicit solution of the drift-diffusion transport and electrostatics, including Fermi–Dirac statistics. The Ward–Dutton linear charge partitioning scheme is then employed for terminal charges and capacitance calculations. The model accurately predicts the electrical behavior of experimental MoS₂ FETs, and it is applied to simulate neuromorphic-circuit building blocks, including a floating-gate (FG) current-mirror (CM) vector-matrix multiplier (VMM), extracting the effective number of bits under different operation conditions.

Index Terms—2-D materials (2DMs), current mirror (CM), explicit compact model, neural network, vector-matrix multiplier (VMM), Verilog-A model.

I. INTRODUCTION

TWO-DIMENSIONAL materials (2DMs) offer the opportunity to develop ultrathin-channel transistor technology with reduced low-power requirements due to their atomic thickness, which results in optimal electrostatic gate control over short-channel effects in ultrascaled geometries [1]. Furthermore, they show mechanical flexibility [2] and good mobility harnessing the development of flexible electronic systems. These outstanding properties have attracted the wide and long-time attention of the device research community [1],

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[2], [3], [4], [5], [6], [7], [8], recently and more particularly for their application in floating-gate (FG) architectures enabling brain-inspired computation [9].

However, in order to materialize the research accomplishments into industrial technological realizations, it is necessary to assess the circuit and system-level performance of 2DM-based field-effect transistors (FETs), which demands industry standard compatible models. A device model must be: 1) accurate by including all the important physics and 2) robust to ensure circuit simulation convergence in as small as possible computation burden and time. Several SPICE models for 2DM-based transistors have already been proposed [10], [11], [12], [13], [14], [15], but in many cases, they use complicated numerical methods to calculate the electrical parameters [14], which increases computation time. Sometimes, the model accuracy is traded off against simplifications such as ballistic transport approximation [11], [12] that is not valid for long-channel devices or assuming a Maxwell–Boltzmann (MB) distribution of charge carriers [13], [14] that is inaccurate for 2DM-FETs operating in strong inversion. Dynamic regime behavior descriptions of 2DM-based FETs are rarely available in the literature. In [15], a first large-signal model describing terminal charges and capacitances in 2DM-based FETs was presented. This model used an iterative numerical algorithm to solve the chemical potential and eventually obtain the charges and capacitances. Although the model showed a very good agreement with experimental results and it is the first of its class, its computational speed might be compromised due to the iterative numerical calculations that are not suitable for large circuit simulations.

Here, we present an explicit, i.e., with fully analytical noniterative solution for the terminal charge and capacitances implemented in Verilog-A for 2-D channel material FETs, which is charge-based and leverages the results presented by some of the authors of this work in [16], while considering 2-D density of states and Fermi–Dirac statistics, self-consistently solved with a drift-diffusion transport. It is assumed that the source and drain contacts are ohmic and that Schottky barrier injection at the contacts is neglected. The terminal charges are calculated using the Ward–Dutton linear charge partitioning approach, and the intrinsic capacitances are calculated by differentiating the terminal charge with respect to the corresponding terminal voltages. The model is validated against both in-home experimental MoS₂ transistor data [16], [17] and

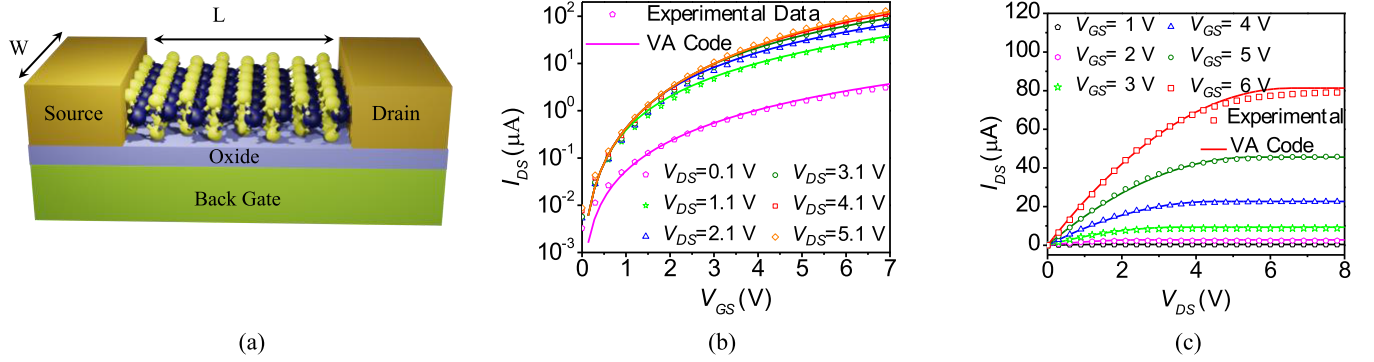


Fig. 1. (a) Schematic of the 2DM-based FET and Verilog-A model. (b) Transfer and (c) output characteristics calibrated against experimental data [11].

numerical calculation results. Finally, as an application of the developed model, we have simulated an FG CM multiplier implementing a vector-matrix multiplier (VMM) [18], a fundamental block of analog neuromorphic circuits [19].

This article is organized as follows. Section II presents the formulation of the FET model. The terminal charges and capacitances, calculated using the Ward–Dutton linear charge partitioning scheme, are discussed in Section III. In Section IV, an FG CM is implemented to demonstrate the VMM cell operation. Final remarks and conclusions are drawn in Section V.

II. DRAIN CURRENT MODEL

A schematic of the device structure considered to model the 2-D material-based FET is presented in Fig. 1(a). It is a back-gate MoS₂ transistor, where source and drain are patterned on the top of the MoS₂ channel, that is separated from a back gate through a dielectric gate oxide. Electron concentrations in the channel region can be expressed as [16]

$$n = n_0 + \Delta_n \quad (1)$$

where n_0 and Δ_n are the equilibrium electron concentration and Newton correction in electron concentration, respectively, as presented in Appendix A. The total drain current can be calculated using the electron and hole carrier concentration as suggested in [16] as follows:

$$I = W\mu_p \frac{p_q^2 kT}{L} \left[\left(\frac{p^2}{2n_b p_q^2} \right) + \frac{1}{p_q} \left(\frac{p^2}{2p_q^2} - e^{-\frac{p}{p_q}} \right) \right]_{p_s/p_q}^{p_d/p_q} - W\mu_n \frac{n_q^2 kT}{L} \left[\left(\frac{n^2}{2n_b n_q^2} \right) + \frac{1}{n_q} \left(\frac{n^2}{2n_q^2} - e^{-\frac{n}{n_q}} \right) \right]_{n_s/n_q}^{n_d/n_q} \quad (2)$$

where $n_s(p_s)$ and $n_d(p_d)$ are the electron (hole) concentrations at the source and drain sides, respectively. n and p are electron and hole concentration in the channel, quantity $n_q(p_q)$ is defined as $D_n K T (D_p K T)$ being $D_n (D_p)$ electron (hole) diffusion coefficient. μ_p and μ_n are the gate-bias-dependent mobility of the electrons and holes defined as $\mu_{n/p} = \mu_{n0/p0} (V_{GS} - V_T)^\alpha$, with the fitting parameters $\mu_{n0/p0}$ and $\alpha (=1.354)$. In (2), current contribution due to both electron and hole carrier concentration is presented accounting for

TABLE I
DEVICE PARAMETERS USED FOR VALIDATION
WITH EXPERIMENTAL RESULTS

Parameters	Value
L (μm)	5
W (μm)	20
ϵ_{ox} (ϵ_0)	9
t_{ox} (nm)	30
D_n ($\text{eV}^{-1} \text{cm}^{-2}$)	3.45×10^{12}
ϕ_M (eV)	4.2
χ_s (eV)	4.33
N_D^+ (cm^{-2})	1×10^{10}
E_g (eV)	1.8
μ_{n0} (cm^2/Vs)	2

the most general case. However, in the calculations for MoS₂-based FET, the contribution of hole carriers in the total drain current is negligible due to the large bandgap, E_g (1.8 eV) of monolayer MoS₂ channel. As a consequence, we have neglected the contribution of holes in current and capacitance calculations. The I_D – V_{DS} and I_D – V_{GS} characteristics obtained from the Verilog-A model have been fit against the MoS₂ FET experimental device from [16] and [17] in Fig. 1(b) and (c). We fixed all the geometrical and device parameters to the experimental ones, except for the metal work function (χ_s), electron diffusion coefficient, and channel mobility that were trimmed to get the best fitting. Unless otherwise stated, the geometrical and device parameters considered in the model are reported in Table I and are consistent with [16]. It can be observed that the Verilog-A model accurately predicts both the transfer [Fig. 1(b)] and the output [Fig. 1(c)] characteristics obtained from experiments.

III. CAPACITANCE MODEL

The total gate capacitance (C_{GG}), gate-to-source capacitance (C_{GS}), and gate-to-drain capacitances (C_{GD}) are crucial for transient simulations. These capacitances can be calculated by differentiating the gate, source, and drain terminal charges with respect to terminal voltages. The source, drain, and gate terminal charges can be calculated using the Ward–Dutton linear charge partitioning scheme as

$$Q_g = -W \int_0^L Q_n(x) dx \quad (3)$$

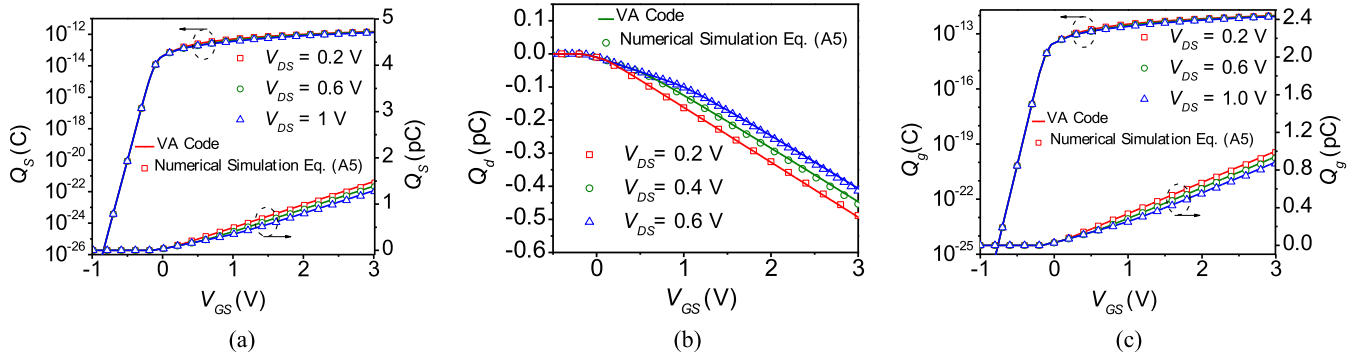


Fig. 2. Terminal charges at (a) source, (b) drain, and (c) gate terminal versus V_{GS} characteristics obtained using Verilog-A code and numerical calculation using (A5).

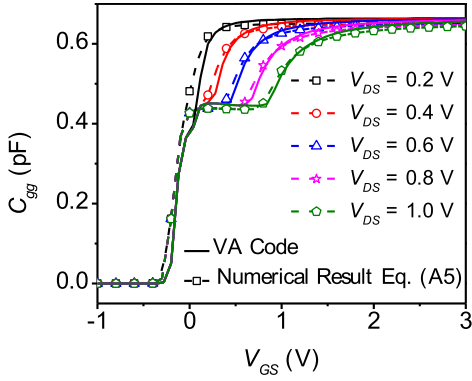


Fig. 3. Total gate capacitance versus V_{GS} obtained from Verilog-A code and numerical calculation using (A5).

$$Q_d = W \int_0^L \frac{x}{L} Q_n(x) dx \quad (4)$$

$$Q_s = -(Q_g + Q_d) = w \int_0^L \left(1 - \frac{x}{L}\right) Q_n(x) dx \quad (5)$$

where $Q_n(x)$ is the channel charge at a point x , which can be calculated invoking current continuity (i.e., $I_{ds} = I_{xs}$), leading to the expressions for $Q_n(x)$. For $n_s < 0.1$, the channel charge can be approximated by expression as presented in (6), as shown at the bottom of the next page, that results in terminal charges as expressed in (A12)–(A14) of Appendix B. In (6), $C_{dq} = q^2 g_v g_s (m^*/2\pi \hbar^2)$ is the degenerated quantum capacitance [14] and $C_g = (C_{ox}^{-1} + C_{dq}^{-1})^{-1}$ is the total gate capacitance of the transistor. g_v , g_s , and m^* are the valley degeneracy, the spin degeneracy, and the electron effective mass in the conduction band, respectively. For $n_s > 0.1$, the channel charge can be approximated by expression (7), as shown at the bottom of the next page, that results in terminal charges as expressed in (A15), (A16), and (A17) of Appendix B.

A detailed derivation of (6) and (7) is presented in Appendix B. The piecewise model for terminal charges obtained from (6) and (7) is not suitable for SPICE modeling as derivatives of this kind of functions are discontinuous leading to convergence issues, artifacts, and undesired harmonics in the output signals. To overcome this issue, it is common practice to use smoothing functions that result in a soft transition between two regions. The expressions for

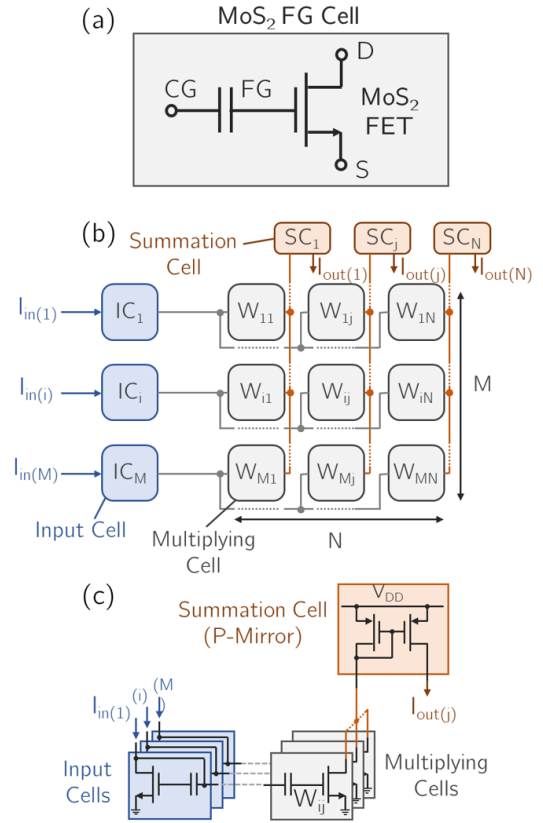


Fig. 4. (a) Equivalent circuit of used FG transistor. (b) Block diagram of the analog VMM architecture. (c) FG CM circuit implementation of the VMM.

source (Q_s), drain (Q_d), and gate (Q_g) terminal charges using smoothing functions are presented in (A9)–(A11) in Appendix B. Once the terminal charges have been obtained, the intrinsic capacitances are calculated by differentiating the terminal charges with respect to the corresponding terminal voltages. The charges at the terminals obtained from (A9)–(A11) are compared with numerical results using (A5) for the same device and geometrical parameters in Fig. 2. It can be observed that the Verilog-A compact model can accurately predict the terminal charges. The C_{GG} versus V_{GS} characteristics is compared in Fig. 3 with the results obtained by the numerical solution of implicit equations (A5)

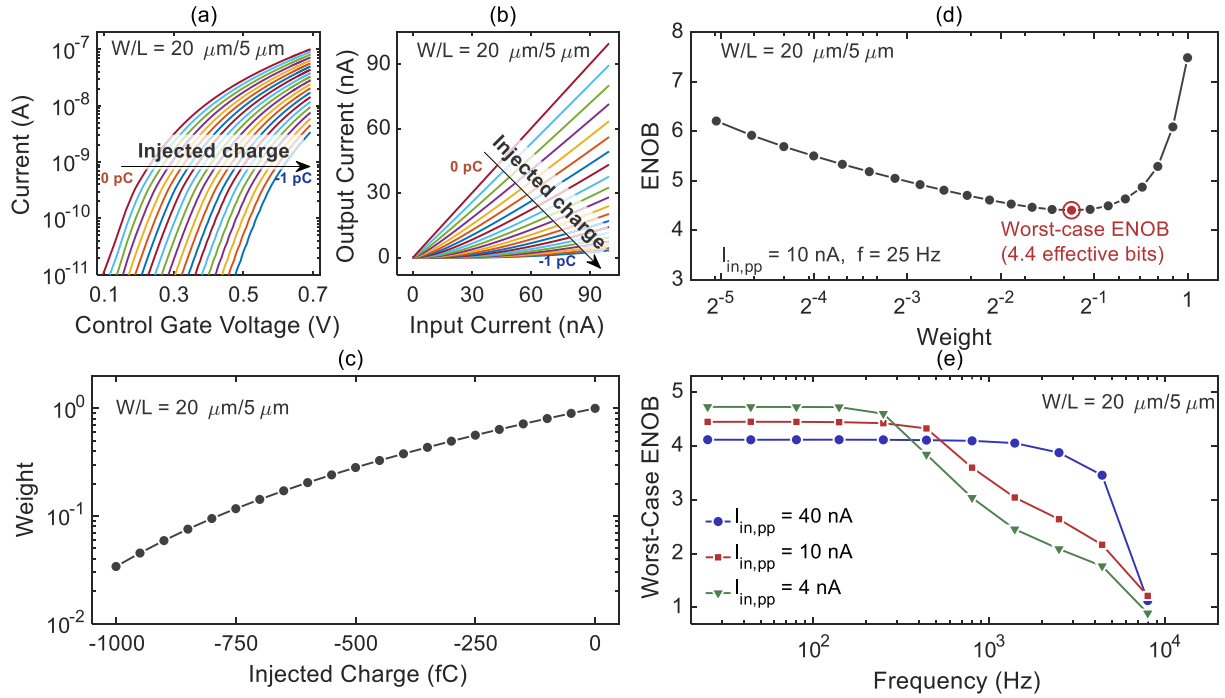


Fig. 5. (a) FG cell transfer characteristics for different injected charge conditions (from 0 to -1000 fC) and corresponding (b) FG CM I_{out} versus I_{in} characteristics. (c) Extracted weight as a function of the charge injected in the FG. (d) ENOB of the CM VMM cell extracted for different weights. (e) Worst case ENOB as a function of the input current waveform frequency. FG cell $W/L = 20/5 \mu\text{m}$.

again with very good agreement. The results obtained using the model presented in this article are compared against the model presented in [15] with the same device parameters that are presented in Appendix C. The validation of the model with large signal ac measured data is presented in Appendix C, which shows the capability of the model to predict the waveform of five-stage ring oscillator circuit.

IV. CIRCUIT-LEVEL SIMULATIONS: CM VMM

Next, we test the Verilog-A 2DM-based FET model within brain-inspired circuit simulations, performed in the Cadence Virtuoso IC 6.1.7 design environment. As a vehicle circuit, we have selected the analog VMM cell, which can be appointed as a relevant building block of analog neuromorphic circuits, realized with FG CMs [18]. It is assumed that the transistor cell shown in Fig. 1(a) is enhanced with an FG, which is separated from an external control gate (CG) by means of an additional oxide layer, realizing the FG transistor basic cell in

Fig. 4(a). The concept of the VMM architecture implementation using FG CM circuits is presented in Fig. 4(b) [18]. The arithmetic operation implemented by a VMM is the multiply-and-accumulate operation (MAC). In any single cell of the matrix, a multiplication between the row signal—encoded as an input current—and the cell weight—programmed by means of the charge stored in the FG—is performed. This is simply realized considering that the output current of any current-mirror (CM) cell is the result of the product between the input current and the CM magnification factor. The accumulation, instead, is trivially obtained by summing up all the currents in the same column, connected to the same node, by relying on Kirchhoff's current law. Finally, a p-type CM [summation cell in Fig. 4(c)] is exploited to provide the output current with the proper direction $I_{out(j)}$ as [18]

$$I_{out(j)} = \sum_i^M I_i w_{ij}. \quad (8)$$

$$Q_{0n}(x)$$

$$= qC_{ox} \left[\left\{ -\frac{n_q}{C_{dq}} + \sqrt{\left(\frac{n_q}{C_{dq}}\right)^2 - \frac{2}{C_{ox}} \left[\frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_s}{n_q}\right) - 1 \right\} - \frac{n_s^2}{2C_g} \right] + \frac{x}{L} \left[\frac{(n_s^2 - n_d^2)}{2C_g} + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]} \right\} \right] \quad (6)$$

$$Q_{1n}(x)$$

$$= \sqrt{q \left[n_s^2 - \frac{2C_g n_q^2}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) \right] - \frac{x}{L} \left[(n_s^2 - n_d^2) + \frac{2C_g n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]} \quad (7)$$

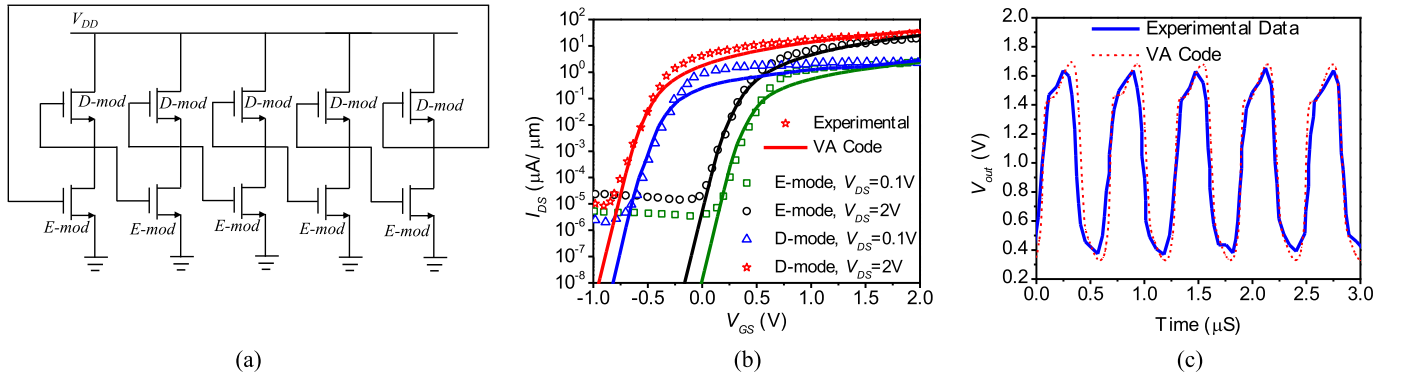


Fig. 6. (a) Ring oscillator circuit considered for ac validation [15]. (b) Transfer characteristics of E-mode and D-mode nMOSFETs. (c) Output waveform of ring oscillator circuit.

Fig. 5 reports the functionality of an FG CM, realized with a nominal device size of $L = 5 \mu\text{m}$, $W = 20 \mu\text{m}$, and a coupling oxide capacitor (between the FG and the CG) of $2.6 \mu\text{F}/\text{cm}^2 \times W \times L$, as obtained by an additional 10-nm-thick oxide with the same footprint of the transistor channel. In real FG devices, the charge can be injected/removed from the FG by relying on physical tunneling phenomena and hot electron injection in the oxide region [20], [21]. In the simulations, we have emulated the injection of the charge (q_{inj}) by using a pulse current source at the FG to set the different weight conditions as in [18]. The obtained FG transfer characteristics, at $V_{DS} = 400 \text{ mV}$, are shown in Fig. 5(a). In Fig. 5(b), the I_{out} versus I_{in} characteristics of a single CM cell is reported for the same injected charge conditions as shown in Fig. 5(a), and the extracted relation between the injected charge and the corresponding CM magnification factor (i.e., the weight) is reported in Fig. 5(c).

Noise and nonlinearity, which are typical nonidealities of analog circuits, can degrade the precision of the analytical operation described by (8). In order to study the precision of the MAC analog operation realized with our cell, based on the 2DM-FET model, we have exploited the methodology proposed in [18], based on the characterization of the signal-to-noise-and-distortion ratio (SINAD), which can be converted into an equivalent number of bits (ENOBs) of the arithmetic operation, according to the equation $\text{ENOB} = (\text{SINAD} - 1.76) / 6.02 - \log_2(\text{weight})$ [18]. The SINAD (and thus the ENOB) is extracted by means of a fast Fourier transform (FFT) of the output current waveform, as obtained in a transient analysis of the FG CM VMM cell stimulated with an input sine waveform exploring the full input scale, with a peak-to-peak current $I_{in,pp}$ of 10 nA and a frequency f of 25 Hz. This extraction is performed for different weight conditions as in the example provided in Fig. 5(d), which shows the worst case condition for the precision of the analog operation in the explored weight range.

Finally, we have plotted the extracted worst case ENOB as a function of the frequency of the input waveform, for three $I_{in,pp}$ values of 4, 10, and 40 nA in Fig. 5(e). By lowering the input current scale from 40 toward 4 nA, there is an increase of the low-frequency worst case ENOB, but at the cost of a lower bandwidth. In fact, in order to guarantee an ENOB higher than

4 bits in the whole range of possible weights, a maximum bandwidth of 0.4, 0.5, and 1.5 kHz can be accepted for $I_{in,pp}$ of 4, 10, and 40 nA, respectively.

V. CONCLUSION

A 2DM-based FET Verilog-A explicit model, including both $I-V$ and $C-V$ characteristics, has been developed. The model accurately predicts the characteristics of experimental MoS₂ FETs [15] and has been exploited to design a programmable analog neuromorphic cell for a VMM based on an FG-CM structure, which has been analyzed by means of the extraction of the SINAD and ENOB figures of merit. The designed FG CM can perform the MAC operations, that is, the multiplication of a vector of input currents with programmable weights and subsequent accumulation, with an ENOB higher than 4 bits, a precision can be maintained up to a frequency of 1.5 kHz with a proper design optimization. In conclusion, we have demonstrated that the developed 2DM-FET model can be exploited to simulate and predict the performance of complex brain-inspired circuits, by exploiting a commercial circuit simulation platform such as Cadence Virtuoso IC.

APPENDIX A

CARRIER CONCENTRATION IN MOS₂ CHANNEL

The carrier concentration of electrons (holes) in the MoS₂ channel material can be expressed as a sum of Newton's correction factor Δ_n (Δ_p) and equilibrium electron (hole) concentration n_0 (p_0) as introduced in [16]

$$n = n_0 + \Delta_n \quad (\text{A1})$$

$$p = p_0 + \Delta_p \quad (\text{A2})$$

where

$$n_0 = n_b \times W \left(\frac{n_q}{n_b} e^{\frac{(qV_{GS} - qV_T + E_f)}{\phi_{th}}} \right)$$

$$\Delta_n = -\frac{r_n}{r'_n} \left(1 + \frac{0.5r_n r''_n}{r_n'^2} \right)$$

$$p_0 = p_b \times W \left(\frac{p_q}{p_b} e^{-\frac{(qV_{GS} - qV_T + E_f + E_g)}{\phi_{th}}} \right)$$

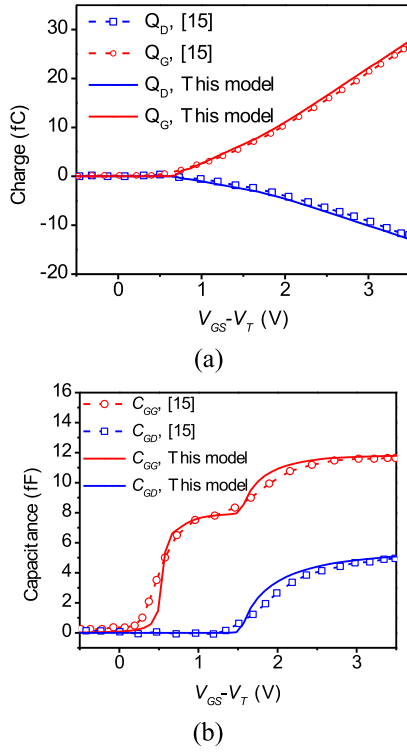


Fig. 7. Comparison of our model with the model presented in [15]. (a) Terminal charge. (b) Capacitance characteristics at a $V_{DS} = 1$ V.

$$\Delta_p = -\frac{r_p}{r'_p} \left(1 + \frac{0.5r_p r''_p}{r'^2_p} \right)$$

where r_n and r_p are the parameters defined as [16]

$$r_n = \frac{C_{ox}}{q} \left(V_{GS} - V_T + \frac{E_f}{q} \right) - n_0 + p_q \ln \left(1 + \frac{e^{-E_g/\phi_{th}}}{e^{n_0/n_q} - 1} \right) - n_b \ln \left(e^{n_0/n_q} - 1 \right)$$

$$r_p = \frac{C_{ox}}{q} \left(V_{GS} - V_T + \frac{E_f}{q} \right) + p_0 - n_q \ln \left(1 + \frac{e^{-E_g/\phi_{th}}}{e^{p_0/p_q} - 1} \right) + p_b \ln \left[\left(e^{p_0/p_q} - 1 \right) + \frac{E_g}{\phi_{th}} \right]$$

$$n_b = p_b = \frac{C_{ox}\phi_{th}}{q}, \quad n_q = D_n\phi_{th} \quad \text{and} \quad p_q = D_p\phi_{th}$$

$$V_T = \phi_M - \chi_s - \frac{qN_d^+}{C_{ox}}$$

where E_f is the Fermi level of the electrons in the channel; V_T , C_{ox} , and ϕ_{th} are the threshold voltage, back-gate oxide capacitance, and thermal voltage, respectively; ϕ_M , χ_s , and N_d are the gate metal work function, channel electron affinity, and channel doping concentration, respectively; and D_n and D_p are the electron and hole diffusion coefficients, respectively.

TABLE II
DEVICE PARAMETERS FOR E- AND D-MODE DEVICES

Parameters	Value
L (μm)	1
W (μm)	4
ϵ_{ox} (ϵ_0)	25
t_{ox} (nm)	18
Dn ($\text{eV}^{-1} \text{cm}^{-2}$)	3.45×10^{12}
$\phi_M, D\text{-mod}$ (eV)	3.8
$\phi_M, E\text{-mod}$ (eV)	4.6
χ_s (eV)	4.33
N_D^+ (cm^{-2})	1×10^{10}
E_g (eV)	1.8
$\mu_{n0, D\text{-mod}}$ (cm^2/Vs)	14
$\mu_{n0, E\text{-mod}}$ (cm^2/Vs)	11.2

APPENDIX B TERMINAL CHARGE CALCULATION

The channel charge at any point x in the channel can be calculated by invoking the current continuity in the channel region. The expression for drain current is given as

$$I_{DS} = q^2 \frac{W}{L} \mu \left[\left(\frac{n_s^2 - n_d^2}{2C_g} \right) + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right] \quad (\text{A3})$$

$$I_D(x) = q^2 \frac{W}{x} \mu \left[\left(\frac{n_s^2 - n^2(x)}{2C_g} \right) + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n(x)}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]. \quad (\text{A4})$$

Since the current in the channel is the same at every point everywhere, we have $I_{DS} = I_D(x)$

$$\begin{aligned} & \frac{n_q^2}{C_{dq}} \exp\left(\frac{-n(x)}{n_q}\right) - \frac{n^2(x)}{2C_g} \\ &= \left[\frac{n_q^2}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) - \frac{n_s^2}{2C_g} \right] \\ &+ \frac{x}{L} \left[\left(\frac{n_s^2 - n_d^2}{2C_g} \right) + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]. \end{aligned} \quad (\text{A5})$$

As $n(x) \rightarrow \infty$, $\exp((-n(x))/n_q) \rightarrow 0$, (A4) reduces to (A5) as follows:

$$\begin{aligned} & n^2(x) \\ &= \left[n_s^2 - \frac{2C_g n_q^2}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) \right] \\ &+ \frac{x}{L} \left[\left(n_s^2 - n_d^2 \right) + \frac{2C_g n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]. \end{aligned} \quad (\text{A6})$$

Equation (A6) gives (7) of this article.

Equation (A5) can be written as follows:

$$\begin{aligned} & \frac{n_q^2}{C_{dq}} \left(1 - \frac{n(x)}{n_q} + \frac{n(x)^2}{n_q^2} - \frac{n(x)^3}{n_q^3} + \frac{n(x)^4}{n_q^4} - \dots \right) - \frac{n^2(x)}{2C_g} \\ &= \left[\frac{n_q^2}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) - \frac{n_s^2}{2C_g} \right] \\ &+ \frac{x}{L} \left[\left(\frac{n_s^2 - n_d^2}{2C_g} \right) + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]. \end{aligned} \quad (\text{A7})$$

As $n(x) \rightarrow 0 (< 0.1)$, we can neglect higher order terms of $n(x)$ [e.g., $n(x)^3$ and $n(x)^4$] and (E7) reduces to (E8) as

$$\begin{aligned} & \frac{n_q^2}{C_{dq}} \left(1 - \frac{n(x)}{n_q} + \frac{n(x)^2}{n_q^2} \right) - \frac{n^2(x)}{2C_g} \\ &= \left[\frac{n_q^2}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) - \frac{n_s^2}{2C_g} \right] \\ &+ \frac{x}{L} \left[\left(\frac{n_s^2 - n_d^2}{2C_g} \right) + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]. \end{aligned} \quad (\text{A8})$$

Solution of (A8) gives (6) of this article. As we mentioned in Section III, the piecewise model obtained using (6)–(7) is not suitable for SPICE modeling as discontinuities could result in convergence issues and undesired harmonics in the output waveforms. To overcome this issue, we have used smoothing function for a soft transition between two region expressions as

$$Q_s = \frac{Q_{0s}}{1 + \alpha e^{\beta(V_{GS} - V_T)}} + \frac{Q_{1s}}{1 + \alpha e^{-\beta(V_{GS} - V_T)}} \quad (\text{A9})$$

$$Q_D = \frac{Q_{0d}}{1 + \alpha e^{\beta(V_{GS} - V_T)}} + \frac{Q_{1d}}{1 + \alpha e^{-\beta(V_{GS} - V_T)}} \quad (\text{A10})$$

$$Q_G = \frac{Q_{0g}}{1 + \alpha e^{\beta(V_{GS} - V_T)}} + \frac{Q_{1g}}{1 + \alpha e^{-\beta(V_{GS} - V_T)}} \quad (\text{A11})$$

where Q_{0s} , Q_{1s} , Q_{0d} , Q_{1d} , Q_{0g} , and Q_{1g} are defined as in (A12)–(A17), shown at the bottom of the page, respectively.

APPENDIX C

LARGE-SIGNAL AC VALIDATION OF THE MODEL

To validate the ac capabilities of the model, we have simulated a five-stage ring oscillator as presented in Fig. 6(a) and validated the results against experimental results presented in [15] and [22]. The transfer characteristics of both E-mode (enhancement mode) and D-mode (depletion mode) nFET devices is presented in Fig. 6(b). To match the device characteristics, we have considered the same device geometrical parameters as the experimental device and adjusted mobility and gate metal work function (Table II). The output waveform is compared with experimental data in Fig. 6(c). It can be observed that the VA-model reproduces the experimental waveform accurately showing the capability of the model to perform ac simulations.

The terminal charge and capacitances obtained here are compared against model presented in [15] for the same device parameters in Fig. 7(a) and (b). The results show that the explicit closed-form model presented here matches the model presented in [15], which employs iterative numerical calculations.

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The Verilog-A code is available to the readers on demand.

$$Q_{0g} = \frac{WLC_{ox}n_q}{C_{dq}} + \frac{W}{6C_{ox}b} \left[\left(C_{ox}^2 \left(\frac{n_q}{C_{dq}} \right)^2 - 2C_{ox}a - 2C_{ox}bL \right)^{3/2} - \left(C_{ox}^2 \left(\frac{n_q}{C_{dq}} \right)^2 - 2C_{ox}a \right)^{3/2} \right] \quad (\text{A12})$$

$$\begin{aligned} Q_{0d} &= \frac{-WLC_{ox}n_q}{2C_{dq}} + \frac{W}{10C_{ox}^2Lb^2} \left[\left(C_{ox}^2 \left(\frac{n_q}{C_{dq}} \right)^2 - 2C_{ox}a - 2C_{ox}bL \right)^{5/2} - \left(C_{ox}^2 \left(\frac{n_q}{C_{dq}} \right)^2 - 2C_{ox}a \right)^{5/2} \right] \\ &+ \frac{W}{6C_{ox}^2Lb^2} \left[\left(C_{ox}^2 \left(\frac{n_q}{C_{dq}} \right)^2 - 2C_{ox}a - 2C_{ox}bL \right)^{3/2} - \left(C_{ox}^2 \left(\frac{n_q}{C_{dq}} \right)^2 - 2C_{ox}a \right)^{3/2} \right] \end{aligned} \quad (\text{A13})$$

$$Q_{0s} = -Q_{0g} - Q_{0d} \quad (\text{A14})$$

$$Q_{1g} = \frac{2}{3}WL \frac{\left(\left\{ n_s^2 - \frac{2n_q^2 C_{ox}}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) \right\} - \left[(n_s^2 - n_d^2) + \frac{2C_g n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right] \right)^{3/2} - \left\{ n_s^2 - \frac{2n_q^2 C_{ox}}{C_{dq}} \exp\left(\frac{-n_s}{n_q}\right) \right\}^{3/2}}{\left[(n_s^2 - n_d^2) + \frac{2C_g n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]} \quad (\text{A15})$$

$$Q_{1d} = -\frac{WL}{\left[(n_s^2 - n_d^2) + \frac{2C_g n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right]} \left(\frac{n_q^2 L^2}{3C_{dq}^2} + \frac{n_q L}{4C_{ox} C_{dq}} \right) \quad (\text{A16})$$

$$Q_{1s} = -Q_{1g} - Q_{1d}$$

$$\text{being } a = \left[\frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_s}{n_q}\right) - 1 \right\} - \frac{n_s^2}{2C_g} \right], \quad \text{and } b = \frac{1}{L} \left[\frac{(n_s^2 - n_d^2)}{2C_g} + \frac{n_q^2}{C_{dq}} \left\{ \exp\left(\frac{-n_d}{n_q}\right) - \exp\left(\frac{-n_s}{n_q}\right) \right\} \right] \quad (\text{A17})$$

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