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High-Performance Monolayer MoS_2 Field-Effect Transistors on Cyclic Olefin Copolymer-Passivated SiO_2 Gate Dielectric

Sirri Batuhan Kalkan, Emad Najafidehaghani, Ziyang Gan, Jan Drewniok, Michael F. Lichtenegger, Uwe Hübner, Alexander S. Urban, Antony George, Andrey Turchanin, and Bert Nickel**

Trap states of the semiconductor/gate dielectric interface give rise to a pronounced subthreshold behavior in field-effect transistors (FETs) diminishing and masking intrinsic properties of 2D materials. To reduce the well-known detrimental effect of SiO_2 surface traps, this work spin-coated an ultrathin (≈5 nm) cyclic olefin copolymer (COC) layer onto the oxide and this hydrophobic layer acts as a surface passivator. The chemical resistance of COC allows to fabricate monolayer MoS_2 FETs on SiO_2 by standard cleanroom processes. This way, the interface trap density is lowered and stabilized almost fivefold, to around 5×10^{11} cm^{-2} eV^{-1}, which enables low-voltage FETs even on 300 nm thick SiO_2. In addition to this superior electrical performance, the photoresponsivity of the MoS_2 devices on passivated oxide is also enhanced by four orders of magnitude compared to nonpassivated MoS_2 FETs. Under these conditions, negative photoconductivity and a photoresponsivity of 3×10^7 A W^{-1} is observed which is a new highest value for MoS_2. These findings indicate that the ultrathin COC passivation of the gate dielectric enables to probe exciting properties of the atomically thin 2D semiconductor, rather than interface trap dominated effects.

1. Introduction

Owing to their atomic scale thickness, 2D materials are promising candidates for next generation beyond Moore nanoelectronics.[1,2] However, in contrast to conventional metal oxide semiconductor (MOS) fabrication steps where buried oxide interfaces are employed, here the SiO_2 surface is exposed to ambient conditions and organic solvent during the transfer steps of the 2D materials via the poly(methyl methacrylate) (PMMA) assisted transfer method.[3,4] As a result, the oxide surface is a source of trap states, giving rise to dominant nonidealities in output and transfer characteristics.[5–9] This obstructs the fundamental investigations of 2D materials on SiO_2/Si wafers[10,11] tremendously; and their integration in complementary metal oxide semiconductor (CMOS) technologies[12] is an ongoing challenge.

The amount of these trap states can be quantified by extending Shockley's equations for ideal linear and saturation field effect transistor (FET) regimes by a pronounced subthreshold regime.[13] Here, the subthreshold swing, S, is the gate voltage difference that is required to increase the FET drain current by one decade. An ideal device at room temperature shows a subthreshold swing of around 60 mV decade^{-1} known as the thermionic limit.[14] In presence of traps and depletion effects, the subthreshold swing increases according to,[14]

$$S = \left(60 \text{ mV decade}^{-1}\right) \times [1+\alpha] \quad (1)$$

Here, α is a correction to account for depletion of the semiconductor and for interface traps at the semiconductor/gate dielectric interface. For ultrathin FETs, usually interface traps dominate the correction.[15] Then the equation for S reads,[16]

S. B. Kalkan, B. Nickel
Faculty of Physics and CeNS
Ludwig-Maximilians-Universität
Geschwister-Scholl-Platz 1, 80539 München, Germany
E-mail: nickel@physik.uni-muenchen.de

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E. Najafidehaghani, Z. Gan, A. George, A. Turchanin
Institute of Physical Chemistry and Abbe Center of Photonics
Friedrich Schiller University Jena
Lessingstr. 10, 07743 Jena, Germany
E-mail: andrey.turchanin@uni-jena.de

J. Drewniok, M. F. Lichtenegger, A. S. Urban
Faculty of Physics
Nanospectroscopy Group and Center for NanoScience
Nano-Institute Munich
Ludwig-Maximilians-Universität München
Königinstr. 10, 80539 Munich, Germany

U. Hübner
Leibniz Institute of Photonic Technology (IPHT)
Albert-Einstein-Str. 9, 07745 Jena, Germany

$$S = \left(60\ \text{mV decade}^{-1}\right) \times \left[1 + \frac{e^2 N_{\text{inter}}}{C_i}\right] \quad (2)$$

Here, C_i is the capacitance of the gate dielectric, e is elementary charge, and the interface trap states are quantified as N_{inter} with units $\text{cm}^{-2}\text{eV}^{-1}$. According to Equation (2), ultrathin, high-k dielectrics such as Al_2O_3[15,17] and HfO_2,[18] and low trap densities are needed to approach the intrinsic limit. For 2D materials, especially hexagonal boron nitride (h-BN) is heavily studied for this purpose. Exfoliation of h-BN was one of the first approaches to fabricate a dielectric for field effect applications.[19] Although the trap density was record low, this approach lacks scalability for standard cleanroom fabrication. A more recent and potentially scalable attempt was to grow h-BN by chemical vapor deposition (CVD) on atomic layer deposition (ALD) grown Al_2O_3.[20] However, FETs still exhibited rather large subthreshold swings of around $S = 250$ mV decade^{-1} suggesting that the trap densities of the high-k oxide with h-BN stack are rather large.

Here, we introduce an ultrathin film of cyclic olefin copolymer (COC) for passivating the SiO_2 surface traps. We already used COC as an oxide passivator for organic semiconductor FETs fabricated with the help of shadow masks.[21] The chemical inertness of the COC layer also enables us to fabricate 2D material FETs by PMMA transfer and subsequent standard cleanroom lithography. A comparison of MoS_2 FETs on nonpassivated and passivated 300 nm thick SiO_2 reveals that the subthreshold swing of these rather thick dielectrics is lowered almost fourfold as N_{inter} is reduced to 5.05×10^{11} $\text{cm}^{-2}\text{eV}^{-1}$. We demonstrate a subthreshold of $S = 189 \pm 54$ mV decade^{-1} using commercially available 100 nm SiO_2 dielectrics, as predicted by the scaling properties of Equation (2). Furthermore, we investigated the optoelectronic properties of devices on COC-passivated oxides at different frequencies and laser powers. We observed a significant enhancement in photoresponse by four orders of magnitude through the COC passivation and a negative photoconductivity phenomenon (NPC), which shows the highest photoresponsivity ever observed for MoS_2. Our findings clearly confirm that the electrical and optoelectronic potential of 2D materials can be enhanced significantly by introducing a simple and scalable method of COC passivation of SiO_2 gate dielectric.

2. Results and Discussion

Single crystals of MoS_2 monolayers were grown on 300 nm thermal oxide layers on Si by chemical vapor deposition (CVD).[3,22] The as-grown monolayers were transferred onto SiO_2/Si substrates using the PMMA-assisted transfer method.[23] Here, doped Si serves as the global back-gate and SiO_2 as the gate dielectric. The schematic cross-section of the complete FET and its optical microscopy image are shown in **Figure 1**a; Section S1 and Figure S1a (Supporting Information), respectively. To reduce N_{inter}, a thin COC layer was spin-coated prior to MoS_2 transfer for some devices. Typical thickness of the COC layer is 5–6 nm with a root mean square (RMS) roughness of ≈0.2 nm as obtained by atomic force microscopy (AFM) (see Section S2, Supporting Information). COC layer is fully compatible with subsequent standard fabrication steps (see Section S2 in Supporting Information for details). The schematic cross-section of the passivated FET and an optical microscopy image thereof are shown in Figure 1b; Section S1 and Figure S1b (Supporting Information), respectively.

To evaluate the effect of the COC surface passivation on the MoS_2 monolayers, we first investigated their optical properties by photoluminescence (PL) and Raman spectroscopy. On bare oxide, we see the characteristic PL peak of MoS_2 around 670 nm (Figure 1c). With COC passivation, the PL intensity increases by at least six times. This PL enhancement is due to a decrease in charge transfer, reduction of interface trap states, and probably a lower lattice strain between MoS_2 and COC.[24,25]

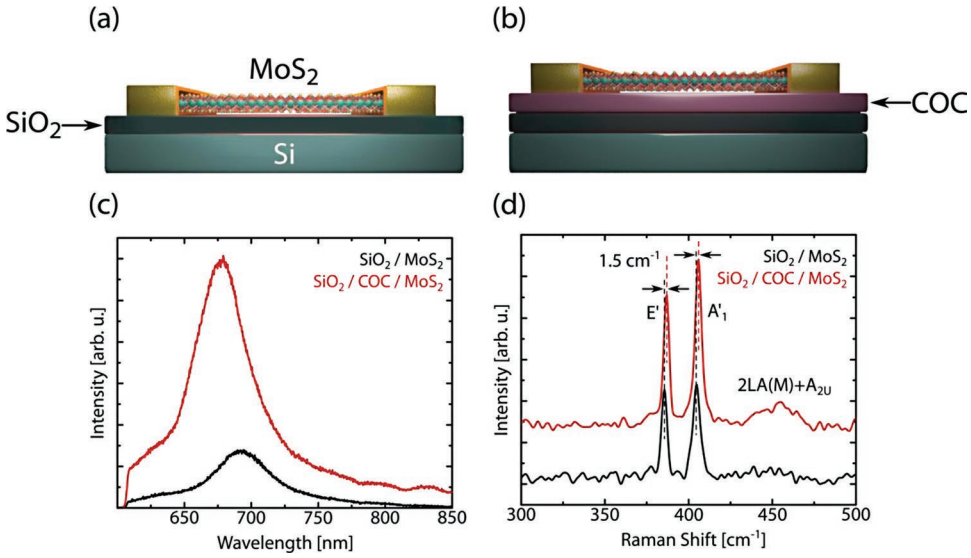

Figure 1. Bottom-gate top-contact MoS_2 field-effect transistors (FETs) on nonpassivated and passivated oxide and their optical characterization. a,b) Schemes of MoS_2 FETs with and without cyclic olefin copolymer (COC) passivation (in cross-section). c) Photoluminescence (PL) spectra of MoS_2 on bare (black) and COC-passivated oxide (red). d) Raman spectra of monolayer MoS_2 on bare (black) and COC-passivated oxide (red).

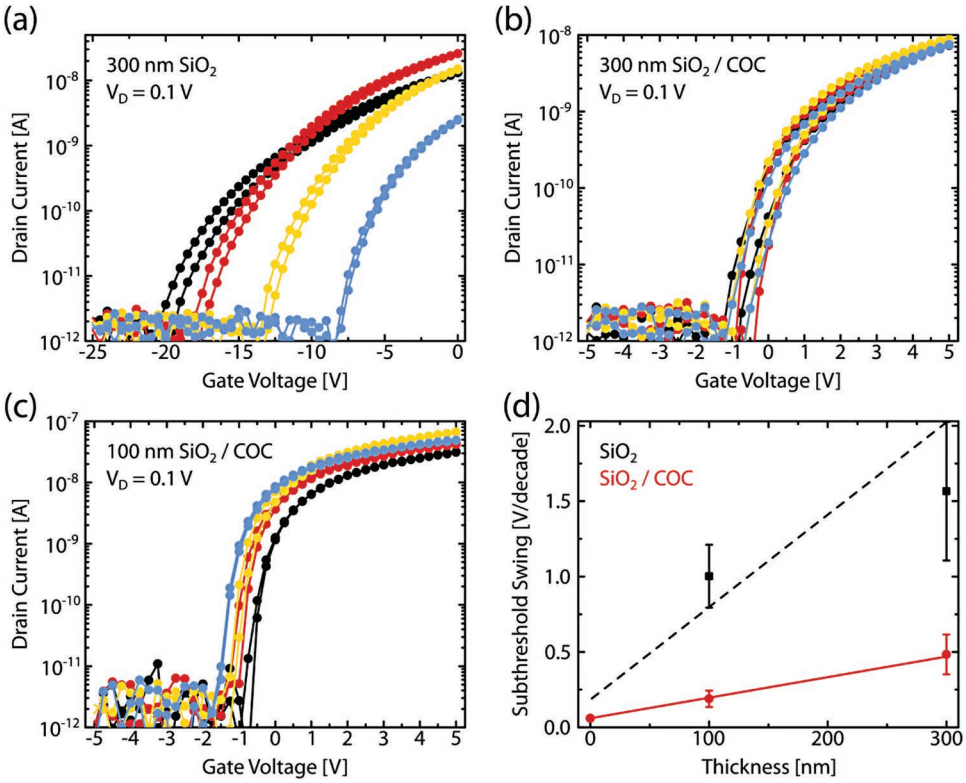

Figure 2. Transfer curves of bottom-gate top-contact MoS_2 field-effect transistors (FETs) on nonpassivated and passivated SiO_2 under a drain bias of 0.1 V. a) Transfer characteristics of four individual monolayer MoS_2 FETs on 300 nm thick bare oxide. b) Transfer characteristics of four MoS_2 FETs on 300 nm thick cyclic olefin copolymer (COC) passivated oxide. c) Transfer characteristics of four monolayer MoS_2 FETs on 100 nm thick COC-passivated oxide. d) Subthreshold swings of FETs on bare and COC-passivated oxide for different oxide thicknesses. The dashed and solid line are fits according to Equation (2) including thermionic limit at infinite capacitance.

Furthermore, Figure 1d shows the Raman spectra of MoS_2 on bare and COC-passivated oxides, featuring the typical E′ and A'_1 vibrational modes of MoS_2.[26] We observe higher intensity and lower FWHM for MoS_2 on COC-passivated oxide indicating a reduced exciton-phonon coupling between the soft COC layer and MoS_2. Moreover, we observe a blueshift of the E′ and A'_1 peaks of MoS_2 on COC-passivated oxide. Similar blueshifts have been observed for h-BN/MoS_2[27] and are associated with reduced strain of the 2D semiconductor,[28] suggesting that COC has a comparable beneficial effect here. In Table S1 (Supporting Information), we provide a comparison of Raman peak characteristics between MoS_2 on bare and passivated substrates.

Next, we investigated the electrical performance of FETs fabricated on bare and on COC-passivated oxide. The characteristic transfer curves of four FETs on 300 nm bare oxide are shown in **Figure 2**a. Although the FETs are on the same chip, the transfer curves show pronounced variances. All FETs show quite high onset voltages varying statistically from −20 to −8 V. These differences indicate that the surface consists of heterogeneous traps. We investigated the subthreshold swing and estimated the mean S value as 1566 ± 460 mV decade^{-1}. This rather large S value corresponds to a mean trap density of $N_{inter} = 1.88 \times 10^{12}$ cm^{-2}eV^{-1} for 300 nm bare SiO_2, extracted by Equation (2). Devices with higher onset voltage shows larger S. If the onset voltage is lower (see Figure 2a blue curve) then the FET also displays a lower hysteresis. We calculated the mean value of hysteresis to be 725 ± 375 mV. All these findings prove that the FETs on bare SiO_2 are highly dominated by a large amount of heterogeneous interface traps.

COC passivation prior the transfer of the MoS_2 monolayer improves the electronic properties of the FET devices

Table 1. Onset voltage, subthreshold swing, trap density, and hysteresis values of the field-effect transistors (FETs) on nonpassivated and passivated SiO_2 as a parameter of oxide thickness.

	300 nm thick SiO_2 (11.5 nF)	100 nm thick SiO_2 (34.5 nF)	300 nm thick passivated SiO_2 (11.2 nF)	100 nm thick passivated SiO_2 (31.9 nF)
Onset voltage [V]	−15 ± 6	−4.3 ± 1.3	−0.9 ± 0.5	−1.1 ± 0.5
Subthreshold swing [mV decade^{-1}]	1566 ± 460	1002 ± 208	484 ± 133	189 ± 54
Trap density [cm^{-2} eV^{-1}]	1.88×10^{12}	3.45×10^{12}	5.05×10^{11}	4.40×10^{11}
Hysteresis [mV]	725 ± 375	1475 ± 225	595 ± 45	125 ± 105

significantly, as seen in the transfer curves of four devices in Figure 2b (and see **Table 1** for direct comparison). The mean onset voltage is reduced to −0.9 V ± 0.5 V. This remarkable decrease is a direct indication of reduced number of interface traps N_{inter}. Since the variation of the onset voltage is reduced as well, we suggest that such devices are readily compatible with low voltage applications. Here, the mean value of S is 484 mV decade^{-1}, which is lowered by a factor of 4 compared to FETs on bare oxide. This value of subthreshold swing corresponds to a trap density of $N_{inter} = 5.05 \times 10^{11}$ cm^{-2} eV^{-1}, i.e., COC passivation reduced the interface trap density roughly fourfold. This trap density is one of the lowest values ever reported for CVD-grown and transferred monolayer MoS_2 on 300 nm SiO_2. Moreover, the COC passivation is able to compete with sophisticated ultrathin atomic layer deposition (ALD) grown oxides[15,29] in terms of trap density. The remaining traps may relate to the intrinsic defects in MoS_2 rather than to the gate dielectric interface[30] and low-temperature transport measurements can help to clarify their nature.

In order to explore the lowest S value of this approach, we increased the capacitance of the gate oxide by reducing its thickness from 300 to 100 nm (full comparison can be found in Table 1). Equation (2) predicts a reduction of S by nearly a factor of 3 due to the enhanced gate capacitance. On the 100 nm thick bare oxide, the subthreshold swing indeed decreased, but only by 1.5 times (Section S3, Figure S4, Supporting Information). Instead, on the 100 nm thick COC-passivated oxide, the subthreshold swing was successfully decreased from 484 mV decade^{-1} on COC/300 nm SiO_2 to S = 189 mV decade^{-1} on COC/100 nm SiO_2. This huge reduction of S is in line with the projected higher gate capacitance for 100 nm oxide (see Figure 2d). The mobility for the COC-passivated device is ≈4 cm^2 V^{-1} s^{-1}. Devices on bare SiO_2 surface approach this value at a gate voltage of ≈5 V (see Section, Supporting Information, for details).

COC passivation enhances both optical (PL, Raman) as well as transport properties (S, N_{inter}). It is well-understood that large amounts of surface traps are detrimental to the optoelectronic performance of MoS_2 based devices.[25] Therefore, we expect enhanced optoelectronical properties for COC-passivated devices. Accordingly, we performed time-resolved photocurrent (PC) measurements under ambient conditions for the FETs on bare and COC-passivated oxides as shown in **Figure 3**a,b. By analyzing a series of PC measurements, we identify optimal drain and gate voltages of 10 V and 5 V, respectively. We illuminated the devices with a 635 nm laser diode with a pulse frequency of 1 kHz and power density of 100 µW cm^{-2}. COC passivation increased the photoresponsivity values massively by almost three orders of magnitude, see **Table 2**. The detectivity limit is improved by at least one order of magnitude, as well, according to standard photoresponsivity and detectivity equations, as given in Section S4 (Supporting Information). The performance of the COC-passivated devices clearly outperforms the devices using bare oxide. Furthermore, for COC-passivated

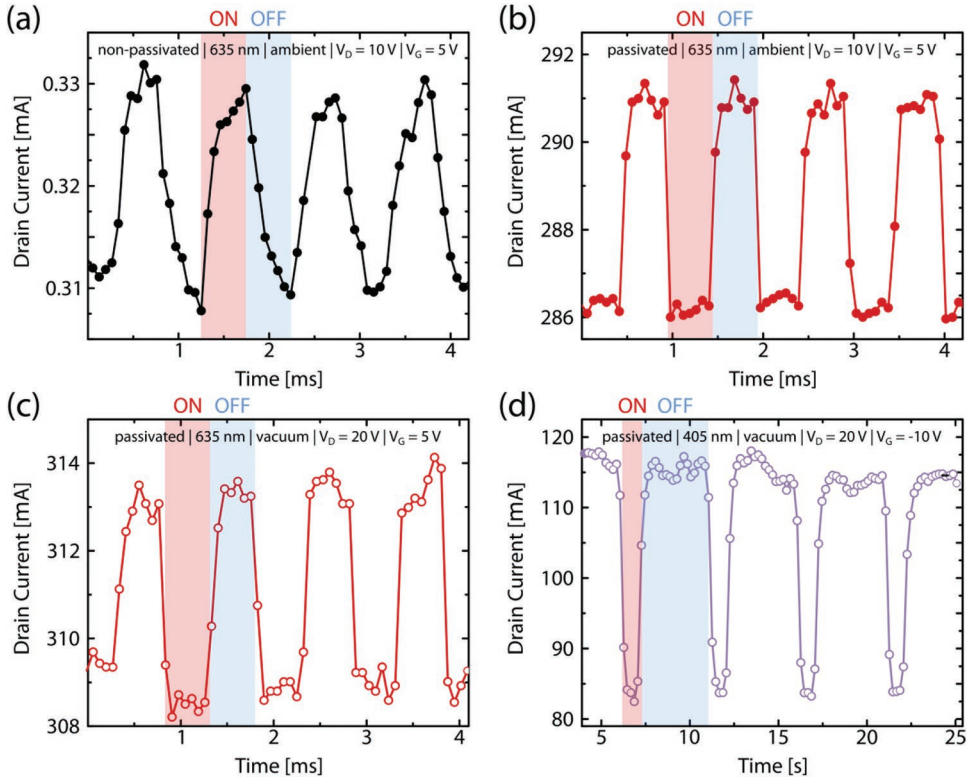

Figure 3. Optoelectronic performance of monolayer MoS_2 on nonpassivated and passivated SiO_2. Time-resolved photocurrent (PC) measurement performed on MoS_2 devices on a) bare oxide and b) cyclic olefin copolymer (COC) passivated oxide under ambient conditions. The measurement and illumination conditions of the devices are indicated over the graphs. The measurements were performed at V_D = 10 V and V_G = 5 V with a laser power (I) of 100 µW cm^{-2} and a frequency (f) of 1 kHz. c,d) The time-resolved PC measurements performed on passivated oxide under vacuum and illumination by 635 nm (V_D = 20 V, V_G = 5 V, I = 10 µW cm^{-2}, f = 1 kHz) and 405 nm (V_D = 20 V, V_G = −10 V, I = 1.1 µW cm^{-2}, f = 0.2 Hz) lasers, respectively.

Table 2. Photoresponsivity and detectivity of the field-effect transistors (FETs) on nonpassivated and passivated SiO_2 as a function of wavelength.

FETs on	Nonpassivated oxide @ambient 635 nm | 100 μW cm^{-2} | 1 kHz	Passivated oxide @ambient 635 nm | 100 μW cm^{-2} | 1 kHz	Passivated oxide @vacuum 635 nm | 10 μW cm^{-2} | 1 kHz	Passivated oxide @vacuum 405 nm | 1 μW cm^{-2} | 0.2 Hz
Photoresponsivity [A W^{-1}]	6.8×10^1	4.7×10^4	5.6×10^5	3.0×10^7
Detectivity [Jones]	2.2×10^{11}	4.8×10^{12}	5.6×10^{13}	4.8×10^{15}

FETs, the PC rise and decay time constants are estimated in the range of 50 μs which is the resolution limit of our source measure unit. Moreover, we also observe qualitative changes. While devices on bare oxide exhibit the common positive photoconductivity (PPC), the devices with COC passivation show a negative photoconductivity (NPC). NPC is a rather rare but well studied phenomenon, which occurs for well-balanced traps.[31–34] In more detail, upon illumination one kind of trap releases minority charge carriers. For MoS_2 these are hole traps, i.e., localized states close to valence band, as previously shown by us.[30] The released minority carriers recombine nonradiatively via recombination centers with majority carriers, i.e., electrons in MoS_2. In this way, the conductivity is reduced and NPC is observed.[34] Here, we observe that the dielectric interface of the bare oxide is apparently a huge source of such recombination centers evidenced by a reduction of PL. The COC functionalization suggests that there are less but still sufficient recombination centers to establish NPC. Only very few cases of NPC have been reported for MoS_2 elsewhere.[30,35,36] Since devices with bare oxide interfaces are dominated by interface traps N_{inter}, most other devices apparently lack the proper balance of traps required for NPC.

Adsorbates may act as trap states, thus also influencing photoconductivity under ambient conditions.[37–39] In order to verify if the observed PC effects are influenced by adsorbates, we conducted further experiments in high vacuum conditions. Time-resolved PC measurements are shown in Figure 3c. These PC data were obtained under pulsed illumination of a 635 nm laser at an intensity of 10 μW cm^{-2} and a frequency of 1 kHz for optimum biasing conditions of V_D = 20 V and V_G = 5 V. High vacuum further increases the photoresponsivity and detectivity values at least 10-fold compared to ambient conditions (see Table 2 for direct comparison). This suggests that the PC effects are not caused by adsorbates in the first place. We also investigated the wavelength dependence of the photoresponsivity and the detectivity of the device. We illuminated the device with a 405 nm laser at an intensity of 1 μW cm^{-2} and a frequency of 0.2 Hz (Figure 3d). We estimated the corresponding photoresponsivity and detectivity to be 3.0×10^7 A W^{-1} and 4.8×10^{15} Jones, respectively. The photoresponsivity values obtained from the time-resolved measurements in vacuum are the highest ever reported values for transition metal dichalcogenides (TMD)-based photodetectors (see Table S2, Supporting Information, for literature comparison). Thus, COC passivation reveals ultrahigh photoresponsivity of MoS_2, demonstrating the potential of the atomically thin 2D materials as gate tunable photodetectors.

In summary, we fabricated high-performance MoS_2 FETs for electronic and optoelectronic applications. The FETs are drastically influenced by surface traps of the bare gate oxide, masking the electrical and optoelectronic performance properties of MoS_2. COC passivation enabled us to lower the interface trap density N_{inter} by almost an order of magnitude, as verified by the analysis of the subthreshold swing. The calculated interface trap densities are similar to the lowest ever reported. On the other side, the photoresponsivity of the MoS_2 FETs was improved by almost four orders of magnitude by the COC passivation. The highest photoresponsivity value that we obtain is in the range of 10^7 A W^{-1}, originating from the negative photoconductivity of MoS_2. These findings may lead to low-voltage high-response 2D material-based FETs and high performance hybrid van der Waals heterostructures.[40]

3. Experimental Section

MoS_2 Growth: MoS_2 crystals were grown on thermally oxidized silicon substrates (Siltronix, oxide thickness 300 nm, roughness < 0.2 nm RMS) by a modified CVD growth method in which a Knudsen-type effusion cell is used for the delivery of sulfur precursors.[3]

COC Thin Film Preparation: TOPAS 6013-S04 was used as COC and dissolved in toluene with 0.25 wt%. The solution was centrifuged for 10 min at 8000 rpm prior to spin coating. Then, the layer was spin-coated for 60 s at 6000 rpm. Afterwards, the sample was annealed at 100 °C for 3 min for solvent evaporation.

Optical Characterization: Steady-state PL measurements were conducted using a pulsed laser (NKT Photonics, SuperK Fianium FIU-15) and an excitation wavelength of 532 nm. The laser was operated with an excitation power of 10 μW cm^{-2}. The light was collected with a 20× objective. Steady-state PL spectra were measured using a SpectraPro HRS-500 spectrometer with a 150 mm^{-1} grating and a PIXIS charge coupled device (all Teledyne Princeton Instruments).

Raman Spectroscopy: The Raman spectra were acquired using a Bruker Senterra spectrometer operated in backscattering mode at ambient conditions. Measurements at 532 nm were obtained with a frequency-doubled Nd:YAG Laser, a 50× objective, and a thermoelectrically cooled CCD detector. The spectral resolution of the system was 2 to 3 cm^{-1}. For all spectra the Si peak at 520.7 cm^{-1} was used for peak shift calibration of the instrument.

FET Fabrication: After PMMA assisted transfer of ML MoS_2 on COC-passivated oxides, substrates were immersed to acetone for 2 h to remove PMMA supporting layer. Then, 950 K A4 PMMA was spin-coated and annealed at 100 °C for 10 min. MIBK:2-propanol (1:3) solution was used as developer for 50 s. After the metal electrode deposition, the sample had been left in acetone for another 3 h to complete lift off process. The bare devices used for optoelectronic measurements were fabricated using cleanroom nanofabrication procedure described.[3,41]

Device Characterization: A home-built ambient probe station coupled to Keithley 2612B as source measure unit was used for the characterization of the FETs under dark conditions.

Optoelectronic Measurements: The optoelectronic characterization was carried out with two Keithley 2634B source measure units. First unit was used to change the gate voltage and measure gate current, where second unit was used to apply the drain voltage and measure drain current with respect to the grounded source. A Lakeshore vacuum needle probe station TTPX was used to measure the devices in ambient as well as in vacuum at a residual pressure about 10^{-6} mbar at room temperature.

The samples were illuminated using 635 and 405 nm single mode fiber pigtailed laser diodes (LP520-SF15 and LP405C1, Thorlabs). The laser diode was driven using Thorlabs laser diode controller (ITC4001).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

A patent application is being prepared based on the findings described in this paper.

Author Contributions

S.B.K. and E.N. contributed equally to this work. The oxide passivation for FETs was initiated by S.B.K. and B.N. and the photodetector work was suggested and carried out by E.N., A.G., and A.T. MoS_2 samples were grown and characterized by Z.G., E.N., and A.G. PL measurements were carried and analyzed by J.D., M.F.L., and A.S.U. Passivated and nonpassivated samples were fabricated by S.B.K. and U.H., respectively. S.B.K. and B.N. measured and analyzed the FET characteristics and E.N., A.G., and A.T. analyzed the optoelectronic device performance. S.B.K., E.N., A.G., A.T., and B.N. wrote the manuscript with contribution of all co-authors.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

gate oxide passivation, high-performance photodetectors, interface traps, low-voltage field-effect transistors, MoS_2 field-effect transistors

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