Digital One-Shot Charge-balancing Method for Implantable Current-Mode Electrical Stimulation

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***Abstract*—A low-power digital charge balancing system, which ensures the safe operation of constant-current biphasic stimulation is presented. The concept of the proposed charge-balancing technique is to utilize a hybrid method consisting of anodic pulse modulation and short-term offset current injection. Furthermore, a dual thresholding strategy is employed to guarantee precise and low-power imbalance compensation. The charge-balancing system is capable of canceling large persistent imbalances by adjusting the input code of an 8-bit current-steering digital-to-analog converter (DAC) as well as injecting an offset current in a power-efficient way. The performance of the designed charge balancer is evaluated by modeling a 1 mA biphasic constant-current stimulator with 8-bit DAC resolution. The charge-balancing system is implemented on a Cyclone IV FPGA, and measurement results evidence the safe, accurate and low-power charge-balancing performance in which the balance offset current injection is performed in less than 5% of the stimulation time while the dynamic power consumption is at $0.76\ mW$.**

***Keywords*—Safe neurostimualtion, Active charge balancing, FPGA implementation**

I. Introduction

Neurostimulators are implantable medical devices that are used to treat a wide variety of diseases including Epilepsy, Parkinson, movement disorders, and chronic pains. Neurostimulation is performed by delivering electrical stimulation to specific tissues to generate desired action potentials. Electrical stimulation techniques are categorized into 1) Voltage-mode, 2) Current-mode, and 3) Charge-mode stimulation. The most prevalent stimulation method used in implantable medical devices is constant-current stimulation, thanks to its inherent accurate charge transfer and compact implementation [1]–[3]. A notable difficulty in current-mode stimulation is the lack of control over the electrode-electrolyte output voltage since the residual potentials accumulate in long-term stimulation.

The basic technique to overcome the accumulation of residual potential on electrodes is to apply biphasic pulses. A favorable neural response is induced by a cathodic pulse that is followed by an anodic pulse to release the previously injected charge. It should be noted that small charge imbalances accumulate on electrodes even with a highly careful matching between anodic and cathodic current pulses due to some inevitable imperfection factors such as device mismatches, supply noise, switch device skew, and interface impedance fluctuations [4]. These small charge imbalances can contribute to irreversible tissue and electrodes damages. Thus, charge-balancing circuits are indispensable for long-term safe stimulation.

In active charge balancing, the charge imbalances are neutralized according to the amplitude of the residual potentials. [4] and [5] performs the active charge balancing using anodic pulse modulation. The shortcoming of this technique is that the amplitude of the anodic pulse is adjusted by specific constant values (I_{CB+} and I_{CB-}). Therefore, it can take several stimulation phases to cancel large charge imbalances. Cathodic pulse width modulation is done in [6] based on real-time interface impedance calculation. Furthermore, [1] employs anodic pulse modulation in addition to the offset current injection. However, the offset current injection requires the operation of an analog-to-digital converter (ADC) in an iterative way which contributes to high power consumption.

In this work, a digital low-power charge balancing method is proposed which applies anodic pulse modulation and offset balance current injection. The proposed power-efficient and accurate charge balancer guarantees to maintain the residual potential within a safe range in the long-term stimulations. Furthermore, defining a dual threshold according to the pulse modulation and offset current injection avoids activation of the charge balancer after each stimulation phase while the residual potential is constantly kept within a safe region.

The rest of this paper is organized as follows. Section II describes the topology of a current-mode stimulator with the proposed closed-loop charge neutralization method. Section III explains the novel one-shot charge balancing methodology with dual thresholds. Section IV demonstrates the hardware implementation of the charge balancer as well as the measurement results. Lastly, Section V concludes the paper.

II. System architecture

A neural stimulator with a closed-loop charge balancer consists of a level shifter, current steering DAC, output current

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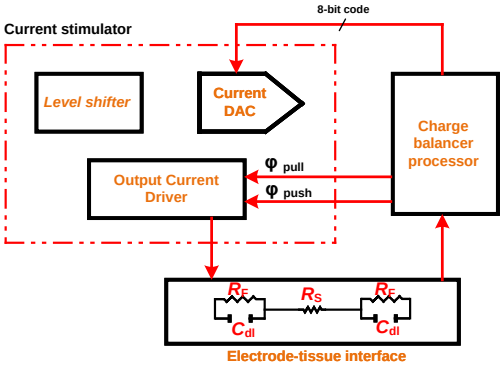

Fig. 1: Block diagram of a charge-balanced stimulator

driver and digital charge balancing processor. The top-level block diagram of the system is illustrated in Fig. 1.

The model of a current-mode stimulator is used in this work to simulate the electrical stimulation and assess the charge balancer effectiveness. The level shifter is in charge of converting the level of digital control signals to be used in the output current driver. A current steering DAC generates appropriate current amplitudes according to its digital input signal. The maximum DAC current amplitude is $1\,mA$ with an 8-bit resolution which results in the LSB current amplitude equal to 3.9 μA. The output current driver is in charge of delivering current pulses to the electrode-electrolyte interface in cathodic and anodic phases as well as injecting the offset balance currents during the inter-pulse resting time.

The model of the electrode-tissue interface is depicted in Fig. 1. R_F, C_{dl} and R_s represent Faradaic charge transfer, chemical charge redistribution and tissue impedance, respectively.

The focus of this paper is to develop a charge-balancing processor that is capable of neutralizing small and large persistent charge imbalances by generating control signals for the current steering DAC and the output current driver to ensure safe and precise electrical stimulation.

III. Active Charge Balancing Methodology

The goal of the design is to achieve accurate, power-efficient, and one-shot charge neutralization. The pulse injection method suffers from inducing unwanted stimulation, and offset current injection during the entire inter-pulse interval causes significant power consumption. Moreover, the effectiveness of the anodic pulse modulation to neutralize charge imbalances is mainly dependent to the current steering DAC properties such as the maximum current and bits resolution.

Thus, the proposed digital charge balancing system utilizes both anodic amplitude pulse modulation and offset balance current injection to offer a trade-off between safety and accuracy of charge neutralization in which the large persistent imbalances are canceled by the anodic pulse modulation and small imbalances are compensated by a time-limited offset current injection. The charge balancing is executed in a one-shot manner in which only one sampling by an ADC is required to monitor the residual potential in each stimulation phase.

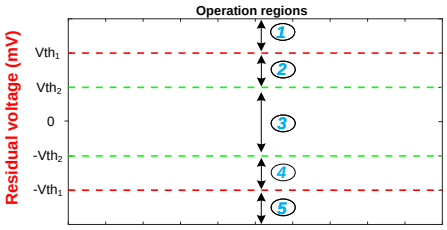

Fig. 2: Operation regions of the charge balancer

A. Charge balancing operation regions

A challenging matter in designing a charge-balancing circuit is to define a safe region for the residual voltage accumulated on the electrodes. The thresholds of $\pm 50\,mV$ and $\pm 100\,mV$ are considered in conventional implantable electrical stimulators [4]. It is noteworthy that choosing a single threshold increases the risk of returning to the unsafe region after each stimulation phase [1]. In this condition, the charge balancing must be performed after every stimulation phase that contributes to increased energy consumption. As a consequence, a threshold is defined according to the anodic pulse modulation method (V_{th1}) and another threshold is considered with respect to the balance current injection method (V_{th2}) that are shown in Fig. 2.

The flowchart that demonstrates the charge balancing process is illustrated in Fig. 3. The residual potential (V_E) on the electrodes is sampled only once after the anodic pulse in each stimulation phase, and the operation region is determined by the charge balancing processor. The *count* variable demonstrates whether the charge imbalances are persistent. If the residual potential stays in an unsafe region for at least three consecutive stimulation phases, the charge imbalances are considered as persistent imbalances. Therefore, random large imbalances that occur only in a single stimulation phase do not cause anodic pulse modulation.

If the residual potential is in the unsafe region with non-persistent charge imbalances ($count < 3$), the charge neutralization is conducted by the balance current injection. In addition, if the residual potential is in the unsafe region with persistent imbalances, the anodic pulse modulation lowers the residual voltage below $|v_{th1}|$. The amplitude of this compensation is denoted as V_{c1} . Subsequently, a limited-time balance current injection brings the residual voltage below $|v_{th2}|$. Otherwise, if the residual voltage is in the safe regions (Regions 2,3 and 4), the charge balancer stays in idle mode.

B. Anodic pulse modulation

The anodic pulse modulation technique enables residual charge neutralization without injecting any pulse or offset current during the inter-pulse resting interval. The effectiveness of this method mainly depends on the maximum stimulation current, DAC resolution, and the double-layer

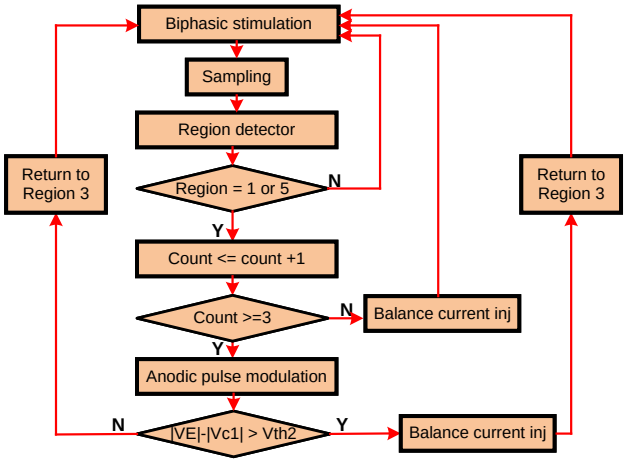

Fig. 3: Flow chart of the proposed charge-balancing system

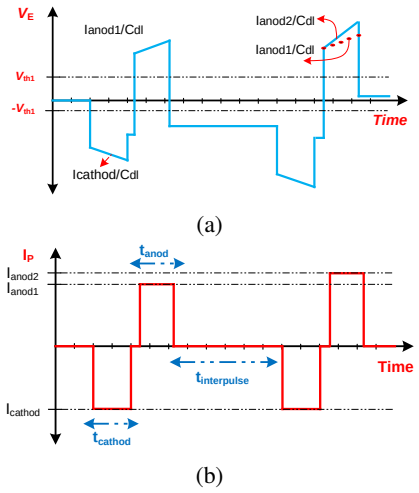

Fig. 4: (a) Residual potential and (b) Biphasic current pulses with anodic pulse modulation

capacitor of the interface model. The electrode-electrolyte interface shown in Fig. 1 is modeled with $R_F = 10\,M\Omega$, $C_{dl} = 100\,nF$ and $R_S = 10\,K\Omega$ with reference to the platinum electrode used in retinal implants [4]. In addition, a programmable DAC is modeled that delivers a maximum current of $1\,mA$ with 8-bit resolution.

The threshold of the anodic pulse modulation is given in (1) where a relatively high stimulation frequency of 100 Hz is considered with a 10% duty cycle. It represents the minimum amplitude of the residual potential that can be compensated by adjusting the anodic pulse amplitude.

$$V_{th1} = \frac{I_{LSB} \times t_{anod}}{C_{dl}} = 20\,mV \tag{1}$$

Fig. 4 demonstrates the charge neutralization process using the anodic pulse modulation technique. The cathodic pulse amplitude remains constant to induce a desired action potential. However, the anodic current amplitude is increased in the second stimulation phase since a negative residual potential, that is beyond the V_{th1}, was observed in the first phase. Adjusting the amplitude of the anodic current is done by modifying the DAC code which results in a change in the linear voltage gradient from $\frac{I_{anod1}}{C_{dl}}$ to $\frac{I_{anod2}}{C_{dl}}$ as depicted in Fig. 4a. It should be noted that anodic pulse modulation is performed when a persistent imbalance occurs in at least three consecutive phases since some large imbalances originate from random processes that do not take place in consecutive phases. Therefore, a time-limited offset balance current injection is utilized to neutralize the non-persistent imbalances.

C. Offset balance current injection

The concept of offset balance current injection is to inject an offset DC-current during inter-pulse resting intervals to cancel charge imbalances. The amplitude of the balance current must be small enough to avoid inducing unwanted stimulations. The maximum balance current duration is $1\,ms$ that is only 10% of the entire stimulation time to reduce the ADC power consumption. The balance current duration is calculated in the charge balancing processor in a one-shot manner based on only a single sample from the ADC after the anodic phase. The amplitude of the offset balance current is chosen at $1\,\mu A$ that is low enough to prevent unintentional stimulations.

According to the system flow chart, the balance current injection is conducted in two conditions as demonstrated in Fig. 5. The first condition occurs after the first stimulation phase in which the residual potential is in the Region 5 with non-persistent imbalances ($count < 3$). Thus, the offset balance current is injected with the maximum defined duration ($t_{balance-max} = 1ms$). The second condition takes place after the next stimulation phase as the charge imbalances are detected to be persistent. Thus, the anodic pulse modulation is performed to decrease the residual potential to Region 4. Subsequently, the charge balancing processor calculates the required balance current duration to lower the residual voltage to $-V_{th2}$ in a one-shot manner. V_{th2} is defined as the maximum residual voltage that can be compensated by the offset balance current that is given in (2).

$$V_{th2} = \frac{I_{LSB} \times t_{anod}}{C_{dl}} = 10\,mV \tag{2}$$

IV. Hardware Implementation of the Design

The proposed charge-balancing system is implemented on a Cyclone IV FPGA and an Analog Discovery 2 device is used in the measurement of a physical model of the electrode-tissue interface. The top-level block diagram of the digital charge balancer is depicted in Fig. 6.

The residual voltage of the previous stimulation phase is delivered to the input multiplexer. Subsequently, the input residual potential progresses through the region detector block to determine the operation region of the signal. Then, the processor generates the pull and push signals for the output current driver to inject the appropriate balance current during the resting interval. Furthermore, the 8-bit $I_{anod-modulated}$ signal is delivered to the current steering for anodic pulse

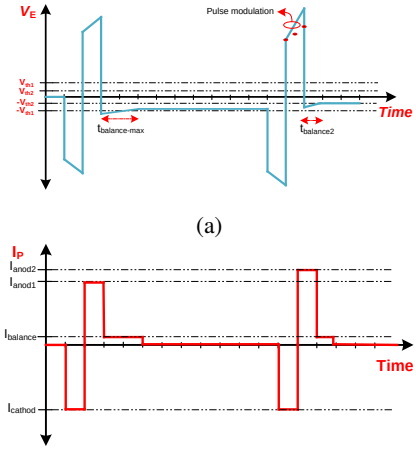

Fig. 5: (a) Residual potential and (b) Current profile with hybrid pulse modulation and offset current

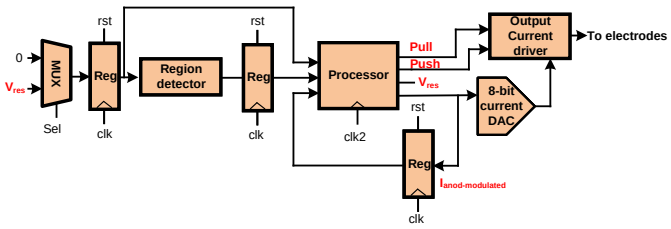

Fig. 6: Charge balancing top-level view

TABLE I: FPGA implementation performance

Logic elements	2439	**Total registers**	1206
Processor Freq	1 MHz	**Dynamic Power**	0.76 mW
Stim Freq	100 Hz	**Electrode model**	$100\,nF \parallel 1\,M\Omega$
Memory	27648 bits	**Tissue impedance**	$10\,k\Omega$

modulation. It is noteworthy that the first clock is selected according to the ADC sampling frequency ($clk = 1\,MHz$), and the second clock is determined by the stimulation frequency ($clk2 = 100\,Hz$). The FPGA implementation parameters are given in Table I.

Fig. 7 depicts a 1 sec charge balancing duration including 100 stimulation cycles and the offset residual voltage of $15\,mV$ for each stimulation phase. Fig. 7a shows that the initial amplitude of the anodic and cathodic phases are equal to $100 \times I_{LSB}$. Then, the anodic pulse amplitude is modulated and settles to $91 \times I_{LSB}$ after 40 stimulation cycles.

Fig. 7b shows the control signal of the offset current injection during the inter-pulse interval. It reveals that the duration of balance current injection is $53.2\,ms$ in a 1-sec stimulation measurement. Thus, it enables a power-efficient stimulation compared to the state-of-the-art that injects the offset current during the entire inter-pulse interval. Lastly, Fig. 7c evidences that the proposed hybrid charge balancer is capable of maintaining the residual potential within the safe regions while $1.5\,V$ residual voltage was expected without

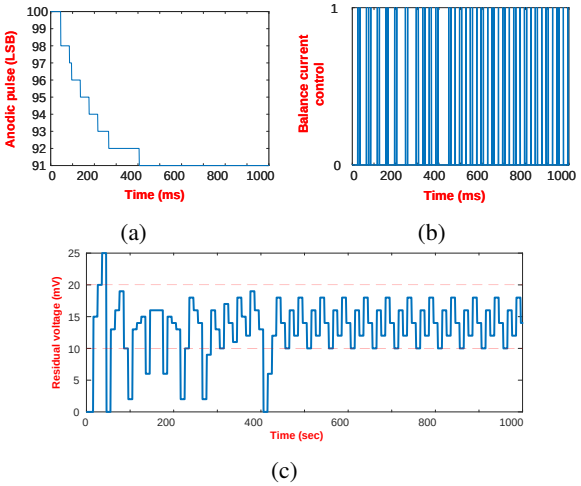

Fig. 7: (a) Anodic pulse amplitude, (b) balance current control signal and (c) residual voltage

charge balancing.

V. Conclusion

The design and FPGA implementation of a digital hybrid charge-balancing technique was presented. This work realizes power-efficient and precise charge balancing using anodic pulse modulation in conjunction with offset balance current injection. The one-shot approach can significantly reduce the power consumption of the ADC since it is activated only once in each stimulation phase. Additionally, the large persistent imbalances are neutralized by anodic pulse modulation and small imbalances are compensated by a short-term offset current injection. The design is implemented on a Cyclone IV FPGA and the measurement results are also provided.

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