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Selective Harmonic Mitigation: Limitations of Classical Control Strategies and Benefits of Model Predictive Control

Leyre Rosado, Javier Samanes, Eugenio Gubia and Jesus Lopez
Department of Electrical, Electronic and Communication Engineering, Public University of Navarre (UPNA), Campus de Arrosadía, 31006 Pamplona, Spain
Institute of Smart Cities, Public University of Navarre (UPNA), Campus de Arrosadía, 31006 Pamplona, Spain
Corresponding author: leyre.rosado@unavarra.es

***Abstract*—Selective harmonic mitigation pulsewidth modulation (SHMPWM) combined with model predictive control (MPC) is a promising approach for grid-connected power converters. SHMPWM can guarantee grid code compliance in steady state, e.g. grid harmonic injection, with a reduced output converter filter, while MPC improves dynamic response and allows grid code compliance in the event of grid transients. This paper presents a survey of the MPC strategies already published in the literature developed for their use with SHMPWM. The existing strategies fall into two categories: direct model predictive control with an implicit selective harmonic mitigation modulator, and direct model predictive control based on finite control set (FCS-MPC). One representative control strategy of each group is compared to each other and to the performance of classical proportional-integral (PI) controllers combined with SHMPWM. The goal is to identify the potential benefits of MPC for grid-connected power converters, and determine the main advantages and limitations of the two selected state-of-the-art control strategies. Their performance is assessed through Hardware-in-the-Loop (HIL) experimental results in terms of real-time implementation, harmonic content grid code compliance, dynamic response and performance under grid transients.**

***Index Terms*—Selective Harmonic Mitigation PWM, Model Predictive Control, Linear Control, Stability Analysis**

I. Introduction

Model predictive control is a promising alternative to classical linear control strategies for medium voltage high power grid-connected converters [1]. These converters are widely used for grid-connected renewable energy generation and storage systems [2], and therefore, must comply with grid code requirements. Among these requirements, it is worth highlighting a fast dynamic response in grid transients [3], and compliance with voltage and current harmonic emission limits in the point of common coupling (PCC) [4], [5]. The switching frequency of high power converters is limited in order to reduce switching losses and operate within the converter thermal limits. Therefore, meeting harmonic emission limits with carrier-based PWM or space vector PWM would require bulky and expensive filters in the case of L filters, or very low resonance frequencies would be obtained in the case of LCL filters, which introduces additional stability issues. In order to reduce the size of the output filters, selective harmonic mitigation pulsewidth modulation is a very interesting modulation technique [6]. It allows to adapt the harmonic content to a certain grid code for a given output filter, using a reduced number of switching angles.

Traditionally, this modulation technique has been combined with classical control strategies such as PI regulators with the objective of properly tracking the current reference. However, the SHMPWM technique is designed considering that the control action is constant over one fundamental period, whereas linear controllers demand a control action each sampling period. This way, the combination of a PI controller with SHMPWM limits the dynamic performance of the converter [7], which compromises the fulfillment of other aspects of grid codes like a fast dynamic response in the case of grid transients such as low voltage ride through (LVRT) [8].

In order to improve the system dynamic response when a power converter implements SHMPWM, model predictive control has emerged as a potential alternative. Model predictive control strategies can be classified as indirect MPC, in which the controller computes a modulation index or duty cycle that is fed into a modulator, and direct MPC, in which the control and modulation problems are formulated and solved in one computational stage [9]. Direct control strategies that combine SHMPWM and MPC have been proposed in the literature to exploit the benefits of selective harmonic mitigation while achieving a fast dynamic response. The existing strategies can be classified into two main groups: direct model predictive control with an implicit SHMPWM, and direct model predictive control based on finite control set. The calculation of the selective harmonic mitigation switching pattern is computationally demanding, so in any case, the switching angles are computed offline over a range of modulation indexes and stored in a look-up table (LUT). The main difference between these two sets of strategies is how the closed-loop control modifies the precomputed switching angles to achieve the desired control objectives.

Direct model predictive control with an implicit SHMPWM is based on an online time modification or correction of the precomputed switching instants. With this purpose, the MPC action is expressed as a time increment that is applied

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to the selective harmonic mitigation pulse pattern previously computed offline. The first controllers that belong to this group were current tracking strategies developed for motor drives [10], [11]. The current fundamental component is controlled in [10] by a conventional PI regulator that is used to load the required switching pattern in steady state. This pattern is used to calculate the reference current trajectory, and a tracking controller based on a deadbeat algorithm, modifies the switching angles to obtain a fast dynamic response. In [11] a similar control strategy is proposed, but in this case, the machine parameters must be known in order to estimate the current fundamental component. As an alternative, a stator flux trajectory control is proposed in [12]. The stator flux reference trajectory is obtained from the precalculated pulse pattern and the real flux is estimated using the machine model. The error is used in a trajectory controller that modifies the switching pattern in order to follow the stator flux reference. These strategies require to separate the fundamental and the harmonic components of the variables to compute the controller action. More recently, and with the aim of avoiding the separation of the stator flux fundamental and harmonic components, model predictive pulse pattern control (MP3C), was proposed in [13] for motor drives. This MPC strategy included an interesting concept, the receding horizon policy. The switching instant modifications computed by the MP3C are applied to the precomputed switching transitions that fall in a prediction horizon [14].

In the last years, direct model predictive control with an implicit selective harmonic mitigation pulsewidth modulator has also been applied to grid-connected power converters. For instance, MP3C is used for a static synchronous compensator (STATCOM) [15], where a virtual converter reference flux is created from the precomputed switching pattern and tracked by the controller, and for a grid-connected converter [16], where the current reference harmonic and fundamental components are tracked. The precomputed switching pattern associated to the steady state operation is loaded, and it is modified by the closed-loop controller. A benefit of this control strategy is that it is not necessary to ensure the continuity of the precomputed switching angles, and thus, the limits on harmonics imposed by grid codes can be fulfilled with a reduced set of switching angles. This continuity is a desirable characteristic when SHMPWM is combined with classical linear controllers, such as PIs, to avoid dynamic modulation errors that lead to overcurrents in transients [11], [13]. In [15], [16] MP3C was applied to a first order dynamic system, a grid-connected converter with an inductive filter. However, power converters frequently have *LCL* filters, for this reason, in [17], [18] it is generalized for higher order dynamic systems. To obtain a convex quadratic optimization problem that can be solved online for high order dynamic systems, the switching instant modifications of the precomputed switching pattern are modeled by the strength of impulses. In the previous MP3C strategies, the current or flux error at the end of the prediction horizon is controlled. However, in [19], [20] to control the trajectory of the current along the prediction horizon, its gradient is controlled.

Direct MPC based on finite control set strategies combined with selective harmonic mitigation PWM have also been proposed in the literature. The main difference with the previous strategies that included an implicit modulator is that the control strategy does not directly compute a switching instant modification of the precomputed selective harmonic mitigation pattern. Instead, every sampling interval, the converter evaluates all the possible converter switching states and imposes the one that minimizes an objective function that includes, among other control objectives, tracking of the precomputed selective harmonic mitigation pattern [1], [21], [22]. So far, the strategies proposed for their use with SHMPWM use a single step prediction horizon [21], [22]. In [21] the control objective is to obtain a fast dynamic response, while switching according to a precomputed switching pattern in steady state in order to achieve the desired switching frequency and harmonic content. This strategy was designed for a standalone converter with a *RL* load, and was later adapted to control a three-level neutral point clamped (NPC) grid-connected converter [1]. With this purpose, a modification in the cost function is introduced to guarantee that the power converter is operated within its thermal limits. Finally, in [22] a similar approach is presented. In this case, the objective function includes an additional term to balance the capacitor voltage of modular multilevel converters.

This extensive introduction reviews the main MPC control strategies already published in the literature developed for their use with selective harmonic mitigation PWM, strategies that are categorized as direct model predictive control with an implicit selective harmonic mitigation modulator, and direct model predictive control based on finite control set. In this paper, one representative control strategy of each group is compared to each other and to the performance of classical PI controllers combined with SHMPWM. The goal is to identify the potential benefits of MPC for grid-connected power converters, and determine the main advantages and limitations of the two selected state-of-the-art control strategies. Their capabilities are tested in terms of real-time implementation, harmonic content grid code compliance, dynamic response and performance under grid transients, such as LVRT, an analysis that has not been performed so far in the existing papers. The FCS-MPC strategy [21] with the modification presented in [1] is considered as the representative example of the strategies that belong to the category direct MPC based on finite control set. For those that include an implicit modulator, MP3C is selected [14]. The control strategies are tested for a three-phase neutral point clamped (NPC) grid-connected power converter with an inductive output filter, a first order dynamic system to which both strategies can be applied.

The paper is structured as follows, first, the optimization problem to compute the switching instants for the SHMPWM is presented in Section II. In Section III the limitations of SHMPWM in conjunction with a PI controller are studied. Section IV presents the FCS-MPC strategy, while in Section V MP3C is described. Finally, the three strategies are compared through experimental results performed in a Hardware-in-the-Loop (HIL). This paper further develops the work presented in [1], where the benefits of MPC for grid-connected power converters were studied. A more in-depth literature review is

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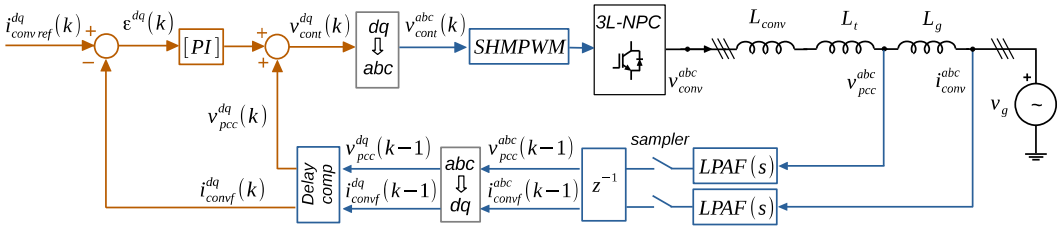

Fig. 1: Three-level NPC power converter with an L filter connected to the grid and a PI-based current control loop with SHMPWM.

presented in this paper and the comparison of the control strategies is enlightened thanks to the experimental results carried out in a HIL.

II. Selective Harmonic Mitigation Pulsewidth Modulation

A. System Description

Multilevel converters are commonly used in high-power and medium-voltage applications since they allow to increase the output voltage with reduced harmonic distortion [23]. Fig. 1 shows a three-level NPC power converter connected to the high voltage grid through a step-up transformer at the PCC. L_t is the transformer leakage inductance and L_g is the grid inductance. An additional inductor, L_{conv}, is added between the converter and the transformer to filter the converter harmonics. The system parameters are reported in Table I.

B. Offline Computation of the Switching Angles

The SHMPWM is designed to comply with the limits for voltage harmonics and the voltage total harmonic distortion, THDv, defined in the IEC 61000-3-6 code [4]. The converter output voltage is assumed to have odd quarter-wave symmetry, therefore, only the non triplen odd harmonics up to the 50th must be limited. The solution, i.e., the switching angles, α_i, is found by solving the following optimization problem over a range of modulation indexes [6].

$$\begin{aligned}
\min_{\alpha_i} \quad & c_{THDv} THDv + c_1 E_1 + \sum_{n=5,7,\ldots,49} c_n H_n \\
\text{s.t.} \quad & E_1 = |M - H_1| \leq L_1 \\
& H_1 = \left|\frac{4}{\pi}\frac{V_{DC}}{2}\sum_{i=1}^{N_\alpha}(-1)^{i-1}cos(\alpha_i)\right| \\
& H_n = \left|\frac{4}{n\pi}\frac{V_{DC}}{2}\sum_{i=1}^{N_\alpha}(-1)^{i-1}cos(n\alpha_i)\right| \leq L_n \\
& THDv = \sqrt{\sum_{n=5}^{49}\left(\frac{H_n}{H_1}\right)^2} \leq Lim_{THDv} \\
& \alpha_{i+1} - \alpha_i > \theta \quad \alpha_0 > \theta/2 \quad \pi/2 - \alpha_{N_\alpha} > \theta/2
\end{aligned} \tag{1}$$

The problem constraints include control of the fundamental component, limits for each harmonic and for the THDv, and a minimum pulsewidth denoted as the angle θ. H_1 is the amplitude of the fundamental component. Note that H_1 is not forced to be equal to the desired modulation index, M, but the deviation is kept below an acceptable level given by $L_1 = 0.001$. H_n is the amplitude of the nth harmonic, V_{DC} is the dc bus voltage, N_α is the number of switching angles in a quarter wave, n is the harmonic order and L_n is the limit imposed by the grid code to the nth harmonic. Note that the THDv is calculated considering all the non triplen odd harmonics up to the 50th.

The costs c_{THDv}, c_1 and c_n of the objective function are defined as explained in [6]. c_1 always equals 10000. c_{THDv} and c_n take different values depending on whether the THDv and the hamonics comply with the limits imposed by the grid code. If they are below the limit, c_{THDv} and c_n equal 1, while if they are higher, the costs equal 1000. This way we ensure that the solutions have the desired modulation index and all the limits are met.

The switching angles are computed offline and stored in a look-up table. The minimum pulsewidth, θ, equals 0.01 rad, which is equivalent to 30 μs, which accounts for the dead time and the minimum turn-on time of the semiconductor. $N_\alpha = 11$

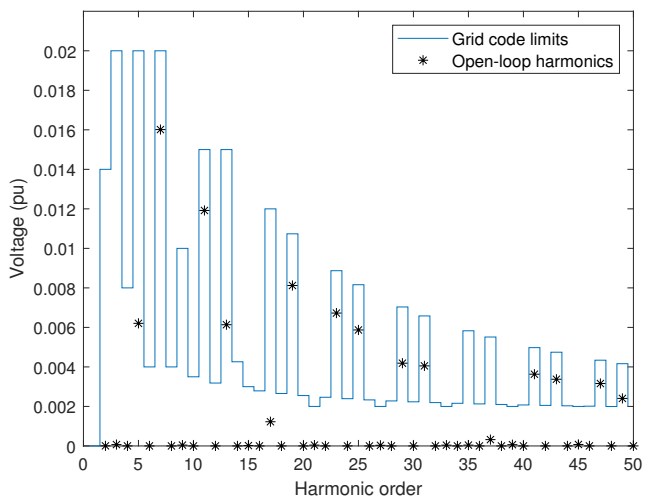

Fig. 2: Harmonic content of the voltage at the PCC when the converter modulates a constant modulation index equal to 1.062.

angles, which results in a switching frequency of 1100 Hz. Fig. 2 shows the harmonic content of the voltage at the PCC compared to the grid code limits. In this simulation, the converter rated active power is injected to the grid ($M = 1.062$) and there is no closed-loop control. This result shows that the grid code is fulfilled with the solution that we obtain. Besides, the THD is 2.6 % which is also below the maximum allowed value.

III. PI-BASED CONTROL STRATEGY

A. System Model

The three-level power converter shown in Fig. 1 is controlled as a current source, assuming that the grid is an ideal voltage source with an inductance L_g. The current is controlled in the synchronous reference frame, *dq*, where the fundamental component becomes a dc component and thus, a PI controller offers zero tracking error. For this reason, the digital current control loop in Fig. 1 is modeled in this reference frame.

The model of the system plant in the Laplace domain is given by

$$i_{conv}^{dq} = [Z_{RL_{ct}}]^{-1}(v_{conv}^{dq} - v_{pcc}^{dq}) = [Z_{RL_g}]^{-1}(v_{pcc}^{dq} - v_g^{dq}), \tag{2}$$

where i_{conv}^{dq} is the converter current, v_{conv}^{dq} is the converter differential voltage, v_{pcc}^{dq} is the voltage at the PCC, and v_g^{dq} is the grid voltage. Note that the superscript dq indicates that the variables are two-component vectors in the synchronous reference frame. The general expression for the impedance matrix $[Z_{RL}]$ is given by

$$[Z_{RL}] = \begin{bmatrix} R + Ls & -L\omega_0 \\ L\omega_0 & R + Ls \end{bmatrix}. \tag{3}$$

For $[Z_{RL_{ct}}]$, $L = L_{ct} = L_{conv} + L_t$, and $R = R_{ct} = R_{conv} + R_t$. R_{conv} is the converter inductance series resistance, and R_t is the transformer resistance. In the case of $[Z_{RL_g}]$, $L = L_g$, and $R = R_g$, R_g being the grid resistance. ω_0 is the angular speed of the *dq* axis, which is equal to the grid fundamental angular speed.

The converter current and the voltage at the PCC are filtered with a low pass analog filter, $LPAF(s) = 1/(\tau s+1)$, used to filter noise at the switching frequency. The cutoff frequency is $f_s/2$, f_s being the sampling frequency. Both signals are sampled at time kT_s, k being the current sample and T_s the sampling period. There is also a sample delay due to the computational time of the digital signal processor (DSP). These two elements are modeled using the second order Padé approximation of a pure delay, which is denoted as $D_{conv}(s)$. All the elements of the control loop must be modeled in the same reference frame in order to perform the stability analysis, which in this case is the synchronous reference frame. For that reason, the transformation in [24] is used to rotate the transfer functions $LPAF(s)$ and $D_{conv}(s)$ from the stationary to the synchronous reference frame, obtaining two 2x2 transfer function matrices. This rotation is done at ω_0.

The current and the voltage are transformed to the *dq* reference frame by means of the Park transformation, which uses the angle of the voltage measured at the PCC. The *delay comp* block in Fig. 1 represents the compensation of the computational delay, which is done by adding $\omega_0 T_s$ to the current angle.

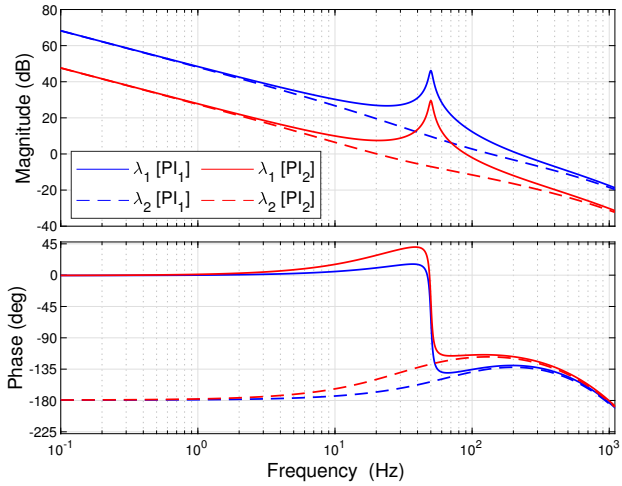

Fig. 3: Eigenvalues' Bode diagram of the open-loop transfer matrix for the two PI controllers.

Finally, the PI controller is defined in *dq* axis by the following transfer matrix

$$[PI] = \begin{bmatrix} K_p \frac{T_n s+1}{T_n s} & 0 \\ 0 & K_p \frac{T_n s+1}{T_n s} \end{bmatrix}. \tag{4}$$

The PI output voltage is the voltage across the inductance L_{ct}, therefore the voltage at the PCC, v_{pcc}^{dq}, is added as a feedforward term to obtain the final control action.

B. PI Controller Design and Stability Analysis

The system under study is a 2x2 MIMO system and its stability can be evaluated through the analysis of the open-loop matrix eigenvalues [25]. The open-loop transfer function matrix correlates the filtered converter current in *dq* axis, $i_{convf}^{dq}(s)$, with the tracking error, $\varepsilon^{dq}(s)$.

The PI controller is designed following the procedure proposed in [25], which uses the MIMO Generalized Bode Criterion (MIMO-GBC) to asses the system stability.

The PI parameters K_p and T_n are adjusted to obtain the desired dynamics. In this case, two controllers are designed. The first one, denoted $[PI_1]$, has fast dynamics with a bandwidth of 200 Hz and a phase margin of 50 degrees, whereas the second one, $[PI_2]$, is slower with the bandwidth reduced to 90 Hz and a phase margin of 65 degrees. The controllers are designed for the system parameters given in Table I and the resulting PI parameters also appear in Table I.

The eigenvalues' Bode diagram of the open-loop matrix for both controllers is represented in Fig. 3. According to the MIMO-GBC, there are no closed-loop unstable poles in both cases and the system is stable.

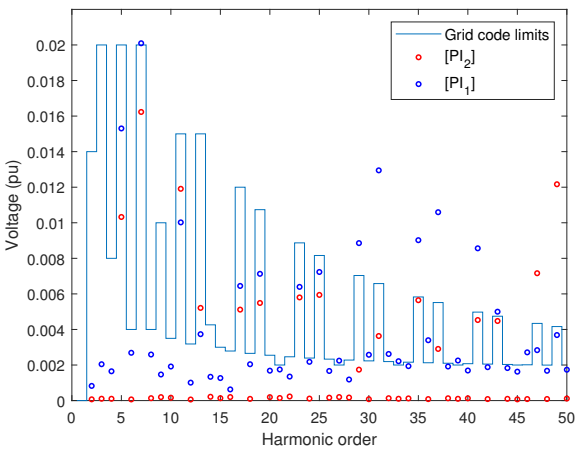

Fig. 4: Harmonic content of the voltage at the PCC for the two PI controllers.

C. Limitations of PI-based Control with SHMPWM

This subsection analyzes the steady state performance of the two PI controllers. For that purpose, the harmonic content of the voltage at the PCC with both controllers is shown in Fig. 4. It is observed that with the fast PI controller, the harmonic content worsens significantly. As the switching pattern is stored for different modulation indexes in a LUT, the fast variations in the control action force to use different switching patterns during consecutive sampling periods, which causes the harmonic content to become very distorted. In this case, the modulation index varies ± 7 %, and the control action even saturates at some points. This causes the quarter-wave symmetry not to be maintained so triplen and even harmonics appear and various harmonics do not meet the grid code. In the case of the slower PI controller the modulation index varies ± 0.5 %, so the resulting harmonic content is similar to the one showed in Fig. 2. Even in this case the grid code is not fulfilled since harmonics 47 and 49 are above their limit. In conclusion, slower controllers are required when a linear control strategy is combined with SHMPWM, which limits the dynamic performance of the converter [26].

IV. Direct Model Predictive Control Based on Finite Control Set with SHMPWM: FCS-MPC

A. Control Strategy Overview

In order to improve the system dynamic response while using SHMPWM, model predictive control is a promising alternative to PI-based control. First, a direct model predictive control strategy based on finite control set is analyzed. In [21], the authors proposed a FCS-MPC strategy combined with SHEPWM, that was adapted for grid-connected converters in [1]. The following is a brief explanation of the key aspects of the control strategy in [21], while in subsection IV-B the modification in [1] for grid-connected converters is presented.

A representation of the FCS-MPC strategy combined with SHMPWM for a NPC converter is shown in Fig. 5. The control loop consists of two parts. First, the converter voltage reference is calculated in order to inject the desired current $i_{ref}^{abc}(k)$ into the PCC (green blocks of Fig. 5). This voltage reference is obtained by solving the phasor diagram represented in Fig. 6 for phase a. The converter voltage reference phasor for this phase, V_{ref}^{a}, is given by

$$V_{ref}^{a} = V_{pcc,fund}^{a} + Z_{ct} I_{ref}^{a} \tag{5}$$

where $V_{pcc,fund}^{a}$ is the phasor of the fundamental component of the voltage at the PCC, which is obtained by using a SOGI filter [27]; I_{ref}^{a} is the fundamental current reference phasor; ϕ is the angle of phase difference between the reference current and the voltage at the PCC; and $Z_{ct} = R_{ct} + j\omega_0 L_{ct}$.

The modulation index, M, is calculated by dividing the modulus of the phasor V_{ref}^{a} by $V_{DC}/2$, and the angle of phase difference between this phasor and $V_{pcc,fund}^{a}$ is denoted as δ. The angle of the reference voltage of phase a at sample k, $\delta^{a}(k)$, is the sum of δ and the angle of the voltage at the PCC of phase a. The angles of the reference voltage vectors of phases b and c are obtained by shifting $\delta^{a}(k)$ by $-2\pi/3$ and $-4\pi/3$, respectively. With these variables, the SHMPWM look-up table is accessed. The modulation index, M, is used to select the switching pattern, while $\delta^{abc}(k)$ is used to determine the theoretical switching state of each phase. This way, the converter differential voltage at sample k associated to the precomputed switching pattern, $v_{SHM}^{abc}(k)$, is obtained.

Second, a closed-loop control is performed in order to track both the current and voltage references, $i_{ref}^{abc}(k)$ and $v_{SHM}^{abc}(k)$ (orange block). For that purpose, the converter current at the next sample $i_{conv}^{abc}(k+1)$ is estimated with the objective of minimizing the tracking error at the sample *k + 1*. This is done using the discrete-time model of the plant, which is an inductance with a series resistance in the system under study

$$i_{conv}^{abc}(k+1) = (1 - \frac{R_{ct}T_s}{L_{ct}}) i_{conv}^{abc}(k) + \frac{T_s}{L_{ct}}(v_{conv}^{abc}(k) - v_{pcc}^{abc}(k)). \tag{6}$$

Where $v_{conv}^{abc}(k)$ is the differential voltage applied by the converter and $v_{pcc}^{abc}(k)$ is the voltage at the PCC.

The converter current, i_{conv}^{abc}, and the voltage at the PCC, v_{pcc}^{abc}, are filtered using a low pass analog filter, $LPAF(s)$, with a cutoff frequency of $f_s/2$, to filter noise at the switching frequency. Note that FCS-MPC should run at higher sampling frequencies than PI-based control strategies [28], thus the cutoff frequency of the filter is higher in this case. There is also one sample delay due to the computational time of the DSP that must be compensated [29]. In the case of the converter current, the measured variables, $i_{conv}^{abc}(k-1)$ and $v_{pcc}^{abc}(k-1)$, and the differential voltage that has been applied by the converter in the previous sampling period, $v_{conv}^{abc}(k-1)$, are used in (6) to estimate the value of the current at time kT_s, $i_{conv}^{abc}(k)$. For the voltage at the PCC, $v_{pcc}^{abc}(k)$ can be computed from $v_{pcc}^{abc}(k-1)$ assuming that it is a sinusoidal waveform.

Therefore, the control objective is to track the current reference $i_{ref}^{abc}(k+1)$, while the converter voltage $v_{conv}^{abc}(k)$ resembles the precalculated SHMPWM pattern. This goal is expressed in an objective function, $J(k)$, that has two terms and is evaluated every sampling period for the 27 possible switching states of a NPC converter. The control action applied

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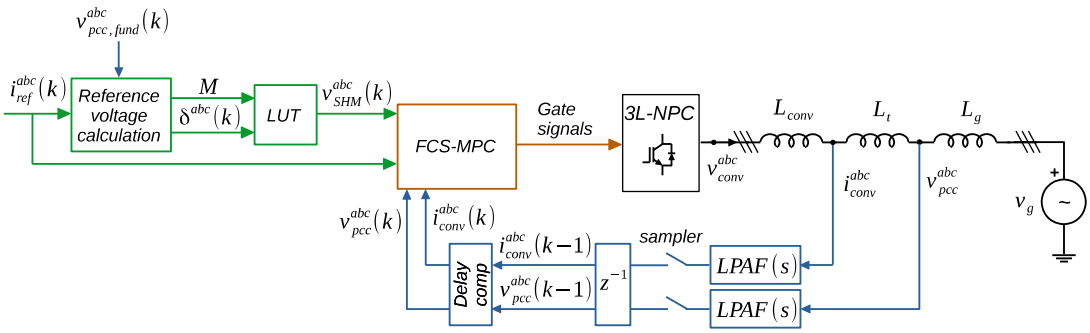

Fig. 5: Representation of the FCS-MPC strategy combined with SHMPWM for a three-level NPC power converter connected to the grid.

by the converter will be the one that minimizes the following objective function

$$J(k) = \frac{\|i_{conv}^{abc}(k+1) - i_{ref}^{abc}(k+1)\|_2^2}{I_n^2} + \sigma(k)\frac{\|v_{conv}^{abc}(k) - v_{SHM}^{abc}(k)\|_2^2}{(V_{DC}/2)^2}, \tag{7}$$

where $v_{conv}^{abc}(k)$ are all the tentative differential converter voltages that lead to the predicted currents $i_{conv}^{abc}(k+1)$; and $v_{SHM}^{abc}(k)$ is the required differential converter voltage to obtain the reference current $i_{ref}^{abc}(k+1)$ in steady state. This reference current at *k + 1* is obtained from $i_{ref}^{abc}(k)$ assuming that it is a sinusoidal waveform. I_n is the rated converter current and $\sigma(k)$ is a weighting factor used to adjust the closed-loop performance, which is defined as explained in [21]

$$\sigma(k) = \begin{cases} \bar{\sigma}(k) & \text{if } \sigma_{min} \leq \bar{\sigma}(k) \leq \sigma_{max} \\ \sigma_{min} & \text{if } \bar{\sigma}(k) < \sigma_{min} \end{cases} \tag{8}$$

where

$$\bar{\sigma}(k) = \sigma_{max} - \frac{(i_{conv}^{abc}(k) - i_{ref}^{abc}(k))^T (i_{conv}^{abc}(k) - i_{ref}^{abc}(k))}{I_n^2}. \tag{9}$$

B. Limitations of the FCS-MPC Strategy

FCS-MPC strategies combined with SHMPWM can introduce additional commutations specially in the case of model parameters uncertainties, grid transients or steady state error [30]. This might be dangerous for the power converter since it may be working close to or above its thermal limits, thus

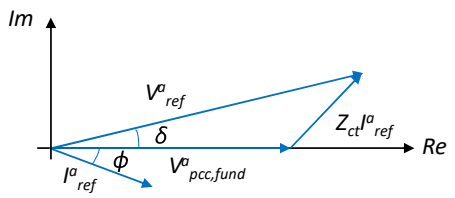

Fig. 6: Phasor diagram of the voltage and current of phase a.

a modification in the cost function as proposed in [1] is introduced to reduce the switching effort

$$J(k) = \frac{\|i_{conv}^{abc}(k+1) - i_{ref}^{abc}(k+1)\|_2^2}{I_n^2} + \sigma(k)\frac{\|v_{conv}^{abc}(k) - v_{SHM}^{abc}(k)\|_2^2}{(V_{DC}/2)^2} + \lambda_{sw}(k)\frac{|u^{abc}(k) - u^{abc}(k-1)|}{3}, \tag{10}$$

where u^{abc} denotes the switching state of the three phases, which can take the values 1, 0 or -1 for each phase leg. Notice that switching between 1 and -1 in a phase leg is prohibited.

$\lambda_{sw}(k)$ is a variable weighting factor that is adjusted to avoid consecutive switching transitions. The general idea is to penalize any switching right after a commutation occurs and allow switching close to the precomputed SHMPWM switching pulses. Thus, $\lambda_{sw}(k)$ is given by

$$\lambda_{sw}(k) = \lambda(k)|\delta^{abc}(k) - \alpha^{abc}|, \tag{11}$$

where $\delta^{abc}(k)$ is the reference voltage angle for each phase leg and α^{abc} is the closest switching angle of the SHMPWM pattern.

This way, when the distance to the precomputed SHMPWM switching angle decreases, so does the cost. The parameter $\lambda(k)$ can take the values λ_{max} or λ_{min} depending on when a commutation has occurred. For example, given phase a, we denote the next switching angle α_i^a and the following one α_{i+1}^a. Besides, we can define the distance between them as $d_i^a = \alpha_{i+1}^a - \alpha_i^a$. We suppose that when $\delta^a(k) = \alpha_i^a$ a switching occurs. In that moment the value of $\lambda_{sw}(k)$ increases so that any switching is penalized, which is done by setting $\lambda(k) = \lambda_{max}$. When $|\delta^a(k) - \alpha_{i+1}^a| < d_i^a/2$, $\lambda(k)$ is set to λ_{min} so that the weighting factor is reduced and switching is permitted again.

The parameters λ_{min} and λ_{max} as well as σ_{min} and σ_{max} are adjusted through simulations [31]–[33] so that the total number of commutations is close to the expected 132 commutations per fundamental period and the converter voltage is similar to the SHMPWM pattern. Extra commutations are allowed when the current error increases, but it is limited to 10 % more. The values for the weights are given in Table I.

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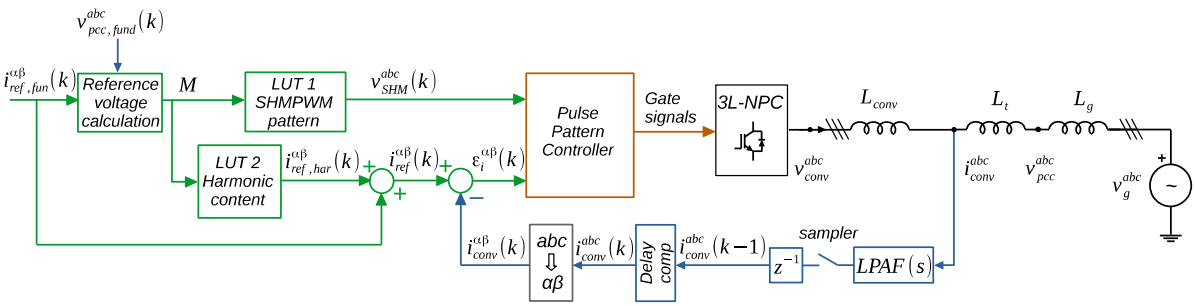

Fig. 7: Representation of the MP3C strategy for a three-level NPC power converter connected to the grid.

Another limitation of the FCS-MPC strategy combined with SHMPWM is that, sampling introduces a quantization effect in the precalculated SHMPWM pattern. In order to avoid skipping commutations, the sampling period should be lower or equal to the minimum pulsewidth. The sampling period is limited by the computation capabilities of the DSP. Thus, it may be necessary to increase the minimum pulsewidth to meet this requirement, which may result in a suboptimal solution of the SHMPWM problem that requires a larger filter to comply with the grid code.

V. Direct Model Predictive Control with Implicit SHMPWM: MP3C

A. Control Strategy Overview

Another alternative is the use of direct model predictive control strategies with an implicit SHMPWM, such as MP3C [13]. The controller modifies the precalculated switching pattern in a certain prediction horizon, T_p, in order to correct the current error. Only the modifications that fall within the next sampling period, T_s, are applied and, at the next sampling instant, the solution is recomputed over a shifted horizon. This section briefly explains the control strategy proposed in [13] in order to understand the main differences with the FCS-MPC strategy.

Fig. 7 shows a representation of the MP3C strategy. This control loop also consists of two parts, as in the previous strategy. Indeed, the first part is the same as before, namely the calculation of the converter voltage reference. In this case, the modulation index, M, is used to access two look-up tables. In the first LUT, the precalculated SHMPWM pulse pattern, $v_{SHM}^{abc}(k)$, associated to the modulation index M is selected, and, using the second LUT, the corresponding harmonic current reference, $i_{ref,har}^{\alpha\beta}(k)$, is obtained. There are two options to compute this harmonic current reference. The first one is to store this reference at certain time instants for one fundamental period. The second option is to store the Fourier coefficients of the converter voltage harmonic content. Then, the harmonic current reference is calculated using Fourier series and knowing that this voltage is applied to an inductive filter. In both cases, the harmonic content is computed offline and it is stored in a LUT. However, these two options require knowledge of the grid inductance, which is a major disadvantage of this strategy, since it is generally unknown. The fundamental current reference, $i_{ref,fun}^{\alpha\beta}(k)$, is added to the harmonic reference to obtain the total current reference, $i_{ref}^{\alpha\beta}(k)$. The harmonic current could also be included in the reference current in the FCS-MPC strategy to prevent the expected ripple of the SHMPWM from being considered a current error.

The converter current, i_{conv}^{abc}, is filtered using a low pass analog filter, $LPAF(s)$. It only filters high frequency noise since this strategy controls both the fundamental and the harmonic current. Thus, the cutoff frequency is $2f_s$. As before, the delay due to the computational time of the DSP must be compensated using the voltage applied by the converter in the previous sampling period [29].

The current tracking error, $\epsilon_i^{\alpha\beta}(k)$, and the precomputed SHMPWM pulse pattern, $v_{SHM}^{abc}(k)$, are the inputs for the MP3C controller. The objective of the controller is to minimize the current error within the prediction horizon by modifying the switching angles in this horizon. For example, if a commutation in phase a is shifted by the time Δt_a as shown in Fig. 8, the current in phase a is changed by

$$\Delta i^a(\Delta t_a) = -\frac{1}{L_{ct}}\frac{V_{DC}}{2}\Delta u_a \Delta t_a, \tag{12}$$

where $\Delta u_a = u_{a1} - u_{a0}$. u_a denotes the switching state of phase a. $\Delta t_a = t_a - t_a^*$, t_a^* being the precomputed switching time and t_a the actual switching time.

The same applies to phases b and c. The total correction of the current within the prediction horizon in $\alpha\beta$ axis is given by

$$\Delta i^{\alpha\beta}(\Delta t) = -\frac{1}{L_{ct}}\frac{V_{DC}}{2}[C]\begin{bmatrix}\sum_{i=1}^{n_a}\Delta u_{ai}\Delta t_{ai}\\ \sum_{i=1}^{n_b}\Delta u_{bi}\Delta t_{bi}\\ \sum_{i=1}^{n_c}\Delta u_{ci}\Delta t_{ci}\end{bmatrix}, \tag{13}$$

where $[C]$ is the Clarke transformation matrix and $\Delta t = [\Delta t_{a1}...\Delta t_{an_a}\Delta t_{b1}...\Delta t_{bn_b}\Delta t_{c1}...\Delta t_{cn_c}]$. n_a, n_b and n_c are

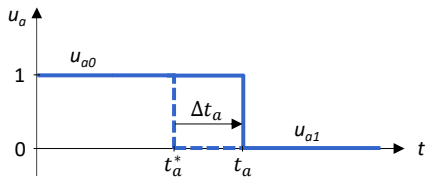

Fig. 8: Modification of a switching transition in phase a by Δt_a.

the number of switching transitions of each phase within the prediction horizon, T_p. Again, $L_{ct} = L_{conv} + L_t$.

The control objective is expressed as an optimization problem with the following objective function and constraints

$$\begin{aligned} \min_{\Delta t} \quad & \|\epsilon_i^{\alpha\beta}(k) - \Delta i^{\alpha\beta}(\Delta t)\|_2^2 + \Delta t^T Q \Delta t \\ \text{s.t.} \quad & kT_s \leq t_{a1} \leq t_{a2} \leq \ldots \leq t_{an_a} \leq t^*_{a(n_a+1)} \\ & kT_s \leq t_{b1} \leq t_{b2} \leq \ldots \leq t_{bn_b} \leq t^*_{b(n_b+1)} \\ & kT_s \leq t_{c1} \leq t_{c2} \leq \ldots \leq t_{cn_c} \leq t^*_{c(n_c+1)}. \end{aligned} \tag{14}$$

The objective function penalizes the uncorrected current error at the end of T_p and the modifications of the switching angles. The constraints ensure that the correct sequence of the precomputed SHMPWM pattern is maintained. The prediction horizon, T_p, is a design parameter but it must be chosen so that there is at least one commutation in each phase.

This optimization problem is solved using the active set method for quadratic programming. For that purpose, some simplifications must be done. The weighting factor Q is a diagonal matrix, whose diagonal terms are all set to the same value q. Also, all the commutations of each phase are modified by the same absolute value, i.e., $|\Delta t_{x1}| = \ldots = |\Delta t_{xn_x}|$, with $x = a, b, c$. The resolution of the problem includes the following steps:

1) Determine the number of switching angles per phase within the prediction horizon, n_a, n_b and n_c.
2) Compute the unconstrained solution. This solution is obtained by solving an algebraic expression that only depends on the value of q, n_a, n_b and n_c, which simplifies the resolution process.
3) Impose the constraints in (14) to the previous solution. The switching angles that violate a constraint are limited to the maximum modification allowed by the constraint, yielding the final solution. These commutations are removed from the optimization problem and the uncorrected current error is updated.
4) Iterate over these steps until the solution remains unchanged or all the switching angles are fixed.

This strategy is based on slightly modifying the already precomputed SHMPWM pattern to eliminate the current error. Therefore, it does not introduce additional commutations, which guarantees that the converter is operated within its thermal limits. Besides, we only need to adjust the control parameter q through simulations as in the previous strategy.

VI. Comparison Between PI-based and MPC Strategies Combined with SHMPWM

In this section the strategies that have been previously explained are compared in terms of real-time implementation, harmonic content grid code compliance, dynamic response and performance under low voltage ride through. For this purpose a Hardware-in-the-Loop system is used. Fig. 9 shows a schematic of the HIL test bench used for the experimental validation. The Typhoon HIL402 is used to create a model of the system with the parameters of Table I. The HIL402 allows to perform a real-time simulation of the system with a simulation step of 2 μs, which makes it possible to faithfully represent phenomena such as the dead time. Besides, it is also possible to assess the influence of the delay in the measurement acquisition and the communication. The control strategy is implemented in a commercial real-time control platform called BRAIn that includes a TMS320C6748 DSP from Texas Instrument and a XC7A35T field programmable gate array (FPGA) from Xilinx. An analog-to-digital converter transforms the analog output signals from the HIL device to digital signals. Then, the FPGA performs the data acquisition. These signals are used in the control algorithm that is implemented in the DSP. Every sampling period the DSP provides to the FPGA, where the modulator is implemented, the calculated switching times, t_{sw}, that must occur in the next sampling period. The output of the FPGA are the switching gate signals for the HIL device. Table II shows the utilization of the FPGA resources.

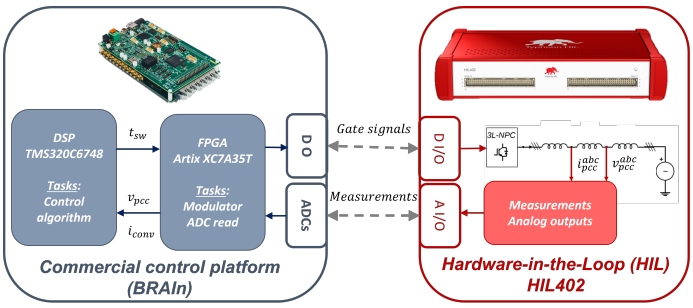

Fig. 9: Schematic of the HIL test bench used for the validation.

TABLE I: System Parameters

Parameter	Magnitude
Grid	
Fundamental frequency	50 Hz
Grid voltage	3100 V
Power converter	
Rated power	5 MW
DC bus voltage	5000 V
Switching frequency	1100 Hz
Converter output inductance	0.149 p.u.
Converter output resistance	0.005 p.u.
Transformer inductance	0.108 p.u.
Transformer resistance	0.003 p.u.
Short circuit ratio	15
PI-based control	
Sampling frequency	6 kHz
Fast PI $[PI_1]$ proportional gain, K_p	1.4518
Fast PI $[PI_1]$ integral constant, T_n	0.002
Slow PI $[PI_2]$ proportional gain, K_p	0.3384
Slow PI $[PI_2]$ integral constant, T_n	0.005
Low-pass analog filter time constant	$5.31{\cdot}10^{-5}$ s
FCS-MPC	
Sampling frequency	15 kHz
Low-pass analog filter time constant	$2.12{\cdot}10^{-5}$ s
σ_{min}	0.001
σ_{max}	0.1
λ_{min}	0.001
λ_{max}	0.2
MP3C	
Sampling frequency	6 kHz
Low-pass analog filter time constant	$1.33{\cdot}10^{-5}$ s
q	0.0001

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TABLE II: FPGA resource utilization

Resource	Utilization	Available	% utilization
LUT	7163	20800	34.44
FF	8878	41600	21.34
IO	128	250	51.20
BUFG	1	32	3.13

A. Real-time implementation in the DSP

In this subsection the execution time of the three control strategies is analyzed, which is particularly relevant when working with control strategies that are computationally demanding. Table III shows the average execution time in μs of each strategy. These execution times depend on the control platform that is used. For instance, they could be reduced if the control algorithm was implemented in a FPGA. However, what is most interesting is the comparison between the execution times of the three control strategies. It is observed that the time required to execute the FCS-MPC strategy is similar to the PI-based control strategy. The MP3C strategy takes twice as long to execute, but it can be solved in real time without an excessive computational burden. Finally, it is worth mentioning that the execution time of the FCS-MPC strategy is 55 μs, thus the minimum pulsewidth in the SHMPWM should be 55 μs to avoid skipping commutations, which almost doubles the minimum pulsewidth required by the other strategies. This is a disadvantage of this control strategy since it forces to work with a suboptimal modulation.

TABLE III: Average DSP execution times

Control strategy	Execution time
PI	50 μs
FCS-MPC	55 μs
MP3C	110 μs

B. Harmonic Emissions

Fig. 10 shows the harmonic content of the voltage at the PCC in steady state with the three control strategies compared to the limits given in the IEC61000-3-6 grid code [4]. The harmonics are measured at nominal operating conditions, that is, injecting the rated active power into the PCC with unity power factor. The spectrum of the SHMPWM reference pattern in this operation point also appears in Fig. 10 with black asterisks. As expected from the analysis of section III.C, the grid code is not fulfilled when the PI-based control strategy is applied, because the controller modifies the control action in each sampling period and the SHMPWM LUT is not accessed with a constant modulation index over the whole fundamental period. Note that the slow PI controller, $[PI_2]$, is used in the experimental validation. The THDv equals 3 % in this case.

In the case of the FCS-MPC strategy the 37th harmonic is above the limit and the THDv is also 3 %. Fig. 11 (a) shows the converter output voltage of phase a for half fundamental period, $T_0/2$. The black dashed line is the SHMPWM reference pattern, while the blue straight line is the actual voltage applied by the converter. Since this strategy does not include a modulator, in each sampling instant, the converter can switch and the voltage that minimizes the objective function is selected as control action. For this reason, it is easier that the converter voltage deviates from the precomputed SHMPWM pattern, and even additional commutations are introduced in some sampling periods. As a result, the voltage harmonics are not the precomputed ones and the grid code is not fulfilled.

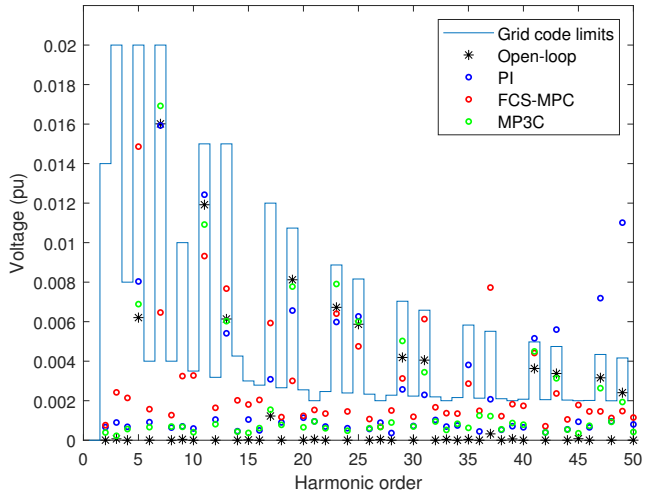

Fig. 10: Comparison of the harmonic content of the voltage at the PCC in open-loop and with the three control strategies.

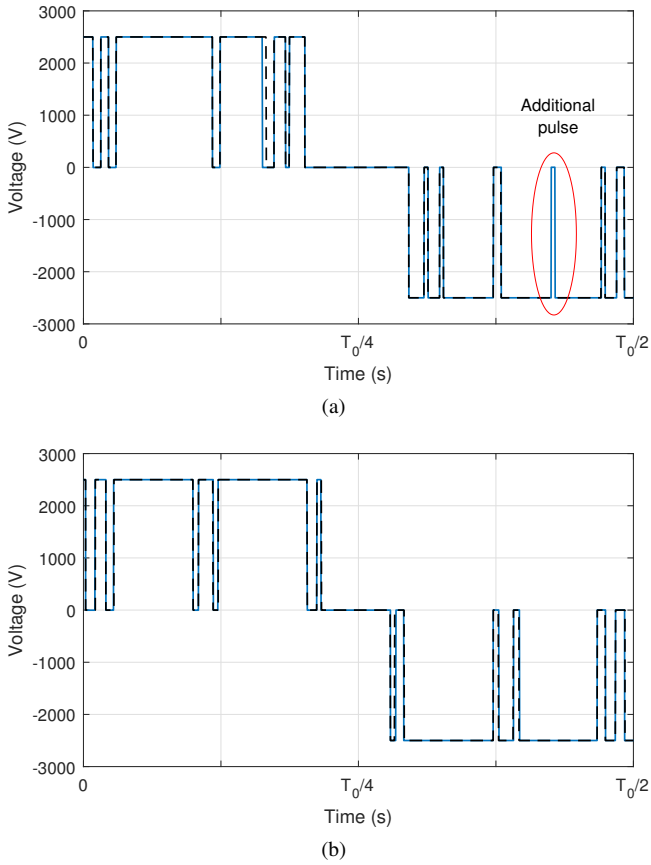

Fig. 11: Converter output voltage of phase a with the FCS-MPC strategy (a), and the MP3C strategy (b), compared in both cases to the SHMPWM reference pattern.

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Finally, the grid code is fulfilled when the MP3C strategy is used and the THDv equals 2.7 %. The converter output voltage of phase *a* is shown in Fig. 11 (b). In this case it is observed that the control strategy slightly modifies the precomputed SHMPWM pattern in steady state, thus meeting the grid code requirement.

C. Step Response

In this subsection the step response of the control strategies is analyzed. For that purpose the current reference in *d* axis is changed from 50% to 100% of the rated value, with unity power factor. In Fig. 12 it is represented the converter current in *dq* axis with the PI-based control and the FCS-MPC. It is observed that the FCS-MPC strategy has faster dynamics than the PI-based strategy. Specifically, the settling time is equal to 4 ms with the FCS-MPC strategy, whereas it is 85 ms when the PI-based strategy is implemented. Additionally, Fig. 13 shows the step response in *dq* axis of the PI-based control and the MP3C. In this case, it is also observed that the MP3C strategy has faster dynamics than the PI-based strategy, with a settling time of 5 ms. Therefore, considering only the step response, both MPC strategies offer similar and enhanced dynamics.

The current total harmonic distortion, THDi, of the PI-based control strategy is 4.8 %, that of the FCS-MPC strategy is 5.9 %, and that of the MP3C strategy is 4.6 %. It is observed that FCS-MPC has the highest THDi value, while it is lower and very similar in the other two strategies.

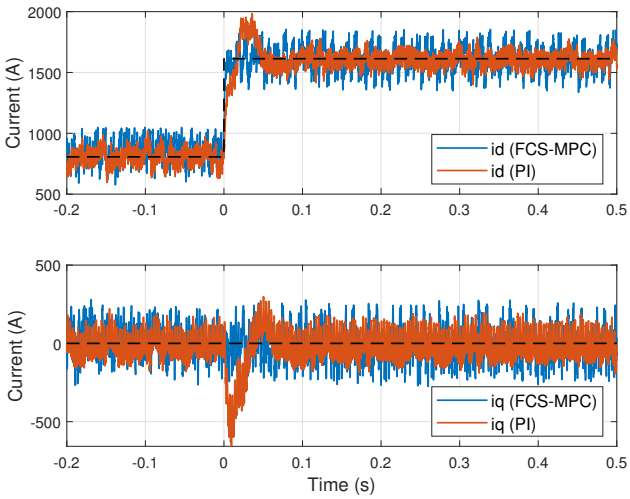


Fig. 12: Comparison of the step response in *dq* axis of the PI-based control and FCS-MPC.

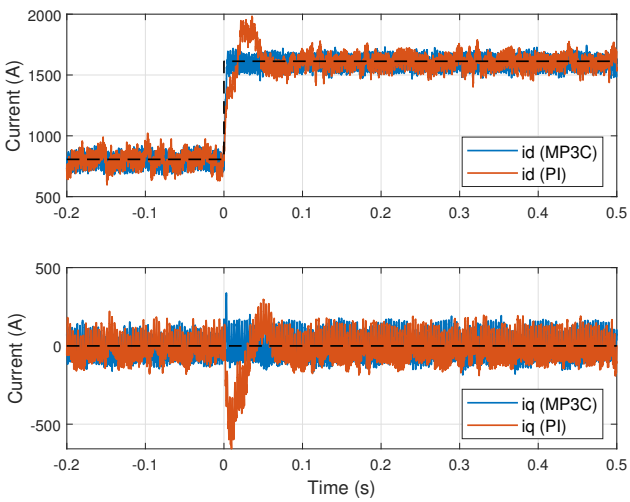
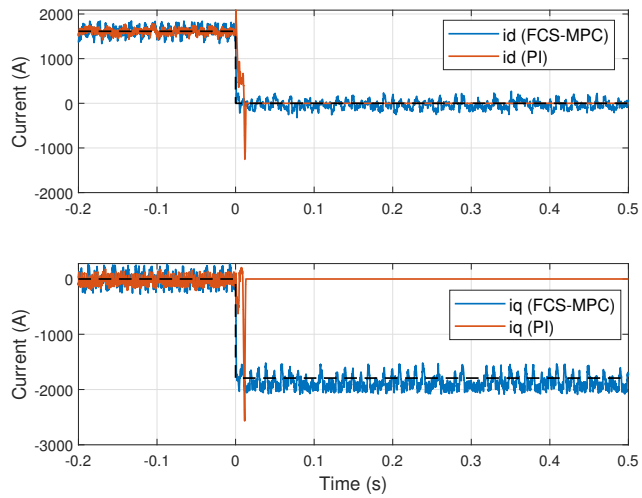


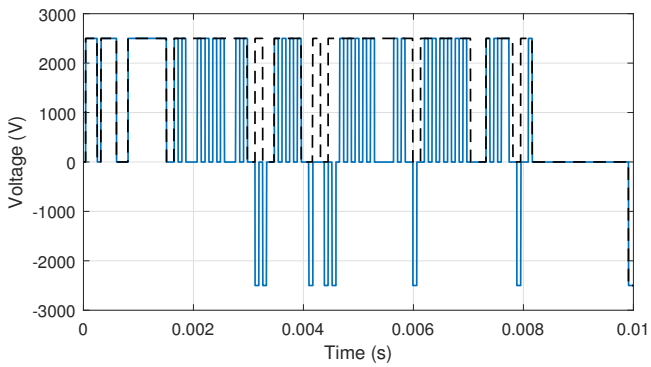
Fig. 13: Comparison of the step response in *dq* axis of the PI-based control and MP3C.

D. Low Voltage Ride Through

In this subsection the response in the case of a grid transient event such as a voltage dip is analyzed. For that purpose, the three strategies are tested under a voltage sag of 80% of the rated value. The voltage at the PCC is measured in all the methods. In the PI-based strategy it is included in the control loop as a feedforward term, whereas in the MPC strategies it is used in the calculation of the converter reference voltage. In this type of fault, grid codes in Europe require that the



(a)



(b)

Fig. 14: Comparison of the current response in *dq* axis of the PI-based control and FCS-MPC during a voltage dip (a), and converter output voltage of phase *a* of the FCS-MPC strategy compared to the SHMPWM reference pattern (b).

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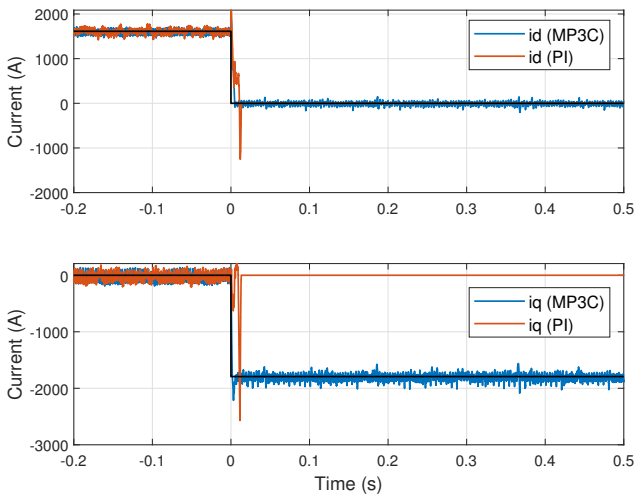
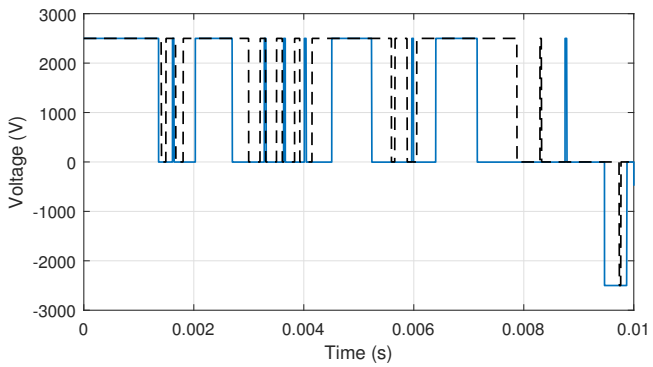
converter supplies rated reactive current with a settling time of 60 ms [8], thus the current reference in d axis equals zero and in q axis equals the rated value. Fig. 14 (a) shows the converter current during the fault in dq axis with the PI-based control and the FCS-MPC strategy. It is observed that, in the case of the PI controller, the converter trips due to overcurrent after the voltage dip. Therefore, this control strategy is not able to meet the LVRT requirement. FCS-MPC has a fast dynamic response, with a settling time of 10 ms, therefore it allows to fulfill the grid code requirement. However, FCS-MPC introduces several additional commutations right after the voltage dip, as shown in Fig. 14 (b). This figure shows the converter output voltage of phase a during 10 ms after the voltage dip. During two fundamental cycles after the voltage dip there are 300% more commutations. In order to solve this problem, the weighting factor that penalizes the switching effort should be modified during this time interval. The parameters λ_{min} and λ_{max} should be adjusted for different type of faults, and their values could be dynamically modified depending of the type of fault that occurs. This would require to perform more simulations to adjust these parameters, which is a disadvantage when working with these type of direct model predictive controllers [9].

Fig. 15 (a) shows the current response in dq axis with the PI-based control and the MP3C. It is observed that the MP3C strategy has fast dynamics, with a settling time of 15 ms, therefore it also fulfills the grid code requirement. Furthermore, on the contrary to the FCS-MPC strategy, the converter does not introduce additional commutations, as shown in Fig. 15 (b). The control algorithm modifies the precomputed switching angles to minimize the current tracking error within the prediction horizon. It is observed that the SHMPWM pattern is significantly modified after the voltage dip due to the large error that needs to be corrected, but the controller does not introduce any additional switching transitions. Thus, in this control strategy it is not necessary to readjust the control parameters for different operating points and it ensures a safe operation of the converter. For these reasons, the use of direct model predictive control strategies with an implicit SHMPWM is more suitable than the FCS-MPC strategy in the case of grid transients.



(a)



(b)

Fig. 15: Comparison of the current response in dq axis of the PI-based control and MP3C during a voltage dip (a), and converter output voltage of phase a of the MP3C strategy compared to the SHMPWM reference pattern (b).

VII. Conclusion

This paper conducts a survey of model predictive control strategies developed for their use with selective harmonic mitigation pulsewidth modulation. Two representative strategies are selected for comparison with the classical linear controller: MP3C as an example of direct model predictive control with an implicit selective harmonic mitigation modulator, and a direct model predictive control based on finite control set.

In terms of dynamic response, both MPC strategies outperform classical PI regulators. This holds also in case of grid voltage dips, as both FCS-MPC and MP3C can comply with the dynamic requirements imposed by grid codes, while PI regulators do not. Even though FCS-MPC achieves a faster dynamic response than MP3C, it introduces additional commutations, so the weights that penalize switching transitions should be readjusted in case of grid transients to avoid converter overheating. Regarding harmonic emission grid code compliance, only MP3C complies. In PI-based controllers, the modulation index varies and the modulator applies different switching patterns during consecutive sampling periods, distorting the voltage and the current. FCS-MPC imposes in some sampling periods a converter voltage that differs from the precomputed switching pattern, which causes the harmonic content to deviate from the precomputed one and a failure to comply with the grid code limits.

The control strategy has an influence on the offline optimization problem of the SHMPWM switching pattern. For instance, PI regulators require continuity of the precomputed switching angles, and FCS-MPC a minimum separation between consecutive switching angles equal to the execution time of the control algorithm to avoid skipping commutations. MP3C does not impose additional requirements on the SHMPWM pattern optimization problem, so the converter output filter can be reduced in size for the same number of switching transitions. However, as a drawback, MP3C requires knowledge of the grid inductance to compute the current harmonic reference.

In summary, the combination of SHMPWM with MPC proves to be a promising solution for grid-connected power converters, since it improves the performance of traditional PI controllers that use this modulation technique. Among the MPC strategies, direct model predictive control with an implicit modulator allows to fulfill the grid code requirements in terms of harmonic emissions and dynamic response in grid transients without imposing additional requirements on the SHMPWM problem.

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REFERENCES

[1] L. Rosado, J. Samanes, E. Gubia, and J. Lopez, "Selective harmonic mitigation: Limitations of classical control strategies and benefits of model predictive control," in *2021 IEEE International Conference on Environment and Electrical Engineering and 2021 IEEE Industrial and Commercial Power Systems Europe (EEEIC ICPS Europe)*, 2021, pp. 1–6.

[2] I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy conversion and management*, vol. 52, no. 2, pp. 1114–1128, 2011.

[3] T. TenneT, "Gmbh, requirements for offshore grid connections in the grid of tennet tso gmbh," *TenneT TSO GmbH, Bayreuth, Germany*, 2012.

[4] P. CODE and C. PRIX, "Electromagnetic compatibility (emc)–part 3-6: Limits–assessment of emission limits for the connection of distorting installations to mv, hv and ehv power systems," 2008.

[5] I. of Electrical and E. Engineers, *IEEE recommended practice and requirements for harmonic control in electric power systems*. IEEE, 2014.

[6] L. G. Franquelo, J. Nápoles, R. C. P. Guisado, J. I. León, and M. A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level pwm converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3022–3029, 2007.

[7] J. R. Tibola, H. Pinheiro, and R. F. de Camargo, "Closed loop selective harmonic elimination applied to a grid connected pwm converter with lcl filter," in *XI Brazilian Power Electronics Conference*. IEEE, 2011, pp. 746–752.

[8] C. Sourkounis and P. Tourou, "Grid code requirements for wind power integration in europe," in *Conference Papers in Science*, vol. 2013. Hindawi, 2013.

[9] P. Karamanakos, E. Liegmann, T. Geyer, and R. Kennel, "Model predictive control of power electronic systems: Methods, results, and challenges," *IEEE Open Journal of Industry Applications*, vol. 1, pp. 95–114, 2020.

[10] J. Holtz and B. Beyer, "Fast current trajectory tracking control based on synchronous optimal pulsewidth modulation," *IEEE Transactions on industry applications*, vol. 31, no. 5, pp. 1110–1120, 1995.

[11] J. Holtz and . B. Beyer, "The trajectory tracking approach-a new method for minimum distortion pwm in dynamic high-power drives," *IEEE Transactions on Industry Applications*, vol. 30, no. 4, pp. 1048–1057, 1994.

[12] J. Holtz and N. Oikonomou, "Synchronous optimal pulsewidth modulation and stator flux trajectory control for medium voltage drives," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 3. IEEE, 2005, pp. 1748–1791.

[13] T. Geyer, N. Oikonomou, G. Papafotiou, and F. D. Kieferndorf, "Model predictive pulse pattern control," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 663–676, 2011.

[14] T. Geyer, *Model predictive control of high power converters and industrial drives*. John Wiley & Sons, 2016.

[15] V. Spudić and T. Geyer, "Model predictive control based on optimized pulse patterns for modular multilevel converter statcom," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6137–6149, 2019.

[16] E. Rohr, P. Al-Hokayem, and T. Geyer, "Control of electrical converter based on optimized pulse patterns," jun. " 4" 2019, uS Patent 10,312,793.

[17] T. Dorfling, H. d. T. Mouton, and T. Geyer, "Generalized model predictive pulse pattern control based on small-signal modeling—part 1: Algorithm," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 476–10 487, 2022.

[18] ——, "Generalized model predictive pulse pattern control based on small-signal modeling—part 2: Implementation and analysis," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 488–10 498, 2022.

[19] M. A. W. Begh, P. Karamanakos, T. Geyer, and Q. Yang, "Gradient-based predictive pulse pattern control of medium-voltage drives—part ii: Performance assessment," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 237–14 251, 2022.

[20] M. A. W. Begh, P. Karamanakos, and T. Geyer, "Gradient-based predictive pulse pattern control of medium-voltage drives—part i: Control, concept, and analysis," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 222–14 236, 2022.

[21] R. P. Aguilera, P. Acuna, P. Lezana, G. Konstantinou, B. Wu, S. Bernet, and V. G. Agelidis, "Selective harmonic elimination model predictive control for multilevel power converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2416–2426, 2016.

[22] A. Routray, R. K. Singh, and R. Mahanty, "Selective harmonic elimination and balancing of capacitor voltage in hybrid cascaded multilevel inverter using model predictive control," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2597–2602.

[23] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on industrial electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[24] D. N. Zmood, D. G. Holmes, and G. Bode, "Frequency domain analysis of three phase linear current regulators," in *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No. 99CH36370)*, vol. 2. IEEE, 1999, pp. 818–825.

[25] J. Samanes, A. Urtasun, E. L. Barrios, D. Lumbreras, J. López, E. Gubia, and P. Sanchis, "Control design and stability analysis of power converters: The mimo generalized bode criterion," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1880–1893, 2019.

[26] H. Aggrawal, J. I. Leon, L. G. Franquelo, S. Kouro, P. Garg, and J. Rodríguez, "Model predictive control based selective harmonic mitigation technique for multilevel cascaded h-bridge converters," in *IECON 2011-37th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2011, pp. 4427–4432.

[27] Z. Xin, X. Wang, Z. Qin, M. Lu, P. C. Loh, and F. Blaabjerg, "An improved second-order generalized integrator based quadrature signal generator," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8068–8073, 2016.

[28] B. Stellato, T. Geyer, and P. J. Goulart, "High-speed finite control set model predictive control for power electronics," *IEEE Transactions on power electronics*, vol. 32, no. 5, pp. 4007–4020, 2016.

[29] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 1323–1325, 2011.

[30] R. P. Aguilera, P. Lezana, and D. E. Quevedo, "Finite-control-set model predictive control with improved steady-state performance," *IEEE Transactions on Industrial informatics*, vol. 9, no. 2, pp. 658–667, 2012.

[31] P. Cortés, S. Kouro, B. La Rocca, R. Vargas, J. Rodríguez, J. I. León, S. Vazquez, and L. G. Franquelo, "Guidelines for weighting factors design in model predictive control of power converters and drives," in *2009 IEEE International Conference on Industrial Technology*. IEEE, 2009, pp. 1–7.

[32] P. Zanchetta, "Heuristic multi-objective optimization for cost function weights selection in finite states model predictive control," in *2011 Workshop on Predictive Control of Electrical Drives and Power Electronics*. IEEE, 2011, pp. 70–75.

[33] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7434–7450, 2019.