Power Loss Calculation Tool for N-level Half-bridge Sub-module Modular Multilevel Converter used for Offshore Wind Energy

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Abstract

This paper presents a power loss calculation tool for a half-bridge sub-module (HBSM) modular multi-level converter (MMC). The tool can calculate both conduction and switching losses for an N-level HBSM-MMC for a range of user specifications. A semi-analytic approach is used to estimate the steady-state behaviour to accelerate the calculations. The speed and accuracy of this tool enables holistic design optimisation of the MMC. The tool's performance is verified using a detailed PLECS model of the converter and the error rate for both conduction and switching loss is within 5%.

1 Introduction

As a result of its 24-hour availability, wind energy is regarded as more reliable than solar energy and 102 GW of new wind power systems were installed in 2021, accounting for nearly 30% of all new renewable power additions [1]. The average power rating of a single wind turbine (WT) is also increasing in conjunction with a growing market. At present, the largest WTs have rated powers of up to 14 MW, with higher power levels reported in the literature [2]. Onshore wind is the most economical way to generate power, among renewable sources onshore because it costs less to install and maintain [3,4]. In spite of this, it is subject to high variability, low operating efficiency, and adverse effects on humans and animals [5,6]. The development of offshore generation has proven to be an effective solution for addressing this issue and harnessing stronger winds (i.e. greater generation capacity, improved reliability, and a remote location.) This type of wind generation is more likely to experience high wear and tear due to stronger winds, as well as higher installation and maintenance costs, resulting in higher costs of production [7]. In the coming decades, the technology is expected to improve further, resulting in a significant decrease in the price of this product. Approximately 20% of all wind energy will come from offshore wind by 2050 [1].

Traditionally, the most common approach for offshore wind farms to transport their generated power is through HVAC systems. Depending on the distance and power ratings of the offshore wind farm, the choice of transmission mode must be carefully considered to minimize losses and ensure system stability. Increasing transmission voltage levels can improve the compensation for reactive power over longer distances, but there are limitations to the distance over which active power can be transmitted for both overhead and submarine transmission lines [9]. By utilizing HVDC transmission, these concerns can be addressed with the advancement of semiconductor technology. By rectifying an AC voltage to DC and then transmitting it, this technology eliminates the issue of compensating for reactive power.

One of the most promising systems in HVDC is the HBSM-MMC, which has the advantages of high fault tolerance and low AC side output harmonics compared to conventional two and three-level voltage source converters [10]. Traditionally, MMCs are implemented with IGBT/thyristor pairs connected in series to achieve the required voltage level, which results in a significant number of components in each converter branch. Therefore, the system's conduction and switching losses are large in comparison to other traditional systems. Power devices based on wide bandgap (WBG) materials have the potential for low on-resistance, high-temperature operation, and high switching

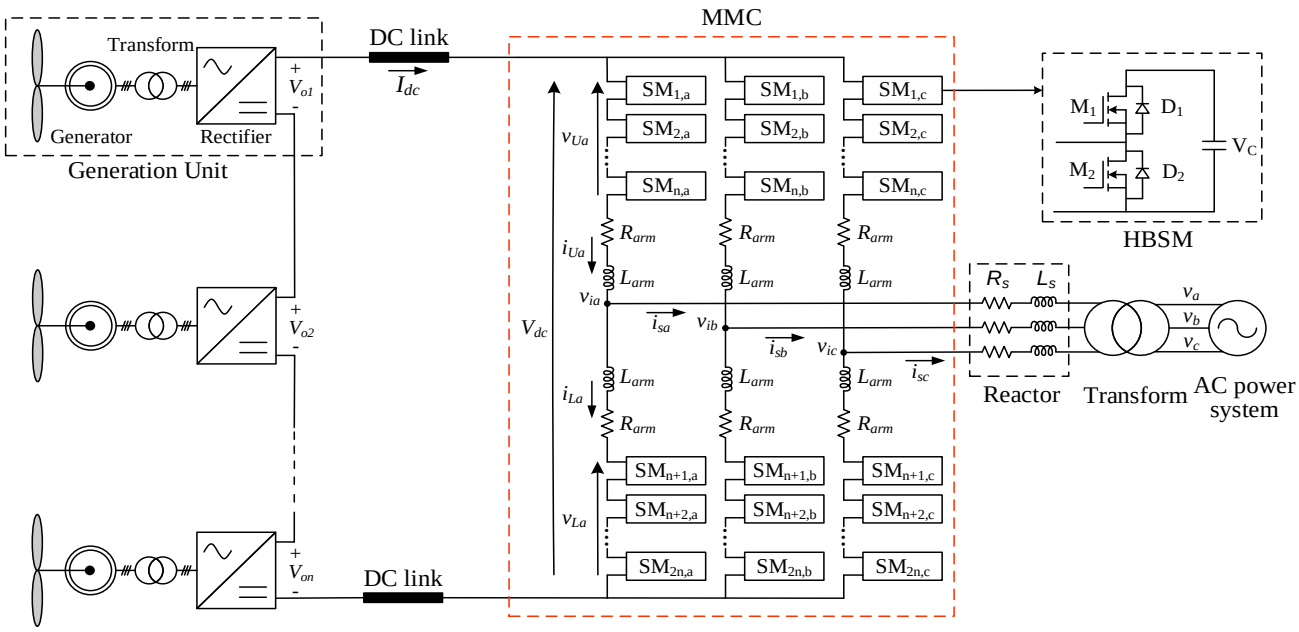

Fig. 1 MMC System in HVDC Wind Farm

frequencies, and thus are suitable for an MMC system [11].

Complex control schemes are required for an MMC. Examples include the capacitor balancing algorithm used to maintain sub-module (SM) voltages, and the circulating current suppression control (CCSC) eliminates the second-order harmonic, and thus reduces the power loss and output distortion, in the upper and lower arms. However, the DC component and higher-order harmonics cannot be eliminated by the CCSC [12]. These factors, along with the high number of SMs, make modelling and simulating the MMC time-consuming, which in turn makes determining the optimal design difficult.

MMC design is subject to a number of trade-offs. Decreasing the number of SMs reduces the conduction losses, but will require a higher switching frequency to produce the desired output voltage quality, which in turn will result in higher switching losses. Fewer SMs also places greater strain on each switching device, thus limiting the device selection range. Therefore, a tool that returns the key design parameters to meet different system requirements would be highly beneficial.

This paper aims to show the critical parameters of an MMC system in order to design an optimisation tool that uses relevant specifications to give the lowest total power loss under steady-state operation. It includes the following contributions:

- In Section 2, a review of the HBSM MMC system used in the report is presented.
- In Section 3, the main findings used to design the tool are shown as well as the operation process of the tool.
- Section 4 compares the calculation results from the tool and simulation results from PLECS.

2 Operation of HBSM MMC

2.1 Operation of the circuit

The arm of the MMC in each phase consists of n HBSMs in each arm and an arm inductor in series, which is shown in Fig. 1. Each HBSM has the following operating states: charging, discharging, and bypassing the capacitors, depending on the current direction. The operating status of the HBSM and its corresponding status in combination with the Phase Disposition (PD) Pulse Width Modulation (PWM) control scheme are presented in Fig. 2 and 3.

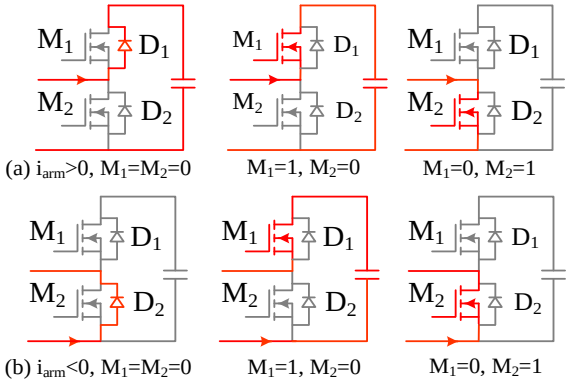

Fig. 2 Operating status of each HBSM

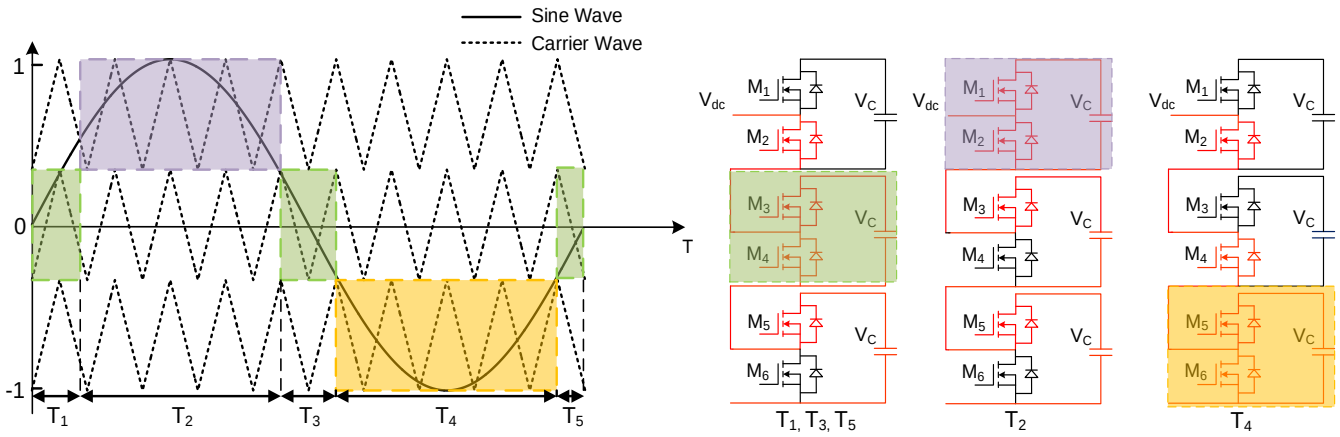

Fig. 3 Operating status combined with the PD PWM (For example the green region in the middle during T_1, T_3 and T_5 signifies regardless of current direction, the capacitor on the upper HBSM is bypassed, while the middle HBSM in green is being switched and the lower HBSM is always turned on to either charge or discharge the capacitors)

2.2 Main parameter calculation

From [13], there is always an uncontrolled circulating current in each phase which includes a constant DC component, fundamental current and mainly the second harmonics. The DC current cannot be eliminated and can be derived as follows for each phase

$$I_d = \frac{1}{4} m I_m \cos\varphi \tag{1}$$

where m is the modulation index, I_m is the maximum phase current and φ is the power angle.

In order to choose the minimum required cell capacitors size, paper [14] provides the equation shown below

$$C_{sub} = \frac{n|S|}{3\omega m V_C^2 \Delta V_{max}} \tag{2}$$

where n is the HBSM numbers in each arm, S is the system's apparent power, ω is the fundamental frequency, V_c is the SM capacitor voltage and ΔV_{max} is the maximum voltage fluctuation rate.

The series-connected arm inductor in each arm of the HB-MMC can limit the circulating current caused by the voltage difference between the DC side and phase leg. The minimum required arm inductance can be obtained according to [15]

$$L_{arm} = \frac{5n}{2\omega C_{\text{sub}} f_s} \tag{3}$$

where f_s is the switching frequency.

It can be clearly noticed that the value of C_{sub} and L_{arm} is inversely proportional to each other, as shown in Fig. 4, which uses the system specifications in table 2.

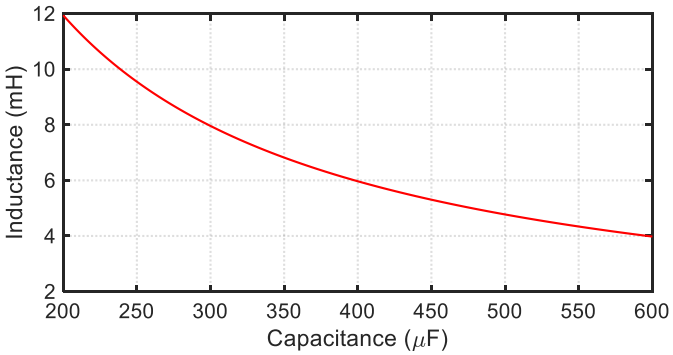

Fig. 4 The relationship of C_{sub} and L_{arm}

2.3 Control of HBSM MMC

In an ideal scenario, the submodule voltage should always be stable so that multiple levels can be generated. However, in the PD-PWM method, the uneven switching operation leads to an unbalanced voltage on the submodule capacitors. To mitigate this issue, this paper proposes the use of a bubble sort algorithm to stabilize the voltage change.

As discussed in section 2.2, a significant second harmonic can circulate through each phase, resulting in substantial power dissipation within the system [13]. To minimize the impact of these harmonics, the paper employs a PI controller [12]. This control method is aimed at reducing the level of second harmonics, to ensure optimal performance of the system and the tool.

3 Operation of the Tool

The tool uses the following assumptions:

1. It is assumed that the circulating current only contains DC and fundamental current. In other words, the PI controller can eliminate all second harmonics and ignore higher-order harmonics.

2. All the switches and capacitors are identical.

3. The voltage on submodule capacitors is all considered to be constant with the bubble sort algorithm.

3.1 Duty Cycle Ratio of PD-PWM

The PD-PWM technique utilizes multiple carriers of equal magnitude ranging from -1 to 1, as shown in Fig. 5 (a). For an N-level system, there are N-1 carriers that share the entire range. The magnitude of each carrier is calculated as $2/(N-1)$. The vertical axis boundary of each carrier area is determined by the number of carriers present in the system. In other words, the value of the multi-area boundary on the vertical axis for N carriers can be represented as:

$$Y(x) = 1 - \frac{2}{N-1}x \tag{4}$$

where N is level number (N ≥ 2) and X (1 ≤ X ≤ N) is the order number of carriers from top to bottom (1 ≤ X ≤ N). Depending on the different levels, the duty cycle should be expressed differently. Similar to [16], the duty cycle ratio of N level PD PWM can be generalised to

$$d(\alpha) = \frac{1}{2}\Big((2x - N + 1) + (N-1)V_{ref}\Big) \tag{5}$$

where $V_{ref} = sin(\alpha + \varphi)$ within which, φ is the power angle and $\alpha \in [0, 2\pi]$.

Figure 5(b) and (c) illustrate a three-level PD-PWM (N=3) with two carriers. The first carrier, C_1 ($x = 1$), is applied to the upper MOSFET of the first HBSM with a duty cycle ratio of $d_1(\alpha) = 0.5(0 + 2sin(\alpha + \varphi))$, while the lower MOSFET has a duty cycle ratio of $1 - d_1(\alpha)$. In the second HBSM, the upper switch is always on during the period with a duty cycle ratio of 1. When the reference sine wave goes negative, the second HBSM is switched and the second carrier C_2 ($x = 2$) is applied to the upper MOSFET with a duty cycle ratio of $d_2(\alpha) = 0.5(2 + 2sin(\alpha + \varphi))$, while the lower MOSFET on the first HBSM is on during the period. Furthermore, the different conduction intervals can be obtained by equating (4) and voltage reference, which is

$$m\,sin(\alpha + \varphi) = 1 - \frac{2}{N-1}x \tag{6}$$

Solving for all values of α over $[0, 2\pi]$ determines the numerous conduction intervals that are used in the equations to calculate losses.

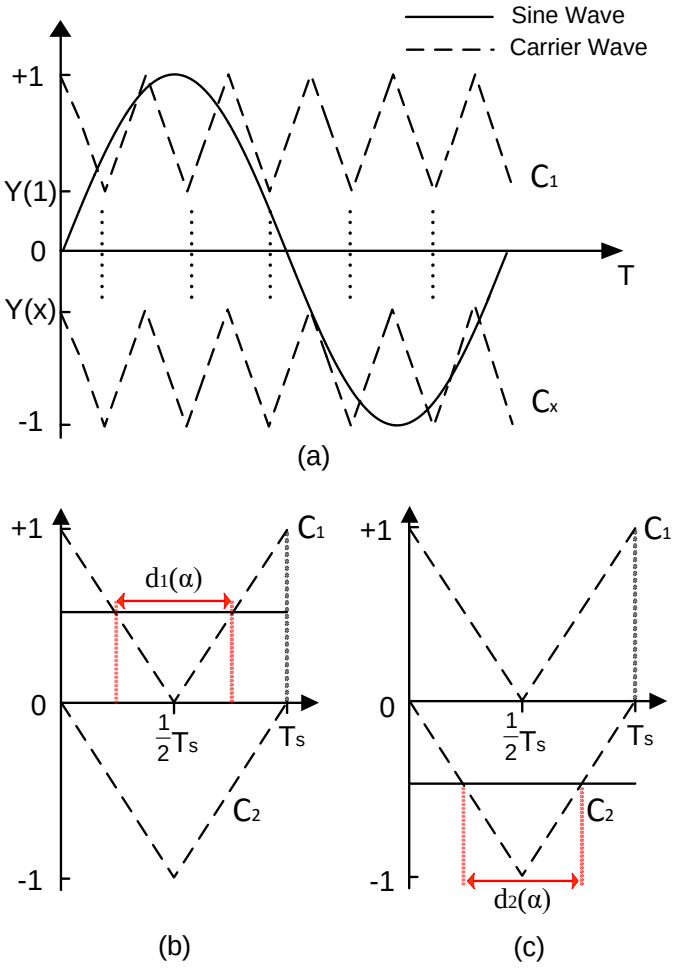

Fig. 5 The N-level PD-PWM (a) and 3-level PD-PWM for upper HBSM (b) and lower HBSM (c). (The carrier frequency is exaggerated as it is typically much higher than the fundamental frequency)

3.2 Power Loss Calculation

In this paper, only conduction loss in the channel and the switching loss are considered when synchronous conduction is applied. Based on [17], the energy loss of MOSFETs during conduction in an MMC is

$$E_{con} = v_{ds} i_{ds} d(\alpha) \tag{7}$$

where $d(\alpha)$ is duty cycle ratio and v_{ds} can be approximately expressed as $i_{ds} r_{on}$. r_{on} can be obtained from the chosen MOSFET data sheet. Thus, the conduction power loss for PD-PWM HBSM-MMC is

$$P_{con} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} i_{ds}^2 r_{on} d(\alpha) \mathrm{d}\alpha \tag{8}$$

$$P_{con} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} r_0 \left(\frac{1}{2}\mathrm{m}\, I_m \sin(\alpha) + I_{\mathrm{dc}}\right)^2 \frac{1}{2}[(2x - N + 1) + (N - 1)\, sin(\alpha + \varphi)]\mathrm{d}\alpha \quad (9)$$

$$P_{sw} = \frac{f_s V_c}{2\pi V_b}\int_{\alpha_1}^{\alpha_2} \left[A + B\left|\frac{1}{2}\mathrm{m}\, I_m \sin(\alpha) + I_{\mathrm{dc}}\right| + C\left(\frac{1}{2}\mathrm{m}\, I_m \sin(\alpha) + I_{\mathrm{dc}}\right)^2\right]\mathrm{d}\alpha \quad (10)$$

where i_{ds} is the arm current going through the MOSFET and $d(\alpha)$ is the duty cycle ratio. For an N level PD-PWM modulation HBSM MMC, the conduction power loss can be concluded in Eq. (9).

One of the switching energy loss calculation methods is to take the data from the switching energy vs drain current figure in the datasheet. Based on the present current, the switching loss can be calculated by modelling as a quadratic function [18] as shown in Fig. 6.

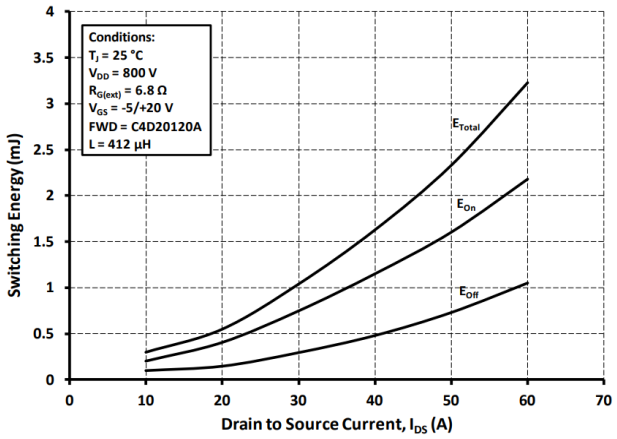

Fig. 6 Switching loss of CREE-C2M0025120D (Figure taken from [18])

The energy loss due to switching in a power converter can be determined using Eq. (10), where the coefficients A, B, and C exhibit a dependence on the switching state, i.e., whether the switch is turning on or off. However, it is important to note that the provided data sheet does not include information about the low-current range (0-10 A), which can result in increased calculation errors when using a quadratic function approximation. In particular, within the current range of 10-60 A, the quadratic approximation for turn-on switching energy loss demonstrates a more pronounced error than its cubic counterpart for most ranges except for the range between 30 A to 42 A approximately, as illustrated in Fig. 7. To enhance the accuracy of the energy loss calculation, a polynomial of a higher degree may be utilized, which can provide a more accurate estimate overall. Therefore, the degree of the polynomial should be selected based on careful consideration of the data range and the desired accuracy of the energy loss calculation.

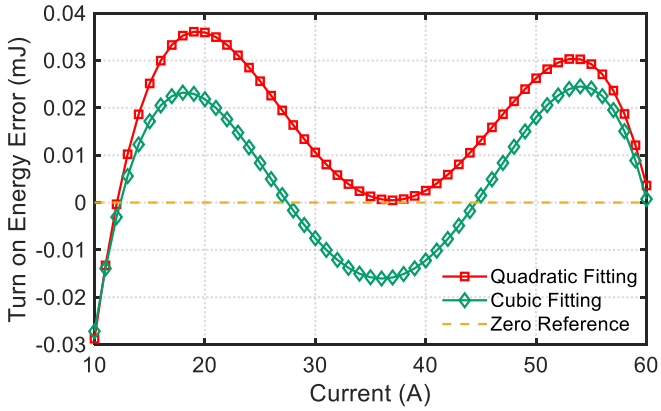

Fig. 7 Error of Turn on Switching loss approximation of CREE-C2M0025120D at 25 ℃

It is noteworthy that the bubble sort algorithm has an impact on the switching and conduction behaviour of the MOSFETs in the system, resulting in a more uniform distribution of switching and conduction intervals over each cycle when the system reaches a steady state. For switching loss, the results are almost the same as the case without the sorting algorithm for each MOSFET. Although the conduction loss for each MOSFET is different after applying the sorting algorithm, the total conduction loss for each arm during each cycle remains the same approximately which in turn does not affect the calculation process of the tool as the tool focuses on the total power loss of the system on each cycle.

3.3 Overview of the Tool

Potential devices are parameterized in MATLAB using data-sheet information, and the user specifies system parameters such as power rating (*P*), DC voltage (V_{dc}), power factor (*PF*), modulation index (*M*), and fundamental frequency (*f*). This information is used by the tool to perform an initial reduction of the design space, such as by calculating voltage and current limits to eliminate under-rated devices and determining the maximum level number based on the chosen modulation index (*M*). Furthermore, the tool also automatically calculates

the minimum values of capacitance and inductance required for the system, based on the different levels and switching frequencies specified. The tool then calculates the conduction and switching losses, based on the PD-PWM for N levels, using Eq. 6, 8, and 9, for each conduction interval. This provides an efficient and accurate tool for determining the power losses in an N-level HBSM-MMC operating under PD-PWM.

Figure 8 represents the tool's logical operating process. In particular, the user input specifications include rated power, input voltage, power factor, modulation index, fundamental frequency, level number range, and switching frequency range which are also the top seven parameters listed in table 2 for the PLECS verification.

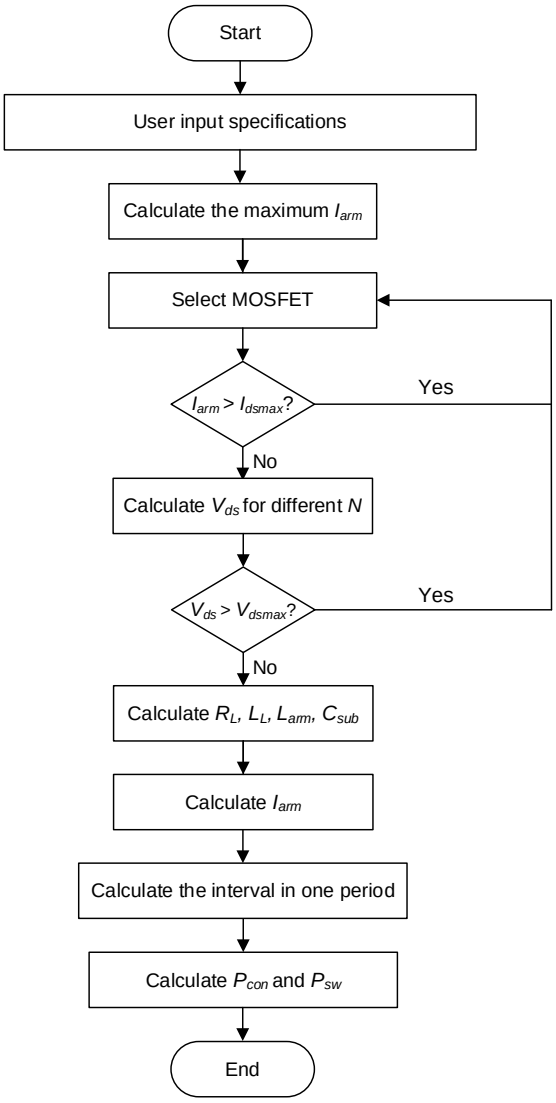

Fig. 8 Operational flow diagram of the tool

4 Results Comparison

Table 1 indicates the parameters used in a 4-level 3-phase HB MMC system built in PLECS. The system uses CREE-C2M0025120D and C3M0350120D as switches in each HBSM to verify the accuracy of the tool.

Parameters	Values
Rated Power (*P*)	5 kW
Input Voltage(V_{dc})	800 V
Power Factor (*PF*)	0.95
Modulation Index (*M*)	0.9
Fundamental Frequency (f_1)	50 Hz
Level Number (*N*)	3 - 8
Switching Frequency (f_{sw})	1 - 10 kHz
Load Resistance (R_L)	35.1 Ω
Load Inductance (L_L)	22.68 mF

Table 1 Specifications for PLECS simulation

Figures 9 and 10 illustrate the conduction and switching losses, respectively, for the upper arm in the system under consideration when using C2M0025120D devices. The losses in the upper arm of phase A in the system are illustrated before and after the implementation of the CCSC scheme. Prior to the application of the CCSC scheme, the losses in the system were found to be substantial. However, after two seconds, with the CCSC scheme, both the conduction and switching losses approach the theoretical values, which were calculated with the tool based on steady-state conditions. It is worth noting that there are certain discrepancies between the tool's predictions and the simulation results. For example, the tool assumes that the resistance r_{on} of the MOSFETs remains constant, despite the fact that it varies with the drain current I_{ds} and the drain-source voltage V_{ds} in reality. Additionally, the tool assumes that each MOSFET conducts during specific intervals, as shown in Fig. 3. In reality, however, each MOSFET conducts randomly, based on the status of the SM capacitor, which is controlled by the sorting algorithm. Despite these limitations, the error rate of the calculated conduction and switching losses was found to be within 2.5% in this case. This indicates that the tool used for calculating the losses in the system under stable state is highly accurate and can be relied upon to provide accurate results.

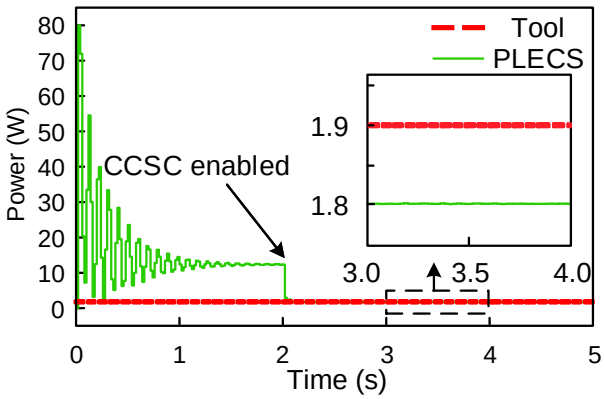

Fig. 9 Conduction loss comparison at 25 ℃ for C2M0025120D

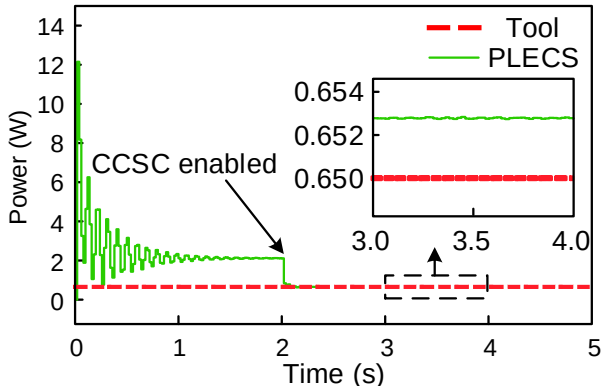

Fig. 10 Switching loss comparison at 25 ℃ for C2M0025120D

To further validate the computational tool, it was applied to a range of different MOSFETs, including C2M0025120D and C3M0350120D, and subjected to simulations with varying level numbers from 3 to 8 and switching frequencies from 1 kHz to 10 kHz. The results of the tool were compared with those obtained from PLECS simulations.

It was found that the tool provides results that are in close agreement with PLECS simulations for both MOSFETs, for example when the level number is 4 or 6 and the switching frequency is within the range of 1 to 10 kHz. The calculated results also track the tendencies observed in the PLECS simulations when the level number varies from 3 to 8 while the switching frequencies are fixed at 1 or 10 kHz. Moreover, it was observed that the difference between the simulation results and the tool results decreases as the number of levels increases when the switching frequency is kept constant. This is due to the fact that the more sinusoidal the voltage/current waveform becomes, as the number of sub-modules increases, the closer it will resemble the assumptions made in the tool, leading to improved accuracy.

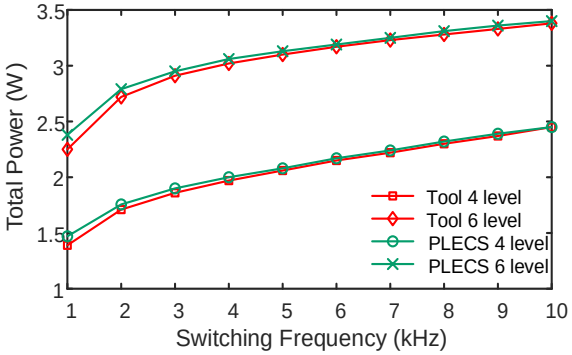

Fig. 11 Total power losses with different frequencies for C2M0025120D at 25 ℃

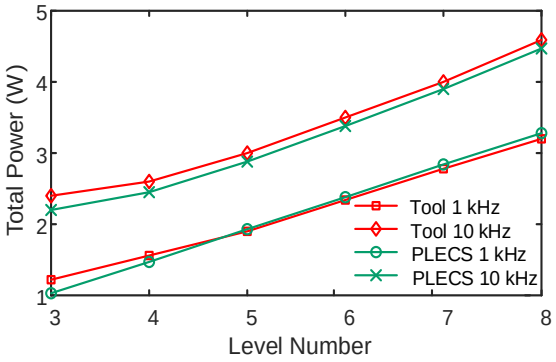

Fig. 12 Total power losses with different level numbers for C2M0025120D at 25 ℃

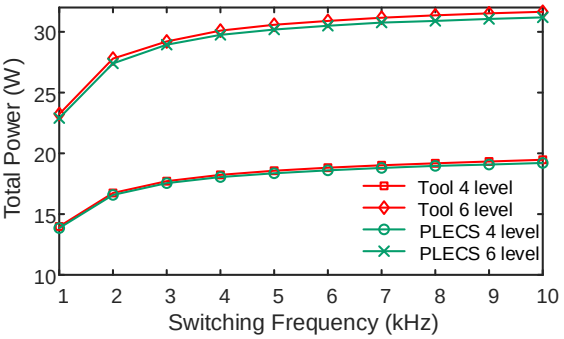

Fig. 13 Total power losses with different frequencies for C3M0350120D at 25 ℃

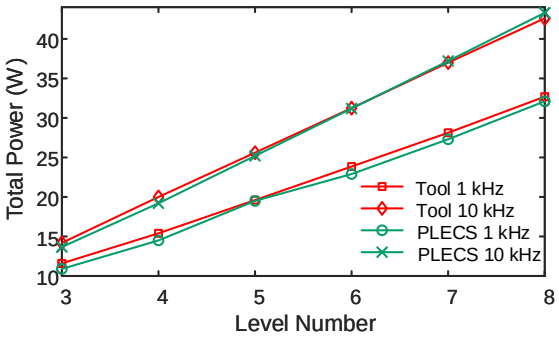

Fig. 14 Total power losses with different level numbers for C3M0350120D at 25 ℃

5 Conclusion

This paper has presented a computational tool that effectively and accurately determines both conduction and switching losses for an N-level HBSM-MMC systems operating under PD-PWM. The tool is based on the derivation of general N-level equations for the duty cycle ratio, which enable efficient calculation of power losses for a user-specified MMC system. The validity of the tool's high accuracy was verified through PLECS simulations, which showed that calculation errors were less than 5% across a range of comparisons including varying switching frequencies and leqevel numbers. This study provides a foundation for a comprehensive design optimization approach for MMC systems.

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