The Design of a Resistive Switching Characterisation Platform Based on Discrete Current-Conveyors

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***Abstract*—In this paper we propose a current-conveyor based circuit to characterise resistive switching devices. The circuit relies on open-loop current-mode techniques that are in principle faster than existing solutions that rely on transimpedance amplifiers for biasing and current sensing [1]. The circuit is able to apply a voltage across a test device and simultaneously provide a measure of current flowing through it. The circuit therefore, results in a compact solution that can be scaled-up to characterise crossbar devices in parallel. In this paper we describe, simulate and evaluate a discrete version of the proposed circuit. We also verify a PCB implementation that is capable of forming, writing and reading different types of resistive switching devices.**

I. Introduction

The development of new, non-volatile memory technologies are a popular research topic, with multiple different material stack-ups[2] and device structures[3] currently under investigation. Regardless of the material stack in use, we require purpose built instrumentation to characterise these devices. These instruments are essentially specialised Source Measure Units (SMU) with additional circuitry that can form devices, apply narrow pulses to write to them and to read their resistive states.

Fundamentally, connecting to and characterising a single device is sufficient, however, in practise these devices are fabricated in dense crossbars arranged in columns and rows of devices that need to be characterised individually[4]. Therefore, we require a circuit that is sufficiently small and power efficient to be placed on each of the row/column line of a very large dimensional array as shown in Fig. 2.

Furthermore, we require the circuit to be able to independently apply a stimulus pulse and to simultaneously measure the current being sourced/sunk into its respective row/column line during stimulation. Lastly, as these devices are usually driven with pulses, the settling time of the circuit is a key specification for overall fast operation.

This paper proposes a current-mode technique, based on a current-conveyor topology that can be used for the aforementioned purpose. Furthermore, we evaluate a discrete implementation of the circuit, suitable for the design of a SMU capable of characterising single devices.

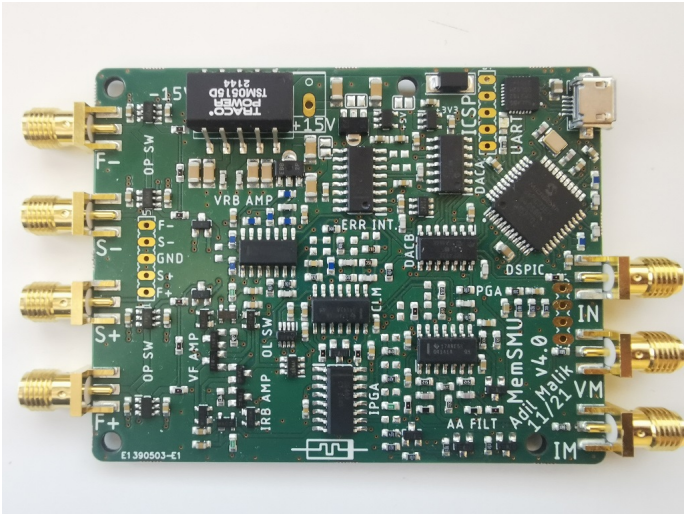

Fig. 1. The assembled PCB of the current conveyor based SMU for resistive device characterisation.

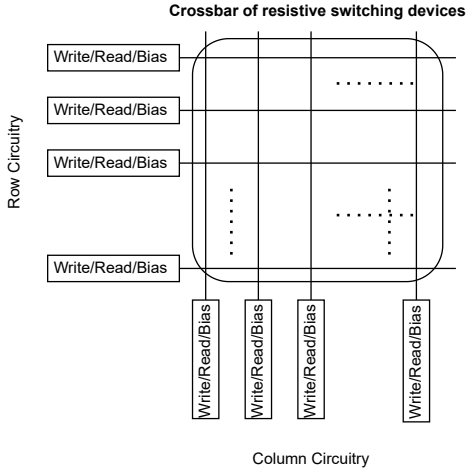

Fig. 2. A crossbar arrangement of resistive switching devices with completely independent row and column circuitry.

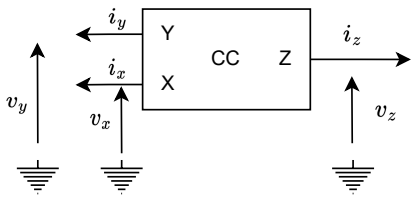

Fig. 3. An ideal current conveyor.

Section II describes the circuit and presents some key simulation results. Section III describes a practical circuit implementation built out of discrete matched bipolar transistors. Section IV describes the complete SMU unit built around the circuit (shown in Fig. 1) and finally Section V presents some experimental results.

II. Circuit Description and Simulation Results

A theoretical current conveyor [5] as shown in Fig 3 is a good candidate for a general purpose circuit for writing to and reading from a non-volatile memory cell.

$$v_x = v_y \tag{1}$$

$$i_y = 0 \tag{2}$$

$$i_x = i_z \tag{3}$$

With reference to the operating equations, the memory cell is connected to terminal X, the stimulus to terminal Y and the current is sensed at terminal Z. A write operation would consist of the application of a pulse on the terminal Y whereas the read operation would consist of the application of a pulse on terminal Y and the simultaneous measurement of the current out of terminal Z. In principle, this circuit is either used to characterise a single memory cell, or if it is sufficiently small, be used to interface to each column/row line of a crossbar to characterise each device.

Fig. 4 shows the proposed practical implementation of the circuit using commercially available matched-pair bipolar transistors.

A. Circuit Operation

With reference to Fig. 4, Transistors Q1,Q2,Q8 and Q7 form a low-offset buffer with a push-pull output stage. The current sunk/sourced into the memory cell is sensed by the current mirrors formed by Q3/Q4 and Q5/Q6. These current mirrors are cascoded via Q9 and Q10 and the current sense output is taken at the collectors of Q9/Q10. The various transistors are appropriately biased via Q11-Q14 and the bias current of the whole circuit is set by the resistor R2. The capacitors serve to decouple the various bias nodes.

The voltage that is to be applied to the memory cell is applied at the base of Q8/Q7 and appears with suitable current drive at the emitter of Q1/Q2. The current flowing through the memory cell connected at the emitter of Q1/Q2 is replicated and reproduced at the drain of Q9/Q10 which

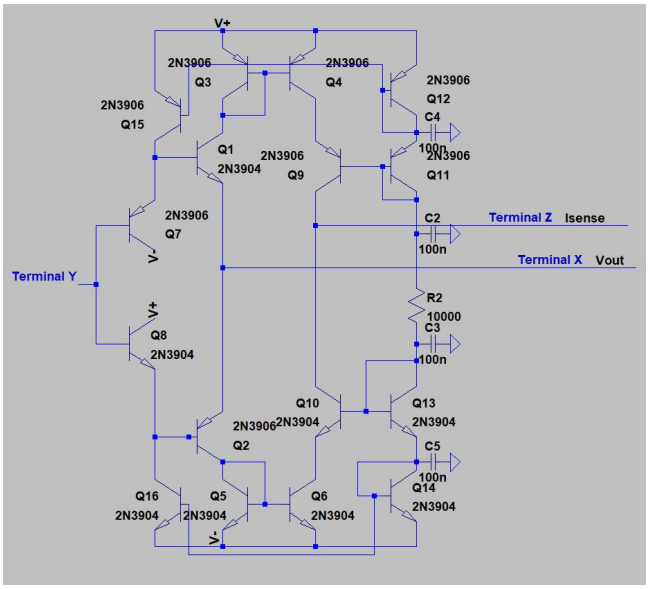

Fig. 4. A practical implementation of circuit suitable for resistive switching device characterisation.

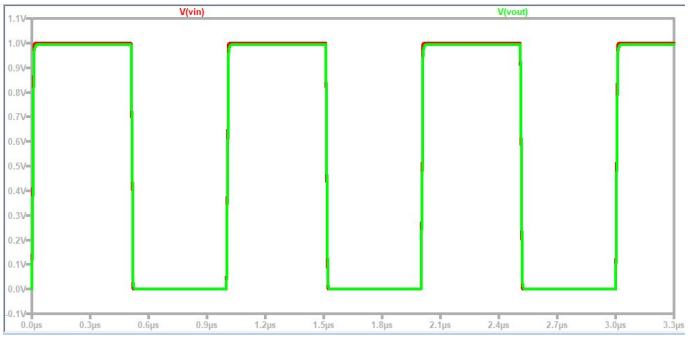

Fig. 5. Applied voltage (red) vs voltage across device (green).

serves as the output where we sense the memory cell current. The resistance of the memory cell is determined by dividing the applied voltage with the sensed current using additional instrumentation.

B. Simulation Results

Fig. 5 and Fig. 6 show the key simulation results consisting of the response of the nodes of the current conveyor when driven with a 500ns 1V pulse. The load memristance is assumed to be fixed at $10k\Omega$. Fig. 5 shows the comparison between the applied voltage (v_y) and the voltage seen across the resistive device (v_x). These track each other very well as would be expected. Fig. 6 shows the analogous comparison between the current flowing through the resistive device (i_x) and the current replicated at the sense terminal Z (i_z). Apart from an initial overshoot and settling period, these currents track each other very well. This results confirm that the circuit operates as expected and can be used as the basis of a characterisation platform.

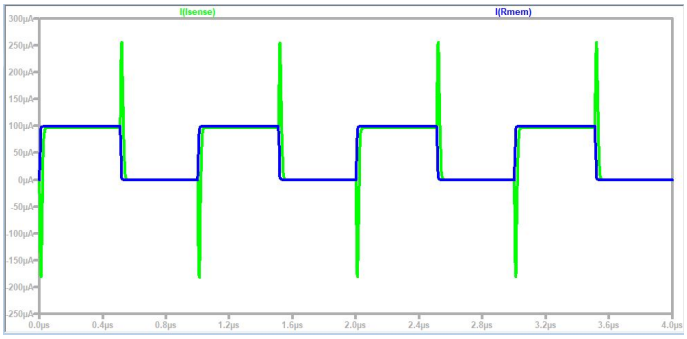

Fig. 6. Device current (blue) vs measured current (green).

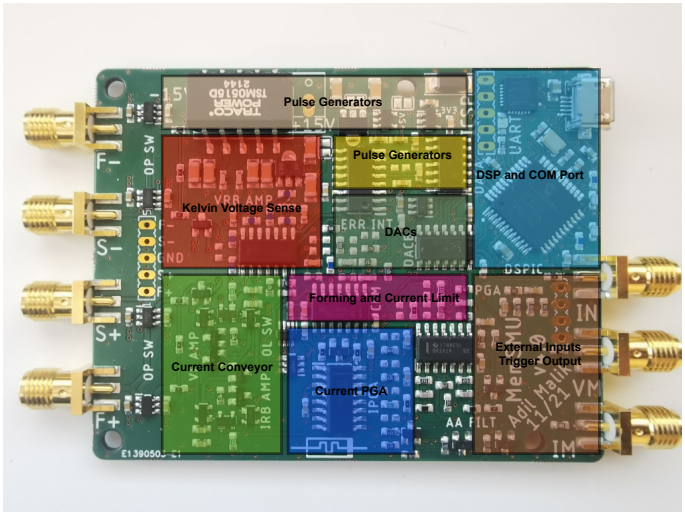

Fig. 7. The assembled PCB of the current conveyor based SMU for resistive device characterisation.

III. Printed Circuit Board Design of the Source Measure Unit

A complete Source Measure Unit (SMU) was designed around the core circuit show in in section IIA. The purpose of this design was to evaluate the performance of the core circuit and to enable the extensive characterisation of single devices. Fig. 7 shows the assembled PCB and the overlay depicts the various blocks. In addition to the core readout circuit, the design also consists of a means to adjust the gain of the current/voltage sense functionality, DACs to generate the various bias voltages and switches to generate the pulsed stimulus. Furthermore, there is also an onboard DSP with integrated 16-bit ADCs to control various circuits and to compute the state of the resistive switching devices.

IV. Experimental Setup and Results

The experimental setup consists of a probe station and a pair of needle probes accessing a single cross-point device as shown in Fig. 8. The devices consists of a Pt-TiO2-Pt stack [2]. A Graphical User Interface (GUI) was written in Visual C that controls the SMU and helps user visualise the data as a resistance vs time plot. Fig. 9 shows actual data taken from

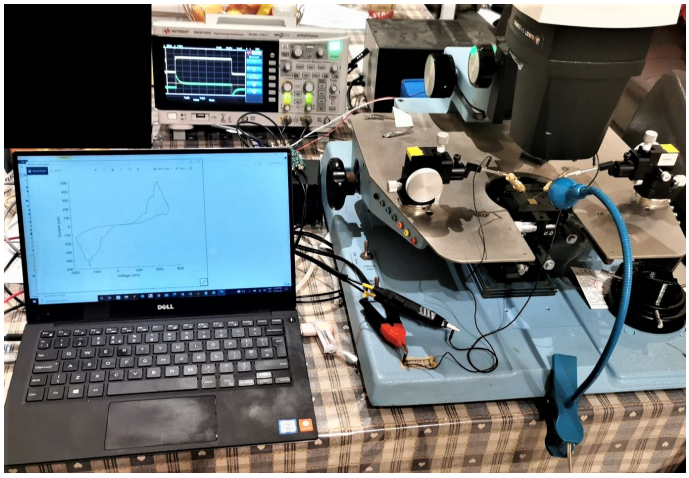

Fig. 8. The experimental setup consisting of the SMU and probe station interfacing to a single device being formed by the SMU.

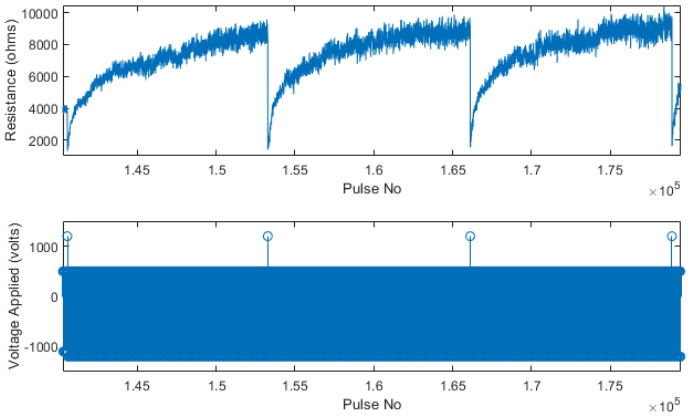

Fig. 9. Experimental output of the SMU showing the response of the memristor to a few thousand pulses. The ”noise” is inherent to our devices and not a consequence of the SMU design.

the current-conveyor based SMU where a DUT is programmed through a range of different resistive states after an initial forming step.

V. Conclusion

In this paper we have proposed a current-conveyor based circuit as the basis of a SMU for resistive switching device characterisation. The proposed circuit has enabled us to characterise our in-house Pt-TiO2-Pt devices through a wide range of operating conditions. Future work will present more comprehensive evaluation results of this SMU. As the proposed circuit is also sufficiently compact to be used as part of a monolithic crossbar characterisation platform; a CMOS variant has also been fabricated in TSMC 180nm and will be elaborated in future publications.

References

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