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High-Density Integration of Ultrabright OLEDs on a Miniaturized Needle-Shaped CMOS Backplane

Sabina Hillebrandt, Chang-Ki Moon, Adriaan J. Taal, Henry Overhauser, Kenneth L. Shepard, and Malte C. Gather**

Direct deposition of organic light-emitting diodes (OLEDs) on silicon-based complementary metal–oxide–semiconductor (CMOS) chips has enabled self-emissive microdisplays with high resolution and fill-factor. Emerging applications of OLEDs in augmented and virtual reality (AR/VR) displays and in biomedical applications, e.g., as brain implants for cell-specific light delivery in optogenetics, require light intensities orders of magnitude above those found in traditional displays. Further requirements often include a microscopic device footprint, a specific shape and ultrastable passivation, e.g., to ensure biocompatibility and minimal invasiveness of OLED-based implants. In this work, up to 1024 ultrabright, microscopic OLEDs are deposited directly on needle-shaped CMOS chips. Transmission electron microscopy and energy-dispersive X-ray spectroscopy are performed on the foundry-provided aluminum contact pads of the CMOS chips to guide a systematic optimization of the contacts. Plasma treatment and implementation of silver interlayers lead to ohmic contact conditions and thus facilitate direct vacuum deposition of orange- and blue-emitting OLED stacks leading to micrometer-sized pixels on the chips. The electronics in each needle allow each pixel to switch individually. The OLED pixels generate a mean optical power density of 0.25 mW mm^{-2}, corresponding to >40 000 cd m^{-2}, well above the requirement for daylight AR applications and optogenetic single-unit activation in the brain.

1. Introduction

Organic light-emitting diode (OLED) technology has revolutionized our ability to realize portable, high-resolution displays for smartphones and TVs. OLEDs consist of thin layers of organic semiconductor materials that are sandwiched between two conductive electrodes, one of which is (semi)transparent. This stack design makes them a few hundred nanometers thin. Unlike conventional LEDs, because of their vertical structure, they can emit from the entire device surface area, thus dramatically enhancing fill factor. Due to their direct emission, OLED pixels offer high contrast at low power consumption. The amorphous, thin film nature of OLEDs allows for their integration on many different substrates, including transparent glass, fully flexible substrates with thin-film transistor backplanes, and substrates with unconventional forms and shapes as well as opaque silicon-based backplanes. Silicon-based substrates containing complementary metal–oxide–semiconductor (CMOS) circuits allow serial addressing and active driving of pixels with unmatched spatial and temporal resolution.[1] This has facilitated wearable AR/VR near-eye devices with high fill-factor arrays of micrometer-sized pixels, yielding resolutions >5000 ppi.[2,3] Furthermore, the fabrication of OLEDs on CMOS backplanes is compatible with high-throughput wafer-level processing for parallel device fabrication.

While today's OLED displays reach sufficient brightness for most applications in consumer electronics (where the typical requirement is a luminance of 300–1000 cd m^{-2}), many emerging applications, in particular near-eye daylight AR and biomedical applications, require much higher luminance levels.[4–6] For instance, to provide readable information, head-mounted displays (HMDs) need to reach an ambient contrast ratio of at least 3:1 against a bright background, e.g., in avionics and automotive use. With the background luminance of an average clear sky being around 8000 cd m^{-2}, the operational light output requirement of HMDs is thus in the range of several 10 000 cd m^{-2}.[7,8] Furthermore, any OLED-based lightengine will need to be integrated with the optical combiner in a light-efficient manner, while keeping footprint and weight to a minimum.[5] To achieve

S. Hillebrandt, C.-K. Moon, M. C. Gather
Organic Semiconductor Centre
SUPA School of Physics and Astronomy
University of St Andrews
North Haugh, St Andrews KY16 9SS, UK
E-mail: sabina.hillebrandt@uni-koeln.de; mcg6@st-andrews.ac.uk
S. Hillebrandt, C.-K. Moon, M. C. Gather
Humboldt Centre for Nano- and Biophotonics
Department of Chemistry
University of Cologne
Greinstr. 4–6, 50939 Cologne, Germany
A. J. Taal, H. Overhauser, K. L. Shepard
Columbia University
New York, NY 10027, USA

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adma.202300578

DOI: 10.1002/adma.202300578

this, the compatibility of OLEDs with substrates having unconventional, non-rectangular form factors may prove useful, but this has not been studied in detail for OLEDs on CMOS backplanes. Another example of an ultrahigh brightness application of OLEDs is as a light source in optogenetics. Optogenetics is an emerging method in neuroscience that uses genetic modification of brain cells to render them light sensitive, thus achieving non-contact and minimally invasive all-optical control of neuronal networks, with applications ranging from basic research in animal models to potential future medical use in patients.[9,10] In optogenetics, light sensitivity is conferred through the introduction of light-switchable ion channel proteins, typically channelrhodopsins (ChRs), into the cell membrane of neurons. First generation ChRs required relatively high intensity blue light, but recent advances in ChR design enable stimulation with orange to red light at intensities of a few tens of μW mm^{-2}.[11] However, to achieve spatially controlled light delivery deep inside the brain, it would be useful to have implantable light sources that mimic the shank-shaped electrical stimulation arrays already used in the neuroscience community.[12]

Inorganic LEDs are an obvious choice for high brightness applications, and high brightness inorganic LEDs can be readily fabricated at the micrometer scale. However, the fabrication of these micro-LEDs is based on epitaxial growth, typically on sapphire substrates, which greatly limits the fill factor and maximum number of micro-LEDs that can be integrated on a CMOS backplane because they have to be transferred and attached to the corresponding contacts on the substrates with a (sometimes manual) pick and place approach or via (monolithic) array hybridization.[13–16] Patterning of the growth wafer can in this case be performed before or after the bonding process, but needs extra photolithography steps in order to achieve high resolution micro-LED arrays.[17–19] By contrast, the amorphous organic layers forming an OLED can be deposited directly on the CMOS backplane. The emissive area of each OLED pixel on the backplane is then merely defined by the size and shape of the underlying anode pad. Anode pads on a CMOS backplane can be readily scaled to micrometer-sized dimensions using commercially available high-throughput semiconductor device fabrication in a silicon foundry. As such, pixel size and pixel number are no longer limited by the resolution achievable by deposition through shadow masks and the number of separate electrical contacts that the device can have without becoming too bulky.

The brightest single color, monochromatic OLED microdisplays based on CMOS backplanes currently reach 5000 cd m^{-2} at 7 V[20] or 5.5 V[21] and 24 000 cd m^{-2} at 9 V,[22] also see ref. [23] for a comprehensive review on the performance of current OLED microdisplays. An important remaining challenge is achieving a higher pixel brightness in high resolution displays (HD/UXGA), which is needed for AR/VR applications as well as for optogenetic single cell stimulation. A further issue is that most publications on OLED microdisplays do not reveal details on the used OLED stack architecture, materials, and fabrication process.

Conventional CMOS technology is limited in the forward voltage that it can provide to OLEDs, generally to 5–7 V.[24] High-voltage implants in custom CMOS processes can sustain voltages up to ≈20 V, but this comes at the cost of integration density due to spacing constraints. Therefore, to fully exploit the scalability of modern CMOS processes with OLED technology, doped charge-transport layers are essential to achieve high brightness at the low voltages provided by OLED-on-CMOS devices.[25] Ensuring sufficient operational stability for these high brightness OLEDs is also challenging but can be achieved by careful choice of injection layers, suitable stack design and thin film encapsulation, the latter rendering the devices stable under a wide range of conditions, including even in water or inside biological tissue.[26–28]

Even with the above points addressed, a remaining important requirement for OLED-on-CMOS integration is the creation of ohmic contacts to ensure optimum performance in terms of brightness, stability, and yield. The morphology and surface composition of the contact, which is typically formed by aluminum, depends on the foundry and the available processes. To make use of existing standard CMOS processes, the aluminum contacts must be defined using the same layers and process as the bondpads on conventional CMOS chips. For these bondpads the aluminum is purposely grown with large grain sizes to generate a rough "wire-bondable" surface, and the pads are further deposited within etched wells for electrical isolation and subject to various cleaning steps before leaving the foundry. This results in oxidized aluminum surfaces with a rough surface topology. Removal of the surface aluminum oxide layer by chemical–mechanical polishing (CMP) can improve the contact quality but is time-consuming and can contaminate the pads with surrounding passivation material.[21] Another way to improve the quality of the aluminum pad is to passivate them with a thin layer of titanium nitride (TiN), preferably before the wafers leave the foundry.[29] The work function of TiN allows for decent OLED performance; however, brightness and efficiency are typically reduced compared to devices with indium tin oxide (ITO) anodes. Furthermore, a TiN process is not available in most silicon foundries.

Here, we demonstrate the deposition of high-brightness, high-yield OLED arrays on needle-shaped CMOS backplanes, using standard foundry-provided aluminum contact pads to define the OLED pixels. To guide our process optimization, we first determine the thickness and composition of the topmost contact layer. We then establish a plasma process that allows to condition the aluminum contacts at wafer or die level or even on processed and fully packaged CMOS dies. We optimize the aluminum contacts for OLEDs by applying reactive ion etching as well as a 3 nm-thick silver interlayer that improves charge injection through the surface oxide layer. To further optimize brightness, we used p–i–n orange- and blue-emitting OLED multilayer stacks. Pixel homogeneity and yield are investigated for a range of different wafer processing steps by directly depositing these OLEDs on prototype silicon dies with varying pixel sizes. Using the resulting optimized process, we achieve a pixel yield of >90% on CMOS chips that have undergone trenching to define the needle shape and standard wire bonding to a printed circuit board before the deposition of OLEDs. The final devices comprise four needles with a length of 6 mm, a thickness of 75 μm, a width of 150 μm, and a total of 1024 OLED pixels each measuring 19 × 21 μm^{-2}. The OLED pixels on these devices reach a mean power density of 0.25 mW mm^{-2} at 7 V, corresponding to >40 000 cd m^{-2} for the orange-emitting OLEDs. The device shape and design presented here is of particular use for applications in deep-brain stimulation where our device promises to bridge a current technology gap, namely, to achieve cell specific light stimulation in

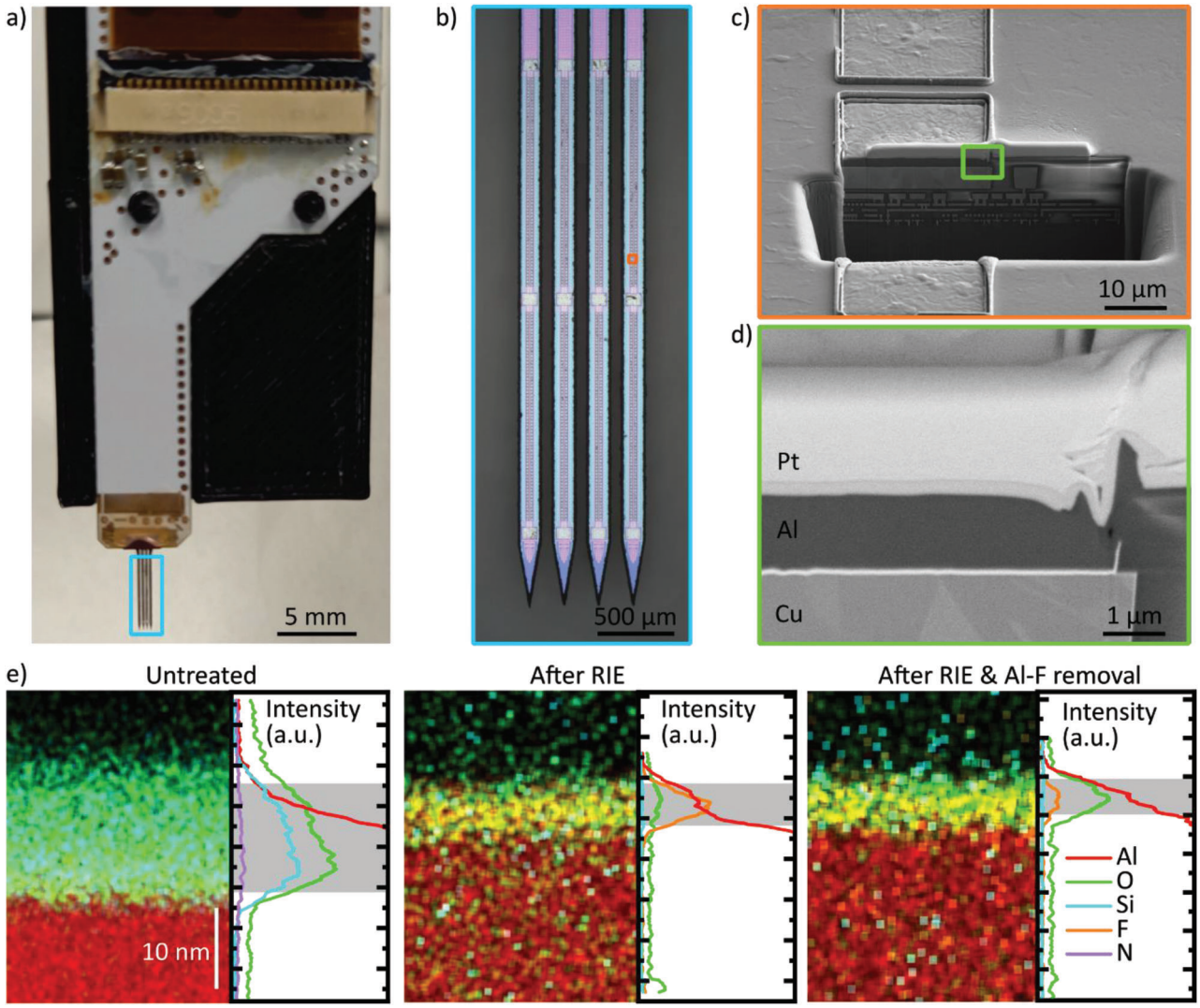

Figure 1. a) Shank-shaped CMOS device wire bonded to a PCB that in turn is connected to an external driver board with a flat band cable. b) Microscopy image of the blue-marked area in (a), showing the four needles and the individual anode pads onto which OLEDs are deposited. Each needle contains three larger cathode pads at the top, center, and end of each needle. c) Scanning electron microscopy (SEM) image of the area marked in orange in (b), with a focused ion beam (FIB) cross-section through the upper layers of the CMOS device and thus revealing the driving circuit underneath the anode pads. d) SEM image of the green marked area in (c), showing the Cu interconnect layer, the aluminum contact, and the side walls of the pad. The Pt surface layer was deposited during the preparation of the FIB cross-section to improve image quality and is not present in actual devices. e) Scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS/EDX) mapping of lamellae cross-section of the top Al contact (left) and the integrated elemental depth profiles obtained from these maps (right). Shown are an untreated anode pad, a pad after reactive ion etching (RIE) with CHF_3 plasma, and after RIE treatment and Al–F removal. The scaling of the integrated depth profiles is identical to the scaling of the EDS/EDX maps and is given by the scale bar in the left-most map.

optogenetics. Beyond this, our process for direct integration of ultrahigh-brightness OLEDs on CMOS chips with high-density arrays of aluminum contact electrodes and microscopic dimensions can be translated to a wide range of other areas requiring pixelated and bright light sources, including other forms of bioimplants, HMDs for AR/VR, and wearable devices.

2. Results

Figure 1a and 1b show the geometry of the CMOS chips used in this work. The rectangular CMOS die received from the foundry is patterned into a shank structure of four needles and subsequently wire bonded to a printed circuit board (PCB, Figure 1a) that connects via a flat ribbon cable to an external driver, using state-of-the-art methods in silicon post-processing and electronics packaging (see Experimental Section and Section S5, Supporting Information). The driver board controls the chip using a field programmable gate array (FPGA) that stores the OLED patterns and runs a programmable state machine. Each of the four needles of the device features two rows of 128 aluminum anode pads with a size and pitch of $19 \times 21\ \mu m^2$ and 24.5 µm, respectively, i.e., a total of 1024 anode pads. The emissive area of each OLED pixel

will be defined by the size and shape of these anode pads. Each needle also contains three larger cathode pads at the top, center and end of each needle as shown in Figure 1b. These pads will be connected to a thin semitransparent metal top-electrode that is deposited on top of the OLED stack and that covers all pixels.

2.1. Aluminum Contact Investigation and Cleaning Procedure

To optimize OLED brightness and yield on the CMOS chips, we first characterized the morphology and chemical composition of the contact pads. Figure 1c shows a scanning electron microscopy (SEM) image of three aluminum anode pads as received from the foundry, indicating significant morphological inhomogeneity of the aluminum surface. Under higher magnification, a focused ion beam (FIB) cross-section through one of the pads reveals the presence of side walls as tall as 800 nm (Figure 1d). By comparison, the total thickness of the OLEDs to be deposited onto the chip is <400 nm, leading to concerns about the formation of electrical shorts at the edges of each pixel.

Apart from these morphological challenges, the electronic properties of the contact pad are crucial to form ohmic contacts and ensure efficient charge injection for OLEDs deposited onto these pads. We thus investigated the chemical composition of the aluminum, which is expected to be covered by at least a few nanometers of native aluminum oxide. We examined the cross-section of the aluminum pad via scanning transmission electron microscopy (STEM) and analyzed the chemical composition of the pad near its surface via energy-dispersive X-ray spectroscopy (EDS/EDX, Figure 1e). This revealed a 15 nm-thick layer on top of the aluminum contact that contains aluminum, silicon, oxygen, and nitrogen, indicating the presence of both aluminum oxide and Si–O–N composites. While a thin native aluminum oxide layer might still allow for the formation of an electrical contact, this large thickness and unexpected elemental composition of the surface layer will most likely prevent effective charge injection and in turn drastically reduce the performance of OLEDs deposited on top. We chose reactive ion etching (RIE) with CHF_3 to remove the insulating layer from the aluminum contact. After the RIE treatment, the surface layer thickness was reduced to 5.4 nm, and in the EDS/EDX profile, the silicon peak was eliminated, and the oxygen peak was significantly reduced. However, a new fluorine peak emerged across the surface layer, indicating that a new composite layer, likely AlF_3, which is also an insulator, formed on the surface by a chemical reaction between CHF_3 and aluminum. After dissolving this layer by rinsing in heated deionized water (80 °C), the EDS/EDX depth profile shows that most fluorine is substituted with oxygen throughout the composite layer. The thickness of the composite layer, estimated by the full width of the layer at which oxygen is detected, is 4.4 nm (see Figure S1, Supporting Information for more details on the thickness determination).

2.2. OLED Brightness Optimization Through RIE and Al–F Removal

We chose a p–i–n top-emission OLED stack with a fluorescent blue or a phosphorescent orange emitter (**Figure 2**a) for the integration on CMOS backplanes since the doped charge-transport layers enable high brightness at the limited voltages available from the CMOS backplane (up to 7 V in our case). We further chose to use a thin semitransparent silver top-electrode to achieve a low sheet resistance (<10 Ω sq^{-1}).[30,31] While on its own, this silver electrode has lower optical transmission than a transparent conductive oxide cathode, tuning the thickness of the microcavity formed between the bottom and top metal contacts can fully compensate for the effect of the lower optical transmission and yield efficient, narrowband and directed emission.[28] The OLEDs were initially optimized for maximum brightness by fabricating 4 × 4 mm^2-sized reference pixels on a display-grade glass substrate. By thermally evaporating aluminum anodes, coating them with 15 nm of Al_2O_3 via atomic layer deposition to mimic the oxide layer thickness on the CMOS backplane, and then subjecting them to the different steps of the protocol described above, we emulated the situation encountered with the silicon chips but for a macroscopic device that can be more readily and accurately characterized, including a correction of efficiency measurements for the angle-resolved emission characteristics of the OLED.[32]

Figure 2b summarizes the current density–voltage–luminance (*J*–*V*–*L*) characteristics of reference OLEDs deposited on aluminum anode contacts exposed to different treatments. On an aluminum contact coated with 15 nm of Al_2O_3, blue-emitting OLEDs show very low current densities and no emission. Adding an RIE treatment with the CHF_3 plasma increases current density and leads to some, yet relatively dim emission (luminance of 100 cd m^{-2} at 5 V), in line with the presence of a thin and insulating Al–F layer. Adding the rinsing step and thus removing the Al–F improves the devices further, current densities are increased and a luminance of 1000 cd m^{-2} is reached at 5 V with the prevailing ≈4.4 nm-thick aluminum oxide layer. Using the same cleaning recipe and in addition incorporating an ultrathin interfacial silver layer (3 nm nominal thickness) on the aluminum pad facilitates tunneling of charges, presumably due to interdiffusion of the silver into the aluminum oxide, and thus allows current densities as high as 1000 mA cm^{-2} and a luminance of 17 500 cd m^{-2} at 5 V for the fluorescent blue-emitting OLED stack. The orange-emitting OLED stack reaches a maximum luminance of 45 900 cd m^{-2} at 5 V on aluminum pads prepared in the same optimized manner. For simplicity the silver interlayer was evaporated through the same mask as the OLED stack; its thickness was limited to 3 nm to avoid electrical shorting between neighboring pixels.

As a photometric quantity, luminance is weighted with the sensitivity of the human eye that is not relevant for some of the emerging applications discussed above, e.g., ChRs in light-sensitive neurons show a light sensitivity spectrum that is distinct from the spectral sensitivity of the human eye. For such applications, the angle-integrated optical power density emitted by a light source is a more general measure of brightness. The optical power densities reached by the optimized fluorescent blue and phosphorescent orange OLEDs on the glass substrates are comparable, with 0.46 mW mm^{-2} and 0.26 mW mm^{-2} at 5 V, respectively (Figure 2c), but the orange device achieves a higher external quantum efficiency (Figure S2a, Supporting Information). All data for OLEDs deposited on glass substrates are corrected for their angle-resolved emission characteristics, Figure S2b (Supporting Information). The emission spectra of the blue and

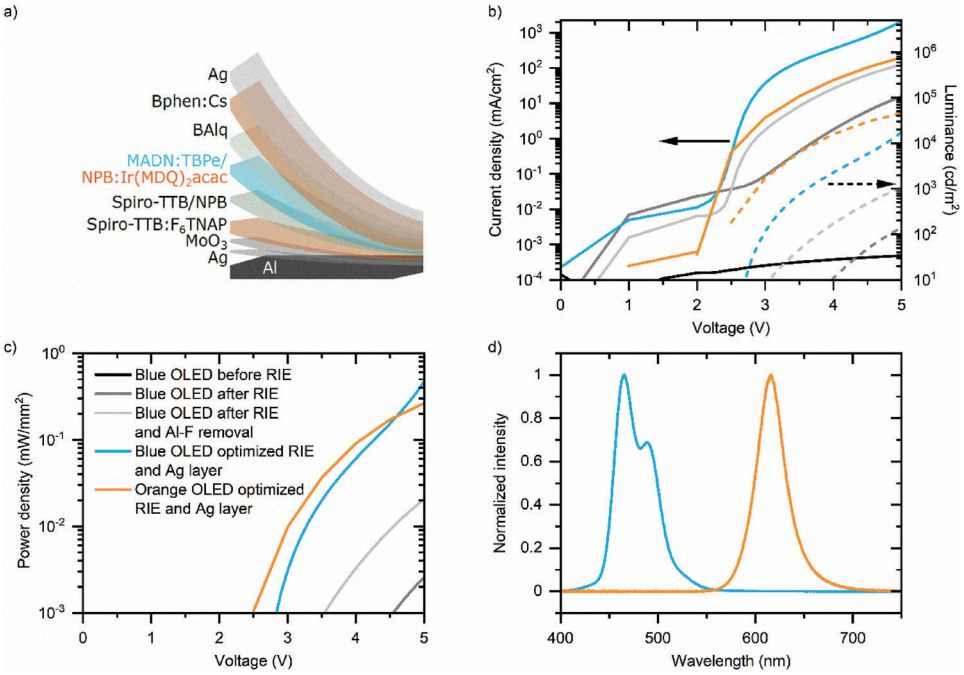

Figure 2. a) Fluorescent blue and phosphorescent orange top-emission OLED stack architectures used for all OLEDs in this work. b) *J–V–L* characteristics of blue reference OLEDs for different anode conditions; with a 15 nm-thick layer of Al_2O_3 (black), RIE cleaned (dark gray), RIE cleaned, and Al–F removed (light gray), RIE cleaned, and Al–F removed with an additional Ag interlayer (blue). Also shown is the orange reference OLED with the optimized RIE/Al–F removal treatment and Ag interlayer (orange). c) Optical power densities plotted against applied voltage for the same devices. d) Electroluminescence spectra of the optimized blue and orange OLEDs.

orange OLED (Figure 2d) exhibit maxima at 465 and 615 nm, respectively.

2.3. OLED Integration on Prototype Dies—Brightness and Yield

To test the compatibility of the foundry-produced aluminum contact pads with the deposition of OLEDs, prototype dies were produced that feature a series of anode pads of different sizes. Specifically, the prototype dies have two 425 × 425 μm² pixels, two rows with intermediate-size pixels (50 × 50 μm²), and two rows with 40 pixels measuring 19 × 21 μm² each, i.e. with the same dimensions and pitch as the pixels on the final shank-shaped CMOS chip (**Figure 3**a; Figure S3, Supporting Information). These prototype wafers are fabricated in the same foundry and utilize identical metal deposition and passivation etchback processes as the CMOS wafers but lack their active transistor implants. Instead, groups of OLED anode pads are hard-wired to large contact pads at the edge of the prototype die. This arrangement allows to operate OLEDs deposited on the die by using microprobes and without a need for additional packaging or wire bonding, which dramatically increases throughput during further testing and optimization of OLED brightness and yield.

The prototype die was subjected to the RIE/rinse protocol described above, and the blue- and orange-OLED stacks shown in Figure 2a, including the thin silver interlayer and the semitransparent silver top contact, were deposited onto the pixels on the prototype die using one shadow mask. The cathode pads were then connected with a 100 nm-thick silver layer deposited onto the cathode pads and onto the edge of the semitransparent top contact of the OLED using a second, complimentary shadow mask as shown in Figure S5d (Supporting Information). The areas across which the OLED stack and the thick silver layers were deposited are visible as deposition shadows in Figure 3a. Like for the final CMOS chip, OLED deposition does not require microstructuring of the OLED stack on the single pixel level as the emitting area is defined by the position and size of the anode pads. To render the devices stable under ambient conditions, we applied our recently developed chemical vapor deposition (CVD) based passivation process prior to any testing of the devices.[33]

We first investigated the 425 × 425 μm²-sized pixels, using microprobes to make electrical contact. The microscopy dark-field image of an operating orange-emitting pixel in Figure 3b gives an indication of the achievable emission homogeneity; the underlying chip structure is clearly visible, emphasizing the need to optimize contact morphology in the future. Figure 3c shows the current density and optical power density reached by the pixel at different applied voltages. At 5 V, the power density of the orange OLED on the prototype die is 0.074 mW mm^{-2}, which compares to a power density of 0.26 mW mm^{-2} for the reference device with aluminum deposited on the display-grade glass substrate. This reduction in brightness is most likely due to larger electronic and morphological inhomogeneity and residual contact resistance of the anode pads produced at the foundry. At 7 V, the maximum voltage available from our final CMOS chips, the emitted power density is 0.27 mW mm^{-2}; at 10 V, it reaches 0.77 mW mm^{-2}, illustrating the value of increasing the voltage in future CMOS designs.

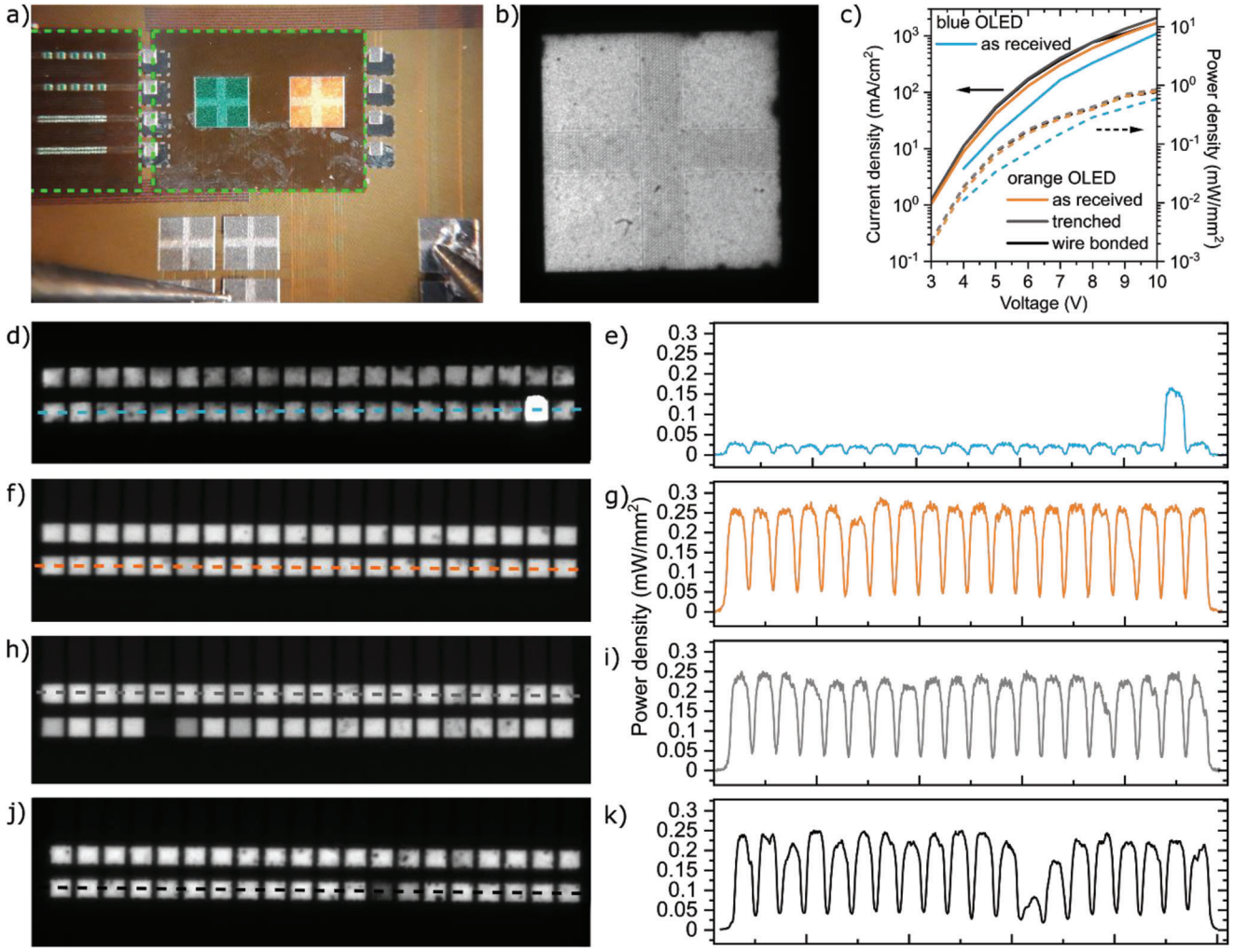

Figure 3. a) Bright-field microscopy image of the prototype die with microprobes contacting the pads for the 425 × 425 μm^2 sized orange-OLED pixel. The deposition shadow of the OLED shadow mask is outlined by green dashed lines. The cathode interconnect layer that covers the cathode pads and overlaps with the semitransparent top silver electrode is marked by the gray dotted lines. b) Dark-field microscopy image of an active, orange-emitting, 425 × 425 μm^2-sized pixel. c) Current density and optical power density of the large pixel on prototype wafer dies for different driving voltages. d–k) Dark-field microscopy images of groups of 19 × 21 μm^2-sized OLED pixels at an applied voltage of 7 V for different wafer processing steps (left) and power density profiles along a line of pixels as indicated in the respective dark-field images (right). d,e) Unprocessed die with blue OLED stack. f,g) Unprocessed die with orange-OLED stack. h,i) Die exposed to trenching protocol with orange-OLED stack. j,k) Die exposed to wire bonding protocol with orange-OLED stack. All dies were cleaned with the standard RIE/rinse removal protocol.

The performance of blue-emitting OLEDs deposited on the prototype dies was slightly lower than for the orange-OLED stack. An optical power density of 0.035 and 0.15 mW mm^{-2} was achieved at 5 and 7 V, respectively. The maximum power density at 10 V was 0.59 mW mm^{-2}. The blue devices also show a higher turn-on voltage, in line with their higher photon energy. If the contact resistance between the aluminum anode pads on the die and the OLED stack is still an issue, it is more likely to show up for blue devices that require higher current densities. This presumably causes the larger gap in power density between reference OLEDs (0.46 mW mm^{-2} at 5 V) and the OLED on the prototype wafer dies (0.035 mW mm^{-2} at 5 V). Several variations to the RIE cleaning protocol were tested to improve the performance of the blue OLEDs (Figure S4, Supporting Information), but without significant further improvements.

To obtain the final shank-shaped device, CMOS wafer dies are trenched, which involves depositing a pad protection layer by spin coating and dissolving this layer again after the trenching step. Furthermore, the wire bonding step is performed at elevated temperatures of up to 100 °C for several minutes, and epoxy glue is applied to the wire bonding pads and cured with UV light after wire bonding (see Experimental Section and Figure S5, Supporting Information). Residues left over from trenching and the heat and light exposure during wire bonding might alter the properties of the anode pads and therefore affect the performance of OLEDs fabricated on top of these contacts. Thus, these processes are tested with the prototype wafer dies. The power density emitted by the large pixels on the prototype die was therefore analyzed for dies processed to a different extent and compared to the performance of an orange-OLED pixel on the reference prototype

die. This experiment showed that the power density was comparable for all dies, irrespective of their process history (Figure 3c), indicating that our RIE/rinse cleaning process can remove any residues and modifications to the anode pads introduced during trenching and wire bonding.

Apart from the achievable device brightness, the pixel yield is another key requirement for high-density devices. The yield and brightness of the 40 individual 19 × 21 μm^2-sized pixels on the prototype dies were therefore investigated for the different processing steps, i.e., RIE/rinse cleaned but otherwise as received from the foundry (unprocessed), after trenching and after wire bonding.

For blue OLEDs, on the prototype die as received from the foundry, a 100% pixel yield was obtained (Figure 3d). The emissive area shows a few darker spots, probably due to inhomogeneous morphology or electronic properties of the anode pads. A profile of the optical power density across one line of pixels shows 0.03 mW mm^{-2} at 7 V for 39 of the 40 pixels, and a power density of 0.16 mW mm^{-2} for the one remaining single pixel (Figure 3e). While encouraging overall, these observations confirm earlier concerns about the blue-OLED stack being particularly prone to contact resistance at the anode pads surface.

The orange OLEDs deposited on the prototype die that was used as received from the foundry show 100% yield (Figure 3f) and in contrast to the blue devices feature homogenous emission and power density across the pixel area and across different pixels (Figure 3g). The average power density of 40 individual 19 × 21 μm^2-sized OLEDs is 0.25 mW mm^{-2} at 7 V, similar to the power density of the 425 × 425 μm^2 pixel, and significantly higher than for the blue devices. On the prototype die exposed to the trenching process, the yield of the orange OLEDs reduces slightly, with 1 of the 40 pixels not showing emission (i.e., a nominal yield of 97.5%, Figure 3h). The average brightness also reduces marginally to 0.23 mW mm^{-2} at 7 V (Figure 3i). The emission uniformity is similar to OLEDs on as received prototype dies. The yield of orange OLEDs on wire bonded dies is nominally 100%, but the emission uniformity is reduced, and the emissive area of the pixels shows some dark spots (Figure 3j). One pixel shows a markedly reduced brightness (<0.1 mW mm^{-2}), but the average power density for the rest of the pixels remains comparable to the value obtained for the die used as received from the foundry (Figure 3k).

2.4. OLED Integration on Fully Packaged Shank-Shaped Devices

The results obtained with the prototype dies demonstrate the feasibility of integrating OLEDs on trenched and wire bonded silicon chips while reaching brightness levels compatible with the requirements for use in ultrahigh brightness applications. Thus, we take the OLED integration further and next fabricate the blue- and orange-OLED stacks on the fully packaged shank-shaped CMOS-based devices introduced in Figure 1a,b. The CMOS backplane and driver setup allows to drive and individually switch OLEDs and delivers a voltage of up to 7 V to each anode pad in a programmable fashion. To determine the pixel yield of our OLED deposition, all pixels were switched on at the same time.

Blue OLEDs deposited on the CMOS backplane showed a yield of 91.5%, with 937 of 1024 pixels lighting up across the four needles of the shank (**Figure 4**a). As already observed for the prototype dies, the overall brightness of most OLED pixels is below 0.05 mW mm^{-2} at 7 V (76%, Figure S7, Supporting Information). The mean brightness is 0.07 mW mm^{-2} (corresponding to a luminance of 2 500 cd m^{-2}); however, a few pixels achieve power densities of up to 0.4 mW mm^2, which corresponds to a promising peak luminance of ≈15 000 cd m^{-2}.

Figure 4b shows a microscopy image of a shank-shaped CMOS chip with orange OLEDs and with two needles, i.e., a total of 512 pixels; all pixels are operated simultaneously. The power density is very homogenous across most pixels on the chip. The thick cathode top-contact layer blocks emission from the first four OLED pads on each sub-shank (Figure S8b, Supporting Information). Out of the remaining 496 available OLED pads, a total of 480 show emission, which corresponds to a yield of 97%. A histogram of the power density reached by each pixel reveals a median power density across the whole device of 0.25 mW mm^{-2} (corresponding to a luminance of 43 300 cd m^{-2}) at 7 V, with 70% of the pixels reaching more than half of the median brightness (i.e., >0.125 mW mm^{-2}, Figure 4c). The maximum power density generated by orange OLEDs on this shank-shaped device is 0.33 mW mm^{-2}.

Next, we tested that the OLEDs on the CMOS devices can be switched individually. Figure 4d shows a sequence of microscopy images of a device displaying a pixel pattern with a line of OLEDs moving along and across the two needles of the device. Further stimulation patterns and the ability to dynamically reprogram the patterns in real-time are shown in Videos S1–S4 (Supporting Information).

3. Conclusion

We have demonstrated the direct integration of blue and orange OLEDs on a miniaturized CMOS backplane with a complex, shank-shaped geometry. The devices contain 1024 individually addressable OLED pixels, each 19 × 21 μm^2 in size and spread out over a length of 3.33 mm along the 6 mm-long needles. Our devices thus reach the highest density of light sources reported for any shank-shaped emissive device so far. The OLED integration required optimization of the aluminum anode contact pads on the CMOS backplane. After analyzing the chemical composition of the surface layer on these pads, a plasma cleaning process was developed that leaves the contacts with an aluminum oxide layer of 4.4 nm thickness. Combining this plasma process with the deposition of an ultrathin silver interlayer led to a dramatic reduction in contact resistance due to interdiffusion of the silver into the insulating aluminum oxide layer. By further using a top-emitting p–i–n OLED architecture with doped charge-transport layers, we obtained efficient and bright devices operating at low driving voltages. The final implantable device with orange phosphorescent top-emitting OLEDs showed a pixel yield of 97% and the median of the brightness distribution was 0.25 mW mm^{-2} at a peak emission wavelength of 615 nm. To the best of our knowledge, the corresponding median luminance of 43 300 cd m^{-2} is the highest value ever reported for OLEDs on a CMOS backplane.

The size and density of the devices paired with the achieved brightness and yield sets the base for applications requiring ultrahigh-brightness and high-resolution light sources. A particularly relevant example is in optogenetics, where the

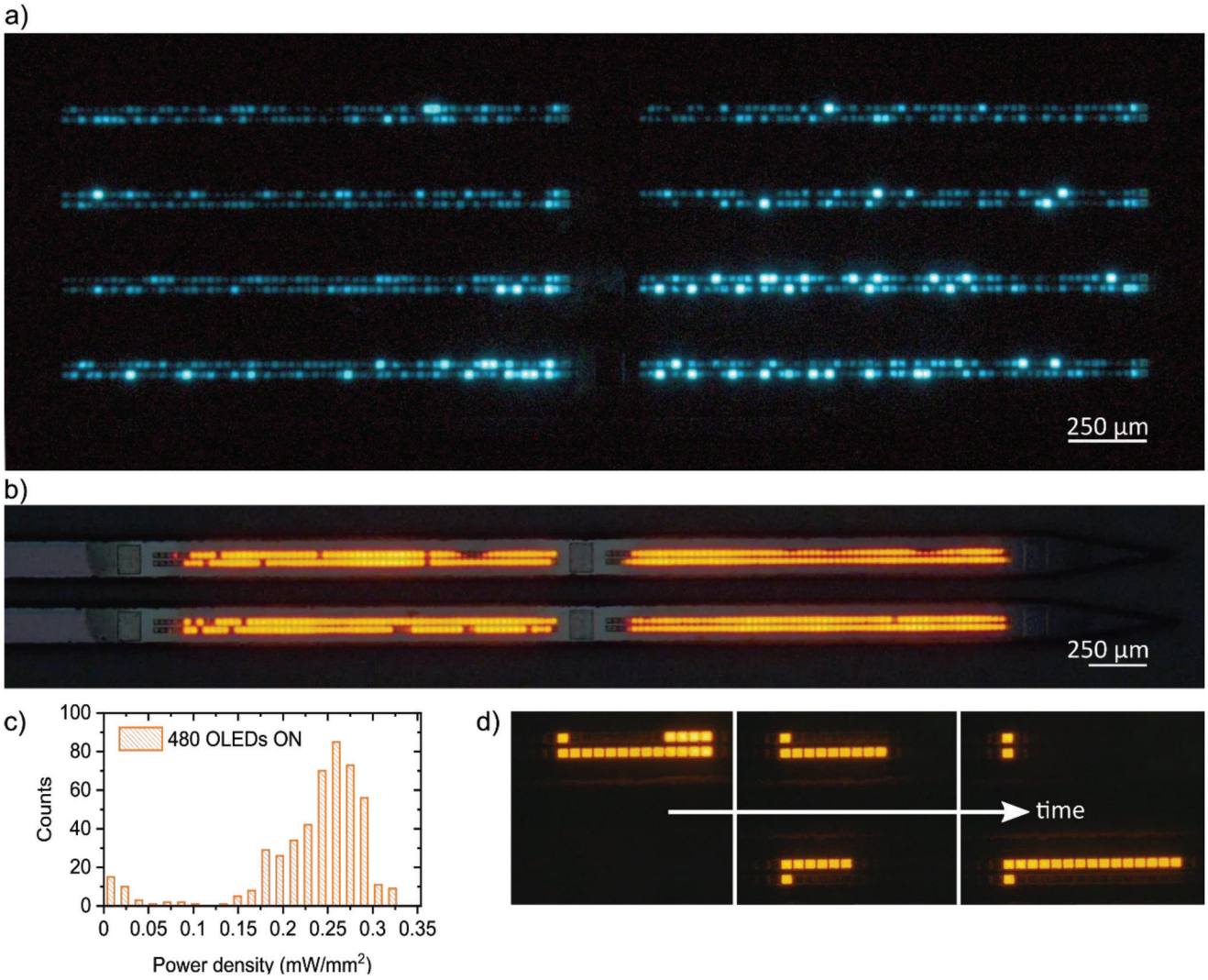

Figure 4. a) Dark-field microscopy image of blue-emitting device with all OLEDs switched on. b) Dark-field microscopy image of orange-emitting device with two needles and all OLEDs switched on. c) Histogram of optical power density generated by different pixels on the orange-emitting device in (b), see experimental details for more information. d) Sequence of the temporal evolution of a stimulation pattern displayed by the orange-emitting device (b) with a line of OLEDs moved along and across the two needles.

shank-shaped geometry of our devices provides a unique and unprecedented platform for deep brain photostimulation, offering a route to single-OLED–single-cell stimulation while at the same time allowing excitation of thousands of neurons in parallel. The brightness of the OLEDs is well above the threshold for stimulation of genetically modified neurons, especially when considering the latest generation ChRs like CheRiff and ChRmine.[34,35] Additionally, the CMOS backplane allows for a variety of stimulation patterns in constant or pulsed operation, with varying duty cycles, thus optimizing stimulation efficiency. In the future, the CMOS backplane could also serve to detect neuronal activity by sensing changes in electrical potential. By modifying and refining the shadow masks used during OLED deposition, it would also be possible to realize dual color OLED arrays, which might allow for simultaneous excitation of two different light-sensitive ion channels, including for simultaneous stimulation and inhibition of neuronal activity in neighboring cells.[36,37]

The luminance provided by our devices exceeds the values reached by current state-of-the-art monocolored OLED microdisplays. At a luminance of over 40 000 cd m^{-2}, the orange devices are of particular interest for AR applications in bright daylight, including in aviation. In future devices, the brightness and homogeneity, especially of the blue OLEDs, needs to be improved further, which can be achieved for example by switching from constant voltage to constant current driver logic. Developing backplanes providing higher driving voltages/currents can further increase the total brightness. In addition, higher voltage would allow for the use of tandem OLEDs stacks, which reduces the stress on each sub-stack, thus allowing for a further increase in brightness.[28]

In our present work, the described method of contact modification followed by deposition of OLEDs was demonstrated on the die level and on the level of wire bonded and packaged devices. However, in the future, it could be

scaled to the whole wafer level, thus dramatically increasing throughput.

4. Experimental Section

Fabrication, Postprocessing and Driving for Prototype and CMOS Dies: Both the prototype dies, and CMOS devices were produced in a 130 nm process node (TSMC, Taiwan). Prototype and CMOS dies with sizes of 8 × 3.1 mm^2 were obtained by dicing full wafers. For fabrication of CMOS devices with a shank layout, the CMOS dies as received from the foundry were trenched by first bonding 20–30 dies with adhesive (Crystalbond 555) to a carrier wafer. A protective film (ProtectLED) was spun onto the wafer to protect the contact pads from trenching debris. The shank outlines are then defined by thermally ablating 100 µm-deep and 25 µm-wide trenches with a Cu-vapor micromachining laser (IPG Photonics, Oxford, MA, USA). After trenching, the probes were sonicated in acetone and isopropanol to remove the protective film and clean away any debris. In the subsequent thinning process, dies were glued upside-down onto a glass slide with superglue. Using a mechanical polisher (X-PREP, Allied High Tech, Compton, CA, USA), dies were thinned to a thickness of 55 µm, thus releasing the shank-shaped device from the die. The devices were subsequently cleaned with acetone and isopropanol before wire bonding. The shank-shaped devices were aligned to the PCB ground pad and the p-doped Si substrate for the CMOS device was connected using conductive silver epoxy (100 °C for 20 min). Once cured, the chips were rinsed with acetone and isopropanol and then wire bonded to the PCB at 100 °C. The probes were tested for shorts; the bonds were covered and secured with UV-curable epoxy.

The daughterboard PCB was connected through a flexible cable to a motherboard, carrying voltage regulators and an FPGA responsible for transferring the arbitrarily programmable patterns into the CMOS in-pixel 1-bit enable memory. The FPGA contains a state machine that controls the OLED patterning and clocking. A global OLED shutter activates all OLEDs that were set to enable in the in-pixel memory. The CMOS circuitry was implemented underneath each anode pad, and includes local addressing, level shifting and decoupling capacitance (see Figure S6, Supporting Information).

FIB/STEM/SEM: Cross-sections for scanning transmission electron microscopy (STEM) were prepared using FEI Scios DualBeam instrument using a Ga-ion source with milling performed at an acceleration voltage of 30 kV, followed by final polishing at 5 kV. STEM measurements were performed on FEI Titan Themis operated at 200 kV and equipped with a SuperX energydispersive X-ray spectrometer and a CEOS DCOR probe corrector. Data were acquired with a probe convergence angle 21.2 mrad with high-angle annular dark-field (HAADF) inner and outer collection angles of 56.3 and 200 mrad, respectively.

OLED Fabrication and Substrate Preparation: The OLED deposition was performed in a high-vacuum chamber (Angstrom, Canada) via thermal evaporation from temperature-controlled crucibles at a base pressure ≈10^{-7} mbar. Deposition rates and thicknesses were monitored by quartz crystal balances.

The reference OLEDs with an emissive area of 4 × 4 mm^2 were fabricated on display-grade glass substrates with a thickness of 1.1 mm (Eagle XG, Howard Glass), which were cleaned in an ultrasonic bath with acetone and isopropanol (10 min each). The substrates were dried with nitrogen and subjected to oxygen plasma treatment (3 min). The mask change required during deposition to obtain the anode, organics and cathode patterns was performed automatically without opening the vacuum-chamber.

For prototype dies and CMOS devices, the aluminum anode contacts were pre-conditioned via a reactive ion etch (RIE) plasma process. The RIE treatment (SI 500, Sentech Instruments GmbH) was performed at 20 sccm CHF_3 flow with 100 W RF and 100 W ICP. The etch rate for aluminum oxide at these parameters was 0.9 Å s^{-1}. After etching for 200 s, the dies were immersed in 80 °C DI water for 60 s to wash away the topmost Al–F formed during the RIE step.[38] After drying with nitrogen, they were mounted in a custom-made sample holder with precision alignment pins to guide accurate alignment between the contact pads on the wafer dies and each of the shadow masks used during deposition. The alignment of each mask was checked and if needed adjusted under a microscope inside a nitrogen inert gas glovebox. The OLED stack and the 20 nm-thick silver cathode layers were then deposited on the CMOS devices. Afterwards, the devices were transferred into the nitrogen glovebox without air exposure to exchange the deposition shadow mask for another shadow mask with cut-outs for depositing the interconnects from the cathode layer on the OLED stack to the large cathode pads on the chip. Once this mask was positioned accurately, the devices were placed back into the deposition chamber for the final deposition step of a 100 nm-thick silver interconnect layer (see Figure S5d, Supporting Information).

The organic materials used in the OLEDs were 2,2′,7,7′-tetra(*N*,*N*-di-p-tolyl)amino-9,9-spirobifluorene (Spiro-TTB), 2,2′-(perfluoronaphthalene-2,6-diylidene)dimalononitrile (F_6TNAP), *N*,*N*′-bis(naphthalen-1-yl)-*N*,*N*′-bis(phenyl)-benzidine (NPB), bis(2-methyldibenzo-[f,h]quinoxaline)(acetylacetonate)iridium(III) ($Ir(MDQ)_2acac$), 2-methyl-9,10-bis(naphthalen-2-yl)anthracene (MADN), 2,5,8,11-tetra-tert-butylperylene (TBPe), bis(2-methyl-8-quinolinolate)-4-(phenylphenolato)-aluminium (BAlq), and 4,7-diphenyl-1,10-phenanthroline (BPhen). They were purchased from Lumtec (Taipei, Taiwan) and used without further purification.

The OLED stack on the CMOS backplane consists of a 3 nm-thick silver layer, a 1 nm-thick MoO_3 layer, a p-doped hole-transport layer (HTL) of Spiro-TTB:F_6TNAP (4 wt%, 190 nm for orange-emitting OLEDs, 150 nm for blue-emitting OLEDs), an electron-blocking layer (EBL) of NPB (10 nm, for orange) or Spiro-TTB (10 nm, for blue), an emission layer (EML) of NPB doped with the phosphorescent orange emitter $Ir(MDQ)_2acac$ (10 wt%, 40 nm) or MADN doped with the fluorescent blue emitter TBPe (1.5 wt%, 20 nm), a hole-blocking layer (HBL) of BAlq (10 nm), an electron-transport layer (ETL) of Cs-doped BPhen (4 wt%, 60 nm), and a semitransparent silver top cathode (20 nm). The total thickness of the OLED microcavity was tuned to the second optical maximum using optical modelling to achieve efficient operation, forward-directed emission, and robustness to substrate roughness. Modelling was performed using a transfer matrix model.[39]

After the OLED and interconnect deposition was completed, all devices were again transferred from the vacuum chamber to the nitrogen glovebox without intermittent exposure to air and then encapsulated/passivated by a combination of atomic layer deposition (ALD) of nanolaminates and parylene-C (diX C, KISCO) as described by Keum et al.[33] In brief, the layer sequence of the encapsulation was 50±5 nm nanolaminate, 5 ± 1 µm parylene-C, 50 ± 5 nm nanolaminate, and 5 ± 1 µm parylene-C leading to a total thickness of 75 µm for the final the shank-shaped CMOS device since the encapsulation was deposited on all surfaces. The nanolaminates and the parylene-C were deposited using an ALD reactor (Savannah S200, Veeco) and a parylene coater (P8, Diener), respectively, with both coaters directly connected to the nitrogen-filled glovebox. For the nanolaminate, an alternating series of 3 nm-thick sublayers of Al_2O_3 and ZrO_2 was deposited using 33 cycles of a 15 ms trimethylaluminum (TMA) pulse/10 s N_2 purge/15 ms H_2O pulse/10 s N_2 purge and 17 cycles of a 300 ms tetrakis(dimethylamino)zirconium (TDMAZr) pulse/7 s N_2 purge/30 ms H_2O pulse/7 s N_2 purge. The TDMAZr precursor was heated to 75 °C; the TMA and H_2O cylinders were maintained at room temperature. The process temperature and base pressure of the ALD reactor were 80 °C and 0.1 Torr, respectively. The parylene-C powder was vaporized at 130–140 °C and the gaseous dimer was pyrolyzed into a monomer at 690 °C. The polymeric films of parylene-C were then formed on the devices in the main vacuum chamber of the parylene coating system which was kept at room temperature and at a base pressure of <25 mTorr.

OLED Characterization: The characterization of the reference OLEDs was performed as described by Archer et al.,[32] measuring the angular emission characteristics with a goniometer and including any deviations from ideal Lambertian characteristics when computing optical power density and EQE.

The emission power of OLEDs deposited on the prototype dies and CMOS devices were characterized using a stereo microscope (Nikon Instruments Europe, SMZ25). The reference OLEDs with known optical power density were measured with a 12-bit CCD camera mounted on the

microscope (DL-604M-OEM, Andor), and the magnification and integration time were then kept constant for measuring OLEDs on the CMOS backplanes. This allowed to convert the counts recorded by the camera into absolute optical power density values. The yield and brightness of individual pixels were determined by a line scan across the image.

Full-color microscopy images of the devices were taken with an upright inspection microscope (Axiolab5, Zeiss) with a CMOS camera (Axiocam 208, Zeiss).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under Contract N6600117C4012, by the National Institutes of Health under Grant U01NS090596, and by the Leverhulme Trust (RPG-2017-231). This work was performed in part at the Columbia Nano Initiative. C.K.M. acknowledges funding from the European Commission through a Marie Skłodowska Curie individual fellowship (101029807). M.C.G. acknowledges funding from Alexander von Humboldt Stiftung (Humboldt-Professorship). The authors thank Aaron Naden for the FIB/STEM measurements (Engineering and Physical Sciences Research Council under grant numbers EP/L017008/1, EP/R023751/1 and EP/T019298/1).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are openly available in University of St Andrews Repository at https://doi.org/10.17630/b082523d-7242-4edf-bd71-9eacf6adbd34.

Keywords

aluminum contacts, implants, organic light-emitting diodes, optogenetics, reactive ion etching, shanks

Received: January 18, 2023
Revised: May 24, 2023
Published online:

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