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Degradation Pattern of Parallel Symmetrical and Asymmetrical Double-Trench SiC MOSFETs under Repetitive Short Circuits

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Abstract

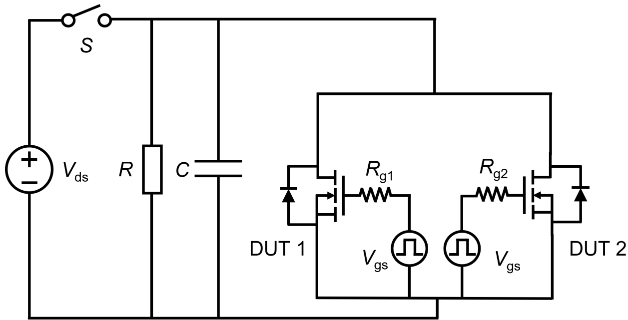
In practice, SiC MOSFET chips are often parallel-connected to promote the power rating. However, due to the potentially unequal circuit parameter and temperature distribution inside the power module, parallel devices suffer from different electrothermal stress, which may result in long-term reliability challenges. In this paper, the short circuit performance of parallel-connected Planar, Symmetrical and Asymmetrical Double-Trench SiC MOSFETs have been investigated. The impact of gate resistance and case temperature difference on current distribution of parallel SiC MOSFETs have been analyzed. The degradation pattern of key parameters of three types of devices have been studied.

1 Introduction

With advantages of wider bandgap, higher critical electric field and higher carrier mobility, Silicon Carbide (SiC) devices have faster switching speed, lower on-state resistance (R_{on}), higher breakdown field and smaller chip area compared with Silicon counterparts. These outstanding characteristics have brought significant improvements to the industry, greatly reducing the weight and cost of the power electronics system. However, the reliability of SiC devices has been a constraint, especially in extreme conditions such as short circuits [1]–[4].
Moreover, discrete SiC chip is unable to conduct high current, so SiC chips are often parallel connected to increase the power level. The uneven parameter distribution among chips will easily result in different current and temperature distribution among devices, and the inconsistent electrical-thermal stress will cause chip degradation to varying degrees, which will ultimately lower the overall reliability. In [5], the short circuit behavior of Wolfspeed 1.2 kV/300 A and Rohm 1.2 kV/180 A multi-chip SiC module were compared. Test results found out that the Cree module can only withstand 3.2 μs while the Rohm module can suffer from the stress for 7 μs at 800 V. In [6], a half-bridge module was tested and it failed within 3 μs. After post-failure investigation, both papers discovered that only some of the chips failed, and it was inferred that the unequal parameter distribution was the root cause: the least reliable device determined the overall reliability of the module. In [7]–[9], the disparity of chip parameter was discussed and electrical-thermal models were developed to explain the mechanism of short circuit current distribution. The spread of threshold voltage V_{th} was found to be the most responsible factor. In [10], the impact of parasitic inductance mismatches on short circuit reliability was clarified. Suggestions were given to the design of power module.
Current studies mainly focus on reliability testing of power modules, or finding responsible parameters for uneven current distribution. The evolution pattern of parallel-connected SiC MOSFETs under different electrical-thermal stress in the short circuit event should be further investigated, which is helpful to shed light on the device degradation mechanism and is crucial to the long-term reliability of SiC MOSFET devices. Thus, the short circuit reliability test rig for parallel SiC MOSFET devices is established in this paper. The short circuit current distribution and the degradation of key parameters of parallel-connected Planar, Symmetrical and Asymmetrical trench SiC MOSFETs are investigated in different electrical-thermal stress.

2 Experimental Setup

The short circuit schematic diagram and test board for parallel-connected SiC MOSFET devices are shown in Figure 1. The devices under test (DUTs) were Planar, Symmetrical, and Asymmetrical trench MOSFETs. Each DUT had a separate gate driver. Before the test, DUTs had been tested by source measuring unit (Keysight B2902A) to make sure they have similar static parameters, and the difference would only be caused by the external factors. The PCB board had been carefully designed to ensure that two DUTs have symmetrical current path and similar parasitic parameters. The synchronicity of the gate signal was tested, and both gate drivers can give same +18/-5 V output simultaneously. Besides, short circuit currents were measured by Rogowski coil (CWT1), and the drain-source voltage (V_{ds}) was measured by the differential probe (GW-Instek GDP-100). All waveforms were captured using the oscilloscope (Keysight MSO7104 A 1-GHz 4 GSa/s). The short circuit waveform and the static performance of parallel devices were characterized every 20 cycles.



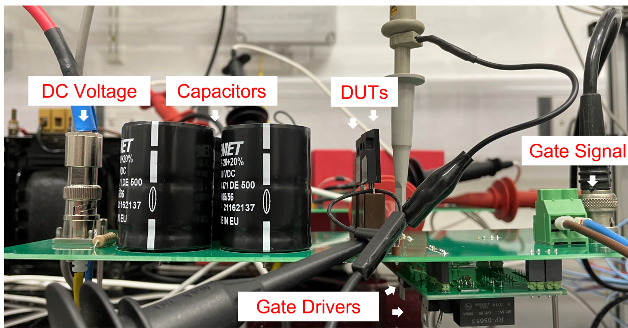


Fig. 1: Experimental set-up for short circuit test of parallel devices, including the two devices under test (DUTs) of the three SiC MOSFET structures, gate driver signal outputs, DC link capacitors and probes.

3 Effect of R_g mismatch

3.1 Test results and analysis

In the test, all parameters were kept same and only R_g was different. The test was carried out at 400 V V_{ds} and room temperature. The R_g of DUT 1 (Planar SiC MOSFET 1, Symmetrical trench SiC MOSFET 1, Asymmetrical trench SiC MOSFET 1) and DUT 2 (Planar SiC MOSFET 2, Symmetrical trench SiC MOSFET 2, Asymmetrical trench SiC MOSFET 2) was 11 Ω and 22 Ω, respectively. The short circuit duration (t_{sc}) was 10 μs, and test period was 10 s. Key static parameters of devices have been listed in Table 1. For all types of devices, the variations of V_{th} and on-state resistance (R_{on}) are both below 2%. In this way, the difference between devices can be ignored and the only variable was R_g.

	V_{th} (V)	R_{on} (mΩ)
Planar 1	3.34	145.11
Planar 2	3.34	144.42
Variance	0%	0.48%
Symmetrical Trench 1	4.42	133.96
Symmetrical Trench 2	4.44	133.30
Variance	0.45%	0.49%
Asymmetrical Trench 1	4.74	105.25
Asymmetrical Trench 2	4.74	103.68
Variance	0%	1.51%

Tab. 1: Key parameters of parallel devices under short circuit test with different R_g.

The short circuit current distribution of three types of devices after the first cycle are shown in Figure 2. It can be discovered that the devices with higher R_g has lower peak current, but the difference is negligible in the current dropping phase. The 11 Ω difference in R_g seems to have no impact on the short circuit current distribution between planar devices, which is because of its large input capacitance that reduces the switching speed. Compared with Symmetrical trench devices, Asymmetrical trench devices are more sensitive to R_g difference due to smaller input capacitance and faster switching speed.

3.2 Degradation of key parameters

3.2.1 Degradation of V_{th}

The degradation of V_{th} of three types parallel devices are shown in Figure 3. The Planar devices almost exhibit no degradation after 100

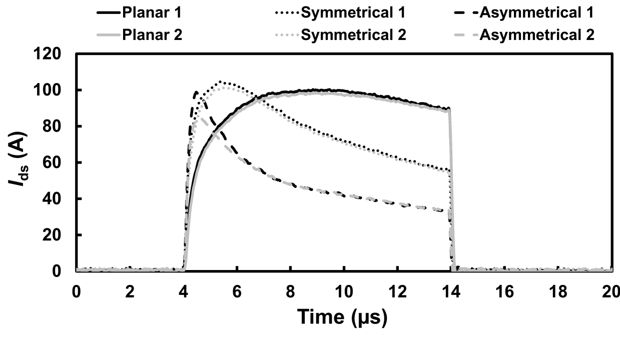


Fig. 2: Impact of R_g difference on short circuit current distribution.

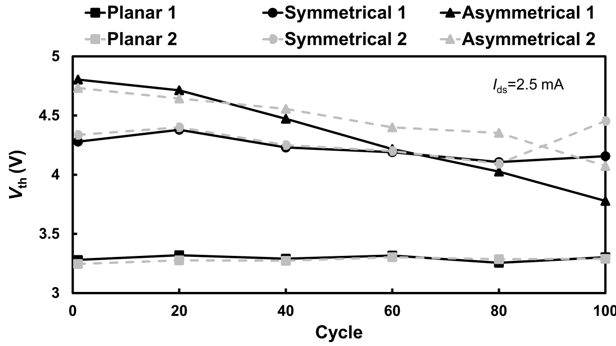


Fig. 3: Degradation of V_{th} under short circuit test with different R_g.

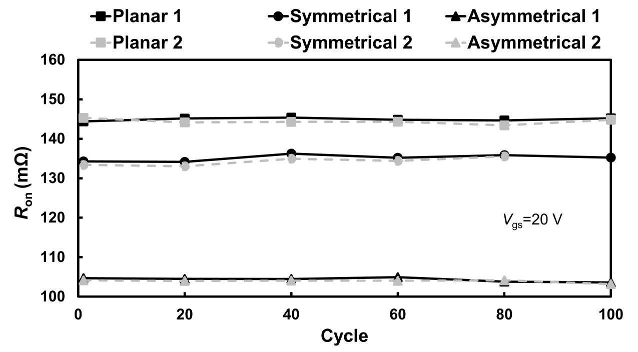


Fig. 4: Degradation of R_{on} under short circuit test with different R_g.

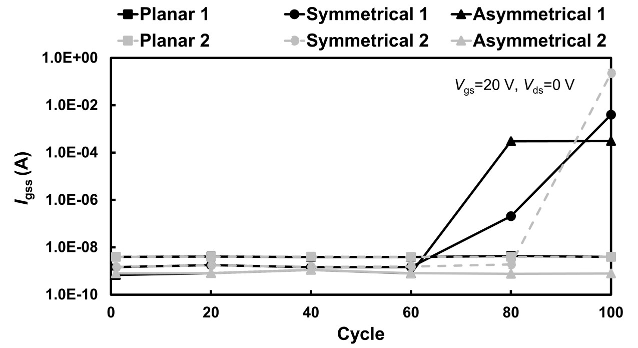


Fig. 5: Degradation of I_{gss} under short circuit test with different R_g.

cycles, and V_{th} remains stable around 3.2-3.3 V. For Symmetrical trench devices, V_{th} gradually reduces before 80 cycles with similar extent, which is the result of positive charge injection into the gate oxide under the negative turn-off V_{gs} stress [11], [12]. At the 100th cycle, V_{th} increases for both parallel-connected devices, indicating the degradation mode of the gate oxide has been different. With regard to Asymmetrical trench devices, V_{th} of both DUTs continuously reduces throughout the test, but the device with lower R_g degrades faster. This makes sense because according to Figure 2, the device with lower R_g has higher current, thereby having higher short circuit energy and higher junction temperature, which increases the possibility for holes to overcome the SiC/SiO_2 barrier and causes more significant V_{th} drift [13].

3.2.2 Degradation of R_{on}

The degradation of R_{on} of three types of parallel-connected devices are demonstrated in Figure 4. It can be discovered that R_{on} of Planar and Asymmetrical devices remains rather stable and almost shows no degradation, which indicates that the bond wires and the top Al layer of the chip are still in healthy state [14]. The degradation of V_{th} has minor impact on R_{on} measured at high V_{gs}. For Symmetrical trench device with higher R_g, R_{on} could not be measured at the last cycle anymore because its gate has been damaged and the test condition has gone beyond the limit of source measuring unit.

3.2.3 Degradation of I_{gss}

I_{gss} is a indicator of gate oxide healthiness. The I_{gss} degradation of DUTs are depicted in Figure 5. Based on the test results, the gate oxides for both Planar devices are healthy and show no indication of degradation after 100 cycles. For Symmetrical and Asymmetrical trench devices, I_{gss} degrades faster for devices with lower R_g. The reason behind is because the current switches faster and is larger when lower R_g is applied. With same V_{ds}, devices with lower R_g suffer from higher short circuit energy and their gate oxides undergo higher electrical-thermal-mechanical stress.

3.2.4 Degradation of E_{sc}

To analyze the degradation of chip parameters on short circuit performance of parallel-connected

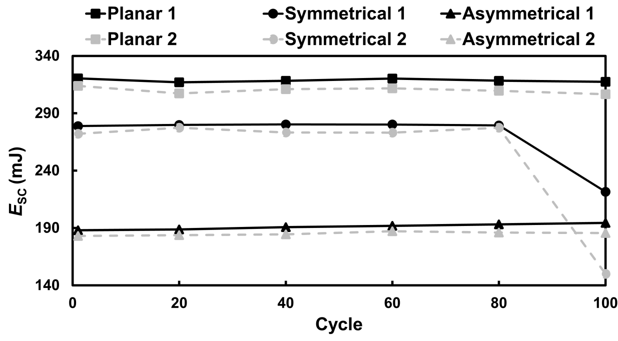


Fig. 6: Degradation of E_{sc} under short circuit test with different R_g.

	V_{th} (V)	R_{on} (mΩ)
Planar 3	3.30	142.87
Planar 4	3.26	144.60
Variance	1.23%	1.21%
Symmetrical Trench 3	4.56	142.96
Symmetrical Trench 4	4.55	139.47
Variance	0.21%	1.79%
Asymmetrical Trench 3	4.70	111.08
Asymmetrical Trench 4	4.74	111.04
Variance	0.85%	0.04%

Tab. 2: Key parameters of parallel devices under short circuit test with different temperature.

devices, short circuit energy (E_{sc}) has been calculated and plotted in Figure 6. It could be discovered that the devices with smaller R_g always have larger E_{sc} compared with the devices with larger R_g. For Planar devices, since no parameters degrade significantly, E_{sc} for both devices remains roughly unchanged. For Symmetrical trench devices, E_{sc} drops at the end of test cycle due to the large I_{gss}, which reduces the V_{gs} and short circuit current. As for Asymmetrical trench devices, E_{sc} slightly increases for both devices, and the device with lower R_g has greater increase. This is because the reduced V_{th} speeds up the turn-on of devices.

4 Effect of T_{case} mismatch

4.1 Test results and analysis

To investigate the effect of case temperature (T_{case}) mismatch on current distribution, DUT 3 (Planar SiC MOSFET 3, Symmetrical trench SiC MOSFET 3, Asymmetrical trench SiC MOSFET 3) was kept at 25 °C, and DUT 4 (Planar SiC MOSFET 4, Symmetrical trench SiC MOSFET 4, Asymmetrical trench SiC MOSFET 4) was attached to a heating block to heat up the device to 125 °C. The test was carried out at V_{ds} of 400 V & R_g of 22 Ω. The t_{sc} and test period were 10 μs and 10 s, respectively. Key static parameters of devices have been listed in Table 2. Similarly, the variations of V_{th} and R_{on} for all types of devices are both below 2%. The only variable in the test is T_{case}.

According to the results in Figure 7, it could be discovered that the higher the temperature, the faster the devices switch, but the lower peak current will be. The underlying reason is due to the negative temperature coefficient of V_{th} and carrier mobility. With higher temperature, V_{th} and lower mobility are

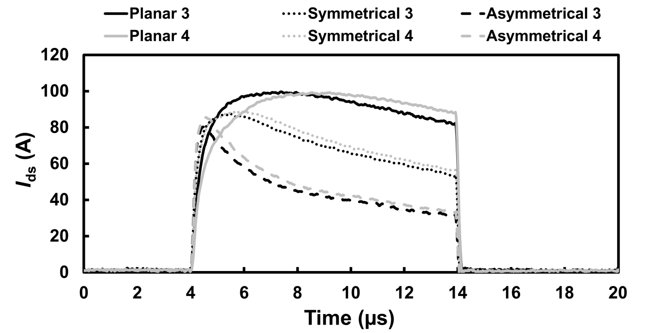


Fig. 7: Impact of T_{case} difference on short circuit current distribution.

reduced, resulting in the asynchronous turn-on and uneven current distribution, which is particularly obvious for Planar devices.

4.2 Degradation of key parameters

4.2.1 Degradation of V_{th}

The degradation of V_{th} of DUTs are illustrated in Figure 8. The V_{th} of both planar devices does not present any sign of degradation after 100 cycles of short circuit stress, albeit slight fluctuation. For Symmetrical trench devices, the device with higher T_{case} ultimately has more V_{th} degradation, which decreases from 4.58 V to 4.42 V. With respect to Asymmetrical trench devices, a more significant degradation has also occurred to the device with higher T_{case}, whose V_{th} reduces from 4.71 V to 3.58 V within 100 cycles, while V_{th} for the device tested at room temperature only drops from 4.72 V to 4.29 V. It seems that for Symmetrical and Asymmetrical trench devices, although the higher short circuit current is higher for devices with lower T_{case}, the initial high T_{case} has more impact on the device degradation.

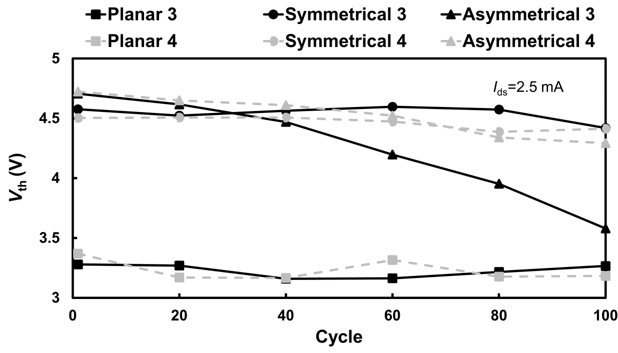


Fig. 8: Degradation of V_{th} under short circuit test with different T_{case}.

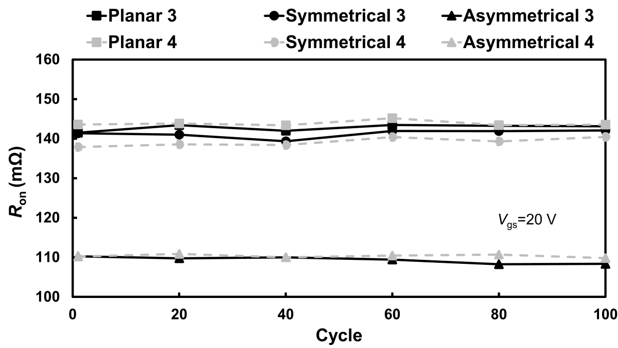


Fig. 9: Degradation of R_{on} under short circuit test with different T_{case}.

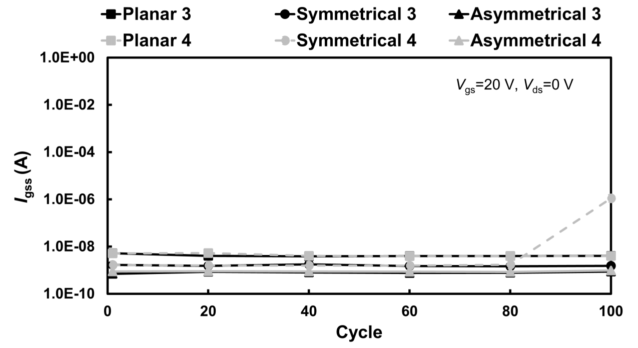


Fig. 10: Degradation of I_{gss} under short circuit test with different T_{case}.

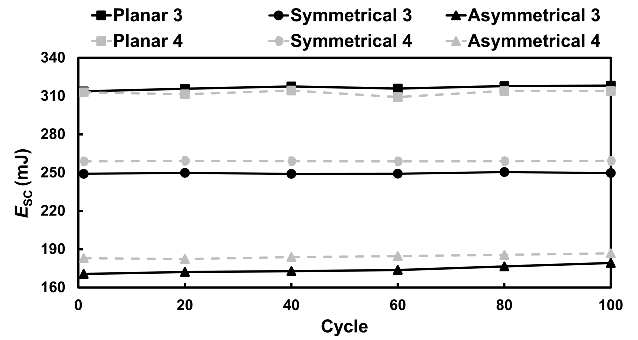


Fig. 11: Degradation of E_{sc} under short circuit test with different T_{case}.

4.2.2 Degradation of R_{on}

The degradation of R_{on} of DUTs with different T_{case} are illustrated in Figure 9. For three types of devices, the effect of uneven T_{case} distribution will not cause obvious R_{on} degradation between parallel-connected devices after 100 cycles of short circuit impulses. The drift region, chip surface and packaging of Planar, Symmetrical and Asymmetrical trench devices are still intact.

4.2.3 Degradation of I_{gss}

The degradation of I_{gss} after 100 short circuit cycles are shown in Figure 10. According to the test results, the Symmetrical trench device with lower T_{case} has the lowest gate oxide reliability. Although its I_{gss} is still low, the sudden increase of I_{gss} after 80 cycles indicates irreversible damages has already arisen inside. As for the rest of devices, I_{gss} remains at nA level, suggesting their gate oxides are still healthy.

4.2.4 Degradation of E_{sc}

To investigate the degradation of static parameters on the short circuit behaviour of parallel-connected devices under different T_{case}, E_{sc} under different test cycles has been computed and demonstrated in Figure 11. Interestingly, E_{sc} is smaller for planar device with lower T_{case} while it is smaller for Symmetrical and Asymmetrical trench devices with higher T_{case}. In addition, E_{sc} is quite steady for Planar and Symmetrical trench devices. For both Asymmetrical trench devices, E_{sc} increases, and the device with higher temperature has larger variation because larger V_{th} reduction.

5 Conclusion

In this paper, the impact of R_g and T_{case} difference on short circuit current distribution and device degradation of parallel-connected SiC MOSFETs is discussed. Results indicate that parallel Asymmetrical trench devices are sensitive to uneven R_g because of its fast switching speed, while the Planar and Symmetrical trench SiC MOSFETs are less affected by R_g differences. In addition, the devices with lower R_g degrade faster because of higher electrical-thermal stress caused by larger short circuit current and higher E_{sc}. The uneven distribution of T_{case} has a significant effect on current distribution for all types of devices.

Based on test results, Planar devices almost exhibit no degradation after 100 cycles of short circuit test, and the device with higher T_{case} has larger E_{sc}. However, Symmetrical and Asymmetrical trench devices with higher T_{case} degrade faster and have lower E_{sc}.

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