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Experimental Analysis of Short Circuit Robustness of GaN and SiC Cascode Devices

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Abstract

The short circuit evaluation of the GaN and SiC cascode devices is characterized in this paper. The effects of three different parameters, gate resistors, DC-link voltages and temperature on the short circuit have been analyzed and discussed. Since the short circuit incapability of 650 V GaN cascode device, most of the parameters are decreased as much as possible. On the other hand, 650 V SiC power cascode device shows the highest short circuit current and energy in comparison with high rated GaN and SiC power cascode devices under various conditions.

1 Introduction

The gallium nitride (GaN) and silicon carbide (SiC) have become the most promising materials compared to conventional silicon (Si) material for power semiconductor devices due to their predominant features, containing of lower on state resistance, the higher saturation velocity and larger critical electric field concluding the high speed switching performance and high power density [1], [2]. One of the most significant parameter to asses the reliability of these devices is their capability for withstanding the short circuit state that could cause thermal and mechanical stress on the device. This test can be set with the single pulse. Regarding the oxide thickness of the SiC MOSFET, it is smaller than that of the conventional Si MOSFET. This can cause the increase of the sensitivity of the electron tunneling in the gate-oxide layer. The tunneling is the one of the reliability concern in SiC MOSFETs [3], [4]. Short circuit current may increase this tunneling impact in SiC MOSFETs [5]. The SiC cascode devices differ from the SiC MOSFETs with Si MOSFET as a gate, therefore SiC cascode device has advantage with the absence of the gate oxide layer in terms of the device reliability [6], [7]. In this paper, the short circuit capability of the GaN and SiC cascode devices have been tested and compared each other under various conditions, such as temperature gate resistors and DC-link voltage levels.

2 Experimental Results

The short circuit test is set up to understand the functioning and robustness of 650 V GaN (TPH3212PS), 650 V SiC (UJ3C065080T3S), 900 V GaN (TP90H180PS) and 1200 V SiC (UJ3C120150K3S) cascode devices as illustrated in Fig. 1 with the test rig that is used in the experiments. The effect of the three parameters have been analyzed on the short circuit current of the power devices, such as DC-link voltage level, temperature and gate resistor. The DC-link voltage is increased from 10 V to 30 V, in steps of 10 V for 1 μs period to see the impact on the short circuit currents of the SiC and GaN cascode devices at room and high temperature as well as two different gate resistors 10 Ω and 100 Ω are used in the experiments to investigate the influence on the short circuit currents of the cascode power devices.

2.1 The impact of the gate resistors on the short circuit currents

To analyze the effect of the gate resistors on the short circuit ruggedness of the four cascode devices, 10 Ω and 100 Ω gate resistors are used and drain currents and gate voltages of the cascode devices under 10 V DC-link voltage at room tem-

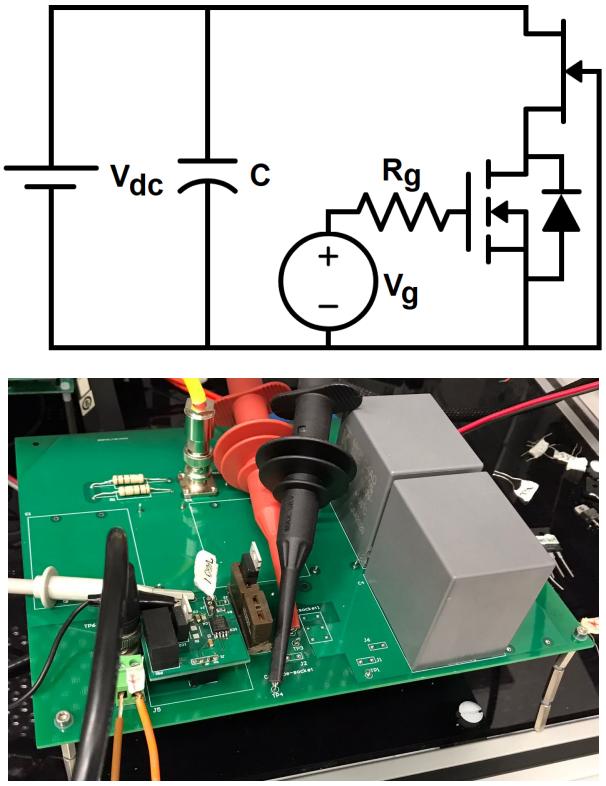

Fig. 1: The schematic of the short circuit test for cascode devices and test rig that is used in experimental measurements.

perature are shown in Fig. 2 and Fig. 3. As it is seen in the figures, the decreasing the gate current, slower the switching of all four devices and this can be clearly seen in the 650 V GaN cascode devices which has the smallest input capacitances compared to other devices that results in that this device has the highest short circuit current under same condition. As it is clearly seen in all plots, the turn off transients of the cascode shows great oscillations this might cause the failure of the 650 V GaN cascode devices since its fast switching rate leads the larger stray inductance through the cascode configuration and this results in the ruggedness failure of the HEMT [8].

For establish a precise comparison between the cascode devices, the drain currents of all cascode devices are combined and illustrated in Fig. 4. The 650 V GaN device is directly failed after applying 10 V DC link voltage for the short circuit with 10 Ω and 100 Ω gate resistors, therefore it could not be tested under the higher short circuit stresses with higher DC-link voltage and high temperature. As it is seen, the only difference can be seen in the drain current trends of the 650 V GaN with 10 Ω and 100 Ω, it results in the peak current of nearly

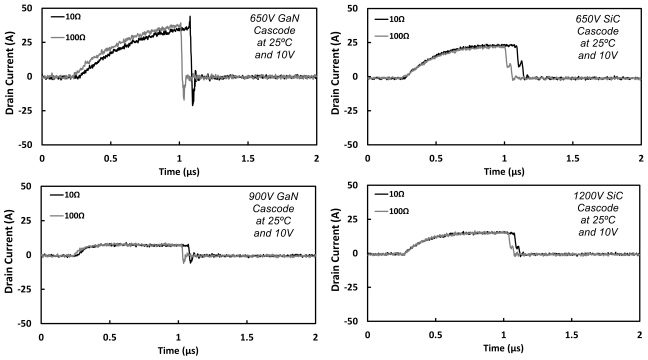

Fig. 2: The short circuit currents of the 650 V SiC, 650 V GaN, 1200 V SiC and 900 V GaN cascode devices with different gate resistors under 10 V DC-link voltage at 25 °C.

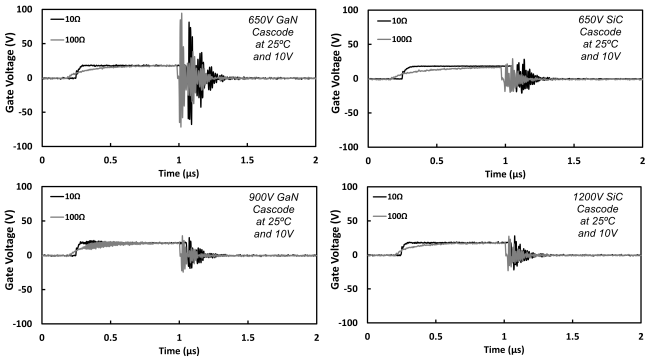

Fig. 3: The gate voltages of the 650 V SiC, 650 V GaN, 1200 V SiC and 900 V GaN cascode devices with different gate resistors under 10 V DC-link voltage at 25 °C.

48 A, then the device is failed.

The short circuit stress level is increased by rise of the DC-link voltage to 30 V as well as temperature is risen to 175 °C to observe the impact of the gate resistors on the short circuit currents and gate voltages of the 650 V SiC, 900 V GaN and 1200 V SiC cascode devices under high DC-link voltage at high temperature. The results are demonstrated in Fig. 5. Concerning the drain currents of the cascode devices under 30 V DC-link voltage at 175 °C, it is unvarying for the 650 V SiC cascode with larger gate resistor, whereas it is increasing for the 900 V GaN cascode device and decreasing for the 1200 V SiC cascode device with higher gate resistor. The increase of the short circuit current with increasing the gate resistor for GaN cascode can be related to that the increase of the resistor can lead increase gate source voltage that causes the increase of the on state resistance and higher current density in the device. With respect to short circuit current of SiC cascode device, its decrease with increasing

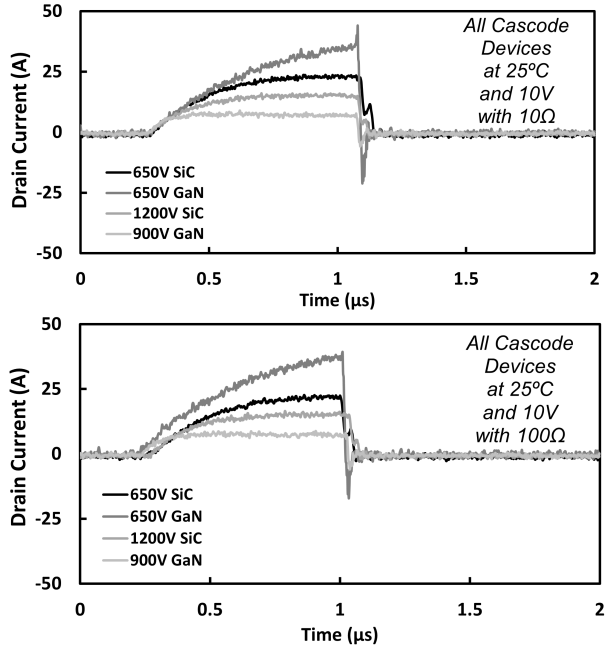

Fig. 4: The short circuit currents of the four cascode devices with 10 Ω and 100 Ω gate resistors under 10 V DC-link voltage at 25℃.

gate resistor can be associated with that increasing gate resistor slow down the device switching and causes the delay that leads the decrease of the current rise rate and short circuit current peak.

The short circuit currents of the all three cascode devices are integrated and shown in Fig. 6 to make a clear comparison between them under DC-link of 30 V with two different gate resistors at high temperature. Regarding to current level, it is high for the 650 V SiC with both gate resistor compared to high rated cascode devices,while it is higher for the 900 V GaN with 10 Ω gate resistor than the 1200 V SiC and it is vice versa with 100 Ω gate resistor. The 650 V SiC encounters larger short circuit current, since the power dissipation in this device is much larger than high rated counterparts. The short circuit energy of the low rated and high rated cascode devices has been calculated under 10 V DC-link voltage at room temperature for both gate resistors and illustrated in Fig. 7. It is clearly seen that the low rated cascode devices have been faced larger short circuit energy compared to high rated cascode devices, particularly with low gate resistor around 100 mj. However, the 650 V GaN is not durable to overcome higher short circuit energy. In addition to this the voltage and temperature are increased, then the short circuit energy of three cascode devices has been calculated and indicated in Fig. 8 to distinguish the short circuit capability of the

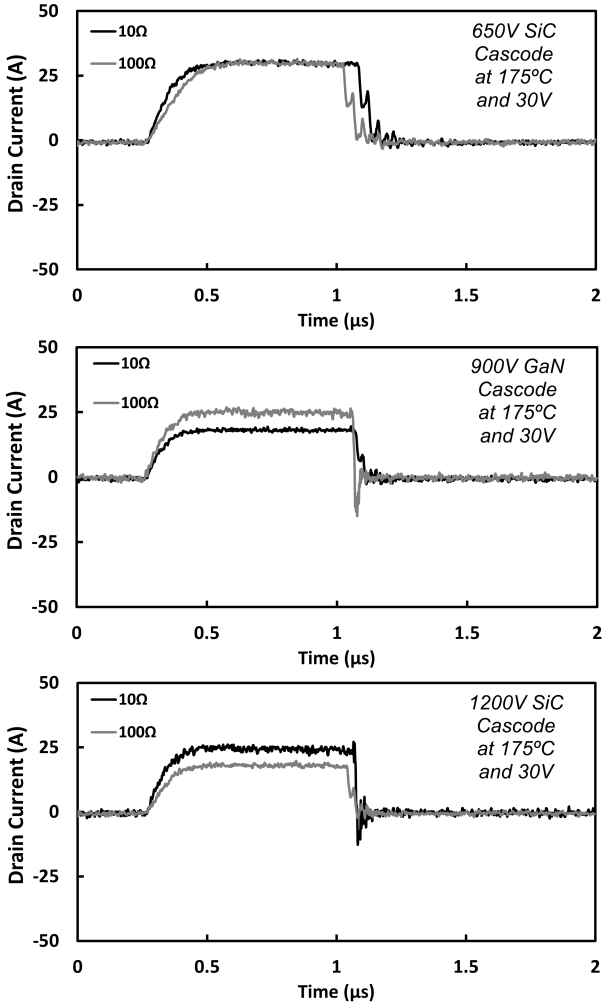

Fig. 5: The short circuit currents of the 650 V SiC, 900 V GaN and 1200 V SiC cascode devices with different gate resistors under 30 V DC-link voltage at 175℃. The 650 V GaN cascode device is failed after 10 V single pulse.

cascode devices. With increasing temperature and DC-link voltage level, 900 V GaN cascode device presents higher short circuit energy compare to 1200 V SiC, unlike with lower level of temperature and DC-link voltage.

The comparison between the low rated and high rated cascode devices regarding the short circuit energy has been demonstrated in Fig. 9. As it is seen in the figure, the low rated SiC exhibits larger short circuit energy in comparison with high rated cascode devices. The 650 V SiC cascode devices dials with the largest short circuit energy under different conditions.

2.2 Short circuit currents concerning the DC-link voltages

The short circuit stress is increased with DC-link voltage level, for that reason the DC-link voltage is

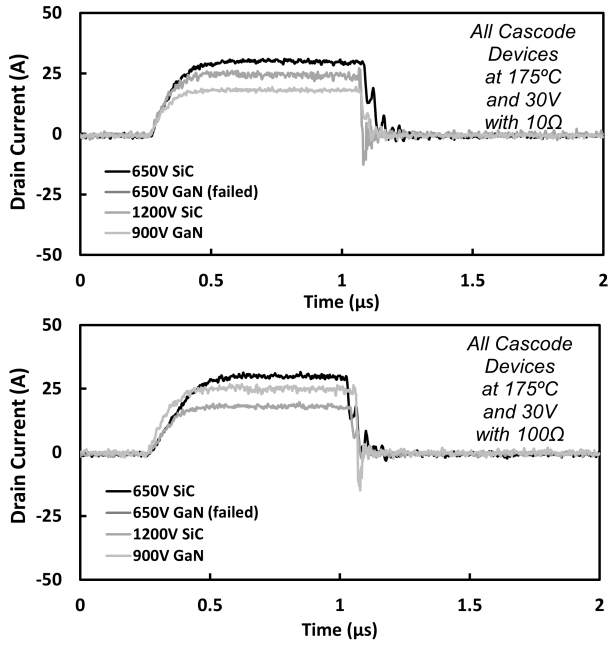

Fig. 6: The short circuit currents of the three cascode devices with 10 Ω and 100 Ω gate resistors under 30 V DC-link voltage at 175℃.

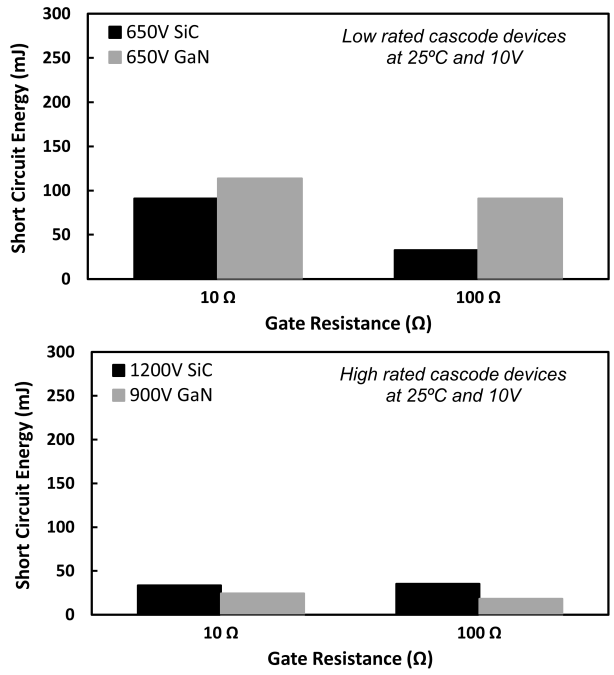

Fig. 7: The short circuit energy of the cascode devices with 10 Ω and 100 Ω gate resistors under 10 V DC-link voltage at 25℃.

changed from 10 V to 30 V to perceive the alteration in the drain source currents of the 650 V SiC, 900 V GaN and 1200 V SiC cascode power devices at room temperature with 10 Ω gate resistor, as it is shown in Fig. 10. The changes of the DC-link voltage level is proportional to the short circuit current

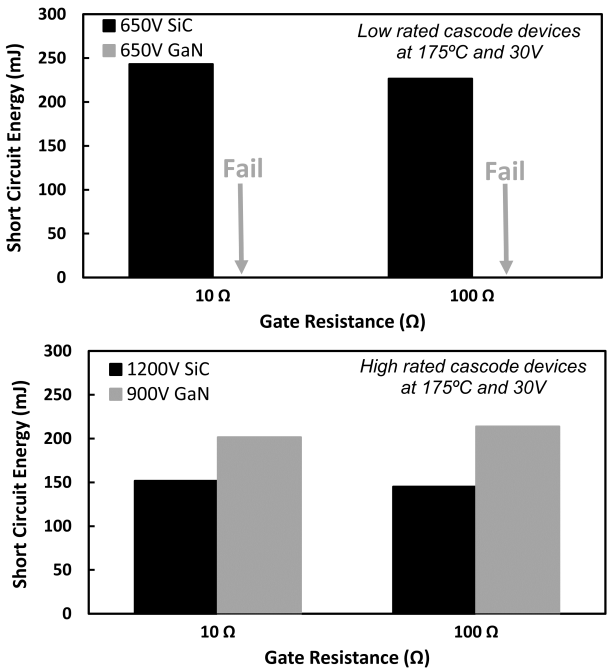

Fig. 8: The short circuit energy of the cascode devices with 10 Ω and 100 Ω gate resistors under 30 V DC-link voltage at 175℃.

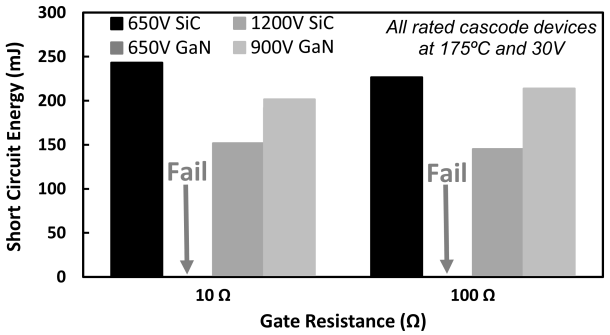

Fig. 9: The short circuit energy of the cascode devices with 10 Ω and 100 Ω gate resistors under 30 V DC-link voltage at 175℃.

of the cascode devices with 10 Ω at 25℃. Furthermore, the short circuit energies of these three cascode devices have been calculated with 10 Ω gate resistor at 25℃ as they are highlighted in Fig. 11 to evaluate the impact of the DC-link voltage levels on them. It is obvious that the short circuit energy of three cascode devices has multiplied by the DC-link voltage that is directly used in calculation of the short circuit energy as a parameter.

2.3 The temperature sensitivity of the short circuit currents

In this part, the temperature impact on the short circuit performance of the cascode devices have been investigated. The short circuit currents of the SiC

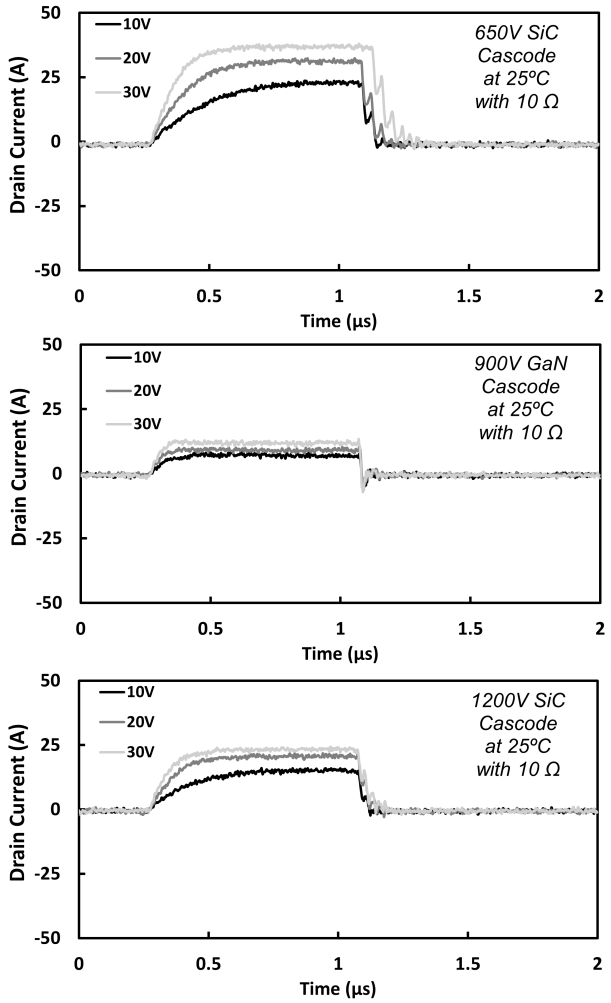

Fig. 10: The short circuit currents of the 650 V SiC, 900 V GaN and 1200 V SiC cascode devices with 10 Ω and 100 Ω gate resistors under vary DC-link voltages at 25℃. The 650 V GaN cascode device is failed after 10 V single pulse.

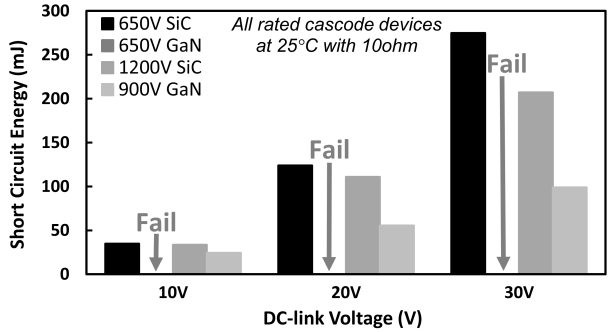

Fig. 11: The short circuit energy of the cascode devices with 10 Ω gate resistor under vary DC-link voltage at 25℃.

cascode devices are decreasing with increasing of the temperature, whilst it is increasing for the GaN as it is illustrated in Fig. 12. The increase of the short circuit current in GaN cascode can be related to current collapse phenomenon that rises the channel resistance temporarily during switching period. This phenomenon is especially seen in the device at high temperature where current density have become irregular and concentrated on narrow regions that results in the higher on state resistance and reduction of the current carrying capacity [9], [10].

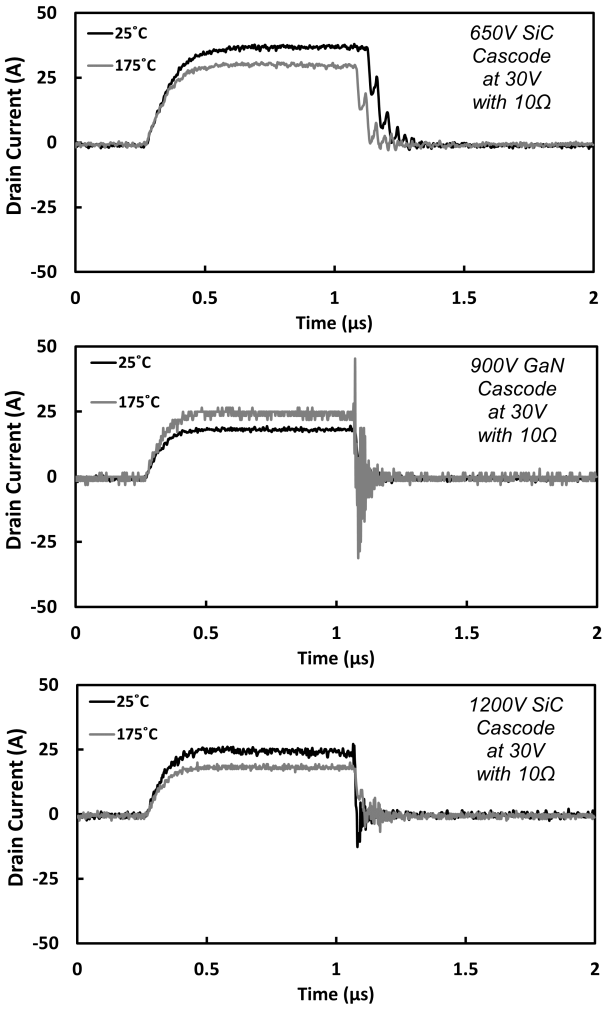

Fig. 12: The short circuit currents of the 650 V SiC, 900 V GaN and 1200 V SiC cascode devices with 10 Ω gate resistors under 30 V DC-link voltages at 25℃ and 175℃. The 650 V GaN cascode device is failed after 10 V single pulse.

Considering the short circuit energy of the WBG cascode power devices under 30 V with 10 Ω gate resistor, indicated in Fig. 13, the 650 V SiC cascode device displays greater short circuit energy than the high rated cascode power devices. This is due to smaller chip area and smaller thermal energy storage in 650 V SiC cascode device that causes quicker heating and cooling of the device during the short circuit test. These processes results in

the hot spots in the device structure that increases short circuit energy dissipation of the device [11].

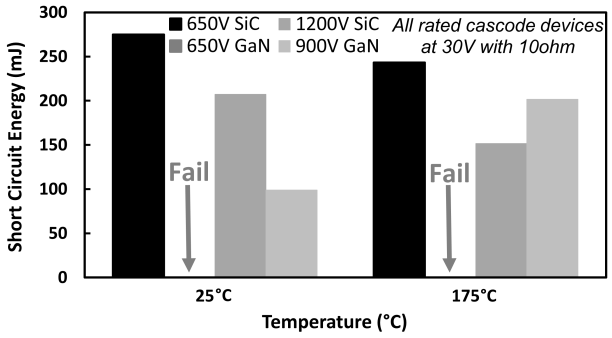

Fig. 13: The short circuit energy of the cascode devices with 10 Ω gate resistor under 30 V DC-link voltage at different temperature.

The temperature coefficient of the pinch off voltage leads increase of the drain current with higher temperature in SiC cascode devices, whereas the negative temperature coefficient results in decrease of the drain current with higher temperature. From this perspective, the impact of the temperature coefficient is higher than the temperature coefficient of the pinch-off voltage for the 650 V and 1200 V SiC cascode devices [12].

3 Conclusion

In this paper, the short circuit ruggedness capability of the power cascode devices have been evaluated and compared with each other under different conditions, such as the variety of gate resistor, DC-link voltage, temperature. As it shown, the 650 V GaN cascode device has failed, even with very low level of DC-link voltage for very short period. This can be related to that the 650V GaN has less capability of the short circuit with poor thermal management in comparison with other counterparts. Besides, low rated cascode devices have more short circuit energy, than the high rated cascode devices even when the temperature, DC-link voltage and gate resistor are increased in turn by reason of the internal resistances of low rated devices is higher and leading higher power dissipation in the device structure and concluding larger short circuit energy in low rated devices.

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