Degradation Analysis of Planar, Symmetrical and Asymmetrical Trench SiC MOSFETs Under Repetitive Short Circuit Impulses

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***Abstract*—In this paper, the reliability of Planar, Symmetrical, and Asymmetrical trench SiC MOSFETs is analysed under repetitive short circuit impulses at 300 K and 450 K. Both static and dynamic parameters are measured to characterize the degradation pattern of the three MOSFET structures. The degradation mechanisms are analysed and the internal electro-thermal behavior of MOSFETs is revealed through TCAD models. It has been found out that there is minor degradation for Planar SiC devices under both test conditions. The Symmetrical trench SiC MOSFET has the lowest reliability, which fails after 200 and 80 cycles at room and elevated temperature. The Asymmetrical trench SiC MOSFET has slightly higher reliability, failing after 1500 cycles and 500 cycles at room and elevated temperature, respectively. A comprehensive range of measurements until failure and the corresponding Silvaco TCAD analysis confirms that for both trench SiC MOSFETs, the deterioration of the gate oxide is responsible for the degradations and device failure. The higher the temperature, the higher electro-thermo-mechanical stress the devices suffer.**

***Index Terms*—Device Degradation, Trench, SiC MOSFET, Short Circuit, Reliability, TCAD**

I. Introduction

DUE to extraordinary properties of Silicon Carbide (SiC) material, SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices have received wide attention. Compared with Silicon (Si) Insulated Gate Bipolar Transistor (IGBT), SiC MOSFETs have smaller chip area, higher switching speed, and smaller on-state resistance (R_{on}), and such advantages are being further exploited together with the improving device technology. Since the first commercial SiC MOSFET was produced in 2012, many manufacturers have launched different kinds of products to make better use of the SiC material [1], [2]. However, the improvement of figures of merit (FOM) of SiC MOSFET devices proposes new challenges to the device reliability, especially under extreme conditions such as short circuit, where massive heat is produced and concentrated inside the chip and cannot be dissipated outside timely [3]. Typical short circuit withstand time (SCWT) is over 10 μs for Si-IGBTs, but it is currently considered too onerous for SiC MOSFET to withstand the short circuit electrothermal stress for a similar period, as this will currently result in irreversible degradation or direct failures [4], [5].

The short circuit reliability is one of the most important indicators when selecting devices. To compare and characterize the short circuit performance of SiC MOSFETs, many researchers have carried out experiments on SiC MOSFETs from different vendors and with different structures. For instance, SCWT and critical energy of Rohm and Cree SiC MOSFETs were compared in [6]. The effect of the dc-link voltage and case temperature were discussed. In [7], the short circuit robustness of 650 V SiC Planar MOSFET and trench MOSFET was compared. According to experimental results, the trench MOSFET failed much earlier than the Planar MOSFET because of higher current and heat density. In [8], the failure modes of Asymmetrical trench and double trench SiC MOSFETs were clarified. The results indicated that the Asymmetrical trench MOSFET failed either because of gate rupture or thermal runaway, depending on the dc-link voltage, whereas the double trench MOSFET always failed due to thermal runaway. Except from destructive tests, non-destructive experiments have also been performed to shed light on the long-term short circuit reliability. F. Boige et al. explained the degradation pattern of SiC MOSFETs from different manufacturers and derived the relational model between gate leakage current (I_{gss}) and test condition [9], [10]. In [11], [12], J. Wang et al. applied repetitive short circuit stress to Planar MOSFETs for hundreds of cycles. Static parameters such as threshold voltage (V_{th}), R_{on} and I_{gss} were monitored. The degradation of parameters was attributed to the traps at the SiC/SiO_2 interface and the injection of negative charges into the gate oxide. In [13], repetitive experiments were carried out on Planar SiC MOSFETs under various gate voltages (V_{gs}) and time durations. Thermal models were developed and the degradations were proved to be affected by thermal stress. The mechanical failure at the gate dielectric and gate-source short circuit were observed. In [14], the impact of short circuit time on the direction of drift of V_{th} in repetitive tests was investigated on Planar SiC MOSFET devices. Two competing mechanisms (hot hole injection and thermally activated electron emission) were found to be responsible

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for the bidirectional drift of V_{th}. In [15], [16], different magnitudes of V_{gs} were applied on Planar and Trench Gate SiC MOSFETs in repetitive short circuit tests. It has been found that the trapping of holes and electrons were dependent on V_{gs}, but the degradation of Planar MOSFET was more pronounced because the trapping of carriers was located at the channel region for Planar device, while it happened at the trench corner for the Trench Gate SiC MOSFET. In [17], the degradations of the dynamic performances such as turn-on/off time and turn-on/off energy were monitored with limited insights. Above-mentioned research has provided valuable information on the device reliability, but they failed to evaluate the device performance and reliability more comprehensively, clarify the degradation mechanism of dynamic parameters in addition to static parameters, and identify the potential reasons causing the reliability difference among MOSFETs with different structures at various stress conditions. Nevertheless, filling these gaps and figuring out underlying mechanisms are of importance to understand the long-term reliability of SiC MOSFETs. Thus, repetitive short circuit tests are conducted to Planar, Symmetrical and Asymmetrical trench SiC MOSFETs at different temperatures in this paper. The degradations of static and dynamic parameters are characterized and underlying mechanisms are thoroughly illustrated. Technology Computer Aided Design (TCAD) models for all three MOSFETs are developed to reveal the internal electro-thermal behaviour and to provide support for explaining their reliability difference.

The contents of the paper are arranged as follows: Section II introduces the test setup and test conditions. Basic test results of Planar, Symmetrical and Asymmetrical trench MOSFETs are presented and the difference among devices is compared. Section III and Section IV focus on the degradation patterns and mechanisms of a wide range of static and dynamic parameters at 300 K and 450 K, respectively. TCAD models for Planar, Symmetrical and Asymmetrical trench MOSFETs are established in Section V. The electro-thermal behavior inside the chip during the short circuit process are simulated and demonstrated. Section VI concludes the paper.

II. Experiment Methodology

A. Experimental Setup

The devices under test (DUTs) are from Rohm and Infineon. The Planar, Symmetrical and Asymmetrical trench SiC MOSFETs are with same voltage rating and similar current rating (1200 V/22 A, 1200 V/17 A, 1200 V/19 A, respectively). The gate driver provides a V_{gs} of +17 V to reduce R_{on}, and a negative V_{gs} of -5 V is applied to turn off the device safely [18], [19]. The R_g is selected to be 20 Ω to avoid ringing and voltage spikes. In repetitive short circuit experiments, the dc-link voltage is 400 V. The short circuit duration (t_{sc}) of 10 μs is chosen, as it is the typical required time in industry [5], [20]. Although well-designed protection circuits for SiC MOSFET devices are able to cut off the short circuit fault within several μs, the worst condition should be investigated to leave margin to assure long-term reliability. The interval between each short circuit impulse is 5 s to make sure that there is not any heat accumulation after each impulse, and the initial temperature is same in the repetitive test. The test setup is shown in Fig. 1(a), where the drain-source current (I_{ds}) is measured by the Rogowski coil (CWT1), and the drain-source voltage (V_{ds}) is measured by the differential probe (GW-Instek GDP-100). The data are recorded by the oscilloscope (Keysight MSO7104 A 1-GHz 4GSa/s). To heat up the device to a certain temperature, a heating block is attached to the back of the device in the elevated temperature measurement.

To monitor the degradations of DUTs throughout the test, static and dynamic performances are characterized after 1, 5, 50, 500, 1000, ... up to 5000 cycles. If significant degradation or distortion of waveforms is observed, the test cycle is reduced to capture useful data. Static parameters (V_{th}, R_{on}, and I_{gss}) are measured by the source meter (Keysight B2902A) shown in Fig. 1(b). The dynamic parameters are calculated based on the switching waveforms, achieved by the double pulse test (DPT) board shown in Fig. 1(c). To avoid random error, all static parameters are tested three times.

B. Experimental Results

The variations of I_{ds} and V_{gs} of three DUTs at 300 K and 450 K after the first and at the last cycle are shown in Fig. 2 and Fig. 3, respectively. According to experimental results at room temperature, the Planar MOSFET has the highest reliability and is able to withstand 5000 times of short circuit impulses without significant degradation. The Symmetrical trench MOSFET has the lowest reliability and fails after 200 cycles. Both I_{ds} and V_{gs} are greatly lowered after the test. The Asymmetrical trench MOSFET has the lifetime of 1500 cycles. It also suffers from the decrease in I_{ds} and V_{gs}, indicating the increase in R_{on} and I_{gss}.

When the case temperature is increased to 450 K, all SiC MOSFETs experience degradation to varying degrees, and their reliability is reduced significantly compared with the results at 300 K. I_{ds} of Planar SiC MOSFET decreases after 5000 cycles, but the gate oxide remains intact because there is no degradation in V_{gs}. For Symmetrical trench MOSFET, I_{ds} decreases after 80 cycles and V_{gs} is reduced at the end of the test, indicating that the gate oxide has been damaged. With regard to the Asymmetrical trench MOSFET, it fails within 2 μs at the 500th cycle test, which is only one third of the lifetime at room temperature. However, it is interesting to observe that its current at the last cycle is slightly higher than the initial value. One reasonable assumption is that V_{th} is decreased after the test, which enables earlier and faster switch of the device in the short circuit transient.

The dimension of three types of devices are scanned by computerized tomography (CT) to compare the short circuit energy (E_{sc}) density after the 1st cycle at both temperatures. It has been calculated that the chip area of Planar, Symmetrical and Asymmetrical trench MOSFETs are 24.52, 5.76 and 3.61 mm^2, respectively. The E_{sc} density comparison of three types of MOSFETs is plotted in Fig. 4. Thanks to the largest chip area of Planar SiC MOSFETs, the devices have the lowest energy density, and the least temperature dependence, which

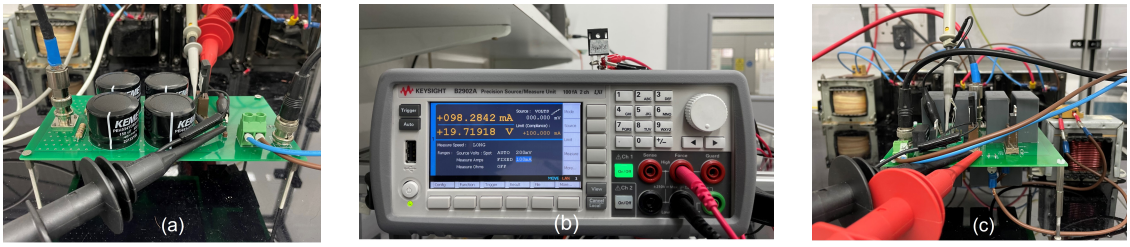

Fig. 1. Experiment setup (a) Short circuit test rig, (b) Static parameter test rig, (c) DPT test rig.

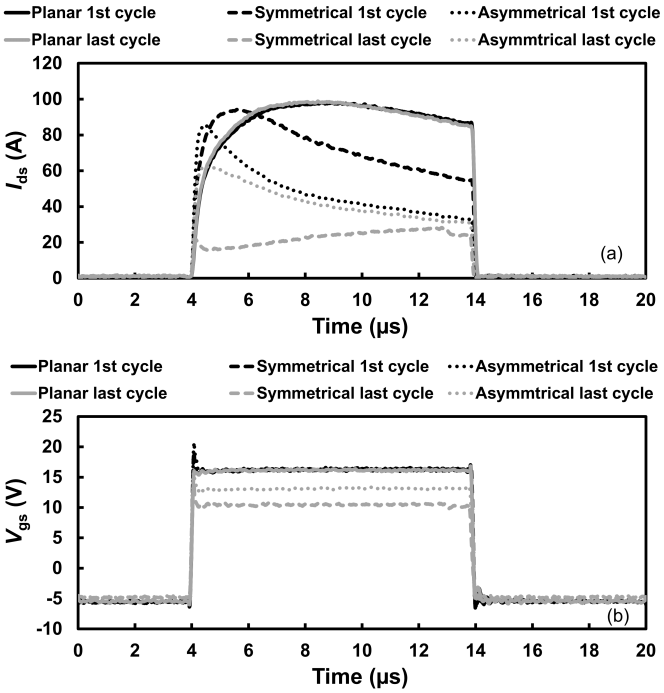

Fig. 2. Comparison of DUTs at 300 K. (a) I_{ds}, (b) V_{gs}.

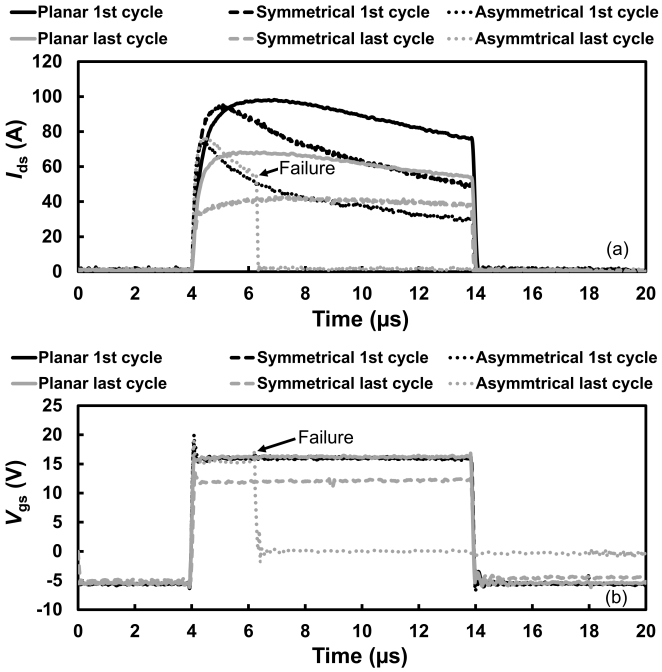

Fig. 3. Comparison of DUTs at 450 K. (a) I_{ds}, (b) V_{gs}.

contributes to the high reliability at elevated temperature. Compared with Symmetrical trench MOSFET, the chip area of Asymmetrical trench MOSFET is smaller, so the latter device has higher E_{sc} density and shows more sensitivity to temperature because of more concentrated heat. However, compared with Asymmetrical trench MOSFETs, Symmetrical trench MOSFETs fail faster, indicating that the high E_{sc} density induced by the small chip area may not be the only reason leading to the device failure.

III. Degradation of SiC MOSFETs under 300 K Repetitive Short Circuit Test

A. Static Parameters

1) V_{th}: V_{th} is one of the paramount parameters for SiC MOSFET. In this test, the constant current method is adopted to measure V_{th} [21], and no preconditioning protocol was applied. V_{th} is measured under the condition of V_{ds}=0.1 V, and is defined by sweeping V_{gs} from 0-20 V and when I_{ds} reaches 2.5 mA, in line with datasheets parameters. As can be seen in Fig. 5, V_{th} of Planar MOSFET remains stable at around 3.1-3.2 V, indicating that its gate oxide is stable. For

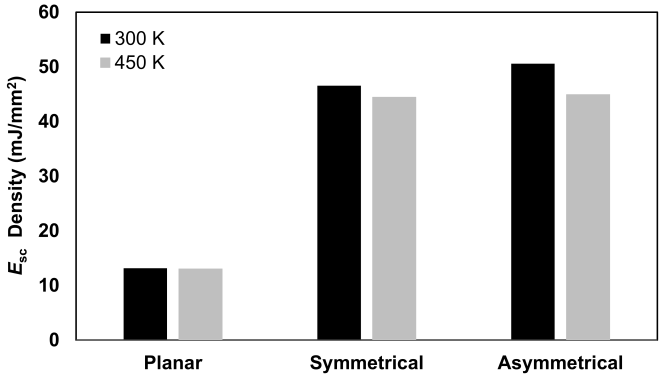

Fig. 4. E_{sc} density comparison of three SiC MOSFETs in 300 K and 450 K experiments.

Symmetrical trench SiC MOSFET, V_{th} maintains at 5.0 V at first 50 cycles, but it starts to decrease afterwards and reaches to 4.76 V at the end of the test. The Asymmetrical trench SiC MOSFET suffers from the severest V_{th} degradation among three devices. V_{th} falls sharply from 4.74 V to 2.87 V from the first cycle to the 500th cycle. Then the degradation becomes

slower, and V_{th} eventually drops to 2.74 V. The reason of negative V_{th} drift is speculated to be the result of the capture and accumulation of positive charges inside the oxide [22].

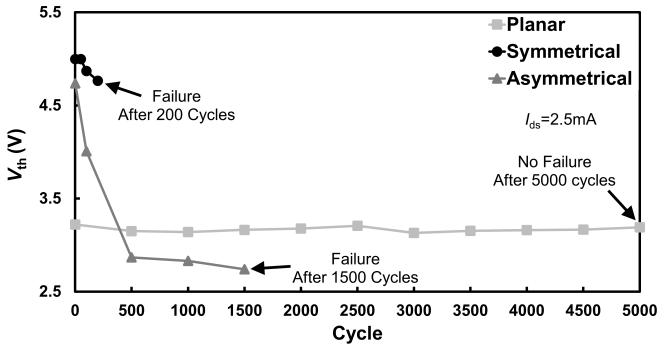

Fig. 5. Variation of V_{th} of three SiC MOSFETs in 300 K experiment.

2) R_{on}: R_{on} of SiC MOSFET is mostly composed of source contact resistance (R_{cs}), channel resistance (R_{ch}), accumulation resistance (R_a), JFET region resistance (R_{jfet}), drift region resistance (R_{drift}), N^+ substrate resistance (R_{sub}), drain contact resistance (R_{con}), and the resistance caused by the packaging (R_p). At low V_{gs}, R_{ch} accounts for the majority of the overall resistance, while R_{drift} dominates at high V_{gs}. Also, when the packaging is degraded to certain extent, R_p will also be increased. Thus, by selecting different test V_{gs} to measure R_{on}, a rough degradation reason could be speculated. To characterize R_{on} degradation, V_{gs} is swept from 0-20 V, and V_{ds} is kept at 0.1 V. For all types of devices, R_{on} is calculated based on the I_{ds} at low V_{gs} (10 V) and high V_{gs} (20 V), respectively.

According to Fig. 6(a), R_{on} of Planar MOSFET barely changes at low V_{gs}, indicating there is almost no degradation in the channel region. R_{on} of Symmetrical trench MOSFET fluctuates a little bit at first, but it decreases from 547 mΩ after the 50th cycle to 516 mΩ at the last cycle, which is the reflection of the decreased V_{th}. The initial variation before 50 cycles is because the MOSFET has not degraded yet. With regard to R_{on} of the Asymmetrical trench MOSFET, it decreases by 25.21% from the first cycle to the last cycle, and the trend is similar to the degradation of V_{th}. When higher V_{gs} is applied, R_{on} of Planar MOSFET still does not exhibit obvious degradation, indicating there is no degradation in the drift region or packaging. The trend of R_{on} degradation is different for Symmetrical trench SiC MOSFET compared with results at lower V_{gs} test. One explanation is that the gate oxide gradually degrades as the short circuit test continues, resulting in the increase in I_{gss} and voltage cross R_g. With lowered V_{gs} that actually applies on the gate, the measured R_{on} is increased. As for Asymmetrical trench MOSFET, there is minor variation of R_{on} at V_{gs} of 20 V. After 500 cycles, R_{on} cannot be measured at given condition because the V_{gs} is largely reduced.

3) I_{gss}: I_{gss} is a intuitive indicator of the gate oxide healthiness. Although I_{gss} is 100 nA for three devices in the datasheet, the value is quite conservative. In this paper, I_{gss} is tested by sweeping V_{gs} from 0 to 20 V while keeping drain-source electrodes short-circuited. The plotted I_{gss} is

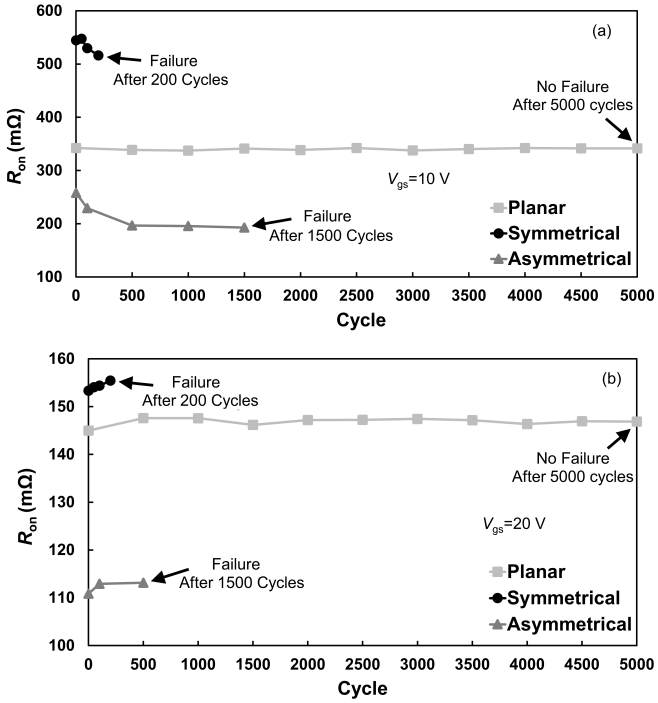

Fig. 6. Variation of R_{on} of three SiC MOSFETs in 300 K experiment (a) At low V_{gs}, (b) At high V_{gs}.

selected at the point of V_{gs}=20 V and V_{ds}=0 V, referred to datasheets. The degradation of the I_{gss} is shown in Fig. 7. For Planar MOSFET, the overall trend for I_{gss} is flat despite slight fluctuation, and I_{gss} keeps stable at nA level, which means its gate oxide is not degraded. However, I_{gss} for Symmetrical and Asymmetrical trench MOSFETs rises sharply after 50 and 100 cycles, respectively, implying initial defects has been created. With the progress of test, the defects gradually evolve to irreversible and fatal damages to the device. As mentioned above, since I_{gss} gradually increases, the voltage drop caused by R_g is increased. In this way, the effective V_{gs} applied to the chip will be decreased, which leads to the increase in R_{on} in the measurement.

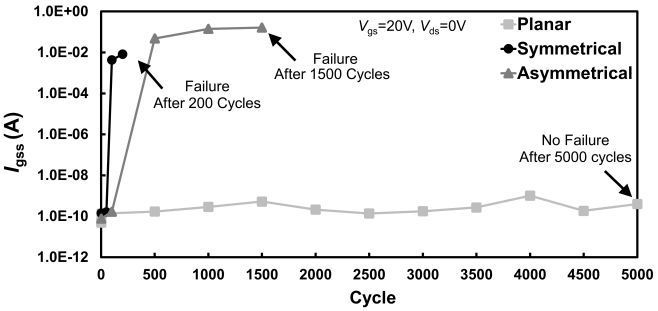

Fig. 7. Variation of I_{gss} for Planar, Symmetrical, and Asymmetrical trench SiC MOSFETs in 300 K experiment.

B. Dynamic Parameters

Since SiC MOSFET devices often work in switching states, it is necessary to investigate the effect of degradation induced by short circuit events on the switching performances and understand the underlying mechanisms. Thus, DPT is performed, where the inductor is 1.2 mH, V_{ds}=400 V, and I_{ds}=12 A. It is noted that in the test, R_g is chosen to be 100 Ω to help slow down the switching speed and capture more details during the process. The following key parameters are all acquired from the switching waveforms.

1) t_{off} and t_{on}: t_{off} and t_{on} reflect the switching speed of the three SiC MOSFETs. According to [17], t_{off} is specified as the period from 90% V_{gs} to 90% V_{ds} in the turn-off transient, and t_{on} is specified as the duration from 10% V_{gs} to 10% V_{ds} in the turn-on transient. In Fig. 8, the degradation of switching time has been plotted. It can be seen that Planar MOSFET has the longest switching time, while the Asymmetrical trench MOSFET switches the fastest. Also, the switching time of Planar MOSFET barely changes from the first to the last cycle. For Symmetrical trench MOSFET, t_{off} decreases slightly but t_{on} does not show pronounced degradation. For Asymmetrical trench MOSFET, t_{off} and t_{on} decrease at first because the decrease in V_{th} increases the switching speed. However, when there is significant degradation within the gate oxide (large I_{gss}), the switching time is increased.

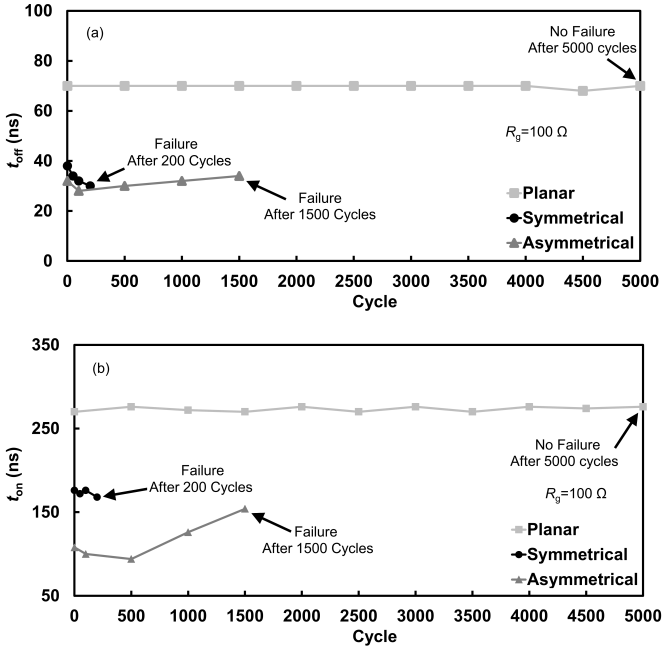

Fig. 8. Switching time of three devices at R_g=100 Ω in 300 K experiment. (a) Turn-off, (b) Turn-on.

2) Turn-off |dv/dt| and |di/dt|: The turn-on and turn-off transient for the SiC MOSFET is symmetrical, so the equations for current and voltage in these two processes are similar. According to [23], dv/dt of the device can be written as Eq.(1), where the voltage switching rate is related to V_{gs}, R_g, miller platform voltage (V_{gp}), and transfer capacitance (C_{gd}).

$$\frac{dV_{ds}}{dt} = \frac{V_{gs} - V_{gp}}{R_g \cdot C_{gd}(V_{ds})} \tag{1}$$

The current of SiC MOSFET can be written as Eq.(2), and its switching rate can be derived as Eq.(3) [24]. The current slew rate is transferred into the derivative of V_{gs}. Since the change of V_{gs} is the charging process of the input capacitance (C_{iss}), the variation of V_{gs} can be illustrated as Eq.(4), where V_{gg} is the voltage provided by the gate driver. The final form of di/dt is written as Eq.(5), where W_g and L_g are the width and length of the gate. It can be seen that the current switching rate is related to geometric parameters and other key parameters, such as oxide capacitance (C_{ox}), electron mobility (μ_n), V_{th}, R_g and C_{iss}.

$$I_{ds} = \mu_n C_{ox}\left(\frac{W_g}{L_g}\right)\frac{\left(V_{gs} - V_{th}\right)^2}{2} \tag{2}$$

$$\frac{dI_{ds}}{dt} = \frac{\mu_n W_{ch} C_{ox}\left(V_{gs} - V_{th}\right)}{L_{ch}}\frac{dV_{gs}}{dt} \tag{3}$$

$$V_{gs} = V_{gg}\left(1 - e^{\frac{-t}{C_{iss}R_g}}\right) \tag{4}$$

$$\frac{dI_{ds}}{dt} = \frac{\mu_n W_g C_{ox}\left(V_{gg}\left(1 - e^{\frac{-t}{C_{iss}R_g}}\right) - V_{th}\right)V_{gg}}{L_g C_{iss} R_g e^{\frac{t}{C_{iss}R_g}}} \tag{5}$$

Since the switching transient is fast and short, if two points are arbitrarily selected from the switching waveforms to calculate dv/dt and di/dt, large errors may occur. To avoid errors in data processing, the voltage and current waveforms during the switching process are differentiated to time. The absolute peak value of dv/dt in the voltage rising phase and the absolute peak value of di/dt in the current falling phase are referred to the turn-off dv/dt and di/dt, and are plotted in Fig. 9. For Planar MOSFET, |dv/dt| and |di/dt| stay stable with minor variation. For Symmetrical trench MOSFET, both |dv/dt| and |di/dt| increase in the first few cycles. After 50 cycles, |dv/dt| and |di/dt| start to decrease because large I_{gss} has been detected. Thus, the effective V_{gs} applied on the device is reduced, which is responsible for the reduced slew rates based on Eq.(1) and Eq.(5). With regard to Asymmetrical trench MOSFET, when I_{gss} is insignificant before 500 cycles, the reduced V_{th} helps to increase the |dv/dt| and |di/dt| according to Eq.(1) and Eq.(5). After 500 cycles, the turn-off speed gradually decreases. During this time, V_{gs} is significantly decreased because of large I_{gss}. V_{gp} is also reduced due to the decrease in V_{th}. However, the drop of V_{gs} is larger than the reduction of V_{gp}, and plays a more important role in the switching transient. The combined effect leads to the decrease in |dv/dt| and |di/dt| eventually. It should be mentioned that although V_{th} has shifted throughout the test, C_{iss} does not change and affect the switching speed. On one hand, C_{gd} is saturated at high V_{ds}, so the thickness of depletion region barely changes, which stands for both Planar and trench MOSFETs [17], [25]. On the other hand, despite large I_{gss} reduces V_{gs}, C_{gs} is actually not affected by the applied

V_{gs} [26]. Thus, the degradation of dynamic parameters has nothing to do with the capacitance of the SiC MOSFET, and is virtually caused by the degradation of V_{th} and I_{gss}.

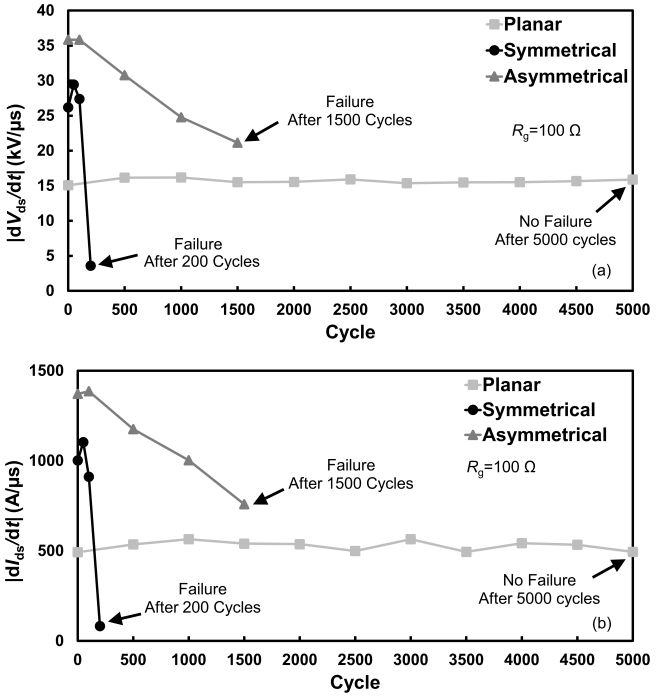

Fig. 9. Turn-off speed of three devices at R_g=100 Ω in 300 K experiment.

3) Turn-on |dv/dt| and |di/dt|: Similarly, the degradation mechanism of turn-on |dv/dt| and |di/dt| for three DUTs can also be explained like the turn-off process (|dv/dt| refers to the absolute peak value of dv/dt in the voltage falling phase and |di/dt| refers to the absolute peak value of di/dt in the current rising phase during turn-on transient). For Planar SiC MOSFET, the degradations of turn-on |dv/dt| and |di/dt| are still negligible as shown in Fig. 10, indicating its high stability. For Symmetrical trench MOSFET, |dv/dt| and |di/dt| remain relatively stable compared with the turn-off transient. As to Asymmetrical trench MOSFET, at the first 100 cycles, |dv/dt| and |di/dt| increase merely because of the decreased V_{th}. From 100 cycles to 500 cycles, I_{gss} increases sharply from 20 nA to 47.9 mA, resulting in the large decrease in V_{gs} in the DPT. The reduced V_{gs} outperforms the effect of V_{th}, which represents as the decrease in |dv/dt| and |di/dt|.

4) Switching Energy: Switching energy is affected by multiple factors, such as transient switching rates, oscillations, and dynamic R_{on}. The turn-on/off switching energy for the three devices, as E_{on}/E_{off}, and total switching energy for the three devices as E_{sw}, which is the sum of E_{off} and E_{on}, are depicted in Fig. 11. For Planar MOSFET, the device is still healthy because the other dynamic parameters are not degraded. The fluctuations in E_{off}, E_{on}, and E_{sw} are amplified due to its slowest switching speed. For Symmetrical trench MOSFET, the decreased V_{gs} leads to the increase in dynamic R_{on} and E_{off}. The reduction of E_{on} is attributed to the decrease in V_{th}, and E_{sw} increases after large I_{gss} appears. With regard to the Asymmetrical trench MOSFET, the increase in E_{off}

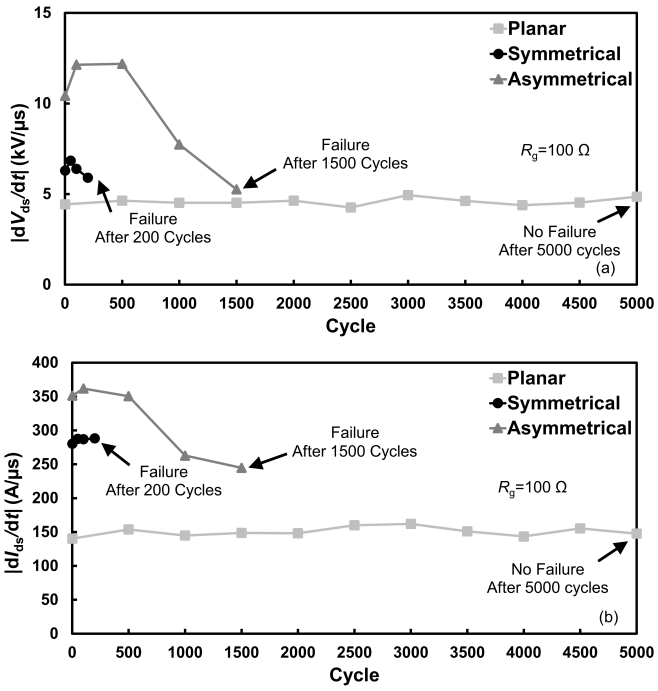

Fig. 10. Turn-on speed of three devices at R_g=100 Ω in 300 K experiment.

before 100 cycles is owing to the increased oscillation in the switching process, and the decrease in E_{on} is caused by the increase in switching rate. After 100 cycles, E_{off} is reduced because the oscillation is mitigated by the reduced turn-off speed, while E_{on} is increased because of the prolonged turn-on time. The combined impact of E_{off} and E_{on} finally leads to the increase in E_{sw}. It should be noted that the oscillation is only discussed in the turn-off transient because turn-off speed is much faster compared with the turn-on speed. Based on the degradation of dynamic parameters discussed above, it could be found out that before the gate oxide suffers from severe degradation (large increase in I_{gss}), the degradation of dynamic parameters is mostly influenced by V_{th}. After the gate oxide is damaged, the dynamic performances of the device depend more on the lowered V_{gs} instead of the drift in V_{th}.

IV. Degradation of SiC MOSFETs under 450 K Repetitive Short Circuit Test

SiC MOSFET devices often work under elevated temperatures. It is necessary to carry out repetitive short circuit experiments and understand the long-term reliability of devices at elevated temperature.

A. Static Parameters

1) V_{th}: The degradation of V_{th} is shown in Fig. 12. Similar to the results at 300 K, V_{th} of Planar SiC MOSFET remains stable around 3.2 V, proving its high reliability even at elevated temperature. The V_{th} drift of Symmetrical trench SiC MOSFET is minor and there is only a 0.2 V fluctuation between the highest and lowest value throughout the experiment. The Asymmetrical trench SiC MOSFET still has the largest V_{th} drift. From the first cycle to the 100th cycle,

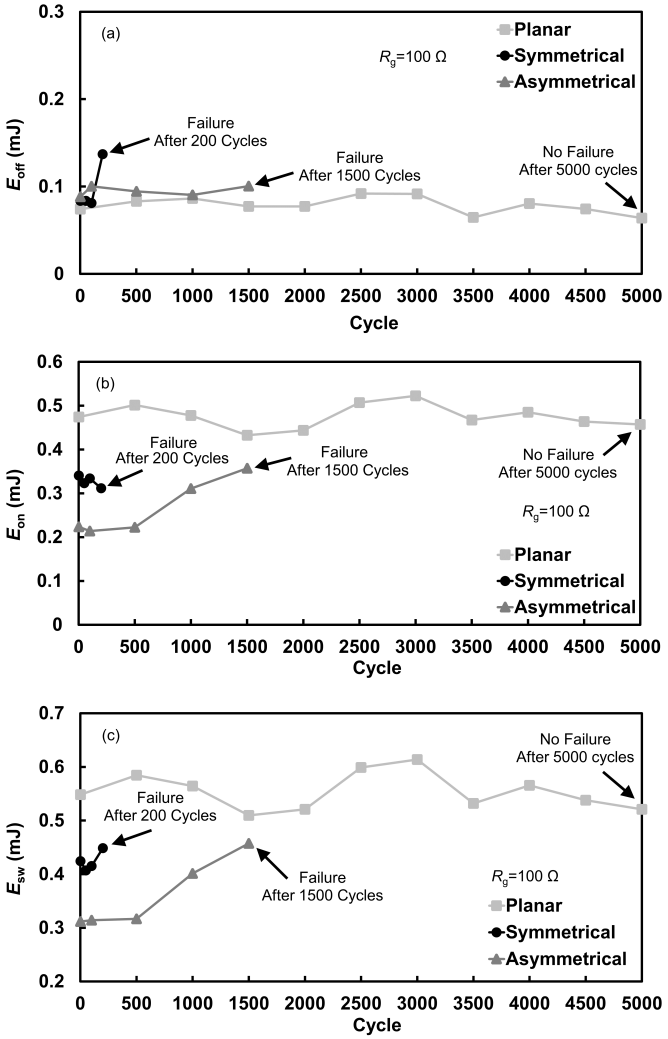

Fig. 11. Switching Energy of three devices at R_g=100 Ω in 300 K experiment (a) E_{off}, (b) E_{on}, (c) E_{sw}.

V_{th} is lowered by 1.73 V. It should be mentioned that at the 500th cycle, the gate and source electrodes of Asymmetrical trench MOSFET are short-circuited, so the degradation of parameters cannot be tested anymore.

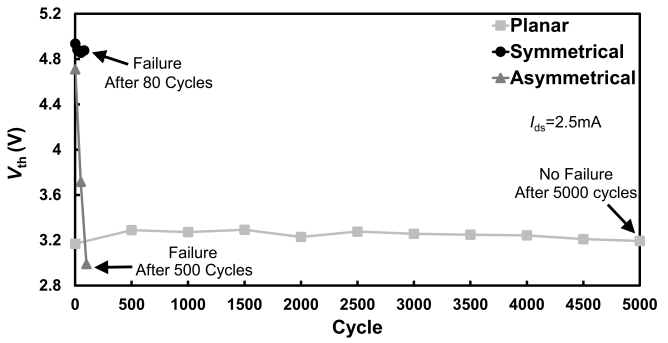

Fig. 12. Variation of V_{th} of three SiC MOSFETs in 450 K experiment.

2) R_{on}: As mentioned before, when V_{gs} is low, the channel region occupies most resistance. When V_{gs} is high, the resistance in the drift region accounts for the majority. It can be seen in Fig. 13, at low V_{gs}, the variation of R_{on} for Planar and Symmetrical trench MOSFETs is small, but R_{on} of Asymmetrical trench MOSFET keeps decreasing, which is the reflection of the reduced V_{th} due to the injection of holes into the oxide. At elevated V_{gs}, R_{on} of Planar MOSFET increases with test cycles. Since its V_{th} does not have obvious degradation, the increase in R_{on} might not be caused by the degradation of chip itself, but is more likely to be related to the fatigue failure of bond wires due to large thermo-mechanical stress [27]. R_{on} of Symmetrical and Asymmetrical trench MOSFETs remain stable, and their variations can be neglected (maximum 3.5 mΩ for Symmetrical trench MOSFET and 2.6 mΩ for Asymmetrical trench device), indicating no drift region or packaging related degradation.

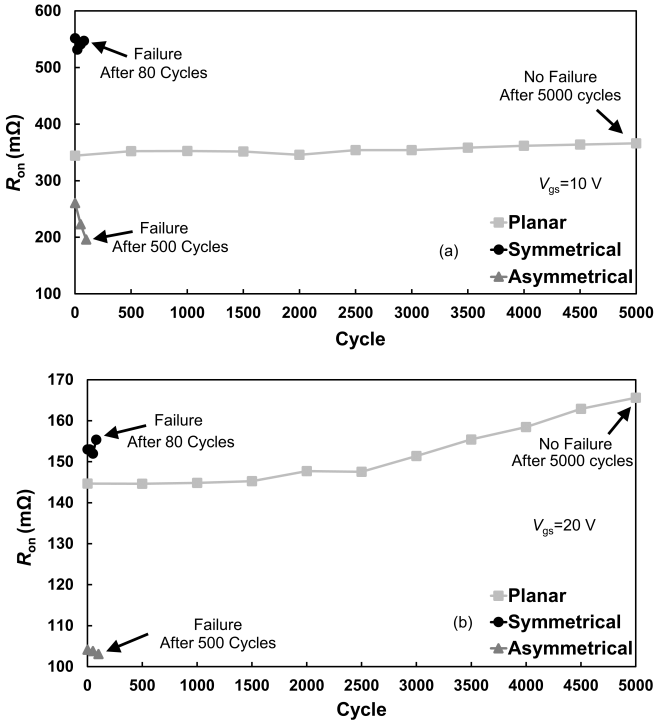

Fig. 13. Variation of R_{on} of three SiC MOSFET in 450 K experiment (a) At low V_{gs}, (b) At high V_{gs}.

3) I_{gss}: The degradation of I_{gss} directly reflects the reliability of gate oxide at 450 K experiment. It can be seen from Fig. 14 that the Planar MOSFET is very reliable even under 450 K test. After 5000 cycles of short circuit impluse, I_{gss} is still at nA level, indicating that the gate oxide is still intact. The Symmetrical trench MOSFET is a rather vulnerable device, whose I_{gss} sharply increases only after the 5th cycle. The reliability of Asymmetrical trench MOSFET is a bit higher, but the device is still very fragile. I_{gss} remains at a low value before 100 cycles, but the gate and source electrodes are short-circuited together at the 500th short circuit test. During the process, the oxide suffers from large electro-thermo-mechanical stress.

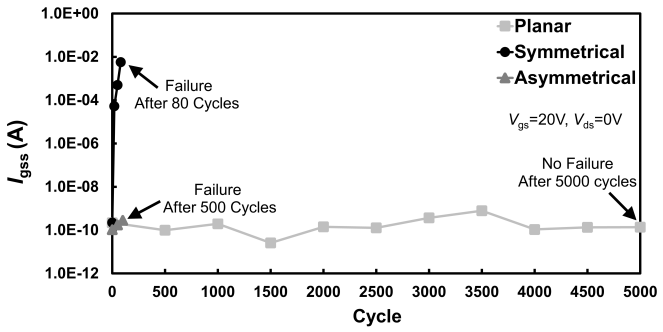

Fig. 14. Variation of I_{gss} for Planar, Symmetrical, and Asymmetrical trench SiC MOSFETs in 450 K experiment.

B. Dynamic Parameters

The switching performances of three devices at 450 K short circuit test are measured under the same test condition as stated above. The current and voltage waveforms after different cycles are captured and key parameters are analyzed.

1) t_{off} and t_{on}: Based on switching waveforms, t_{off} and t_{on} are calculated and the variations are plotted in Fig. 15. Both parameters of Planar MOSFET remain stable throughout the 5000 cycles. The change of Symmetrical trench MOSFET is also negligible, which is reasonable since its V_{th} variation is minor. For Asymmetrical trench MOSFET, the reduced V_{th} leads to a decrease in t_{on} because it takes shorter time for V_{gs} to V_{th} [17]. Since the switch-off period is rather fast, the effect of degraded V_{th} on t_{off} is not obvious.

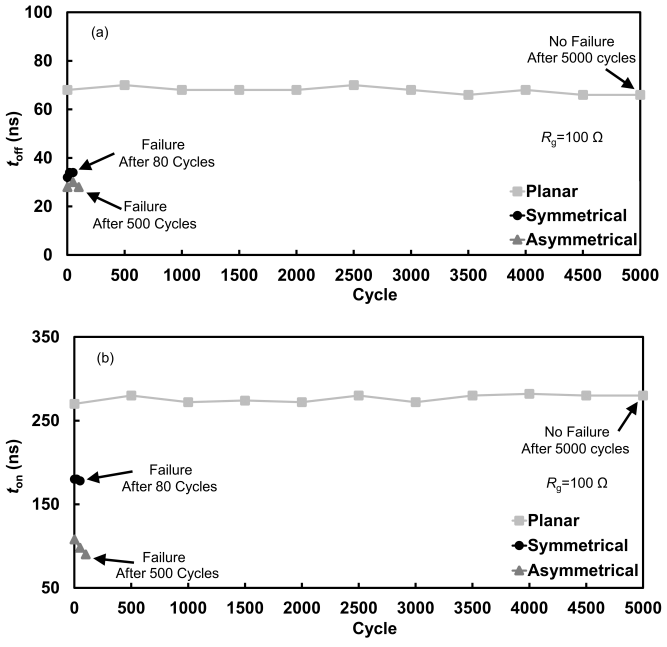

Fig. 15. Switching time of three devices at R_g=100 Ω in 450 K experiment (a) Turn-off, (b) Turn-on.

2) Turn-off |dv/dt| and |di/dt|: Similar to the calculation method at 300 K, the peak turn-off switching rates for Planar, Symmetrical and Asymmetrical trench MOSFETs after certain cycles are compared in Fig. 16. Both |dv/dt| and |di/dt| of Planar SiC MOSFET barely degrade from the first cycle to the last cycle. For Symmetrical trench MOSFET, |dv/dt| and |di/dt| maintain large values before 80 cycles. At the last cycle, the large I_{gss} and the significantly reduced V_{gs} slow down the switching speed. With respect to Asymmetrical trench MOSFET, since no degradation in V_{gs} is seen before 100 cycles, the increase in turn-off speed is only influenced by the decrease in V_{th}.

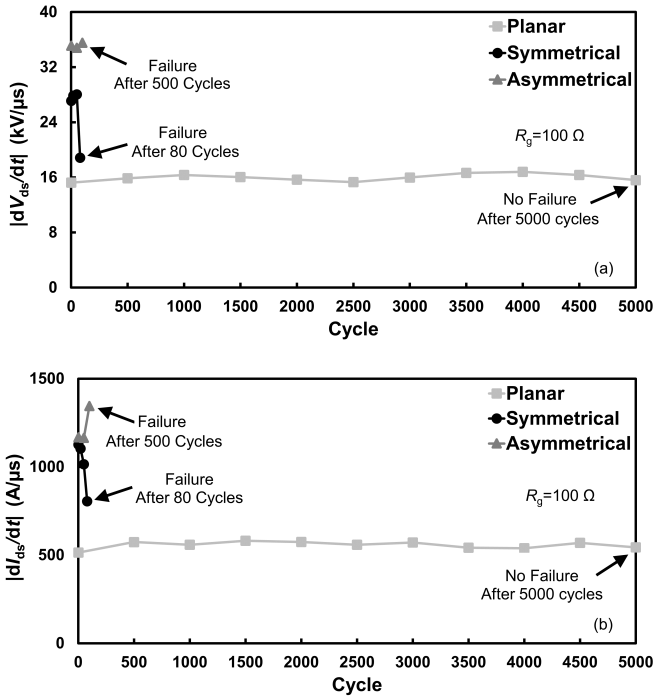

Fig. 16. Turn-off speed of three devices at R_g=100 Ω in 450 K experiment.

3) Turn-on |dv/dt| and |di/dt|: The peak turn-on voltage and current slew rates for Planar SiC MOSFET remain almost invariant before and after repetitive tests, as shown in Fig. 17. For Symmetrical trench MOSFET, the switching speed is decreased at the last cycle because V_{gs} is low and the device performs like a large resistor during the test. For Asymmetrical trench MOSFET, |dv/dt| and |di/dt| increase with the progress of the experiment. In this case, I_{gss} and V_{gs} are not degraded, and the decreased V_{th} is the only influencing factor, different from the results at room temperature.

4) Switching Energy: As mentioned in the last section, the switching energy is decided by switching rates, oscillations, and dynamic R_{on} altogether. For Planar MOSFET, although E_{off}, E_{on}, and E_{on} fluctuate because of oscillation in Fig. 18, the device is relatively reliable. For Symmetrical trench MOSFET, E_{off} and E_{on} remain stable before 80 cycles. After that, the increase in dynamic R_{on} induced by the decreased V_{gs} causes the increase in E_{off}, while the reduced current results in the decrease in E_{on}. Thus, the final E_{sw} exhibits minor variation. For Asymmetrical trench MOSFET, the improved switching speed ultimately causes the decrease in E_{off}, E_{on}, and E_{sw}.

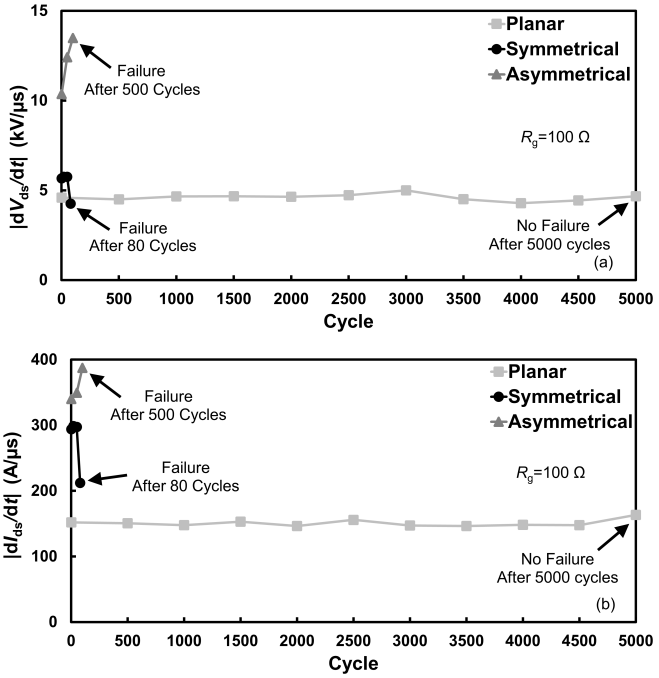

Fig. 17. Turn-on speed of three devices at R_g=100 Ω in 450 K experiment.

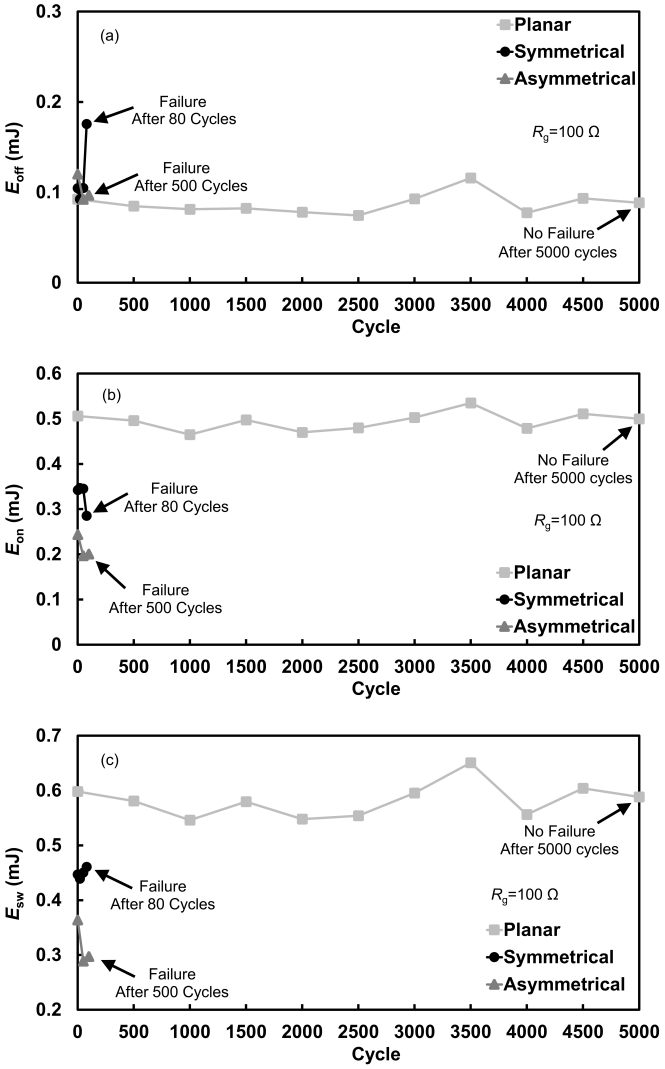

Fig. 18. Switching Energy of three devices at R_g=100 Ω in 450 K experiment (a) E_{off}, (b) E_{on}, (c) E_{sw}.

V. Modeling of SiC MOSFETs during short circuit impulses

A. TCAD Modeling

Typical Planar, Symmetrical and Asymmetrical trench MOSFETs models are referred to [8], [28], [29]. Key parameters have been listed in Table I. The thickness of the substrate is used as a demonstration of a complete device structure, and does not represent the actual thickness of the device. According to [30], most power and heat will be generated above the substrate region, and the temperature is difficult to dissipate to the substrate region during the short circuit transient. Thus, the reduction of the substrate will not affect accuracy of the temperature profile in the heating phase in the simulation. At the meantime, the computational space can be saved and the simulation speed can be improved. Similar method was also adopted in [16].

The electrical stress during the short circuit impulse in the simulation is the same as the experiment: dc-link voltage is 400 V, V_{gs}=17 V, and t_{sc}=10 μs. According to datasheets, the transient junction to case thermal resistance is 0.05 K/W for all three devices within 10 μs short circuit pulse. Thus, the thermal boundary is set from the top of the N channel to the bottom of the drain electrode with a thermal resistance of 0.05 K/W. The ambient temperature is set to be 300 K for the room temperature test, and 450 K is set to simulate the effect of the heating block for the elevated temperature test. Besides, the temperature coefficients of thermal conductivity and thermal capacitance of the SiC material are considered to improve the accuracy referred to [31], [32]. Before the transient simulation, the static characteristics of three devices have been simulated and verified with datasheets within a reasonable margin of error.

TABLE I
Key Parameters of Different SiC MOSFETs

Device Type	Planar	Symmetrical	Asymmetrical
Cell Width (μm)	9	3.6	3
Gate Oxide Thickness (nm)	50	50 (sidewall) 100 (bottom)	75
Channel Length (nm)	500	500	500
N-Drift Thickness (μm)	10	10	11
N+ Substrate Thickness (μm)	1	1	1
Doping of N^+ (cm^{-3})	1×10^{20}	1×10^{20}	1×10^{20}
Doping of P base (cm^{-3})	1×10^{18}	8×10^{17}	5×10^{17}
Doping of P well (cm^{-3})	-	-	5×10^{18}
Doping of N-Drift (cm^{-3})	8×10^{15}	7.5×10^{15}	1×10^{16}
Doping of N+ Substrate (cm^{-3})	1×10^{20}	1×10^{20}	1×10^{20}

The experimental and simulated short circuit currents of Planar, Symmetrical, and Asymmetrical trench MOSFETs at 300 K and 450 K after the first cycle are compared and shown in Fig. 19. It can be seen that the simulation results for all devices match with the measured currents well under both temperatures. Although there are minor differences between results, the overall trends are similar and can be used as general case studies to reveal the electro-thermal behavior of three devices during short circuit.

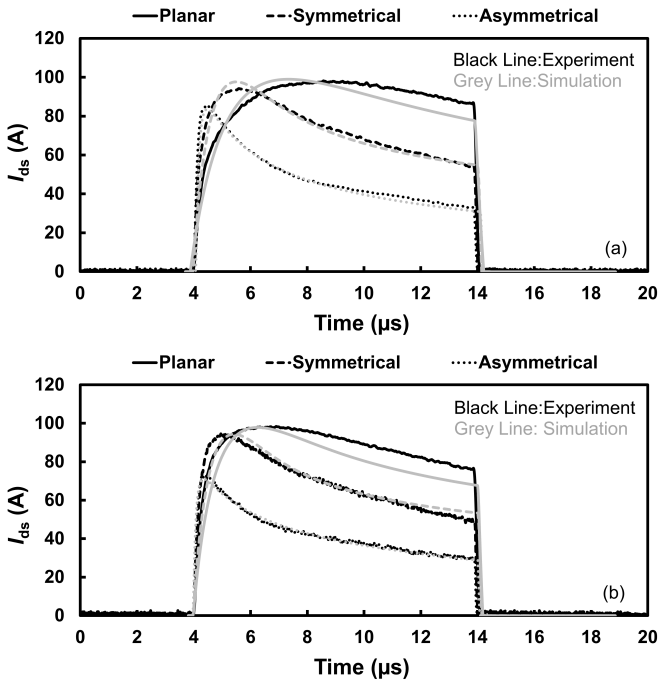

Fig. 19. Comparison of short circuit current between experiments and simulations at (a) 300 K, (b) 450 K.

B. Simulation Analysis

There are three questions for simulation models to answer: 1. What are the underlying reasons for parameter degradation? 2. What causes the reliability difference among different devices? 3. What is the reliability difference between experiments at room temperature and elevated temperature?

To answer the first question, the electric fields and impact ionization rates of Planar, Symmetrical and Asymmetrical trench MOSFETs at room temperature are plotted in Fig. 20. According to the results of Planar MOSFET, it has moderate electric field and low impact ionization rate at the end of the short circuit stress. However, impact ionization rates of Symmetrical and Asymmetrical trench MOSFETs are much higher and concentrated in the channel region, around the corner or at the bottom of the gate oxide, which means electron-hole pairs are likely to be activated in these areas. Due to the manufacture technology and the existence of C atom in SiC MOSFET devices, traps exist inside the gate oxide, at the surface of SiC/SiO_2 or deeper energy levels, and because of the reduced band offsets between SiC and SiO_2 material, carriers are easily captured by traps, which can reduce the reliability of the gate oxide in the long run [33]. At this moment, positive V_{gs} is applied, and the highest electric field locates at sidewalls of the oxide for both trench MOSFETs. The electric field inside the oxide tends to push electrons into the channel and sidewalls while holes are repulsed away from the gate oxide. Thus, during the 10 μs short circuit event, electrons will be injected into the oxide and accumulated in the sidewalls.

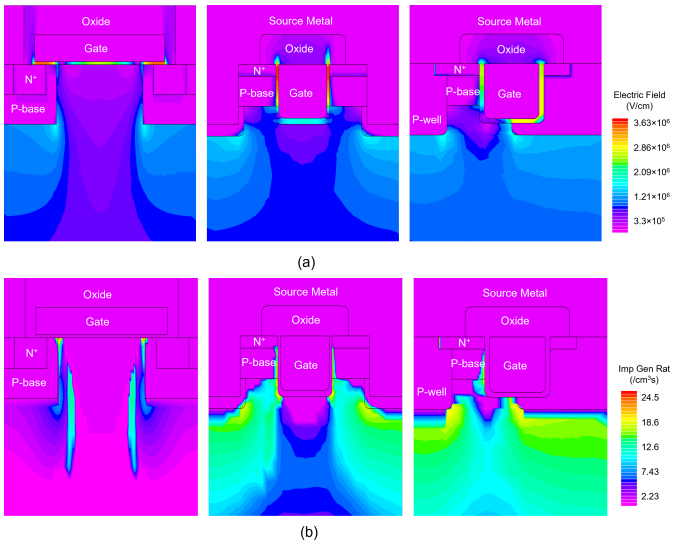

Fig. 20. Electric field and impact ionization rate distribution of Planar, Symmetrical and Asymmetrical trench SiC MOSFETs at t=14 μs, 300 K test. (a) Electric field, (b) Impact ionization rate.

However, the situation is completely opposite when the devices are turned off, and performs more like a high temperature negative gate bias stress because of the residual heat inside the chip after short circuit stress within several μs [34]. The electric field and impact ionization distribution of three MOSFETs with the combined effect of negative V_{gs} and V_{ds} are shown in Fig. 21. The Planar SiC MOSFET still has much lower impact ionization rate compared with the other two devices, which indicates that few electron-hole pairs will be generated and further have the chance to be injected into the gate oxide to cause parameter drift. Nevertheless, the impact ionization rates for Symmetrical and Asymmetrical trench MOSFETs are high under the gate oxide and around the P-N junctions due to rather high temperature and high electric field. Therefore, holes are able to gain enough energy to cross the SiC/SiO_2 barrier and get trapped in the oxide [22]. Based on the distribution of the electric field, the holes trapped at the bottom gate oxide layer move towards the sidewalls and the electrons that previously stored in the sidewalls move downwards. Since the negative V_{gs} lasts longer, more holes are injected into the gate oxide compared with the previous injected electrons and will be trapped deeper as the repetitive short circuit events progress. Thus, the overall drift trends of V_{th} for Symmetrical and Asymmetrical trench MOSFETs are negative, which is the reflection of holes accumulation. It should be mentioned that the interface states or defects are also dependent on MOSFET technology, and it can be reasonably inferred that the oxide of the Planar MOSFET has few interface states, while Asymmetrical trench MOSFET has

higher interface defects compared with the Symmetrical trench one since the V_{th} of Asymmetrical trench one drops much faster.

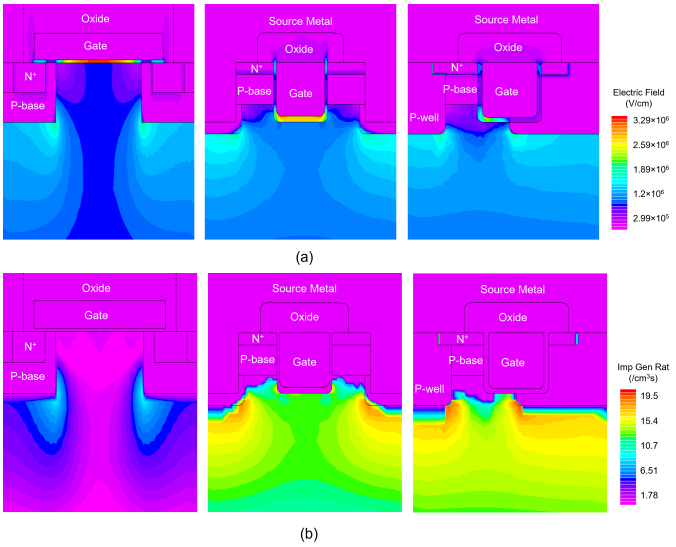

Fig. 21. Electric field and impact ionization rate distribution of Planar, Symmetrical and Asymmetrical trench SiC MOSFETs at t=17 μs, 300 K test. (a) Electric field, (b) Impact ionization rate.

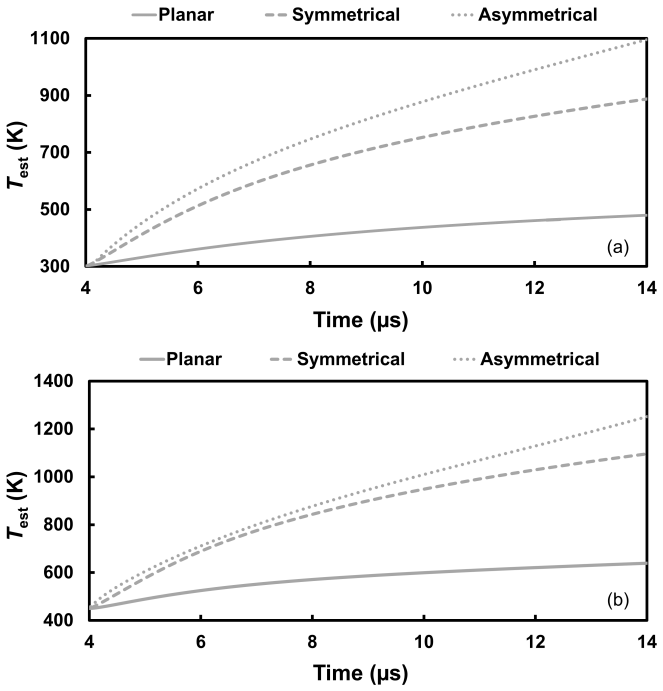

Fig. 22. Temperature comparison of Planar, Symmetrical and Asymmetrical trench SiC MOSFETs at (a) 300 K, (b) 450 K.

Secondly, to reveal the reliability difference among devices, the average estimated temperature based on TCAD (T_{est}) at different temperatures are compared, which is shown in Fig. 22. At room temperature, the Asymmetrical trench MOSFET has the highest average temperature of 1101 K at the end of the short circuit impulse, followed by Symmetrical trench SiC MOSFET (890 K), and the Planar MOSFET with the lowest T_{est} of 480 K. The results are in accordance with the E_{sc} density shown in Fig. 4, where the Planar MOSFET has much lower energy density. The E_{sc} density of Asymmetrical trench MOSFET is higher than the Symmetrical trench MOSFET, resulting in higher temperature correspondingly. At elevated temperature, the Planar SiC MOSFET still has much lower E_{sc} density, thereby having much lower T_{est} compared with trench MOSFETs, which is 640 K. The low T_{est} indicates that the Planar MOSFET is not likely to suffer from internal degradation caused by impact ionization and almost no parameter is degraded indeed. As for Symmetrical and Asymmetrical trench MOSFETs, T_{est} is greatly increased to 1098 K and 1251 K at the end of 450 K experiment. It can be deduced that the elevated temperature is one of the factors that causes the reduced reliability.

According to the conclusion from [35], [36], the failure of SiC MOSFET at medium V_{ds} in destructive short circuit experiment was caused by the gate destruction and underlying reason was explained by the thermo-mechanical models in [37], [38]. The researchers attributed the failure mechanism to be the crack of oxide and the infiltration of the melting Al layer. Thus, the temperature distribution inside Planar, Symmetrical and Asymmetrical trench MOSFETs at the end of the short circuit impulses is depicted in Fig. 23. For Asymmetrical trench MOSFET, with the increase in short circuit time, the internal temperature gradually increases, leading to the increase in mechanical stress between gate oxide and adjacent materials. At the end of short circuit pulse, the temperature at source metal is high enough to melt the Al layer (over 933 K). With the increase in repetitive short circuit impulse, the accumulated mechanical stress will lead to cracking of the gate oxide. Once the crack is formed, the melting Al will seep into the oxide and gradually form a conductive path, resulting in the large increase in I_{gss}. Hence, the accumulation of the thermo-mechanical stress in the gate oxide caused by high temperature is one of the potential reasons to cause the degradation of Asymmetrical trench MOSFET at room temperature. Furthermore, as reported in [34], [39], [40], if the trapped charges in the oxide surmount a certain value or the charges are too close to each other, the electric field across the oxide will be enhanced. Once the critical electric field is reached, the gate oxide breaks down easily. Compared with the Asymmetrical trench MOSFET, the oxide thickness of Symmetrical trench MOSFET is thinner, as listed in Table.I. Thus, the gate oxide of Symmetrical trench MOSFET suffers from higher electric field compared with Asymmetrical trench MOSFET in Fig. 20 and Fig. 21. Also, the gate oxide of Symmetrical trench MOSFET is less tolerable to the accumulation of charges and its maximum sustainable electric field is lower. The high temperature around the gate oxide induces the thermo-mechanical stress and the high impact ionization rate near the gate region. Combined with the high electric field across the thin gate oxide, the dielectric breakdown of the Symmetrical trench device is accelerated, resulting in the large increase in I_{gss} within tens of cycles. It should be noted that although the gate oxide of Planar MOSFET is as thin as the Symmetrical trench

MOSFET, the low temperature and the low impact ionization rate lead to weaker electro-thermo-mechanical stress to the gate oxide, thereby having higher reliability.

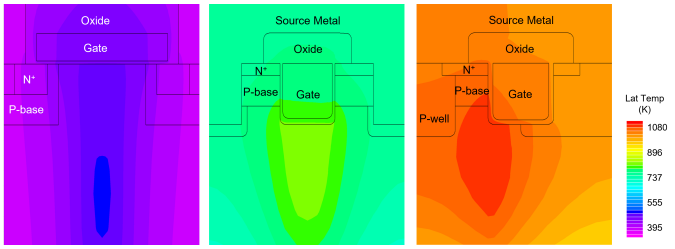

Fig. 23. Temperature distribution of Planar, Symmetrical and Asymmetrical trench SiC MOSFETs at t=14 μs, 300 K test.

Finally, when the case temperature is increased from 300 K to 450 K, T_{est} increases accordingly. For Planar MOSFET, T_{est} is still low enough not to cause any further chip-related degradation, but higher temperature may cause higher fatigue stress between chip surface and wire bonds, resulting in the gradual lift off of wire bonds and the increase in R_{on}. For both Symmetrical and Asymmetrical trench MOSFETs, more electron-hole pairs will be ionized at higher temperature and carriers will gain more energy to overcome the barrier. Hence, degradations and failures are faster. Besides, the temperature distribution of Symmetrical and Asymmetrical trench MOSFETs at 450 K test shown in Fig. 24 reflects that the temperature at the source metal under this test condition is greatly increased, which leads to larger thermo-mechanical stress and reduces the time to cause gate rupture and Al infiltration. Overall, the reduced reliability of three devices gives rise to the enhanced electro-thermo-mechanical stress.

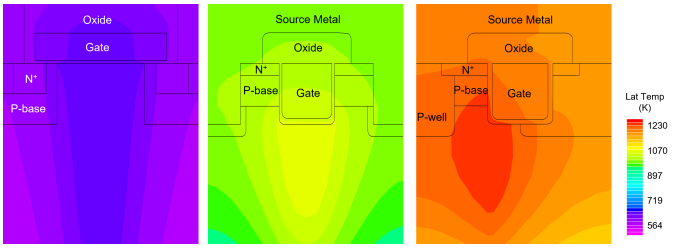

Fig. 24. Temperature distribution of Planar, Symmetrical and Asymmetrical trench SiC MOSFETs at t=14 μs, 450 K test.

VI. Conclusion

In this paper, the degradation patterns and underlying mechanisms of static and dynamic parameters for Planar, Symmetrical and Asymmetrical trench SiC MOSFETs under repetitive short circuit impulses are analyzed using extensive experimental measurements at different temperatures until failure coupled with TCAD analysis. According to experimental results, the Planar SiC MOSFETs exhibit almost no degradation at both 300 K and 450 K experiments, while Symmetrical and Asymmetrical trench SiC MOSFETs undergo severe degradation and eventually fail after a few consecutive short circuit cycles because of large E_{sc} density. It has been found out that the deterioration of the gate dielectric is the root cause of the degradations of parameters in trench structures, and can be reflected from the V_{th} drift and the I_{gss} increase. TCAD models of the three structures of SiC MOSFETs are developed to reveal the internal electro-thermal behavior. Based on the results, the degradation is attributed to the combined stress of negative V_{gs} bias, V_{ds} stress and residual temperature after the short circuit event. With the increase in temperature, the devices suffer from higher stress which leads to the accelerated failures.

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