electronics

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A 19.5 GHz 5-Bit Digitally Programmable Phase Shifter for Active Antenna Arrays

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Abstract: This paper presents the design of a new phase shifter to be used in a receiver of active antenna array operating in the range from 17 GHz to 22 GHz. Beamforming is achieved by controlling the phase of the signal in each radiant element. In this context, the phase shift is obtained by the combination of a quadrature signal generator (QSG) and a variable gain amplifier (VGA). This work is focused on the design of a VGA which has a set of dummy transistors to keep the input and output impedance constant. The phase shifter is digitally programmable using a 5-bit word. The system was laid out using a 65 nm CMOS process, and the physical post-layout results show that the phase shifter achieves root mean square errors of 4.5° for the phase and 0.79 dB for the gain at a frequency of 19.5 GHz. A comparative analysis with other recently published phase shifters shows that the proposed phase shifter presents a good compromise between power consumption and accuracy.

Keywords: active antenna array; beamforming; CMOS technology; phase shifter; VGA

Citation: Esteban Eraso, U.; Sánchez-Azqueta, C.; Aldea, C.; Celma, S. A 19.5 GHz 5-Bit Digitally Programmable Phase Shifter for Active Antenna Arrays. *Electronics* **2023**, *12*, 2862. https://doi.org/10.3390/electronics12132862

Academic Editor: Gaetano Palumbo

Received: 16 May 2023
Revised: 23 June 2023
Accepted: 25 June 2023
Published: 28 June 2023

1. Introduction

Nowadays, the saturation of the lower part of the electromagnetic spectrum requires moving to higher frequencies, such as those in the Ka-band. Operating at these frequencies implies an increment in the design complexity but also brings some benefits, with the most relevant one being that higher frequencies allow it to diminish the size of the antennas, making it easier to build antenna arrays. Using active antenna arrays allows us to increase the total gain and the directivity of the transceiver [1,2], allowing us to steer the radiation pattern electronically (beamforming) [3,4]. Beamforming techniques also provide an increased signal-to-noise ratio (SNR) and accurate focus on the angular direction of incoming signals [5,6]. Owing to these advantages, active arrays are used in the new generation of wireless communication systems (5G) and satellite communications (SATCOM).

In recent years, there has been a growing demand in SATCOM communications for faster beam steering, lower power consumption and higher reliability [7]. In this way, one of the main benefits of the electronic beamforming is that it is faster than mechanical steerable antennas: the beam can be reoriented in just a few microseconds [8]. Moreover, as electric motors or moving parts are not needed, the power consumption decreases, and the reliability increases. Moreover, antenna arrays also allow it to work with multiple beams simultaneously.

There are different techniques for beamforming [5]. These techniques can be classified into time-domain beamforming [9] and frequency-domain beamforming [10]. In this work, we used the time-domain technique, in which the signals are phase-shifted and summed to form a single beam. As this technique requires adjusting the phase of each of the radiant elements, phase shifters become essential components in active antennas [11].

Phase shifters can be passive or active depending on their components. As passive phase shifters are composed of passive elements, they are more lineal but cause higher signal attenuation. In turn, active phase shifters are composed of transistors so that they

can amplify while performing the phase shifting [12]. For a phase shifter operating in a transmission path, the linearity can be critical since the signal will be distorted before it reaches the antenna. In the case of the receiver path, the signal that reaches the antenna is very small, so a high gain amplification stage is necessary. Taking this into account, a digitally programmable phase shifter was designed.

As this work is focused on a receiver path of an antenna, an active topology was chosen. As shown in Figure 1, after each radiating element, there is a low-noise amplifier (LNA); the phase shifter then adds the desired phase shift to the signal; and, finally, there is a power combiner to mix the signals from different paths [12].

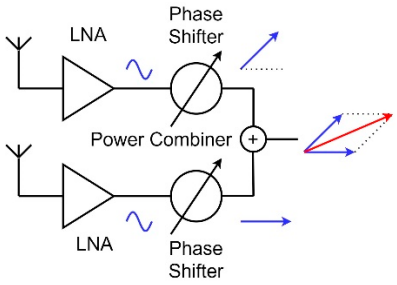

Figure 1. Receiver block diagram for two radiating elements. Directly after being amplified by an LNA, the desired phase shift is introduced into the signal. Subsequently, a power combiner combines the signals from different paths.

While continuous phase shifters can cover all incident angles without quantization errors, discrete phase shifters have the benefit of being digitally controlled [6,13]. However, this results in phase-quantization errors and pattern-direction errors. To diminish these errors, phase steps have to be small to minimize quantization errors. Using an N-bit phase shifter allows us to obtain phase shifts from 0° to 360° in steps of 360°/2N. Obviously, the higher the resolution in the phase shifter, the higher the accuracy on the beamforming. However, for many applications, a very high resolution is not necessary. We found in 5 bits a balance between enough resolution and design complexity, but it can be scaled to, e.g., 4 bits or 6 bits, according to different system requirements. For example, using a 4-bit phase shifter is sufficient for an 8-path phased array to cover all incident angles with signal loss less than 1 dB [14].

In [15], the conceptual idea and a preliminary design of only 4 bits (22.5°) with no extracted layout analysis was reported. In this work, we improved the resolution to 5 bits, which provides steps of 11.25°, and the bandwidth was adjusted from 17 GHz to 22 GHz, making it suitable for SATCOM-on-the-move communications [3], as a variety of commercial and military devices operate in this frequency band. The first results of a 5-bit phase shifter were advanced in a local PhD-student forum [16].

In [12,17,18], 4-bit phase shifters were designed for operation frequencies of 60 GHz, 20 GHz and 35 GHz, respectively. The phase RMS errors obtained in each of these works at their work frequency are 7° ([12]), 8° ([17]) and 1.5° ([18]). On the other hand, in [19,20], 5-bit phase shifters were designed with working frequencies of 27 GHz and 62 GHz, respectively. The obtained RMS phase errors at the work frequency are 2.5° in [19] and 4° in [20]. In [20], the designed phase shifter was passive, while in [19], it was active, with a power consumption of 17 mW.

In this work, a 5-bit phase shifter was designed to be used at 19.5 GHz. In Section 2, the proposed topology is described, whereas in Section 3, the main results obtained through a simulation are contained and discussed. Finally, the conclusions are drawn in Section 4.

2. Topology

The topology of the phase shifter proposed in this work consists of two processing blocks: a quadrature signal generator (QSG) and a variable gain amplifier (VGA), as

shown in Figure 2. Firstly, an in-phase (I) and a quadrature (Q) signal are generated in the quadrature signal generator (QSG). Then, each of these signals are weighted by two independent VGAs programmable by a 5-bit word.

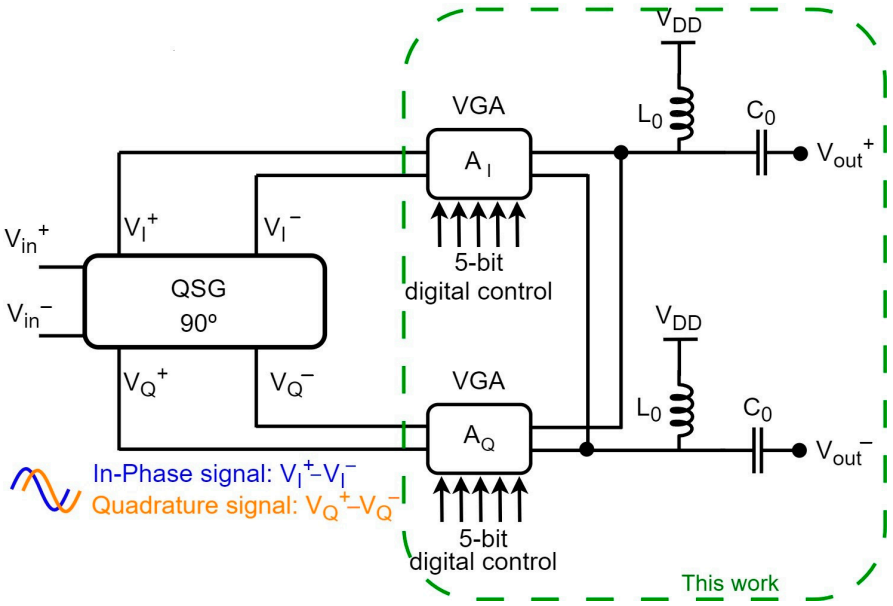

Figure 2. Block diagram of the phase shifter. V_I and V_Q denote, respectively, the in-phase and quadrature signals generated by the quadrature signal generator (QSG). Each of these signals is driven to two independent variable gain amplifiers (VGAs) whose gains (A_I y A_Q) are controlled by a 5-bit word.

Calling A_I the gain of the VGA that weighs the in-phase signal (I) ang and A_Q the gain of the VGA that weighs the quadrature signal (Q), the ideal phase shift, ϕ, obtained is given by the following calculation:

$$\phi = tan^{-1}\frac{A_Q}{A_I} \tag{1}$$

To generate a 5-bit phase shifter, the normalized gain of each VGA must vary from 1 to -1 in steps of $1/6$. Thus, from the ratio A_Q/A_I, the necessary phase shift can be obtained. With A_Q/A_I ratios of $0/6$, $1/6$, $2/6$, $3/5$, $4/4$, $5/3$, $6/2$, $6/1$, or $6/0$, the phase shift will vary from $0°$ to $90°$ in steps of approximately $11.25°$. To increase the range up to $360°$, the polarity of A_Q and A_I must be changed independently. As there are thirty-two different phase states, each of them with its own error, in this work, the root mean square (RMS) error is used to provide global information about the error of the system.

In practice, ideal phase shifts will not be exactly $11.25°$. For example, when introducing a phase shift of $11.25°$, a normalized gain of 1 is needed in the in-phase signal, while in the quadrature signal, the normalized gain must be $1/6$. Looking to Equation (1), it can be seen that the ideal phase shift is not $11.25°$; it is about $9.5°$. To obtain an exact value of $11.25°$, non-integer A_Q/A_I ratios are needed, and, consequently, it would be necessary to connect transistors in parallel with different dimensions, and this considerably complicates the design and layout. In consequence, the RMS error due to this structure is $2.6°$. Additionally, there are often gain and phase errors in the weighed in-phase and quadrature signals due to non-idealities and parasitic effects. These errors will be present on the output signal.

By modelling the gain and phase errors in the weighed I/Q signals as ε and α, respectively, one can obtain the equation for the RMS phase error (2) and the equation for the RMS gain error (3) [12].

$$\Delta\phi_{RMS} = \frac{\sqrt{2}}{4}\sqrt{3\alpha^2 + \varepsilon^2} \tag{2}$$

$$\Delta A_{RMS,\,dB} \cong 3.1\sqrt{\alpha^2 + 3\varepsilon^2} \quad (3)$$

It can be observed that the phase error mostly affects the final phase, and the gain error mostly affects the final gain.

Variable Gain Amplifier (VGA)

Figure 3 shows the topology of the 5-bit digitally programmable VGAs. As can be seen, they are formed by six stages of six NMOS transistors (M_A, M_B and M_C) and two stages of two NMOS transistors (M_D). Depending on which transistor is turned on, the desired portion of the current is steered to the output. The M_B transistors connect the positive input with the positive output and the negative input with the negative output, whereas the M_C ones invert the signal. The remaining transistors are dummies: the M_A transistors are the input dummy transistors, and the M_D ones are output dummy transistors, as they do not directly affect the signal operation. Thus, the ratio between the I/Q gains shown in (1) can be seen, in this case, as the number of pass transistors connecting the inputs and the outputs. Dummy transistors must be on the same operation point as the rest of the transistors; in this way, the source terminal of transistors D must be connected to a bias DC voltage, V_B, which is the same DC voltage that appears in V_{in}^+ and V_{in}^-.

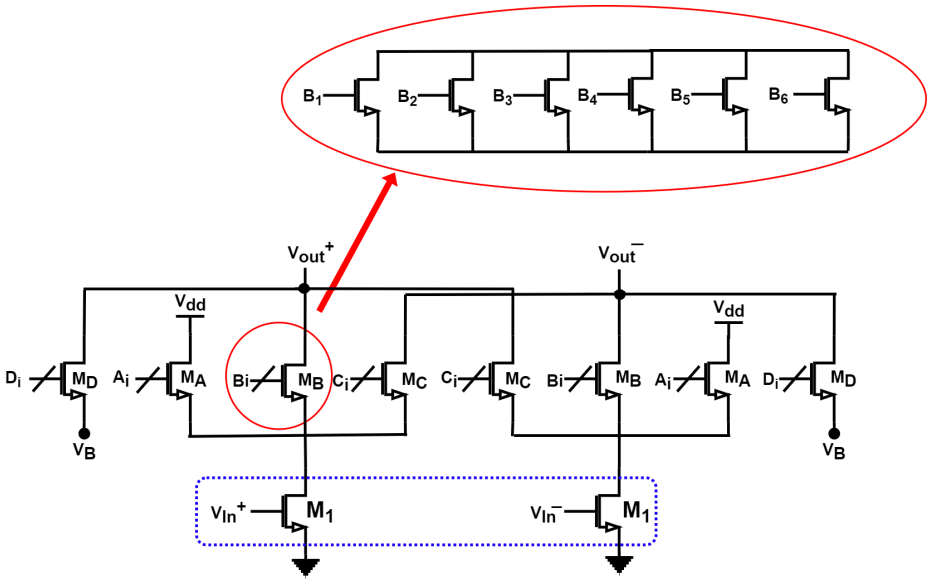

Figure 3. Topology of the VGA composed of common gate transistors (M_A, M_B, M_C and M_D) and the intermediate stage (marked with blue) composed of common source transistors (M_1). The M_A transistors are the input dummies, and the M_D transistors are the output dummies.

The maximum number of pass transistors connected to each differential input is set by the configurations in which the entire signal is allowed to pass through the input to the output, meaning the 0°, 90°, 180° and 270° phase-shift configurations. In these cases, one of the VGAs has six pass transistors (all M_B or M_C groups, depending on the configuration) connected to each differential input. For other phase shifts, we need to add dummy transistors to maintain the number of pass transistors connected to each input, keeping the input impedance constant. For example, for a 45° phase shift, the gain ratio must be 4/4; i.e., four transistors of each B group are required in each VGA, meaning that eight transistors are connected to each output but only four with each input, so, for this phase shift, two transistors of the M_A group are needed as well. If the desired phase shift is 11.25°, the gains ratio should be 1/6. In this case, each input of the in-phase VGA has connected six pass transistors, while the quadrature VGA has only one pass transistor connected. Therefore, there is no need to connect input dummies to the in-phase VGA,

whereas five input dummy transistors have to be connected to the input of the quadrature VGA. In turn, the total number of pass transistors connected to the output is seven, and therefore one output dummy transistor (M_D) is needed. Output dummies are needed in all the configurations in which the total number of pass transistors connected to the output is less than eight.

By keeping constant the total number of on transistors connected to the input and to the output, the input and output impedance variations between different configurations are reduced, and, consequently, the RMS phase and gain errors are as well.

3. Results and Discussion

An iterative approach was carried out, focusing on the following specifications: low RMS errors in phase and gain, low variations in output and input impedances between different configurations and low power consumption. The values chosen for the different elements of the circuit are as follows: L_0 = 260 pH (Q = 21.0 @ 19.5 GHz) and C_0 = 330 fF. The size of the VGA transistors is W/L = 2 µm/60 nm, while the size of the transistors that conform to the intermediate stage is W/L = 16 µm/60 nm. To achieve the desired polarization of the transistors, the DC voltage at the input has to be set to 800 mV, and V_B has to be 372 mV. Because the next stage after the phase shifter is a power combiner whose input impedance is capacitive (C_{gs} of a NMOS transistor), when the phase shifter and power combiner are integrated on-chip, it will not be necessary to include an output impedance-matching network. However, to measure the behavior of the phase shifter, it is necessary to adapt its output impedance to 50 Ω. Considering this, the output matching network shown in Figure 4 was used in the simulation, where C_A = 180 fF, C_B = 70 fF and L_C = 675 pH (Q = 11.2 @ 19.5 GHz).

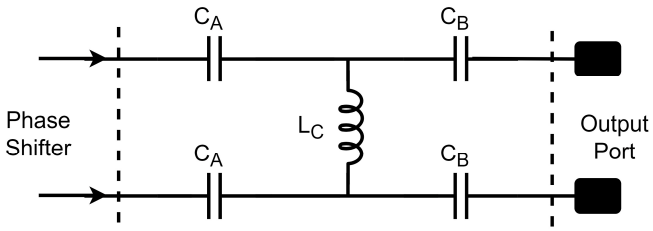

Figure 4. Output matching network topology, where C_A = 180 fF, C_B = 70 fF and L_C = 675 pH (Q = 11.2 @ 19.5 GHz).

Figure 5 shows the layout of the beamformer core, which occupies an active area of 0.1 mm^2. It can be seen that the more critical elements for the occupied area are the inductors, followed by the capacitors. It was very important to maintain the symmetry between the I/Q paths in order to avoid errors due to signal-imbalance effects. The design was laid out and simulated using the TSMC 65 nm CMOS Process Design Kit (PDK).

Figure 6 shows the phase shifts obtained for a frequency of 19.5 GHz, taking as a reference the phase of the configuration 00000. As can be seen, by combining the weighted in-phase and quadrature signals, the desired phase shift is obtained for each configuration with a practically constant gain. At this frequency, we obtained a 4.5° RMS phase error and a 0.79 dB RMS gain error.

These phase shifts were verified in a frequency range from 17 GHz to 22 GHz, and the results can be seen in Figure 7 for the RMS gain and phase error in this frequency range. It can be seen how the phase steps are maintained in the whole frequency range with a phase RMS error lower than 7° and a gain RMS error lower than 0.90 dB. Having a resolution of 5 bits means that we can tolerate an RMS phase error lower than 5.6° (half of the phase step). That happens for frequencies higher than 18 GHz.

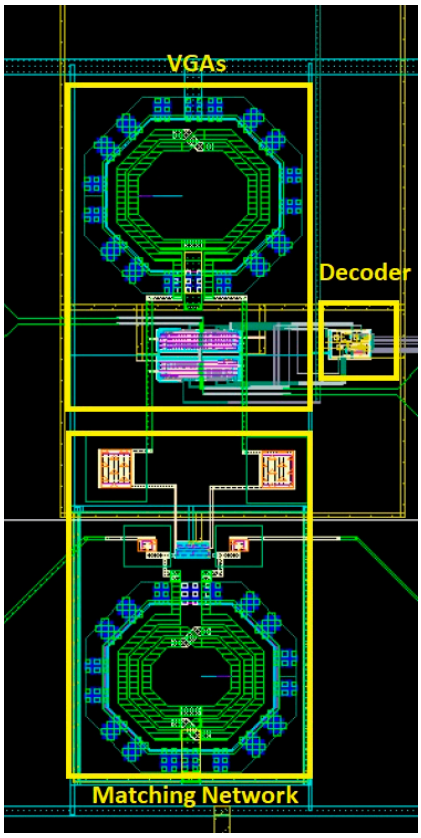

Figure 5. Layout of the beamformer core with indication of the main parts described in this work. The full system comprises a digital decoder stage that is not described in this work but is necessary to change between the different configurations.

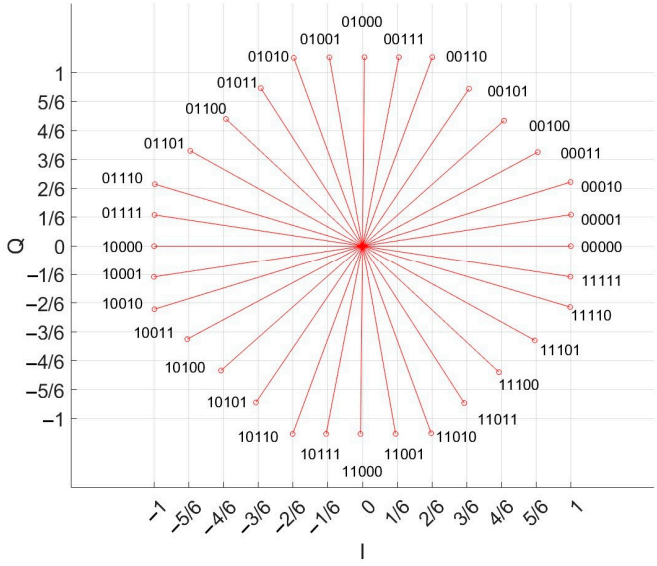

Figure 6. Constellation diagram of the different phase steps from 0° (00000) to 348.75° (11111), in steps of 11.25°, at the center frequency, 19.5 GHz.

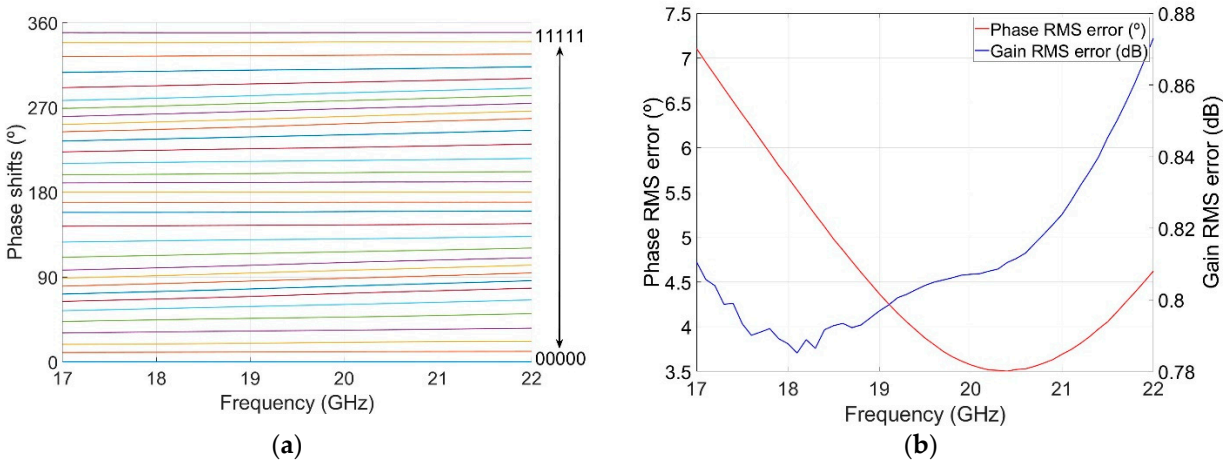

Figure 7. (**a**) Phase shifts from 17 GHz to 22 GHz, taking as reference the phase of the 00000 configuration, each line corresponds to each of the different phase shifts from 00000 to 11111; (**b**) gain (blue) and phase (red) root mean square errors.

For this application, we can tolerate these errors [21]. However, they can be reduced if the application requires it. One possibility for reducing these phase and amplitude errors could be to look for a more symmetric layout design, since the performance of the design is very sensitive to mismatch on the paths for the I/Q signals. In Figure 5, it can be seen that we created a symmetric design. However, in Figure 6, it can be seen that there are still some differences between the I/Q paths. In an ideal design, the y-coordinate of points from 00110 to 01010 and from 10110 to 11010 should be 1, and it can be seen that is somewhat higher. This means that the amplitude of the quadrature signal is bigger than the amplitude of the in-phase signal. By diminishing this error, the RMS errors for amplitude and phase will decrease too.

The input and output impedance adaptation to 50 Ω were evaluated by using the S-parameters. The obtained results for parameters S_{21}, S_{11} and S_{22} are summarized in Figure 8. The reflection coefficient, S_{11}, is lower than −10 dB in the whole frequency range, resulting in a good input impedance matching. For S_{22}, the result is lower than −8 dB from 17 GHz to 22 GHz. It can be seen that the power gain has a maximum of −6 dB at the work frequency, with an RMS maximum error of 0.78 dB. As the main performance of this work was to obtain the desired phase shifts with a low RMS error (less than 50% of the phase step), we prioritized this to have a high gain. With the proposed topology, we saw that when we were looking for a higher gain, the RMS phase error increased too. In this work, we tested our idea in the frequency band from 17 GHz to 22 GHz. In order to improve the S_{22} result, the output matching network must be adjusted to the specific frequency band for the desired application. In this work, we adjusted it to the central frequency, 19.5 GHz. This is the reason why, at the lower and higher frequencies of the tested band, the return losses increase.

We also obtained the linearity and the power consumption. At the work frequency, the average of the 1 dB compression point is −0.56 dBm ± 0.33 dBm. For the power consumption, the average between the different configurations at 19.5 GHz is 9.78 mW.

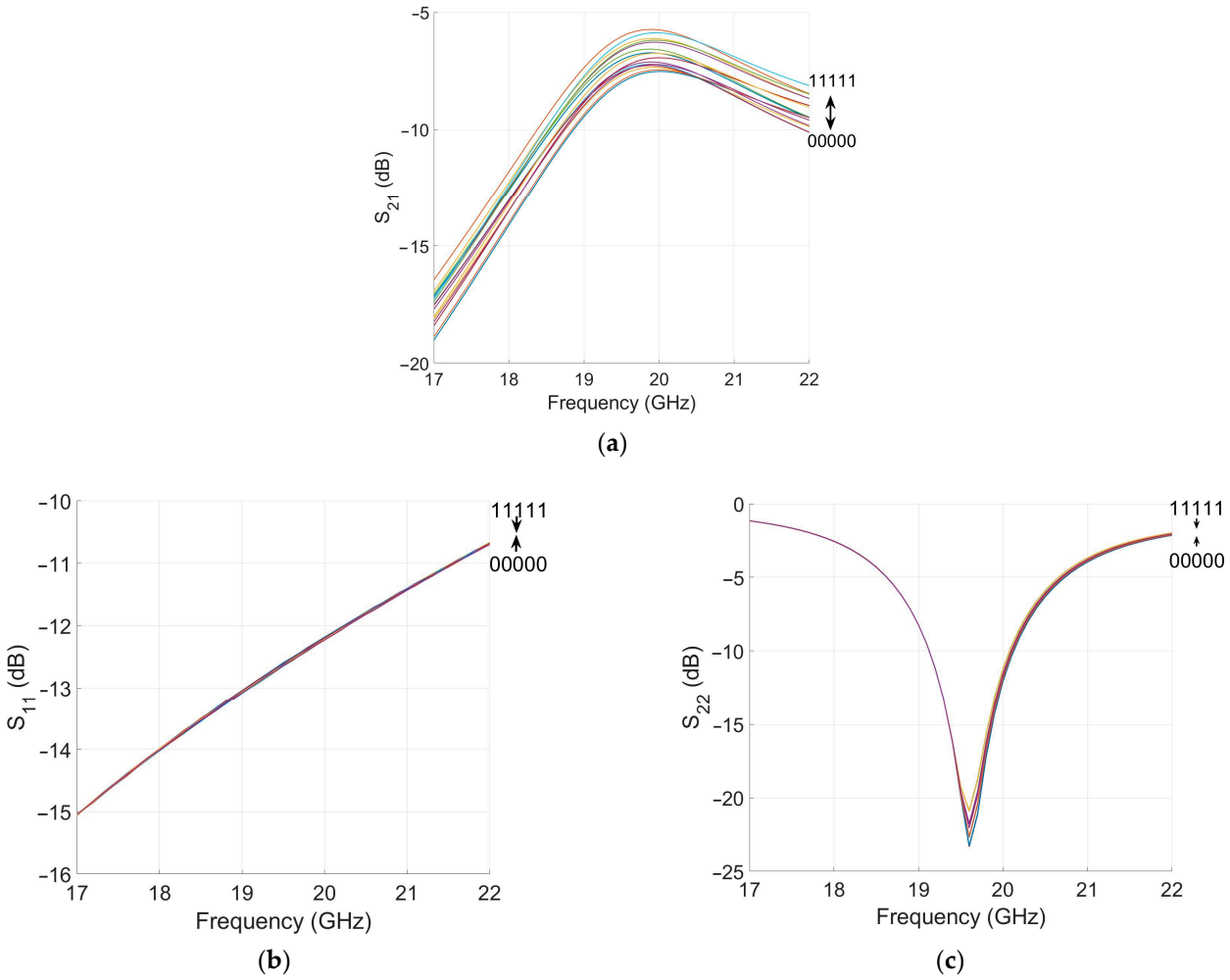

Figure 8. Scattering parameters from 17 GHz to 22 GHz for each of the phase shifts. (**a**) Power gain for each configuration, S_{21}; (**b**) input power reflection coefficient, S_{11}; and (**c**) output power reflection coefficient, S_{22}.

Table 1 offers a comparison of these results with the results obtained in competitive phase-shifter realizations of [12,17–20]. As can be seen, the results obtained are of the order of those obtained in these references but, in this case, for a lower power consumption than the other active phase shifters. Even though the designed phase shifter has a resolution of 5 bits, we include 4-bit designs in the table too, because they use similar parameters that we can use to compare them. As the maximum phase error tolerable is a half of the phase step, the lower the resolution, the higher the RMS error allowed. Considering this, we decided to include in the comparison table information about the RMS error relative to the phase step at the center frequency. It can be seen that the best relative error was obtained in [18], with just a 7% of error at their span center frequency, but it is at the expense of power consumption. Keep in mind that the maximum tolerable error is 50%. It can be seen that all the works cited in the table have a lower error at their work frequency.

Although the references compared in Table 1 work in very different frequency ranges and higher frequencies require higher power consumption, we can compare the power consumption of our work with those active phase shifters that operate in close frequencies. If we consider the power/frequency ratio in References [17–19], the lower ratio is 0.5 mW/GHz, which was obtained for Reference [17]. In our work, we also obtained 0.5 mW/GHz, so we can conclude that the phase shifts were successfully maintained over a wider range and with low power consumption.

Table 1. Comparison with other reported phase shifters.

	Freq. (GHz)/ Resolution	Technology (nm)/Supply (V)	$\Delta\phi_{RMS}$ (°) /RMS rel. Error (%)	ΔA_{RMS} (dB)	S_{11} (dB)	S_{22} (dB)	Input P1dB (dBm)	Power (mW)
This work	17–22/ 5 bits	CMOS (65)/ 1.2	3.5–7.1/ 40 (@19.5 GHz)	0.78–0.87	<−10.7 @17–22 GHz	<−8 @17–22 GHz	−0.5 ± 0.3 @19.5 GHz	9.78 @19.5 GHz
[12] * 2011	50–68/ 4 bits	CMOS (65)/ 1.5	4–12/ 31 (@60 GHz)	0.8–1.0	<−10 @ 59–67 GHz	<−5 @57–64 GHz	−9 @60 GHz	78 @60 GHz
[17] 2007	15–26/ 4 bits	CMOS (130)/ 1.5	6.5–13/ 36 (@21 GHz)	<2.1	<−10 @16.8–26 GHz	<−10 @17–26 GHz	−0.8 ± 1.1 @24 GHz	11.7 @24 GHz
[18] 2022	32.5–36.5/ 4 bits	CMOS (28)/ 1.8	<12/ 7 (@35 GHz)	<3.5	<−6 @32.5–36.5 GHz	<−5 @32.5–36.5 GHz	-	27
[19] 2019	24–30/ 5 bits	CMOS (90)/ 1.8	<4/ 22 (@27 GHz)	<0.6	<−9 @20–45 GHz	-	>−2.8 @24–30 GHz	17.5 @24–30 GHz
[20] 2016	57–66/ 5 bits	CMOS (65)/ (Passive)	<8/ 36 (@62 GHz)	<0.23	<−8.2 @57–66 GHz	<−8.2 @57–66 GHz	13	(Passive)

* Results given with LNA and a combiner.

4. Conclusions

This paper presents the design and post-layout verification of a 5-bit digitally programmable variable gain amplifier (VGA) used to independently weigh the in-phase signal.

In the design presented in this work, a new design technique using a set of dummy transistors was implemented to keep the input and output impedance almost constant between different configurations, allowing for an improvement in its performance by minimizing the errors in the amplitude and phase of the I/Q signal. Dummy transistors contribute to the impedance matching with the previous and the next stages of the receiver path, since the number of turned-on transistors connected with each input and out is maintained constant.

The proposed system was laid out, and post-layout simulations show that it is possible to obtain phase shifts in the full range, from 0° to 360°, in even steps of 11.25°, with a phase RMS error of 4.5° and a gain RMS error of 0.79 dB at the target frequency of 19.5 GHz. We also verified that the phase states remain practically constant in a frequency range from 18 GHz to 22 GHz, while the input and output impedances are kept invariant, as well.

The results were compared with those of recently published programmable phase shifters. As for a higher resolution, the phase RMS errors that are permissible are smaller, and we obtained the root mean square error relative to the phase step at the central frequency for each work. Regarding the power consumption, our work was compared with those in a similar frequency range, because higher frequencies require higher power consumption. For the comparison, the power/frequency ratio was considered. Comparing it with the works of References [17–19], we can conclude that the designed phase shifter can shift the phase in a range of 360° in discrete steps of 11.25°, with low RMS errors in phase and amplitude, and also a low power consumption.

Author Contributions: Circuit design, U.E.E., C.S.-A., C.A. and S.C.; simulations, U.E.E.; writing—original draft preparation, U.E.E.; writing—review and editing, C.S.-A., C.A. and S.C.; supervision, C.S.-A., C.A. and S.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work is part of research projects supported by the Spanish State Research Agency (RTC2019-007039-7, PID2020-114110RA-I00) and the Aragón Regional Government (LMP106_21).

Data Availability Statement: The data that support this study are available from the corresponding author, U.E.E., upon reasonable request.

Conflicts of Interest: The authors declare no conflict of interest.

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