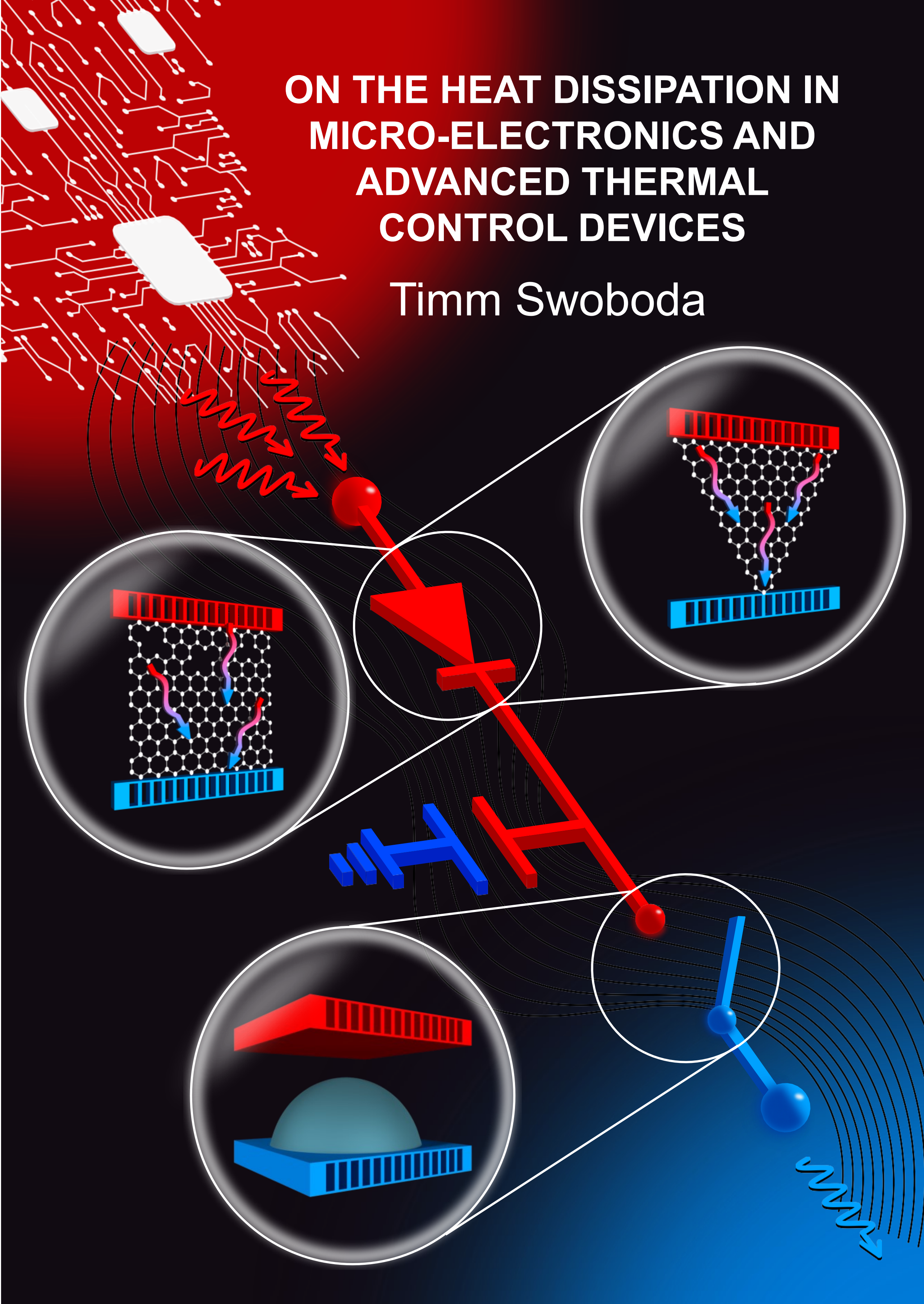
ON THE HEAT DISSIPATION IN MICRO-ELECTRONICS AND ADVANCED THERMAL CONTROL DEVICES
Timm Swoboda

ON THE HEAT DISSIPATION IN MICRO-ELECTRONICS AND ADVANCED THERMAL CONTROL DEVICES

Timm Philipp Erik Swoboda

ON THE HEAT DISSIPATION IN MICRO-ELECTRONICS AND ADVANCED THERMAL CONTROL DEVICES

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. ir. A. Veldkamp,
on account of the decision of the Doctorate Board
to be publicly defended
on Monday 25 September 2023 at 14.45 hours

by

Timm Philipp Erik Swoboda

born on the 18th of July, 1994
in Frankfurt am Main, Germany

This dissertation has been approved by:

Supervisors

prof. dr. ir. G. Brem
prof. dr. M. Muñoz Rojo

The presented research was funded by and carried out in the Thermal and Fluid Engineering group, Faculty of Engineering Technology, University of Twente, The Netherlands.

Cover design: Timm Swoboda, partially linked to the following article:

T. Swoboda, K. Klinar, A. S. Yalamarthy, A.Kitanovski and M. Muñoz Rojo, Adv. Electron. Mater., 2020, 7, 2000625.

Link: https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.202170008

Printed by: Ipskamp printing

ISBN (print): 978-90-365-5773-3

ISBN (digital): 978-90-365-5774-0

URL: https://doi.org/10.3990/1.9789036557740

© 2023 Timm Philipp Erik Swoboda, The Netherlands. All rights reserved. No parts of this thesis may be reproduced, stored in a retrieval system or transmitted in any form or by any means without permission of the author. Alle rechten voorbehouden. Niets uit deze uitgave mag worden vermenigvuldigd, in enige vorm of op enige wijze, zonder voorafgaande schriftelijke toestemming van de auteur.

Graduation Committee:

Chair / secretary:	prof.dr.ir. H.F.J.M. Koopman
Supervisors:	prof.dr.ir. G. Brem Universiteit Twente, ET, Thermal Engineering prof. dr. M. Muñoz Rojo Spanish National Research Council (CSIC), Instituto de Ciencia de Materiales de Madrid (ICMM)
Committee Members:	prof. dr. A. Kitanovski University of Ljubljana, Faculty of Mechanical Engineering prof. dr. ir. H. Hilgenkamp University of Twente, TNW prof. dr. J.B. Roldán University of Granada, Electronics and Computer Technology Department prof.dr.ir. W. Rohlfs Universiteit Twente, ET, Department of Thermal and Fluid Engineering dr. K.M. Dowling TU Delft, Faculteit Elektrotechniek, Wiskunde & Infomatica dr. ir. W.W. Wits Multiscale Modeling & Simulation group at EEMCS, UTwente Mechanical & Electrical Engineering department at Thales Nederland B.V.

This thesis is dedicated to Hans, Renate, Maria, Josef, Fabian, Erik and Anita.

It is the job that is never started as takes longest to finish.

Samwise Gamgee

Summary

Future and current technologies aim for the improvement of our energy conservation, conversion and harvesting capabilities. Heat, as a form of energy, is essential to generate electricity in thermodynamic processes but it is also behind the limited efficiency or performance of some technology. For example, heat is a limiting factor for the performance of our electronic devices or low grade waste heat is the major source of losses in multiple thermodynamic processes.

This thesis addresses aspects around the concept of heat in two different domains. On the one hand, fundamental understanding of heat dissipation and its impact on the operation of nanostructured electronic devices is studied. For the characterization of the heat dissipation, I calibrate and use a scanning thermal microscope (SThM). On the other hand, a novel thermal diode design is developed by means of finite element modelling to obtain modulated heat rectification factors beyond the start of the art. Based on this design, I propose to integrate this diode in heat storage tanks to improve our energy management and storage capabilities.

As the power density of electronics increases with device size reduction, heat dissipation has become a growing concern in modern electronic design. Electronic devices in operation generate Joule heating, which can negatively impact device performance, cause thermal stresses, and eventual failure due to overheating. Therefore, efficient heat dissipation is key to improve the energy efficiency in modern electronics.

The characterization of heat dissipation of electronic devices is very challenging due to the nano- or micro-scale size of the devices and eventual non-uniformity and local nature of the heating features. Optical-based techniques, such as Raman thermometry or infrared scopes, are diffraction limited, meaning that their spatial resolution is not enough to characterize nanoscale heating features. Scanning thermal microscopy presents nanoscale spatial resolution and it has emerged as a promising tool for studying local heating features of devices. However, the calibration of the SThM for quantitative temperature analysis is one of the most challenging aspects of this approach due to complex thermal exchange processes between the tip and the surface. Calibrated SThM systems have been employed to study the heat dissipation in multiple electronic devices,

including filamentary based memory devices like resistive random access memories (RRAM).

RRAM devices are based on the formation and rupture of nanoscale confined conductive filaments (CF) with high power densities. The capabilities of these devices make them specially interesting for neuromorphic computing. Several theoretical and experimental studies have been carried out to determine the electrical switching capabilities of RRAMs, but little information is known about their heating features. SThM is a powerful tool to be employed for studying the hot spots that are generated at the surface of RRAMs when CFs are formed. The characterization of these heating features provides a better fundamental understanding of the electro-thermal mechanism that affects RRAM´s operation.

The experimental focus of this thesis is on the thermal characterization of metal-oxide RRAMs. Particularly, titanium-oxide (TiO_2) RRAMs are studied with a calibrated scanning thermal microscope (SThM) to quantify the effect of heat generation of CF in operation. These measurements aim to provide deep insights on the electro-thermal switching mechanism of RRAM devices and how it affects their performance variability. Such fundamental information is crucial for the effective thermal design and management of such devices.

First, a calibration method to investigate the impact of the probe-sample thermal exchange processes based on the characterization of metal lines of different widths is performed. The calibration allows converting the electrical response of thermo-resistive probes into temperature and takes into account variable probe-sample thermal exchange processes.

Second, the SThM measurements on the investigated RRAM devices reveal a correlation of the heat dissipation with its electrical characteristics. In this context, the results indicate that a shift of the filament position within the device area correlates with a significant source of performance variability. The shift of the hot spot position appears in devices with larger area sizes. The results offer the possibility to develop electro-thermal models of filaments that do not only rely only on electrical data but also in thermal data. This will advance our fundamental knowledge of RRAMs and it could favor the design of more reliable devices.

Regarding advanced thermal management, solid-state thermal control devices have emerged as potential candidates for heat management in electronics and beyond e.g., energy conversion or storage systems. They distinguish themselves from traditional passive thermal management

devices in that they possess a sharp non-linear relation in their heat transfer characteristics which can be modulated by the heat flow direction or the operating temperature. As a promising example, thermal diodes present an asymmetrical heat flow depending on the temperature gradient direction. This feature makes them interesting for application in a vast field of heat related subjects ranging from thermoelectric and nanoelectronics to heat storage systems. Nonetheless the application of thermal diodes is still limited by the moderate rectification ratios of current device designs.

This thesis also focusses on the design and application of solid-state thermal diodes as advanced heat control devices. For that purpose, a finite element method (FEM) model of a novel solid-state thermal diode design that presents state-of-the-art rectification ratios is developed. In the context of this study the rectification ratio of two novel thermal diode designs based on the combination of multiple phase change material (PCM) layers are analyzed. The two structures display rectification ratios ranging from 96 to 133 % for temperature differences of up to 250 K in between the heat terminals at around room temperature conditions. These values are 50-80 % higher than other studied PCM thermal diodes. Moreover, the existence of multiple layers of PCMs and phase invariant materials (PIMs) allows better control of the temperature gradients across materials. This facilitates modulation of the rectification factor depending on the gradient of temperature. Finally, an analytical study shows that these thermal diodes can be implemented in thermal storage elements to increase their heat retention up to 17 %. Overall, these thermal diodes represent new opportunities for efficient energy management.

Samenvatting

Toekomstige en huidige technologieën zijn gericht op de verbetering van onze mogelijkheden om energie te behouden, om te zetten en te verkrijgen. Warmte, als een vorm van energie, is essentieel om elektriciteit op te wekken in thermodynamische processen, maar het is ook de oorzaak van de beperkte efficiëntie of prestaties van sommige technologieën. Warmte is bijvoorbeeld een beperkende factor voor de prestaties van onze elektronische apparaten of laagwaardige afvalwarmte is de belangrijkste bron van verliezen in meerdere thermodynamische processen.

Deze dissertatie behandelt aspecten rondom het concept warmte in twee verschillende domeinen. Aan de ene kant wordt fundamenteel begrip van warmteafvoer en de invloed ervan op de werking van nano elektronische apparaten bestudeerd. Voor de karakterisering van de warmtedissipatie kalibreer en gebruik ik een zogeheten scanning thermal microscope (SThM). Aan de andere kant wordt een nieuw ontwerp van een thermisch diode ontwikkeld door middel van een eindige-elementenmethode (FEM) om gemoduleerde warmte-rectificatie factoren te verkrijgen die verder gaan dan de nieuwste technieken. Op basis van dit ontwerp stel ik voor om deze diode te integreren in warmteopslagtanks om ons energiebeheer en onze opslagmogelijkheden te verbeteren.

Omdat de vermogensdichtheid van elektronica toeneemt naarmate de apparaten kleiner worden, is warmteafvoer een steeds groter probleem geworden in het moderne elektronische ontwerp. Elektronische apparaten genereren Joule-warmte, wat de prestaties van het apparaat negatief kan beïnvloeden, thermische spanningen kan veroorzaken en uiteindelijk defecten kan veroorzaken door oververhitting. Daarom is efficiënte warmteafvoer essentieel om de energie-efficiëntie van moderne elektronica te verbeteren.

Het karakteriseren van de warmteafvoer van elektronische apparaten is een grote uitdaging vanwege de nano- of micro grootte van de apparaten en de eventuele niet-uniformiteit en lokale aard van de verwarmingseigenschappen. Optische technieken, zoals een Raman thermometrie of een infraroodcamera, zijn buigingsbegrensd, wat betekent dat hun ruimtelijke resolutie niet voldoende is om verwarmingseigenschappen op nanoschaal te karakteriseren. SThM biedt een ruimtelijke resolutie op nanoschaal en is een veelbelovend hulpmiddel geworden voor het bestuderen van lokale verwarmingseigenschappen van

apparaten. De kalibratie van de SThM voor kwantitatieve temperatuuranalyse is echter een van de meest uitdagende aspecten van deze techniek vanwege de complexe thermische uitwisselingsprocessen tussen de tip en het oppervlak. Gekalibreerde SThM-systemen zijn gebruikt om de warmtedissipatie in verschillende elektronische apparaten te bestuderen, waaronder op filamenten-gebaseerde geheugenapparaten zoals het zogeheten resistive random access memory (RRAM).

RRAM-apparaten zijn gebaseerd op de vorming en breuk van op nanoschaal ruimtelijk begrensde conductieve filamenten (CF) met hoge vermogensdichtheden. De mogelijkheden die deze apparaten bieden maken ze speciaal interessant voor neuromorfische computersystemen. Er zijn verschillende theoretische en experimentele studies uitgevoerd om de elektrische schakelmogelijkheden van RRAMs te bepalen, maar er is weinig informatie bekend over hun verwarmingseigenschappen. SThM is een krachtig hulpmiddel om de hotspots te bestuderen die ontstaan aan het oppervlak van RRAMs wanneer CFs worden gevormd. De karakterisering van deze verwarmingseigenschappen zorgt voor een beter fundamenteel begrip van het elektrothermische mechanisme dat de werking van RRAMs beïnvloedt.

De experimentele focus van deze dissertatie ligt op de thermische karakterisering van metaaloxide RRAMs. Specifiek, titanium-oxide (TiO_2) RRAMs worden bestudeerd met een gekalibreerde SThM om het effect van warmtedissipatie van CF tijdens operatie te kwantificeren. Het doel van deze metingen is om beter inzicht te verkrijgen in het elektrothermische schakelmechanisme van RRAM-apparaten en hoe dit de variabiliteit van hun prestaties beïnvloedt. Dergelijke fundamentele informatie is cruciaal voor een effectief thermisch ontwerp en beheer van dergelijke apparaten.

In eerste instantie wordt een kalibratiemethode uitgevoerd om de invloed van de thermische uitwisselingsprocessen tussen sonde en monster te onderzoeken, gebaseerd op de karakterisering van metaallijnen van verschillende breedtes. De kalibratie maakt het mogelijk om de elektrische respons van sondes met thermoweerstand om te zetten in temperatuur waarbij rekening gehouden wordt met variabele thermische uitwisselingsprocessen tussen de sonde en het monster.

Ten tweede onthullen de SThM-metingen aan de onderzochte RRAM-apparaten een correlatie tussen de warmtedissipatie en de elektrische karakteristieken. In deze context geven de resultaten aan dat een verschuiving van de positie van de CF binnen het RRAM-gebied correleert

met een significante bron van prestatievariabiliteit. De verschuiving van de hotspotpositie treedt op in apparaten met een groter oppervlak. De resultaten bieden de mogelijkheid om elektrothermische modellen van CFs te ontwikkelen die niet alleen gebaseerd zijn op elektrische gegevens, maar ook op thermische gegevens. Dit zal onze fundamentele kennis van RRAMs vergroten en kan het ontwerp van betrouwbaardere apparaten bevorderen.

Met betrekking tot geavanceerd thermisch management, zijn solid-state thermisch controleapparaten gekomen als potentiële kandidaten voor warmtemanagement in elektronica en daarbuiten, bijvoorbeeld energieomzettings- of opslagsystemen. Ze onderscheiden zich van traditionele passieve apparaten voor thermisch management doordat ze een scherpe niet-lineaire relatie hebben in hun warmteoverdrachtskarakteristieken die gemoduleerd kunnen worden door de richting van de warmtestroom of de bedrijfstemperatuur. Een veelbelovend voorbeeld zijn thermische dioden met een asymmetrische warmtestroom afhankelijk van de richting van de temperatuurgradiënt. Deze eigenschap maakt ze interessant voor toepassing in een breed gebied van warmtegerelateerde toepassingen, variërend van thermo-elektrische en nano-elektronica tot warmteopslagsystemen. Toch is de toepassing van thermische dioden nog steeds beperkt door de geringe rectificatie ratios (RR) van de huidige apparaten.

Deze dissertatie richt zich ook op het ontwerp en de toepassing van solid-state thermische dioden als geavanceerde apparaten voor warmteregeling. Voor dat doel is een eindige-elementenmethode ontwikkeld van een nieuw ontwerp van een solid-state thermische diode met de hoog RR. In het kader van deze studie wordt de RR van twee nieuwe thermische dioden ontwerpen geanalyseerd die gebaseerd zijn op de combinatie van meerdere lagen van fase-veranderbare materialen (PCMs). De twee structuren vertonen een RR van 96 tot 133 % voor temperatuurverschillen tot 250 K tussen de warmtebron en warmteput bij kamertemperatuur. Deze waarden zijn 50-80% hoger dan andere bestudeerde PCM thermische dioden. Bovendien maakt het bestaan van meerdere lagen PCMs en fase-onveranderbare materialen (PIMs) een betere controle van de temperatuurgradiënten over de materialen mogelijk. Dit maakt modulatie van de RR afhankelijk van de temperatuurgradiënt mogelijk. Tot slot toonde een analytische studie aan dat deze thermische dioden geïmplementeerd kunnen worden in elementen voor thermische opslag om hun warmtebehoud tot 17 % te verhogen. In het algemeen bieden deze thermische dioden nieuwe mogelijkheden voor efficiënt energiebeheer.

Table of contents

Summary i

Samenvatting iv

Table of contents vii

Chapter 1 Introduction 1

1.1 Energy dissipation in electronics.. 4

1.1.1 RRAM device fabrication 6

1.1.2 RRAM operation principle 7

1.1.3 Electrical performance in RRAM 8

1.1.4 Limitations and potential sources of device failure 10

1.2 Thermal characterization of RRAM devices 11

1.2.1 Operation principle of SThM.. 12

1.2.2 SThM calibration approaches for sensing nanoscale heating features.. 14

1.2.3 RRAM filamentary hot spot characterization with SThM............ 14

1.3 Thermal control devices for advanced thermal management........... 16

1.3.1 Operation of thermal diodes 17

1.3.2 Introduction to two-segment thermal diodes.............................. 18

1.3.3 Junction of materials with different thermal properties (JMT)..... 18

1.3.4 Phase change material (PCM) thermal diodes 21

1.4 Scope of this thesis 25

1.5 Research questions and lines... 26

1.6 Thesis organization 27

1.7 Research contributions... 28

1.8 Introduction references... 30

Chapter 2 Nanoscale temperature sensing of electronic devices with calibrated scanning thermal microscopy 37

2.1 Introduction.. 38

2.2 Experimental setup 40
2.2.1 Fabrication of the calibration sample 40
2.2.2 Atomic force microscopy (AFM) analysis of the topography of the lines 42
2.2.3 Electrical characterization of the lines 42
2.2.4 Operation of the SThM calibration 44
2.2.5 COMSOL simulation for characterization of the temperature increase 46
2.2.6 Estimation of the probe power during the measurement 48
2.2.7 Estimation of the temperature of the probe utilizing null-point method (NPM) measurements 49
2.3 Results 52
2.3.1 Estimation of the *CaF* 52
2.3.2 Comparison of the results with a second probe 53
2.3.3 Calibration factor at high power 55
2.4 Discussion and SThM application to measure electronic devices 55
2.4.1 Validation of calibration 56
2.5 Conclusions 57
2.6 References 58
2.7 Appendix 60
2.7.1 SThM measurements 60
2.7.2 Conversion of SThM signal into temperature signal 61
Chapter 3 Spatially resolved thermometry of filamentary nanoscale hot spots in TiO_2 resistive random access memory devices 63
3.1 Introduction 64
3.2 Experimental setup 65
3.2.1 Synthesis of the RRAM device structure 65
3.2.2 Characterization of the current-voltage characteristics 67
3.2.3 Device-to-device and cycle-to-cycle variability 68
3.2.4 Thermal characterization with SThM 69

3.2.5 Conversion of SThM electrical signal into temperature..............70
3.3 Results 72
3.3.1 Steady state measurements..72
3.3.2 COMSOL model for the characterization of the filament temperature 76
3.3.3 Estimation of the hot spot characteristics 78
3.3.4 In-operando SThM measurements at the hot spot 80
3.3.5 Steady state characterization after cycling 81
3.4 Discussion 82
3.4.1 Influence of the area size 83
3.4.2 Characterization of the line resistance.......................................83
3.4.3 STEM characterization of the layer structure in pristine and cycled devices 85
3.5 Conclusions...87
3.6 References..88
3.7 Appendix 90
3.7.1 Electrical characterization in RRAM 90
3.7.2 Hot spot location with cycling 92
3.7.3 Simulation characteristics..93
Chapter 4 Thermal rectification in multilayer phase change material structures for energy storage applications 95
4.1 Introduction...96
4.2 Modelling approach 99
4.2.1 Geometry 99
4.2.2 Material selection 100
4.2.3 Heat transfer model...102
4.2.4 Mesh 104
4.2.5 Study 105
4.3 Results 106
4.3.1 Rectification ratio of 2- & 3- PCM/PIM multilayers at a constant thermal bias 106

4.3.2 *RR* of 2- & 3-PCM/PIM multilayers vs heat source temperature 108
4.3.3 Calculation of thermal conductivity vs heat source temperature 110
4.3.4 Validation 111
4.3.5 Influence of geometry, interfaces and number of layers in thermal rectification of PCM/PIM diodes 112
4.4 Discussion on thermal diode applications 115
4.4.1 Application design 115
4.4.2 Analytical model 116
4.4.3 Calculation heat losses 120
4.4.4 Cycling of thermal storage system 121
4.4.5 Integration of thermal contacts 122
4.5 Conclusion and prospects 123
4.6 References 124
4.7 Appendix 126
4.7.1 Verification heat losses 126
Chapter 5 Conclusion and future perspectives 127
5.1 Characterization of electro-thermal switching in metal-oxide RRAMs with SThM 127
5.2 Development of a novel solid-state thermal diode and evaluation of its potential for advanced heat control 129
5.3 Recommendations & outlook 130
List of publications 132
Acknowledgments 135

Chapter 1 Introduction

Chapter 1.3 is derived from the publication:

T. Swoboda, K. Klinar, A. S. Yalamarthy, A. Kitanovski and M. Muñoz Rojo, Adv. Electron. Mater., 2020, 7, 2000625.

Energy consumption, dissipation and waste are behind some key challenges of our modern society. Heat, as a form of energy, plays an essential role in many applications, such as thermodynamic processes or heat storage. On the other hand, heat could also limit the efficiency and performance of some technologies, such as electronics. As an example, data centers consume enormous amount of energy that is used for example in servers or networks. However, a major part of the energy input in data centers is dedicated to cool down their electronic racks. As shown in Fig. 1.1 roughly 40 % of the whole energy consumption in data centers is related to cooling purposes (e.g., air conditioning).[1,2] From an energy consumption point of view this is especially relevant as the combined electricity consumption of data centers in the world (220-320 TWh) was approximately twice as high as the total electricity consumption of the Netherlands (116 TWh) in 2020.[3]

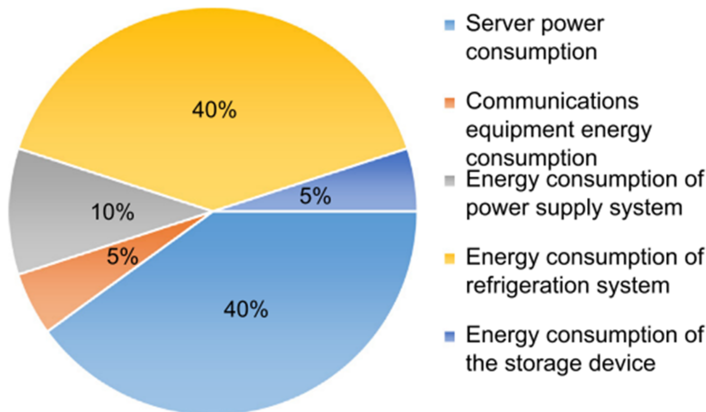

Figure 1.1 Energy consumption distribution of data centers Adapted with permission from Rong *et al.*[2]

In the coming years the demand for data network services is expected to increase even further due to data intensive activities like video streaming, augmented reality or more currently crypto mining.[4] In that context the data volume of the global internet traffic increased by 440 % from 2015 to 2021[4] and the cooling demands are becoming more drastic.[5,6] This has made companies like Google or apple to move their data centers to cold places like northern Europe, where they can take advantage of the environment to cool down electronics more efficiently.[6]

The heat generated in data centers comes primarily from electronic devices that heat up due to Joule heating effects.[6] On the one hand, efficient management of this heat is necessary to avoid malfunctioning or damage of the electronics racks.[7] On the other hand, gaining more insights about how heat dissipates in individual electronic devices, like nanoscale transistors or memories, can favor the development of more efficient electronic architectures. These new electronics will avoid unpleasant effects, like reduction of device performance, thermal stresses, thermal crosstalk or eventual failure due to overheating.[8–10] Therefore, heat dissipation at different scales is behind the core of the energy efficiency of data centers.

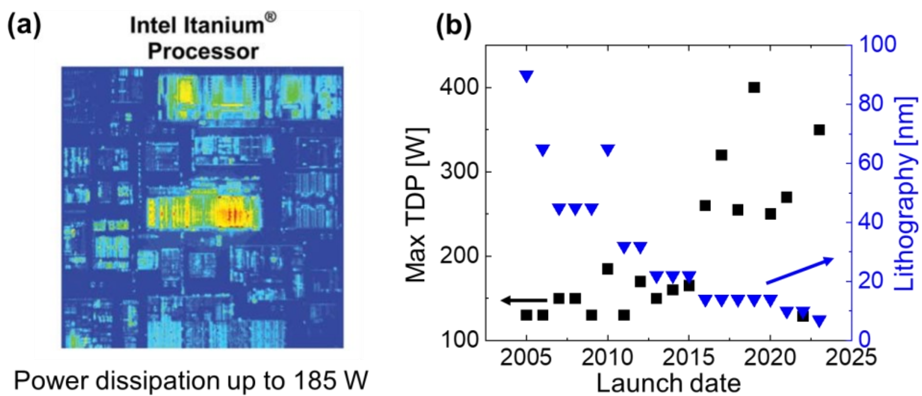

Figure 1.2 (a) Temperature map of an Intel Itanium Processor. **(b)** Highest thermal design power (TDP) of new released Intel processors (left axis) as a function of their launch data. The right axis displays the used lithography size of the same processors. **(a)** Adapted with permission from Mahajan *et al.*[9] **(b)** Data obtained from the Intel product database.[12]

Thermal management of electronic components is therefore essential to keep electronics at a safe temperature and reliable performance. We often refer to Moore's law as an indicator for the exponential growth of the transistor count in electronics and the power density of our computing capabilities.[11] However, from a microscopic point of view the urge for improved thermal designs in electronics has therefore increased at the same time.[9] As an example, confined electronics' self-heating hot spots with power densities from 300 W/cm^2 and above are a significant threat for the long-term use of microprocessors.[9] To illustrate the impact of heat in electronics, Fig. 1.2 (a) shows a temperature map of an Intel Itanium processor with an asymmetric heat spreading along the processor.[9] An important metric related

with thermal management in these processors is the thermal design power (TDP). TDP describes the average power dissipation of the processor when operating at base frequency. Fig. 1.2 (b) shows the maximum TDP and the lithography size of new released processors from Intel as a function of their launch date.[12] We can observe that the max TDP tends to increase while the miniaturization of the device level continues. Therefore, improving our thermal management capabilities at lower scales is an essential need for the reduction of the TDP in microprocessors.[8] Thermal control devices at the micro and nanoscale that can manage heat in a more advanced way will not only have an impact in electronics but also in other energy related applications, such as storage or scavenging technologies.

The following sub-sections elaborate in detail the domains of energy dissipation in electronics and novel thermal management strategies which are relevant to this thesis.

1.1 Energy dissipation in electronics

The flow of charge carriers along a material under the presence of an electric field results in scattering with the atoms of the lattice. This leads to the generation of Joule (self) heating.[1] The magnitude of this heat dissipation scales with the current density and the electrical field of the flow. Following the trends of power density in electronics, the magnitude of Joule heating becomes an equally growing issue in nanoscale devices like transistors and interconnects.[13] In that context Fig. 1.3 shows various performance limitations in different nanoscale electronics which are originated from heating.[14–16] As an example, in modern transistor device heat dissipation is a severe limitation for their reliability and can lead to thermal breakdown as illustrated in Fig. 1.3 (a) and (b).[13–15] As another example, in modern memory devices, heat is a major source for the variability of operation leading to a strong shift of the current vs voltage behavior in between cycles, as illustrated in Fig. 1.3 (c).

This thesis focuses on the thermal characterization of memory resistive switching (RS) devices, which are very promising compared to other state-of-the-art memories.[17] The unique features of RS devices include non-volatility, high storage density and fast parallel computing ability which make them ideal for neuromorphic computing.[17] In comparison to commercially available memory technologies, as static random-access memory (SRAM) or dynamic random access memory (DRAM) devices, RS devices are

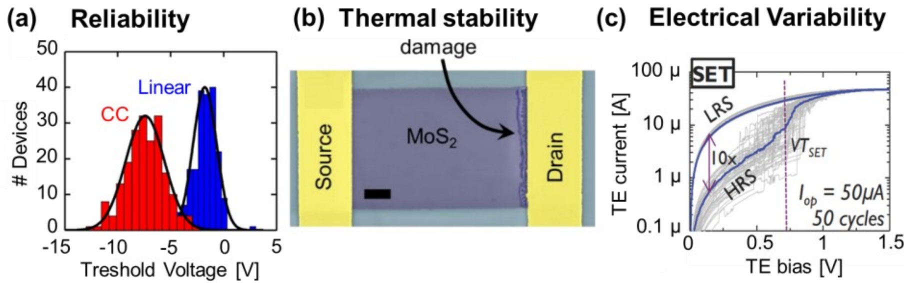

Figure 1.3 (a) Distribution of the threshold voltage of hundreds of MoS_2 field effect transistors (blue: linear method, red: constant current method). **(b)** colored SEM image of a MoS_2 2D transistor channel after thermal breakdown (scale bar 1 µm). **(c)** electrical current at the top electrode (TE) as a function of the applied bias during the set process of a resistive switching (RS) device during 50 cycles. **(a)** Adapted with permission from Lanza *et al.*[14] **(b)** Adapted with permission from Yalon *et al.*[15] **(c)** Adapted with permission from Lanza *et al.*[16]

typically non-volatile and therefore do not require a power intensive refresh.[18] Currently used non-volatile memories as flash devices require a comparably high programming voltage (< 10 V) with a typical endurance of > 10^4-10^5 cycles. RS devices can be operated at relative low programming voltages (< 3V) with a higher endurance (> 10^6 cycles).[18]

Promising candidates for RS memory include conductive bridge random access memory (CBRAM), phase change memory (PCMe) and resistive random access memory (RRAM) devices.[19] In PCMe structures a phase change material, like vanadium dioxide (VO_2) or chalcogenides that can change between an insulating and conductive state, is placed in between two electrodes.[19–21] The phase change is induced by applying a current through the material that heats it up. The two different resistive states of the two phases represent the logic states.[19] On the other hand, RRAM devices consist of a metal-insulator-metal (MIM) structure.[22] By applying a bias across the two electrodes one can form and disrupt an electrically conductive path based on oxygen vacancies in an oxide based insulating material.[19] Finally, in CBRAM the metal oxide is replaced by a solid electrolyte and an easily oxidizable metal is used as the top electrode. By applying a bias, mobile metal atoms from the top electrode form an electrical path to the

bottom electrode.[19] Challenges of RS devices are connected with the variability, reliability and thermal stability of the switching process.[17]

In that regard, heat dissipation plays an essential role in the operation and performance of RS devices in many ways.[17] As an example, the operation of PCMe devices is based on the thermally activated phase transition of the active material.[21,23] However, heat dissipation can be a potential source of device failure for PCMe as well. In filamentary-type RRAM the switching process is based on the formation and rupture of spatially confined conductive paths mostly referred to conductive filaments (CF).[24] Due to the extremely confined area of the filament, potentially down to 10 - 7 nm in diameter, extremely high power densities > 10^{13} W/cm^3 are estimated to be achieved during operation.[25] Hence, Joule heating in these devices can facilitate thermal activated processes as ionic diffusion.[26] However, the development of this technology is limited by its high operation variability that originates partially from the spatial extent and temperature of the filaments.[17,27] The following section focuses on challenges related to heat dissipation in RRAM devices, which are characterized in the course of the experimental work in this thesis.

1.1.1 RRAM device fabrication

As mentioned above, RRAM devices consist of a metal-insulator-metal structure, where the insulator is typically a metal oxide. In the recent years, a wide variety of metal oxides have been studied for RRAM devices, like HfO_2,[25,28,29], Ta_2O_5[30,31], or TiO_2[32–34].

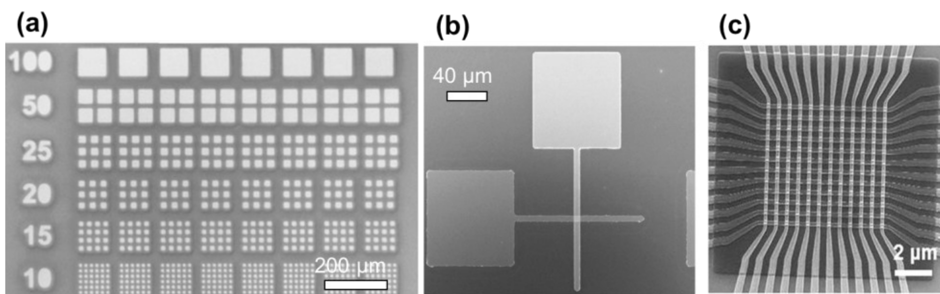

Figure 1.4 Common device structures in resistive random access memory (RRAM) devices. **(a)** Common bottom electrode structure (scale bar 200 µm), **(b)** cross-point structure (40 µm), **(c)** crossbar structure (2 µm). Adapted with permission from Lanza *et al.*[16]

Concerning the RRAM device structure, one usually distinguishes between three different types, as presented in Fig. 1.4.[16] Fig. 1.4 (a) shows the typical bottom electrode method. In this case an insulating layer is grown all over a conducting substrate. The metallic top electrodes are patterned on top of the insulating layer. However, this method is limited to a minimum electrode size of ~ 100 µm^2 for allowing the probe access for electrical characterization.[16] Fig. 1.4 (b) shows an example of a cross-point device area. The fabrication process of the cross-point structure is more complex than the common bottom electrode approach, as it requires at least two lithography steps.[16] However these structures allow a characterization of single devices with areas below microscale. For the analysis of the switching characteristics on a circuit level, crossbar structures as depicted in Fig. 1.4 (c) are widely used. In this case the individual device areas are interconnected with thin wires to common large electrode pads.[16]

1.1.2 RRAM operation principle

In RRAM devices based on metal oxides we can switch from a high resistive (HRS) to a low resistive (LRS) state. We transition between these states through processes of set, i.e., HRS to LRS, and reset, i.e., LRS to HRS.[16,35] Fig. 1.5 shows a schematic illustration of the initial forming, set and reset process of the filament in a metal-insulator-metal based RRAM device. We can consider Ti/Au-TiO_2-Ti/Au for illustration purposes.[36] At the beginning,

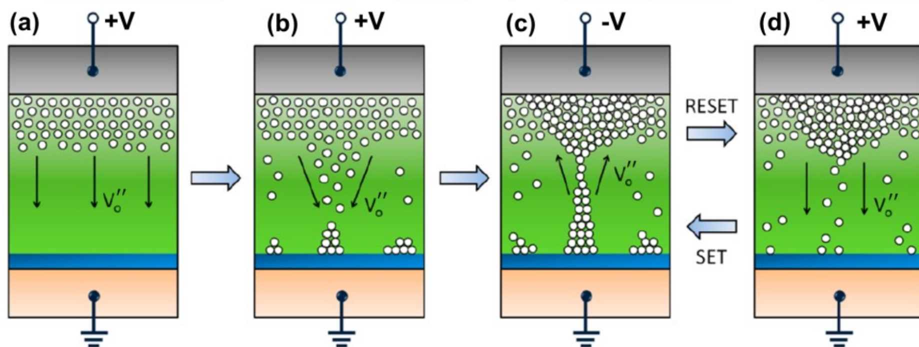

Figure 1.5 Schematic of the forming, set and reset mechanisms in an oxygen vacancy driven RRAM device with a metal-insulator-metal (MIM) structure. The figures present the oxygen vacancy V_O'' distribution (white circles) of the RRAM device in **(a)** pristine, **(b)** during set, **(c)** in the ON and **(d)** OFF state. The operation is achieved by applying a voltage bias of different polarity +V and -V across the electrodes. Adapted with permission from Hu *et al.*[36]

i.e., pristine state (Fig. 1.5 (a)), the RRAM devices are in their HRS. An oxygen vacancy rich layer on top of the TiO_2 layer is originated during the metallization of the top electrode. When applying a sufficiently high electric field, a CF is formed in the oxide between the top and bottom electrodes (Fig. 1.5 (b-c)).[24] The device is then in the LRS, i.e., set process. Due to the application of a positive voltage bias, drifting vacancies are partially reduced and redistributed towards the bottom electrode (as shown in Fig. 1.5 (b)).[36] As a result, a localized path of oxygen vacancies is formed in the active area (Fig. 1.5 (c)),[36] which create a small conductive path. The breakdown of the filament happens when applying a sufficiently high bias of reversed polarity (bipolar) or at the same polarity (unipolar).[24] For this particular example, by applying a reverse bias the CF is dissolved and oxygen vacancies are pulled back to the top electrode (as shown in Fig. 1.5 (d)). When the CF breakdown occurs, the device returns to its HRS, i.e., reset process (Fig. 1.5 (d)). For the initial forming of the CF usually a higher voltage is required than for the subsequent set processes due to the low intrinsic defect density in the pristine state.[24] RRAM devices can be set and reset during multiple cycles with endurances of up to 10^{12} cycles and beyond.[37]

It is worth noting that this explanation is not a universal answer to describe the physical mechanisms of switching in all RRAM devices, since the process of forming can be more complex. However, It is a good representation of the operation principles of the metal-oxide RRAMs presented in this thesis.

1.1.3 Electrical performance in RRAM

RRAM devices are electrically characterized through current vs voltage (*IV*) measurements during cycling.[16] Fig. 1.6 shows typical *IV* curves obtained in a bipolar RRAM device for three different current compliances.[38] Starting in HRS, the electrical current displays a small magnitude at low bias during the set process. Once the applied voltage exceeds the set voltage, the current increases abruptly due to the formation of the conductive filament. The device remains in LRS after turning off the voltage, showing non-volatile behavior. When applying a sufficiently high voltage at the reversed polarity, V_{reset}, the current drops again showing the transition from LRS to HRS.

Usually, a higher electrical power is required for the reset process than for the set process. The type and the size of the filament during the forming can be customized by adjusting the current compliance I_c during the set process. The filament size and thus the resistance in the set state correlates with the intensity of the current applied. However, the higher the I_c is, the higher V_{reset}

is required for the filament breakdown. If filaments with too large diameter are formed, they cannot be reset anymore.[17] Therefore, during RRAM operation one must consider a tradeoff between high ON/OFF ratios and cycling reliability.

The electrical performance of RRAM devices has been characterized in a broad number of studies.[16,18,24,39] Therefore, the reliability of the cycling in RRAM devices is most commonly evaluated by the endurance, state retention, switching time and energy consumption, variability and scalability of the *IV* behavior.[16] A common tool for the electrical characterization of RRAM devices is a semiconductor parameter analyzer (SPA). This tool can perform simple *IV* sweeps in a reliable way to obtain the characteristic *IV* curves of the device, as displayed in Fig. 1.6. However, this technique is time intensive (30-60 seconds per cycle). Pulsed voltage stresses (PVS) methods can be employed for a more convenient characterization of the endurance of the device for a high cycle number > 1000.[16]

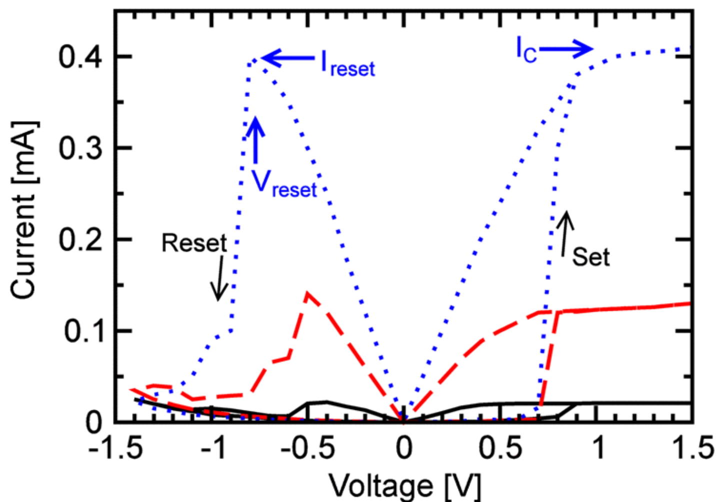

Figure 1.6 Electrical current vs voltage of a RRAM device during the set (at positive voltage) and reset (at negative voltage). The cycles are obtained for different current compliances (I_C), which correspond to black, red and blue lines. The reset is achieved by applying a reverse bias (V_{reset}) corresponding to the initial bias polarity. The magnitude of the reset current (I_{reset}) depends on the I_C applied during the set. Reproduced with permission from Ielmini *et al.*[38]

1.1.4 Limitations and potential sources of device failure

RRAM devices combine excellent stability, high switching speed, a long endurance, low power consumption and a simple structure, making it especially interesting in a vast field of applications.[18,40] On the flipside, performance variability of the operation resistive switching memories is still a major limitation for an extended application of these devices.[16] For example, high variability limits the reliable programming of multiple resistive states. Thermal stresses can reduce the lifetime and reliability of devices significantly.[41]

The lack of reliability in device operation and storage mechanisms in RRAM devices results in high variability of their electrical performance.[42,43] In that context one distinguishes between the cycle-to-cycle (C2C) variability and the device-to-device (D2D) variability of the electrical switching. On the one hand, the C2C variability shows how *IV* curves vary for different cycles within the same device. On the other hand, the D2D variability describes how the *IV* curves change between different devices of the same kind. While variability might be even beneficial for some applications e.g., for random number generators, it is a major limitation for information storage.[16] This variability is in a great level intrinsically related with the nature and formation process of the filament.

Therefore, understanding the underlying fundamental operation, like filament sizes[44] and positions,[45] current densities[46] and heating,[47] is essential for the

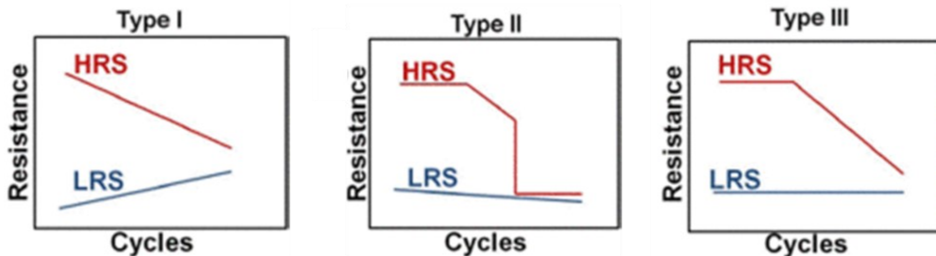

Figure 1.7 Illustration of the resistance vs cycle behavior for three main failure mechanisms of RRAM devices. Type 1 refers to the formation of an interfacial electron barrier. Type 2 refers to the enlarging of the conductive filament by means of redundant oxygen vacancies. Type 3 illustrates the gradual change of the HRS due to a decreasing recombination rate of oxygen vacancies. Adapted with permission from Chen *et al.*[27]

evaluation, design and optimization of RRAM devices. Different studies estimated that the diameter of conductive filaments could reach values down to 10 nm and below.[48,49] High power densities during device operation can result in extremely high temperature increments of >1000 K in memories.[25] These elevated temperatures are a major source for a potential failure of RRAM devices, affecting their endurance. Fig. 1.7 shows the three types of failure mechanisms in RRAMs.[27] One type of failure, label as type 1 in Fig. 1.7, originates from the development of an interfacial electron barrier sourced from high temperature and high current.[17] As a consequence the switching in the active area gets less relevant. Another type of failure, i.e., type 2 in Fig. 1.7, corresponds to the electric field and elevated temperature that led to an excess production of oxygen vacancies. This phenomenon results in an increment of the filament size. If the filament size becomes too big, the device cannot be reset anymore. Finally, failure type 3 in Fig. 1.7 appears at frequent cycling, when the recombination of oxygen ions and vacancies is reduced during the reset process. This leads to a gradual decay of the HRS.[17]

Beyond this threat for the individuals components, extensive heat dissipation from single devices can also affect the performance characteristics of devices in proximity, referred to as thermal crosstalk.[50] Within this context, thermal management is becoming essential in memory based circuits, like neuromorphic computing, where controlling temperature variations is needed for efficient and stable data processing.[51] Therefore, further observations and analysis of filamentary induced hot spots in RRAMs remain relevant as they reveal the need for thermal management to achieve optimum, reliable and efficient performance of their resistive states.

Even though there has been an extensive amount of research on the characterization of the electrical current vs voltage behavior in these devices, only few studies on the exact characterization of the energy dissipation have been conducted. Therefore, further studies concerning the thermal characterization of the energy dissipation in these devices are essential. We must obtain better understanding of how heat affects the resistive switching in memories, and thus, to facilitate the development of new thermal designs that reduce variability.

1.2 Thermal characterization of RRAM devices

Several experimental[25,52,53] and theoretical[25,54–57] approaches have been applied to study the temperature of CFs in RRAM devices. As an example,

thermal analysis with finite element modelling have been conducted to estimate the filament temperature and thermo-dynamics in memories.[25,54–57] However, the experimental investigation of the temperature reached by filaments during operation remains challenging.

On the one hand a high spatial resolution is required to map accurately the hot spots generated by conductive filaments with sizes down to 100 nm. On the other hand, the CF is buried under the top electrode surface, which needs to be taken into account during the analysis. Optical based techniques, like Raman thermometry or infrared scopes, do not present enough spatial resolution to resolve the hot spots generated by CFs in RRAMs. Recently, scanning thermal microscopy (SThM),[23,58–63] i.e., a scanning probe microscopy based technique, has been able to resolve successfully localized heating features at the surface of RRAM devices.[25,52,53]

SThM operates in contact mode obtaining both topographic and thermal maps of the sample surface. It combines a high temporal resolution with a thermal time constant of few hundreds of microseconds and nanoscale spatial resolution.[64] Given these features, SThM has become a popular choice in different studies for the characterization of thermal properties at the nanoscale, like in thermoelectric materials, phase change materials or filamentary based memory.[63,65,66]

1.2.1 Operation principle of SThM

The SThM uses a special thermal probe that can work both as nanoscale heater and/or thermometer. Over the years, there has been a wide variety of probes that have been developed to allow this functionality, such as thermoresistive or thermovoltage probes among others.[64,67] In this thesis, only thermoresistive probes are used.

A thermoresistive SThM probe is made of an element whose electrical resistance correlates with changes in temperature. This probe senses differences in the temperature of a scanned surface due to changes in its electrical resistance.[60,64,68,69] The electrical resistance of the probe (R_{probe}) can be written as a function of the probe temperature T as follows,

$$R_{\mathrm{probe}}\,(T) = R_0 \cdot \left(1 + TCR \cdot (T - T_0)\right) \quad (1.1)$$

where (R_0) is the probe resistance at a reference temperature (T_0) and TCR is the temperature coefficient of resistance. The TCR indicates how much the resistance of a thermoresistive material changes when it increases one degree in temperature. Fig. 1.8 (a) shows a scanning electron microscopy (SEM) image of the thermoresistive probe model that is used in this thesis. It consists of a thin palladium (Pd) line on top of a silicon nitride (SiN) substrate. The Pd-film is the thermoresistive element, which is a popular material for this type of probes as it possesses a high TCR and thus a high temperature sensitivity.[64]

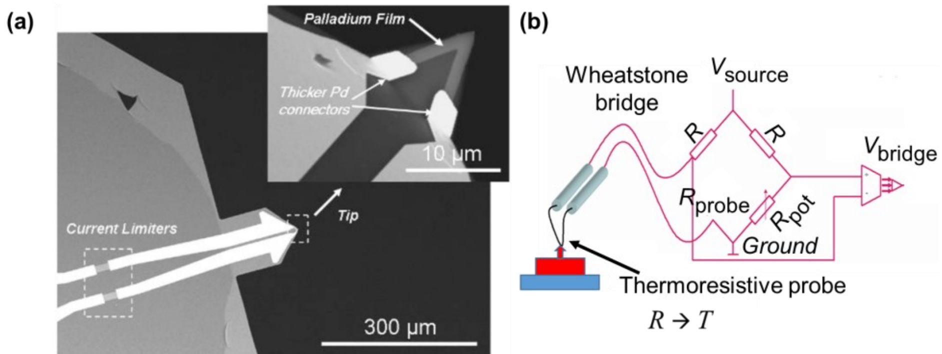

Figure 1.8 Scanning electron microscopy (SEM) image of a Pd film based thermoresistive SThM probe, **(b)** Schematic illustration of an electrical Wheatstone bridge connected to a SThM probe resistance (R_{probe}). The remaining bridge consists of two fixed resistances (R) and an adjustable potentiometer (R_{pot}). During SThM measurements, variations in the temperature of the probe can be sensed by electrical variations across the bridge (V_{bridge}). Adapted with permission from Puyoo *et al.*[69]

For accurately reading the electrical response of the probe due to thermal variations, the SThM probe is usually connected to an external circuit called Wheatstone bridge. Fig. 1.8 (b) shows a schematic illustration of the SThM probe within a Wheatstone bridge.[69] The Wheatstone bridge consists of four resistances, two fixed resistances (R), one adjustable potentiometer (R_{pot}) and the resistance of the probe itself (R_{probe}). When using the SThM as temperature sensor a small bias is applied along the bridge (V_{source}) to read the electrical resistance of the probe while minimizing its self-heating. When scanning the SThM probe under this configuration over a heated sample, one can sense an increase in the potential signal across the bridge (V_{bridge}).

The electrical resistance of the probe, i.e., and hence V_{bridge}, varies during the scan as the temperature along the sample surface modifies.

1.2.2 SThM calibration approaches for sensing nanoscale heating features

One of the major challenges of the SThM is to convert the electrical signal measured in the Wheatstone bridge (mV) into temperature readings (K). For that purpose, one requires to employ a careful calibration approach.[25,52,70–72] As an example, Deshmukh *et al.*[25] suggested a calibration method based on scanning heated Pd metal lines of different widths, *w*. In this approach, the SThM signal is obtained when scanning the heated surface lines. The temperature of the metal lines at certain power are calculated once one determines their *TCR* and using equation 1.1. By connecting the SThM signal in mV with the temperature in K of the lines, a calibration factor (*CaF*) is obtained. Fig. 1.9 (a) schematically illustrates the main heat transfer mechanisms between the probe and the sample at atmospheric conditions during this calibration approach. The authors assumed that the major source of heat exchange at the vicinity of the probe are due to convection (Q_{conv}), water meniscus (Q_{water}) and conduction (Q_S) between the sample and the tip. The water meniscus is formed when the probe tip is in contact with the sample in humid or atmospheric air conditions. Hereby a liquid water bridge is formed between the tip and the sample surface which pulls the cantilever in contact with the sample.[145] In this case additional heat is transported through the water meniscus.[64] The area of heat exchange between them can be approximated by a disc with a thermal exchange radius of r_{th}. Fig. 1.9 (b) shows the calibration factors obtained as a function of the line width. From this graph they observed a saturation on the calibration factor for line widths larger than 200 nm. The authors argued that this cut-off in the line width should define the natural thermal exchange radius of the probe. At line widths lower than that, the thermal exchange radius between probe and tip is truncated and thus the calibration factor varies.[25]

1.2.3 RRAM filamentary hot spot characterization with SThM

Recently, a calibrated SThM has been used to characterize the hot spots in filamentary based RRAM devices.[25,52,53] Fig. 1.9 (c) shows the schematic set up and device structure of the study conducted by Deshmukh *et al.*[25]. In this work, the authors characterized the heat dissipation in HfO_2 based RRAM devices by means of a SThM that is calibrated as explained in section 1.2.2. Fig. 1.9 (d) shows the temperature profiles and thermal maps of hot spots measured with SThM (left inset image). The results are compared to the

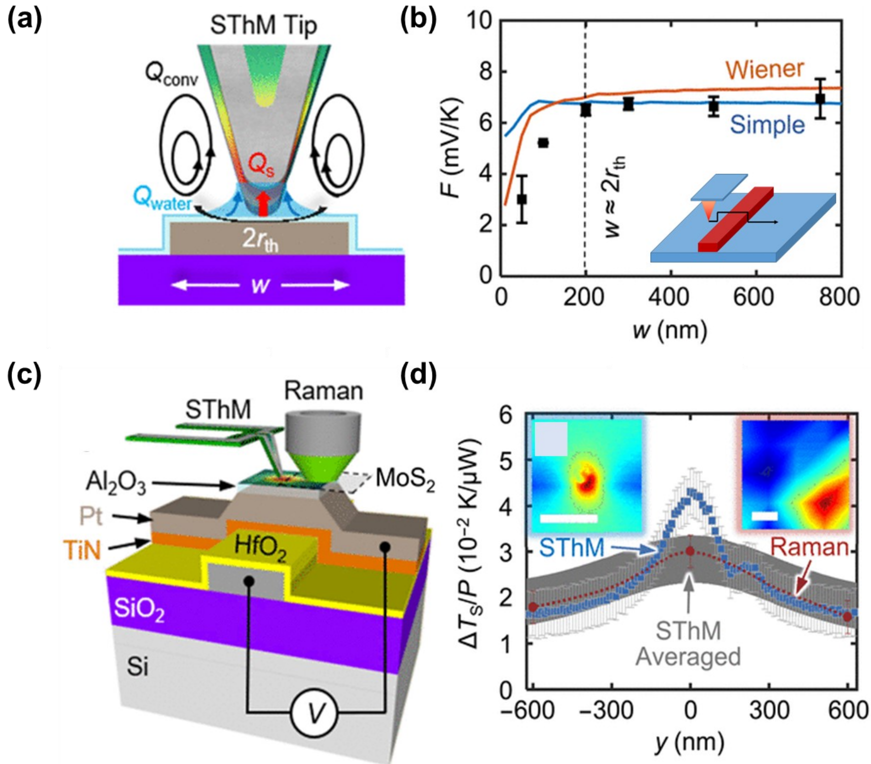

Figure 1.9 (a) Schematic illustration of the heat transfer mechanisms in between a SThM probe and a Pd metal line with the width *w*. The heat between tip and sample is exchanged due to thermal conduction (Q_S), water meniscus (Q_{water}) and convection (Q_{conv}) in a thermal exchange area with a thermal exchange radius of r_{th} (the contribution of radiation in this experiment is negligible); **(b)** SThM calibration factor estimated by characterizing Pd metal line as depicted in (a) as a function of the line width; **(c)** Setup for the thermal measurement of hot spots in HfO_2 based RRAM devices by means of SThM and Raman thermometry; **(d)** SThM and Raman temperature maps and top temperature profiles along the hot spot, normalized by the applied power of hot spots in the same RRAM device (scale bars 750 nm). Adapted with permission from Deshmukh *et al.*[25]

thermal analysis carried out with Raman thermometry, an optical based technique (right inset image). Raman thermometry is not capable to resolve spatially the hot spot generated from CFs, which highlights the advantage and need of using SThM to characterize nanoscale thermal features.

Similarly, Nandi *et al.*[53] investigated the temperature distribution in NbO_x based RRAM devices.

Apart from the above mentioned examples, experimental studies on heat dissipation in RRAM remain scarce. This thesis aims to expand our knowledge in various aspects of the energy dissipation in RRAM devices to offer innovative design routes that improve their performance. For this purpose, I plan to characterize the electrical properties and heat dissipation in TiO_2 based RRAM devices with different areas and compare these features with the device variability. For achieving this, I first extend the calibration approach described in section 1.2.2 to enlarge the versatility of SThM for thermal characterization of electronic devices. Based on the knowledge gained, I draw conclusions on how to take advantage of the electro-thermal analysis of the RRAMs to design future devices.

1.3 Thermal control devices for advanced thermal management

Thermal management of electronics can help to regulate the temperature of devices to favor optimum performance.[73–75] Being at frontiers of thermal management that expand our capabilities to control heat will not only improve our heat dissipation in electrical based technology, but it will bring new opportunities to fields related with energy conversion or storage. As an example, better heat management has a high potential to improve the efficiency of thermoelectric devices or heat storage tanks.[76,77]

In this context, the field of solid-state thermal control devices, i.e., thermal diodes, regulators, switches and transistors has received an increased attention during the last decade.[76,78–80] These thermal control devices are made of materials that exhibit non-linear and switchable thermal behavior.[76] They offer new opportunities to control the heat compared to the traditional toolkit of thermal resistors and capacitors. Solid-state thermal devices are silent, reliable, do not present moving parts and can be easily scaled down, which represents an advantage compared to fluidic or mechanical thermal devices.[81,82] This makes them ideal for thermal management of batteries[83] and electronics,[84] or the development of novel thermal technologies such as phonon logic.[85–87] On the other side, the performance shown by solid-state thermal devices is typically lower than the ones obtained by mechanical or fluidic devices.[88] The higher performance characteristics of mechanical and fluidic devices is enabled due to the activation principle of moving parts and

comes on the cost of the advantage of the reliable operations in solid state as mentioned above.

Nevertheless, solid-state devices have plenty of room for improvement because of their high degree of material tunability (size,[89–94] shape,[95,96] physical-chemistry,[97] etc.). Currently, there is an increasing number of experimental and theoretical publications that focus on the study of new structures and materials for advanced thermal control.[90] This thesis will only focus on one type of non-linear thermal device, i.e. the thermal diode.

1.3.1 Operation of thermal diodes

Solid-state thermal diodes present an asymmetric heat flow that depends on the direction of the temperature gradient, i.e., forward (fwd) vs reverse (rev) direction.[98] This is typically achieved by material engineering[99] or by connecting materials (junction) with dissimilar thermal properties.[78] The research of solid-state thermal diodes started when Starr[100] showed thermal rectification in copper oxides in 1936. More recently, nanotechnology has brought new material engineering opportunities to design reliable and efficient thermal rectifiers.[101] The development of these devices has shown promising features for better management of heat in electronics,[102–105] electrocaloric refrigeration[76] or for thermal computing.[87]

Nanotechnology offers multiple strategies to improve the performance of thermal diodes.[99] This section mainly focuses on nano- to micro-scale thermal diodes based on the combination of different materials, i.e., two-segment materials.[106] Different diode designs can be compared using the following parameters, which are key to determine the device performance:

i) *Rectification ratio* (*RR*): Corresponds to the ability of the device to rectify heat. It is typically expressed as,

$$RR = \frac{|\dot{Q}_{\mathrm{fwd}}| - |\dot{Q}_{\mathrm{rev}}|}{|\dot{Q}_{\mathrm{rev}}|} \tag{1.2}$$

where $\dot{Q}_{\mathrm{fwd}}$ and $\dot{Q}_{\mathrm{rev}}$ are the heat fluxes in the forward and reverse direction when $|\dot{Q}_{\mathrm{fwd}}| > |\dot{Q}_{\mathrm{rev}}|$.

ii) *Thermal bias:* It is the difference of temperature across the device, where T_{h} and T_{c} correspond to the temperatures of the heat source (hot terminal) and the heat sink (cold terminal).

1.3.2 Introduction to two-segment thermal diodes

The simplest design of a thermal diode in solid-state is based on two-segment materials. Such a device consists of a combination of two different material blocks with dissimilar thermal properties.[78] The basic idea to achieve thermal rectification is that the two materials have a different thermal conductivity dependence with temperature.[107–110] Under this condition, an inversion of the thermal bias (temperature gradient) direction results in a different magnitude of the heat flow (forward vs reverse) due to a change in the effective or overall thermal conduction across the two-segment material structure.[78]

In solid state, we differentiate between three approaches to develop a thermal diode based on two-segment materials. First, devices in which the two material blocks have opposite thermal conductivity trends with rising temperature. For the sake of convenience, we define them as junction of materials with different thermal properties (JMT) diodes. Second, thermal diodes based on phase change materials (PCM). In these PCM diodes a solid to solid phase change is the basis for thermal rectification. Third thermal diodes based on radiative heat transfer. Radiative thermal diodes are less relevant for this thesis. Hence, the following part only focuses on the first two types of thermal diodes in the following.

1.3.3 Junction of materials with different thermal properties (JMT)

A JMT thermal diode is a two-segment material thermal diode made of two dissimilar material blocks, e.g., block A and block B.[108,109] These two blocks present different temperature (T) dependent thermal conductivity (k) trends, as presented in Fig. 1.10. Fig. 1.10 (a) and (b) illustrate the thermal conductivity of the two material blocks (k_A) and (k_B) as a function of the temperature. Fig. 1.10 (a) shows that material block A has an increase in the thermal conductivity with increasing temperature. Fig. 1.10 (b) shows that the thermal conductivity of material block B is decreasing with increasing temperature. To understand how such a material system leads to thermal rectification, we must consider the effective thermal properties of the two-segment material structure depending on the thermal bias directionality. Hence, we need to consider two cases, i.e., when the thermal bias is applied in the forward (A → B) vs the reverse direction (B → A).

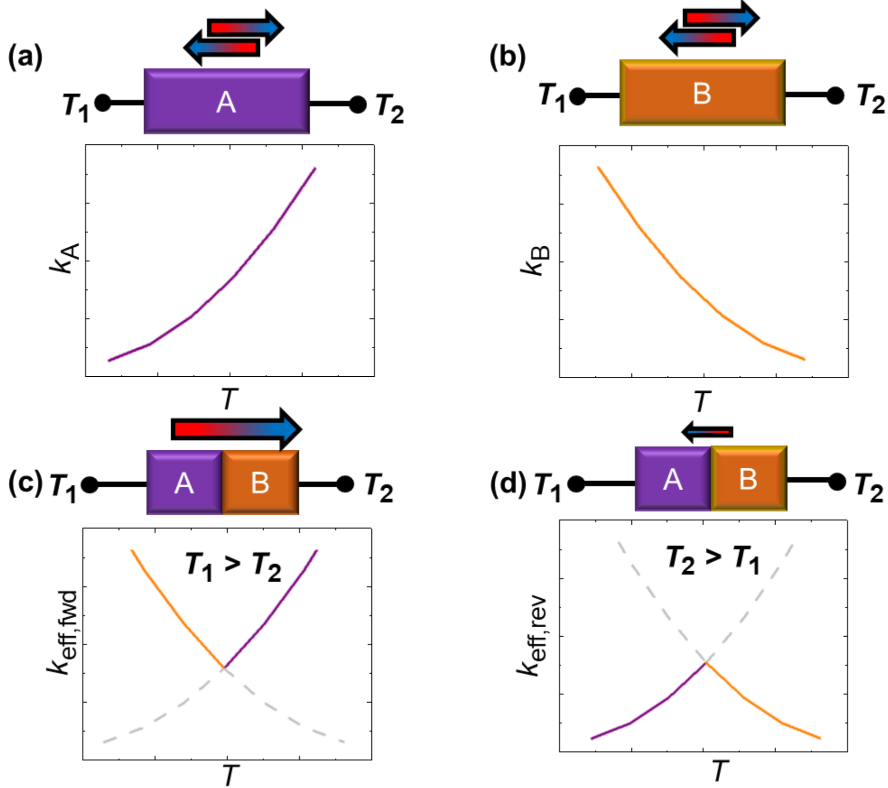

Figure 1.10 Schematic drawing of the thermal conductivity (k) as a function of the temperature (T) in a JMT diode. Thermal conductivity of **(a)** block A and **(b)** of block B separately. Effective thermal conductivity (k_{eff}) (continuous line) of the JMT diode in the **(c)** forward and **(d)** reverse direction.

Fig. 1.10 (c) and (d) illustrate the effective thermal conductivity of the material junction A-B structure in the forward and reverse direction. In the forward direction, a temperature gradient from the hot block A to the cold block B is established. Therefore, the effective thermal conductivity ($k_{eff,fwd}$) of the segment structure, i.e., continuous purple (block A) and orange lines (block B) of Fig. 1.10 (c), is high in the forward direction. In the reverse configuration, the temperature gradient is established from the hot block B to the cold block A. In this case the thermal conductivity trend of both blocks is now reversed compared to the forward case. As a result, the effective total thermal conductivity ($k_{eff,rev}$) of the two-segment structure is lower than in the

forward direction, i.e., continuous purple (block A) and gold (block B) lines of Fig. 1.10 (d). Hence, the total heat flux is expected to be higher in the forward direction in comparison to the reverse configuration under the condition that the temperatures of the terminals (T_h and T_c) are held constant.

Fig. 1.11 shows the thermal conductivity trends of some materials as a function of temperature.[78,111–116,124] These trends are in agreement with the theory of thermal transport expected for these materials.[117–119] From a simplistic point of view, the temperature-dependent thermal conductivity ($k(T)$) trends of typical materials can be described as: i) At low temperatures, $k(T)$ is increasing with T due to the increase of the heat capacity until it reaches a peak.[117,120] The peak position and magnitude of the thermal conductivity depends on the material. ii) At higher temperatures, the thermal conductivity decreases due to a reduction in the phonon mean free path (MFP).[117,120] A combination of two materials with thermal conductivity peaks at different temperatures will result in the desired two-segment material junction structure.

In general, the thermal conductivity peak is reached below room temperature for most of the materials presented in Fig. 1.11. Additionally, there are some materials that present an increase of the thermal conductivity at room temperature (e.g., carbon nanotubes,[112] amorphous silicon oxide,[111] or caloric materials like gadolinium[121]). To take advantage of the asymmetry in the effective thermal properties of the two blocks that form part of the JMT diode, the design is usually limited to low temperatures.

Jezowski and Rafalowicz[106] developed the first JMT diode experimentally in 1978. The authors investigated a junction of graphite and quartz considering absolute temperatures between 6 K and 95 K. The peak of the thermal conductivity of quartz can be found near 6 K.[116,122] In graphite this peak in the thermal conductivity is reached at around 100 K.[115,123] On the one hand, for temperatures below 100 K, graphite presents an increase in the thermal conductivity with rising temperature (block A). On the other hand, the thermal conductivity of quartz decreases for temperatures above 6 K (block B). This thermal diode reaches a maximum rectification of RR = 70% for a thermal bias of 40 K between heat source and heat sink.[33] Similarly, Kobayashi *et al.*[107,124] investigated $LaCoO_3/La_{0.7}Sr_{0.3}CoO_3$ (LCO/LSCO) structures for thermal rectification. LSCO has an increasing $k(T)$ with rising temperature, while LCO presents a decreasing $k(T)$ behavior below 200 K. The authors

observed a thermal rectification of *RR* = 43% between 40 K (heat sink) and 98.9 K (heat source).[107]

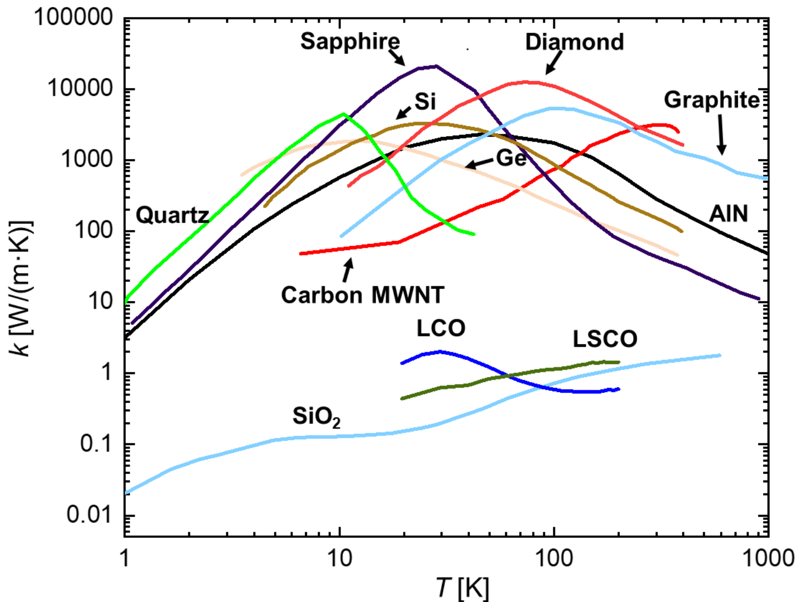

Figure 1.11 Thermal conductivity (k) of some materials as a function of the temperature (T). Data obtained from refs.[78,111–116,124]

1.3.4 Phase change material (PCM) thermal diodes

A phase change material (PCM) thermal diode is another type of two-segment material thermal diode. Here, the two-segment structure is made of a PCM block and a phase invariant material (PIM) block. On the one hand, a solid to solid structural change of the PCM occurs at a critical transition temperature (T_{crit}), leading to a variation of the PCMs thermal conductivity. On the other hand, the phase of the PIM remains invariant at the temperature of application. Bringing together a PCM and a PIM can lead to thermal rectification by taking advantage of the thermal conductivity change due to the phase transition of the PCM block. When the PCM block is in direct contact with the heat source and the temperature is higher than the transition temperature, a phase change in the PCM is induced. However, in the reverse case, when the temperatures in the PCM block are lower than the transition one, no phase change occurs.

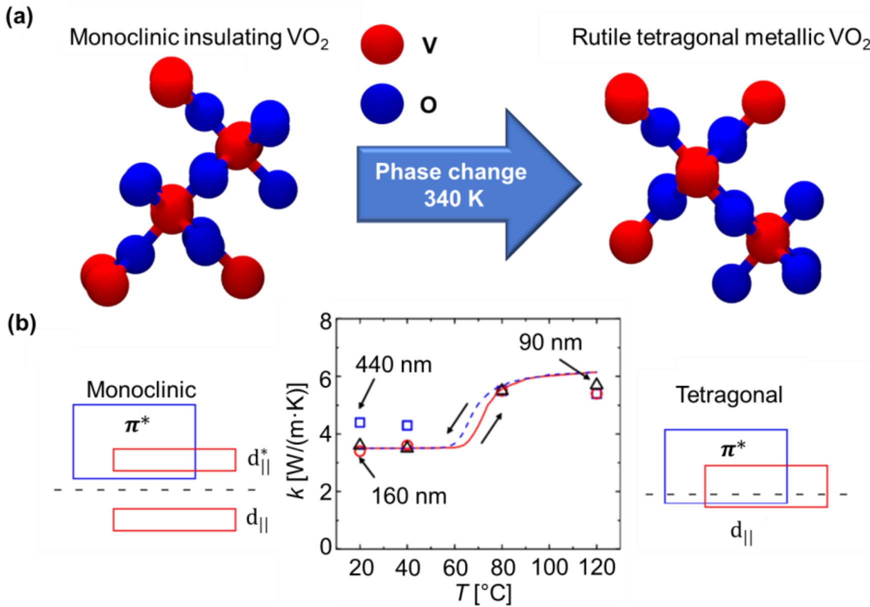

Figure 1.12 Schematic drawing of the changes of VO_2 at its phase transition. **(a)** Crystallographic structure phase change at 340 K from a monoclinic to a tetragonal phase, **(b)** Simple band diagrams and plot of the thermal conductivity (*k*) changes along the phase transition of VO_2 films with thicknesses ranging from 90 to 440 nm as a function of the temperature (*T*). **(a)** Data obtained for the crystal structures from refs.[140–144] **(b)** Adapted with permission from Oh *et al.*[129] and Eyert.[134]

Therefore, two different effective thermal conductivities result from applying a gradient of temperature in the forward vs reverse direction. Recently, some research projects showed that a combination of two different PCMs is a promising approach to achieve high thermal rectification which may exceed values obtained by the regular PCM/PIM structures.[125–127]

In many PCMs the change in the thermal properties occur in a small temperature range (few K) due to a change in the material crystalline structure when the temperature is higher than T_{crit}.[128–130] For that reason, in comparison to JMT diodes, high rectification ratios can already be achieved for small thermal biases (few K).[128] However, the main challenge of PCM diodes is to choose a material that exhibits a phase change resulting in a large difference in thermal conductivity. As an example, vanadium dioxide

(VO_2) is a PCM that has been used in thermal diodes.[131,132] VO_2 presents a metal insulator phase transition (MIT) near room temperature.[133]

Fig. 1.12 depicts the MIT in VO_2 and its change in the thermal conductivity. Fig. 1.12 (a) shows that VO_2 has a monoclinic insulating state that typically changes to a rutile tetragonal metallic state when the temperature rises above ~ 340 K. The thermal conductivity increases across this phase transition.[129,130] As an example, Oh *et al.*[129] reported a ~ 60% increase of k (from k ~ 3.5 W/(m·K) to k ~ 5.5 W/(m·K)) in thin film VO_2 as a consequence of the phase change. The reason for this thermal transition is based on the changes in the band structure and the influence of the electronic heat transport, illustrated in Fig. 1.12 (b).[129,134] While in the insulating state the valence band $d_{||}$ is separated from the conduction band due to a large band gap, the two bands overlap in the metallic state.[134] As a result, the electrical conduction is increased and hence the thermal conductivity, given the influence of the electrons as heat carriers. It is also worth noting that VO_2, like other PCMs, might present hysteresis, meaning that the temperature at which the phase change happens when cooling vs heating might shift slightly.[135]

An example of a PCM diode using VO_2 is illustrated in Fig. 1.13. This structure corresponds to the thermal diode based on a VO_2/Sapphire material combination which is reported by Ordonez-Miranda *et al.*[136] In the forward direction, the heat is flowing from the VO_2 heat source to the sapphire heat sink. The temperature at the heat source is above T_{crit} = 340 K, inducing the VO_2 block to transition to its metallic state. However, in the reverse direction, the VO_2 block is now at the insulating phase because the temperature is below its transition temperature. The phase of sapphire remains the same in both scenarios, i.e., PIM block. Under this scenario, the effective thermal conductivity of the PCM diode in the forward direction is higher than in the reverse one.

Kobayashi *et al.*[128] developed a millimeter sized PCM thermal rectifier based on $La_{1.98}Nd_{0.02}CuO_4$ (PIM) and MnV_2O_4 (PCM). MnV_2O_4 has a structural phase change at T_{crit} = 57 K that leads to an abrupt decrease in the thermal conductivity as the temperature increases. At this temperature the structure is converted from a tetragonal phase with a high thermal conductivity to a cubic phase with a lower one.[128,137] The authors observed a thermal rectification of RR = 14% for a temperature span between 55.4 K (heat sink)

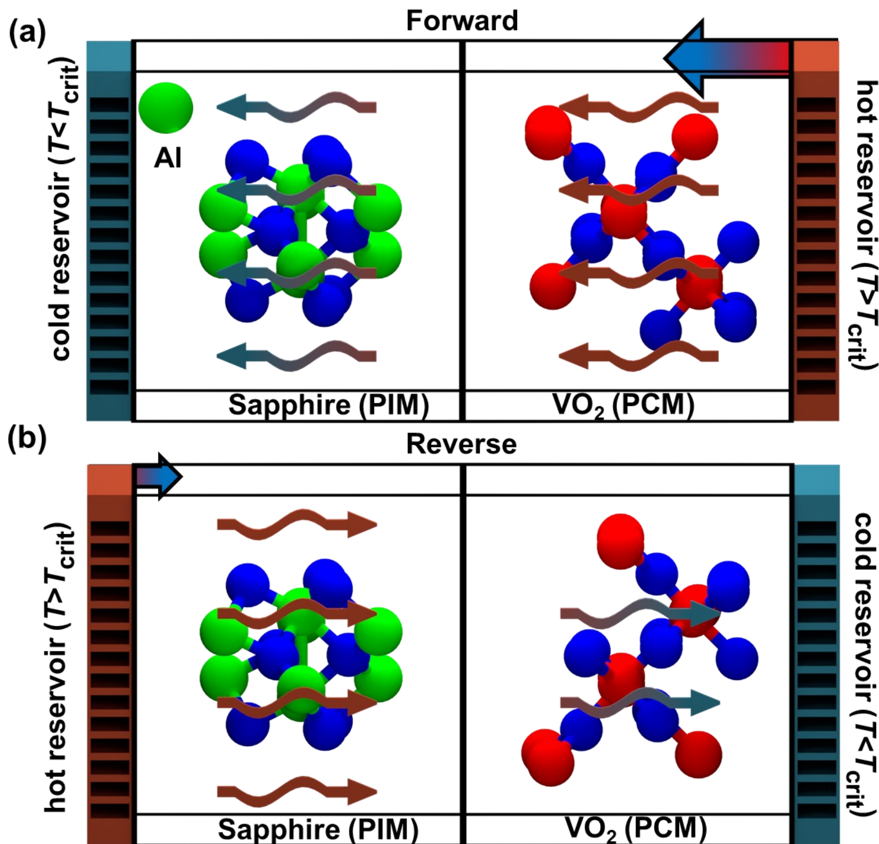

Figure 1.13 Schematic drawing of a sapphire/VO_2 diode. **(a)** Heat flux in forward direction (from the hot VO_2 to the cold sapphire), **(b)** Heat flux in reverse direction (from the hot sapphire to the cold VO_2). The arrows show the direction of heat and indicate that the higher heat flux is in the forward direction. Data obtained for the crystal structures from refs.[140–144]

and 57.4 K (heat source), which can be considered as a high value considering the small thermal bias below 2 K.[128] Additionally, Garcia-Garcia and Alvarez-Quintana[138] investigated the thermal rectification in a Nitinol/Graphite PCM thermal diode. In this case Nitinol is used as the PCM and graphite as the PIM. Nitinol has a structural phase change at around T_{crit} = 330 K from a monoclinic martensite phase to a cubic austenite phase at temperatures higher than the transition one.[138] The authors observed a rise in the thermal conductivity of the Nitinol from k ~ 7.8 W/(m·K) in the

martensite to k ~ 17.3 W/(m·K) in the austenite phase. They obtained a maximum thermal rectification of RR = 47% at a temperature of 290 K with a thermal bias of 160 K.[138] The thermal conductivity rose gradually above the phase transition temperature and not as stepwise, which involved a significant enhancement of the thermal rectification at higher temperatures.

Solid-state thermal control devices like thermal diodes represent an emerging field that could make the leap into advanced heat control, expanding our thermal management capabilities. However, one of the limiting factors of these thermal devices is related to their characteristic performances.[88] Solid state thermal diodes typically display rectification ratios below 100 %.[139] Therefore this thesis aims to characterize a new design for the development of a thermal diode based on multilayer phase change materials. In that context I attempt to extend the prior described PCM/PIM structures. Due to that I expect to exceed rectification ratios obtained in simple state of the art PCM/PIM solid state thermal diodes. Moreover, I attempt to create additional degrees of freedom in the operation of such devices. Finally, I make on effort on presenting a potential application approach in which these thermal diodes can be implemented in thermal storage elements to increase their heat retention.

1.4 Scope of this thesis

This thesis revolves around the concept of heat at nano- and micro-scales and how to improve its management and control for applications related with electronics and heat storage.

On the one hand, my first general goal is to gain deep insights on the electro-thermal switching mechanism of RRAM devices and how it affects their performance variability. For that purpose, I used scanning thermal microscopy (SThM) as a powerful and versatile tool for quantitative nanoscale thermal characterization of energy dissipation in electronics. A deeper understanding of the heat generated by modern memory devices will help our scientific and technological communities to develop design strategies that result in more efficient electronics. To achieve that, I had to overcome challenges related with the calibration of SThM and to carry out complex electro-thermal analysis of distinct types of TiO_2 RRAM devices.

On the other hand, my second general goal was to develop new routes to advance in the control of heat through novel solid-state thermal diodes. For that purpose, I developed a finite element model of a novel thermal diode

design based on phase change materials. To achieve that, I had to overcome challenges related with the design of the thermal diode and to conduct a deep analysis to find its most suitable application. I set the foundations of a pioneer solid-state thermal diode with high and modular rectification ratios. Based on the device rectification factor and average operating temperature, the most proper integration was found to be in heat storage.

1.5 Research questions and lines

Based on the scope of the thesis I will give answers to the following Research questions connected to the two major goals:

Goal 1: To gain deep insights on the electro-thermal switching mechanism of RRAM devices and how it affects their performance variability.

- *Research question 1 (RQ1)*: How do I need to calibrate the SThM to obtain quantitative and accurate characterization of filamentary nanoscale hot spots in memory devices?
- *Research question 2 (RQ2):* How can I reduce the variability in resistive random access memories based on their electro-thermal behavior?

Goal 2: To develop new routes to advance in the control of heat through novel solid-state thermal diodes.

- *Research question 3 (RQ3)*: How can we exploit the properties of phase change materials to develop a novel thermal diode with state of the art rectification ratios?
- *Research question 4 (RQ4):* What is the most suitable energy related application for this novel thermal diode design?

To answer these research questions, I formulated the following specific research lines:

Research line 1 (connected to RQ1): Develop a SThM calibration approach that allows accurate measurements of nanoscale hot spots. To this end, I plan to measure with SThM different metal lines that Joule heat and that mimic variable probe-sample thermal exchange processes. From this approach, I will obtain a calibration factor that accounts for the thermo-resistive SThM probe measuring conditions and the size of the heating features observed.

Research line 2 (connected to RQ2): Characterize electrically (*IV* curves) and thermally (with SThM) TiO_2 based RRAM devices. The calibrated SThM system conduct temperature measurements of CF in steady state and in-operando conditions. Combining both electrical and thermal measurements, I attempt to understand how the CFs behave under different device structures and electrical cycling.

Research line 3 (connected to RQ3): Develop a FEM of a thermal diode based on a multilayer structure made of phase change and phase invariant materials. The idea is to expand the concept of two-segment diodes to more layers, providing high and modular rectification ratios that offer new possibilities of thermal control.

Research line 4 (connected to RQ4): Based on the performance of the multilayer thermal diode, develop an analytical model to determine its potential for energy related applications.

1.6 Thesis organization

This thesis is divided into 5 chapters. In the first chapter I provide an introduction to the operation and energy dissipation of electronic devices, highlighting memory devices. Moreover, I introduce the SThM as a powerful tool to characterize localized heating features on these electronic devices. Last but not least, I also review our current capabilities to manage heat as an essential need in electronics and beyond. Subsequently, I present the scope of the thesis and the research questions and research lines that I plan to address. Moreover, I elaborate on the specific contributions that I made in the frame of this thesis.

In the second chapter I show how to conduct careful calibration of SThM signals for obtaining quantitative analysis of the temperature at the surface of heated samples. This approach consists of a set of metal lines with different widths that mimic different thermal exchange processes between the SThM probe and the sample surface. Based on this analysis, I determine a calibration factor that can adapt to different measuring conditions. This allows to obtain accurately the temperature of electronic devices.

In the third chapter, I use the calibrated SThM system for the characterization of hot spots in TiO_2 based RRAM devices. I study the localized heating generated by conductive filaments in individual cross-point structures with

different area sizes (2x2 μm^2 and 5x5 μm^2). Thermal maps of these devices are obtained in steady-state and in-operando conditions. The thermal analysis combined with their electrical performance allows us to determine potential sources of variability in RRAM devices and suggest modern design routes to improve their performance.

In the fourth chapter, I look into the development of a new thermal diode design consisting of a multilayer structure made of phase change materials (PCM-diode). For that purpose, I develop a finite element electro-thermal model to study the performance of different diode material configurations. The thermal conduction properties of this diode depending on the heat flow direction are studied for multiple temperature gradients. I compare these results with the state of the art of solid-state thermal diodes and propose a potential energy related applications for this kind of devices.

In the fifth and concluding chapter, I draw conclusions based on the results from the prior chapters. In that context I compare the outcome with the initial research questions and research lines. Finally, I provide recommendations to be considered in future studies.

1.7 Research contributions

During the course of this thesis my experimental focus relied on the operation of a SThM for the quantitative characterization of TiO_2 based RRAM devices. Moreover, I conducted the related FEM simulations for the analysis of the thermal diode designs and applications. The outcome of the individual studies was obtained in collaboration with multiple researchers from different research institutes. In the following text, I would like to specify my contributions and those provided from the collaborators.

Prof. Gerrit Brem from the University of Twente was the supervisor of this PhD project. In that context he provided feedback for the orientation and organization of the PhD planning. Moreover, he provided the lab and research facilities in which frame the SThM measurements were performed.

During the whole course of my project, Prof. Miguel Muñoz Rojo from the University of Twente, and the Spanish National Research Council (CSIC) daily supervised this PhD project. He provided constant guidance for the research carried out in this thesis. In that context he was engaged in all of the below mentioned projects and provided constant feedback to the design, discussion, conceptualization, and results of the outcome of the research.

For the calibration study of the SThM in chapter 2, I conducted the SThM and electrical measurements for the characterization of the calibration samples as well as the PCM devices. I carried out the corresponding data analysis and data processing. Based on that I calculated and evaluated the Calibration Factors. Finally, I applied and evaluated the null point measurements. Çağıl Köroğlu and Dr. Sanchit Deshmukh from Stanford University provided the COMSOL model which I used for the characterization of the line temperature. The calibration samples were fabricated by an external company, MicroCreate, and by Xing Gao from the University of Twente. Dr. Nicolas Wainstein and Prof. Eilam Yalon fabricated the PCM devices and prepared the corresponding FEM COMSOL simulation for the characterization of the PCM temperature. Prof. Eric Pop from Stanford University, Prof, Hans Hilgenkamp from the University of Twente and Prof. Mario Lanza from the King Abdullah University of Science and Technology (KAUST) provided feedback for the arrangement and the discussion of the results.

During the course of the RRAM study in chapter 3, I performed the electrical characterization of the cycling behavior of the RRAM devices by means of a semiconductor parameter analyzer (SPA). I received help from Xing Gao and Dr. Carlos M. M. Rosário from the University of Twente. Moreover, I was responsible for the experimental execution of the SThM measurements and data analysis (steady state, in operando and calibration) for the quantified characterization of the heat dissipation in the RRAM devices. Prof. Mario Lanza (KAUST), Dr. Fei Hui (Zhengzhou University) and Kaichen Zhu (University of Barcelona) fabricated the RRAM devices and provided help with the discussion of the results. Çağıl Köroğlu and Dr. Sanchit Deshmukh (Stanford University) provided the COMSOL model which I used as the base for the characterization of the filament temperature. Yue Yuan (KAUST), Dr. Martina Tsvetanova (University of Twente) and Dr. Melissa Goodwin (University of Twente) conducted the STEM measurements and FIB preparation for the characterization of the RRAM structure. Prof. Eric Pop (Stanford University), Prof. Mario Lanza (KAUST) and Prof. Hans Hilgenkamp (University of Twente) provided feedback for the arrangement and the discussion of the results.

In the context of the theoretical study of the thermal diode presented in chapter 4, I developed the models and developed the COMSOL simulations and data analysis for the characterization of the thermal rectification of the thermal diode design structure. Dr. Katja Klinar from the University of

Ljubljana assisted me during the initial design of the model. I designed the theoretical model for the evaluation of the potential of the thermal diode for the application in thermal storage. In this case I received guidance from Dr. Shahzaib Abbasi (University of Twente) to discuss in which energy related application we could optimally integrate the device. Prof. Andrej Kitanovski (University of Ljubljana) and Prof. Gerrit Brem (University of Twente) provided feedback for the arrangement and the discussion of the results.

Apart from that Dr. Katja Klinar (University of Ljubljana), Prof. Andrej Kitanovski (University of Ljubljana) and Dr. Ananth Saran Yalamarthy (Stanford University) provided feedback during the development of the review on “Solid-State Thermal Control Devices” published in Advanced Electronic Materials.

All of the SThM measurements were done in the Kleinhorst laboratory of the University of Twente operated by Henk-Jan Moed. In that context Henk-Jan Moed, Bob Siemerink and Robert van Wijk provided support for the research arrangement of the SThM measurements.

All the electrical characterization measurements with the SPA were conducted in the laboratories of the Interfaces and Correlated Electrons (ICE) group of Prof. Hans Hilgenkamp of the University of Twente. Frank Roesthuis provided support for the research operation conducted in that context.

The cover of this thesis is partially based on the front cover design linked to the following article:

T. Swoboda, K. Klinar, A. S. Yalamarthy, A. Kitanovski and M. Muñoz Rojo, Adv. Electron. Mater., 2020, 7, 2000625.

This design was created by the authors of this article, is published in and adapted with permission from Advanced Electronic Materials.

Link: https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.202170008

In order to acknowledge the contributions of all involved researcher I will refer to ‘’we’’ in the description of the following chapters.

1.8 Introduction references

1 E. Pop, *Nano Res.*, 2010, **3**, 147–169.

2 H. Rong, H. Zhang, S. Xiao, C. Li and C. Hu, *Renew. Sustain. Energy Rev.*, 2016, **58**, 674–

691.

3 IEA, IEA Energy Report, https://www.iea.org/countries/the-netherlands.

4 IEA, Data Centres Data Transm. Networks, https://www.iea.org/reports/data-centres-and-data-transmission-networks.

5 A. C. Kheirabadi and D. Groulx, *Appl. Therm. Eng.*, 2016, **105**, 622–638.

6 M. Wahlroos, M. Pärssinen, S. Rinne, S. Syri and J. Manner, *Renew. Sustain. Energy Rev.*, 2018, **82**, 1749–1764.

7 Y. Jaluria, A. Sunder and J. Z. Benner, *Front. Heat Mass Transf.*, 2020, **15**, 12

8 J. L. Smoyer and P. M. Norris, *Heat Transf. Eng.*, 2019, **40**, 269–282.

9 R. Mahajan, C. P. Chiu and G. Chrysler, *Proc. IEEE*, 2006, **94**, 1476–1485.

10 Z. He, Y. Yan and Z. Zhang, *Energy*, 2021, **216**, 119223.

11 M. M. Waldrop, *Nature*, 2016, **530**, 144–147.

12 Intel, Intel Processors Product Specifications, https://ark.intel.com/content/www/us/en/ark/search/featurefilter.html?productType=873.

13 D. G. Cahill, P. V Braun, G. Chen, D. R. Clarke, S. Fan, K. E. Goodson, P. Keblinski, W. P. King, G. D. Mahan, A. Majumdar, H. J. Maris, S. R. Phillpot, E. Pop and L. Shi, *Appl. Phys. Rev.*, 2014, **1**, 011305.

14 M. Lanza, Q. Smets, C. Huyghebaert and L. J. Li, *Nat. Commun.*, 2020, **11**, 1–5.

15 E. Yalon, C. J. McClellan, K. K. H. Smithe, M. Muñoz Rojo, R. L. Xu, S. V. Suryavanshi, A. J. Gabourie, C. M. Neumann, F. Xiong, A. B. Farimani and E. Pop, *Nano Lett.*, 2017, **17**, 3429–3433.

16 M. Lanza, H. S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. C. Regan, L. Larcher, M. A. Villena, J. J. Yang, L. Goux, A. Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. Magyari-Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T. H. Hou, B. Hudec, D. Akinwande, R. Ge, S. Ambrogio, J. B. Roldan, E. Miranda, J. Suñe, K. L. Pey, X. Wu, N. Raghavan, E. Wu, W. D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. C. Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui and Y. Shi, *Adv. Electron. Mater.*, 2019, **5**, 1800143.

17 M. Zhao, B. Gao, J. Tang, H. Qian and H. Wu, *Appl. Phys. Rev.*, 2020, **7**, 011301.

18 F. Zahoor, T. Z. Azni Zulkifli and F. A. Khanday, *Nanoscale Res. Lett.*, 2020, **15**, 15:90.

19 H. P. Wong and S. Salahuddin, *Nat. Nanotechnol.*, 2015, **10**, 191–195.

20 X. Gao, C. M. M. Rosário and H. Hilgenkamp, *AIP Adv.*, 2022, **12**, 015218.

21 J. Lappalainen, J. Mizsei and M. Huotari, *J. Appl. Phys.*, 2019, **125**, 044501.

22 D. Kumar, R. Aluguri, U. Chand and T. Y. Tseng, *Ceram. Int.*, 2017, **43**, S547–S556.

23 S. M. Bohaichuk, M. Muñoz Rojo, G. Pitner, C. J. McClellan, F. Lian, J. Li, J. Jeong, M. G. Samant, S. S. P. Parkin, H. S. P. Wong and E. Pop, *ACS Nano*, 2019, **13**, 11070–11077.

24 H. P. Wong, F. Ieee, H. Lee, S. Yu, S. M. Ieee, Y. Chen, Y. Wu, P. Chen, B. Lee, F. T. Chen and M. Tsai, *Proc. IEEE*, 2012, **100**, 1951–1970.

25 S. Deshmukh, M. Muñoz Rojo, E. Yalon, S. Vaziri, Ç. Köroğlu, R. Islam, R. A. Iglesias, K. Saraswat and E. Pop, *Sci. Adv.*, 2022, **8**, eabk1514.

26 J. Lee and W. D. Lu, *Adv. Mater.*, 2018, **30**, 1–33.

27 B. Chen, Y. Lu, B. Gao, Y. H. Fu, F. F. Zhang, P. Huang, Y. S. Chen, L. F. Liu, X. Y. Liu, J. F. Kang, Y. Y. Wang, Z. Fang, H. Y. Yu, X. Li, X. P. Wang, N. Singh, G. Q. Lo and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2011, 283–286.

28 H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien and M. J. Tsai, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2008, 1–4.

29 M. Lanza, K. Zhang, M. Porti, M. Nafra, Z. Y. Shen, L. F. Liu, J. F. Kang, D. Gilmer and G. Bersuker, *Appl. Phys. Lett.*, 2012, **100**, 123508.

30 A. Schonhals, D. Wouters, A. Marchewka, T. Breuer, K. Skaja, V. Rana, S. Menzel and R. Waser, *2015 IEEE 7th Int. Mem. Work. IMW 2015*, 2015, 15–18.

31 C. M. M. Rosário, B. Thöner, A. Schönhals, S. Menzel, M. Wuttig, R. Waser, N. A. Sobolev and D. J. Wouters, *Appl. Phys. Lett.*, 2018, **112**, 213504.

32 K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Park, J. Shin, K. P. Biju, J. Kong, K. Lee, B. Lee and H. Hwang, *Nanotechnology*, 2011, **22**, 254023.

33 H. Y. Jeong, Y. I. Kim, J. Y. Lee and S. Y. Choi, *Nanotechnology*, 2010, **21**, 115203.

34 B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg and S. Tiedke, *J. Appl. Phys.*, 2005, **98**, 033715.

35 H. Y. Chen, S. Brivio, C. C. Chang, J. Frascaroli, T. H. Hou, B. Hudec, M. Liu, H. Lv, G. Molas, J. Sohn, S. Spiga, V. M. Teja, E. Vianello and H. S. P. Wong, *J. Electroceramics*, 2017, **39**, 21–38.

36 C. Hu, M. D. McDaniel, A. Posadas, A. A. Demkov, J. G. Ekerdt and E. T. Yu, *Nano Lett.*, 2014, **14**, 4360–4367.

37 C. Hsu, I. Wang, C. Lo, M. Chiang and W. Jang, *2013 Symp. VLSI Circuits*, 2013, 166–167.

38 D. Ielmini, *IEEE Trans. Electron Devices*, 2011, **58**, 1–9.

39 X. L. Hong, D. J. J. Loy, P. A. Dananjaya, F. Tan, C. M. Ng and W. S. Lew, *J. Mater. Sci.*, 2018, **53**, 8720–8746.

40 H. Wang and X. Yan, *Phys. Status Solidi - Rapid Res. Lett.*, 2019, **13**, 1900073.

41 J. Lee, H. Y. Chang, T. J. Ha, H. Li, R. S. Ruoff, A. Dodabalapur and D. Akinwande, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2013, 491–494.

42 Z. Shen, C. Zhao, Y. Qi, W. Xu, Y. Liu, I. Z. Mitrovic, L. Yang and C. Zhao, *Nanomaterials*, 2020, **10**, 1437.

43 A. Grossi, E. Nowak, C. Zambelli, C. Pellissier, S. Bernasconi, G. Cibrario, K. El Hajjam, R. Crochemore, J. F. Nodin, P. Olivo and L. Perniola, *IEEE Int. Electron Devices Meet.*, 2016, **2016**, 471–474.

44 G. Molas, G. Sassine, C. Nail, D. Alfaro Robayo, J.-F. Nodin, C. Cagli, J. Coignus, P. Blaise and E. Nowak, *ECS Trans.*, 2018, **86**, 35.

45 A. Belmonte, D. Linten and M. Jurczak, *Microelectron. Eng.*, 2015, **147**, 171–175.

46 D. Ielmini, *Semicond. Sci. Technol.*, 2016, **31**, 063002.

47 S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy and D. Ielmini, *IEEE Int. Electron Devices Meet.*, 2013, **2013**, 31.5.1-31.5.4.

48 U. Celano, L. Goux, R. Degraeve, A. Fantini, O. Richard, H. Bender, M. Jurczak and W. Vandervorst, *Nano Lett.*, 2015, **15**, 7970–7975.

49 D. H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X. S. Li, G. S. Park, B. Lee, S. Han, M. Kim and C. S. Hwang, *Nat. Nanotechnol.*, 2010, **5**, 148–153.

50 P. Sun, N. Lu, L. Li, Y. Li, H. Wang, H. Lv, Q. Liu, S. Long, S. Liu and M. Liu, *Sci. Rep.*, 2015, **5**, 1–9.

51 F. Torres, A. C. Basaran and I. K. Schuller, *Adv. Mater.*, 2022, **accepted**.

52 S. Deshmukh, M. M. Rojo, E. Yalon, S. Vaziri and E. Pop, *Device Res. Conf. - Conf. Dig. DRC*, 2018, **2018-June**, 2017–2018.

53 S. K. Nandi, E. Puyoo, S. K. Nath, D. Albertini, N. Baboux, S. K. Das, T. Ratcliff and R. G. Elliman, *ACS Appl. Mater. Interfaces*, 2022, **14**, 29025–29031.

54 D. Niraula and V. G. Karpov, *IEEE Trans. Electron Devices*, 2017, **64**, 4106–4113.

55 E. Yalon, I. Riess and D. Ritter, *IEEE Trans. Electron Devices*, 2014, **61**, 1137–1144.

56 E. Yalon, S. Member, A. A. Sharma, S. Member, M. Skowronski, J. A. Bain, D. Ritter, I. V Karpov and S. Member, *IEEE Trans. Electron Devices*, 2015, **62**, 2972–2977.

57 N. Polino, M. Laudato, E. Ambrosi, A. Bricalli and D. Ielmini, *Eur. Solid-State Device Res. Conf.*, 2019, **2019-Septe**, 126–129.

58 E. Yalon, S. Deshmukh, M. Muñoz Rojo, F. Lian, C. M. Neumann, F. Xiong and E. Pop, *Sci. Rep.*, 2017, **7**, 1–8.

59 P. Yasaei, Q. Tu, Y. Xu, L. Verger, J. Wu, M. W. Barsoum, G. S. Shekhawat and V. P. Dravid, *ACS Nano*, 2019, **13**, 3301–3309.

60 E. Puyoo, S. Grauby, J. M. Rampnoux, E. Rouvìre and S. Dilhaire, *J. Appl. Phys.*, 2011, **109**, 024302.

61 M. Muñoz Rojo, J. Martín, S. Grauby, T. Borca-Tasciuc, S. Dilhaire and M. Martin-Gonzalez, *Nanoscale*, 2014, **6**, 7858–7865.

62 S. Gomès, A. Assy and P. O. Chapuis, *Phys. Status Solidi Appl. Mater. Sci.*, 2015, **212**, 477–494.

63 K. Kim, W. Jeong, W. Lee and P. Reddy, *ACS Nano*, 2012, **6**, 4248–4257.

64 Y. Zhang, W. Zhu, F. Hui, M. Lanza, T. Borca-Tasciuc and M. Muñoz Rojo, *Adv. Funct. Mater.*, 2020, 30, 1900892.

65 Y. Zhang, W. Zhu, F. Hui, M. Lanza, T. Borca-Tasciuc and M. Muñoz Rojo, *Adv. Funct. Mater.*, 2020, **30**, 1900892.

66 S. Gomès, A. Assy and P. O. Chapuis, *Phys. Status Solidi Appl. Mater. Sci.*, 2015, **212**, 477–494.

67 K. Luo, Z. Shi, J. Lai and A. Majumdar, *Appl. Phys. Lett.*, 1995, **68**, 325.

68 T. Dinh, H. P. Phan, A. Qamar, P. Woodfield, N. T. Nguyen and D. V. Dao, *J. Microelectromechanical Syst.*, 2017, **26**, 966–986.

69 E. Puyoo, S. Grauby, J. M. Rampnoux, E. Rouvìre and S. Dilhaire, *Rev. Sci. Instrum.*, 2010, **81**, 073701.

70 J. Chung, K. Kim, G. Hwang, O. Kwon, Y. K. Choi and J. S. Lee, *Int. J. Therm. Sci.*, 2012, **62**, 109–113.

71 G. Hwang, J. Chung and O. Kwon, *Rev. Sci. Instrum.*, 2014, **85**, 114901.

72 D. G. Cahill, W. K. Ford, K. E. Goodson, G. D. Mahan, A. Majumdar, H. J. Maris, R. Merlin and S. R. Phillpot, *J. Appl. Phys.*, 2003, **93**, 793–818.

73 M. M. S. Aly, M. Gao, G. Hills, C. Lee, G. Pitner, M. M. Shulaker, T. F. Wu, M. Asheghi, J. Bokor, F. Franchetti, K. E. Goodson, C. Kozyrakis, I. Markov, K. Olukotun, E. Pop, J. Rabaey, C. Re, H. S. P. Wong and S. Mitra, *I E E E Comput. R SOC I E T Y*, 2015, **December 2**, 25–33.

74 M. M. Sabry Aly, T. F. Wu, A. Bartolo, Y. H. Malviya, W. Hwang, G. Hills, I. Markov, M. Wootters, M. M. Shulaker, H. S. Philip Wong and S. Mitra, *Proc. IEEE*, 2019, **107**, 19–48.

75 V. Chiriac, S. Molloy, J. Anderson and K. Goodson, *Proc. 15th Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. ITherm 2016*, 2016, 1393–1397.

76 G. Wehmeyer, T. Yabuki, C. Monachon, J. Wu and C. Dames, *Appl. Phys. Rev.*, 2017, **4**, 041304.

77 T. Swoboda, K. Klinar, S. Abbasi, G. Brem, A. Kitanovski and M. Muñoz Rojo, *iScience*, 2021, **24**, 102843.

78 C. Dames, *J. Heat Transfer*, 2009, **131**, 061301.

79 B. Li, L. Wang and G. Casati, *Appl. Phys. Lett.*, 2006, **88**, 143501.

80 S. Narayana and Y. Sato, *Phys. Rev. Lett.*, 2012, **108**, 214303.

81 No Moving Parts : The Promise of Solid-State Drives, https://software.intel.com/en-

us/articles/no-moving-parts-the-promise-of-solid-state-drives.
82 C. Y. Tso and C. Y. H. Chao, *Int. J. Heat Mass Transf.*, 2016, **93**, 605–611.
83 C. Alaoui, *IEEE Trans. Veh. Technol.*, 2013, **62**, 98–107.
84 C. Acar and I. Dincer, *Energy Storage*, 2019, **1**, e47.
85 L. Wang and B. Li, *Phys. Rev. Lett.*, 2007, **99**, 177208.
86 L. Wang and B. Li, *Phys. Rev. Lett.*, 2008, **101**, 267203.
87 S. R. Sklan, *AIP Adv.*, 2015, **5**, 053302.
88 K. Klinar, T. Swoboda, M. Muñoz Rojo and A. Kitanovski, *Adv. Electron. Mater.*, 2020, **7**, 2000623.
89 T. Luo and G. Chen, *Phys. Chem. Chem. Phys.*, 2013, **15**, 3389–3412.
90 M. Nomura, J. Shiomi, T. Shiga and R. Anufriev, *Jpn. J. Appl. Phys.*, 2018, **57**, 80101.
91 D. Vasileska, K. Raleva and S. M. Goodnick, *J. Comput. Electron.*, 2008, **7**, 66–93.
92 Q. Liang, Y. L. He, Y. P. Zhou and T. Xie, *Energy Procedia*, 2017, **105**, 4915–4920.
93 Y. Hasegawa, M. Murata, D. Nakamura and T. Komine, *J. Appl. Phys.*, 2009, **106**, 063703.
94 G. Xie, Y. Guo, X. Wei, K. Zhang, L. Sun, J. Zhong, G. Zhang and Y. W. Zhang, *Appl. Phys. Lett.*, 2014, **104**, 233901.
95 K. A. Brucker and J. Majdalani, *Int. J. Heat Mass Transf.*, 2005, **48**, 4779–4796.
96 J. Chen, G. Zhang and B. Li, *J. Chem. Phys.*, 2011, **135**, 1–8.
97 A. Fallahi, G. Guldentops, M. Tao, S. Granados-Focil and S. Van Dessel, *Appl. Therm. Eng.*, 2017, **127**, 1427–1441.
98 Z. Chen, C. Wong, S. Lubner, S. Yee, J. Miller, W. Jang, C. Hardin, A. Fong, J. E. Garay and C. Dames, *Nat. Commun.*, 2014, **5**, 5446.
99 H. Liu, H. Wang and X. Zhang, *Appl. Sci.*, 2019, **9**, 344.
100 C. Starr, *J. Appl. Phys.*, 1936, **7**, 15–19.
101 C. W. Chang, D. Okawa, A. Majumdar and A. Zettl, *Science*, 2006, **314**, 1121–1124.
102 N. A. Roberts and D. G. Walker, *Int. J. Therm. Sci.*, 2011, **50**, 648–662.
103 Alto University, Heat flow control for future nanoelectronics, https://phys.org/news/2012-08-future-nanoelectronics.html.
104 G. Zhang and H. Zhang, *Nanoscale*, 2011, **3**, 4604–4607.
105 J. Cheh and H. Zhao, *J. Stat. Mech. Theory Exp.*, 2012, **2012**, P06011.
106 A. Jeżowski and J. Rafalowicz, *Phys. Status Solidi*, 1978, **47**, 229–232.
107 W. Kobayashi, Y. Teraoka and I. Terasaki, *Appl. Phys. Lett.*, 2009, **95**, 171905.
108 Y. Yang, H. Chen, H. Wang, N. Li and L. Zhang, *Phys. Rev. E*, 2018, **98**, 1–8.
109 T. Majdi, S. Pal and I. K. Puri, *Int. J. Therm. Sci.*, 2017, **117**, 260–265.
110 X. Sun, S. Kotake, Y. Suzuki and M. Senoo, *heat tra*, 1998, **64**, 2986–2990.
111 V. Kuryliuk, A. Nadtochiy, O. Korotchenkov, C. C. Wang and P. W. Li, *Phys. Chem. Chem. Phys.*, 2015, **17**, 13429–13441.
112 P. Kim, L. Shi, A. Majumdar and P. L. McEuen, *Phys. Rev. Lett.*, 2001, **87**, 215502.
113 G. A. Slack, R. A. Tanzilli, R. O. Pohl and J. W. Vandersande, *J. Phys. Chem. Solids*, 1987, **48**, 641–647.
114 C. J. Glassbrenner and G. A. Slack, *Phys. Rev.*, 1964, **134**, A1058–A1069.
115 E. Pop, V. Varshney and A. K. Roy, *MRS Bull.*, 2012, **37**, 1273–1281.
116 R. C. Zeller and R. O. Pohl, *Phys. Rev. B*, 1971, **4**, 2029–2041.

117 T. M. Tritt, *Thermal Conductivity: Theory, Properties, and Applications*, Physics of Solid and Liquids, 2004.

118 S. H. Simon, *The Oxford Solid State Basics*, Oxford, 2013.

119 A. Amith, I. Kudman and E. F. Steigmeier, *Phys. Rev.*, 1965, **138**, A1270-1276.

120 J. Callaway, *Phys. Rev.*, 1959, **113**, 1046–1051.

121 J. A. Leon-Gil, J. J. Martinez-Flores and J. Alvarez-Quintana, *J. Mater. Sci.*, 2019, **54**, 3211–3221.

122 M. Omini and A. Sparavigna, *Phys. Rev. B*, 2000, **61**, 6677–6688.

123 C. Uher, *Cryogenics (Guildf).*, 1980, **20**, 445–447.

124 D. Sawaki, W. Kobayashi, Y. Moritomo and I. Terasaki, *Appl. Phys. Lett.*, 2011, **98**, 081915.

125 K. Hirata, T. Matsunaga, S. Singh, M. Matsunami and T. Takeuchi, *J. Electron. Mater.*, 2020, **2019**, 1–7.

126 S. O. Kasali, J. Ordonez-Miranda and K. Joulain, *Int. J. Therm. Sci.*, 2020, **153**, 106393.

127 H. Kang and F. Yang, *Phys. Rev. Appl.*, 2018, **10**, 024034.

128 W. Kobayashi, D. Sawaki, T. Omura, T. Katsufuji, Y. Moritomo and I. Terasaki, *Appl. Phys. Express*, 2012, **5**, 027302.

129 D. W. Oh, C. Ko, S. Ramanathan and D. G. Cahill, *Appl. Phys. Lett.*, 2010, **96**, 151906.

130 H. Kizuka, T. Yagi, J. Jia, Y. Yamashita, S. Nakamura, N. Taketoshi and Y. Shigesato, *Jpn. J. Appl. Phys.*, 2015, **54**, 053201.

131 A. Fiorino, L. Zhu, P. Ben-Abdallah, D. Thompson, N. El-Bondry, S. Bansropun, O. Bezencenet, R. Mittapally, S.-A. Biehs, E. Meyhofer and P. Reddy, *ACS Nano*, 2018, **12**, 5774–5779.

132 K. Ito, K. Nishikawa, H. Iizuka and H. Toshiyoshi, *Appl. Phys. Lett.*, 2014, **105**, 253503.

133 A. Kinaci, M. Kado, D. Rosenmann, C. Ling, G. Zhu, D. Banerjee and M. K. Y. Chan, *Appl. Phys. Lett.*, 2015, **107**, 262108.

134 V. Eyert, *Ann. der Phys.*, 2002, **11**, 650–704.

135 M. M. Qazilbash, M. Brehm, G. O. Andreev, A. Frenzel, P. C. Ho, B. G. Chae, B. J. Kim, S. J. Yun, H. T. Kim, A. V. Balatsky, O. G. Shpyrko, M. B. Maple, F. Keilmann and D. N. Basov, *Phys. Rev. B - Condens. Matter Mater. Phys.*, 2009, **79**, 1–10.

136 J. Ordonez-Miranda, J. M. Hill, K. Joulain, Y. Ezzahri and J. Drevillon, *J. Appl. Phys.*, 2018, **123**, 085102.

137 A. Kiswandhi, J. Ma, J. S. Brooks and H. D. Zhou, *Phys. Rev. B*, 2014, **90**, 155132.

138 K. I. Garcia-Garcia and J. Alvarez-Quintana, *Int. J. Therm. Sci.*, 2014, **81**, 76–83.

139 T. Swoboda, K. Klinar, M. Muñoz Rojo and A. Kitanovski, *Adv. Electron. Mater.*, 2020, **7**, 2000625.

140 S. Gražulis, A. Merkys, A. Vaitkus and M. Okulič-Kazarinas, *J. Appl. Crystallogr.*, 2015, **48**, 85–91.

141 A. Merkys, A. Vaitkus, J. Butkus, M. Okulič-Kazarinas, V. Kairys and S. Gražulis, *J. Appl. Crystallogr.*, 2016, **49**, 1–10.

142 S. Gražulis, D. Chateigner, R. T. Downs, A. F. T. Yokochi, M. Quirós, L. Lutterotti, E. Manakova, J. Butkus, P. Moeck and A. Le Bail, *J. Appl. Crystallogr.*, 2009, **42**, 726–729.

143 S. Gražulis, A. Daškevič, A. Merkys, D. Chateigner, L. Lutterotti, M. Quirós, N. R. Serebryanaya, P. Moeck, R. T. Downs and A. Le Bail, *Nucleic Acids Res.*, 2012, **40**, 420–427.

144 R. T. Downs and M. Hall-Wallace, *Am. Mineral.*, 2003, **88**, 247–250.

145 L. Shi, S. Plyasunov, A. Bachtold, P. L. McEuen, A. Majumdar, *Appl. Phys. Lett.*, 2000, **77**, 4295.

Chapter 2 Nanoscale temperature sensing of electronic devices with calibrated scanning thermal microscopy

Abstract

Heat dissipation threatens the performance and lifetime of many electronic devices. As the size of the devices shrink to the nanoscale, we require spatially and thermally resolved thermometry to observe their fine thermal features. Scanning thermal microscopy (SThM) has proven to be a versatile measurement tool for characterizing the temperature at the surface of devices with nanoscale resolution. SThM can obtain qualitative thermal maps of a device using an operating principle based on a heat exchange process between a thermo-sensitive probe and the sample surface. However, the quantification of these thermal features is one of the most challenging parts of this technique. Developing reliable calibration approaches for SThM is therefore an essential aspect to accurately determine the temperature at the surface of a sample or device. In this work, we calibrate a thermo-resistive SThM probe using heater-thermometer metal lines with different widths (50 nm to 750 nm), which mimic variable probe-sample thermal exchange processes. The sensitivity of the SThM probe when scanning the metal lines is also evaluated under different probe and line temperatures. Our results reveal that the calibration factor depends on the probe measuring conditions and on the size of the surface heating features. This approach is validated by mapping the temperature profile of a phase change electronic device. Our analysis provides new insights on how to convert the thermo-resistive SThM probe signal more accurately to the scanned device temperature.

This chapter is derived from the publication:

T. Swoboda, N. Wainstein, S. Deshmukh, Ç. Köroğlu, X. Gao, M. Lanza, H. Hilgenkamp, E. Pop, E. Yalon and M. Muñoz Rojo, Nanoscale, 2023, 15, 7139–7146.

2.1 Introduction

Scanning thermal microscopy (SThM) has become a popular scanning probe technique to measure nano- and micro-scale sample thermal features.[1–3] SThM can be used to determine the thermal properties of different types of nanostructured materials, like polymeric nanowires,[4] thermoelectric materials[5,6] and phase change materials (PCM),[7] when using thermal probes as small heaters and with proper calibration. Furthermore, calibrated SThM thermal probes can be also used as nanoscale sensors to obtain surface temperature maps. Compared to other spatially resolved thermometry techniques, such as infrared or Raman thermometry, SThM has the advantage of a better spatial resolution.[8,9] More recently, nanoscale spatially resolved temperature sensing approaches via SThM have attracted particular interest for determining the energy dissipated in electronic devices, where often heat hinders performance and reliability.[10] For example, SThM has recently been applied to determine temperatures of transistors based on two-dimensional materials like MoS_2[11], and memory devices like resistive random-access memory (RRAM)[12–14] and phase change memory (PCMe)[15], as well as thermally-activated phase change devices based on VO_2.[16] The evaluation of the heat dissipated in individual electronic devices can open doors to establish new device engineering designs and architectures on the basis of devices' thermal signatures.[17,18] However, while SThM is a promising technique for the thermal characterization of electronic devices, its main challenge relates to its complex calibration. In this work, we use a thermo-resistive SThM probe, whose electrical resistance varies with temperature, to scan surface heater metal lines with multiple widths and applied power levels. Based on these measurements, we can determine how the SThM probe calibration factor, a parameter that converts electrical probe signals into temperature, varies under different measuring conditions.

SThM uses a temperature-sensitive probe, like a thermocouple,[19] thermal expansion[20] or a thermo-resistive probe.[1] Among them, thermo-resistive probes are the most widely used for temperature sensing. During measurements, a small current is applied across the thermo-resistive element. This allows to track changes in the electrical resistance of the probe, which depends on temperature[21] as described by

$$R_{\mathrm{probe}}\,(T) = R_0 \cdot \left(1 + TCR \cdot (T - T_0)\right) \qquad (2.1)$$

The probe electrical resistance R_{probe} at temperature T can be calculated by means of a resistance reference value R_0 at temperature T_0. The temperature coefficient of resistance TCR, which is an intrinsic material specific property, defines the slope of the relation between resistance and temperature which in practice is usually linear. As a consequence, an increment of the temperature of the tip correlates with changes in the electrical resistance of the probe, and vice versa.[1,22,23] Using this working principle, SThM can be used to obtain surface thermal maps with high thermal and spatial resolution (less than 1 K and ~50 nm, respectively).[12,13] However, the probe requires careful calibration to quantitatively correlate changes in the electrical resistance of the probe (mV) with temperature variations (K), i.e., a calibration factor *CaF*. For that purpose, several calibration approaches have been suggested in the past.

As an example, one common method for SThM calibration is based on measuring the electrical resistance of the probe while keeping it in contact with a hot-plate stage with an adjustable temperature.[24,25] Alternatively, calibration approaches based on knowing the melting temperature of materials have also been used for thermo-resistive probes.[26] In this approach, the probe is brought into contact with a material of well-defined melting point. The probe is heated until the material melts, which is detected by a sharp decrease in the probe deflection. With this method, the tip resistance can be correlated to the melting temperature of the sample under study. These methods are straightforward for application. However, they do not account the probe thermal exchange area and its dependence on probe power on the calibration, which is especially relevant at the nanoscale.

More recently, Deshmukh *et al.*[13] employed nanoscale metal lines to determine a *CaF* that transforms the electrical SThM probe response into temperature changes.[13] They observed a change in *CaF* depending on the width of the heating metal lines, which was correlated to variations in the tip-sample thermal exchange radius. This method used an electrical insulating capping layer between the tip and the sample that avoids conducting surfaces to interfere with the electrical signal of the Wheatstone bridge or even probe damage. This feature is especially relevant for the characterization of electronic devices when sensitive thermo-resistive probes are used. Additionally, it allows comparability of the results with samples of similar capping surfaces, i.e., comparable thermal contact resistance between tip and sample. If a capping of the sample surface is not convenient for the measurement one could also operate the SThM in non-contact

mode.[27] However this method does not allow a simultaneous topography detection which is important for localization of thermal features in devices. To advance this calibration approach, it is essential to study the influence of a broader range of line widths as well as the impact of the self-heating probe to better understand their influence on the *CaF*.

In this work, we extend the results of the calibration method described in reference.[13] We use palladium (Pd) on silicon nitride (SiN) based thermo-resistive SThM probes[22] to characterize the heating produced by thin Pd metal lines of different widths. Pd possesses a high and well-known *TCR*, which makes it an ideal material to use in this experiment, to characterize and to compare with previous results.[28–30] We carefully evaluate the *CaF* based on the probe-sample thermal exchange area, which causes different line widths to yield different SThM probe temperatures. Additionally, we investigate the impact of the power applied to the SThM probe to sense temperature at the surface. Apart from that we characterize the heating behavior for each power applied to the probe. Overall, we aim to shed light on the need to carefully choose the *CaF* based on the size of the sample as well as the tip-sample energy balance.

2.2 Experimental setup

The measurement approach of our calibration including the SThM setup, and the calibration sample structure is sketched in Fig. 2.1. Regarding our calibration samples, we used Pd metal lines of different widths (50 – 750 nm). The SThM probe is connected to an external Wheatstone bridge as illustrated in the figure. The details of the fabrication and measurement setups are described in the following subsections.

2.2.1 Fabrication of the calibration sample

Firstly, four heater pads were patterned on a SiO_2/Si Substrate by using optical lithography. The substrate was made of boron doped silicon with a thickness of 525 ± 25 µm. The thickness of the SiO_2 was measured to be 309 nm employing an ellipsometer. 2 nm Ti/50 nm Pd contact pads were evaporated through e-beam evaporation. Secondly, 50-750 nm wide heater patterns were fabricated using e-beam lithography using poly-methyl methacrylate (PMMA) as a resist layer. Using e-beam evaporation, we deposited 2 nm Ti/30 nm Pd metal lines. The mask design is illustrated in Fig. 2.2. We capped the devices with a thin insulating layer to keep the sample electrically isolated from the SThM probe. Therefore, an Al_2O_3 thin

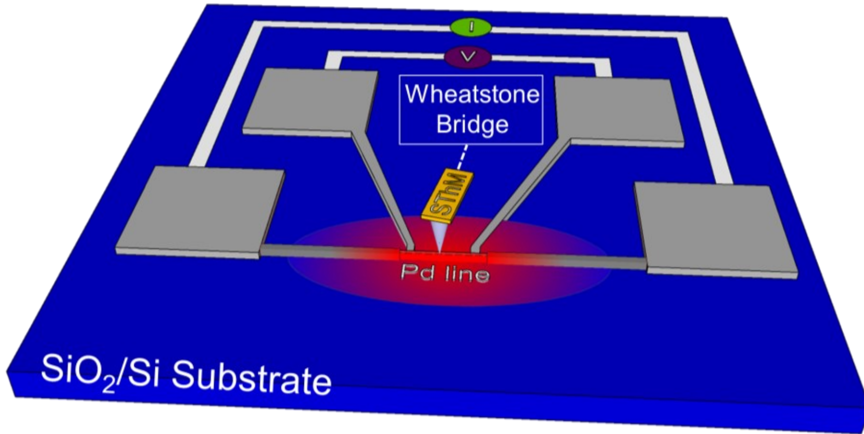

Figure 2.1 Sample and measurement configuration. Palladium (Pd) lines with different widths (50-750 nm) and four Pd pads are deposited on a SiO_2/Si substrate. For the measurement, the heated lines are scanned using SThM. A Wheatstone bridge is used to track changes in the electrical resistance of the probe.

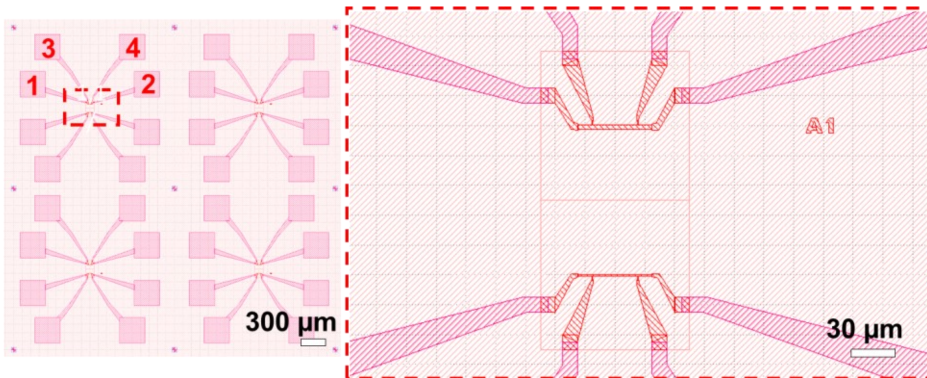

Figure 2.2 Mask design of the calibration samples. The heater pads (1-4) are used for four-point probe measurements. The four heater pads are connected via metal lines of a width of 50-750 nm as indicated in the right image.

film was deposited on these calibration samples using pulsed laser deposition (PLD) from a crystalline Al_2O_3 target at room temperature. The distance between the target and sample was ~ 45 mm. A KrF excimer laser (λ = 248 nm, 20 ns pulse duration) was used with an energy density of ~ 1.5

J/cm^2 and a pulse repetition rate of 5 Hz. The oxygen background pressure was 10^{-1} mbar. All films were grown using the same number of laser pulses (500) and the target thickness was ~10 nm.

2.2.2 Atomic force microscopy (AFM) analysis of the topography of the lines

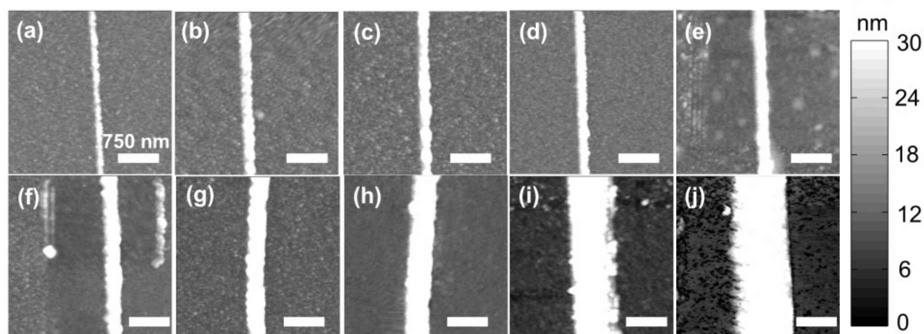

Figure 2.3 Atomic force microscopy (AFM) maps obtained for the Pd metal lines of the calibration samples with a line width of **(a)** 50 nm, **(b)** 60 nm, **(c)** 75 nm, **(d)** 100 nm, **(e)** 120 nm, **(f)** 150 nm, **(g)** 200 nm, **(h)** 300nm, **(i)** 500 nm, **(j)** 750 nm (scale bar 750 nm).

We used an Asylum MFP-3D atomic force microscope (AFM) as the tool of all our scans in this study. First, we started scanning the different lines in AFM tapping mode. We scanned the surface by using a constant speed and scan size. Fig. 2.3 (a-j) show the topography obtained for the different lines (all scale bars 750 nm).

2.2.3 Electrical characterization of the lines

First, the metal lines were characterized electrically to determine their electrical resistance. For that purpose, we used four-point probe measurements as shown in Fig. 2.1 to characterize each line. By means of this measurement approach we exclude the contact resistance. Therefore, we applied current between the two exterior pads while measuring the potential difference across the inner ones. Using this approach, the resistance of the line was measured as a function of the applied power. For that purpose, we used a 4200 A-SCS Parameter Analyzer from Keithley. Additionally, we used thin tungsten needles to contact the heater pads. We adjusted the maximum current applied to the lines depending on the line width. We aimed to not exceed a power value of 3 mW to avoid any heating

damage to the lines. Moreover, these power magnitudes enabled a considerable elevated temperature increase which fulfilled our measurement

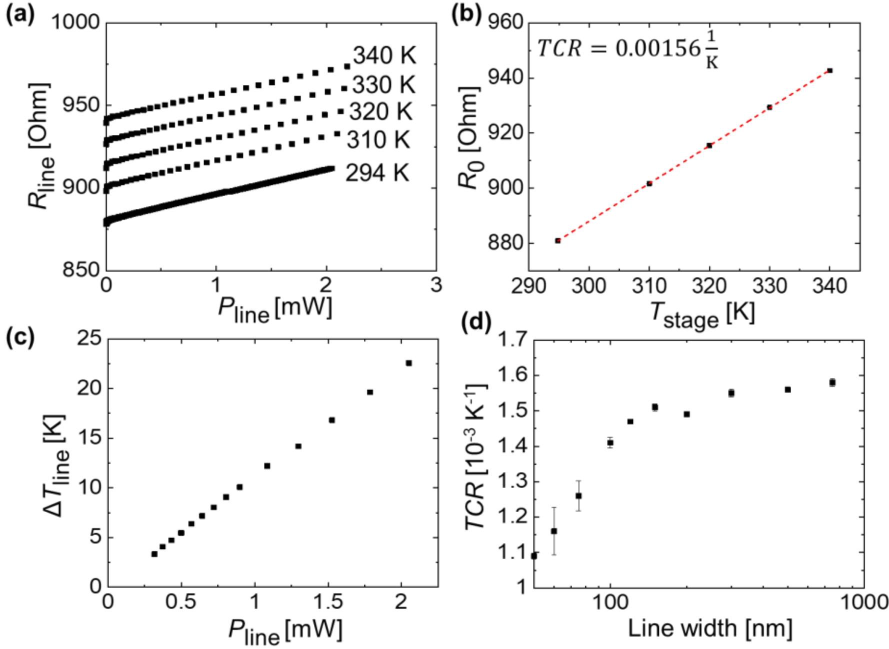

Figure 2.4 (a) Resistance of a 500 nm wide Pd metal line (R_{line}) as a function of the power applied to the line (P_{line}) obtained at five different temperatures. **(b)** Resistance at zero power (R_0) obtained from the results in **(a)** plotted against the temperature of the sample stage (T_{stage}) during the measurement. The *TCR* of the specific line is calculated on base of the slope of this graph. **(c)** Calculated temperature increase of the self-heated line (ΔT_{line}) plotted against the power applied to it (P_{line}). **(d)** Temperature coefficient of resistance (*TCR*) of each line plotted against their line width.

requirements. Using a sample stage with an adjustable temperature, we repeated this measurement at four different temperatures above the ambient temperature (310, 320, 330, and 340 K).

Since the resistance of the thermoresistive Pd lines depends on its temperature linearly,[31] as described by equation 2.1, one observes a linear increase of the resistance with the power applied. Fig. 2.4 (a) shows an example of the R_{line} vs P_{line} results for a Pd metal line of 500 nm line width. The graph at 294 K represents the non-heated measurement at room

temperature. On the base of these graphs, we calculated the resistance at zero power R_0 by linearly extrapolating the R_{line} vs P_{line} graphs at higher power values. Based on these measurements, we were able to determine the resistance at zero power, i.e., R_0, for each temperature of the stage T_{stage}. Fig. 2.4 (b) shows R_0 obtained at the five temperature configurations as a function of T_{stage} for the same line width. We extracted the *TCR* from the slope of the R_0 vs T_{stage} graph using,

$$TCR = \frac{Slope(R_0\ vs\ T)}{R_0(294\ K)} \quad (2.2)$$

In combination with the resistance vs power data, we extracted the temperature increase of the lines as a function of the power applied to them as follows,

$$\Delta T_{\text{line}} = \frac{\frac{R_{\text{line}}}{R_0} - 1}{TCR} \quad (2.3)$$

Fig. 2.4 (c) shows the estimated ΔT_{line} as a function of P_{line} obtained on the results in Fig. 2.4 (a). We conducted these measurements for all of the other line widths. Fig. 2.4 (d) shows the *TCR* of the lines as a function of their line width.

2.2.4 Operation of the SThM calibration

For the thermal measurements, we used a SThM system from Bruker Anasys connected to our AFM system and thermal probes model GLA-1 from Bruker. These probes consist of a thin Pd resistor on top of a SiN film. The tip radius is around 100 nm. During the measurements, the thermoresistive probe was connected to a Wheatstone bridge**.** This electrical network consists of two fixed resistances with R = 1 kΩ, the resistance of the probe R_{probe} and an adjustable potentiometer resistance R_{pot}. In operation we apply a voltage V_{source} across the Wheatstone bridge to induce a small current that allows us to monitor changes in the electrical resistance of the probe. Given the thermoresistive nature of our probes an increase in the probe temperature results in an increment of the resistance of the probe.[1] In contact with the surface, we adjust R_{pot} to be equal to R_{probe}, balancing the bridge. In this configuration, the nullified bridge voltage, which we refer to as SThM signal V_{SThM}, is approximately proportional to the change in R_{probe} and allows changes in probe temperature to be sensed as the probe scans over the sample.

Fig. 2.5 (a) shows a flattened 2D SThM plot obtained when scanning a non-

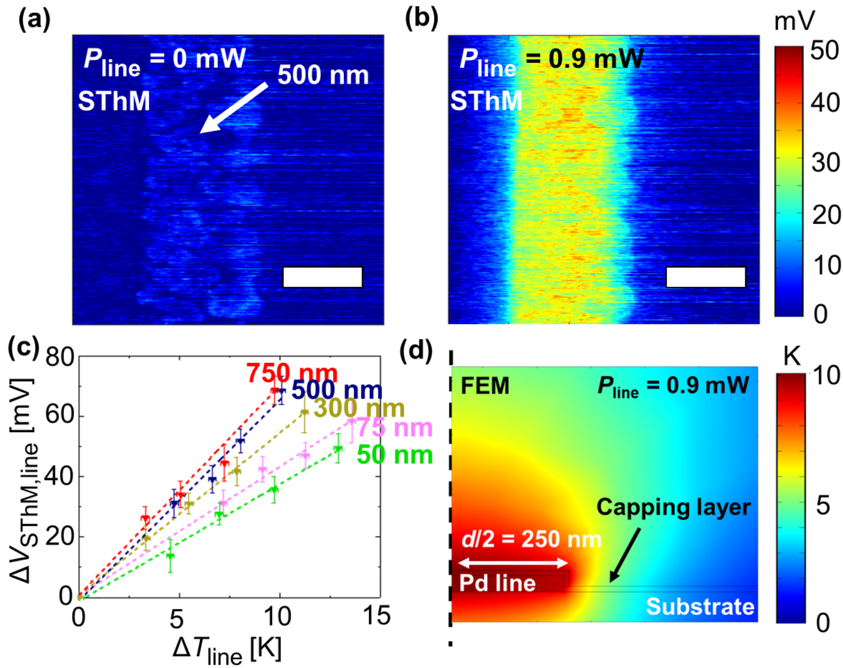

Figure 2.5 (a,b) SThM maps of a 500 nm wide line at **(a)** 0 W, **(b)** 0.9 mW power applied, scanned while a voltage of 0.5 V is applied at the Wheatstone bridge (scale bar equal to 500 nm). Variations observed at the line in the non-heated case are originated by differences in the tip-surface interaction. **(c)** Changes of the SThM signal ($\Delta V_{SThM,line}$) measured at a heated line as a function of the temperature increase (ΔT_{line}) respect to the non-heated case for different widths. **(d)** FEM results for the heating of a 500 nm wide line at an applied power of 0.9 mW. The dashed line at the left edge indicates the plane of symmetry.

heated metal line with a width of 500 nm. As expected, the SThM signal remained constant along the scan, with minor topography related differences at the line as consequence of tip-surface interaction changes.[32] In Fig. 2.5 (b) we show a flattened 2D SThM plot of the same line when heating the line by applying an electrical power P_{line} of 0.9 mW. In this case we observed a significant increment of the SThM signal at the location of the heated metal line.

For the purpose of a better illustration, we applied a 0 order flattening on the images in Fig. 2.5 (a) and (b). For the characterization of the *CaF* we used the raw data later. We repeated the measurements while heating the lines at different powers. The magnitude of the signal linearly depends on the heating power and hence on the temperature rise of the line. Fig. 2.5 (c) shows the rise in the SThM signal observed at the line ($\Delta V_{\text{SThM,line}}$) plotted against the corresponding temperature increase of the line during the measurements (ΔT_{line}) for various line widths. ΔT_{line} was obtained from the 4-point probe measurements. To subtract the influence of the topography on our results, we determined $\Delta V_{\text{SThM,line}}$ at ΔT_{line} as the difference of the maximum SThM signal in the heated case $V_{\text{SThM,max,line}}(\Delta T_{\text{line}})$ vs the maximum SThM signal at the non-heated $V_{\text{SThM,max,line}}(0)$ case as follows:

$$\Delta V_{\text{SThM,line}}(\Delta T_{\text{line}}) = \Delta V_{\text{SThM,max,line}}(\Delta T_{\text{line}}) - \Delta V_{\text{SThM,max,line}}(0) \quad (2.4)$$

From the graphs in Fig. 2.5 (c) we extracted our *CaF* as the slope of the $\Delta V_{\text{SThM,line}}$ vs ΔT_{line} graphs.

Fig. 2.5 (c) presents the $\Delta V_{\text{SThM,line}}$ vs ΔT_{line} behaviour, which increases until it saturates at higher line widths. This behaviour can be explained from the thermal exchange interaction between the tip and sample surface. The heat exchange between the tip and the sample is typically considered as a circular area with a defined thermal exchange radius.[23] The intrinsic thermal exchange diameter around the tip is given by its heat transfer mechanisms (solid-solid, water meniscus, convection, and radiation). Then, when this thermal exchange radius is larger than the width of the line, heat exchange is reduced and the SThM signal drops. As a result, we observed a decrease of the *CaF* below a certain cut-off line width. These results match with previously obtained results.[13] Fig. 2.5 (d) shows the results of a FEM simulation of a 500 nm wider Pd line to verify the results of our electrical characterization.

2.2.5 COMSOL simulation for characterization of the temperature increase

We implemented a finite element method (FEM) model in COMSOL Multiphysics 5.3 to validate the four-point probe measurements. Fig. 2.6 (a) shows the geometry of the developed model structure. For that purpose, we assigned the according material from the COMSOL database to the geometries as illustrated in Fig. 2.6 (a). We choose a lower thermal conductivity for Pd (25 W/(m·K)) and Al_2O_3 (1.5 W/(m·K)) in comparison to

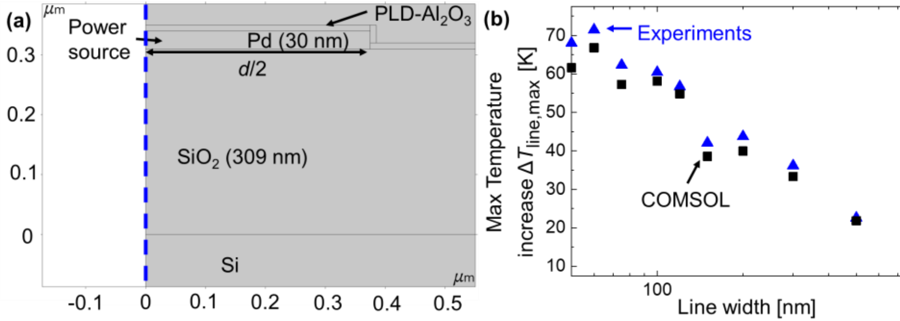

Figure 2.6 (a) Geometry of the COMSOL model; **(b)** Max temperature increase ($\Delta T_{line,max}$) at the line as a function of its line width, the blue triangles and the black squares represent the results of the 4 Point probe measurements and the COMSOL simulation, respectively. The results were obtained at a power applied to the line of 50 nm P_{line} = 2.45 mW, 60 nm P_{line} = 2.77 mW, 75 nm P_{line} = 2.51 mW, 100 nm P_{line} = 2.72 mW, 120 nm P_{line} = 2.76 mW, 150 nm P_{line} = 2.09 mW, 200 nm P_{line} = 2.42 mW, 300 nm P_{line} = 2.4 mW, 500 nm P_{line} = 2.05 mW, 750 nm P_{line} = 2.35 mW.

their bulk values to take the effect of nanoscale confinement into account. We varied the line width of the Pd (*d*) according to the values of our materials e.g., 750 nm in Fig. 2.6 (a). Concerning the computation of the results we employed COMSOL's Heat Transfer in Solids module, which solves the heat equation assuming Fourier's law. The ambient temperature was set to 300 K. For the heating of the structure, we applied a heat source to the Pd line geometry. We used a symmetry function on the left edge of the model.

Fig. 2.6 (b) shows the maximum temperature increase of our measurements as a function of the line width. Here the blue triangles and the black squares represent the outcome of the four-point probe measurements and the COMSOL simulation, respectively. Therefore, we extracted the maximum temperature increase computed at the Pd line while applying the same power density magnitudes as in the measurements of each line indicated in the caption. The results in Fig. 2.6 (b) were estimated at the maximum power values measured during the four-point probe measurements. We concluded that the results of the simulation fit well with the results of the measurements. However, especially at lower line widths the simulated temperature slightly falls below the results of the measurements. This difference results from

changes in thermal conductivity at the lower scale as also due to variability of the real line width. Additionally, we observed that the calculated temperature drop between Pd line and surface on top of the capping layer is well below < 1K.

2.2.6 Estimation of the probe power during the measurement

Since the heat exchange between the probe and the sample changes significantly with the voltage applied to the Wheatstone bridge V_{source}, we further conducted measurements to estimate its impact on the calibration. The larger the power applied to the probe, the higher its temperature during the scan. Aiming to evaluate the impact of the probe heating on *CaF*, we conducted the same $\Delta V_{SThM,line}$ vs ΔT_{line} analysis for four different Wheatstone bridge voltages (V_{source} = 0.1, 0.3, 0.5 and 0.7 V). However, V_{source} is difficult to compare between different probes as it depends on the resistance of the

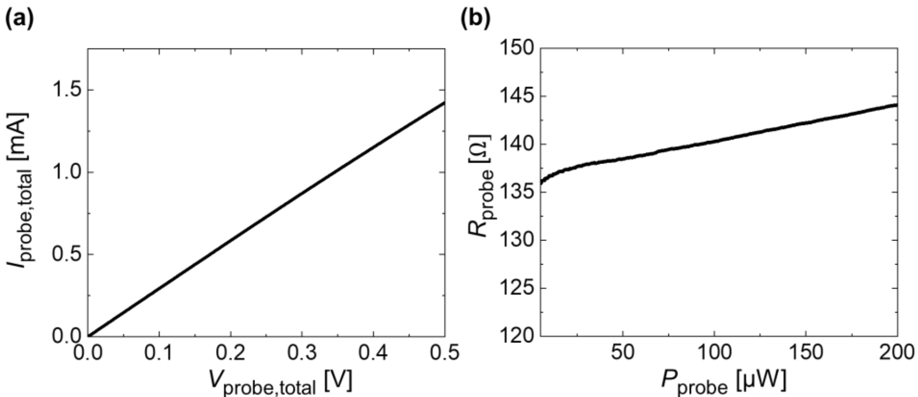

Figure 2.7 (a) Electrical current measured at probe ($I_{probe,total}$) as a function of the voltage applied to it ($V_{probe,total}$) **(b)** Resistance of the SThM probe (R_{probe}) plotted against the electrical power applied to it (P_{probe}).

probe. Thus, we measured the total resistance $R_{probe,total}$ = 340 Ω of the probe by measuring its *I-V* behavior. Based on that, we estimated the power applied to the probe $P_{probe.}$

To estimate P_{probe}, we measured the resistance of the probe externally by measuring its *R* vs *P* characteristics with the Keithley semiconductor parameter analyzer (SPA). Fig. 2.7 (a) shows the measured electrical current of the whole probe $I_{probe,total}$ as a function of the applied voltage $V_{probe,total}$. The total resistance includes the thermo-resistive element but also two current limiters. We measured the resistance of the current limiters externally to be

$R_{current\text{-}limiter}$ = 203.6 Ω in total (~102 Ω each). The resistance of the probe R_{probe} was calculated as follows,

$$R_{\text{probe}} = R_{\text{probe,total}} - R_{\text{current-limiter}} \tag{2.5}$$

We calculated $R_{probe,total}$ by means of the I vs V results displayed in Fig. 2.7 (a). Fig. 2.7 (b) shows the from equation 2.5 resulting R_{probe} plotted against the electrical power applied to the probe P_{probe}. From that we can extract the resistance of the probe at zero power to be $R_{probe}(0) \approx 136.6\ \Omega$.

The Wheatstone bridge is a parallel resistance. We calculated the divided voltage at the probe resistance as follows:

$$V_{\text{probe}} = V_{\text{source}} \cdot \frac{R_{\text{probe}}}{R + R_{\text{current-limiter}} + R_{\text{probe}}} \tag{2.6}$$

Subsequently, we estimated the power of the probe by using the following equation:

$$P_{\text{probe}} = \frac{V_{\text{probe}}^2}{R_{\text{probe}}} \tag{2.7}$$

As a consequence, we obtained the power values of the probe P_{probe} = 0.8; 7; 19; 37 μW for the four V_{source} configurations. As can be seen from Fig. 2.7 (b) the changes of R_{probe} are moderate in the range of applied power. Hence, we can expect that the impact of the temperature dependency of R_{probe} on $P_{probe} < 1\%$.

2.2.7 Estimation of the temperature of the probe utilizing null-point method (NPM) measurements

The higher probe power applied to the tip during scans results in a higher probe temperature. In order to verify that, we applied the NPM to estimate the temperature of the probe as a function of P_{probe}. The NPM is based on the quantification of the probe temperature in contact with the sample (T_c) vs the temperature of the probe in non-contact mode (T_{nc}).[33–35] In non-contact mode, the heat transfer between the tip and the sample (Q_{ts}) is assumed to be 0. Essentially, the temperature of the tip in contact T_c is equal to the temperature of the sample (T_s) when T_{nc} is equal to T_c.[33] To apply this method to our SThM system we used the logger option of the corresponding SThM software. This option allows to record the SThM signal of the Wheatstone bridge in operando.

Fig. 2.8 (a,b) show the logger signal (V_{logger}) as a function of the run time (t_{np}) without and with AFM laser on during the measurement. First, we tracked the

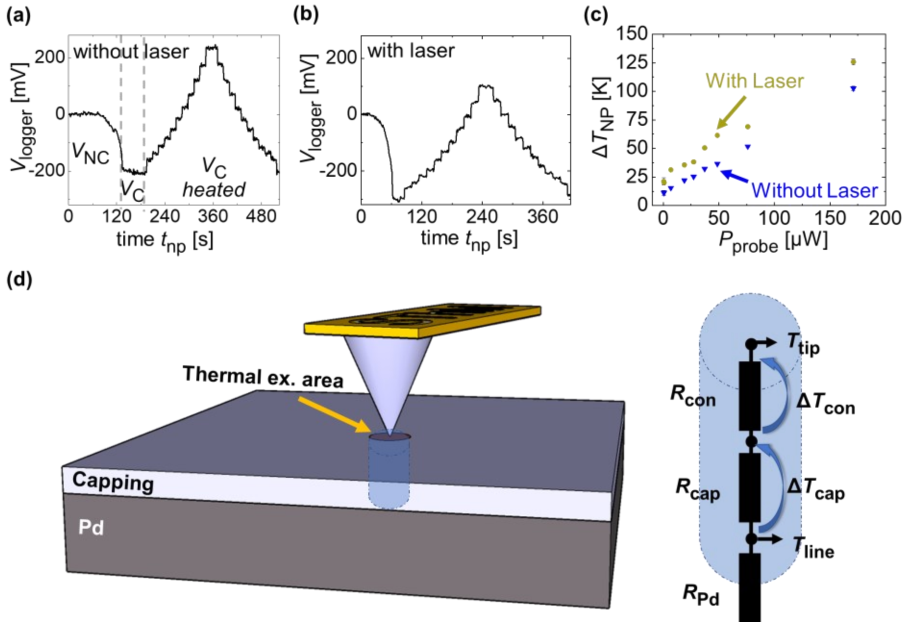

Figure 2.8 (a,b) Recorded logger SThM signal V_{logger} of the null-point method estimation as a function of the run time (t_{np}) while the laser is turned **(a)** off and **(b)** on during the measurements (heating power P_{line} = 0.58-5.22 mW) **(c)** Temperature increase of the probe (ΔT_{NP}) estimated by the null-point method (NPM) as a function of the power applied to the probe (P_{probe}). The blue triangles shapes represent the results obtained without AFM laser. The yellow dots show the results with laser during the measurements. The results are obtained at V_{source} = 0.08, 0.1, 0.3, 0.5, 0.6, 0.7, 0.8, 1, 1.5 V. The corresponding power values are calculated as described in section 2.2.6 **(d)** Schematic view of the 1D heating model applied to analyze the temperature offset of the NPM measurements.

SThM signal in non-contact (V_{NC}) at which we nullified the signal. Second, we contacted the tip to a 750 nm wide Pd line, lowering the SThM signal V_C as a consequence of the tip to sample heat dissipation. Third, we heated the Pd line steadily to increase the SThM signal again. At one point the SThM signal reached its initial value close to zero i.e., $T_{nc} \approx T_c$ (i.e., $V_{nc} \approx V_c$). Finally, we extracted T_c, ΔT_{NP} as the temperature of the sample at which this condition becomes true. We repeated these measurements for seven values of P_{probe} and for two cases with the AFM laser on and with the AFM laser off.

Fig. 2.8 (c) shows the estimated increase of the probe temperature ΔT_{NP} plotted against the power applied to the probe P_{probe} with and without laser. As expected ΔT_{NP} rises linearly with P_{probe} in both cases. Here, we observed a significant difference between ΔT_{NP} with and without laser. The laser heats the probe during the scan up to 25 K more than without the laser. This difference becomes relevant in measurements in which a self-heating of the sample should be avoided. However, the laser is required for the topographic analysis so in most of the cases the measurement with a laser would be the preferred option. In our case, we needed to use the AFM laser to scan the calibration samples, as this is a necessary element for scanning. However, the laser does not affect the relative changes during measurements, as we observed similar slopes in Fig. 2.8 (c) for both cases. We have measured the samples with the laser on with the effect of having a more elevated background temperature compared to the non-laser case. To reduce the background heating due to laser, one could use different approaches like less laser power or lasers that focus more locally on the tip cantilever. Finally, it is worth noting that ΔT_{NP} does not fall to zero at zero power even without the laser. Here we must mention that the heat transport between the probe and sample is overly complex. Besides the tip-to-sample conduction other parameters must be considered when comparing the non-contact with the contact temperature as heat radiation, thermal contact, or water meniscus.

Fig. 2.8 (d) shows the schematic of a 1D temperature model, which we applied for the characterization of the impact of the contact resistance on the NPM results. Therefore, we approximated the imaginary power $P_{line} \approx 1.27$ mW that we would need to apply to heat the Pd line (line width of 750 nm) to the near zero power temperature of the line $T_{line} \approx 311.2$ K (based on Fig. 2.8 (c) without laser). By using the COMSOL model described in section 2.2.5 we calculated the temperature drop across the capping layer $\Delta T_{cap} \approx 10$ mK. Subsequently, we estimated the resistance of the capping layer $R_{cap} \approx 53000$ K/W on base of a cylindrical shape across the capping layer with a radius $r_{\text{thermal exchange}} \approx 200$ nm approximately equal to the thermal exchange radius of the tip-sample contact as follows:

$$R_{\text{cap}} = \frac{x}{k \cdot A} \tag{2.8}$$

The thickness $x = 10$ nm, thermal conductivity $k = 1.5$ W/(m·K) and the area $A = \boldsymbol{\pi} \cdot (r_{\text{thermal exchange}})^2$ of the capping layer is equal to the values of the simulation. Based on that we can calculate the heating power across the capping layer $P_{cap} = 0.18$ µW as follows:

$$P_{\mathrm{cap}} = \frac{\Delta T_{\mathrm{cap}}}{R_{\mathrm{cap}}} \tag{2.9}$$

We then considered an equal power across the thermal exchange resistance between probe tip and sample (R_{con}) of the same thermal exchange area. From the literature we estimated R_{con} to have a magnitude of around $4\cdot10^6$ K/W.[23,36] By means of that we calculated the estimated temperature drop across thermal exchange resistance (ΔT_{con}) in this way:

$$\Delta T_{\mathrm{con}} = P_{\mathrm{c}} \cdot R_{\mathrm{con}} \tag{2.10}$$

By using R_{con} from the literature we obtained a ΔT_{con} of 0.75 K. By assuming a thermal exchange resistance of one order of magnitude higher than in literature we would obtain a ΔT_{con} of 7.5 K. Considering the large error of ΔT_{NP} at low power we would obtain the tip temperature (T_{tip}) to be close to 0, due to the temperature drop across the thermal exchange resistance. According to our estimated ΔT_{NP} offset close to zero power, R_{con} should be estimated within a range of $4\cdot10^6$ and $4\cdot10^7$ K/W. This result is reasonable as R_{con} can vary significantly in between probes. Additional differences are based on the other heat exchange mechanisms between tip and sample as water meniscus or heat radiation.

2.3 Results

2.3.1 Estimation of the *CaF*

Fig. 2.9 (a-d) show four different flattened SThM thermal maps of the same metal line width of 500 nm. The same power was applied to the line for the different SThM scans, achieving a ΔT_{line} of 10 K. However, we varied the power magnitude of P_{probe} as seen in Fig. 2.9 (a-d) and stated in the figure caption, i.e., from 0.8 to 37 µW. By comparing the four figures we observed that the contrast at the line increases with P_{probe}. In other words, we see a clear contrast between the line signal and the substrate signal in Fig. 2.9 (d), while the line signal is less distinguishable in Fig. 2.9 (a). The same measurements were conducted for each line width and at four different power values to determine the corresponding *CaF*. (see section 2.7.1 for details).

At this point it is worth noting that we calculated the *CaF* by means of the difference of the raw signal at the heated line and the raw signal of the line in a non-heated reference scan (see section 2.7.2 for details). By using this approach, we were able to plot the *CaF* as a function of the line width for all the four configurations described above in Fig. 2.9 (e). We verified our results

by conducting our measurements with a second probe. Furthermore, we observed that the *CaF* keeps on increasing when applying P_{probe} values beyond the configurations displayed here.

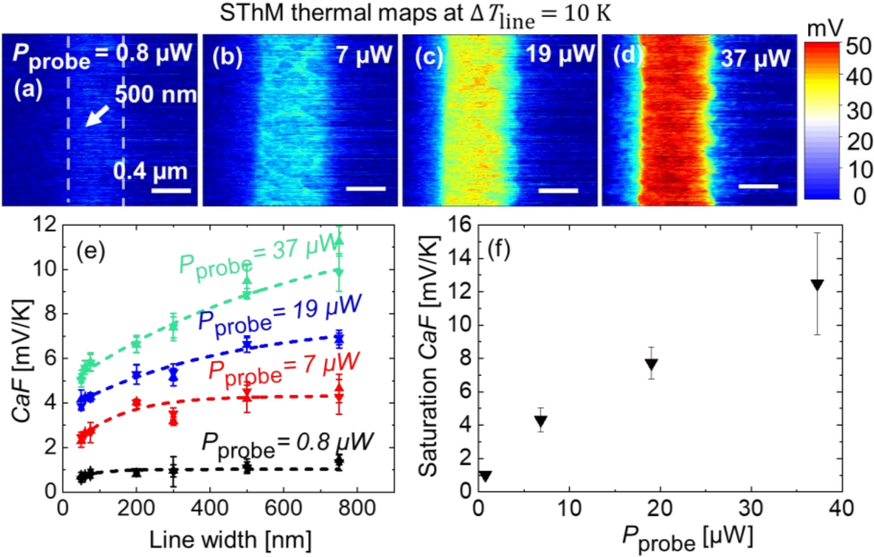

Figure 2.9 (a-d) SThM thermal maps of a 500 nm wide metal line at ΔT_{line} = 10 K when scanning at a probe power (P_{probe}) of **(a)** 0.8 μW, **(b)** 7 μW, **(c)** 19 μW, **(d)** 37 μW (scale bar equal to 400 nm). **(e)** Calculated calibration factor (*CaF*) for different power values as a function of the line width of the scanned metal lines (upwards triangle correspond to the trace signal, downwards triangle correspond to the retrace signal). **(f)** Estimated saturated *CaF* as a function of P_{probe}.

2.3.2 Comparison of the results with a second probe

We repeated the same measurement procedure as described above for a second probe. Fig. 2.10 shows the results of the calibration factor (*CaF)* as a function of the line width of the Pd for both probes. The results of the two tips match well, especially at higher line widths. In both cases, we observed an increase of the temperature sensitivity as well as a shift of the line cut-off width with P_{probe}. At lower line widths we observed a stronger decay of the calibration factor for the second tip. The lower values at the smaller line widths indicate a decreased contact between the tip and the line which might originate from a blunter tip shape of the second probe.

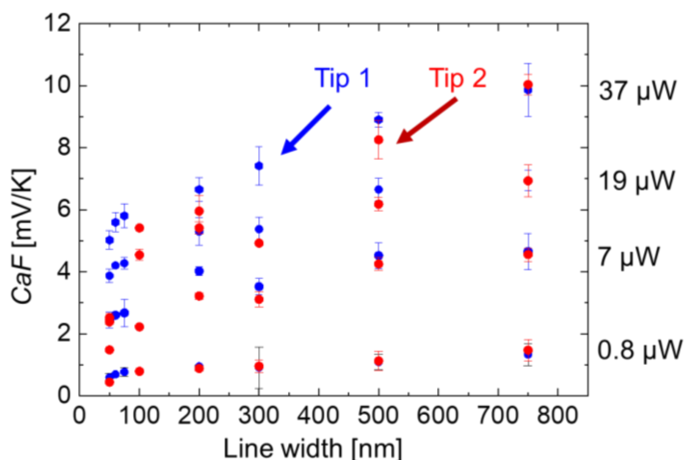

Figure 2.10 Calculated calibration factor (*CaF*) for different power values P_{probe} (0.8, 7, 19, 37 μW) as a function of the line width of the scanned metal lines obtained from the retrace signal. The blue dots correspond to the results obtained from the first tip displayed in Fig. 2.9. The red dots present results obtained on a second reference tip.

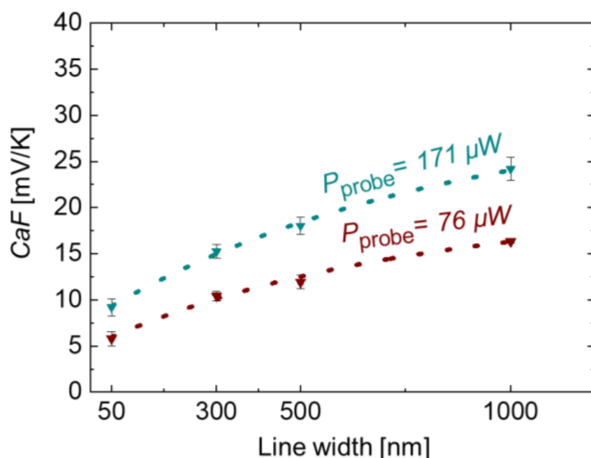

Figure 2.11 Calculated calibration factor (*CaF*) for different power values P_{probe} (76, 171 μW) as a function of the line width of the scanned metal lines obtained from the retrace signal. The results are obtained at a Wheatstone bridge voltage V_{source} of 1 V and 1.5 V. The corresponding power values are calculated as demonstrated in section 2.2.6.

2.3.3 Calibration factor at high power

All the results displayed in the previous chapters are obtained at lower V_{source} values which is common for the operation of the SThM in sensing mode. Fig. 2.11 shows the *CaF* as a function of the line width obtained at higher power (V_{source} of 1 V and 1.5 V). The results show that the maximum *CaF* further increases with P_{probe}. For application, one must consider that the sample itself heats up significantly at these higher power values which might affect the measuring characteristics significantly. The aim of this study was to characterize the SThM calibration factor at low power values for sensing. If one would like to operate the SThM for sensing at higher power values, additional characterizations would be required. Nevertheless, the results in Fig. 2.11 show a preliminary trend for these power configurations.

2.4 Discussion and SThM application to measure electronic devices

Based on the results shown in Fig. 2.9, we observed an increase of *CaF* as a function of P_{probe}. The increment of P_{probe} is a result of pushing higher currents I_{probe} through the probe because of increasing V_{source}. I_{probe} directly impacts the slope of the ΔV_{SThM} vs ΔT_{probe} ($V_{SThM} = I_{probe} \cdot R_{probe}$) function. As a result of that we should expect a stronger increase in V_{SThM} for the same temperature increase when operating at a higher current. Apart from that applying more power to the tip results in a higher probe temperature. This is confirmed by the linear increase of the probe temperature with P_{probe} independent of the heating of the line as demonstrated with the NPM. The increment of heating power and probe temperature causes an increase of the cut-off line width at which the *CaF* started to saturate at higher P_{probe}, as can be seen in Fig. 2.9 (e). The cut-off line width tells us about the size at which the heat transport between probe and sample starts to truncate and is therefore an indicator of the thermal exchange area. As we increased the power applied to the tip, we consequently increase the thermal exchange area around the tip vicinity. We fitted the data in Fig. 2.9 (e) graphs with a simple exponential function to estimate the saturation value of *CaF* as drawn by the dotted lines. For higher power values the fit saturates at line widths above 750 nm Fig. 2.9 (f) shows the saturation *CaF* values as a function of P_{probe}, showing a steady trend.

This new information enlarges the toolkit of operating a calibrated SThM system. Depending on the needs of the measurement the bridge power can be adjusted. For example, one could choose to operate the SThM at a higher

power to increase the temperature sensitivity. However, at lower power one obtains less self-heating of the probe and therefore could be the preferred option in other cases.

2.4.1 Validation of calibration

Finally, to verify the results of the calibration, we assessed *CaF* in electronic devices. We investigated the heating characteristics of a phase change material (PCM) device which we characterized in a previous study.[37] Fig. 2.12 (a) shows the sample schematics revealing the PCM sputtered on a 1.5 µm wide metal heater line. We capped the surface of the PCM sample with a thin insulation layer of SiO_2 to electrically isolate the tip from the sample. We scanned the sample surface with our SThM probes while heating the metal line by applying an electrical current between the two heater pads. We repeated the measurements for four power configurations. The applied current and voltage at the metal lines as a function of the run time of the steady state measurements is shown in Fig. 2.12 (b). The finite element model of the PCM structure was reported previously[37,38] to determine the

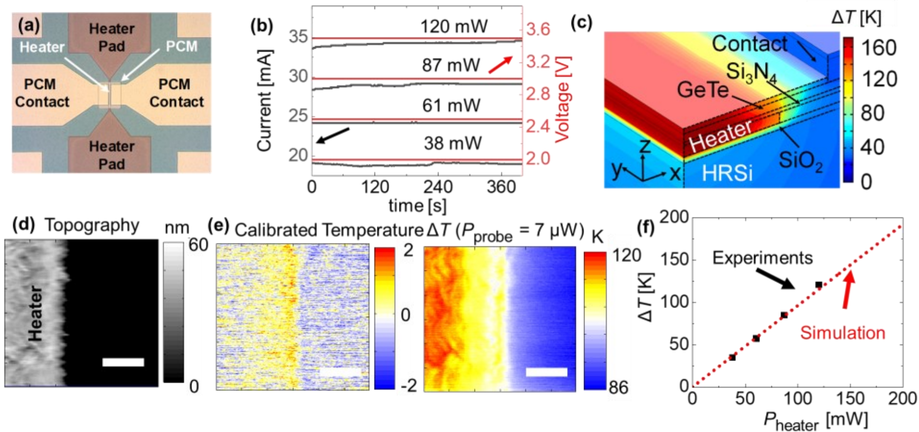

Figure 2.12 (a) Setup of the PCM sample. **(b)** Applied current and measured voltage as a function of the measurement time. **(c)** FEM simulation of the measured sample. **(d)** Topography of the investigated PCM sample obtained with a SThM probe. **(e)** Calibrated temperature maps of the PCM sample without and with power applied and for a power applied to the probe of P_{probe} = 7 µW (scale bar of **(d)** and **(e)** equal to 400 nm). **(f)** Calculated temperature increase at the line obtained with FEM as illustrated from **(c)** and from experiments, using the *CaF* obtained in Fig. 2.9.

value of the temperature of the device based on the power applied. The model considers the thermal conductivity and capacitance of each layer, including the thermal boundary resistance of the interfaces as well as the temperature coefficient of resistance of the heater.

In this FEM, illustrated in Fig. 2.12 (c) the structure of the device was replicated, and a power source was applied to the heater. We calculated the surface temperature to compare them with the calibrated temperature maps obtained with SThM. As an example, the topography and converted temperature maps of one of the heater lines are presented in Fig. 2.12 (d) through (e). Fig. 2.12 (e) displays converted SThM temperature maps obtained with 0 W and 120 mW applied to the device during the scan, respectively. As expected, the maximum temperature is observed towards the center of the heater line area. We converted the signal as described above by determining the difference of the raw SThM signal in the heated vs the non-heated case.

During the scan we applied a power of 7 µW to the probe. The line width significantly exceeded the cut off value of this power configuration. Therefore, we used the saturation *CaF* = 4.31 mV/K of this power configuration as shown in Fig. 2.9 (e). We then calculated the expected temperature increase of the lines with four different power configurations (see Fig. 2.12 (b)). Fig. 2.12 (f) shows the maximum temperature increase of the heater area vs the power applied to the lines. It can be observed that, the results obtained by the calibrated SThM (represented by the black squares) and the results of the FEM simulation illustrated by the red dotted line,[37] are in good agreement. Hence, it can be concluded that this calibrated SThM approach is a promising technique to characterize the temperature of different samples and devices with nanoscale accuracy. A potential source of error might originate because of differences in the probe to sample contact between calibration sample and device due to capping layer. However, the capping layer of SiO_2 and Al_2O_3 present similar surface roughness and thermal conductivities. Therefore, we estimate that this difference is bound to be less than 3%, which agrees well with the analysis of the temperature increase of the PCM sample.

2.5 Conclusions

In conclusion, in this chapter we determined the calibration factor of a thermo-resistive SThM probe using a set of metal lines with different widths

and power applied to them. We determined that the calibration factor depends on the thermal exchange area between the tip and the sample as well as with the power applied to the probe. This calibration method enables adjustable SThM measurement to quantify the heating at the surface of a sample depending on the needed thermal sensitivity and local features of the heating surface. Therefore, the outcome of this work displays the advantages and disadvantages of operating the SThM at different bridge power values. For example, one could prefer to operate the SThM at a higher power to increase the thermal contrast of the measurements. On the other hand, one could operate at a lower power to avoid heating of the sample due to the probe. Moreover, the validation of the calibration results shows that this method can be applied for the characterization of similar structures. Therefore, the results showed the flexibility of the SThM to conduct temperature mapping for a wide range of materials and devices with nanoscale spatial resolution. This technique sheds light on how to carefully calibrate and use SThM for accurate surface thermal sensing. Future studies should put emphasis on investigating the impact of material specific properties such as the surface roughness, probe thermal contact resistance or thermal conductance on the thermal exchange between the probe and sample.

2.6 References

1 Y. Zhang, W. Zhu, F. Hui, M. Lanza, T. Borca-Tasciuc and M. Muñoz Rojo, *Adv. Funct. Mater.*, 2020, **30**, 1900892.

2 S. Gomès, A. Assy and P.-O. Chapuis, *Phys. Status Solidi*, 2015, **212**, 477.

3 K. Kim, W. Jeong, W. Lee and P. Reddy, *ACS Nano*, 2012, **6**, 4248–4257.

4 M. Muñoz Rojo, J. Martín, S. Grauby, T. Borca-Tasciuc, S. Dilhaire and M. Martin-Gonzalez, *Nanoscale*, 2014, **6**, 7858–7865.

5 Q. Zhu, J. Liu, Y. Lin, S. Xie and J. Li, *Appl. Phys. Lett.*, 2020, **117**, 133102.

6 E. N. Esfahani, F. Ma, S. Wang, Y. Ou, J. Yang and J. Li, *Natl. Sci. Rev.*, 2018, **5**, 59–69.

7 J. L. Bosse, M. Timofeeva, P. D. Tovee, B. J. Robinson, B. D. Huey and O. V. Kolosov, *J. Appl. Phys.*, 2014, **116**, 134904.

8 T. Luo and G. Chen, *Phys. Chem. Chem. Phys.*, 2013, **15**, 3389–3412.

9 F. Menges, P. Mensch, H. Schmid, H. Riel, A. Stemmer and B. Gotsmann, *Nat. Commun.*, 2016, **7**, 10874.

10 E. Pop, *Nano Res.*, 2010, **3**, 147–169.

11 E. Yalon, C. J. McClellan, K. K. H. Smithe, M. Muñoz Rojo, R. L. Xu, S. V. Suryavanshi, A. J. Gabourie, C. M. Neumann, F. Xiong, A. B. Farimani and E. Pop, *Nano Lett.*, 2017, **17**, 3429–3433.

12 I. M. Datye, M. Muñoz Rojo, E. Yalon, S. Deshmukh, M. J. Mleczko and E. Pop, *Nano Lett.*, 2020, **20**, 1461–1467.

13 S. Deshmukh, M. Muñoz Rojo, E. Yalon, S. Vaziri, Ç. Köroğlu, R. Islam, R. A. Iglesias, K. Saraswat and E. Pop, *Sci. Adv.*, 2022, **8**, eabk1514.

14 S. K. Nandi, E. Puyoo, S. K. Nath, D. Albertini, N. Baboux, S. K. Das, T. Ratcliff and R. G. Elliman, *ACS Appl. Mater. Interfaces*, 2022, **14**, 29025–29031.

15 E. Yalon, S. Deshmukh, M. Muñoz Rojo, F. Lian, C. M. Neumann, F. Xiong and E. Pop, *Sci. Rep.*, 2017, **7**, 15360.

16 S. M. Bohaichuk, M. Muñoz Rojo, G. Pitner, C. J. McClellan, F. Lian, J. Li, J. Jeong, M. G. Samant, S. S. P. Parkin, H. S. P. Wong and E. Pop, *ACS Nano*, 2019, **13**, 11070–11077.

17 A. L. Moore and L. Shi, *Mater. Today*, 2014, **17**, 163–174.

18 P. K. Schelling, L. Shi and K. E. Goodson, *Mater. Today*, 2005, **8**, 30–35.

19 K. Luo, Z. Shi, J. Lai and A. Majumdar, *Appl. Phys. Lett.*, 1996, **68**, 325.

20 O. Nakabeppu, M. Chandrachood, Y. Wu, J. Lai and A. Majumdar, *Appl. Phys. Lett.*, 1995, **66**, 694.

21 T. Dinh, H. P. Phan, A. Qamar, P. Woodfield, N. T. Nguyen and D. V. Dao, *J. Microelectromechanical Syst.*, 2017, **26**, 966–986.

22 E. Puyoo, S. Grauby, J. M. Rampnoux, E. Rouvìre and S. Dilhaire, *Rev. Sci. Instrum.*, 2010, **81**, 073701.

23 E. Puyoo, S. Grauby, J. M. Rampnoux, E. Rouvìre and S. Dilhaire, *J. Appl. Phys.*, 2011, **109**, 024302.

24 N. Barbosa and A. J. Slifka, *Microsc. Res. Tech.*, 2008, **71**, 579–584.

25 D. Shan, K. Pan, Y. Liu and J. Li, *Nano Energy*, 2020, **67**, 104203.

26 G. Wielgoszewski, M. Babij, R. F. Szeloch and T. Gotszalk, *Sensors Actuators, A Phys.*, 2014, **214**, 1–6.

27 Y. Zhang, W. Zhu, L. Han and T. Borca-Tasciuc, *Rev. Sci. Instrum.*, 2020, **91**, 014901.

28 S. Deshmukh, M. Muñoz Rojo, E. Yalon, S. Vaziri and E. Pop, *Probing Self-Heating in RRAM Devices by Sub-100 nm Spatially Resolved Thermometry*, IEEE, 2018.

29 M. Muñoz Rojo, Z. Li, C. Sievers, A. C. Bornstein, E. Yalon, S. Deshmukh, S. Vaziri, M. H. Bae, F. Xiong, D. Donadio and E. Pop, *2D Mater.*, 2019, **6**, 011005.

30 R. L. Xu, M. Munõz Rojo, S. M. Islam, A. Sood, B. Vareskic, A. Katre, N. Mingo, K. E. Goodson, H. G. Xing, D. Jena and E. Pop, *J. Appl. Phys.*, 2019, **126**, 185105.

31 J. T. W. Kuo, L. Yu and E. Meng, *Micromachines*, 2012, **3**, 550–573.

32 J. Spiece, C. Evangeli, K. Lulla, A. Robson, B. Robinson and O. Kolosov, *J. Appl. Phys.*, 2018, **124**, 015101.

33 J. Chung, K. Kim, G. Hwang, O. Kwon, Y. K. Choi and J. S. Lee, *Int. J. Therm. Sci.*, 2012, **62**, 109–113.

34 G. Hwang, J. Chung and O. Kwon, *Rev. Sci. Instrum.*, 2014, **85**, 114901.

35 D. G. Cahill, W. K. Ford, K. E. Goodson, G. D. Mahan, A. Majumdar, H. J. Maris, R. Merlin and S. R. Phillpot, *J. Appl. Phys.*, 2003, **93**, 793–818.

36 Y. Zhang, W. Zhu, F. Hui, M. Lanza, T. Borca-Tasciuc and M. Muñoz Rojo, *Adv. Funct. Mater.*, 2020, 30, 1900892.

37 N. Wainstein, G. Ankonina, T. Swoboda, M. Muñoz Rojo, S. Kvatinsky and E. Yalon, *IEEE Trans. Electron Devices*, 2021, **68**, 1298–1303.

38 N. Wainstein, G. Ankonina, S. Kvatinsky and E. Yalon, *IEEE Trans. Electron Devices*, 2020, **67**, 5182–5187.

39 C. Metzke, W. Frammelsberger, J. Weber, F. Kühnel, K. Zhu, M. Lanza, G. Benstetter, *Materials.*, 2020, **13**, 518.

2.7 Appendix

2.7.1 SThM measurements

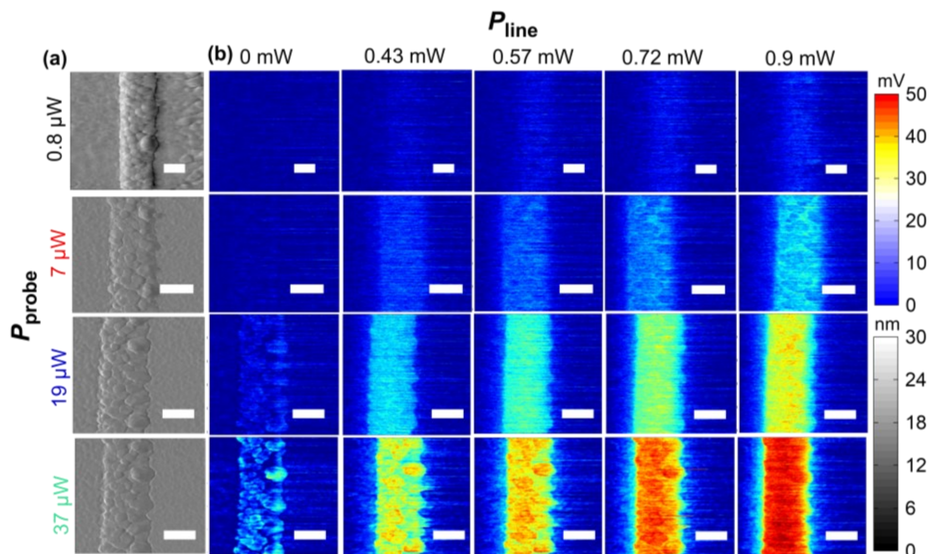

Figure 2.13 (a) Flattened topography images obtained on a 500 nm wide Pd metal line for the four different P_{probe} configurations, **(b)** Flattened SThM thermal maps created by means of SThM on a 500 nm wide Pd line at different power values applied to it (P_{line}), for the four configurations of P_{probe}. (scale bar 500 nm).

For the thermal characterization, we adjusted the potentiometer of the biased Wheatstone bridge in order that $R_{pot} \approx R_{probe}$ after bringing the probe in contact with the sample surface. Subsequently we scanned the Pd lines of all line widths with the prior described SThM probes connected to the nullified Wheatstone bridge. Fig. 2.13 (a) shows the flattened topography images of a 500 nm wide line obtained at the four power configurations. We flattened the images by subtracting the average value from each line. During the scans we applied an electrical current along the metal lines to heat the line. We used the SPA and the probe station of our AFM system to induce the current. Fig. 2.13 (b) shows flattened SThM thermal maps obtained on the same 500 nm wide line as in (a) at zero power, and at four different power magnitudes applied to the lines during measurements.

The SThM probe heats up once it scans over a feature of higher temperature. In this case the heated line increases its electrical resistance. Hence, we used the SThM probe as a thermal sensor that correlates a temperature increase with an increment of the SThM signal across the bridge induced due to changes in the probe resistance. As a consequence, the SThM signal obtained in Fig. 2.13 (b) at the line increases with the power applied to the line. Additionally, we observed that the SThM signal sensitivity improved as a function of the power applied to the probe P_{probe}. We flattened the images so that the left and right edges approximate a signal change of zero. However, by that, remaining heat at the edges is excluded. Hence, we used the raw data to determine the calibration factor as explained in the following section. It is worth mentioning that we observed significant changes in the line signal at zero power at higher P_{probe} values. At the increased power the probe started to heat significantly. Therefore, heat dissipated from the probe to the surface. The magnitude of heat dissipation depends on the thermal resistance of the material resulting in a difference of the signal from the line to the surrounding. To take that into account we calculated the signal difference from the heated vs non-heated case at the line as explained below.

2.7.2 Conversion of SThM signal into temperature signal

For the estimation of the calibration factor, we calculated the SThM signal difference between the heated maps and a reference map at zero power. Therefore, we used the raw SThM signal at the line to take the overall temperature increase of the maps into account. Fig. 2.14 (a) shows the raw SThM signal V_{SThM} obtained at a 500 nm wide line in a heated (red) vs a non-heated case (blue). The change in the thermal resistance of the SThM probe due to nearby topography features causes artifacts in the form of a non-zero SThM signal on the non-heated metal line. Moreover, the general temperature increase causes an elevated signal at the edges of the heated metal line. To determine SThM signals corresponding to the metal line temperatures with minimal influence of topography, we first calculated the maximum signal of each of the scan line $V_{SThM,max,line,n}(T)$. Then we extracted the mean of each line to consider the variation in between each scan line.

Finally, we calculated $\Delta V_{SThM,line}$ between the heated and non-heated case as described in the chapter 2.2 in equation 2.4. Fig. 2.14 (b) shows $\Delta V_{SThM,line}$ of the 500 nm line width as a function of the temperature of the lines during the scan for the four P_{probe} configurations. Here we can see an increase of the *CaF* calculated as the slope of the $\Delta V_{SThM,line}$ vs ΔT_{line} graphs with P_{probe}.

We observed this behavior in the remaining metal line widths, resulting in the differences in the *CaF* vs line width graphs presented in Fig. 2.9 (e).

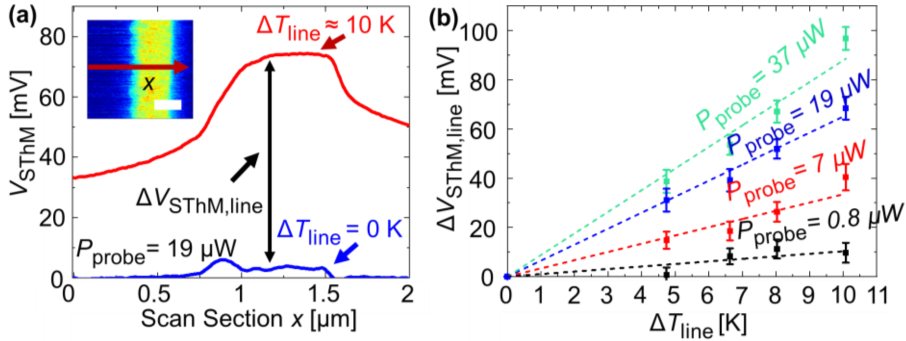

Figure 2.14 (a) SThM raw data thermal signal (V_{SThM}) of a 500 nm wide line obtained at a power applied to the probe (P_{probe}) of 19 μW obtained across the line section *x* (scale bar 500 nm in inset figure). The graphs are obtained while scanning over a non-heated line (blue) and a heated line with a temperature increase of $\Delta T_{line} \approx 10$ K (red). **(b)** SThM signal difference at the metal line ($\Delta V_{SThM,line}$) as a function of the temperature of the line for the four probe configurations at a 500 nm wide line. $\Delta V_{SThM,line}$ is obtained by calculating the difference in the V_{SThM} at the line between the heated vs non-heated case, as illustrated in **(a)**.

In Fig. 2.14 (a), we can observe a slope in the voltage signal for the $\Delta T_{line} \approx$ 10 K. In theory the thermal signal on the right and left side of the heated line should be the same. This is because the figure displays the raw signal, which is affected by measuring artifacts.[39] These effects might result when the tip ramps up vs when the tips ramps down the metal line. One way to check the reason for that and overcome this issue consists of running an additional scan at 180 degree and adjust the steps accordingly. Additionally, using lower scan speed or increasing the measuring points might improve the results. Overall, these additional steps contribute to a proper flattening of the signal, that agrees well with the expected temperature profile.

Chapter 3 Spatially resolved thermometry of filamentary nanoscale hot spots in TiO_2 resistive random access memory devices

Abstract

Resistive random access memories (RRAM) based on the formation and rupture of conductive nanoscale filaments have attracted increased attention for application in neuromorphic computing. However, the development of this technology is limited by its high operation variability that originates partially from the spatial extent and temperature of the filaments. In this study we used scanning thermal microscopy (SThM) to assess the effect of filament-induced heat spreading in metal oxide RRAMs with different device designs. SThM provides dynamic temperature evolution of the filament at the surface of the device that can be compared with its electrical performance. The valuable thermal information provided by SThM, combined with the electrical, interfacial, and geometric characteristics of the device, allowed us to extract insights on the operation and variability of RRAMs. This work suggests new thermal engineering and characterization routes to optimize the efficiency and reliability of these devices.

This chapter is derived from:

T. Swoboda, X. Gao, C. M. M. Rosário, F. Hui, K. Zhu, Y. Yuan, S. Deshmukh, Ç. Köroğlu, E. Pop, M. Lanza, H. Hilgenkamp and M. Muñoz Rojo “Spatially resolved thermometry of filamentary nanoscale hot spots in TiO_2 resistive random access memory devices”, accepted for publication in ACS Applied Electronic Materials.

3.1 Introduction

Resistive switching devices are considered very promising for non-volatile memory and neuromorphic computing.[1–3] In this context, resistive random access memory (RRAM) devices present a high potential due to their low power consumption, high speed and simple device configuration.[4] RRAM devices typically consist of an oxide material sandwiched in a two terminal metal-insulator-metal layered structure.[5] The principle of operation of a RRAM device is based on the formation (set) and breakdown (reset) of a conductive filament in the oxide layer.[6,7] In the last decades, resistive switching has been investigated in a wide variety of metal oxides, like HfO_2[8–10], Ta_2O_5[11,12], or TiO_2.[13–15] Some of the major challenges associated with these devices are related to a lack of reliability in device operation, and storage mechanisms that result in high variability of their electrical performance.[16,17] Understanding the underlying fundamental operation, like filament sizes[18] and positions,[19] current densities[20] and heating[21] is therefore essential for the evaluation, design and optimization of our RRAMs. Different studies have estimated that the diameter of conductive filaments could be below 10 nm.[22,23] This confined conductive region flows large currents that can lead to high power densities >10^{13} W/cm^3.[9] Deshmukh *et al.* [9] determined that these high power densities can result in extremely high temperature increments of >1000 K in HfO_2 memory devices. These elevated temperatures not only reduce the endurance and performance of devices themselves, but it also threatens the lifespan of the electronics in the vicinity because of potential thermal cross-talk. Within this context, thermal management is becoming essential in memory circuits, like those for neuromorphic computing, where controlling temperature variations is needed for efficient and stable data processing.[24] Therefore, further observations and analysis of filamentary induced hot spots in RRAMs remain relevant as they reveal the need for thermal management to achieve optimum, reliable and efficient performance.

Despite the interest in these measurements, the direct observation of filamentary induced hot spots is challenging due to the nanoscale size of the heating. Scanning thermal microscopy (SThM)[25–31] is a scanning probe microscopy (SPM)-based technique. It uses a special temperature sensitive probe with high thermal sensitivity (< 1 K) that enables the characterization of thermal phenomena with nanoscale spatial resolution. SThM has been applied to study the energy dissipation of different devices, like memories

[9,32,33] and PCMs.[27,34] Importantly, the combination of high thermal and spatial resolution makes SThM an ideal tool for analyzing heating in filament-based RRAM devices.[31] As an example, Datye *et al.*[32] employed SThM for surface mapping of the hot spots due to conductive bridges formed in $MoTe_2$ memory devices. Recently, Deshmukh *et al.*[9] imaged the spatial extent and temperature of the filament operation in HfO_x-based RRAMs, assessing the effect of heat spreading on memory operation. Similarly, Nandi *et al.*[33] investigated the temperature distribution in NbO_x based RRAM devices. Additional studies on the fundamental thermal behavior of filamentary memories are essential for gaining further insight on how the switching mechanisms are influenced by geometry, materials, and contacts. This will enable new thermal engineering routes for more efficient and reliable RRAMs.

In this chapter, we use SThM to characterize the localized filamentary heating in TiO_2-based cross-point RRAM devices and connect these observations with device performance and reliability. While previous reports using SThM analysis in memories[9,32,33] focus on the fundamental assessment of filament-induced heat spreading, the evaluation of the memory switching variability by combining electrical and thermal data has not previously been carried out. The analysis of thermal maps obtained by SThM is capable of providing further insights into the cause of device switching variability. We chose TiO_2 as the switching material for the RRAM, given its widespread use for these devices and because it is reliable and is easy to grow, which makes it a good candidate for the characterization of different areas. We observe significant differences in the thermal behavior of devices with two different cross-point areas, i.e., 2×2 μm^2 and 5×5 μm^2, in terms of their *I*-*V* switching variability and the stability of the conductive filament. SThM provides valuable information to evaluate sources for such variations and to suggest routes for optimizing device performance and reducing variability.

3.2 Experimental setup

3.2.1 Synthesis of the RRAM device structure

Fig. 3.1 (a) shows a cross-section schematic of the investigated RRAM structure based on a thin TiO_2/Ti layer (from bottom to top) sandwiched between two gold electrodes. To fabricate this RRAM, we first deposited a thin 10 nm Ti layer for adhesion on top of a SiO_2/Si (300nm) substrate. Second, we used e-beam evaporation to deposit the bottom gold electrode with a thickness of 30 nm. The switching material consists of a TiO_2/Ti bilayer

where each layer has a thickness of 10 nm, deposited by e-beam evaporation (Ti) and atomic layer deposition (TiO_2). A 30 nm thick top Au electrode is evaporated with e-beam. Finally, we covered the whole structure with a 10 nm thick Al_2O_3 capping layer grown by atomic layer deposition (ALD) to electrically insulate the sample. The overview of the device consists of a cross-point structure with contact pad sizes of 100x100 μm^2.

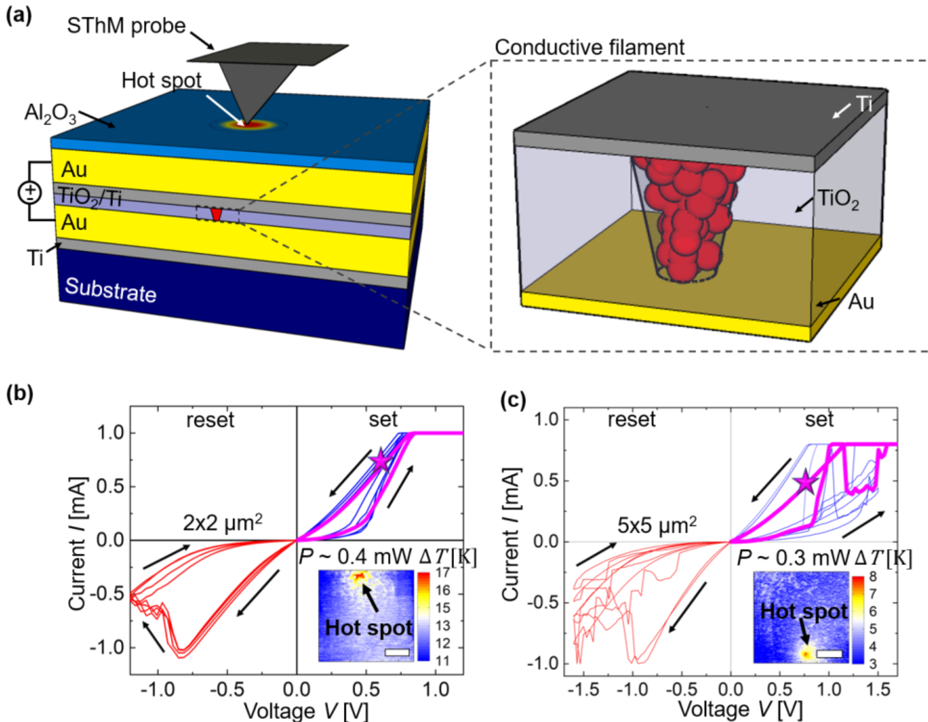

Figure 3.1 Schematic view of the measurement setup that shows the SThM probe on top of the RRAM. The dashed rectangle shows the conductive filament formed in the active TiO_2/Ti layer when applying an electrical bias (*V*). (**b,c**) Measured *I-V* characteristics of the devices for four cycles. The inset figures at the bottom right show the SThM temperature map of the same device at the bias point corresponding to the star symbol. The thermal maps reveal the hot spot generated by the filament for a device area of **(b)** 2x2 μm^2 (scale bar 350 nm) and **(c)** 5x5 μm^2 (scale bar 1 μm).

For the purpose of this study, we fabricated devices with two different areas: 2x2 μm^2 and 5x5 μm^2. The details of the device layers are illustrated in Fig. 3.2. The devices are grown in a cross-point structure with an active area size of 2x2 and 5x5 μm^2.

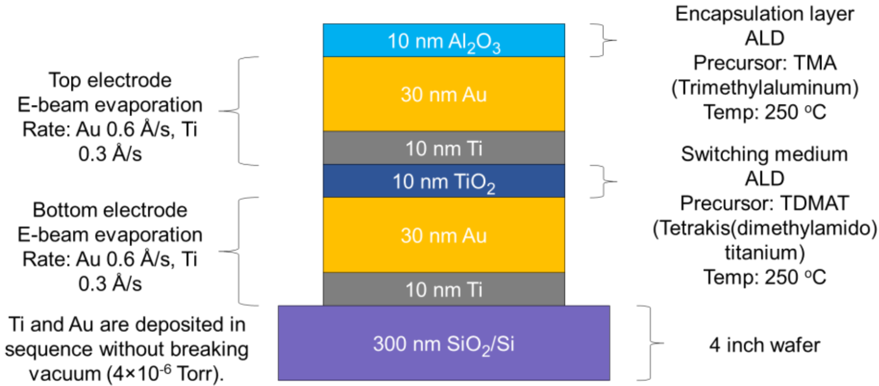

Figure 3.2 Schematic of the fabrication procedure of the investigated samples. The thickness and fabrication method of each layer is indicated in the drawing.

3.2.2 Characterization of the current-voltage characteristics

The filament formation process in metal oxide RRAMs is achieved when applying certain voltage (up to 3 V) to the device, which is associated with the creation of a conductive path that results from the connection of oxygen vacancies.[1] The forming is accompanied by a sharp decrease of the resistance of the device. The filament can be (partially or completely) broken when a sufficiently high reverse bias (-1.5 V < V < -1 V) is applied to the device (reset process), resulting in an increment of resistance. The filament can be re-formed when applying a voltage, lower than during forming (0.5 V < V < 1.5 V), showing the bipolar nature of our devices. The electrical measurements were performed in a probe station connected to a Keithley 4200 A-SCS semiconductor parameter analyzer (SPA) by applying voltage or current bias at room temperature. In pristine TiO_2 RRAMs described above, we formed the filament by applying a positive voltage sweep with an initial current compliance of I_{cc} = 1 μA. After that, we repeated these measurements for ten cycles to ensure cyclability of the devices (examples are presented in section 3.7.1). Fig. 3.1 (b) and (c) show two examples of multiple I-V curves obtained at two devices with an area of (b) 2x2 μm^2 and (c) 5x5 μm^2. In both examples we observed the previously mentioned sharp

increment and decrease of the electrical current during the set and reset processes, respectively. After measuring more than 40 devices both electrically and thermally, we observed a higher cycle-to-cycle variability in the 5x5 μm^2 devices compared to the 2x2 μm^2 ones. Additionally, we observed a higher intrinsic device-to-device variability in the 5x5 μm^2 devices. Both observations are illustrated below.

3.2.3 Device-to-device and cycle-to-cycle variability

One of the major limitations in RRAM devices is connected with this variability of the *I-V* characteristics. Fig. 3.3 (a-f) show *I-V* cycles in six investigated 2x2 μm^2 devices. In all the six devices we observed a relative stable C2C behavior, i.e., the curves of the various cycles matched within the same device. In all the devices we can see a clear trend going from a small slope in the *I-V* curves to a sharp increase at a higher voltage magnitude during the set process. However, these graphs distinguish through the steepness of their slope.

Fig. 3.3 (g-l) show *I-V* cycles in six investigated 5x5 μm^2 devices. On contrary to the 2x2 μm^2 we saw an increased C2C and D2D variability illustrated due to a decay of the current (g), variation of the set voltage and strong reset (h), change of the set slope (i) or by multiple set steps (l). In conclusion we saw a significant difference in the stability of the *I-V* cycle behavior when comparing the 2x2 and the 5x5 μm^2 devices. The different types of set curves of the 5x5 μm^2 devices indicate a non-uniform formation step of the conductive filaments. These results demonstrate the need of thermal characterization of our devices in order to identify the source of the variability in these devices.

It is worth noting that the cycling of the devices can be also operated at lower reset and set voltages than displayed in these figures. When doing so the device switches in between intermediate resistance values. On the one hand one could reduce the severity of full reset processes and therefore reduce the variability. On the other hand, the On/Off ratio in between the set and reset state would be reduced due to the less complete reset.

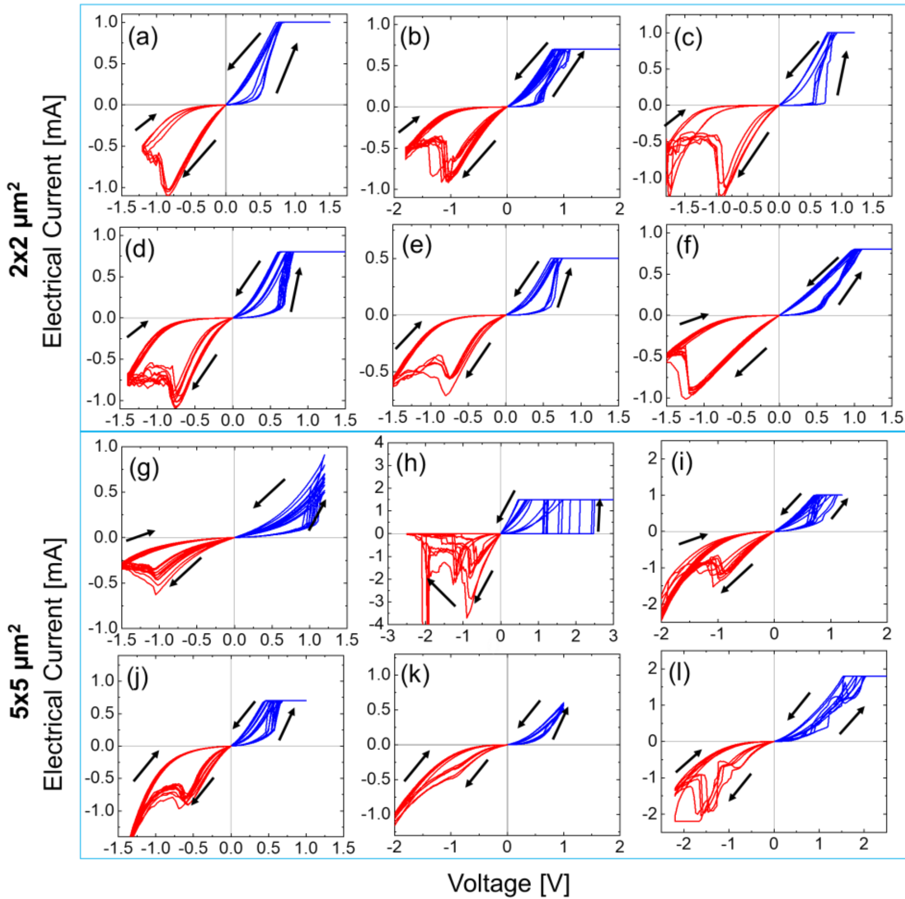

Figure 3.3 Measured *I-V* cycle characteristics for RRAM devices with a crosspoint area of **(a-f)** 2x2 μm^2 and **(g-l)** 5x5 μm^2 for six devices each. The blue and the red graphs symbolize the set and reset processes respectively. The black arrows present the direction of the set and the reset direction.

3.2.4 Thermal characterization with SThM

SThM measurements were performed on our RRAMs to simultaneously image the topography and heating features on the device surface while electrical bias is applied to the device. To obtain thermal maps with the SThM, we used an Asylum® atomic force microscope (AFM) and an SThM

thermo-resistive probe (Pd on SiN from Bruker®). These SThM probes can correlate temperature variations in the tip to changes in electrical resistance with ($R_{probe} \propto T_{probe}$).[35] The details of the SThM operations are presented in chapter 2. During the SThM scans, a constant electrical bias was applied between the two electrodes of the RRAM device.

As illustrated in Fig. 3.1 (a), after the conductive filament is formed in the RRAM device, SThM can map the hot spot generated on the surface of the device due to Joule heating. In the inset of Fig. 3.1 (b) and (c) we present two steady state temperature maps with their corresponding *I*-*V* curves. The star symbol indicates the voltage bias applied to the device while performing the SThM scan. In both cases we observed a hot spot with a surface temperature increase (ΔT) of 17 K and 8 K in the 2x2 μm^2 and the 5x5 μm^2 device, respectively, when a power of ~400 and 300 μW was applied. It is worth mentioning that this temperature was measured at the surface. Therefore, this temperature is not the internal temperature of the filaments, and one needs to consider that the heat generated by the filament in the metal oxide also dissipates greatly along the top and bottom electrodes. Therefore, both the temperature and the size of the heating spot at the surface differ significantly from those of the buried filament, as indicated by Deshmukh *et al.*[9].

3.2.5 Conversion of SThM electrical signal into temperature

Converting the electrical response of the SThM probe, i.e., the voltage signal of the thermo-resistive probe measured at the Wheatstone bridge, into temperature is one of the major challenges of the SThM. We followed the calibration approach presented in chapter 2 to determine the *CaF* that converts the voltage signal (mV) into temperature (K). This approach consists of scanning with the SThM a set of metal (palladium) lines with different widths ranging from 50 to 750 nm that self-heat when applying power to them. As stated in chapter 2, we observed that the *CaF* saturates above a certain line width, which relates to the thermal exchange properties of the probe. Fig. 3.4 shows the *CaF* vs line width graphs obtained for the probes used for a probe power of $P_{probe} \approx 19$ μW. We decided to operate the SThM at this power corresponding to a bridge voltage of 0.5 V because this configuration provides a high temperature sensitivity while the thermal exchange area of the probe is in the range of the targeted heating feature size. In the maps presented in Fig. 3.1 we obtained that the calibration factor of the used tip saturated at a value of $CaF = 7.1 \pm 0.5$ mV/K (tip 2) for surface temperature features above 680 nm. This *CaF* was used to calculate the

temperatures of most of the hot spots observed experimentally, e.g., for the results in Fig. 3.1 where the full widths at half maximum (FWHM) of the hot spots are > 750 nm. The electrical signal in mV measured with SThM (ΔV_{SThM}) was calculated as the difference between the heated maps and a reference map at zero power. Overall, ΔV_{SThM} can be converted to the temperature increase (ΔT) in K as follows:

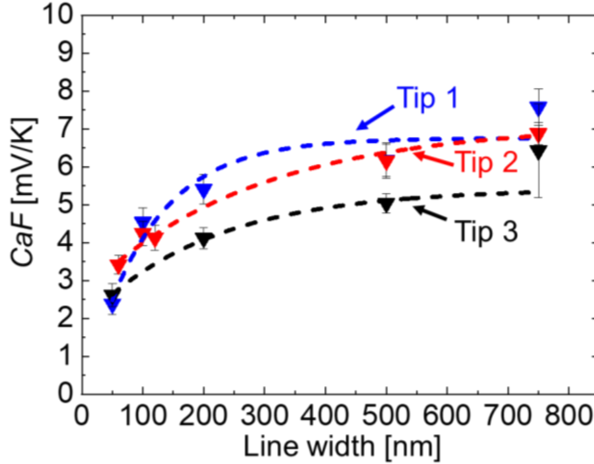

Figure 3.4 SThM calibration factor (*CaF*) estimated by means of the slope of the $\Delta V_{\mathrm{SThM,line}}$ vs ΔT_{line} graphs as a function of the line width for the three different tips we used for the thermal characterization of our devices.

$$\Delta T = \frac{\Delta V_{\mathrm{SThM}}}{CaF} \tag{3.1}$$

At this point it is worth noting that a careful calibration allows this approach to be extended for the study of even smaller devices as presented in this chapter. As can be seen from the graphs in Fig. 3.4 and discussed in chapter 2 we observe a drop in the calibration factor at a certain cut-off line width. This is related to the disc-shaped thermal exchange area between the tip and the sample. When the size of the device heating feature lies below the size of the cut-off line width, the heat exchange between the tip and device is truncated and the calibration factor decreases. However, beyond the cut-off, one should notice that the conversion factor drastically reduces. For devices or hot spots below ~50 nm determining an accurate value could be very challenging and might also involve considerable uncertainty. Therefore,

additional strategies to alleviate it could be to measure in vacuum, i.e., to reduce the thermal exchange radius between the tip apex and the surface by removing heat transfer mechanisms like convection or water meniscus, or to improve the signal processing techniques, like the deconvolution approach described by Deshmukh *et al.*[9]

3.3 Results

3.3.1 Steady state measurements

Fig. 3.5 (a) shows the topography map of a RRAM device with a cross-point area of 2x2 μm^2 obtained with a SThM probe. Fig. 3.5 (b) shows a 3D representation of two thermal maps obtained for the same 2x2 μm^2 device. Hereby we present two maps obtained for a non-heated case (P = 0 mW) and for a heated case (P = 0.57 mW). In the heated case we observed a hot spot induced by current passing through the conductive filament.

Fig. 3.5 (c) and (d) show multiple temperature maps obtained on the same device after the device is (c) set (blue dashed rectangular) vs (d) reset (red dashed rectangular). In the set state we can see that the hot spot is localized at the same location and its temperature scales up as the power applied to the device increases (same set state, i.e., no cycling between images). We observed that the maximum hot spot temperature increased from 13 K at 0.21 mW to 18 K at 0.4 mW.

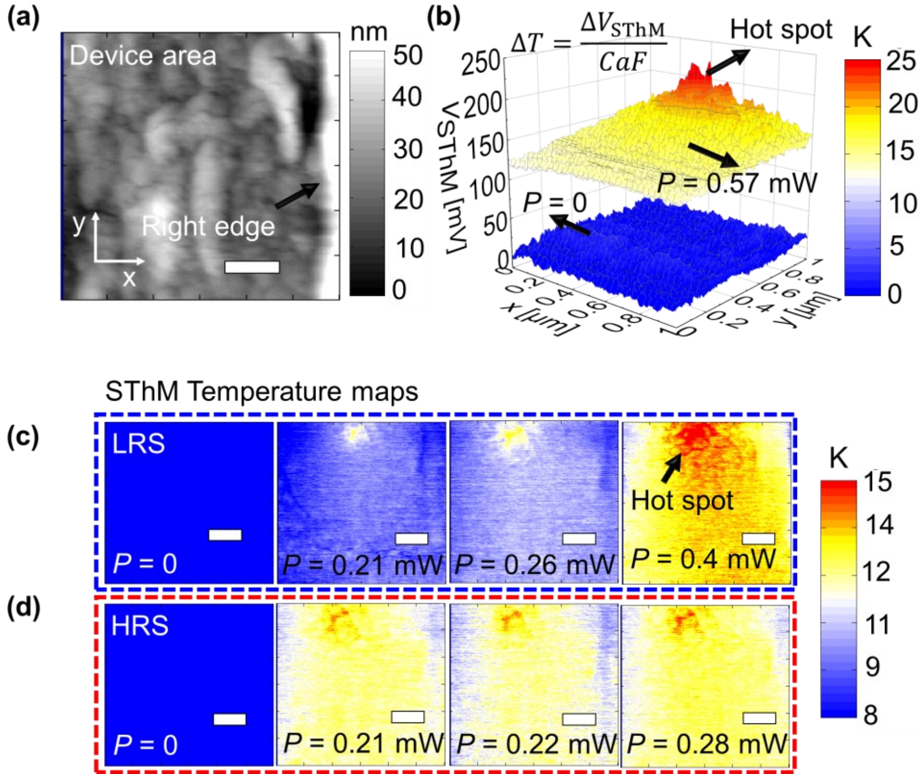

Figure 3.5 Topographic image of a device with an area of 2x2 μm^2 (scale bar 200 nm) **(b)** 3D SThM temperature (z-axis) map obtained for the device shown in (a) when applying a power of *P* = 0.57 mW and under no power applied (*P* = 0). The difference in SThM signal between heated vs non-heated case was converted into a temperature change by using a calibration factor of *CaF* = 7.1 mV/K. **(c)** and **(d)** SThM temperature maps for four different power magnitudes after **(c)** seting the device at a positive polarity (blue dashed rectangle) and after **(d)** reseting the device at the reverse negative polarity (red dashed rectangle). (scale bar 200 nm).

After reseting the device, we carried out temperature maps for similar powers as in the set case but with the reversed polarity (see Fig. 3.5 (d)).

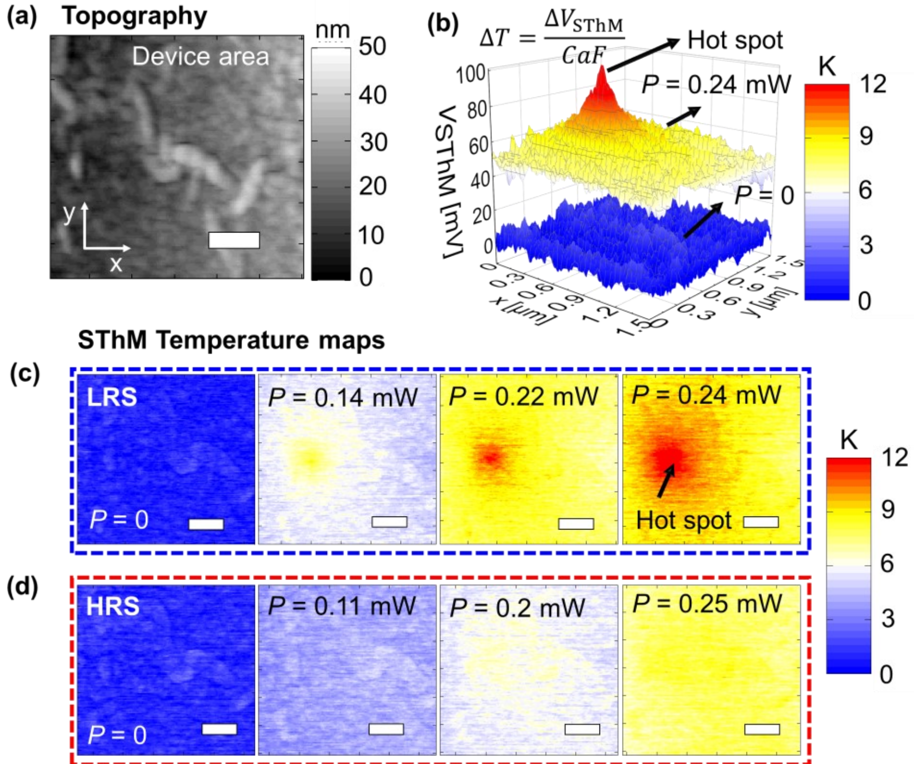

Figure 3.6 (a) Topographic image of a device with an area of 5x5 μm^2 (scale bar 300 nm) **(b)** SThM thermal signal (z-axis) map obtained for the device shown in (a) when applying a power of *P* = 0.24 mW and under no power applied (*P* = 0). The difference in SThM signal between heated vs non-heated case is converted into a temperature change by using a calibration factor of *CaF* = 7.1 mV/K as represented by the color scheme. **(c)** and **(d)** SThM temperature maps for four different powers after **(c)** seting the device at positive polarity (blue dashed rectangle) and after **(d)** reseting the device at negative polarity (red dashed rectangle). (scale bar 300 nm).

Fig. 3.6 (a) shows the topography for a 5x5 μm^2 RRAM device scanned with SThM. Fig. 3.6 (b) shows a 3D representation of two thermal maps obtained for the 5x5 μm^2 device at 0 mW power and at 0.24 mW in its set state. During the first scan at the bottom, we scanned the cross-point area while no power is applied to the device. In this case no current is passing through the filament i.e., the device is not heated. For the second map above, we applied a power of P = 0.24 mW to the device. In this case a current of I_{ON} ~ 0.4 mA passes through the filament, which results in a localized hot spot on the surface. Considering a stable filament resistance, the magnitude of the resulting surface temperature mostly depends on the power and polarity of the electrical current applied to the device.

Fig. 3.6 (c) and (d) shows multiple temperature maps obtained on the same device after the device was (c) set vs (d) reset. In the set state the hot spot is localized at the same location and its temperature scales up as the power applied to the device increases (same set state, i.e., no cycling between images). We observed that the maximum hot spot temperature increased from 9 K at 0.14 mW to 14 K at 0.24 mW. The power itself does not impact the shape of the hot spot but it rises the temperature. After reset, we obtained temperature maps for similar powers as in the set case but with reversed polarity (see Fig. 3.6 (d)). Considering the higher resistance in the reset, we therefore required to apply higher voltages than in the set state. At a power of 0.11 mW, the heating is spread uniformly. At higher power we observed mostly uniform heating on the device, with little localized heating that could eventually be related to a partial but not complete breakdown of the filament during the reset process. As an example, in Fig. 3.6 (d) at 0.2 mW, it looks like the breakdown of the filament is not fully complete as minor elevated temperature is still visible at the initial position of the filament. At sufficiently high power we observed a partial re-forming of the conductive filament in agreement with the *I*-*V* characteristics.

Similar observations are made with the heating maps of the 2x2 μm^2 device of Fig 3.5. However, in the reset state we observed a comparable high elevated heating at the initial hot spot position but less localized than in the set state of the 2x2 μm^2. In agreement with the reasoning above this observation is related with the filament breakdown not being fully complete. In comparison of this particular device, we measured a resistance of the device in between around 4.5 and 9 kΩ in the 2x2 μm^2 and 9 and 16 kΩ in the 5x5 μm^2 device in the reset thermal maps. Therefore, the smaller difference in between set and reset heating might originate from a less

complete breakdown in the 2x2 μm^2 illustrated by the lower resistance in the reset state. This observation has been obtained for these particular devices, since a full breakdown of the filament has been observed in other 2x2 μm^2 devices.

3.3.2 COMSOL model for the characterization of the filament temperature

The results in Fig. 3.5 and 3.6 present the temperature of the RRAM devices at the surface. In order to confirm the experimentally obtained temperatures and to estimate the filament temperature we employed an electrothermal FEM model in COMSOL Multiphysics. We built our model considering the same boundary and heat flux conditions of the results obtained in a study by Deshmukh *et al.*[9] By means of that we replicated the structure of the 5x5 μm^2

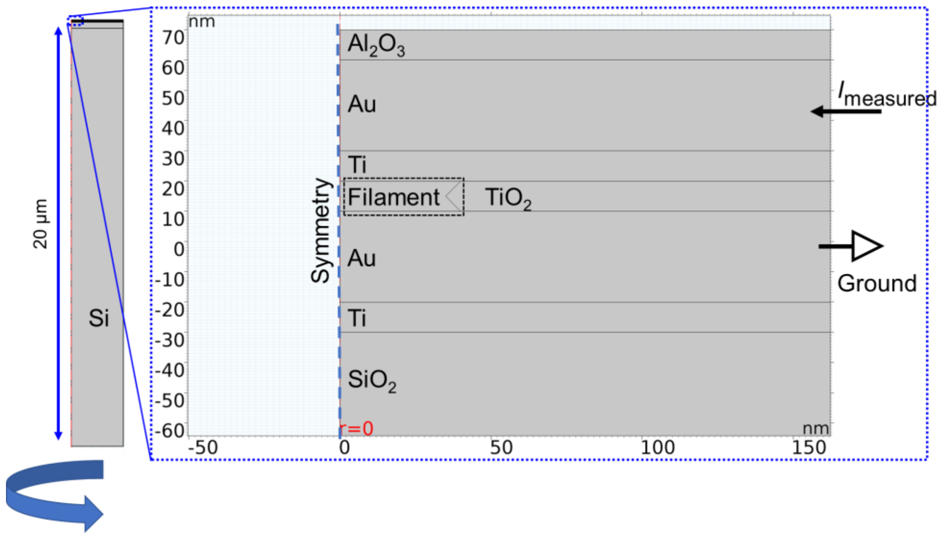

Figure 3.7 Finite element method (FEM) model geometry of the applied model for the characterization of the hot spot temperature. The model has a cylindrical symmetry around the central axis with a structure equivalent to the experimental TiO_2 RRAM devices with an hourglass shaped filament. An electric current ($I_{measured}$) is applied from the top electrode to the bottom electrode.

device which results are shown in Fig. 3.6. Therefore, we used a 2.5 x 2.5 x 20 μm model with a cylindrical symmetry around the central axis as shown in Fig. 3.7. We adjusted the geometry to mimic our current $Si/SiO_2/Ti/Au/TiO_2/Ti/Au/Al_2O_3$ as described in Section 3.2.1. As can be seen

in Fig. 3.7 we shaped the filament on the left edge of the TiO_2 using an hourglass structure, considering the cylindrical symmetry of the model (as indicated in Fig. 3.7), as this approach showed the best fitting. In order to simulate the Joule heating in the devices which is accompanied by the electrical current, we introduce a current source at the top electrode $I_{measured}$ while grounding the bottom electrode in this electrothermal model.

In accordance with previous studies, we estimated the thermal contact conductance in between the oxide and the top electrode ($G_{TiO2\text{-}Ti/Au}$) using the full width at half maximum (FWHM) of our SThM scans of the hot spot as follows.[9] The thermal healing length of the hot spot is defined as follows,

$$L_{\mathrm{H}} = \sqrt{\frac{k_{\mathrm{th,TE}} \cdot t_{\mathrm{TE}}}{G_{\mathrm{TiO2-Ti/Au}}}} \tag{3.2}$$

where $k_{th,TE}$ and t_{TE} are the thermal conductivity and thickness of the top electrode, respectively. In our RRAM devices we can estimate FWHM ≈ $2L_H$ given the small size of our filaments ($d_{CF} \ll L_H$). Therefore, we estimated the FWHM of the hot spot temperature peaks for the three images investigated. The thickness and thermal conductivity of the top electrode as also the remaining material characteristics are assembled from the literature and the COMSOL library. Table 3.1 shows the fixed material and contact parameters used for this FEM simulation.

Table 3.1 Model Parameters used in the COMSOL Simulation.

Parameter	Value at room temperature	Reference
σ_{Au}	$14.28 \cdot 10^6$ S/m	46
k_{Au}	90 W/(m·K)	46
k_{TiO2}	0.8 W/(m·K)	47
k_{Ti}	8.2 W/(m·K)	48
$G_{TiO2\text{-}Ti/Au}$	1.25 MW/(m^2·K)	9
σ_{TiO2}	10^{-15} S/m	9
k_{SiO2}	1.4 W/(m·K)	COMSOL Database
k_{Si}	150 W/(m·K)	9
k_{Al2O3}	3 W/(m·K)	9
$G_{SiO2\text{-}Ti/Au}$	80 MW/(m^2·K)	49
$G_{SiO2\text{-}Si}$	434 MW/(m^2·K)	9

For the characterization of the Joule heating, we adjusted the top electrode as a current source with an applied current equal to the values measured

during the SThM mapping $I_{measured}$. The bottom electrode acts as the electrical ground at which the potential is 0 V.

3.3.3 Estimation of the hot spot characteristics

For the estimation of the hot spot characteristics, we adjusted the remaining model parameters in order to fit the surface temperature, FWHM and the electrical potential measured during the SThM scans. The sweep parameter included the size characteristics of the filament (top radius, bottom radius,

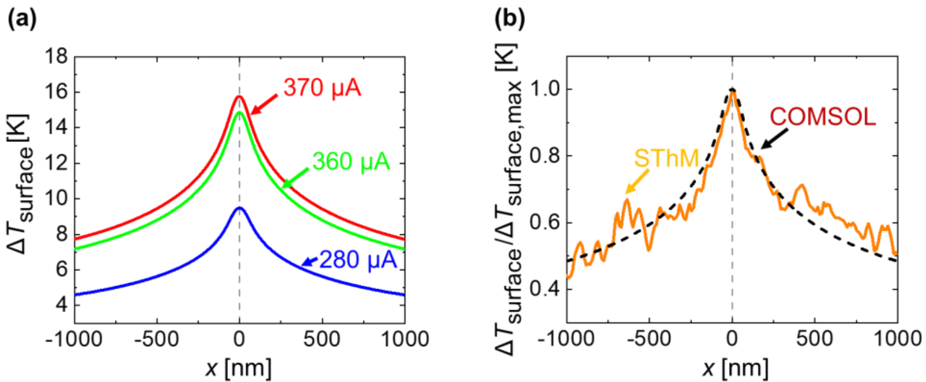

Figure 3.8 (a) Simulated temperature increase along the surface ($\Delta T_{surface}$) of the 5x5 µm^2 RRAM device structure for three different currents $I_{measured}$ (280 µA in blue, 360 µA in green and 370 µA in red). **(b)** Normalized simulated (dashed line) and measured SThM (straight line) temperature increase $\Delta T_{surface}/\Delta T_{surface,max}$ along the surface of the RRAM device for an electric current $I_{measured}$ of 280 µA.

and the center radius) the thermal conductivity of the filament ($k_{th,filament}$) the thermal contact conductance in between the filament and the top and bottom electrode ($G_{CF\text{-}TE}$) and ($G_{CF\text{-}BE}$) respectively and the electrical contact resistance in between the filament and the top electrode ($\rho_{c,CF\text{-}TE}$). The initial values for these parameters were estimated on base of the simulation characteristics displayed in ref.[9]

Table 3.2 shows the sweep parameter and the results of the COMSOL simulation which presented the best fit with the experimental results. Fig. 3.8 (a) shows the corresponding simulated temperature profiles at the surface of the RRAM devices for the best fitting parameters of the three investigated SThM maps. In general, we observed a good fit of the FWHM, and the potential drop in between experiments and simulation. We obtained slightly higher (10-15 %) values for the maximum temperature at the surface

($\Delta T_{max,surface}$) from the simulation in comparison with the experimental results. Considering the error of our calibration factor and the other material parameters this temperature difference is in a reasonable range. Fig. 3.8 (b) shows a fit of the experimentally obtained surface temperature profile (straight line) with the profile obtained from the COMSOL simulation (dashed line) for $I_{measured}$ = 280 µA. In this graph we normalized the temperature in order to take the temperature difference into account.

In comparison to the results of Deshmukh *et al.*[9] we estimated a higher $k_{th,filament}$, which can be originated from the difference in the material characteristics and higher thickness of the titanium oxide layer and thus the filament. Additionally, our simulations results indicate a relatively high filament diameter of around 41-44 nm, which is connected to the relatively

Table 3.2 Comparison of the hot spot characteristics of the SThM measurements and the COMSOL Multiphysics simulation for the three investigated scans. The table shows the corresponding sweep parameters that showed the best fits.

Characteristic	**$I_{measured}$ = 280 µA**	**$I_{measured}$ = 360 µA**	**$I_{measured}$ = 370 µA**
Experimental observations			
FWHM [nm]	1820	1920	1820
$\Delta T_{max,surface}$ [K]	8.62	12.52	13.9
Potential [V]	0.41	0.49	0.54
COMSOL Multiphysics results			
FWHM [nm]	1880	1820	1820
$\Delta T_{max,surface}$ [K]	9.48	14.75	15.82
Potential [V]	0.41	0.49	0.54
$\Delta T_{max,filament}$ [K]	171.61	238.85	245
Sweep Parameter			
$k_{th,\ filament}$ [W/(m·K)]	3	3	3
Bottom radius [nm]	43	44	47
Top radius [nm]	41	43	43
Center radius [nm]	38.5	41	41.5
G_{CF-TE} [MW/(m^2·K)]	12	12	12
G_{CF-BE} [MW/(m^2·K)]	100	100	100
$\rho_{C,\ CF-TE}$ [Ω·cm^2]	$4.76 \cdot 10^{-8}$	$5 \cdot 10^{-8}$	$5.26 \cdot 10^{-8}$

high electric currents applied to the device. Finally, the maximum temperature increases of the filaments ($\Delta T_{max,filament}$) is estimated to be in between 172 and 245 K, correlating with the power applied to the device.

3.3.4 In-operando SThM measurements at the hot spot

Next, we aimed to correlate the heating of the hot spot with the in-operando electrical *I-V* behavior of the devices during cycling. For that purpose, we kept the SThM probe static at the position of the hot spot, which we localized during the steady state measurements, while running *I-V* sweeps in the device. The SThM software provides a logger option that records the in-operando SThM thermal signal as a function of time. This approach allows investigating how the hot spot on the surface heats up depending on the in-

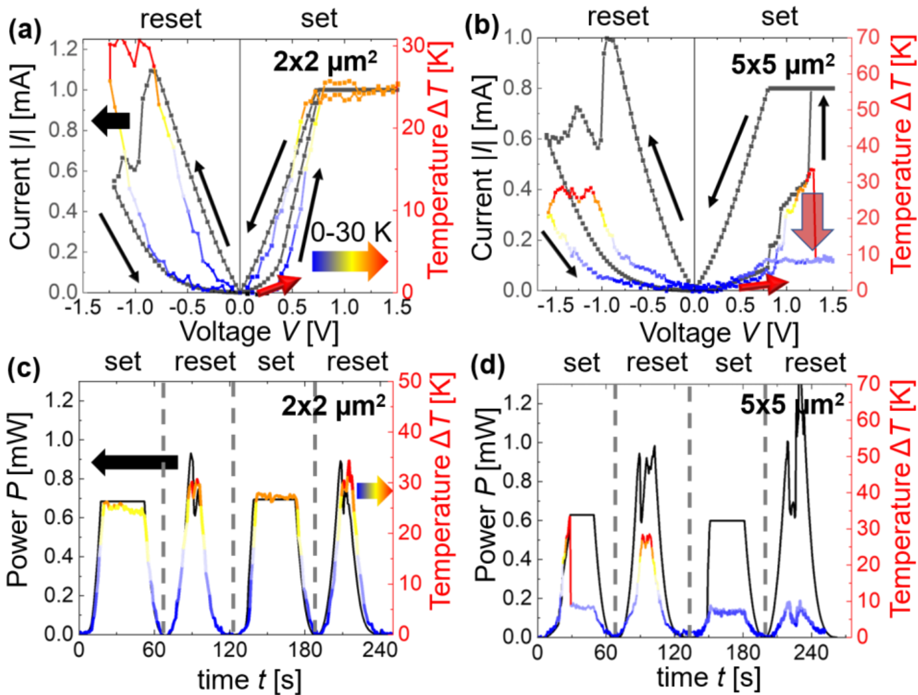

Figure 3.9 (a,b) Absolute electric current |*I*| (left axis) and temperature increase (ΔT, right axis) for one cycle (set and reset) as a function of the sweeping voltage for a device area of **(a)** 2x2 µm^2 and **(b)** 5x5 µm^2 (the red arrows indicate the beginning of the sweep). **(c,d)** Electrical power (left axis) and temperature increase (ΔT, right axis) for two full cycles of set and reset as a function of time for a device area of **(c)** 2x2 µm^2 and **(d)** 5x5 µm^2. The color scale of the temperature graphs ranges from 0 (blue) to 30 (red) K.

operando power applied. Fig. 3.9 (a) and (b) show the *I*-*V* measurements for devices with an area of (a) 2x2 μm^2 and (b) 5x5 μm^2.

The right axes of these figures show the temperature measured by the SThM, which increases as the power of the devices scales up.

The temperature evolution in Fig. 3.9 (a) and (b) for the 2x2 μm^2 and 5x5 μm^2 devices, respectively, follows the same trend as the *I*-*V* curve for low voltages. However, we observed a drop in the temperature in the 5x5 μm^2 device illustrated by the transparent red arrow during the set process which is not in line with the *I*-*V* curve obtained at higher voltages. Simultaneously the current sharply increases which corresponds to the shift from HRS to LRS. With the aim to obtain more insights into this observation, we compared the SThM temperature measurements with the electrical power applied to the device. Fig. 3.9 (c) and (d) shows the power and ΔT over different cycles of set and reset. Fig. 3.9 (c) shows that the heating measured by the SThM probe in the original position of the hot spot for the 2x2 μm^2 device is consistent for different cycles of set and reset. This is indicative of having a reliable filament that forms and breaks in the same device location, which we observed reliably for > 10 devices. However, Fig. 3.9 (d) shows that the heating around the original filament location for the 5x5 μm^2 device varies considerably during set and reset. This is indicative of position variation of the conductive filament, and it was observed in 5 devices. To further analyze this observation, we characterized how the steady state measurements of the same devices as displayed in Fig. 3.9 varied with cycling.

3.3.5 Steady state characterization after cycling

In order to determine whether the location of the hot spot varies between set and reset cycles, we carried out steady state thermal maps of the same devices after the *I*-*V* sweeps. To verify a constant tip position during in-operando measurements we used the same tip offset in the steady state measurements before and after cycling. Fig. 3.10 (a) and (b) show 3D temperature maps (z-axis) together with the topographic image (x and y axis) of the device for the two areas under study, i.e., (a) 2x2 μm^2 and (b) 5x5 μm^2 (a second example is illustrated in section 3.7.2). Each device was set and reset multiple times and the steady state thermal maps were obtained in the low-resistive state between cycles.

The maps of the 2x2 μm^2 device revealed that the position of the hot spot and thus of the filament remained unchanged after cycling. However, we observed a shift of the hot spot location in the maps of the 5x5 μm^2 device

with an average distance of 1.6 μm between each other. Based on the 5x5 μm² devices measured (total of 5), we concluded that there were up to 3

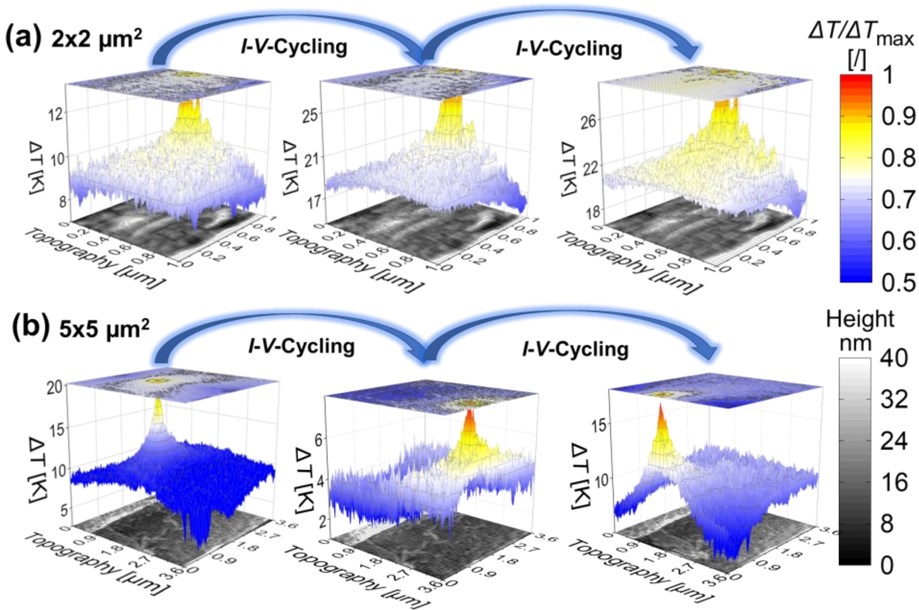

Figure 3.10 3D surface temperature maps (z-axis) plotted over the 2D topography (bottom) of the device with an area of **(a)** 2x2 μm² and **(b)** 5x5 μm² during steady state measurements. Power (*P*) applied to the devices during the scans in **(a)** are 0.21 mW/0.57 mW/0.64 mW and in **(b)** are 0.39 mW/0.21 mW/0.37 mW from left to right.

possible hot spot locations with reversible switching behavior at similar power. These observations with SThM make it possible evaluating the cycle-to-cycle variation by measuring the shift in the filament position in RRAM devices which cannot be done solely through the analysis of the *I-V* curves.

3.4 Discussion

The need to improve the reliability of RRAM devices has been an ample topic of discussion[36–38]. Park *et al.*[37] characterized the existence of multiple conductive paths in Ta_2O_{5-x}/TaO_{2-x} RRAM devices by means of transmission electron microscopy (TEM). However, on the basis of these measurements no conclusions on heat distribution along the individual paths in operation

can be drawn. Baeumer *et al.*[38] observed the change of the position of the active conductive filament as a consequence of *I*-*V* cycling in $SrTiO_3$-based RRAM devices using photoelectron emission microscopy (PEEM). The filament is localized through the analysis of the photoemission threshold difference across the device area. PEEM is limited by its depth of field of few nm and by the lack of information towards the current or heat distribution in steady state. Due to the depth limitation, the PEEM studies must also be carried out in special device structures, for example by using photoelectron-transparent graphene electrodes.[38]

This is not needed for SThM studies, where a typical and more technologically relevant cross-point structure can be investigated. With the thermal information provided in this article we can observe the heat distribution on the surface of relevant RRAM devices during set and reset processes. As an example, from Fig. 3.10 (b) we can see that the hot spot is moving which relates to the formation of filaments in different locations. The electrical information combined with the thermal SThM analysis displayed in this work for TiO_2 RRAM devices provide relevant information into the parameters that affect their reliability. In this case, the electrical and thermal signatures of the device allow us to draw conclusions on how the geometry and electrical connections affect the operation. More specifically, for the better understanding of these results we discuss the differences in heating between the 2x2 μm^2 and 5x5 μm^2 devices considering i) the area of the devices, ii) the resistance of the top and bottom metal lines that connects the device with the pad electrodes, which is equivalent to a series resistor.

3.4.1 Influence of the area size

First, we observed a shift of the hot spot location in five different devices with an area of 5x5 μm^2. The distance between each hot spot (distance between maximum temperature) that was formed varied between 1.5 μm and 3 μm with an average distance of 2.21 ± 0.87 μm. This average distance between hot spots is larger than the size of the 2x2 μm^2 devices. Therefore, we suggest that the size of the device could be a limiting factor for the filament to relocate, being more favorable to form just one filament in devices < 2x2 μm^2 (as hypothesized before[39]).

3.4.2 Characterization of the line resistance

Second, an additional perspective correlates with the different width of the metal lines connecting the top and bottom electrode with the pads. The size of the metal lines in the 2x2 μm^2 devices is smaller than in the 5x5 μm^2

devices, which results in a higher series resistance. The *I-V* curves we measured are the extrinsic *I-V* characteristics. The voltage drops not only on

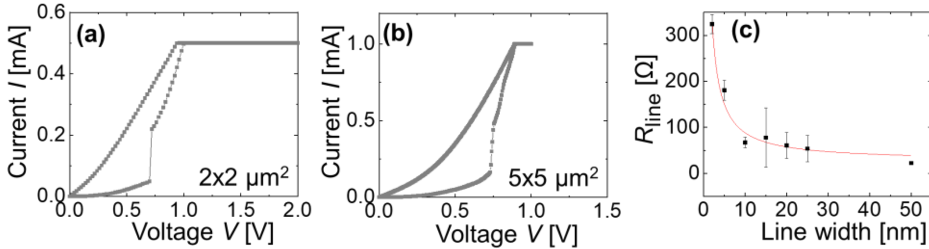

Figure 3.11 (a) and **(b)** Measured *I-V* characteristics of the 2x2 μm^2 and 5x5 μm^2 devices, respectively. **(c)** Measured line resistance (R_{line}) of the bottom and top electrode as a function of the line width of the device.

the memory cell but also on the series resistance, which includes the line resistance of the electrodes, the contact resistance of the probes and pads and other contributions from the device stack, as for example the vertical conduction in the electrodes. By subtracting the voltage drop over the series resistance, the intrinsic *I-V* characteristics can be obtained.[40] Fantini et al.[40] reported that the intrinsic *I-V* behavior of resistive switching devices shows that the set is triggered at a certain threshold voltage and is followed by a snapback to a voltage value where the differential resistance (*dV/dI*) is approximately 0, i.e., a vertical line in the *I-V* characteristics. Taking this into account, the series resistance can be estimated by calculating the series resistance value that transforms the extrinsic *I-V* curve into the intrinsic one, exhibiting the vertical transition behavior.

We extracted the approximate value of the series resistance for 2x2 μm^2 and 5x5 μm^2 devices from the extrinsic *I-V* curves in Fig. 3.11 based on the abovementioned method. During the set process, after the abrupt jump at the threshold voltage, the current shows a linear dependence with the voltage before reaching the compliance. This is caused by the series resistance. Its value can be estimated from the slope of the curve in the linear region. The estimated series resistance of 2x2 μm^2 and 5x5 μm^2 devices is 1 kΩ and 300 Ω, respectively. The contact resistance between the probe and the electrode is similar due to the same measurement method, therefore the line resistance and the other electrode contributions should be the dominating cause of the difference in the series resistance. To be noted,

these values are not for the pristine devices, but for the devices that switched for at least 20 cycles.

Additionally, we measured the line resistance of both the top and bottom electrode for various pristine devices. Fig. 3.11 (c) shows the measured combined line resistance (R_{line}) of the bottom and top electrode as a function of the line width. At a higher line width, we observed a relatively constant value for R_{line}. In these cases, we expect the contact resistance between the measuring probes and the electrode surface to be the dominating factor of R_{line}. For the relevant line widths (2 µm and 5 µm) we measured an increment in the line resistance based on the decreased line area. By subtracting the estimate of the contact resistance, we obtained a R_{line} of 123 Ω and 308 Ω for the 5x5 and 2x2 μm^2 devices respectively. The difference from the measured line resistance and the estimated series resistance stems from the contact resistance between the lines and the active area and possible other resistances which are not included in the line resistance.

The remaining resistance could originate from the conduction through the Ti layer and TiO_2/Ti interface, where a partial oxidation of the Ti occurs due to the oxygen exchange reaction[41,42]. Using an integrated series resistance has been shown to be an effective method to decrease current overshoot in RRAM devices.[43,44] The higher series resistance in the 2x2 μm^2 devices makes them more robust against current overshoot during electroforming and set events, which could be responsible for the change of the active filament position observed in the larger 5x5 μm^2 devices.

3.4.3 STEM characterization of the layer structure in pristine and cycled devices

In order to investigate the impact of the electrical forming and cycling of the device on the material structure we employed high-angle annular dark field scanning transmission microscopy (HAADF-STEM) with an energy-dispersive X-ray spectroscopy (EDX) detector. First, we cut the samples out of the cross-point area of our RRAM devices using the focused ion beam (FIB) technique. Second, we employed transmission electron microscopy (TEM) in the cross-section direction for the characterization and evaluation of the device layer structure. By means of that we aimed to evaluate the chemical composition and distribution of the three main elements i.e., Au, Ti

and O which are the building blocks for the metal/insulator/metal (Au/TiO_2/Ti/Au) structure of our RRAM devices.

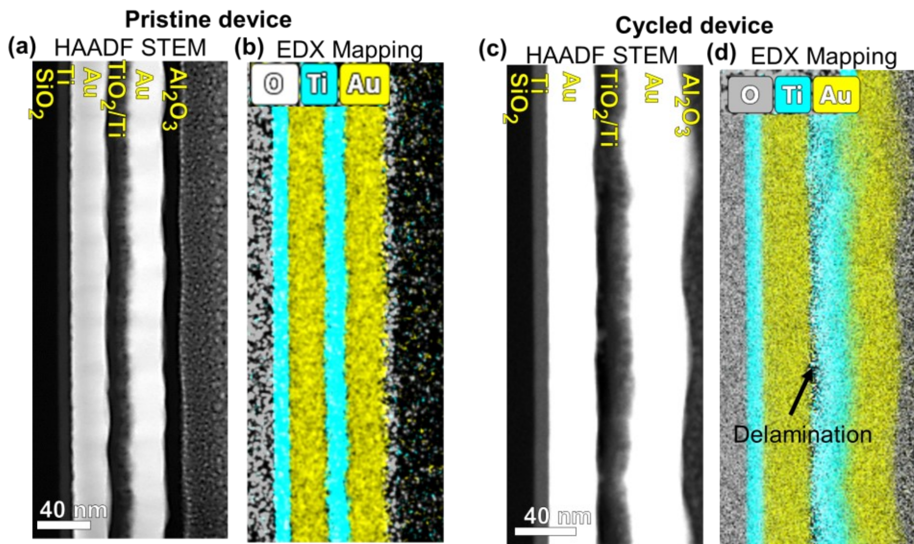

Figure 3.12 (a) High-angle annular dark field scanning transmission electron microscopy (HAADF STEM) images of a Crosspoint device area of one pristine 5x5 μm^2 TiO_2 RRAM device. **(b)** Energy-dispersive X-ray spectroscopy (EDX) images showing the gold (gold), titanium (light blue) and oxygen (grey) compositions of the same area as in **(a)**. **(c)** HAADF STEM images of a cross-point device area of one cycled 5x5 μm^2 TiO_2 RRAM device. **(d)** EDX image showing the Gold (gold), Titanium (light blue) and oxygen (grey) compositions of the same area as in **(c)**.

Fig. 3.12 (a) and (b) show the HAADF and the EDX images obtained from a pristine, i.e., not electrically formed device. Hereby, the HAADF imaging method enables us to clearly identify the high atomic number gold electrodes. The remaining layers are indicated in Fig. 3.12 (a) according to the device structure. We clearly observed a continuous Ti and O signal along the TiO_2/Ti areas in between the electrodes.

Fig. 3.12 (c) and (d) show the HAADF and the EDX images obtained of an already cycled 5x5 μm^2 device. Similar to the pristine device the EDX image shows a clear gold signal at the position of the electrodes. However, we observed a small but not continuous drop of the Ti and O signal at the transition area in between the TiO_2 layer and the bottom electrode.

Similar observations have been made by Carta *et al.*[45] in a Pt/TiO_2/Pt RRAM device. In their study, they investigated the material structure of their RRAM devices in pristine and in formed state. They performed HAADF-STEM measurements with an EDX detector for the characterization of the devices before and after electrical cycling. On the one hand they observed a continuous Ti and O signal in the pristine device. On the other hand, the measurements revealed a drop in the Ti and O signal in between the TiO_2 layer and the Pt top electrode in the formed devices referred to delamination. This delamination effect was claimed to be originated from the development of O_2 gas during the formation of the conductive filament.

From our results we cannot make a solid conclusion about the impact of the layer delamination observed in our devices on their *I-V* or heating variation during cycling. However, we should emphasize that this effect might be a significant cause for variability of RRAM devices. Presumably the delamination should lead to a reduction of the effective cross-point area of the devices. The delamination may contribute to the C2C and D2D variabilities and further lead to performance degradation in the RRAM devices, though more evidence is required. Despite this effect, our *I-V* characteristics and SThM images show that the filament keeps on re-forming and reseting during cycling with similar thermal and electrical characteristics.

3.5 Conclusions

In conclusion, we used the SThM to obtain thermal maps in TiO_2 memory devices with multiple sizes, operating both in steady-state and in-operando conditions, to evaluate their heating features. The thermal insights obtained for the device combined with its electrical characteristics allowed us to correlate the reliability of the devices with their design parameters. The results obtained reveal that the position shift of filaments is a significant source for the *I-V* characteristics variability in RRAM devices. Future studies should continue analyzing the impact of the area, line resistance and interfacial structure during cycling in other RRAM devices to gain a better understanding of how it affects their performance. Overall, SThM proves itself as a powerful approach to gain further insights on RRAM operation. This provides new routes for thermal and electrical characterization and engineering of RRAM not only restricted to metal oxide-based resistive switching.

3.6 References

1 H. P. Wong, F. Ieee, H. Lee, S. Yu, S. M. Ieee, Y. Chen, Y. Wu, P. Chen, B. Lee, F. T. Chen and M. Tsai, *Proc. IEEE*, 2012, **100**, 1951–1970.

2 H. Wu, X. H. Wang, B. Gao, N. Deng, Z. Lu, B. Haukness, G. Bronner and H. Qian, *Proc. IEEE*, 2017, **105**, 1770–1789.

3 X. L. Hong, D. J. J. Loy, P. A. Dananjaya, F. Tan, C. M. Ng and W. S. Lew, *J. Mater. Sci.*, 2018, **53**, 8720–8746.

4 H. Wang and X. Yan, *Phys. Status Solidi - Rapid Res. Lett.*, 2019, **13**, 1900073.

5 D. Kumar, R. Aluguri, U. Chand and T. Y. Tseng, *Ceram. Int.*, 2017, **43**, S547–S556.

6 M. Lanza, H. S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. C. Regan, L. Larcher, M. A. Villena, J. J. Yang, L. Goux, A. Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. Magyari-Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T. H. Hou, B. Hudec, D. Akinwande, R. Ge, S. Ambrogio, J. B. Roldan, E. Miranda, J. Suñe, K. L. Pey, X. Wu, N. Raghavan, E. Wu, W. D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. C. Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui and Y. Shi, *Adv. Electron. Mater.*, 2019, **5**, 1800143.

7 H. Y. Chen, S. Brivio, C. C. Chang, J. Frascaroli, T. H. Hou, B. Hudec, M. Liu, H. Lv, G. Molas, J. Sohn, S. Spiga, V. M. Teja, E. Vianello and H. S. P. Wong, *J. Electroceramics*, 2017, **39**, 21–38.

8 H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien and M. J. Tsai, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2008, 1–4.

9 S. Deshmukh, M. Muñoz Rojo, E. Yalon, S. Vaziri, Ç. Köroğlu, R. Islam, R. A. Iglesias, K. Saraswat and E. Pop, *Sci. Adv.*, 2022, **8**, eabk1514.

10 M. Lanza, K. Zhang, M. Porti, M. Nafra, Z. Y. Shen, L. F. Liu, J. F. Kang, D. Gilmer and G. Bersuker, *Appl. Phys. Lett.*, 2012, **100**, 123508.

11 A. Schonhals, D. Wouters, A. Marchewka, T. Breuer, K. Skaja, V. Rana, S. Menzel and R. Waser, *2015 IEEE 7th Int. Mem. Work. IMW 2015*, 2015, 15–18.

12 C. M. M. Rosário, B. Thöner, A. Schönhals, S. Menzel, M. Wuttig, R. Waser, N. A. Sobolev and D. J. Wouters, *Appl. Phys. Lett.*, 2018, **112**, 213504.

13 K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Park, J. Shin, K. P. Biju, J. Kong, K. Lee, B. Lee and H. Hwang, *Nanotechnology*, 2011, **22**, 254023.

14 H. Y. Jeong, Y. I. Kim, J. Y. Lee and S. Y. Choi, *Nanotechnology*, 2010, **21**, 115203.

15 B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg and S. Tiedke, *J. Appl. Phys.*, 2005, **98**, 033715.

16 Z. Shen, C. Zhao, Y. Qi, W. Xu, Y. Liu, I. Z. Mitrovic, L. Yang and C. Zhao, *Nanomaterials*, 2020, **10**, 1437.

17 A. Grossi, E. Nowak, C. Zambelli, C. Pellissier, S. Bernasconi, G. Cibrario, K. El Hajjam, R. Crochemore, J. F. Nodin, P. Olivo and L. Perniola, *IEEE Int. Electron Devices Meet.*, 2016, **2016**, 471–474.

18 G. Molas, G. Sassine, C. Nail, D. Alfaro Robayo, J.-F. Nodin, C. Cagli, J. Coignus, P. Blaise and E. Nowak, *ECS Trans.*, 2018, **86**, 35.

19 A. Belmonte, D. Linten and M. Jurczak, *Microelectron. Eng.*, 2015, **147**, 171–175.

20 D. Ielmini, *Semicond. Sci. Technol.*, 2016, **31**, 063002.

21 S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy and D. Ielmini, *IEEE Int. Electron Devices Meet.*, 2013, **2013**, 31.5.1-31.5.4.

22 U. Celano, L. Goux, R. Degraeve, A. Fantini, O. Richard, H. Bender, M. Jurczak and W. Vandervorst, *Nano Lett.*, 2015, **15**, 7970–7975.

23 D. H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X. S. Li, G. S. Park, B. Lee, S. Han, M. Kim and C. S. Hwang, *Nat. Nanotechnol.*, 2010, **5**, 148–153.

24 F. Torres, A. C. Basaran and I. K. Schuller, *Adv. Mater.*, 2022, **accepted**.

25 E. Yalon, S. Deshmukh, M. Muñoz Rojo, F. Lian, C. M. Neumann, F. Xiong and E. Pop, *Sci. Rep.*, 2017, **7**, 15360.

26 P. Yasaei, Q. Tu, Y. Xu, L. Verger, J. Wu, M. W. Barsoum, G. S. Shekhawat and V. P. Dravid, *ACS Nano*, 2019, **13**, 3301–3309.

27 S. M. Bohaichuk, M. Muñoz Rojo, G. Pitner, C. J. McClellan, F. Lian, J. Li, J. Jeong, M. G. Samant, S. S. P. Parkin, H. S. P. Wong and E. Pop, *ACS Nano*, 2019, **13**, 11070–11077.

28 E. Puyoo, S. Grauby, J. M. Rampnoux, E. Rouvìre and S. Dilhaire, *J. Appl. Phys.*, 2011, **109**, 024302.

29 M. Muñoz Rojo, J. Martín, S. Grauby, T. Borca-Tasciuc, S. Dilhaire and M. Martin-Gonzalez, *Nanoscale*, 2014, **6**, 7858–7865.

30 S. Gomès, A. Assy and P.-O. Chapuis, *Phys. Status Solidi Appl. Mater. Sci.*, 2015, **212**, 477.

31 K. Kim, W. Jeong, W. Lee and P. Reddy, *ACS Nano*, 2012, **6**, 4248–4257.

32 I. M. Datye, M. Muñoz Rojo, E. Yalon, S. Deshmukh, M. J. Mleczko and E. Pop, *Nano Lett.*, 2020, **20**, 1461–1467.

33 S. K. Nandi, E. Puyoo, S. K. Nath, D. Albertini, N. Baboux, S. K. Das, T. Ratcliff and R. G. Elliman, *ACS Appl. Mater. Interfaces*, 2022, **14**, 29025–29031.

34 N. Wainstein, G. Ankonina, T. Swoboda, M. Muñoz Rojo, S. Kvatinsky and E. Yalon, *IEEE Trans. Electron Devices*, 2021, **68**, 1298–1303.

35 Y. Zhang, W. Zhu, F. Hui, M. Lanza, T. Borca-Tasciuc and M. Muñoz Rojo, *Adv. Funct. Mater.*, 2020, **30**, 1900892.

36 H. L. Chee, T. N. Kumar and H. A. Almurib, *Proc. - 7th IEEE Non-Volatile Mem. Syst. Appl. Symp. NVMSA 2018*, 2018, 113–114.

37 G. S. Park, Y. B. Kim, S. Y. Park, X. S. Li, S. Heo, M. J. Lee, M. Chang, J. H. Kwon, M. Kim, U. I. Chung, R. Dittmann, R. Waser and K. Kim, *Nat. Commun.*, 2013, **4**, 1–9.

38 C. Baeumer, R. Valenta, C. Schmitz, A. Locatelli, T. O. Menteş, S. P. Rogers, A. Sala, N. Raab, S. Nemsak, M. Shim, C. M. Schneider, S. Menzel, R. Waser and R. Dittmann, *ACS Nano*, 2017, **11**, 6921–6929.

39 U. Celano, L. Goux, A. Belmonte, K. Opsomer, C. Detavernier, M. Jurczak and W. Vandervorst, *IEEE Int. Reliab. Phys. Symp. Proc.*, 2015, **2015-May**, MY111–MY113.

40 A. Fantini, D. J. Wouters, R. Degraeve, L. Goux, L. Pantisano, G. Kar, Y. Y. Chen, B. Govoreanu, J. A. Kittl, L. Altimime and M. Jurczak, *2012 4th IEEE Int. Mem. Work. IMW 2012*, 2012, 9–12.

41 D. Y. Cho, M. Luebben, S. Wiefels, K. S. Lee and I. Valov, *ACS Appl. Mater. Interfaces*, 2017, **9**, 19287–19295.

42 A. Hardtdegen, C. La Torre, F. Cuppers, S. Menzel, R. Waser and S. Hoffmann-Eifert, *IEEE Trans. Electron Devices*, 2018, **65**, 3229–3236.

43 K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki and Y. Sugiyama, *Appl. Phys. Lett.*, 2008, **93**, 033506.

44 Y. S. Fan, L. Zhang, D. Crotti, T. Witters, M. Jurczak and B. Govoreanu, *IEEE Electron Device Lett.*, 2015, **36**, 1027–1029.

45 D. Carta, I. Salaoru, A. Khiat, A. Regoutz, C. Mitterbauer, N. M. Harrison and T. Prodromakis, *ACS Appl. Mater. Interfaces*, 2016, **8**, 19605–19611.

46 S. J. Mason, D. J. Wesenberg, A. Hojem, M. Manno, C. Leighton and B. L. Zink, *Phys. Rev. Mater.*, 2020, **4**, 1–12.

47 E. A. Scott, J. T. Gaskins, S. W. King and P. E. Hopkins, *APL Mater.*, 2018, **6**, 058302.

48 S. Sandell, J. Maire, E. Chávez-ángel, C. M. S. Torres, H. Kristiansen, Z. Zhang and J. He, *Nanomaterials*, 2020, **10**, 1–11.

49 J. C. Duda, C. Y. P. Yang, B. M. Foley, R. Cheaito, D. L. Medlin, R. E. Jones and P. E. Hopkins, *Appl. Phys. Lett.*, 2013, **102**, 081902.

3.7 Appendix

3.7.1 Electrical characterization in RRAM

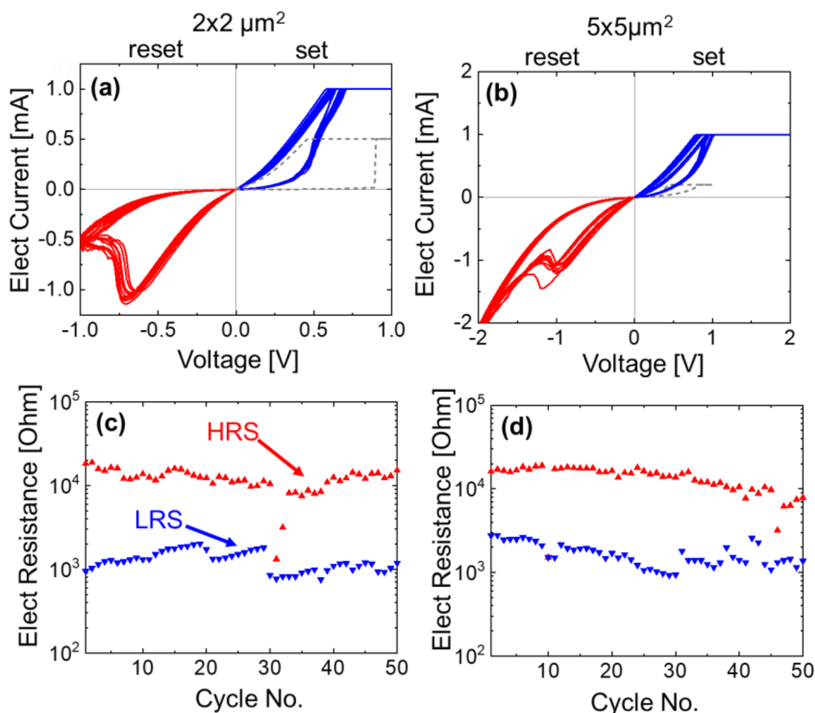

Figure 3.13 (a,b) Electric current as a function of the electrical voltage during the set (blue) and reset process (red) for 10 cycles in a **(a)** 2x2 μm^2 and in a **(b)** 5x5 μm^2 device. The grey dashed curves show the forming process. **(c,d)** Electrical Resistance in the high resistive state (HRS) in red and the low resistive state (LRS) in blue of the RRAM devices vs number of cycles for a cross-point area size of **(c)** 2x2 μm^2 and **(d)** 5x5 μm^2.

For the electrical switching process of our resistive random access memory (RRAM) devices we performed electric voltage sweeps using a semiconductor parameter analyzer (SPA). Before we have formed the filament, we used an initial current compliance of I_{cc} = 1 μA, in order to

decrease the severity of overshooting effects. However typically we required to use higher compliances in order to form the filament completely. The forming voltage ($V_{forming}$) in between devices varied usually in the range of 0.5 to 2 V having a higher magnitude than the subsequent set voltage which is in line with observations in the literature.[1] After the forming process we reset the device by applying a reversed bias with a higher I_{cc} than in the last set or forming process. To ensure the cyclability of the devices we set and reset them for at least 10 cycles before we checked them with the scanning thermal microscope (SThM).

Fig. 3.13 (a,b) show two examples of one 2x2 μm^2 and one 5x5 μm^2 devices representing ten full cycles. During the cycles we applied a constant current compliance during the set process to achieve consistent set conditions.

Fig. 3.13 (c,d) show the electrical resistance in the high resistive state (HRS) and the low resistive state (LRS) for two devices with a cross-point area of (c) 2x2 μm^2 and (d) 5x5 μm^2 during 50 full cycles. The HRS and LRS values were read at 0.07 V before and after the switching in the set process. The results support that our devices are capable of switching for more than 50 cycles.

3.7.2 Hot spot location with cycling

For the characterization of the hot spot moveability, we repeated the steady state measurements of the devices after *I*-*V* cycling, Fig. 3.14 (a) and (b) show two examples of heat dissipation in set devices different from the ones presented before at different stages of cyclability for a (a) 2x2 μm^2 and (b) 5x5 μm^2 device. In addition to the maps of Fig. 3.10, we observed a static hot spot position in the 2x2 μm^2 device while a shift of the hot spot occurred in the 5x5 μm^2 device.

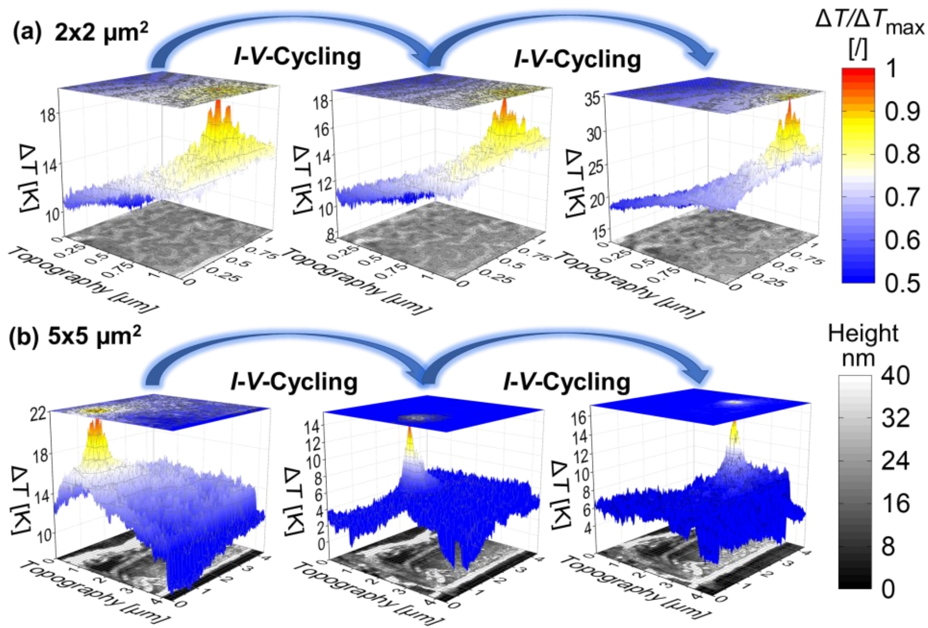

Figure 3.14 3D surface temperature maps (z-axis) plotted over the 2D topography (x and y axis) of devices with an area of **(a)** 2x2 μm^2 and **(b)** 5x5 μm^2. The 2D topographic maps at the bottom show the height differences in the scanned area (greyscale bar on the bottom right). The color scheme of the 3D plots shows the temperature increase during the steady state measurements (colored bar on the top right). Power (*P*) applied to the devices during the scans in **(a)** are 0.33 mW/0.32 mW/0.59 mW and in **(b)** are 0.27 mW/0.55 mW/0.47 mW from left to right.

3.7.3 Simulation characteristics

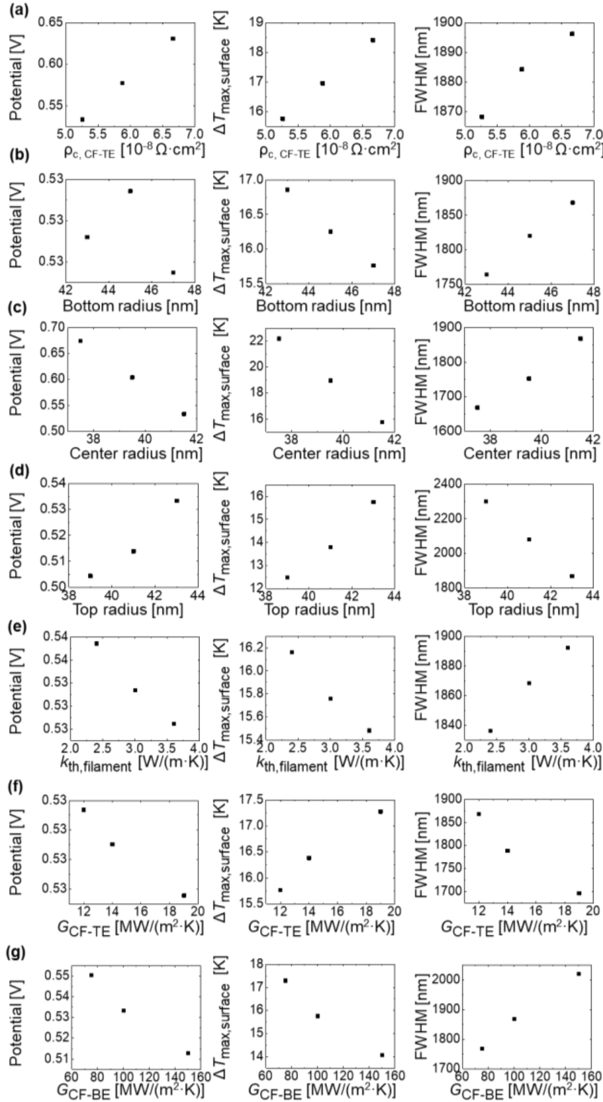

Figure 3.15 Potential, maximum temperature increase at the surface of the device $\Delta T_{max,surface}$ and full width at half maximum (FWHM) of the hot spot temperature profile as a function of the simulation parameters **(a)** $\rho_{C, CF\text{-}TE}$, **(b)** bottom radius, **(c)** center radius, **(d)** top radius, **(e)** $k_{th,filament}$, **(f)** $G_{CF\text{-}TE}$, **(g)** $G_{CF\text{-}BE}$ as described in section 3.3.3.

Regarding the simulation results displayed in chapter 3.3.3 it is worth noting that the characteristics of the simulated device parameters are chosen to be in align with results of the experiments. Furthermore, the simulated device characteristics are selected to be in a similar range as previous realistic results where the study by Deshmukh *et al.*[9] is serving as a reference. Consequently, this solution can be perceived as part of a range of potential fitting solutions. Fig. 3.15 depicts the interplay of the characterized input and output parameters visualizing the influence of each parameter on the outcome.

Fig. 3.15 (a) shows that the potential significantly increases with the electrical contact resistance of the filament and the top electrode $\rho_{C,\ CF\text{-}TE}$. As the network can be understood as a series of resistances including the filament, electrodes and contacts, the total electrical resistance rises with $\rho_{C,\ CF\text{-}TE}$. With current held constant the potential therefore rises at the same time. Consequently, the heating power becomes larger culminating in elevated temperatures at the surface.

Fig. 3.15 (b-d) reveals the impact of the geometrical parameters of the filament on the results. The electrical potential is dominated by the center radius which defines the path of electrical current. The electrical resistance and therefore the potential decreases when the radius increases. Similar to the case in (a) this change results in a reduction of the maximum temperature. However, the heating confines at a lower center radius, resulting in a lower FWHM. Fig. 3.15 (e) shows that the thermal conductivity of the filament has a limited impact on the characteristics.

Interestingly, when comparing Fig. 3.15 (b) and (d), as also (f) and (g), one can observe that both the bottom radius and top radius as also the thermal contact conductance between the filament and the bottom electrode $G_{CF\text{-}BE}$ and the top electrode $G_{CF\text{-}TE}$ have opposing trends in their heating characteristics. When the bottom radius or $G_{CF\text{-}BE}$ increases, the generated heat preferably flows through the bottom electrode and therefore leads to a lower surface temperature. The opposite effect is expected with the parameters of the top radius and $G_{CF\text{-}TE}$.

Chapter 4 Thermal rectification in multilayer phase change material structures for energy storage applications

Abstract

Solid-state thermal control devices that present an asymmetric heat flow depending on thermal bias directionality, referred to as thermal diodes, have recently received increased attention for energy management. The use of materials that can change phase is a common approach to design thermal diodes, but typical sizes, moderate rectification ratios, and narrow thermal tunability limit their potential applications. In this work, we propose a multilayer thermal diode made of a combination of phase change and invariant materials. This device presents state-of-the-art thermal rectification ratios up to 136% for a temperature range between 300 K and 500 K. Importantly, this design allows to switch between distinct rectification states that can be modulated with temperature, achieving an additional degree of thermal control compared with single-rectification-state devices. We analyze the relevance of our thermal diodes for retaining heat more efficiently in thermal storage elements.

This chapter is derived from the publication:

T. Swoboda, K. Klinar, S. Abbasi, G. Brem, A. Kitanovski and M. Muñoz Rojo, iScience, 2021, 24, 102843.

4.1 Introduction

In recent years, solid-state thermal control devices[1] have received increased attention as a potential solution for improved energy management, storage or conversion.[1–4] Thermal diodes, regulators, switches or transistors are capable to manage heat in a manner analogous as how electricity is controlled by their electrical counterparts.[5] Among this toolkit of richer thermal control elements, thermal diodes have received special attention for their unique opportunities in solar thermal energy harvesting[5], caloric refrigeration[5,6] or in thermoelectric modules.[5,7] In thermal diodes, also referred to as thermal rectifiers, the heat flows preferably in one direction, resulting in an asymmetric transfer function.[8–10] The performance of a thermal diode is usually determined by the rectification ratio,

$$RR = \frac{|q_{\mathrm{fwd}}|-|q_{\mathrm{rev}}|}{|q_{\mathrm{rev}}|} \cdot 100\% \tag{4.1}$$

where q_{fwd} and q_{rev} are heat fluxes in the forward (i.e., considered as the higher magnitude of heat flux) and reverse direction (i.e., lower magnitude of heat flux), respectively, when an equal temperature gradient along the device is considered in both directions.

Current approaches to develop solid-state devices with high thermal rectification ratios are typically based on material engineering[11–22] or on a combination of materials with dissimilar properties. Among the materials proposed, PCMs with a solid to solid phase transition are one of the most popular approaches for designing a thermal diode.[23–26] Some PCMs present a phase transition at a critical temperature (T_{trans}), which leads to a change in the thermal conductivity of the material. As an example, VO_2[27,28] is a well-known PCM, widely used for the development of smart windows[29,30] and electronic devices[31,32], that has been studied as thermal rectifier.[23,24,33] It typically presents a phase change transition at $T \sim 340$ K,[34] that results in a change of the lattice structure, from a monoclinic insulating to a tetragonal metallic phase.[35,36] While dynamic changes in the structure of materials are very attractive to develop thermal diodes, the thermal conductivity variation in PCMs is typically moderate.[37] Alternatively, PCMs like VO_2 can be combined with a phase invariant material (PIM), like Si, to enhance their thermal rectification properties by inducing larger asymmetry in the heat flux across this structure.[23–25]

Fig. 4.1 shows an overview of the rectification values obtained in the field of PCM thermal rectification and the obtained *RR* values of the diode design proposed in this work. On the one hand, a rectification ratio of up to *RR* = 28

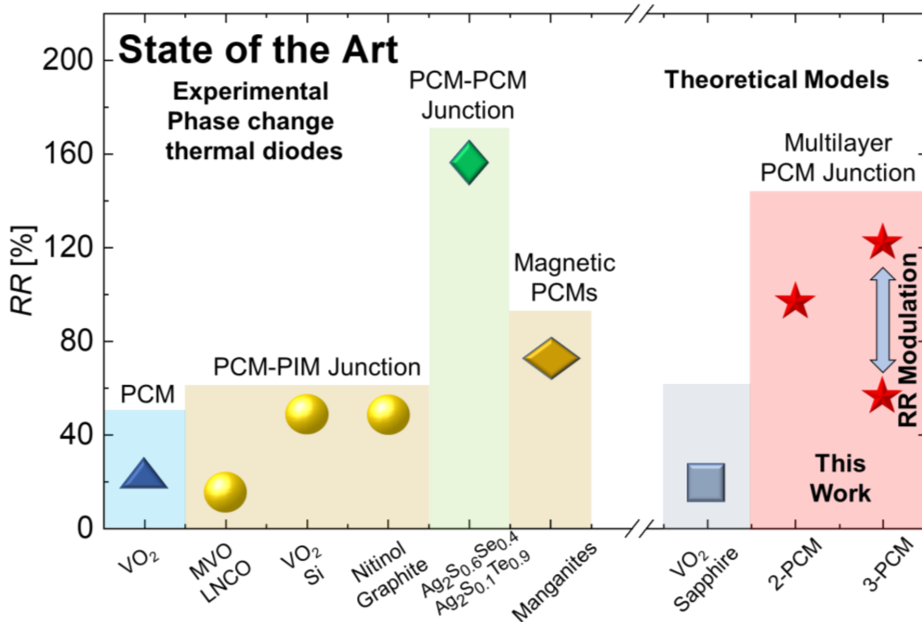

Figure 4.1 State of the art thermal rectification ratio of some of the most relevant thermal diodes and the results of our proposed multilayer diodes for both experimental and theoretical values (2-PCM diode based on PCM_1: Ag_2Te - PIM_1: SiO_2 - PCM_2: $Ag_2S_{0.6}Se_{0.4}$ - PIM_2: Si; 3-PCM diode based on PCM_1: $Ag_2S_{0.6}Se_{0.4}$ - PIM_1: Si PCM_2: $Ag_2S_{0.8}Se_{0.2}$ - PIM_2: SiO_2 - PCM_3: Ag_2Te - PIM_3: Si).[20,24,25,33,38,40,48] For more information about other theoretical and experimental types of thermal diodes based on different operating principles are presented in chapter 1.3.

% has been observed in a pure PCM structure made of a VO_2 beam with an asymmetric shape.[20] On the other hand higher rectification ratios of up to *RR* = 50 % have been observed by combining PCMs like VO_2[24,26] or Nitinol[38] with a PIM. Other examples include MVO (PCM) LNCO (PIM) structures that present a thermal rectification ratio of 14 % at low temperatures (~55 K). Additionally, the combination of two different PCMs is promising for potentially higher thermal rectification values.[39–41] More specifically, a thermal diode with *RR* = 170 % was found by combining two PCMs with an increase ($Ag_2S_{0.6}Se_{0.4}$) and a decrease ($Ag_2S_{0.1}Te_{0.9}$) in thermal conductivity

with temperature.[40] All these efforts aim to the development of high rectification ratio thermal diodes that bring promising opportunities for thermal management in electronics,[42–45] caloric refrigeration[5,6] or new thermal technology, like heat logic.[46]

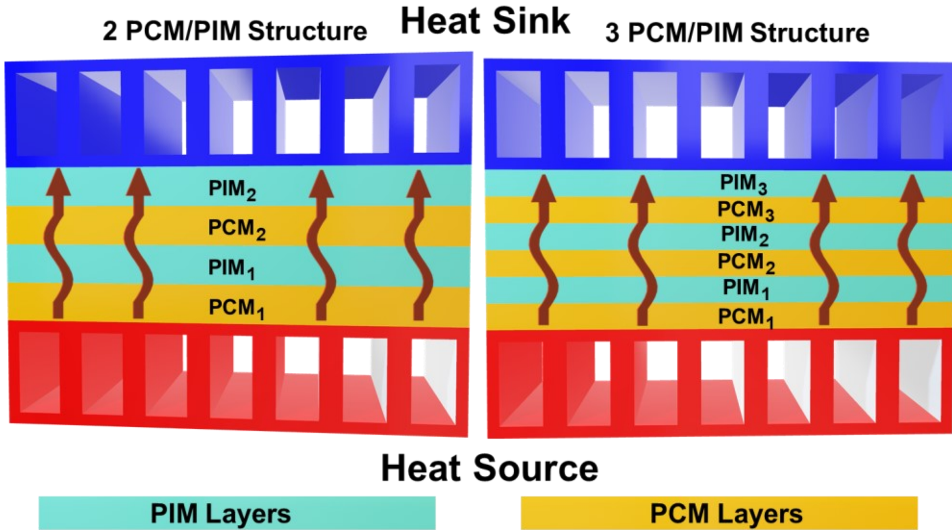

Figure 4.2 Schematic drawing of two diode configurations (left 2 PCM diode, right 3 PCM diode) proposed in this work. The arrows indicate the heat flux direction from the heat source to the heat sink.

In this chapter, we report a distinct approach towards the design of realistic and experimentally achievable thermal diodes using multilayer structures based on PCMs and PIMs. This approach combines the strategies used in PCM-PIM and PCM-PCM devices to develop a novel thermal diode design with high performance and distinct rectification states for advanced thermal control. In chapter 4.2 a FEM model is used to evaluate the optimum design configuration that maximizes the thermal rectification in these structures. Using this tool, we evaluate different geometries (2-PCM/PIM vs 3-PCM/PIM diodes), temperature ranges and material configurations. In Section 4.3, we determine the thermal rectification ratios *RR* to be 106 %, and 133% for the 2-PCM and 3-PCM structures for a thermal bias ΔT = 95 K and ΔT = 170 K respectively ($\Delta T = T_{source} - T_{sink}$). Our approach shows a functional, adjustable thermal diode design, which can be applied for various material configurations. Additionally, we observe that the rectification properties of our

3-PCM can be modulated between an intermediate *RR* to a high *RR* state depending on the thermal bias (ΔT). This feature shows a clear difference from previously reported single rectification state thermal diodes and enables another degree of freedom for thermal management applications. Finally, in Section 4.4, we determine the ability of this diode to retain energy when it is integrated in thermal storage elements.

4.2 Modelling approach

4.2.1 Geometry

The proposed design of the thermal diode consists of a stack of multiple PCM and PIM layers in an alternating configuration (see Fig. 4.2). This design expands current configurations of PCM and PIM diode structures, which are mentioned in the introduction.[23–25,33,38] These diodes specially aim to not only enhance the rectification ratio by using distinct multilayer structures but also to develop a device that is experimental achievable to warrant its use for energy management applications. In order to compare the two examined structures properly we choose to use the same geometrical dimensions in both cases as indicated in Fig. 4.3 (a) and (b). Therefore, we combine individual rectangular shaped polygons to form structures with a total length and width of *l* = 1.2 μm, *w* = 0.6 μm respectively. The length values of each polygon are equally distributed throughout the design. Thus, in the 2-PCM diode the polygons have a length of 0.3 μm, while being 0.2 μm in the 3 PCM

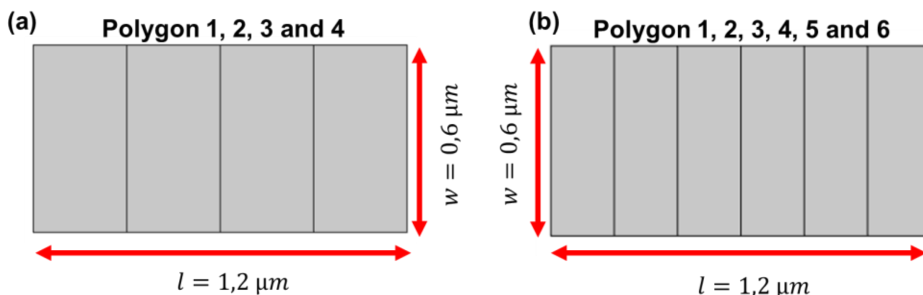

Figure 4.3 (a) Geometry of the 2-PCM diode used in the FEM COMSOL simulations presented in this study. The geometry contains 4 equally shaped rectangular polygons, and it has a total length and width of *l* = 1.2 μm, *w* = 0.6 μm respectively. **(b)** Geometry of the 3-PCM diode used in the FEM COMSOL simulations presented in this study. The geometry contains 6 equally shaped rectangular polygons, and it has a total length and width of *l* = 1.2 μm, *w* = 0.6 μm respectively.

diode. The performance of these thermal diodes is analyzed through FEM, using COMSOL® Multiphysics based on the assigned materials of the individual polygons.

4.2.2 Material selection

The individual polygons are connected to two types of materials, PIMs and PCMs. The material properties are applied to the individual polygons of the geometry as indicated in Fig. 4.4 (a) and (b). In that sense we only consider

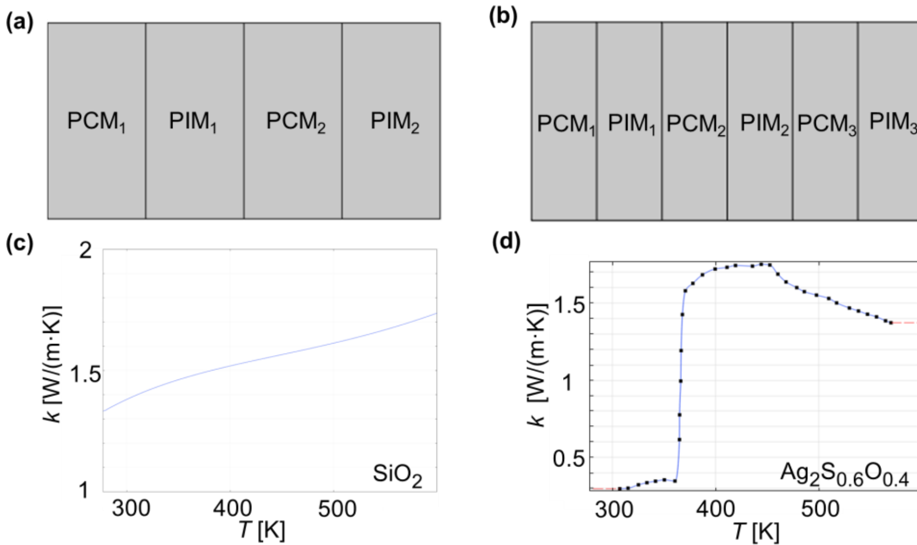

Figure 4.4 (a) Material configuration in the 2-PCM diode structure, **(b)** Material configuration in the 3-PCM diode structure. Thermal conductivity values used in the COMSOL simulations of **(c)** SiO_2 (COMSOL data base) and **(d)** $Ag_2S_{0.6}O_{0.4}$ [40] as a function of temperature.

PCMs for the PCM denoted polygons and only PIMs for PIM denoted Polygons. Both structures consist then of a multilayer material configuration with alternating PCM and PIM layers.

The thermal conductivity values of the PIMs are taken from the COMSOL Database. We only consider PCMs with a solid to solid phase transition to completely remain in solid-state. The maximum and minimum thermal conductivity values of the included PCMs below and above the transition temperature T_{trans} are shown in Table 4.1. We extract experimental data from PCMs which present a strong change in their thermal conductivity along their phase transition from the literature. Hereby, COMSOL allows to include the temperature dependency of the thermal conductivity of the materials

included. For example, the graphical illustration of thermal conductivity of the COMSOL model of the PIM SiO_2 and the PCM $Ag_2S_{0.6}O_{0.4}$ are presented in

Table 4.1 Reported maximum and minimum thermal conductivity values (*k*) of the used phase change materials (PCM), which changes at around the transition temperature (T_{trans}). The PCMs are distinguished between type A and type B PCMs as they present an increase (type A) or decrease (type B) in thermal conductivity above T_{trans}.[37,40,49] Additionally the source of data for the two used phase invariant materials (PIM) are presented.

Material	*k* [W/(m·K)] ($T<T_{trans}$)	*k* [W/(m·K)] ($T>T_{trans}$)	T_{trans} [K]	Type		Reference
PCMs						
Ag_2S	0.5	1	450	A		42
Cu_2Se	0.6	0.9	400	A		42
Ag_2Se	1.15	0.8	400	B		42
Cu_2S	0.45	0.33	380	B		42
Ag_2S	0.5	1.3	450	A		40
$Ag_2S_{0.8}Se_{0.2}$	0.45	1.2	400	A		40
$Ag_2S_{0.6}Se_{0.4}$	0.25	1.6	360	A		40
$Ag_2S_{0.4}Se_{0.6}$	0.7	2.1	350	A		40
$Ag_2S_{0.2}Se_{0.8}$	1.5	2	350	A		40
Ag_2Se	1	0.75	400	B		40
Ag_2Te	1	0.5	420	B		40
$Ag_2S_{0.05}Te_{0.95}$	1.2	0.7	400	B		40
$Ag_2S_{0.1}Te_{0.9}$	1.5	0.7	380	B		40
$Ag_2S_{0.15}Te_{0.85}$	1.8	0.8	340	B		40
VO_2	3.5	5.5	340	A		37
PIMs						
Si			No phase transition			COMSOL Database
SiO_2			No phase transition			COMSOL Database

Fig. 4.4 (c) and (d) as a function of the temperature.[40]

We define type A and type B PCMs as those that exhibit increased and decreased thermal conductivity above the transition temperature, respectively. In both configurations, type A and type B PCMs are combined in an order such that the PCMs are exclusively in their high conductive state in the forward direction while being in the low conductive state in the reverse direction. For the PIM layers we consider a higher conductive material (Silicon) and a lower conductive material (SiO_2) which are predefined in the COMSOL database. The temperature drop in the PIM layers enables a better combination of PCMs with different phase transition temperatures. As a result of that we make sure that each PCM possesses the ideal transition temperature in the applied temperature range. The rectification characteristics of each possible material combination under the predefined configuration is evaluated. Meaning that each of the PCMs in Table 4.1 are considered for the PCM layers of the structure while each PIMs are considered for the PIM layers of the structure. The different material combinations are evaluated by means of a material sweep as specified in section 4.2.5.

4.2.3 Heat transfer model

After the definition of the materials, we use this COMSOL model to analyze the thermal transport in our 2-PCM and 3-PCM diodes. The thermal rectification ratio is calculated along the length of the structure. In order to create a heat flux, we apply a temperature gradient between the two heat terminals on the left and right side edge of the structure, as indicated in Fig. 4.5 (a). One terminal is at a temperature of T_{source}, while the other one is at T_{sink} (forward direction). The position of T_{source} and T_{sink} is swapped (forward vs reverse) in order to evaluate the heat flux of the structures depending on its directionality. In our model the forward direction is always related to the heat terminal configuration which creates the higher magnitude in heat flux. The top edge of the structure is thermally insulating, to verify that the heat flux is only transported between the terminals. To create a quadratic design of the diode, symmetry is implemented at the bottom edge of the structure. The interfacial resistance is located at the transition edge between material layers (see Fig. 4.5 (d)). The aim of this chapter is to compare the potential of the different layer designs (2PCM vs 3 PCM thermal diode) and their thermal rectification performances. Therefore, we use fixed temperature boundary conditions and compare the resulting differences in the thermal conductivity in both directions. It is worth noting that this method allows a fast evaluation but, it also faces limitations such as heat losses or the

influence of contact resistances when it comes to the integration of these structures in applications. In section 4.4.5 we discuss the potential impact of thermal contact on our results.

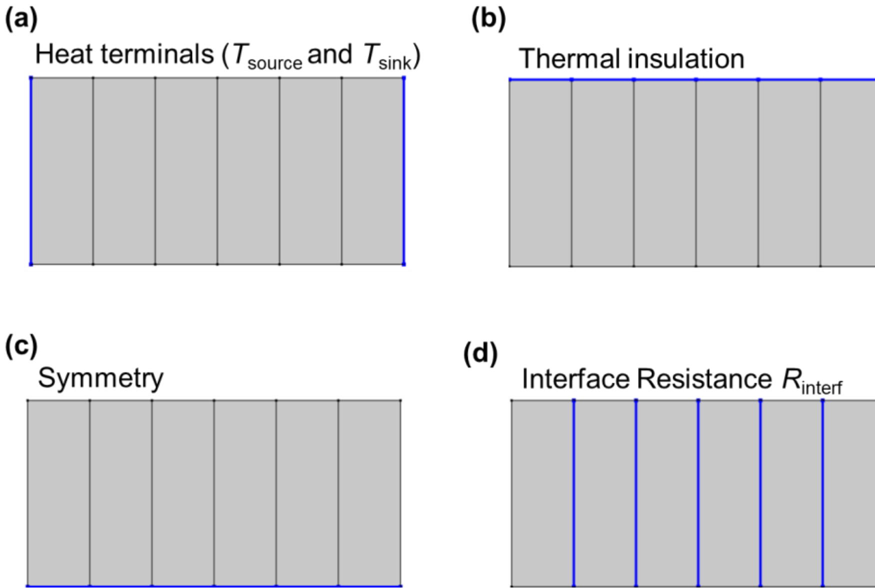

Figure 4.5 (a) Implemented heat terminals T_{source} and T_{sink} to induce a temperature gradient ($T_{source} > T_{sink}$). In the forward heat flux calculations one of the terminals has a temperature equal T_{source} while the other one is equal T_{sink}. In the reverse case the two temperature terminals are swapped. The initial temperature is at ambient conditions, **(b)** applied thermal insulation at the top of the structure, **(c)** applied Symmetry at the bottom of the structure, **(d)** applied interface resistances (R_{interf}) in between the different material layers.

For the characterization of the rectification characteristics, we first fix the temperature of the heat sink (cold side), T_{sink}, at 300 K while varying the temperature of the heat source (hot side), T_{source}, between 300 K and 550 K. The structures are assumed to be thermally insulated at the edges, thus potential heat losses by convection or radiation with the surrounding environment are not included. The heat flux (q), across the structure is calculated in steady state for both cases using Fourier's law,

$$q = -k \cdot \nabla T \tag{4.2}$$

where k is the thermal conductivity of the material and ∇T the temperature gradient across the material.

Additionally, in this model we also account for thermal interface resistances. According to reference[47] the thermal conductance at the border of two dissimilar material, i.e., the thermal interface conductance (G_{interf}) falls within a narrow range of values. Based on their results[47] we approximate the thermal interfacial conductance between layers to be ~100 MW/(m^2·K), which is equal to a thermal interface resistance (R_{interf}) of ~10^{-8} (m^2·K)/W. The number of interfaces between blocks (n_{interf}), is 3 in the case of the 2 PCM diode and 5 in the case of the 3 PCM diode structure. Later in this chapter, we discuss how changes in the thermal interface resistances possibly affect the result of the thermal rectification.

4.2.4 Mesh

In order to reduce the calculation time during our study, we choose to use a coarser mesh element size that possibly doesn't affect the accuracy of the results. The coarse element size is predefined ranging from minimum 2.4 nm up to a maximum of 120 nm. Additionally, we implement a fixed number of elements (20) at the edges in between materials, to increase the accuracy in transitions (see Fig. 4.6 (a) and (b)). Once we find the ideal material configuration by means of the Material sweep, we recalculate the results of the heat flux, by using a finer element size. Therefore, we adjust the fixed number of elements at the layer edges gradually. Finally, we check the results for an extremely coarse mesh without using a fixed number of elements. Fig. 4.6 (c) and (d) show the calculated heat flux in forward and reverse direction of the structures presented in Section 4.3 as a function of the minimum mesh element size of the model. Here we can see that the results barely change when we use finer meshes. However, we observe a small but significant change in the results when using the extremely coarse mesh (minimum mesh element size 60 nm).

As a result, we can confirm that certain coarse meshes are sufficiently accurate and that too fine meshes are not necessary in this study since it mostly extends the computing time.

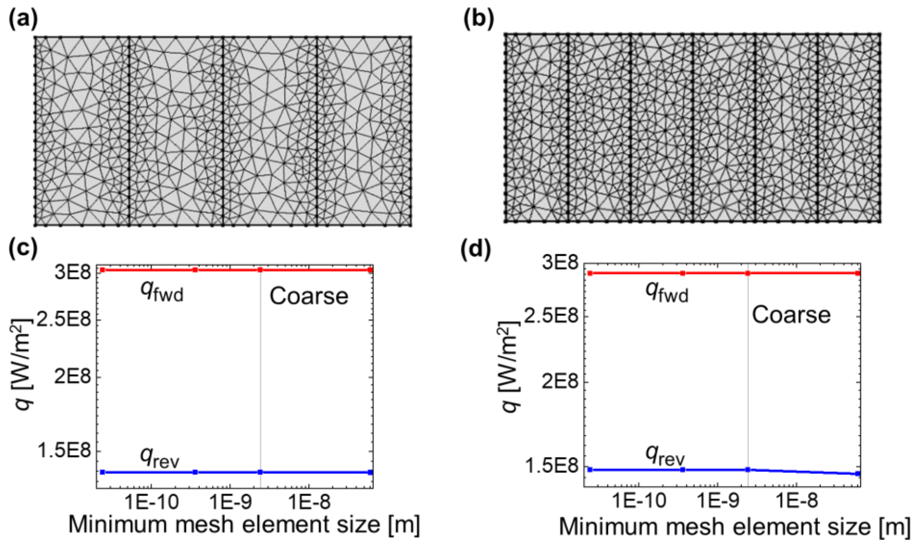

Figure 4.6 Mesh of the **(a)** 2PCM structure and **(b)** 3PCM structure used in the COMSOL simulations (maximum Element size 120 nm, minimum element size 2.4 nm, fixed number of 20 elements at every transition line). Calculated heat flux in forward (red lines) and reverse (blue lines) direction as a function of the minimum mesh element size of the COMSOL geometry of the **(c)** 2 PCM and **(d)** 3 PCM material configuration described in Section 4.3. The vertical lines in **(c)** and **(d)** correspond to the results obtained with the Coarse mesh presented in **(a)** and **(b)**.

4.2.5 Study

We apply a material sweep to find the optimal material configuration. Therefore, we consider every possible material combination (see Table 4.1), related to the alternating PCM/PIM structures indicated in Fig. 4.4 (a) and (b). For each case we calculate the conductive heat flux in x-direction (along the structure) using a stationary solver. Given the fact that our structures represent a series of heat resistances, the heat flux is constant along them. In order to eliminate minor fluctuations at phase transitions we determine the average heat flux of all layers. We repeat the same procedure, while reversing the temperature gradient. COMSOL then allows to calculate the result of each possible material combination. We then calculate the rectification ratio *RR* by using equation 4.1 of this chapter. Therefore, we presuppose that $|q_{\mathrm{fwd}}| > |q_{\mathrm{rev}}|$ in every configuration.

4.3 Results

4.3.1 Rectification ratio of 2- & 3- PCM/PIM multilayers at a constant thermal bias

For the 2-PCM/PIM multilayer structure, we use the reported material data to determine the ideal material combinations that maximize the rectification performance of this diode. For a thermal bias of ΔT = 200 K (heat source and sink at 500 K and 300 K, respectively), the highest rectification ratio of $RR \approx$ 96 % is obtained for the following 4 layers material configuration: PCM_1: Ag_2Te - PIM_1: SiO_2 - PCM_2: $Ag_2S_{0.6}Se_{0.4}$ - PIM_2: Si.

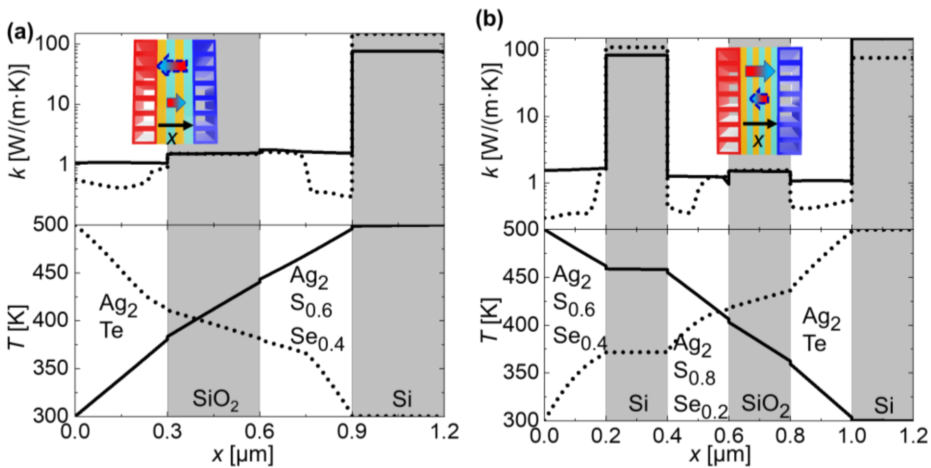

Figure 4.7 Thermal conductivity and temperature profile of the **(a)** 2 PCM structure as a function of *x,* as indicated in the inset drawing and; **(b)** 3PCM structure as a function of *x* as indicated in the inset drawing. The solid and dotted lines correspond to the forward and reverse direction, respectively. The dotted arrows in the inset drawings represent the heat flux magnitudes when the temperature reservoirs are exchanged. The directions with preferred heat transfer are indicated by larger gradient arrows in the inset drawings. The inset drawings show that the arrows are reversed for the 2PCM vs 3PCM designs, which is due to the new material layers and their differences in phase change transition temperatures.

Fig. 4.7 (a) presents the temperature profiles across the structure and thermal conductivities of each layer in the forward and reverse directions for the 2-PCM diode. The effective thermal conductivity in the reverse and

forward direction is $k_{eff,rev}$ ≈ 0.89 W/(m·K), and $k_{eff,fwd}$ ≈ 1.74 W/(m·K), respectively.

In Fig. 4.7 (a), when the heat flows from right to left in the inset figure, the temperature gradient across the two PCMs is above their phase transition temperature, leading to low thermal resistance (PCMs with high thermal conductivity – forward direction). When the heat flow is reversed (left to right), the temperature gradient across the PCM is mainly below the phase transition temperature, resulting in higher thermal resistance phases (PCMs with lower thermal conductivity – reverse direction). Apart from that, the PIMs, Si or SiO_2, present almost negligible variation in its thermal conductivity. In Fig. 4.7 (a) the temperature drop across the PCM and PIM materials is plotted. In the forward direction (PCM_1:Ag_2Te at low temperatures), the temperature drop in SiO_2 warrants that the temperature in PCM_1 Ag_2Te is below its transition temperature across the whole layer. In the reverse direction, the temperature drop in the SiO_2 layer enables the temperature in PCM_2 $Ag_2S_{0.6}S_{0.4}$ to fall below the phase transition temperature. Therefore, the PIM layers allow a better control of the transition temperatures for the PCM layers involved.

Similarly, as for the 2PCM/PIM diode, we use the reported data to determine the thermal rectification ratio in a 3-PCM/PIM multilayer diode configuration. The highest rectification ratio for a thermal bias of ∇T = 200 K (heat source and sink at 500 K and 300 K, respectively) is found to be RR ≈ 119 %, corresponding to the following 6 layer configuration: PCM_1: $Ag_2S_{0.6}Se_{0.4}$ - PIM_1: Si PCM_2: $Ag_2S_{0.8}Se_{0.2}$ - PIM_2: SiO_2 - PCM_3: Ag_2Te - PIM_3: Si. The effective thermal conductivity in the reverse and forward directions is $k_{eff,rev}$ ≈ 0.83 W/(m·K) and $k_{eff,fwd}$ ≈ 1.82 W/(m·K), respectively. Fig. 4.7 (b) presents the temperature gradient across the diode and the thermal conductivity values of each layer. On the one hand, we can see that in the forward direction, when the heat flows from left to right in the inset figure, all the PCM materials are mostly in their high thermally conductive phases. On the other hand, all PCMs are in their low thermally conductive phases when the heat flow is reversed, except small segments in PCM_1 and PCM_2 that are in their high conductive states.

If we compare these results with those presented for 2-PCM/PIM structure in Fig. 4.7 (a), we observe that the number of PCM layers being in their low conductive phase in reverse direction for this temperature gradient is higher.

Therefore, a 3-PCM multilayer structure provides a greater degree of thermal control compared to a 2-PCM structure.

4.3.2 *RR* of 2- & 3-PCM/PIM multilayers vs heat source temperature

The rectification ratio of 2- and 3- PCM/PIM multilayer structures is also studied for different values of T_{source}. For that purpose, we fix T_{sink} at 300 K and vary T_{source}. In that context, we use the material configuration with the highest *RR* to investigate the impact of T_{source} on the rectification behavior. Therefore, we apply a parametric sweep in which we calculate *RR* for the aforementioned structures by varying T_{source} from 300 to 550 K with 1 K steps. We choose this temperature range, because the used experimental data of the PCM materials does not present values above 550 K. The results of this analysis are presented in Fig. 4.8.

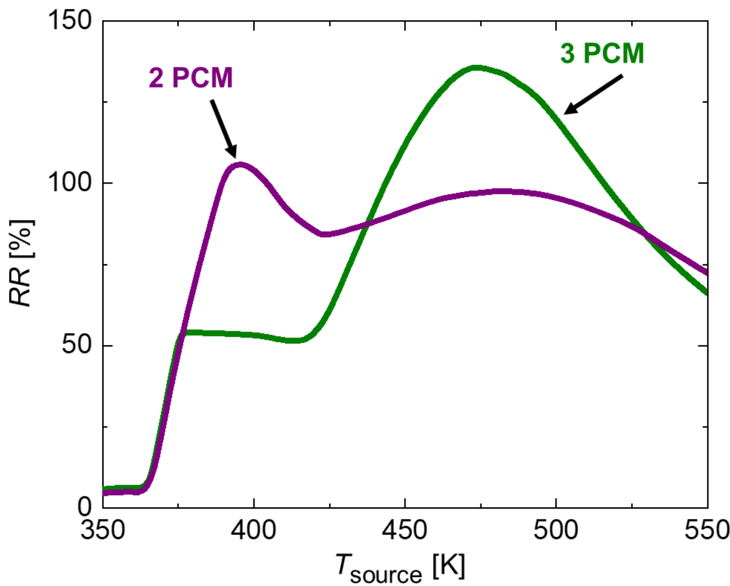

Figure 4.8 Thermal rectification ratio of 2-PCM/PIM (PCM_1: Ag_2Te - PIM_1: SiO_2 - PCM_2: $Ag_2S_{0.6}Se_{0.4}$ - PIM_2: Si) and 3- PCM/PIM (PCM_1: $Ag_2S_{0.6}Se_{0.4}$ - PIM_1: Si PCM_2: $Ag_2S_{0.8}Se_{0.2}$ - PIM_2: SiO_2 - PCM_3: Ag_2Te - PIM_3: Si) multilayer structures as a function of the temperature of the heat source.

Fig. 4.8 displays the results of the rectification ratio of both structures as a function of T_{source}. In the 3-PCM/PIM multilayer structure the highest $RR \approx$

133 % is found for T_{source} = 470 K, while for the 2-PCM/PIM structure a maximum $RR \approx 106\%$ is achieved at T_{source} = 395 K.

As can be seen in Fig. 4.8, nearly no rectification can be observed around 350 K as the temperature of the structure is below the transition temperatures of the PCMs. The small values observed are due to temperature dependent materials thermal properties. In both structures the rectification ratio rises for temperatures higher than T_{trans} of the common PCM block made of $Ag_2S_{0.6}Se_{0.4}$ (T_{trans} ~ 360 K). A higher rectification ratio is achieved for the 2-PCM/PIM multilayer structures for intermediate temperature ranges (375 K < T < 425 K). Differently, for temperatures between 425 K and 525 K, the 3-PCM/PIM multilayer structure leads to higher rectification ratios. Finally, when the temperature becomes above ~ 470 K, the rectification ratio drops as the temperature across PCMs remains above T_{trans} for both forward and reverse directions. Especially interesting is that the *RR* vs *T* dependency of the 3 PCM diode structure increases stepwise from an intermediate value for temperatures at around ~ 400K to higher values at higher temperature, reaching the peak at ~ 470 K. This is related to a stepwise increase of the thermal conductivity in the forward direction. For intermediate temperature only PCM_1 is in its high conductive state in forward direction. When T_{source} is going above 425 K, PCM_2 and PCM_3 start to transition to its high conductive state up to the ideal configuration at around 470 K.

As a result, this thermal diode shows promising properties as a multistate thermal regulator. A temperature gated sequential thermal rectification effect has been previously reported by Martinez-Flores *et al.*[48] in a manganite based material system. However, our results distinguish from them as well as other ones on the fact that we use different materials, multiple segments and two distinct rectification states that are stable in a certain temperature range. In the 2-PCM diode graph the maximum rectification is reached at T_{source} = 395 K. At this point PCM_2 is completely in its low conductive state in the reverse direction. When increasing T_{source} PCM_2 partially transition to its high conductive state in reverse direction and thus *RR* decreases until it reaches a minimum at 423 K. Above this temperature PCM_1 starts to transition to its low conductive state in the reverse direction and as a result *RR* rises again. PCM_1 and PCM_2 remain in their high conductive state in forward direction for T_{source} > 380 K, so the changes in the *RR* are created due to changes in the reverse configuration (see Fig. 4.9 (a)). We choose this temperature range, because the used experimental data of the PCMs does not present values above 550 K. However, we expect that *RR* will fall

down to zero when further increasing T_{source}, as at these temperatures all PCMs will remain above T_{trans} in both directions. Finally, the design parameters of the thermal diode, like temperature, PCMs or PIMs, size or geometry, can be adjusted depending on the application targeted.

4.3.3 Calculation of thermal conductivity vs heat source temperature

The effective thermal conductivity for the diode configurations is calculated by using the basic definitions of the thermal resistance ($R_{thermal}$), presented in equation 4.3 and 4.4,

$$R_{\mathrm{thermal}} = \frac{l}{k_{\mathrm{eff}} \cdot A} \quad (4.3)$$

$$R_{\mathrm{thermal}} = \frac{\Delta T}{q \cdot A} \quad (4.4)$$

In which l, A and k_{eff} correspond to the length, the cross section and the thermal conductivity of the diodes. The temperature gradient (ΔT) corresponds to the temperature difference between T_{source} and T_{sink}, while q is the heat flux per square area in W/m^2. By combining equation 4.3 and 4.4 we obtain an expression to calculate k_{eff}.

$$k_{\mathrm{eff}} = \frac{l \cdot q}{\Delta T} \quad (4.5)$$

We then calculate the thermal conductivity values in forward and reverse direction for the discussed diode design on base of the calculated heat flux and the in the model defined parameters. Fig. 4.9 displays the k_{eff} values for the diode designs as a function of the temperature at T_{source}. Therefore, the results of the parametric sweep are used. In Fig. 4.9 (b) we can see that the thermal conductivity of the 3-PCM structure possesses three different thermal conductivity plateaus in forward direction. The thermal conductivity is low at a lower temperature, intermediately high at higher temperatures and reaches its maximum at high temperatures.

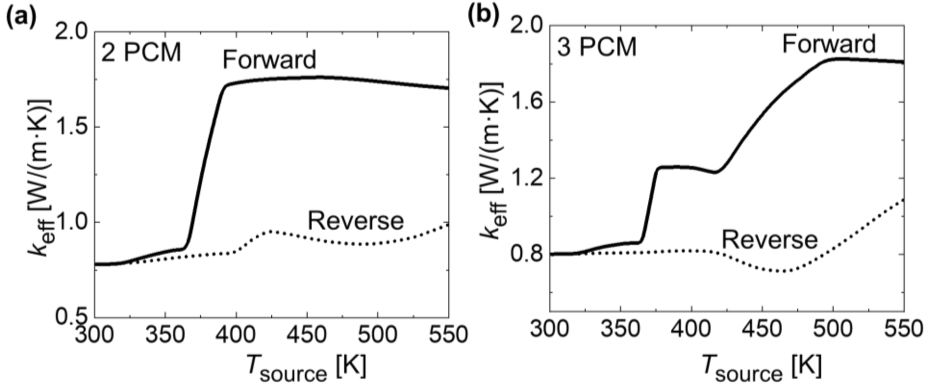

Figure 4.9 (a) Temperature profile and **(b)** Conductive heat flux, of the 3PCM structure described in Section 4.3 in forward direction for T_{source} = 500 K and T_{sink} = 300 K.

4.3.4 Validation

In order to validate our model, we compare our simulation results with the analytical study performed by Ordonez-Miranda *et al.*[33] on a similar diode structure. In their study, the thermal rectification ratio of a diode containing one PCM and one PIM layer is calculated. A maximum $RR_{calibration}$ = 19.7 % is obtained by using VO_2 as the PCM and Sapphire as the Non-PCM (PIM) layer. In this case *RR* is calculated by using equation 4.6.

$$RR_{\mathrm{calibration}} = \frac{|q_{\mathrm{fwd}}|-|q_{\mathrm{rev}}|}{|q_{\mathrm{fwd}}|} \tag{4.6}$$

Hereby q_{fwd} and q_{rev} are the heat fluxes in the forward and reverse direction, where $|q_{\mathrm{fwd}}| > |q_{\mathrm{rev}}|$. Since we use this approach as calibration for our model, we simulate (see Fig. 4.10) the thermal rectification for the exact same diode design ($L_1 = L_2$ =1 µm, T_{source} =369.5 K, T_{sink} = 300 K, R_{interf} = 0.23 (K·mm^2)/W, *k*(Sapphire) = 25 W/(m·K), and *k*(VO_2) vs T)[33]. Using equation 4.6, we obtain a $RR_{calibration}$ = 20.1 %, which matches very well with the results of the original study.[33] One difference between the two approaches is that the authors[33] include the possible impact of thermal hysteresis (relatively small in VO_2) on *RR*. We do not include thermal hysteresis in our model, because the experimental data for the materials mentioned in Table 4.1 from references[37,40,49] that we use do not display this effect. Anyhow, it is worth to

note that this might lead to potential differences of the presented *RR* with experimentally obtained values.

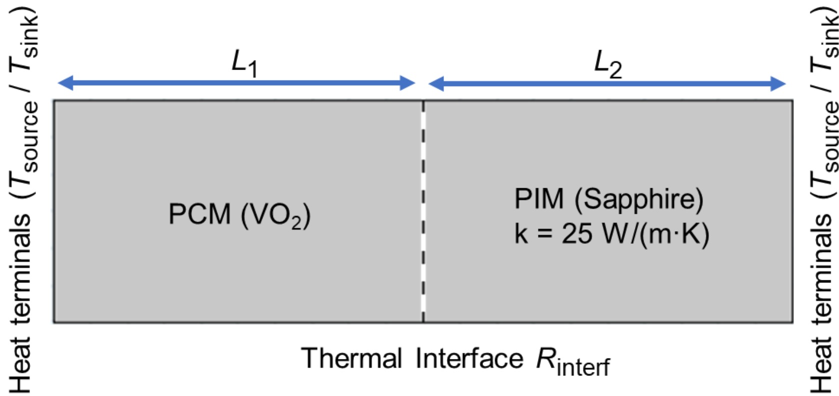

Figure 4.10 Geometry of the validation model. L_1 and L_2 correspond to the length of the studied material blocks. T_{source} and T_{sink} correspond to the temperature at the heat source and heat sink respectively. L_1, L_2, T_{source} and T_{sink} correspond to the same values presented in ref.[33]

4.3.5 Influence of geometry, interfaces and number of layers in thermal rectification of PCM/PIM diodes

The model developed in this work can also offer insights into the different design aspects of a PCM/PIM thermal diode. In this section, we discuss how the length, thermal interface and the number of layers affect the thermal rectification ratio in this type of thermal diodes (see Table 4.2). Additionally, we comment on the feasibility related with the experimental fabrication of this diode and key parameters to take into account during this process.

The signs in the cells of Table 4.2 describe how the column properties change when the model or material parameter mentioned in the rows rises. For instance, when the number of layers in the multilayer diode is increased the degree of temperature control increases as well. When the length of the system is increased the applicability for small-scale reduces. Some of the parameters have been previously investigated. As an example, we know that a thermal rectification has been found in an asymmetric shaped VO_2 beam.[20] Moreover, it has been shown that the thermal hysteresis usually leads to a decrease of the thermal rectification.[33]

As the length of the structure increases, in the presence of a fixed number of layers, the rectification ratio becomes larger because the influence of thermal

Table 4.2 Influence of different model and material parameters on key properties in PCM/PIM thermal diodes. The sign describes how the column properties change (+ increases, - decreases, 0 not affected) when the parameter in the rows is increased.

	RR	**Temperature control**	**Feasibility**	**Small-scale application**	**Reference**
Asymmetric Geometry	+	0	-	0	20
Length	+	0	+	-	
Interface Resistance	-	+/-	-	-	
Number of layers	+/-	+	0/-	0/-	
Thermal Hysteresis	-	-	-	0/-	33

interface resistance becomes smaller. If the thermal interface resistance becomes larger, the thermal rectification becomes smaller. As an example, if the thermal interface resistance is an order of magnitude higher (R_{interf} of ~10^{-7} (m^2·K)/W), the *RR* in the 3-PCM configuration is 83 % instead of 119 % when T_{source} = 500 K (see Table 4.2). The exact values of thermal interfacial resistance can be determined by applying the diffusive mismatch model.[50] However this requires precise information of the phonon dispersion relationship of the materials.[51] Nevertheless a R_{interf} of ~10^{-7} (m^2·K)/W represents the upper limit of the interfacial resistance values.[47] On the one hand, we expect that the experimental value will be within these values. On the other hand, a lower interfacial resistance R_{interf} of ~10^{-9} (m^2·K)/W would lead to a slight increase of the *RR* of the beforementioned configuration to 126 %.

When determining the *RR* of PCM/PIM multilayers, it is also important to consider the total number of PCM and PIM layers (see Table 4.2). As can be

seen from the results presented in this study, the prediction of *RR* is dependent on the choice of materials as well as the total number of PCM/PIM layers. For the same diode size, the 3-PCM/PIM multilayer structure enables a higher degree of control of the thermal conduction phases in PCMs at specific temperature ranges compared to the 2-PCM/PIM structure. Therefore, one could argue that a 4-PCM/PIM multilayer structure could allow an even higher thermal control at higher temperatures. However, it is not necessarily the case because the PCM selection is limited to their T_{trans} values. The reason is that to optimize the diode performance, the PCM transition temperatures need to match with the temperature gradient across the segments added. Since the transition temperatures of the selected materials are partly close to each other, having a combination of 4 PCMs is not bound to add many benefits compared to the 3-PCM structure under the same diode configuration. In this work, we use realistic values, reported in literature for our PCMs. However, future material engineering approaches could lead to materials with tuned T_{trans} that enable optimum PCM/PIM multilayer thermal diodes with higher *RR*.

From the point of view of fabrication and measurements of the *RR* of this thermal diode, one should account for potential sources of discrepancy with this model. For example, the impact of heat losses due to radiation and convection under different working environments could lead to differences between the *RR* results observed in the model vs those measured. However, it has been reported that the thermal radiation energy density rather decreases at lower sizes.[52] Moreover, the thermal properties at phase transition might vary depending on the quality of the PCM layers, the interface thermal resistance as well as whether the PCM blocks transition phase completely or partially under certain temperature gradients across them. Finally, the thermal properties of the individual layers are also size dependent. Size confinement effects can lead to a reduction of the thermal conductivity values and the phase transition temperature and hysteresis.[37,53]

4.4 Discussion on thermal diode applications

4.4.1 Application design

In this section, we analyze the relevance of our thermal diodes based on our optimized PCM/PIM multilayer structures for energy storage applications. Due to the desire to transition to an increasingly renewable energy infrastructure, energy storage is quickly becoming a key factor in designing and developing energy grids that are capable of withstanding the intermittent nature of most renewable energy sources. In terms of reducing carbon emissions and increasing the share of renewable energy sources on a larger scale, energy (or thermal) storage plays an important role.[54] The intermittent and constantly changing power output of e.g. solar and wind power plants, which do not match the current energy demand, require energy storage.

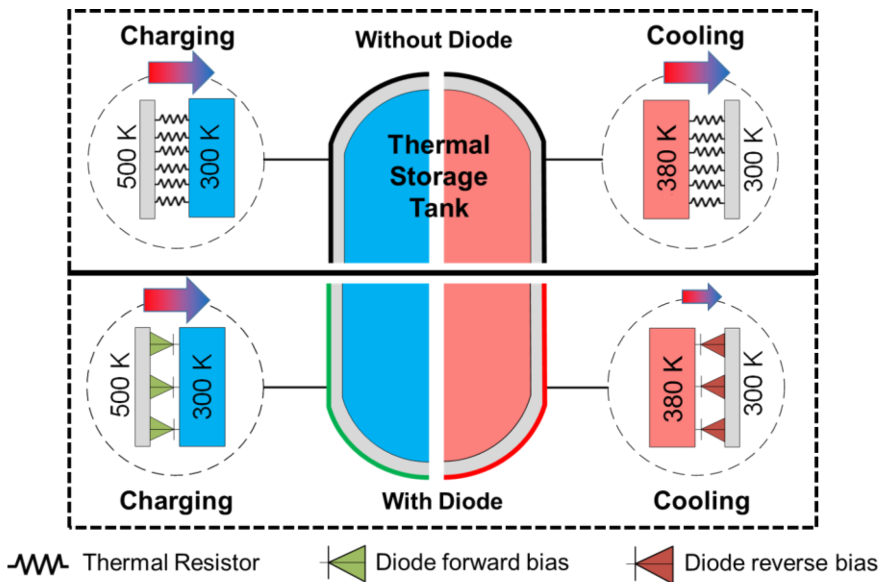

Figure 4.11 Schematic drawing of the heat fluxes from the energy storage element across the wall with and without the presence of PCM/PIM multilayer thermal diodes. The upper half represents the situation without thermal diodes, while the half below shows the situation where the thermal diodes are integrated at the surface of the storage tank. In the left area (blue area in the thermal storage tank) the heat flows in during charging. In the right area (red area in the thermal storage tank) the heat flows out during cooling. The gradient arrows represent the magnitude of heat flux in both cases.

Nowadays, this is mostly done chemically with batteries, which is expensive and cannot guarantee long-term storage. With the development of more efficient power-to-x-to power conversion, thermal storage has advantages in terms of lower cost, higher gravimetric and volumetric energy density and it is environmentally friendly.

Within this context, we analyze thermal storage elements that represent intermediate ways to store surplus heat from fluctuating energy sources (e.g., from solar heat, industrial waste heat, conversion of surplus electricity) and utilize or convert it back when required. In this scenario, we consider an external liquid heat reservoir as an energy storage element that is contained in a shell onto which a thermal diode based on a PCM/PIM multilayer structure is attached. We analyze the processes of charging and cooling across the shell of the energy storage element with and without the presence of thermal diodes at the wall surface. During charging, the diodes are considered to operate in the forward direction and have lower thermal resistance, facilitating heat to be transported towards the storage element. When the heat source is not applied, the outer wall temperature of the PCM/PIM multilayer structure cools down, reversing the temperature gradient across this element. In the later scenario, the thermal diodes begin to transition to a higher thermal resistance, which allows better retention of heat inside the storage element. Fig. 4.11 illustrates these two scenarios. The thermal diodes that are on the wall of the energy storage element correspond to the 3-PCM/PIM multilayer structure presented in Fig. 4.7 (b).

4.4.2 Analytical model

In the analytical model, we consider a number of diodes, (n_{diode}), in parallel with an area (A_{diode}), and thickness (d_{diode}), matching the dimensions of the energy storage element. The thermal conductivity of the diode in the forward and reverse directions are calculated for all temperature gradients using our COMSOL model. The temperature of the outer wall is assumed to be T_{source} = 500 K during the charging process and T_{sink} = 300 K in the cooling hours. We consider Paratherm NF as the heat storage medium with the reported mass (ρ_{liquid}) and the specific heat (c_{liquid}).[55] We separate the charging and cooling process as they are not applied simultaneously. Therefore, t_{ch} (0 to 6 hours) and t_{co} (0 to 49 hours) correspond to the time in the charging and cooling processes respectively. The total run time (t) is then expressed as the sum of t_{ch} and t_{co}. In the charging process the initial temperature of the liquid is at room temperature T_{liquid} (t_{ch} = 0) = 300 K.

In our analytical model, we assume that heat transfer occurs only between the outer wall and the heat reservoir. Hence, the heat conduction is equal to the energy difference in the heated or cooled liquid. The behavior of the charging and cooling processes can be described based on previously mentioned parameters as,

Charging: $n_{\mathrm{diode}} \cdot k_{\mathrm{fwd}} \cdot A_{\mathrm{diode}} \cdot \frac{T_{\mathrm{source}} - T_{\mathrm{liquid}}}{d_{\mathrm{diode}}} = m_{\mathrm{liquid}} \cdot c_{\mathrm{liquid}} \cdot \frac{\delta \Delta T_{\mathrm{charge}}}{\delta t_{\mathrm{ch}}}$
(4.7)

Cooling: $n_{\mathrm{diode}} \cdot k_{\mathrm{rev}} \cdot A_{\mathrm{diode}} \cdot \frac{T_{\mathrm{liquid}} - T_{\mathrm{sink}}}{d_{\mathrm{diode}}} = m_{\mathrm{liquid}} \cdot c_{\mathrm{liquid}} \cdot \frac{\delta \Delta T_{\mathrm{cooling}}}{\delta t_{\mathrm{co}}}$
(4.8)

where $\Delta T_{\mathrm{charge}}(t_{\mathrm{ch}}) = T_{\mathrm{liquid}}(t_{\mathrm{ch}}) - T_{\mathrm{liquid}}(t_{\mathrm{ch}} = 0)$ and $\Delta T_{\mathrm{cooling}}(t_{\mathrm{co}}) = \Delta T_{\mathrm{charge}}(t_1) + T_{\mathrm{liquid}}(t_{\mathrm{ch}} = 0) - T_{\mathrm{liquid}}(t_{\mathrm{co}})$.

The mass of the liquid is calculated by using,

$$m_{\mathrm{liquid}} = \rho_{\mathrm{liquid}} \cdot V_{\mathrm{liquid}} \tag{4.9}$$

In which ρ_{liquid} and V_{liquid} are the density and the volume of the liquid respectively. We choose to use the liquid Paratherm NF™[55], as it possesses a high specific heat c_{liquid}. Fig. 4.12 (b) shows the reference values ρ_{liquid} and c_{liquid} of Paratherm NF™ as a function of the temperature rise ($\Delta T_{\mathrm{liquid}}$) of the liquid from the initial temperature of 300 K.[55] The mass of the liquid remains constant, thus we calculate m_{liquid} by multiplying the density by the volume of the liquid at its initial temperature of 300 K (ρ_{liquid} = 879.2 kg/m^3; V_{liquid} = $1.02 \cdot 10^{-6}$ m^3).[55] For our analytical calculations we fit the data by means of polynomial equations.

The liquid temperature of the energy storage element is calculated with and without the presence of the diode. When no diode is present, we consider a material without rectification properties that presents the same thermal conductivity in the cooling mode as the one observed by the diode during the charging of the storage element ($k_{\mathrm{rev}} = k_{\mathrm{fwd}}$). This results in no differences in the temperature for the cases with and without diode during the charging process. After the charging, the temperature of the liquid is then at $T_{\mathrm{liquid}}(t_1)$, while heat is transported away from the liquid. In this case t_1 is the duration of the charging process.

We implement the beforementioned modifications in the initial equations 4.7 and 4.8 to derive to equation 4.10 and 4.11.

$$\frac{k_{\mathrm{fwd}} \cdot D \cdot (200 - \Delta T_{\mathrm{charge}}(t_{\mathrm{ch}}))}{\rho_{\mathrm{liquid}} \cdot c_{\mathrm{liquid}}} = \frac{\delta \Delta T_{\mathrm{charge}}}{\delta t_{\mathrm{ch}}} \tag{4.10}$$

$$\frac{k_{\mathrm{rev}} \cdot D \cdot (\Delta T_{\mathrm{charge}}(t_1) - \Delta T_{\mathrm{cooling}}(t_{\mathrm{co}}))}{\rho_{\mathrm{liquid}} \cdot c_{\mathrm{liquid}}} = \frac{\delta \Delta T_{\mathrm{cooling}}}{\delta t_{\mathrm{co}}} \tag{4.11}$$

To simplify the denotation of the time and temperature independent parameters in our calculation, we introduce the following temperature independent geometrical factor (D),

$$D = \frac{n_{\mathrm{diode}} A_{\mathrm{diode}}}{d_{\mathrm{diode}} \cdot V_{\mathrm{liquid}}} \tag{4.12}$$

First, we calculate the charging and cooling process for a situation in which the thermal storage element has thermal resistors on the shell wall (material with no thermal rectification). Second, we repeat the same process but replacing the thermal resistors with our thermal diodes. On the one hand, we calculate the temperature rise of the liquid ($\Delta T_{\mathrm{charge}}$), as a result of equation 4.10 during the charging process after t_1 (t_1 = 6 hours; $\Delta T_{\mathrm{charge}}$ (t_1) = 79.7 K). On the other hand, during the cooling process, we calculate the temperature drop of the liquid ($\Delta T_{\mathrm{cooling}}$), in the energy storage liquid by means of equation 4.11. Therefore, we analyze the cooling needed t_2 to reach the initial temperature of the liquid using the non-diode configuration ($\Delta T_{\mathrm{cooling}}(t_2) = \Delta T_{\mathrm{charge}}(t_1)$); t_2 ≈ 49 hours). Afterwards we calculate the temperature decrease for the same time span with the diode configuration.

The temperatures of the heat storage element during the charging and cooling processes are calculated for $D = 23.53\ \frac{1}{m^2}$. For the geometrical parameters we hypothesize the volume of the liquid to be V_{liquid} =1.02·10^{-6} m^3. Therefore, we assume a cubic liquid reservoir with a base length and width of 8 mm and a height of 16 mm. We choose n_{diode} = 20 that distribute over the flat surface of the tank wall, where each diode dimension is set to 1.2 µm for the width, length and thickness. The mass of the system is calculated by multiplying the volume of the liquid by the density of the liquid ($m_{\mathrm{liquid}} = \rho_{\mathrm{liquid}} \cdot V_{\mathrm{liquid}} = 0.9\ g$).[55] We calculate the thermal conductivity of the diode in forward and reverse direction as a function of $\Delta T_{\mathrm{liquid}}$, by using a parametric sweep in our COMSOL model. For the charging process, we sweep T_{sink} from 300 K to 500 K for the diode in the forward direction, while

keeping T_{source} = 500 K. For the cooling process we use the calculated values of the diode in reverse direction of Fig. 4.9 (b).

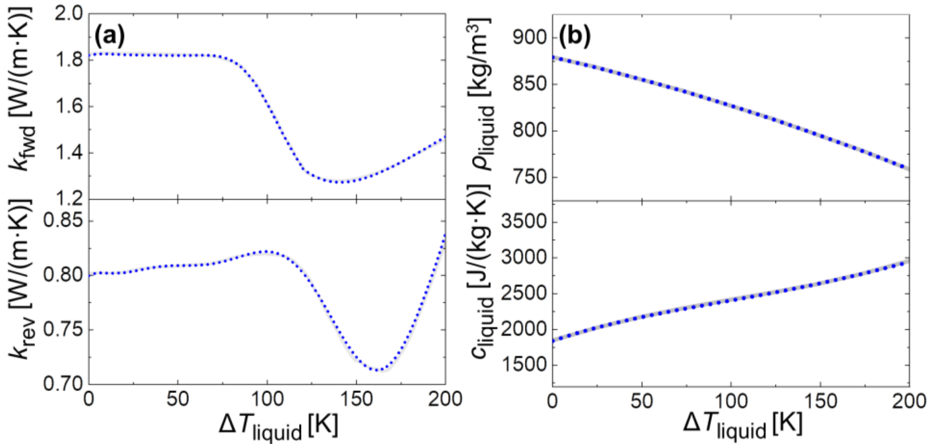

Figure 4.12 Simulated data of the diode behavior for the analytical application model as a function of the temperature change in the liquid reservoir (ΔT_{liquid}). **(a)** Thermal conductivity of the diode during the charging process (k_{fwd}) and the cooling process (k_{rev}). **(b)** Heat capacity (c_{liquid}) and density (ρ_{liquid}) of the liquid Paratherm.[55] The transparent continuous lines correspond to the reference values, the values calculated by COMSOL respectively. The blue dotted lines correspond to the fitting equations used in the analytical calculations. ΔT_{liquid} = 0 K, represents the initial temperature of the liquid T_{liquid} = 300 K. As a consequence, ΔT_{liquid} = 200 K, represents the state of the liquid at T_{liquid} = 500 K.

In Fig. 4.12 (a) we plot the calculated thermal conductivity in the charge k_{fwd} and cooling k_{rev} process as a function of ΔT_{liquid}. For the non-diode configuration, we use the same thermal conductivity values in charge and in the cooling process $k_{rev} = k_{fwd}$ (k_{fwd} in both cases). We calculate the differential equations of 4.10 and 4.11 by using the polynomial fits and a differential equation solver in Python.

Fig. 4.13 shows the calculated T_{liquid} based on the beforementioned approach and on the known material and diode properties. For the analytical model we use polynomial fits for the diode and liquid properties. In the non-diode configuration, we reach the original storage liquid temperature of ~300 K

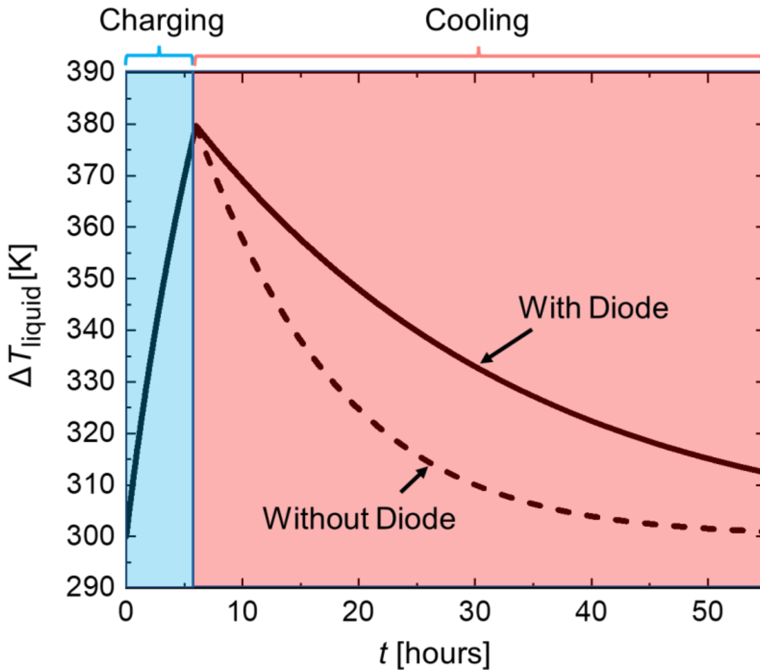

Figure 4.13 Temperature of the heat storage element (T_{liquid}), as a function of time (t), during charging and cooling processes with (solid line) and without (dashed line) thermal diodes.

after approximately 55 hours. For the same time span the liquid temperature remains at ~312.5 K for the diode configuration.

4.4.3 Calculation heat losses

For the characterization of the heat losses, we use the specific enthalpy values (h) reported in literature.[56]. Table 4.3 shows the specific enthalpy values of Paratherm.

Table 4.3 Specific enthalpy (h) of Paratherm for the relevant temperatures.

Temperature T [K]	**Specific enthalpy h [J/kg]**
300	65298
312.5	88891
379.7	230291

We calculate the magnitude of the total heat losses (ΔQ) during the cooling process with and without the diode. In the non-diode configuration, the heat liquid element heats up to 379.7 K. In the cooling process the stored energy

is transferred to the surroundings and the liquid cools down to its initial temperature of 300 K. The heat loss is calculated as the difference in the specific enthalpy states h_1 at 300 K and h_2 at 379.7 K (Δh) of the liquid, which we retrieve from literature (see Table 4.3).[56]. Thus, we can calculate the heat loss by using,

$$\Delta Q = \Delta h \cdot m_{\mathrm{liquid}} \tag{4.13}$$

The charging process in the diode configuration is equal to the charging process in the non-diode configuration. In the cooling process the liquid cools from 379.7 K to 312.5 K. Similar to the approach in the non-diode configuration we determine the heat losses by calculating the differences in the enthalpy states h_3 at 312.5 K and h_2 at 379.7 K.[56] By using equation 4.13 we obtain a heat loss of $\Delta Q_{\mathrm{no\ diode}}$ = 148.5 J for the configuration without diode and $\Delta Q_{\mathrm{diode}}$ = 127.3 J with diode. When we compare these results, we observe that the diode configuration is capable to retain 17 % more heat than in the case without diode.

4.4.4 Cycling of thermal storage system

Apart from the benefits of a single cycle, we observe that the diode configuration enables an even better heat retention when its operation is considered for multiple day cycles. With the intention of evaluating the long term performance of the thermal storage element we investigate the charging and cooling process for several cycles. Therefore, one cycle includes the charging and cooling process which cover one single day (t_{ch} = 6 hours and t_{co} = 18 hours). The cycle is repeated 7 times, in which every cycle starts after the end of the previous one. After one week both cycling processes (with and without diode) reach an equilibrium state. After cooling the temperature stabilizes at a temperature of T_{diode} = 357 K and $T_{\mathrm{no\ diode}}$ = 320 K for the configuration with and without diode respectively as can be seen in Fig. 4.14. As a result of that we are able to store more energy in the heat storage element, using the diode configuration when the steady state is reached.

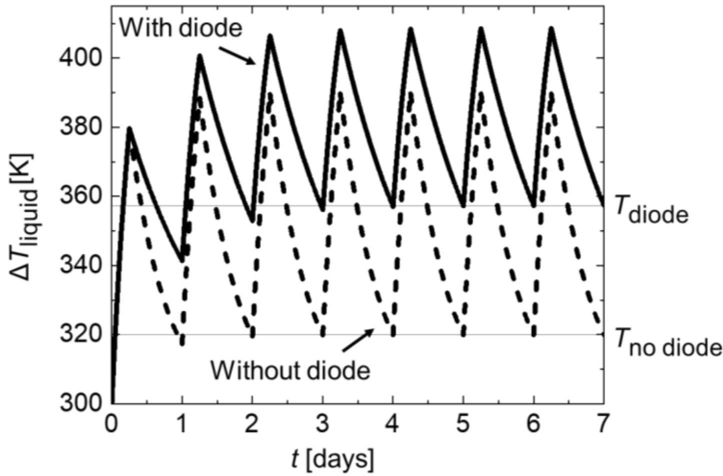

Figure 4.14 Temperature of the liquid heat reservoir of the energy storage element during charging and cooling (ΔT_{liquid}) as a function of the cycling time (t). After a few days the charging and cooling process reach an equilibrium state. In the equilibrium state the temperature after cooling is $T_{no\ diode} \approx 320$ K and $T_{diode} \approx 357$ K without and with diode respectively.

4.4.5 Integration of thermal contacts

It is also important to mention that the experimental heat retention performance is further depending on the thermal contact between the hot/cold reservoirs and the diode. In the original model we assume a constant temperature at the edges of the diode. However, when implementing the diode in between a heat source and heat sink of a certain material the rectification performance would be affected due to the existence of thermal contact resistances between the thermal diode and the heat terminals as illustrated in Fig. 4.15. In order to evaluate the impact of the thermal contact resistance on the diode performance we recalculate the thermal properties of the 3 PCM diode presented in section 4.3. The thermal contact resistance usually varies from 10^{-7} K·m²/W to 10^{-5} K·m²/W.[57] We reevaluate the thermal rectification for two cases in which the thermal contact resistance is equal to 10^{-7} K·m²/W and 10^{-6} K·m²/W respectively. We adjust T_{source} and T_{sink}, so that the temperature gradient in thermal diode itself is as close as possible to the values stated in section 4.3. For a thermal contact resistance of 10^{-7} K·m²/W we observe a slight shift in the rectification ratio and temperature gradient to RR = 101 % at T_{source} = 490 K and T_{sink} = 290 K. However, the thermal rectification and temperature gradient shift strongly for a thermal contact

resistance of 10^{-6} K·m^2/W that leads to *RR* = 32 % between T_{source} = 570 K and T_{sink} = 200 K. We can conclude that an additional increase of the thermal contact resistance would lead to an even bigger shift of the thermal rectification properties. As a result, we conclude that a high thermal contact resistance will result in a significant change of the thermal rectification properties.

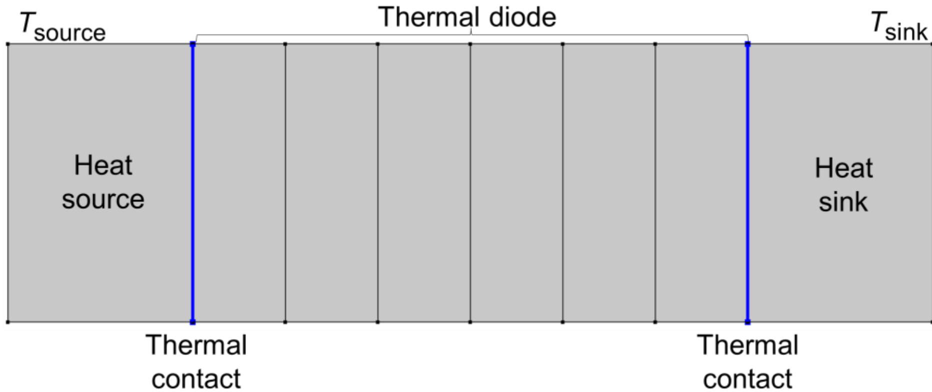

Figure 4.15 Thermal diode configuration with integrated thermal contact between the heat source and heat sink and the thermal diode. In this case the temperature gradient between the source T_{source} and T_{sink} is applied between the outer edges of the structure.

4.5 Conclusion and prospects

In summary, we present the thermal rectification properties of a thermal diode design based on a multilayer structure made of PCMs and PIMs, by means of FEM simulations. The highest rectification ratios are found to be 96 % and 119 % for the 2-PCM/PIM and 3-PCM/PIM diodes, respectively, when T_{source} = 500 K and T_{sink} = 300 K. The temperature dependency of the rectification ratios is also determined, obtaining a maximum value of 106 % and 133 % for 2-PCM/PIM and 3-PCM/PIM when T_{source} = 395 K and T_{source} = 470 K, respectively (T_{sink} = 300 K). These thermal rectification ratios are ~50-80% larger than in simple PCM/PIM junctions, like in a Nitinol (PCM) and Graphite thermal diode (PIM)[38]. Moreover, the existence of multiple layers of PCMs and PIMs allows better control of the temperature gradients across materials, which facilitates the transition between high and low thermally conductive PCM phases at certain range of temperatures. As a result, the thermal conductivity of the 3 PCM thermal diode in forward direction holds

two plateau values at different temperatures which qualifies this device as a multistate thermal regulator. Beyond their exceptional thermal rectification performance, the realistic material sizes and properties considered in this model make the fabrication of the thermal diode feasible. However, experimental investigation of these devices is required to validate the models developed. Finally, these thermal diodes are key enablers of new technology advances related with energy management and storage. We analyze their potential use for the storage of waste or renewable heat. The implementation of these devices allows to retain considerably more heat during the cooling process of the energy storage element than if they were not present. They could be used to develop more compact thermal storage systems as well as for management of heat fluxes from renewable and waste heat sources, or even in processes related to the coupling of sectors (power-to-x). Overall, these thermal diodes represent new opportunities for more efficient energy processes, which are essential for our sustainable future.

4.6 References

1 T. Swoboda, K. Klinar, M. Muñoz Rojo and A. Kitanovski, *Adv. Electron. Mater.*, 2020, **7**, 2000625.

2 H. Liu, H. Wang and X. Zhang, *Appl. Sci.*, 2019, **9**, 344.

3 K. Klinar, T. Swoboda, M. Muñoz Rojo and A. Kitanovski, *Adv. Electron. Mater.*, 2020, **7**, 2000623.

4 M. Y. Wong, C. Y. Tso, T. C. Ho and H. H. Lee, *Int. J. Heat Mass Transf.*, 2021, **164**, 120607.

5 G. Wehmeyer, T. Yabuki, C. Monachon, J. Wu and C. Dames, *Appl. Phys. Rev.*, 2017, **4**, 041304.

6 K. Klinar, M. Muñoz Rojo, Z. Kutnjak and A. Kitanovski, *J. Appl. Phys.*, 2020, **127**, 234101.

7 U. Ghoshal and A. Guha, *J. Electron. Mater.*, 2009, **38**, 1148–1153.

8 C. Starr, *J. Appl. Phys.*, 1936, **7**, 15–19.

9 B. Li, L. Wang and G. Casati, *Phys. Rev. Lett.*, 2004, **93**, 1–4.

10 M. Peyrard, *Europhys. Lett.*, 2006, **76**, 49–55.

11 N. Li, J. Ren, L. Wang, G. Zhang, P. Hänggi and B. Li, *Rev. Mod. Phys.*, 2012, **84**, 1046–1065.

12 G. Wu and B. Li, *Phys. Rev. B - Condens. Matter Mater. Phys.*, 2007, **76**, 1–8.

13 M. Muñoz Rojo, Z. Li, C. Sievers, A. C. Bornstein, E. Yalon, S. Deshmukh, S. Vaziri, M. H. Bae, F. Xiong, D. Donadio and E. Pop, *2D Mater.*, 2019, **6**, 011005.

14 M. Schmotz, J. Maier, E. Scheer and P. Leiderer, *New J. Phys.*, 2011, **13**, 113027.

15 N. Yang, G. Zhang and B. Li, *Appl. Phys. Lett.*, 2008, **93**, 243111.

16 N. Yang, G. Zhang and B. Li, *Appl. Phys. Lett.*, 2009, **95**, 033107.

17 J. W. Jiang, J. S. Wang and B. Li, *Epl*, 2010, **89**, 46005.

18 H. Wang, S. Hu, K. Takahashi, X. Zhang, H. Takamatsu and J. Chen, *Nat. Commun.*, 2017, **8**, 15843.

19 C. W. Chang, D. Okawa, A. Majumdar and A. Zettl, *Science.*, 2006, **314**, 1121–1124.

20 J. Zhu, Y. Abate, X. Yin, K. Wang, K. Hippalgaonkar, J. Wu, X. Zhang, A. Majumdar, S. Lee and S. Shen, *Nano Lett.*, 2014, **14**, 4867–4872.

21 H. Tian, D. Xie, Y. Yang, T. L. Ren, G. Zhang, Y. F. Wang, C. J. Zhou, P. G. Peng, L. G. Wang and L. T. Liu, *Sci. Rep.*, 2012, **2**, 1–7.

22 D. Sawaki, W. Kobayashi, Y. Moritomo and I. Terasaki, *Appl. Phys. Lett.*, 2011, **98**, 2009–2012.
23 K. Ito, K. Nishikawa, H. Iizuka and H. Toshiyoshi, *Appl. Phys. Lett.*, 2014, **105**, 253503.
24 A. Fiorino, L. Zhu, P. Ben-Abdallah, D. Thompson, N. El-Bondry, S. Bansropun, O. Bezencenet, R. Mittapally, S.-A. Biehs, E. Meyhofer and P. Reddy, *ACS Nano*, 2018, **12**, 5774–5779.
25 W. Kobayashi, D. Sawaki, T. Omura, T. Katsufuji, Y. Moritomo and I. Terasaki, *Appl. Phys. Express*, 2012, **5**, 027302.
26 G. Hamaoui, N. Horny, C. L. Gomez-heredia, J. A. Ramirez-rincon, J. Ordonez-miranda, C. Champeaux, F. Dumas-bouchiat, J. J. Alvarado-gil, Y. Ezzahri and K. Joulain, *Sci. Rep.*, 2019, **9**, 1–10.
27 S. M. Bohaichuk, S. Kumar, G. Pitner, C. J. McClellan, J. Jeong, M. G. Samant, H. S. P. Wong, S. S. P. Parkin, R. S. Williams and E. Pop, *Nano Lett.*, 2019, **19**, 6751–6755.
28 S. M. Bohaichuk, M. Muñoz Rojo, G. Pitner, C. J. McClellan, F. Lian, J. Li, J. Jeong, M. G. Samant, S. S. P. Parkin, H. S. P. Wong and E. Pop, *ACS Nano*, 2019, **13**, 11070–11077.
29 T. D. Manning, I. P. Parkin, R. J. H. Clark, D. Sheel, M. E. Pemble and D. Vernadou, *J. Mater. Chem.*, 2002, **12**, 2936–2939.
30 Y. Gao, H. Luo, Z. Zhang, L. Kang, Z. Chen, J. Du, M. Kanehira and C. Cao, *Nano Energy*, 2012, **1**, 221–246.
31 S. M. Bohaichuk, M. M. Pelella, Y. Sun, Z. Zhang, S. Ramanathan and E. Pop, *IEEE Electron Device Lett.*, 2020, **41**, 292–295.
32 Y. Zhou and S. Ramanathan, *Proc. IEEE*, 2015, **103**, 1289–1310.
33 J. Ordonez-Miranda, J. M. Hill, K. Joulain, Y. Ezzahri and J. Drevillon, *J. Appl. Phys.*, 2018, **123**, 085102.
34 G. Stefanovich, A. Pergament and D. Stefanovich, *J. Phys. Condens. Matter*, 2000, **12**, 8837–8845.
35 R. Zhang, Q. S. Fu, C. Y. Yin, C. L. Li, X. H. Chen, G. Y. Qian, C. L. Lu, S. L. Yuan, X. J. Zhao and H. Z. Tao, *Sci. Rep.*, 2018, **8**, 1–7.
36 V. Eyert, *Ann. der Phys.*, 2002, **11**, 650–704.
37 D. W. Oh, C. Ko, S. Ramanathan and D. G. Cahill, *Appl. Phys. Lett.*, 2010, **96**, 151906.
38 K. I. Garcia-Garcia and J. Alvarez-Quintana, *Int. J. Therm. Sci.*, 2014, **81**, 76–83.
39 H. Kang and F. Yang, *Phys. Rev. Appl.*, 2018, **10**, 024034.
40 K. Hirata, T. Matsunaga, S. Singh, M. Matsunami and T. Takeuchi, *J. Electron. Mater.*, 2020, **2019**, 1–7.
41 J. A. Leon-Gil, J. J. Martinez-Flores and J. Alvarez-Quintana, *J. Mater. Sci.*, 2019, **54**, 3211–3221.
42 N. A. Roberts and D. G. Walker, *Int. J. Therm. Sci.*, 2011, **50**, 648–662.
43 Alto University, Heat flow control for future nanoelectronics, https://phys.org/news/2012-08-future-nanoelectronics.html.
44 G. Zhang and H. Zhang, *Nanoscale*, 2011, **3**, 4604–4607.
45 J. Cheh and H. Zhao, *J. Stat. Mech. Theory Exp.*, 2012, **2012**, P06011.
46 S. R. Sklan, *AIP Adv.*, 2015, **5**, 053302.
47 H. K. Lyeo and D. G. Cahill, *Phys. Rev. B - Condens. Matter Mater. Phys.*, 2006, **73**, 144301.
48 J. J. Martinez-Flores, D. Varshney and J. Alvarez-Quintana, *Appl. Phys. Lett.*, 2018, **113**, 264102.
49 H. Chen, Z. Yue, D. Ren, H. Zeng, T. Wei, K. Zhao, R. Yang, P. Qiu, L. Chen and X. Shi, *Adv. Mater.*, 2018, **1806518**, 1–7.
50 E. T. Swartz and R. O. Pohl, *Rev. Mod. Phys.*, 1989, **61**, 605–668.
51 P. Reddy, K. Castelino and A. Majumdar, *Appl. Phys. Lett.*, 2005, **87**, 1–3.
52 S. Yu, S. Joo and H. Kim, *Phys. B Phys. Condens. Matter*, 2010, **405**, 638–641.
53 D. Li, Y. Wu, R. Fan, P. Yang and A. Majumdar, *Appl. Phys. Lett.*, 2003, **83**, 3186–3188.
54 A. Henry, R. Prasher and A. Majumdar, *Nat. Energy*, 2020, **5**, 635–637.
55 Paratherm, Paratherm NF, https://thermalprops.paratherm.com/NFCrange.asp.
56 Estimating Database – EES Data, https://ees-data.co.uk/database, (accessed 24 April 2021).
57 H. Fenech and W. M. Rohsenow, *J. Heat Transfer*, 1963, **85**, 15–24.

4.7 Appendix

4.7.1 Verification heat losses

In order to verify the calculated heat losses of chapter 4.4.3, we solve the integral of $\int_0^{175000} \Delta T_{\text{cooling}}(t_{\text{co}}))\delta t_{\text{co}}$ numerically, on base of the prior obtained results of $\Delta T_{\text{cooling}}$ (175000 s ≈ 49 hours). We calculate the total heat losses ΔQ of the cooling process by means of the conduction between storage tank and wall in both cases with and without the diode, as follows,

$$\Delta Q = \int_0^{175000} (n_{\text{diode}} \cdot k_{\text{rev}} \cdot A_{\text{diode}} \cdot \frac{T_{\text{liquid}} - T_{\text{sink}}}{d_{\text{diode}}})\delta t_{\text{co}} \tag{4.14}$$

We assume the thermal conductivity to be constant in this temperature span (ΔT_{liquid} < 79.7 K). From Fig. 4.12 we evaluate the thermal conductivity of the diode configuration as $k_{\text{rev,diode}}$ = 0.81 W/(m·K), and $k_{\text{rev,no diode}}$ = 1.82 W/(m·K) for the non-diode configuration. We then calculate the heat losses as follows:

$$\Delta Q = \frac{n_{\text{diode}} \cdot k_{\text{rev}} \cdot A_{\text{diode}}}{d_{\text{diode}}} \cdot \int_0^{175000} (\Delta T_{\text{charge}}(t_1) - \Delta T_{\text{cooling}}(t_{\text{co}}))\delta t_{\text{co}} \tag{4.15}$$

$$\Delta Q_{\text{diode}} = \frac{n_{\text{diode}} \cdot k_{\text{rev,diode}} \cdot A_{\text{diode}}}{d_{\text{diode}}} \cdot \Big([\Delta T_{\text{charge}}(t_1) \cdot t_{\text{co}}]_0^{175000} - \int_0^{175000} \Delta T_{\text{cooling,diode}}(t))\delta t_{\text{co}}\Big) = 127.5 J \tag{4.16}$$

$$\Delta Q_{\text{no diode}} = \frac{n_{\text{diode}} \cdot k_{\text{rev,no diode}} \cdot A_{\text{diode}}}{d_{\text{diode}}} \cdot ([\Delta T_{\text{charge}}(t_1) \cdot t_{\text{co}}]_0^{175000} - \int_0^{175000} \Delta T_{\text{cooling,no diode}}(t))\delta t_{\text{co}}) = 145.2 J \tag{4.17}$$

Additionally, we calculate the energy difference in the liquid ΔQ using,

$$\Delta Q(\Delta T_{\text{charge}}) = m_{\text{liquid}} \cdot c_{\text{liquid}} \cdot \Delta T_{\text{charge}} \tag{4.18}$$

while we average the values of the heat capacity of the liquid in the considered temperature span. After the charging process the liquid heats to 379.7 K. By using equation 4.18 the energy difference in the liquid is 148.9 J due to the rise in temperature (ΔT_{charge} = 79.67 K; c_{liquid} = 2076 J/(kg·K); m_{liquid} = 0.9 g). As mentioned before, the storage is cooled to its initial temperature after the cooling process in the non-diode configuration. Hence, the initial energy difference is equal to the heat losses in the cooling process $\Delta Q_{\text{no diode}}$ = 148.9 J. In the diode configuration the temperature in the liquid remains at 312.5 K after the cooling process. In that consequence the energy difference in regard to the initial state is 21.4 J (ΔT_{charge} = 12.5 K; c_{liquid} = 1890 J/(kg·K); m_{liquid} = 0.9 g). By subtracting the remaining energy difference from the energy difference after charging we determine the heat losses of the liquid in the cooling process for the diode configuration ΔQ_{diode} = 127.5 J.

Chapter 5 Conclusion and future perspectives

During the course of this PhD thesis, I have performed theoretical and experimental thermal analysis of nano- and micro-structures. On the one hand, my first aim was the characterization of heating in electronics. By means of a SThM calibration method I showed that the calibration in SThM correlates with the probe power and the size of the heating surface feature. By that means, future studies can adapt the SThM operation parameters to convert accurately the electrical response of thermo-resistive probes into temperature considering variable probe-sample thermal exchange processes. Further the calibrated SThM showed to be a powerful tool for the investigation of the heating of filamentary based RRAM devices during in operando conditions. The thermal analysis of these devices together with their electrical analysis provided a correlation between the hot spot position and the electrical *I-V* variability. On the other hand, my second aim was to also study new routes to expand our thermal management capabilities. In this context, I designed a thermal diode based on multiple PCM/PIM layers with state-of-the-art and variable rectification ratios reaching values in the range of 96-133 % depending on the temperature gradient. This thermal diode showed potential to be integrated in thermal storage tanks to enhance their heat retention by 17 %. Next, I will present my detailed conclusions together with an outlook about prospects and my suggestions for future studies in this field.

5.1 Characterization of electro-thermal switching in metal-oxide RRAMs with SThM

An important part of this thesis was the utilization and extension of previous calibration methods for the quantification of SThM measurements. For that purpose, I employed a calibration approach based on the characterization of metal lines with varying width by a SThM thermo-resistive probe under varying applied power. The results showed that both the line width as also the probe power affect the calibration factor (*CaF*) that one must use to convert the electrical signal of the probe into temperature. In the range of bridge voltages at which the SThM is typically working for temperature sensing (0.1-0.7 V), I observed a span of > 10 in the saturation of the *CaF* (mV/K). **As a consequence, the temperature sensitivity of the SThM can be tailored largely by adjusting the power applied to the probe during scans.**

Therefore, this calibration approach enables adjustable measurements with the SThM depending on the probe power. For example, one could prefer to run the SThM at lower self-heating power in order to protect temperature sensitive samples. On the other hand, a higher probe power allows a better temperature sensitivity which is crucial for the characterization of small heating features. Moreover, the null-point was shown to be valuable method to accurately estimate the temperature of the probe. Based on this, I demonstrated how to estimate the thermal contact resistance between the probe and the sample which was in the range of $4{\cdot}10^6$ and $4{\cdot}10^7$ K/W. This is especially interesting for theoretical studies in which the contact resistance must be estimated.

The results of the calibration were verified by means of the characterization of a PCM sample with the same kind of capping layer. Therefore, **we developed a robust calibrated SThM method that can be applied for quantitative nanoscale temperature measurements of multiple kind of electronic devices with similar surface characteristics**.

In the second part of this work, the calibrated SThM probes were successfully employed to obtain quantified temperature maps in filamentary based metal oxide RRAM devices. The spatially confined nature of the hot spot generated (< 750 nm) by filaments made these RRAMs very challenging to thermally characterize. Based on my calibration, I decided to operate the SThM at a bridge voltage of 0.5 V because this configuration provides a high temperature sensitivity while the thermal exchange area of the probe is in the range of the targeted heating feature size.

By means of the SThM measurements of in-operando RRAM devices, I showed the correlation of the devices´ temperature evolution with their *I-V* cycling behavior. With the combination of theoretical and experimental analysis I estimated the temperature features of the filament and the heat spreading towards the surface in these devices. Moreover, the heating variability directly correlated with the electrical *I-V* characteristics in RRAM devices, giving insights of the fundamental processes of RRAM cycling. By combining the experimentally achieved characteristics of the hot spot with an electrothermal model we were able to estimate the temperature and geometrical characteristics of the buried filament which differ by a factor of 10 and higher from the surface characteristics.

From a device standpoint I observed different correlations between the electrical and thermal characteristics. On the one hand, I observed that the

temperature of the hot spots scaled with the power applied to the device. On the other hand, I observed that the position of the hot spot could change as a consequence of the cycling and the device design. **These results are indicative for the existence of multiple possible filament positions in specific designs of RRAM devices and demonstrated that heat dissipation can vary locally as a function of cycling**.

In general, the SThM was proved to be a valuable and versatile tool for the characterization of RRAM devices. The in this thesis elaborated methods can be and have been transferred for the characterization in other electronics as for example in phase change memories.

5.2 Development of a novel solid-state thermal diode and evaluation of its potential for advanced heat control

In the second part of this thesis, I designed a COMSOL finite element method simulation for the characterization of a new thermal diode design based on a Multilayer PCM/PIM structure. In that context both 2 PCM (up to 106 %) or 3 PCM (up to 133 %) layers showed 50-80 % larger rectification ratios than in simple PCM/PIM structures in a similar temperature range. Amongst the investigated PCMs, silver selenide materials showed the most promising characteristics to be applied in the PCM thermal diode design as they provide sharp and steady thermal conductivity changes close to room temperature. The suggested realistic materials of the design make the fabrication of the thermal diode feasible.

The existence of multiple layers of PCMs and PIMs allows better control of the temperature gradients across materials which facilitates the transition between high and low thermal conductivity PCM phases at certain range of temperature. Apart from the application as a thermal diode, these structures showed a stepwise increase in their thermal conductivity from $k_{low} \approx 0.8$ W/(m·K) to k_{high} 1.8 W/(m·K) making this structure also interesting for the application as a multilevel thermal regulator.

One crucial aspect in the performance of the thermal diodes is the thermal contact resistance in between layers. The results demonstrated that a high contact resistance can lead to a significant reduction of the rectification characteristics. This aspect becomes especially relevant when decreasing the scale of the design.

By means of an analytical model I showed that an improved heat retention of 17 % can be achieved by implementing the thermal diode to the walls of a thermal heat storage element. **In conclusion, more compact thermal storage systems can be built in the future. The results represent new opportunities for the realization of the thermal diode structure as also for thermal management systems**.

5.3 Recommendations & outlook

As a result of the outcome of this thesis new insights and questions arose in the field of this study. Next, I will suggest potential future research lines related with SThM thermal characterization and advanced heat control:

- I observed that the calibration properties of different SThM tips may vary from each other, especially if they come from different batches. Therefore, I suggest repeating the calibration for each probe at least for few lines sizes to secure the accuracy of this calibration approach.
- I observed that heating beyond the edges of the RRAM device structure can be detected with SThM. Consequently, SThM can be a powerful tool to be applied in the characterization of thermal crosstalk in densely packed RRAM crossbar structure experimentally.
- The in-operando SThM temperature measurements of the hot spot generated by the filament showed a valuable connection with the electrical characteristics. This connection offers the possibility to develop electro-thermal models of filaments that do not only rely only on electrical data but also in thermal data. This will advance our fundamental knowledge of RRAMs and it could favor the design of more reliable devices.
- Past studies of RRAM devices have shown that the contact resistance, both electrical and thermal, plays a crucial role in the characteristics of RRAM cycling. I observed a partial delamination of the RRAM oxide layer from the electrodes as a consequence of the filament forming. Therefore, I recommend studying the impact of this delamination on the device performance.
- The thermal diode structure presented in this thesis represents a symmetric rectangular structure. Future studies could consider asymmetrical shapes to enhance the thermal rectification effect.

- The diode structure presented in this thesis could be developed experimentally to evaluate its performance potential and explore its integration in energy storage tanks.

List of publications

The chapter of this thesis are derived from the first author publication prepared over the course of this project. All of the publications and conference contributions are listed below.

First author publications

1) T. Swoboda, K. Klinar, A. S. Yalamarthy, A. Kitanovski and M. Muñoz Rojo "Solid-State Thermal Control Devices", published in Advanced electronic materials in 2021. **(Chapter 1.3)**

   T. Swoboda, K. Klinar, A. S. Yalamarthy, A. Kitanovski and M. Muñoz Rojo, Adv. Electron. Mater., 2020, 7, 2000625.

2) T. Swoboda, N. Wainstein, S. Deshmukh, Ç. Köroğlu, X. Gao, M. Lanza, H. Hilgenkamp, E. Pop, E. Yalon and M. Muñoz Rojo "Nanoscale temperature sensing of electronic devices with calibrated scanning thermal microscopy", published in Nanoscale in 2023 **(Chapter 2)**

   T. Swoboda, N. Wainstein, S. Deshmukh, Ç. Köroğlu, X. Gao, M. Lanza, H. Hilgenkamp, E. Pop, E. Yalon and M. Muñoz Rojo Nanoscale, 2023, 15, 7139–7146.

3) T. Swoboda, X. Gao, C. M. M. Rosário, F. Hui, K. Zhu, Y. Yuan, S. Deshmukh, Ç. Köroğlu, E. Pop, M. Lanza, H. Hilgenkamp and M. Muñoz Rojo "Spatially resolved thermometry of filamentary nanoscale hot spots in TiO_2 resistive random access memory devices", accepted for publication in ACS Applied Electronic Materials. DOI: https://doi.org/10.1021/acsaelm.3c00782 **(Chapter 3)**

4) T. Swoboda, K. Klinar, S. Abbasi, G. Brem, A. Kitanovski and M. Muñoz Rojo "Thermal rectification in multilayer phase change material structures for energy storage applications", published in iScience 2021 **(Chapter 4)**

T. Swoboda, K. Klinar, S. Abbasi, G. Brem, A. Kitanovski and M. Muñoz Rojo, iScience, 2021, 24, 102843.

Co-author publications

1) K. Klinar, T. Swoboda, M. Muñoz Rojo and A. Kitanovski, Adv. Electron. Mater., 2020, 7, 2000623.
2) N. Wainstein, G. Ankonina, T. Swoboda, M. Muñoz Rojo, S. Kvatinsky and E. Yalon, IEEE Trans. Electron Devices, 2021, 1–6.
3) K. Klinar, K. Vozel, T. Swoboda, T. Sojer, M. Muñoz Rojo and A. Kitanovski, iScience, 2022, 25, 103779.
4) X. Gao, T. J. Roskamp, T. Swoboda, C. M. M. Rosário, S. Smink, M. Muñoz Rojo, H. Hilgenkamp, Adv. Electron. Mater. 2023, accepted for publication (arXiv:2305.05259).

.**Conference contributions**

1) T. Swoboda, K. Klinar, A. Kitanovski and M. Muñoz Rojo, MRS Virtual Conference 2021 “High asymmetric heat transport in multilayer phase change materials” (oral talk)
2) T. Swoboda, K. Klinar, A. Kitanovski and M. Muñoz Rojo, Eurotherm Virtual Conference 2021 “Thermal diode based on a multilayer structure of phase change materials” (oral talk and conference proceeding)

   T. Swoboda, K. Klinar, A. Kitanovski and M. Muñoz Rojo, J. Phys. Conf. Ser., 2021, 2116, 012115.

3) T. Swoboda, X. Gao, S. Deshmukh, Ç. Köroğlu, K. Zhu, F. Hui, N. Wainstein, C. M. M. Rosário, E. Yalon, M. Lanza, E. Pop, H. Hilgenkamp and M. Muñoz Rojo, Nano2022 16th International Conference on Nanostructured Materials in Sevilla, Spain “Spatially resolved thermometry of micro- and nano- devices using SThM” (oral talk)
4) T. Swoboda, X. Gao, C. M. M. Rosário, K. Zhu, F. Hui, S. Deshmukh, Ç. Köroğlu, N. Wainstein, E. Yalon, E. Pop, M. Lanza, H. Hilgenkamp, M. Muñoz Rojo, 745th Heraeus Seminar on Photon, Phonon and Electron in Coupled Nanoscale systems in Bad Honnef, Germany “Spatially resolved thermometry on metal oxide RRAM devices by SThM” (poster)

5) X. Gao, T. Swoboda, C. M. M. Rosário, M. Muñoz Rojo and H. Hilgenkamp, Nano2022 16th International Conference on Nanostructured Materials in Sevilla, Spain “Multi-level operation in vanadium dioxide – based resistive switching devices” (oral talk presented by the first author X. Gao)
6) X. Gao, T. Roskamp, T. Swoboda, C. M. M. Rosário, M. Muñoz Rojo and H. Hilgenkamp, Brainspiration in Enschede, The Netherlands “Multi-level operation in VO_2-based resistive switching devices” (poster presented by the first author X. Gao)

Acknowledgments

Over the course of my PhD journey, I have been blessed to work and spend time with a variety of great researchers and people. I sincerely want to show my appreciation to them as they have been a significant part of this journey, inspiring and supporting me, as well as sharing great and memorable times.

First of all, I would like to thank my thesis promoter **Prof. Gerrit Brem** and **Prof. Miguel Muñoz Rojo** for giving me the opportunity to work on this project and for their friendly and valuable support throughout. Miguel, I am deeply grateful to you for believing in me and always having my back throughout this entire journey. Your feedback, reliable and positive communication, and dedication have been both a great support and a source of motivation for me. In our many Friday meetings, you helped me put things in the right context while discussing experiments, papers, and sometimes even more important things like football. Thanks to that, I could always go into the weekend feeling motivated and encouraged. You consistently pushed me to go one step further, whether it was working on a proposal or developing new research output. I am extremely grateful for the friendly exchange we had during this process, and I appreciate your willingness to discuss things whenever I encountered a problem on this path. Being your first PhD student, I can only recommend you for the ones to come. Gerrit, I want to thank you for ensuring that I had all the scientific equipment and experiments I required during my PhD project. During our update meetings, you always asked intriguing questions and made valuable suggestions. I am grateful to have learned from your experiences, skills, and advice.

I would like to express my gratitude to **Xing**, **Carlos**, **Frank** and **Prof. Hans Hilgenkamp** from the ICE group at Utwente. I always enjoyed the sharp, dedicated, and friendly character of our update meetings. I thoroughly enjoyed the time we shared in Sevilla during the Nano conference. A special thank-you goes to Xing for enduring and sharing the sometimes long lab experiences and to Carlos for his constant and knowledgeable support, which often helped me gain a different perspective.

Many thanks go to **Prof. Andrej Kitanovski** and **Katja** from the Ljubljana University, with whom I had the pleasure of writing a review and working on

other projects related with thermal diodes. I embraced your dedication, friendliness, and creative thinking throughout our various meetings.

I want to thank **Prof. Mario Lanza** from KAUST and his group for their massive support with the device fabrication. I always enjoyed the fruitful meetings over the course of the memory project. In that context, I want to thank **Fei**, **Yue**, and **Kaichen** for the scientific exchange.

Further I would like to thank **Prof. Eric Pop**, **Sanchit** and **Chuck** from Stanford University for their valuable input and the many helpful suggestions related to the calibration and modeling methods.

Many thanks to **Prof. Eilam Yalon** and **Nico** from the Technion Institute for the exciting scientific exchange and helpful feedback related to the calibration study.

A big thanks goes to **Henk-Jan**, **Robert** and **Bob** for their technical support and positive attitude during my work in the Kleinhorst laboratory. You helped to establish and maintain the lab conditions for the AFM measurements.

I want to express my gratitude to the Thermal and Fluid Engineering group and all its members for their support, warm (pun intended) work atmosphere, and the friendships I was lucky to form.

Keerthi thank you for your constant will to help and your friendly and open attitude towards everyone. **Ali** and **Sara** thanks for the good spirit and for being the lunch patrol of the office, dragging me out of the office at least sometimes. Thanks to **Balan** and **Umair** for the friendly and fun attitude of the advanced PhD students— perhaps, I can relate to that somehow now. **Mohammad** thank you for your entertaining jokes and your positive attitude. **Shahzaib** thank you for your friendly support over the years. **Marijn** thanks for organizing all the football games and for your help with translation issues. Thanks to **Shuaiqiao**, **Hamid**, **Hamed, Guanxing, Andy, Sriram, Jesse, Berksu, Laura, Hossein, Hao, Rem, Yousef, Julius, Sathya, Yashar, Eddy, Thejas, Ahmed, Abhishek, Genie, Wilko, Artur, Amir, Mina, Dani uno y dos, Yan, Stefano and Xinming** for the comfortable and humorous office/group atmosphere and beyond. Apart from that, I want to thank you all for the activities outside university life, such as the poker nights or watching football games.

Many thanks to our secretaries **Sally**, **Sylvia** and **Susan** for your friendly and warm attitude and all the help you provided me during this time.

Harsha, thanks for the many coffee meetings in the heart of Enschede and the great trip to Finland (Frankfurter Junge). I want to specially thank **Christian** for the many lessons and the good time we had with our good friend Señor Moretti. **Mr. Wang** thanks for always being yourself. I am looking forward for a prompt Reunion (ganbei!). **Shubham** and **Edmond**, I am very grateful for our friendship and the great time we spend both academics as outside academics. I will always remember our various trips to different regions around Europe or the countless hours we spent at the university listening to our good friend David. It has been a joyful time, and I am grateful that I could always count on you.

Special thanks to my office mates **Hidde, Timo, Prasansha, Steve** and **Juan** for the comfortable and relaxed office atmosphere. Steve thanks for the funny conversations and the steady distractions from work. I specially want to thank Juan who has been my office mate from day one. You have been a great friend during that time, and I will always remember the many parties, your drive for la Vida loca, and your Batman-like separation of work and social life.

In conclusion I had a great time doing my PhD at the University of Twente and I am going to and already miss my office and all the people involved. In that context, I also want to thank the friendly staff of the Horst building and the campus who contributed to this comfortable atmosphere.

Apart from the Twente life, I want to thank my friends from outside the Netherlands for their constant cheering, your visits and the memorable times we shared.

Finally, I am very grateful to my family for the massive support during that time and beyond. **Fabian**, thanks for your constant believe and the many happy visits. Danke an **Renate**, für dein konstantes Interesse an meinem Wohlbefinden. And finally, I want to thank **Erik** and **Anita**, to whom I am eternally grateful. Without them, I could not have been the person I am today or have had the experiences that shaped me.