Utilizing the Insulator-to-Metal Transition of Vanadium Dioxide for Neuromorphic Computing
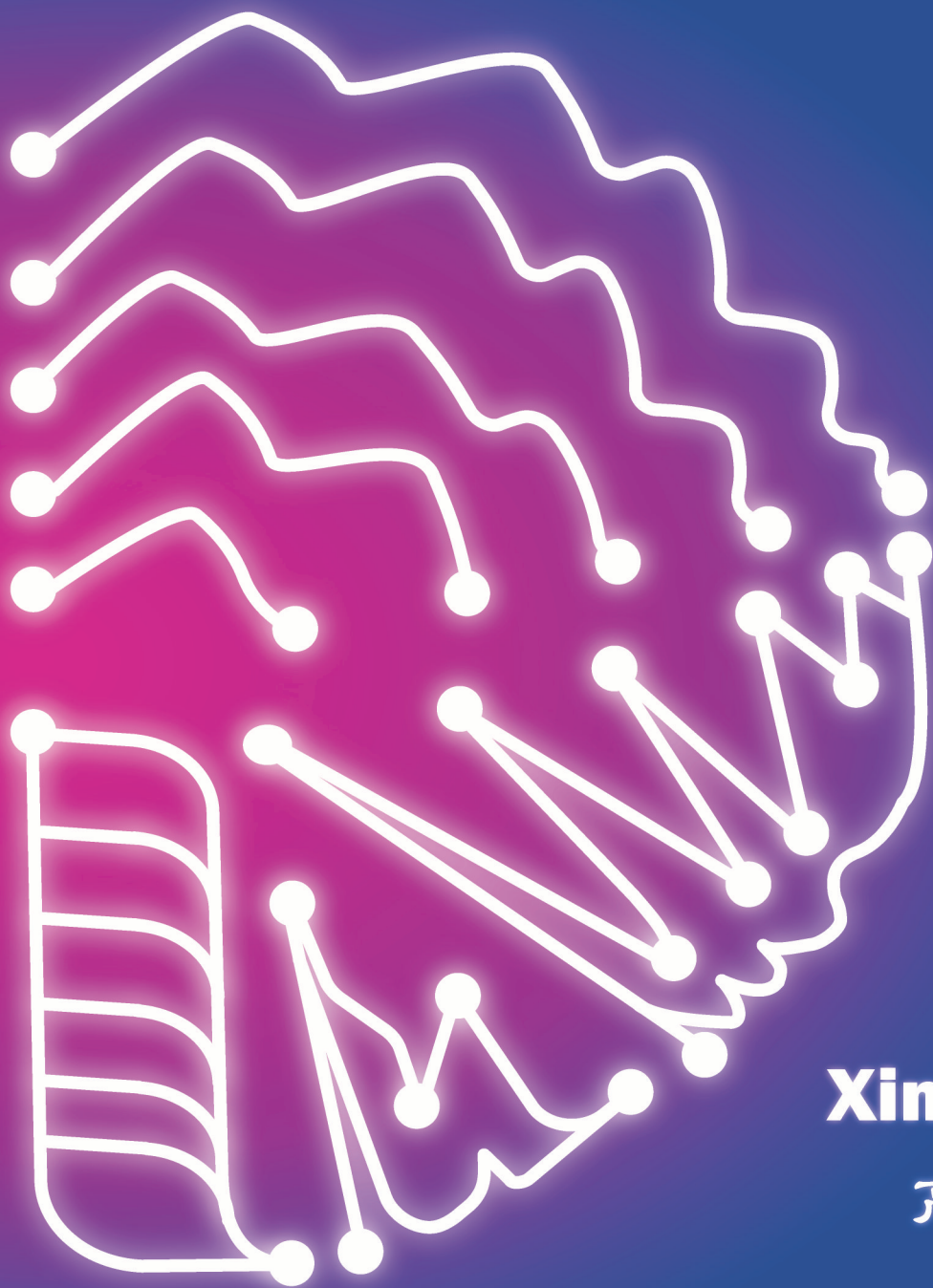
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UTILIZING THE INSULATOR-TO-METAL TRANSITION OF VANADIUM DIOXIDE FOR NEUROMORPHIC COMPUTING

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DISSERTATION

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This dissertation has been approved by the Promotors:

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Graduation Committee:

Contents

Chapter 1.

Introduction

An 'intelligent machine' with a level of intelligence comparable to the human brain has been searched throughout human history. Although current computers have benefited from Moore's law by scaling down transistors, fundamental limits fundamental limits lead to constraints on speed and energy efficiency in data-intensive applications. Neuromorphic computing systems, which are inspired by the human brain, are highly intriguing. To imitate the functions of the human brain, novel circuit elements are required. In this thesis, we propose novel switching devices with highly nonlinear behavior and tunable multi-states, which are assembled by single switching elements in a two-terminal configuration.

1.1 Brain-inspired computing

Throughout human history, people have always strived to create an 'intelligent machine' capable of advanced computation and perhaps even exhibiting a level of wisdom comparable to that of the human brain. From early mechanical computing devices like the ancient Chinese south-pointing chariot[1,2], which relied on geared wheels to navigate, to the more advanced electronic computers based on resistors, amplifiers, and vacuum tubes in the mid-1900s. The invention and development of transistors and integrated circuits enabled greater computing capabilities in a limited space, and by further reducing the size of electronic components, there has been a significant enhancement in computer performance and power[3,4].

The current computing system is based on the Von Neumann architecture[5], where the processing units and memory units are physically separated. This brings the Von Neumann bottleneck for data-intensive applications like Artificial Intelligence (AI) and Internet of Things (IoT). Moreover, the limits of conventional computing systems are fast approaching due to the fundamental constraints and the increasing demand for computing.

On the other hand, in 1948, prior to the development of electronic computers, Alan Turing proposed the concept of 'Intelligent Machinery', an unorganized machine that could learn and adapt like a human being[6]. By examining how infants learn, Turing explored the feasibility of creating an intelligent machine. However, researchers were not able to develop chips and devices that could realize the biological functions at the time, due to the limited understanding of neuroscience and immature device fabrication. Due to the development of neuroscience and device fabrication in the past few decades, more insights have been gained to design intelligent systems. Therefore, researchers have recently revisited the idea of mimicking the human brain.

The human brain is one of the most efficient computational architectures. In comparison to even the most powerful supercomputers today, such as Frontier in the US, which consumes 21 MW of energy, the human brain consumes only 20 W of energy[7] for certain type of information processing such as pattern recognition.

The human brain uses a completely different architecture than the Von Neumann principles.

Though there is still a long way before we comprehensively understand how the brain computes, researchers have uncovered some of the marked features, such as a computing fabric composed of large-scale networks of neurons and synapses[8–10]. Neuromorphic computers inspired by the human brain aim to improve computing efficiency by mimicking the functions of biological neurons and synapses using novel circuit elements[11–13].

1.2 VO$_2$ for neuromorphic devices

The neuromorphic computing circuitry requires novel circuit elements with tunable resistance states, nonlinear response functions and, for the case of spiking neuromorphic circuitry, adaptable dynamic behavior[14,15]. Vanadium dioxide (VO$_2$) is an attractive candidate material to fulfill some of these roles, since it exhibits a near-room-temperature, hysteretic insulator-to-metal transition (IMT) with resistivity changes of several orders of magnitude[16–19]. There are various knobs available for tuning the IMT, such as chemical doping[20], epitaxial strain[20,21], and external stimuli[22–24], making VO$_2$ a versatile and rich platform for realizing neuromorphic computing. Particularly, it can be triggered by electrical voltage/current and the associated Joule heating[25,26]. The electrical and thermal conductivity of VO$_2$ is highly temperature-dependent, leading to nonlinear dynamics in an electrothermal feedback loop[27,28]. Using such nonlinear behavior and the dynamical instabilities associated with a negative differential resistance (NDR), a range of neuronic spiking patterns can be achieved in VO$_2$-based neuromorphic circuits[29]. Furthermore, tunable multilevel resistive states have been achieved in VO$_2$ thin films, VO$_2$ single-bridge and multi-bridge devices[30–32].

1.3 Outline

This thesis aims to contribute to the development of neuromorphic computing by exploring devices based on VO$_2$ with unique switching characteristics. The resistive switching behavior is not only influenced by the intrinsic material properties but can also be tuned on a device level. Utilizing the electrically induced IMT of VO$_2$, we propose strategies to establish a two-terminal device with novel switching behaviors, including multi-switches, multi-level

operation, highly nonlinear responses, etc.

In **Chapter 2**, we review the recent progress in utilizing VO_2 for neuromorphic computing circuits and explain the motivation behind this research, which is to overcome the limitations and bottlenecks of current computing architectures. We focus on hardware aspects of neuromorphic computing systems and introduce a key building block; the memristor. We discuss the physical principles of the memristive phenomena, with a specific focus on the IMT of VO_2 and its driving force. This discussion will serve as the basis for understanding the experimental results presented in the subsequent chapters.

In **Chapter 3**, we introduce the thin film fabrication of VO_2 through pulsed laser deposition (PLD) and the subsequent characterization of the deposited films. The as-deposited films are examined for surface topography, chemical composition, crystal structures, and transport properties. Additionally, the impact of substrate-induced strain is explored by depositing thicker films and their evolution and relaxation has been analyzed. To further fabricate reliable resistive switching devices for room-temperature applications, VO_2 films with a thickness below the critical value are preferred to avoid the emergence of cracks.

In **Chapter 4**, we present the fabrication of two-terminal single-bridge devices and report on their reproducible switching behaviors. Resistive switching can be achieved by applying electrical bias, which creates Joule heating in the device and triggers the IMT. Controllable switching behavior is demonstrated between multiple resistance levels over several orders of magnitude, allowing for multibit operation. We also investigate the influence of fabrication techniques, including etching methods such as Ar ion milling and wet etching, on the switching behavior.

Based on the findings in Chapter 4, we explore devices with more complex configurations, starting with double bridges in **Chapter 5**. By assembling single bridges in a parallel configuration, we can achieve a higher degree of control for multistate characteristics. As one more switching element is added, the switching behaviors are influenced by the intrinsic IMT of individual bridges and the thermal interaction among them. We study the switching dynamics and the effect of thermal crosstalk using current-controlled measurements and in-operando scanning thermal microscopy (SThM). By understanding the switching principles

of VO$_2$ double-bridge devices, novel circuit elements can be obtained through structural manipulation of devices assembled from individual switching elements.

In **Chapter 6**, we further extend the device configuration to multiple bridges. We examine the effect of several factors at a device level, such as the number of bridges, spacing between bridges, and geometries of bridges. We fabricate and measure devices with additional bridges, such as triple-bridge and quintuple-bridge devices, as well as devices with multi-width bridges. We discuss the competition and interaction among the bridges due to the rising complexity in the device configuration. We report that the addition of extra bridges will introduce the potential for more switches and resistive states, providing insights into the switching principles of VO$_2$ multi-bridge devices and enabling novel circuit elements through structural manipulation of devices assembled from individual switching elements.

In **Chapter 7**, we focus on scaling down the dimensions of the parallel bridges from tens of micrometers to several hundreds of nanometers. We report on the resistive switching behaviors of single-bridge, double-bridge, and multi-bridge devices in the nano-scale range. We reveal that the switching principles and rules observed for micro-scale devices are still applicable for nano-scale devices, but with significantly lower switching power requirements. Finally, in **Chapter 8**, we summarize the findings of our study on VO$_2$-based parallel-bridge devices. Considering the needs of the neuromorphic computing research area and our knowledge, we provide perspectives for future research and pose several open questions to be answered. The ability to control the novel switching behaviors at a device level assembled by single bridges may result in the development of novel circuit elements and broaden the application of neuromorphic computing.

Chapter 2.

Motivation and review

Neuromorphic device concepts that imitate the functionality of neurons and synapses are of particular interest in overcoming limitations of computing systems based on the Von Neumann architectures, such as excessive data transfer between memory and logic units. The neuromorphic computing circuitry requires novel circuit elements with tunable resistance states, nonlinear response functions and, for the case of spiking neuromorphic circuitry, adaptable dynamic behavior. VO_2 is an attractive candidate material to fulfill some of these roles, since it exhibits a near-room-temperature, hysteretic insulator-to-metal transition (IMT) with resistivity changes of several orders of magnitude. This chapter aims to provide the motivation for the research on utilizing VO_2 for neuromorphic computing and a basis for understanding the experimental results in the upcoming chapters.

2.1 Introduction

The invention of electronic computers is widely considered one of humanity's greatest achievements and was a defining moment that ushered in the information age. While the introduction of transistors and integrated circuits enabled greater computing capabilities in a limited space and resulted in significant enhancements in computer performance and power through size reduction of electronic components[3,4], current computing architectures still suffer from limitations and bottlenecks, such as the excessive transfer of data between memory and logic units[33]. Neuromorphic device concepts have been explored by researchers as a solution to these constraints. These devices are designed to mimic the functions of neurons and synapses in the human brain and require novel circuit elements with tunable resistance states, nonlinear response functions, and adaptable dynamic behavior[14,15]. VO_2 is a promising material candidate, as it displays a nearly room-temperature, hysteretic IMT with resistivity changes of several orders of magnitude[16,17].

This chapter aims to review the limitations and bottlenecks of current computing architectures and the requirements for novel computing techniques. We will focus on the hardware aspect of neuromorphic computing systems and introduce the foundational unit, memristor. We will discuss the physical principles of the memristive phenomena, with a focus on the IMT of VO_2 and its driving force. The recent progress in utilizing VO_2 for neuromorphic computing circuits will also be discussed.

2.2 Brain-inspired computing systems

2.2.1 The need for novel computing techniques

As Gordon Moore predicted in 1965, the number of transistors on a microchip doubles every two years leading to an increase in the speed and capability of computers[4]. Over the years, semiconductor manufacturers have kept up with Moore's law. However, the progress of the scaling down has also led to a growing demand for computing[14], mainly driven by AI and IoT data, which is generated at an exponential rate (Figure 2.1).

Therefore, computing is constrained by the need to control temperature rise on the chip and

the limitations in the data transfer rate. As a result, the increase in the computing speed has been slowed down recently and the computing gap emerges as shown in Figure 2.1.
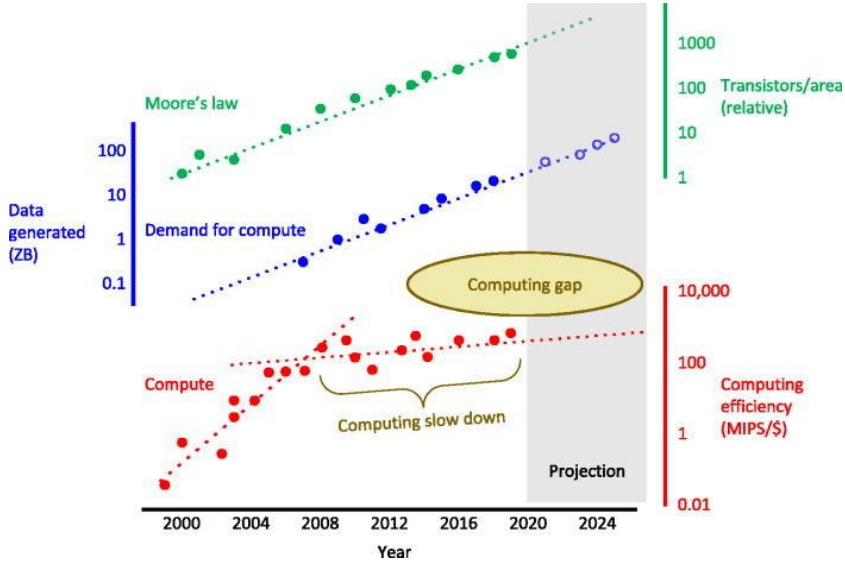
Figure 2.1 A comparison of Moore's law (green circles), demand of compute (blue circles), and computing efficiency (red circles) against years. Solid circles are data and dashed lines are linear fits (on a logarithmic scale). The transistors/area and the generated data are at an exponential pace. The generated data are in zettabyte (ZB) range. 1 ZB = 1021 B. The computing efficiency is measured in terms of the processor speed and the cost, typically quantified as millions of instructions per second per dollar (MIPS/$). This figure is reproduced from [14].

The computing gap can be attributed to several factors. Firstly, the performance of complementary metal-oxide semiconductor (CMOS) components is fundamentally constrained by the Fermi-Dirac distribution of electron energies at room temperature, which limits the steepness of the subthreshold voltage swing to 60 mV per decade increase in current across a transistor channel[34]. This figure of merit, which describes the exponential behavior of the drain current as a function of the gate voltage, is crucial in determining the switching speed and power for transistors.

The other reason is the failure of the Dennard scaling of power density. In 1974, Robert Dennard proposed that as the dimensions of the transistors shrink, power density will remain constant for a given area of chip and the voltage and current will also scale down[35]. However, Dennard scaling ended around 2004; as it became impossible to keep reducing current and

voltage while still ensuring the dependability of integrated circuits. This discontinuation of scaling has resulted in a significant increase in power density that makes it difficult to power on all transistors simultaneously while maintaining safe operating temperatures. Consequently, a growing proportion of the circuitry cannot be powered on at the nominal operating voltage, giving rise to the so-called 'dark silicon' problem[36].

Moreover, further downsizing of transistors is challenging and has its limitations and drawbacks. Decreasing transistor size also means reducing the size of the metal connections that link them, leading to higher electrical resistance and limiting operational frequency. Lowering the operating voltage of circuits is feasible up to a certain extent, but there are minimum threshold voltages for memory circuits that cannot be surpassed. Reducing the voltage below a certain level also results in incomplete switching of transistors, leading to unreliable operation.

Recently, a crucial question has been raised about whether Moore's law has reached its end, given the limitations and inefficiencies of further scaling down the transistors. While it is still premature to conclude that it has ended, it is never too early to explore new and more intelligent computing approaches.

2.2.2   Inspired by the human brain

The basis of current computing is the Von Neumann architecture which emerged in 1945[5]. As illustrated schematically in Figure 2.2, it consists of three primary elements: 1) A central processing unit (CPU), 2) a memory unit and 3) an input/output mechanism. The CPU is the electronic circuit responsible for executing the instructions of a computing program. The CPU contains a control unit (CU) for processor control signals, an arithmetic/logic unit (ALU) for all calculations, and a variety of registers, which are the high-speed storage areas. The memory unit consists of random access memory (RAM) that is directly accessible by the CPU. During computing, there are buses continuously shuttling back and forth data between these physically separate parts. Data buses carry data between memory unit, the input/output devices, and CPU. Address buses carry the address of data between memory and CPU. Control buses convey control commands from the CPU. However, as the instructions can

only be executed one at a time and sequentially, this leads to significant inefficiency in terms of area, energy, and rate for data-intensive applications like AI and IoT. This phenomenon is known as the Von Neumann bottleneck[33].
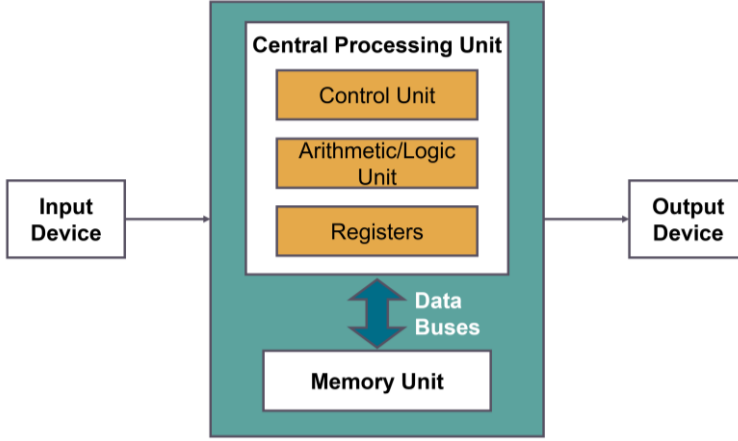
Figure 2.2 Schematic illustration of the Von Neumann computing architecture.

To overcome the limitations and bottlenecks, one promising solution is to adopt new computing alternatives. Neuromorphic computers inspired by the human brain aim to improve computing efficiency by achieving parallel computing, in-memory computing, and analog computing through the realization of both the functions of neurons and synapses. A neuron is used for information processing, and its spiking behaviors can be described by mathematical models such as the Hodgkin-Huxley model[37,38] and the Leaky Integrate-and-Fire (LIF) model[39,40]. In the LIF model, a neuron can be represented as an RC-circuit with a threshold. Once the external potential exceeds this threshold, the neuron releases an action potential, typically in the form of a voltage spike. The neurons are connected with each other through axons (outputs), dendrites (inputs) and synapses in between. The synaptic weight indicates the strength of the connection between two neurons, and the synaptic plasticity, which allows for altering the weight when accommodating new information, is the foundation of the learning ability and memory formation[41,42].

The most commonly used model is the Artificial Neural Network (ANN)[43,44] consisting of

connected nodes called artificial neurons. These neurons process signals through functions; such as a threshold function that enables them to fire a signal when the input surpasses a threshold value. The connections between neurons are artificial synapses with adjustable weights. The simplest version of the neural network with only one hidden layer is depicted in Figure 2.3. However, for more complex computing tasks, Deep Neural Networks (DNNs) with multiple hidden layers are required to perform various signal transformations[45–47]. Several progresses in algorithms have been made to achieve efficient training and computing with ANNs[48,49]. However, implementing these algorithms on conventional CMOS circuitry will lead us back to the Von Neumann bottleneck. As a result, researchers are paying increasing attention to hardware beyond CMOS, based on novel neuromorphic materials and device architectures. Among these, the memristive device is the main functional unit.
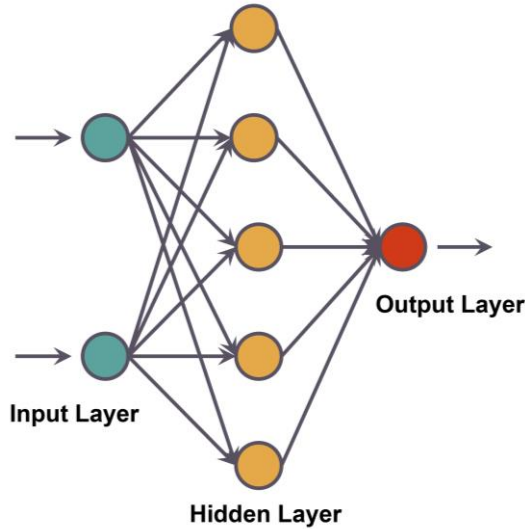
Figure 2.3 Schematic illustration of an artificial neural network with one hidden layer.

2.2.3   Memristor and memristive systems

The memristor, also known as a resistive switching device, is an electronic device whose internal states are dependent on the history of the current and/or voltage it has experienced[50].
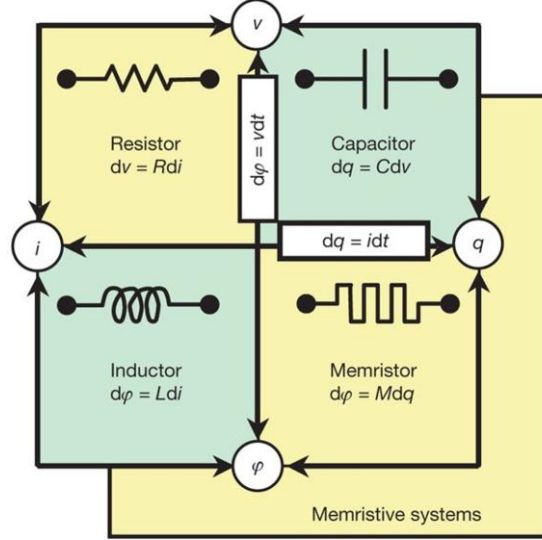
Figure 2.4 (a) The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor. Resistors and memristors are subsets of a more general class of dynamical devices, memristive systems. The figure is reproduced from [51].

In 1971, L. O. Chua first theoretically formulated the concept of the memristor by establishing a theoretical relationship between the charge, q and the flux φ, as given by Equation 2.1[52].

$$d\varphi = Mdq \qquad (2.1)$$

Here, M is the Memristance. This definition is a purely theoretical element to fulfill the missing link in the relation of the voltage, V, the current, I, the charge, q and the flux, φ (Figure 2.4). The relation of q and φ is also given by Equation 2.2.

$$dq = Idt$$
$$d\varphi = Vdt \qquad (2.2)$$

Therefore, Equation 2.1 can be rewritten as Equation 2.3.

$$Vdt = M \cdot Idt \tag{2.3}$$

When the parameter M is constant, a memristor behaves like a conventional resistor. It is only when M is also dependent on q, leading to a nonlinear relationship, that a memristor exhibits its distinctive characteristics as a unique circuit element.

A more general memristive system was introduced in 1976 by Chua. It is a two-terminal device that can be defined by a complex state-dependent Ohm's law and a state equation, as given by Equation 2.4[53].

$$V(t) = R(x, I, t) \cdot I(t)$$
$$\dot{x} = f(x, I, t) \tag{2.4}$$

Here, x is an internal state variable or a vector of n internal state variables $x = (x_1, x_2, \ldots, x_n)$, which can be a chemical composition, the temperature of the device, etc. Based on the equations, the resistance R is nonlinear and dependent on the history of the device. The hysteresic current-voltage (I-V) characteristics during a periodically varying bias and the zero-crossing property are important features of the memristive systems. The zero-crossing property ensures that the output of the system reaches zero, regardless of the device state, when the input is zero.

In practice, the common structure of a memristive device is a metal/insulator/metal (MIM) cell, with the switching medium sandwiched between two electrodes. These devices typically show two stable resistive states: the high resistive state (HRS) or OFF state and the low resistive state (LRS) or ON state. In some cases, the devices can operate at multiple levels with several intermediate resistive states[54].

The memristive systems can be classified into two types according to the retention time of the LRS, namely non-volatile and volatile[55]. Non-volatile memristors can maintain both HRS and LRS after the removal of external bias, while the volatile memristive devices will instantly return to HRS from LRS when the external bias is removed. Figure 2.5 illustrates the voltage-controlled I-V characteristics of the non-volatile switching in two operation modes, depending on different material combination in the MIM cell. In bipolar resistive switching, as shown in Figure 2.5(a), the set process is triggered by increasing the voltage

bias beyond the threshold value (V_{TH1}) from the HRS. A current compliance (I_{CC}) is usually used to protect the device during the set operation. For the reset process, the bias with opposite polarity (V_{TH2}) is applied to switch the device back to the HRS. On the other hand, all the voltage biases are with only one polarity in unipolar resistive switching, as shown in Figure 2.5(b). There are also specific cases such as nonpolar switching, where the switch can be triggered by an electrical bias of either polarity[56], and complementary switching, which can be accomplished by connecting two bipolar switching cells in an anti-serial fashion[57].

Figure 2.5 Non-volatile resistive switching characteristics. (a) A typical *I-V* sweep demonstrating one cycle of bipolar resistive switching, where the set state is triggered with a positive polarity and reset with a negative polarity. (b) A typical *I-V* sweep demonstrating the unipolar resistive switching characteristics, where the set and reset states are achieved with the same bias polarity. The figures are adapted from [58].
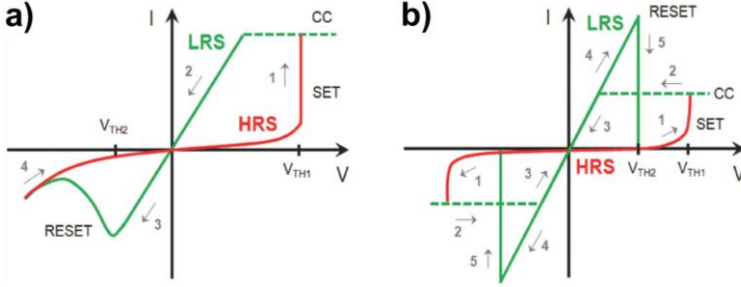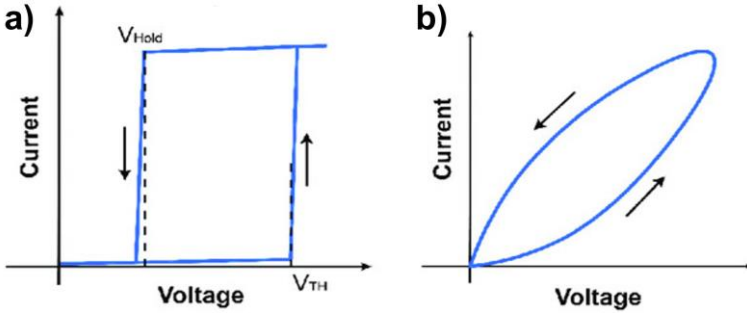

Figure 2.6 Volatile resistive switching characteristics. (a) A typical *I-V* sweep demonstrating one cycle of digital/threshold resistive switching, where the set and reset processes are abrupt. (b) A typical *I-V* sweep demonstrating one cycle of analog resistive switching, where the set and reset processes are gradual. The figures are adapted from [55].

Volatile switching can be generally divided into two types: digital switching (or threshold switching) and analog switching[55], as illustrated in Figure 2.6. In digital switching (Figure 2.6(a)), the device exhibits a sharp increase in current when the applied voltage exceeds the threshold value (V_{TH}). When the applied bias is below the hold voltage (V_{Hold}), the device returns abruptly to the HRS. In contrast, in analog switching (Figure 2.6(b)) there is continuous and incremental transition from the HRS to LRS and vice versa.
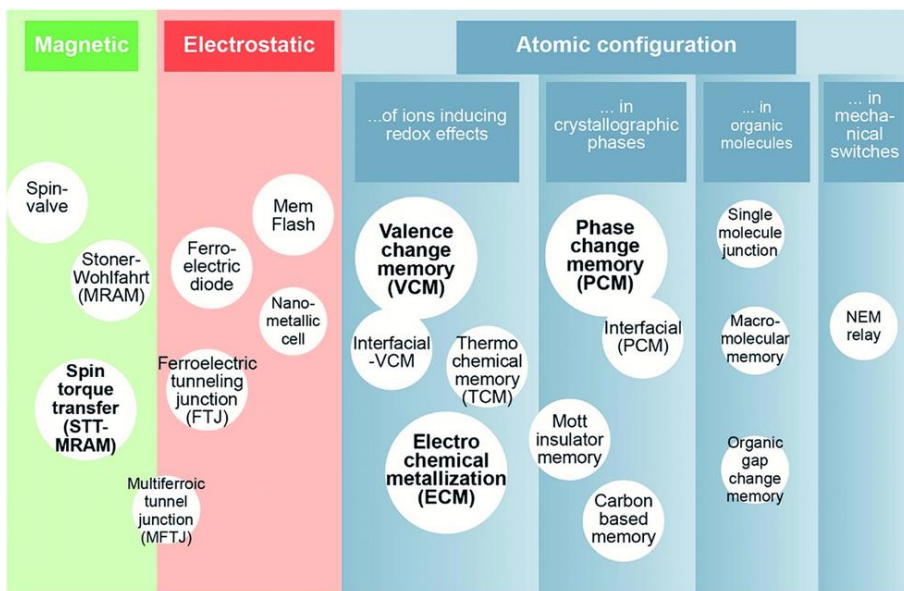
Figure 2.7 Survey of fundamental physical principles of memristive phenomena. The figure is reproduced from [59].

The memristive systems can further be categorized based on the fundamental physical principles of memristive phenomena, including magnetic, electrostatic, and atomic effects. As reported by Waser et al.[59], the majority of these effects stem from the configuration of atoms, which can be further subdivided into the motion of ions on the nanoscale and related redox effects, phase transition, configuration changes in organic molecule and nanoelectromechanical switches (Figure 2.7). Valence change memory (VCM), electrochemical metallization (ECM) and phase change memory (PCM) are among the most prominent effects.
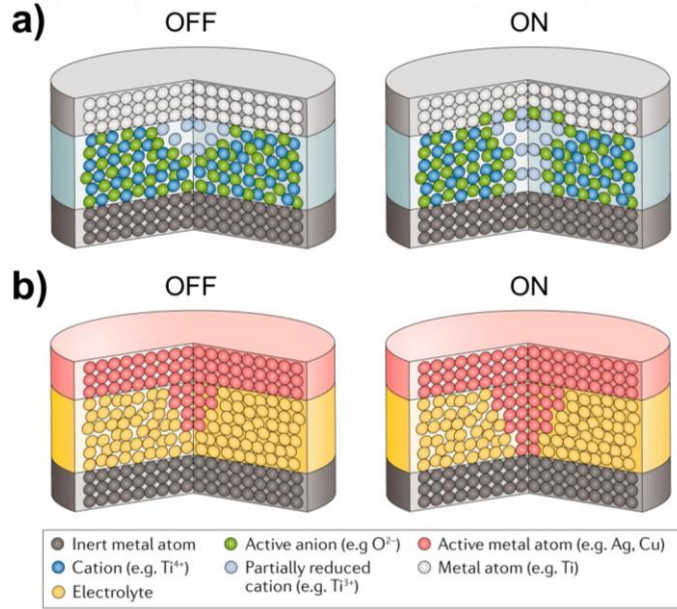
Figure 2.8 (a) Illustration of an oxygen-vacancy filament in the OFF state (left) and ON state (right) in a valence change memory cell. (b) Illustration of a metal-atom filament in the OFF state (left) and ON state (right) in an electrochemical metallization memory cell. The figures are adapted from [60].

The VCM effect is observed in a variety of oxide systems, such as TiO_2[61], Ta_2O_5[62], $SrTiO_3$[63], etc. The mechanism underlying is the migration of anions, such as oxygen vacancies, that modifies the stoichiometry of the insulator region via oxidation-reduction reactions[64]. In most cases, the switching occurs in conductive filaments in the VCM cell[65]. An electroforming step is required to create initial conductive filaments, which involves applying a large electrical bias. The device can then be reproducibly switched by partially forming and rupturing the filaments (Figure 2.8(a)). In contrast, in other cases, the switching happens over the entire cross section of the electrode interface[66].

The ECM effect is usually involved in the MIM cell with an electrochemically active electrode, such as Ag or Cu, and a noble counter electrode, such as Pt[67] or Au[68]. The switching process also involves the formation and rupture of conductive filaments, which are formed by the movement of dissolved metal cations from the interface of the electrochemically active electrode into the insulator region (Figure 2.8(b))[60].
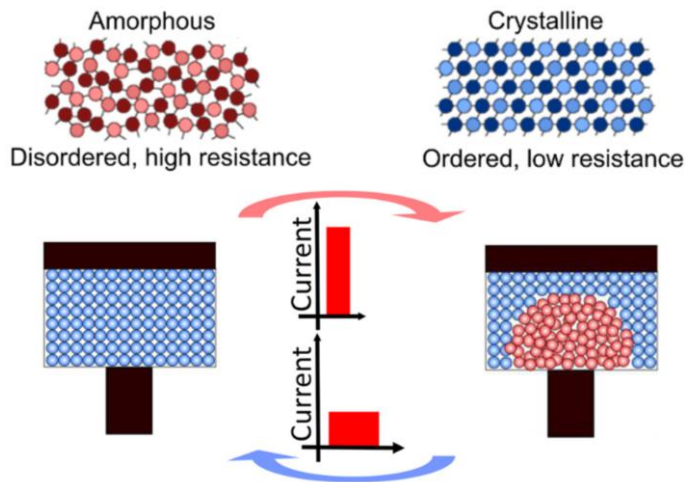
Figure 2.9 Illustration of the amorphous phase (high resistance) and crystalline phase (low resistance) in a phase change memory cell. The rapid and reversible phase transition can be triggered by the application of suitable electrical pulses. The figure is reproduced from [69].

The PCM effect relies on the distinctive electrical property of compounds composed of Fe, Te, and Sb, which show significant different resistivities between their crystalline and amorphous phases[69]. The switching behavior is induced by applying electrical pulses (Figure 2.9). With high-current pulses, the material melts and remains amorphous when the pulse is abruptly stopped, resulting in the HRS. Conversely, when low-current pulses are applied, the amorphous region becomes crystalline, switching the device to the LRS.

One challenge with the techniques discussed is that they involve atomic displacements and reconfigurations, which can lead to variations in device properties and fatigue. As a result, the Mott insulators, such as VO_2 and NbO_2, are gaining attention from researchers due to their ability to undergo rapid electronic transitions and low entropy dissipation[70]. As shown in Figure 2.7, the Mott insulator memory effect is based on the changes of both the structural and electronic structure, which are subtle but can lead to abrupt changes in the electrical conductivity with several orders of magnitude. VO_2 is an attractive example, exhibiting a hysteretic IMT just above room temperature[16,17]. The driving force behind the IMT of VO_2 and the associated memristive behavior will be discussed in the following sections.

2.3 Insulator-to-metal transition in VO_2

2.3.1 Vanadium oxide family

The vanadium-oxygen phase diagram in Figure 2.10 shows the presence of numerous vanadium oxide compounds[71], as vanadium can exist in four different oxidation states: 2^+, 3^+, 4^+, and 5^+. The oxides fall into two homologous series: the Vanadium Magnéli phases, which are represented by V_nO_{2n-1} (n>1), and the Vanadium Wadsley phases, represented by V_nO_{2n+1} (n>1). The Magnéli phases have V_2O_3 (n=2) and VO_2 (n=∞) as their end members, with intermediate compounds having a mixed valence between V^{3+} and V^{4+}. The Wadsley phases have V_2O_5 (n=2) and VO_2 (n=∞) as their end members, with vanadium valences of V^{5+} and V^{4+}. VO_2 lies between the Magnéli and Wadsley phases of vanadium oxides. Interestingly, several of these compounds exhibit simultaneous electronic, structural, and magnetic phase transitions[72]. The underlying factors driving these transitions, such as electron-electron correlations, magnetic exchange energy, and electron-phonon coupling, remain the subject of intense study in condensed matter physics. Figure 2.11 illustrates the remarkable electrical properties, for example the temperature-dependent resistivity, of various vanadium oxides with high oxygen content[73].
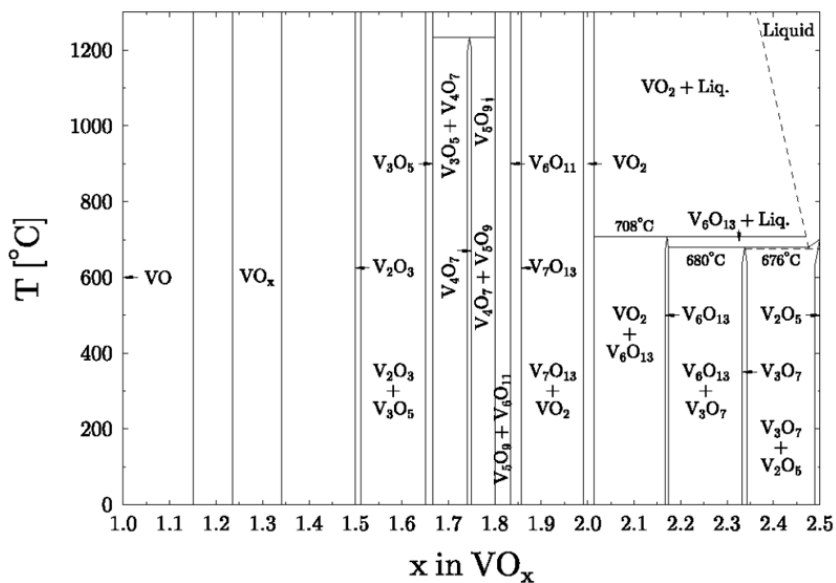
Figure 2.10 V-O phase diagram showing phase equilibria between the various V-O Magnéli and Wadsley phases. This figure is reproduced from [71].
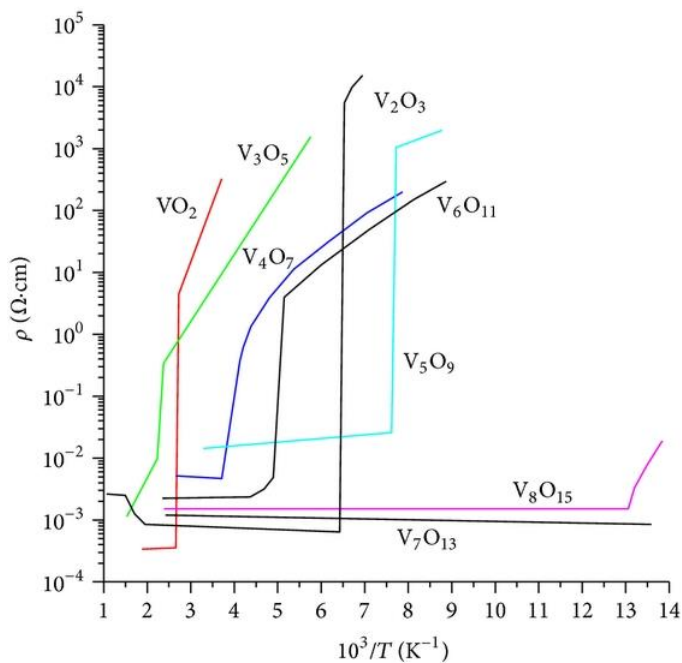

Figure 2.11 Temperature dependence of the resistivity of various vanadium oxides with high oxygen content. This figure is reproduced from [73].

2.3.2   Insulator-to-metal transition of VO$_2$ and phase coexistence

Among the vanadium oxide family, VO$_2$ is a favorable candidate for room-temperature applications due to its sharp IMT occurring near room temperature (T_{IMT} ~340 K in bulk), which results in a resistivity change of 3-5 orders of magnitude. The IMT can be tuned by chemical doping[20], epitaxial strain[21,74], and external stimuli such as temperature[31], electrical current/voltage[23,30] and photoexcitation[75].

An example of resistance-temperature (R-T) measurements performed on a 10-nm VO$_2$ film by Rana et al. at the University of Twente is shown in Figure 2.12[31]. It should be noted that the T_{IMT} of the thin epitaxial film is lower than that of the bulk, and the effects of strain will be discussed in the next chapter. The R-T characteristics exhibit a hysteresis loop, as the phase transition temperatures of the heating and cooling branches are different. This hysteresis is related to energy overpotentials required for nucleation of a new phase in either transition direction and it can be influenced by the microstructure and oxygen stoichiometry[76,77]. The occurrence of hysteresis allows for the coexistence of the metallic and insulating phases within the span of the IMT, enabling the stabilization of intermediate resistive states by reversing the temperature during the cooling (Figure 2.12(a)) or heating process (Figure 2.12(b)).
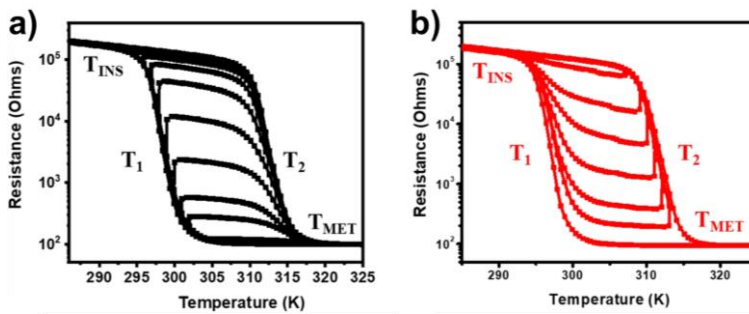

Figure 2.12 Insulator-to-metal transition of a VO$_2$ thin film (thickness ~10 nm) during (a) cooling and (b) heating process. Both show the ability to achieve stable intermediate resistance states, where in (a) during the cool down the temperature is reversed at T_1 and in (b) the temperature is reversed at T_2. The figures are reproduced from [31].

The existence of phase coexistence was also observed by Qazilbash et al. using scanning near-field infrared microscopy (s-SNIM) with a spatial resolution of 20 nm[19]. Optical imaging revealed the formation of a strongly correlated conducting state in the form of nanoscale metallic puddles that arises within the IMT range. Moreover, to quantitatively map the phase coexistence, Madan et al. used scanning microwave microscopy (SMM) to measure the impedance at the nanoscale during the phase transition[78]. Their results show that metallic nanoscale domains appear within the insulating matrix during the IMT transition, and with increasing temperature reach a threshold radius of approximately 100 nm before coalescing to form larger regions. This phase coexistence indicates that the film is composed of nanoscale domains with varying transition temperatures due to defects, composition, and local strain. As a result, adjusting the intermediate resistive states by temperature is essentially achieved by tuning the amount of metallic domains present.

2.3.3   Crystal and electronic structure of VO_2

The IMT is normally accompanied by structural transformation from an insulating monoclinic phase to a metallic rutile phase, as well as by changes in electronic band structure near the Fermi level (E_F)[18,79].

The rutile crystal structure of VO_2 at high temperature exhibits $P4_2/mnm$ space symmetry and has cell parameters of $a_R=b_R=4.55$ Å and $c_R=2.86$ Å[80]. In the VO_2 (R) crystal structure, depicted in Figure 2.13(a) with two units of a rutile VO_2 unit cell, V^{4+} ions occupy both the body center and the vertex of the tetragonal structure. Each V^{4+} ion is surrounded by six O^{2-} ions, forming an octahedral VO_6 unit. The nearest distance between V-V atoms along the c_R-axis direction is 0.286 Å.

During the phase transition, the crystal structure undergoes a change to the low-temperature monoclinic phase with a space group $P2_1/c$ and unit cell parameter of $a_M=5.75$ Å, $b_M=4.52$ Å, $c_M=5.38$ Å and $\beta=122.6^o$[72]. In the VO_2 (M1) structure (Figure 2.13(b)), the V atoms shift away from the vertex angle, which results in the dimerization of the neighboring V atoms along the c_R axis. These V-V dimers are tilted along the rutile [110] and [$1\bar{1}0$] directions, leading to the occurrence of two distinct bond lengths, 2.65 Å and 3.12 Å[72].
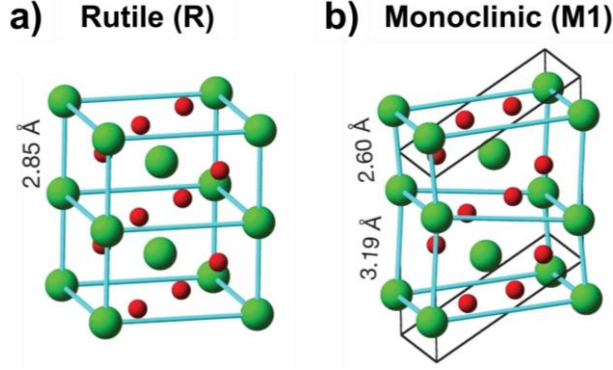
Figure 2.13 VO$_2$ atomic structures in the (a) metallic rutile phase and (b) insulating monoclinic phase (The green balls represent V atoms and red balls represent O atoms). V-V spacings are also shown. The figures are reproduced from [81].
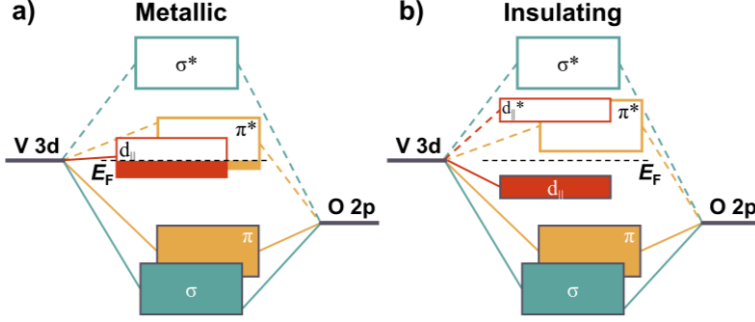
Figure 2.14 VO$_2$ electronic band structures in the (a) metallic phase and (b) insulating phase.

Figure 2.14 illustrates the changes in the electronic band structure of VO$_2$ near E_F during the transition from the metallic phase to the insulating phase, first proposed by Goodenough[18]. The $3d$ electronic levels of the V ions are crystal-field split into a combination of low-energy t_{2g} states and high-energy e_g^σ states, where σ denotes the symmetry of the V-O bonds. The t_{2g} orbitals are further separated by the octahedral crystal field into a single a_{1g} orbital and a two-fold degenerate π^* orbital. The a_{1g} orbitals ($d_\parallel$) are directed parallel to c_R axis and are relatively non-bonding with O $2p$. The π^* and e_g^σ orbitals hybridize with the O $2p$ orbitals and form low-energy bonding combinations with mainly O $2p$ character and high-energy anti-bonding combinations with mostly V $3d$ character[18,82].

In the metallic state, the $d_\parallel$ and π^* orbitals overlap at E_F, where the density of states (DOS) is non-zero, resulting in the metallic behavior[79,83]. When it transitions to the insulating phase,

the dimerization and tilting of the V-V bonds cause several changes in the band structure. Firstly, the dimerization of V-V bonds promotes $3d$-$2p$ hybridization, which splits the highly directional $d_\parallel$ orbitals into a bonding $d_\parallel$ state and an anti-bonding state $d_\parallel^*$. Additionally, the tilting of the V-V dimers enhances p-d overlap causing an upward shift of the π^* orbital in energy[84]. As a result, an energy gap of approximately 0.6 eV emerges and the E_F falls within the forbidden band, making the VO_2 insulating[79].

2.3.4   Driving force behind the insulator-to-metal transition of VO_2

The driving force behind the IMT of VO_2 remains the most challenging topic to unravel and still requires further investigation, since the electronic phase transition and structural phase transition happen nearly at the same time. The transition has been explained by two primary theories: the Peierls transition[85] and the Mott-Hubbard transition[86].

The Peierls transition is supported by the crystal-field model suggested by Goodenough[18], as discussed earlier, which proposes that the opening of the band gap is induced by lattice distortion, resulting in a decrease in the energy of the overall electronic lattice system[87]. Moreover, recently, Budai et al reported the important role of lattice vibrations during the phase transition[81]. They revealed that the IMT arises from a competition between the lower electronic energy in the insulating phase due to the Peierls instability and the higher entropy of the metallic rutile phase caused by soft anharmonic phonons. The soft lattice dynamics in the rutile phase reflect the intrinsic effects of electronic and structural instabilities that drive the IMT.

However, the Peierls transition theory fails to explain the broad experimental band gap of M1-VO_2 (0.6 eV) and the intermediate phases such as the monoclinic M2 phase[85,86]. These issues can be settled by the Mott-Hubbard transition theory by introducing the additional Hubbard energy (U) in the conventional density-functional theory (DFT). DFT+U calculations consider the repulsion of the d/f electrons in the highest occupied orbital of the transition metal atoms[88]. The strong Coulomb interaction between the electrons causes the electronic states near the E_F to split into bonding and antibonding states, leading to the opening of the energy gap[86,89].

These two theories are coupled with each other as both the electron-electron interactions and V-V dimerization distortions contribute to the IMT. Additionally, the discovery of the monoclinic-metallic phase has shed light on the role of electron-lattice interactions[90,91]. Ultimately, the IMT results from the interactions and competition among electrons, orbitals, and lattices.

2.4 VO₂-based memristive devices

2.4.1 Switching behavior of VO₂-based memristive devices

Typically, VO₂-based memristive switching devices show volatile threshold switching behavior due to the sharp resistivity transition. The switching mechanism of the electrical-driven IMT (E-IMT) has been widely studied. The primary mechanism is the conducting filament formation triggered by current-induced Joule heating[26,92]. With various *in-situ* characterization techniques, the forming process of the filaments has been visualized both statically[78,93] and dynamically[25,90]. As reported by Kumar et al., the current flows inhomogeneously due to intrinsic defects in the device where the temperature increases locally, leading to the phase transition and nucleation of the metallic domains[90]. Once a small portion transits to the metallic state, the current increases and the Joule heating triggers filament percolation and expansion. The filament formation is avalanche-like on a time scale of nanoseconds[25]. However, the relaxation of the filament is uniform and much slower, taking a time scale of milliseconds[26].

Besides the Joule-heating induced IMT, Madan et al. proposed an insulating domain network model to study the role of the electrical field in E-IMT[78]. A large voltage applied across many interconnected insulating domains will switch one of them to the metallic domain at some point. As a result, the potential drop across it is significantly reduced, which in turn is redistributed to the neighboring domains. This redistribution increases the probability that one of these neighboring domains will also transition to the metallic state. Due to the interplay between the domains, the formation of the filament is an abrupt process.

There have been efforts to realize non-volatile switching behavior in VO₂-based memristive

devices, given the potential intermediate states provided by the hysteresis nature of the transition. This has been achieved through methods such as chemical doping[94], operating in the hysteretic regime by biasing the operation temperature[95], using a voltage bias[96], current[26] or light illumination[75]. As a result, VO$_2$-based memristive devices show non-volatile switching behavior with switchable and retainable intermediate states. This feature of being able to alter between volatile and non-volatile behaviors is unique and particularly attractive for brain-inspired computing systems, as it allows for the implementation of both artificial neurons and synapses within a single material system.

2.4.2 VO$_2$-based artificial neurons and synapses

As previously discussed, the electrical and thermal conductivity of VO$_2$ is highly temperature-dependent, leading to nonlinear dynamics in an electrothermal feedback loop[27,28], which makes VO$_2$ a promising candidate for artificial neuron applications. To achieve spiking behavior, a Pearson-Anson relaxation oscillator is commonly used, where a VO$_2$ switching element is connected in parallel with a capacitor and in series with a resistor (Figure 2.15). Upon biasing with a constant voltage or current, the circuit generates self-oscillations due to the dynamical instabilities during the E-IMT[97]. While individual VO$_2$ switches operate at nanosecond timescales[98,99], oscillators typically function in the MHz range or slower[100,101].
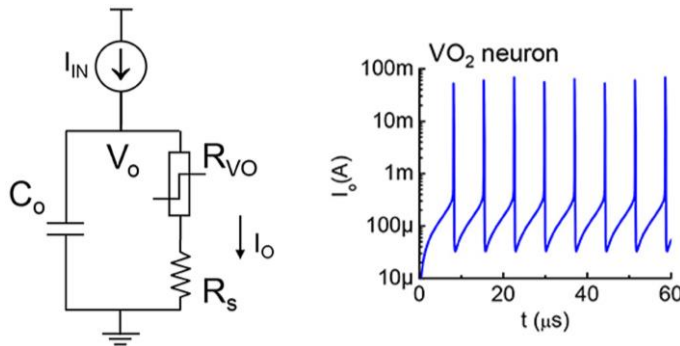

Figure 2.15 LIF neuron circuit with current pulse input and its current spiking behavior. The figures are reproduced from [102].

To achieve more complex neuronal behavior, additional components are needed in the circuit. Yi et al. demonstrated up to 23 kinds of neuronic spiking patterns in VO$_2$-based neuromorphic circuits (Figure 2.16)[29]. In their circuit, two VO$_2$ switching elements are biased with two DC sources and connected to capacitors in parallel to mimic the function of Na$^+$ and K$^+$ ion channels on a neuron membrane. By changing the series connection among the resistor, capacitor, or a capacitor and resistor couple, various neuronal behaviors can be generated, including all-or-nothing firing and tonic spiking.
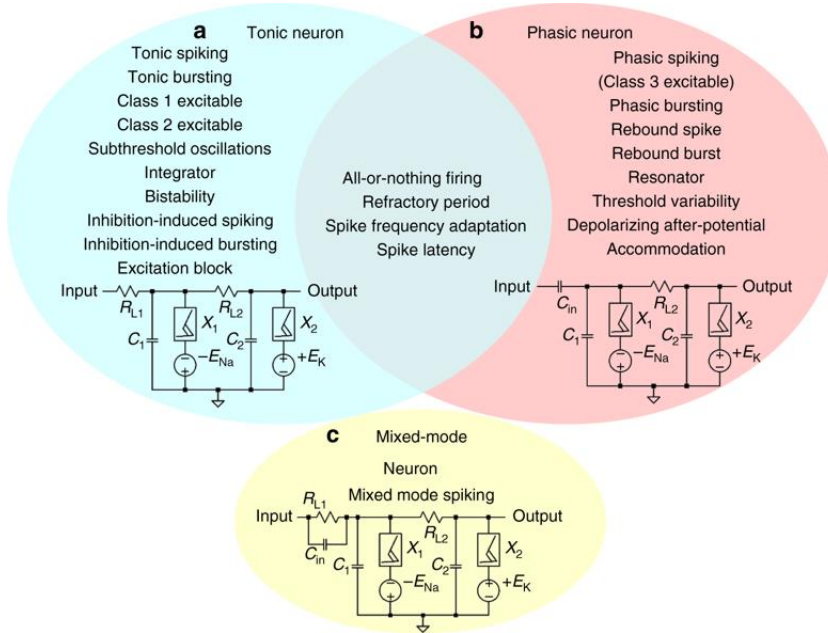
Figure 2.16 Three active memristor prototype neuron circuits and their experimentally demonstrated spiking behaviors. (a) Tonic excitatory neurons, with a resistive coupling to inputs. (b) Phasic excitatory neurons, with a capacitive coupling to inputs. (c) Mixed-mode neurons, with both resistive and capacitive couplings (R_{L1}, C_{in} in parallel) to inputs, show mixed-mode spiking behavior. The figure is reproduced from [29].

Various methods have been studied to induce synaptic behavior in VO$_2$ devices, including dynamically reversible chemical changes induced by ionic liquid (IL) gating to create oxygen vacancies[103], incorporation of dopants such as hydrogen[104] or Li-ion[105], or photochemically

induced structural transformations[75]. For example, non-volatile states with a retention time of several days[103] and short-term plasticity[106] can be achieved in an IL gated VO_2 devices. Although the realization of non-volatile memory can exploit the full potential of VO_2 in neuromorphic architectures, this thesis does not concentrate on non-volatile switching and synaptic behavior of VO_2.

2.5 Conclusion

In conclusion, this chapter has introduced some of the limitations and bottlenecks of current computing architecture, which includes the fundamental constraints of material physics, the limitations of shrinking device size, and the excessive data transfer between memory and logic units. These issues have emphasized the need for novel computing architectures, leading to the concept of neuromorphic computing, inspired by the human brain, one of the most powerful computing systems.

As a key building block, the memristor has been discussed, including its definition, development and switching characteristics. VO_2 has become a promising candidate due to its subtle structural transition leading to significant changes in electrical properties. The IMT of VO_2 has been discussed, while the driving force behind it is still under debate. It appears that lattice distortion and strong electron-electron correlation contribute to the IMT, though the order in which they occur remains unclear.

We have discussed the advancements made in utilizing the IMT of VO_2 for neuromorphic computing systems. On the one hand, it has been shown that VO_2-based switching elements exhibit nonlinear dynamics and can be integrated into circuits to create neural spiking behavior. On the other hand, it is possible to induce non-volatility through doping or gating, which allows for the implementation of synaptic behavior in VO_2. Therefore, the combination of VO_2-based artificial neurons with artificial synapses based on other materials or solely in VO_2 holds promise for achieving brain-like functionality.

Chapter 3.

Synthesis and characterization of VO$_2$ thin films

The experiments throughout this thesis are performed on devices which are fabricated from VO$_2$ thin films. This chapter focuses on the fabrication of VO$_2$ thin films by pulsed laser deposition and the subsequent characterization of the as-deposited films, including the examination of surface topography, chemical composition, crystal structures, and transport properties. The influence of substrate-induced strain is explored by depositing films with varying thickness and analyzing their evolution. The VO$_2$ films with a thickness below a critical value of 12 nm are preferred for further investigation of resistive switching devices.

3.1 Introduction

As introduced in Chapter 2, vanadium dioxide (VO$_2$) is a promising material for low-power oxide electronics and neuromorphic computing applications due to its insulator-metal transition (IMT) with significant resistivity changes of several orders of magnitude[16,19]. Pulsed laser deposition (PLD) is widely used to produce high-quality VO$_2$ thin films[107–109]. To utilize VO$_2$ thin films for resistive switching devices at room temperature, it is beneficial to slightly reduce the transition temperature of the IMT (T_{IMT}), which is ~340 K for bulk material. For this, one approach is by inducing strain in the films. The (001)-oriented TiO$_2$ substrates are chosen since they have the same crystal symmetry as the metallic phase of the VO$_2$ thin films but slightly larger lattice parameters, leading to the growth of tensile-strained films with lower T_{IMT} around 300 to 310 K[21,74,110].

This chapter focuses on the fabrication and characterization of VO$_2$ thin films on TiO$_2$ (001)-substrates by PLD. The films are characterized to determine their surface topography, chemical composition, structural properties, and electrical transport behaviors, using Atomic Force Microscopy (AFM), X-Ray Diffraction (XRD), X-Ray Photoelectron Spectroscopy (XPS), High-Resolution Scanning Transmission Electron Microscopy (HRSTEM), and Physical Properties Measurement System (PPMS), respectively. Furthermore, to study the relaxation of the strain in the films, the structural and electronic properties of VO$_2$ thin films with varying thicknesses are also investigated. The goal of this chapter is to identify ways to produce high-quality VO$_2$ thin films using PLD that are suitable for building resistive switching devices.

3.2 Pulsed laser deposition of VO$_2$ thin films

PLD is a deposition technique, using a high energy pulsed-laser beam to ablate material from a target, forming an energetic plasma plume towards a heated substrate where the particles settle and form a thin film[111,112]. PLD offers the benefits of enabling the transfer of stoichiometric ratios from a solid target to a substrate, as well as being capable of depositing complex oxides. Several parameters can be tuned to optimize the deposition process, for

example, laser frequency, laser spot size, substrate temperature, background pressure and gas composition.

All samples studied in this thesis were grown in the PLD-RHEED system at the University of Twente[113]. A photo of the system and a schematic of the simplified setup are shown in Figure 3.1.
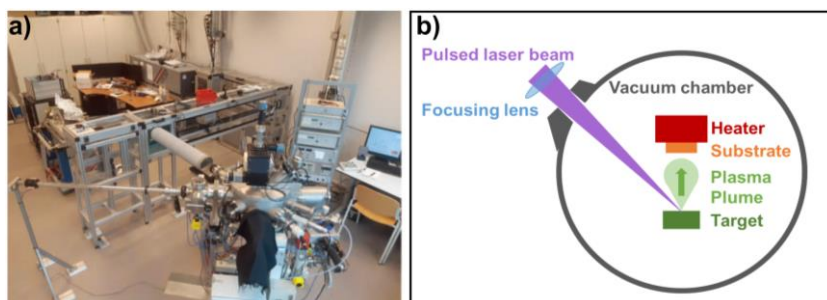

Figure 3.1 (a) Photograph of the PLD-RHEED setup at the University of Twente. The top of the image shows the LPX 200 KrF laser, from where the optical path in the middle of the photo feeds the light into the vacuum system at the bottom of the image. On the vacuum system, the load lock (left), CCD camera cloak (black, bottom), main turbo pump (right), and heater stage (top) are clearly visible. (b) Schematic overview of the vacuum chamber.

For the deposition of VO₂ thin films, $5 \times 5 \times 0.5$ mm³ (001)-oriented TiO₂ substrates (from CrysTec GmbH) were used. The substrates were first cleaned with isopropanol (IPA) or ethanol and then glued to the heater using silver paste. A polycrystalline V_2O_3 target[17] was placed opposite the substrate facing the heater. The distance between the target and sample was ~ 45 mm. Before the deposition, the chamber was filled with oxygen at a constant flow rate of 3.5 ml/min. To achieve a higher pressure of 3.2×10^{-2} mbar, the main valve to the turbo pump was closed and pumping was done through a narrow bypass valve. The deposition was performed with a KrF excimer laser (Plasma Physik LPX Pro 210, $\lambda = 248$ nm, 20 ns pulse duration) at a fluency of 1.3 J/cm² and a spotsize of 1.76 mm². The substrate was heated to 400 °C and the repetition rate was 10 Hz. After the deposition, the film was cooled down to room temperature at a rate of 10 °C/min in the vacuum chamber, while maintaining the same background oxygen pressure as used during deposition. The deposition parameters are summarized in Table 3.1. Unless otherwise stated, for the VO₂ film studied in this thesis, the

number of pulses was 4000, resulting in an approximate thickness of 11 nm. To obtain additional details on the methods used to determine the thickness, please refer to Appendix 3.A.

Parameter:	
Substrate temperature	400 $^{\circ}$C
Oxygen pressure	3.2×10^{-2} mbar
Laser fluence	1.3 J/cm^2
Laser spot size	1.76 mm^2
Spot aspect ratio	1:6.8
Laser repetition rate	10 Hz
Growth rate	~ 363.6 pulses/nm

Table 3.1 PLD growth parameters for VO$_2$ thin films

3.3 Characterization of VO$_2$ thin films

Topography and roughness were investigated by AFM (Bruker Icon) in a tapping mode. The epitaxial growth was observed by STEM (Thermo Scientific Spectra 300 at MESA+ NanoLab). The crystalline quality of the film was investigated by XRD (Panalytical X'pert XRD-MRD) at room temperature as well as higher temperatures. The chemical composition of the film was measured by XPS (Complex Oxide Materials COMAT System). The temperature-dependent electrical transport properties were measured by using van der Pauw geometry in the PPMS (DynaCool Quantum Design).

Figure 3.2 shows the AFM images of a cleaned TiO$_2$ (001) substrate and an as-deposited VO$_2$ film. On top of a smooth substrate (RMS roughness: 0.16 nm), the VO$_2$ film is homogenous with an RMS roughness of 0.65 nm.
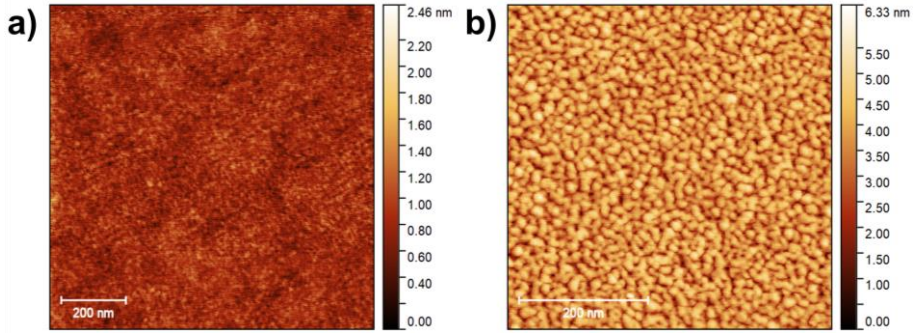
Figure 3.2 (a) Surface topography map of the TiO$_2$ (001) substrate. The image shows an area of 1×1 μm^2. (b) Surface topography map of the as-deposited VO$_2$ film with a thickness of about 11 nm. The image shows an area of 0.5×0.5 μm^2.
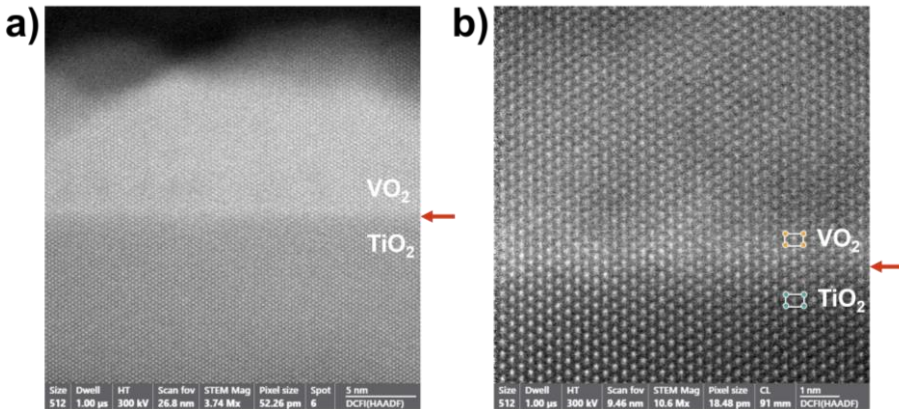
Figure 3.3 Cross-sectional view STEM-HAADF image of a VO$_2$ film on TiO$_2$ (001) substrate. (a) Overview image of the film. (b) Zoom-in view of the interface (indicated by red arrows on the right). Yellow and green circles denote V and Ti atoms, respectively, added for clarity.

The cross-sectional view of a VO$_2$ thin film can be observed in a high angle annular dark field image obtained with STEM (STEM-HAADF). The sample was prepared to be approximately 5 nm thin by focused ion beam (FIB). The images in Figure 3.3 indicate the high-quality epitaxial growth of the VO$_2$ film on top of the TiO$_2$ (001) substrate, as the VO$_2$ film continues the tetragonal atomic arrangement without any noticeable distortion or displacement.

For the XRD measurement, a 2θ-ω scan (Figure 3.4(a)) was performed to collect the diffraction peaks related to crystallographic planes parallel to the sample's surface, therefore pointing to the out-of-plane direction. There are two peaks in the spectra: one from the (001)-oriented TiO_2 substrate at ~ 62.75°, and the other from the rutile phase of VO_2 at ~ 65.70°[30,31]. The clearly resolved thickness fringes indicate the high film quality and the calculated thickness is ~ 11 nm. There are no other peaks in the range from 20° to 80°, which further confirms the epitaxy and phase purity of the VO_2 film.

To study the IMT of the VO_2 film, the temperature evolution of the first-order structural transition has been measured. Temperature-dependent XRD measurements were carried out under 298.15 K, 303.15 K, 313.15 K, 323.15 K, 333.15 K, 343.15 K, 353.15 K and 363.15 K, respectively, focusing on the VO_2 $(002)_R$ diffraction peak. As marked by the black arrow in Figure 3.4(b), the $(002)_R$ peak shifts from ~ 65.70° to ~ 65.55° when the temperature increases from 298.15 K to 363.15 K. The slight shift to a lower angle suggests the expansion of the out-of-plane lattice parameter but there is no obvious structural phase transition[110].
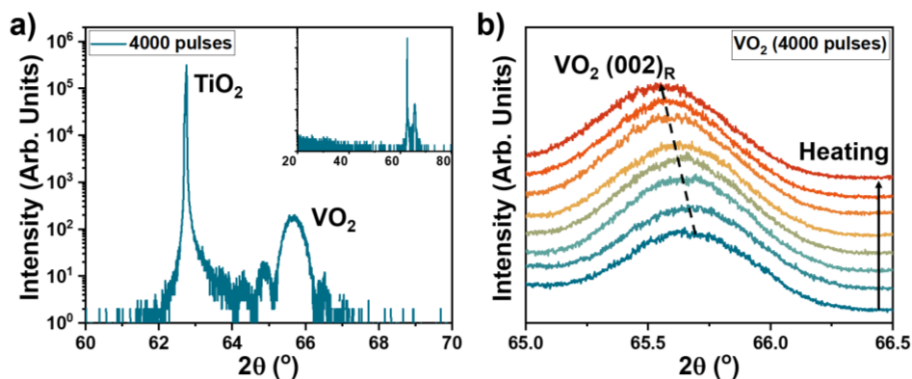

Figure 3.4 (a) XRD 2θ-ω scan of a VO_2 film grown on a TiO_2 (001) substrate in the range of 60° to 70°. The inset is the XDR pattern of the full range from 20° to 80°. (b) Temperature dependence of the VO_2 $(002)_R$ diffraction peak. XRD 2θ-ω scans were taken under 298.15 K, 303.15 K, 313.15 K, 323.15 K, 333.15 K, 343.15 K, 353.15 K and 363.15 K, respectively.
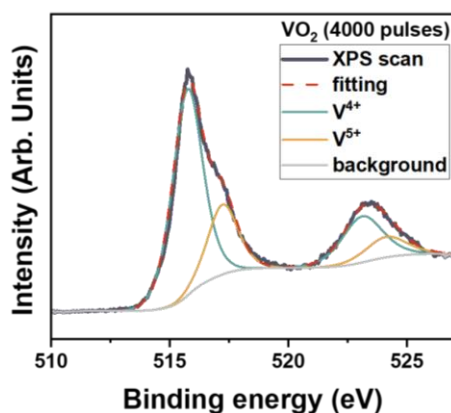
Figure 3.5 Vanadium V 2p core level XPS spectra of a VO₂ film. The measurement was done with the default settings of 12 mA emission current and anode voltage of 12.5 kV. Using CasaXPS software, the measured data (dark grey line) was fitted (red dashed line) and analyzed, after a Shirley background (light grey line) was subtracted.

Components	Binding energy	FWHM	Peak area
$V^{4+}2p_{3/2}$	515.75 eV	1.5 eV	74.7%
$V^{5+}2p_{3/2}$	517.23 eV	2 eV	25.3%

Table 3.2 XPS fit parameters for the V2p$_{3/2}$ signals of a VO₂ thin film.

As discussed in Chapter 2, there are various possible oxidation states of the V cation. In order to determine the oxidation state in the film, we carried out an *ex-situ* measurement and analysis of the V 2p core level XPS spectra, with the C 1s level (285.0 eV) chosen as the reference peak for fitting. The binding energy (BE) of the V 2p level increases with the oxidation state of the V cation, and the V 2p further is split into V 2$p_{3/2}$ and V 2$p_{1/2}$ for each oxidation state due to the spin-orbit splitting[114,115]. As shown in Figure 3.5 and summarized in Table 3.2, the 2$p_{3/2}$ peak is contributed by the V^{+4} and V^{+5} at 515.75 eV and 517.23 eV, respectively. It is indicated that the surface of the film comprises a mixture of 74.7% VO₂ and 25.3% V₂O₅. It is worth noting that the film surface can be easily oxidized in contact with air, and fully oxidized V^{5+} species are commonly found at the surface of vanadium oxide materials.
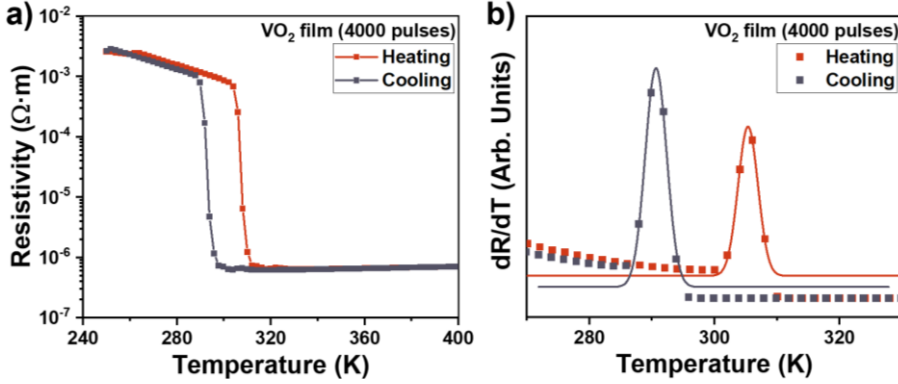
Figure 3.6 (a) Temperature dependence of the resistivity of a VO$_2$ thin film, exhibiting the IMT. (b) The numerical derivative of the resistivity (dR/dT) as a function of temperature of the heating and cooling processes. The data are fitted using Gaussian functions.

The resistivity of the VO$_2$ thin films was measured using a van der Pauw geometry in the range from 250 K to 400 K. The hysteresis loop in Figure 3.6(a) shows that the VO$_2$ film undergoes a sharp transition with a 3-orders-of-magnitude change in resistivity. Figure 3.6(b) is the calculated numerical derivative of the resistivity (dR/dT) with respect to temperature for both the heating and cooling cycle. Fitting the data points with a Gaussian function, the transition temperature is 305 K for the heating branch and 291 K for the cooling branch. T_{IMT} is much lower than the one for bulk VO$_2$ ($\sim$ 340 K) due to the epitaxial strain, revealed by the reduced c-axis of the epitaxial VO$_2$ thin film on TiO$_2$ (001)[80,116]. Within the hysteresis span ($\sim$ 14 K), the coexistence of both the metallic and insulating phases results in intermediate resistive states[77,78]. The intermediate resistive states can be stabilized by tuning the temperature during the sweep before reaching the complete transition for both heating and cooling process[30,31]. These minor loops within the hysteresis span are similar to the mathematical Preisach model of hysteresis[117], which is normally used for ferromagnetic and ferroelectric material systems.

The IMT is normally accompanied by a structural transformation from an insulating monoclinic (M1, P2$_1$/c) phase to a metallic rutile (R, P4$_2$/mnm) phase, as well as the dimerization of neighboring vanadium atoms[79]. However, in this thesis, the 11-nm VO$_2$ film is fully strained in the rutile phase at room temperature. The IMT happens while the

temperature increases without an obvious crystallographic phase transition according to the temperature-dependent XRD results (Figure 3.4(b)), which suggests the IMT can be a purely electronic phase transition. It is also reported that the IMT in strained VO$_2$ films can result from electronic softening of Coulomb correlations within V-V singlet dimers happening at a lower temperature compared to the T_{IMT}[79].

3.4 Strain relaxation in VO₂ films

As the XRD patterns indicated, the epitaxial 11-nm VO$_2$ thin film on TiO$_2$ (001) substrate is fully strained in the rutile phase. The lattice parameters of tetragonal TiO$_2$ are $a = b = 4.5933$ Å and $c = 2.9592$ Å[80]. Compared to the tetragonal lattice parameters of VO$_2$ as given in Chapter 2 there is only a small lattice mismatch between the two materials of 0.863% along a and b and 3.62% along c. Therefore, the substrate-induced tensile strain in the (001) plane along the crystallographic [100] and the [010] axes favors the rutile phase VO$_2$ for the coherent growth, reducing the IMT transition temperature. However, when the film becomes thicker than ~ 15 nm, the strain starts to be relaxed[110]. In order to study the relaxation manner, three additional VO$_2$ films were grown using the same PLD conditions, but with varying numbers of laser pulses: 8000, 12000, and 16000, resulting in a thickness of 22 nm, 33 nm and 44 nm. Together with the 11-nm film, the surface morphology, crystal structure and IMT property were investigated and compared.

The AFM images in Figure 3.7 show that the surface topography changes while the thickness of the film increases. The 11-nm film is smooth and continuous. As the thickness of the films increases, they become rougher in texture, with the RMS roughness increasing from 0.65 nm for the 11-nm film to 0.75 nm for the 22-nm film, and up to 1.62 nm for the 44-nm film. Additionally, there are patterns in the form of strips that are present in the 33-nm film, which then progress into straight cracks that create rectangular tiles in the 44-nm film. The corresponding line-scan profiles 1 and 2 plotted in Figure 3.7(e) and (f) show the development of the surface protrusions on either side of cracks, growing from 2 nm to 6 nm in height and 0.2 μm to 1 μm in width.
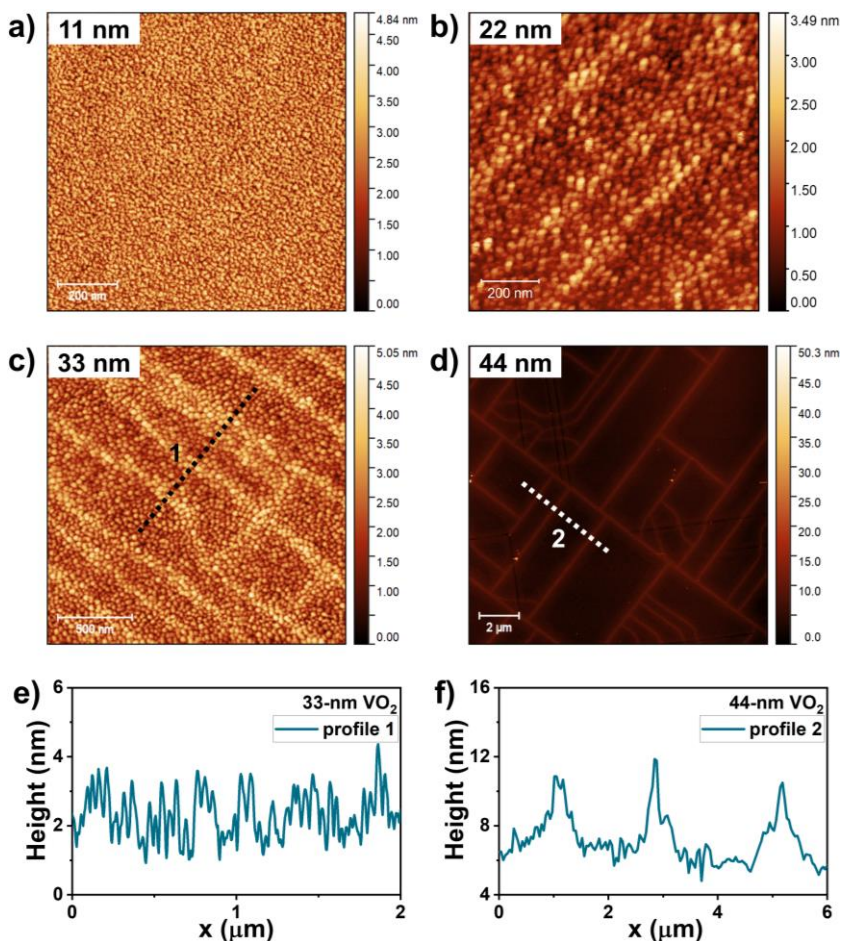
Figure 3.7 Surface topography map of (a) 11-nm, (b) 22-nm, (c) 33-nm and (d) 44-nm VO_2 film. (e) Height profile of the black dashed line in (c). (f) Height profile of the white dashed line in (d).

Figure 3.8(a) shows XRD patterns that exhibit both the TiO_2 (001) diffraction peak and the VO_2 peak. The patterns reveal that films with a thickness of up to 33 nm are composed entirely of rutile VO_2. Additionally, there are indications of diminished film quality and heightened c-axis orientation, evidenced by the absence of fringes and a shift of the peak towards lower angles. Conversely, the 44-nm film displays the simultaneous presence of $(002)_R$ and $(-402)_{M1}$ peaks, indicating that there is a coexistence of rutile and monoclinic phases.

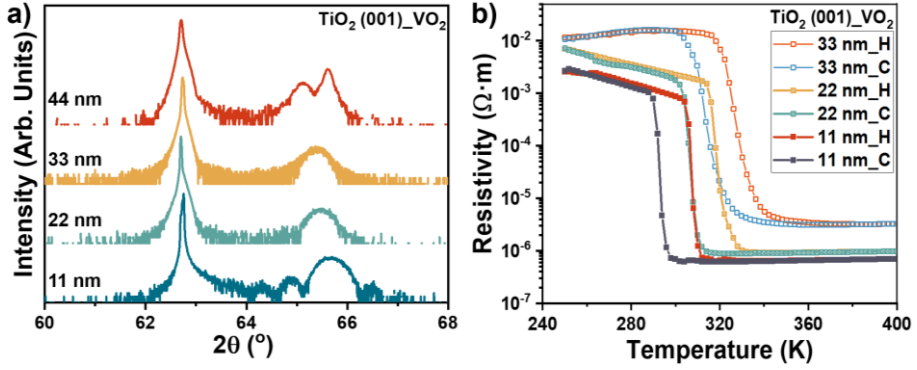**Figure 3.8** (a) XRD 2θ-ω scan of the VO₂ films of different thicknesses in the range of 60° to 68°. (b) Temperature dependence of the resistivity of the VO₂ films of different thicknesses.

Measurements of the resistivity of films as a function of temperature were conducted for films with thicknesses of 11 nm, 22 nm, and 33 nm. Figure 3.8(b) illustrates that the resistivity and T_{IMT} rise in correlation with the film thickness. Although measurements were not performed on the 44-nm film in this study, it is expected that both the resistivity and T_{IMT} will increase significantly due to the emergence of the insulating monoclinic phase.

The results above suggest that the epitaxial strain imposed by the TiO₂ (001) substrate on the VO₂ film will be relaxed with increasing film thickness. This relaxation process occurs via the emergence of cracks. Rodríguez et al. reported that the cracks are aligned with the $<110>_R$ crystallographic directions. The material adjacent to the crack is in monoclinic phase while the square framed by the cracks remains rutile, resulting in individual rectangular rutile VO₂ domains[110]. Although using spontaneous cracks to encompass rutile VO₂ domains is an attractive concept, it is not pursued in this thesis. The preferred VO₂ films for this thesis are those having a thickness less than a critical value of 12 nm[118], being in the rutile phase, and exhibiting lower T_{IMT}.

3.5 Conclusion

VO$_2$ thin films were successfully grown on (001)-oriented TiO$_2$ substrates by PLD using V$_2$O$_3$ as the target. The sufficiently small mismatch between the rutile TiO$_2$ and the metallic phase of VO$_2$ leads to the coherent growth of fully strained thin films. As a result, the 11-nm VO$_2$ films are in rutile phase and exhibit the IMT at a much lower temperature of 305K compared to bulk VO$_2$ (~340 K). However, with increasing film thickness, the substrate-induced tensile strain starts to relax, resulting in a rougher surface texture and ultimately leading to the appearance of monoclinic-phase cracks. Thicker films show coexistence of monoclinic and rutile phases, and higher IMT temperatures. In conclusion, the thinner strained films with transition temperatures near room temperature provide a promising platform for resistive switching devices which are studied in the remainder of the thesis.

Appendix 3.A Determining the thickness

In the main text, the thicknesses of films deposited with different laser pulse numbers are given. They are determined mainly in two ways.

For smooth films, the thickness can be determined by X-ray reflectivity (XRR) measurements. During XRR scans, the source and detector move symmetrically around the lattice plane of the sample, where 2θ is kept at small values, mostly below 5°. Assuming a substrate with one thin film, when the X-rays are focused on the sample under grazing angles, a part is reflected at the surface of the sample and another part is transmitted and travels into the thin film, see Figure 3.A.1. At the next interface of the substrate and film the X-rays are partly reflected and partly transmitted again. These reflected X-rays travel in the opposite direction and approach the surface of the film from the bottom. Again, a part of the X-rays is reflected, and the other part is transmitted. The refracted X-rays interfere with ones that were reflected in first instance. When the phase difference (Δ) between the refracted and reflected X-rays is equal to an integer time the wavelength, a maximum in the intensity is observed. The process repeats and the X-rays also interfere with X-rays that travelled multiple times up and down in the thin film. A pattern of oscillations, so called called Kiessig fringes, is created which is detected by the detector[119,120]. The density, roughness and thickness can be determined by fitting the observed oscillations using the X'Pert Reflectivity software.
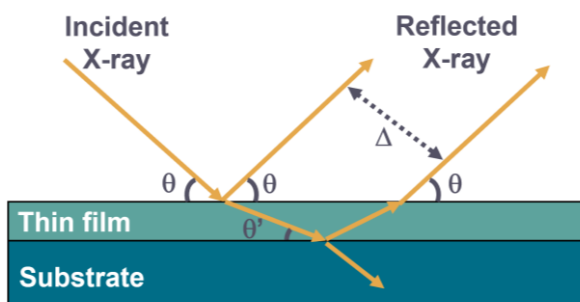

Figure 3.A.1 Schematic representation of an XRR scan. The X-rays arrive at the surface under an incident angle, θ. A part of the beam transmits into the thin film, the other part gets reflected.

For the film grown with 4000 pulses, an XRR measurement was performed using the Panalytical X'pert XRD-MRD system. The experimental data and the fitting of the XRR scan is presented in Figure 3.A.2(a). From the fitting a thickness of 11 nm is observed.

Films that are deposited using a higher number of laser pulses result in a surface that is excessively rough for conducting XRR measurements. Therefore, it is necessary to remove part of the film to locally expose the substrate. Then the step height from the substrate to the top of the film can be measured by AFM. An example is shown in Figure 3.A.2(b) where we etched the edge of the film deposited with 8000 pulses using 35% mass fraction nitric acid. The measured step height is approximately 22 nm.
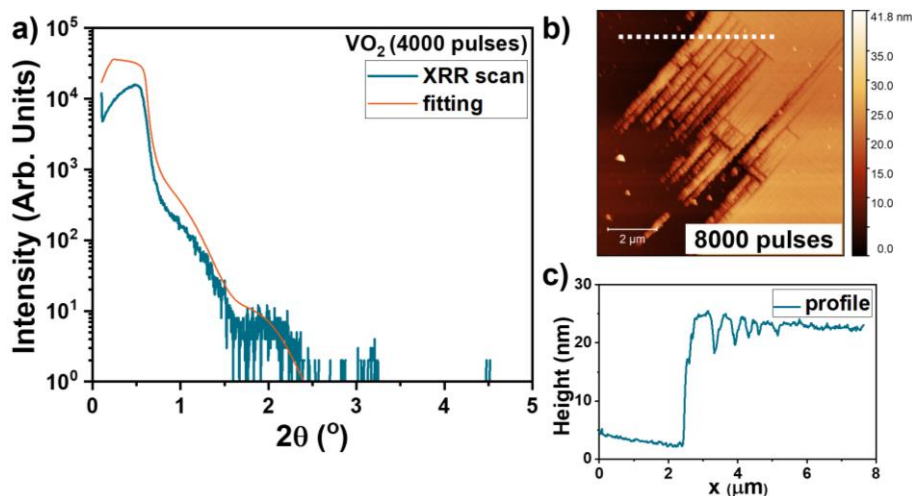

Figure 3.A.2 (a) XRR scan of the 4000-pulse VO$_2$ film in the range of 0.5° to 5°. The green curve shows the experimental data. The red curve shows the thickness fitting using the X'Pert Reflectivity software. (b) Surface topography map of an 8000-pulse VO$_2$ film after wet etching. (c) Height profile of the white dashed line in (b) indicating a thickness of 22 nm.

Chapter 4.

Multi-level operation in VO$_2$ single-bridge devices

The substrate-induced strain makes the VO$_2$ thin film exhibit an insulator-metal transition near room temperature, providing potential for applications in novel memristive devices and brain-inspired neuromorphic computing. In this chapter, two-terminal single-bridge devices and their reproducible switching behaviors are reported. Resistive switching can be achieved by applying electrical bias, which creates Joule heating in the device and triggers the transition. Controllable switching behavior is demonstrated between multiple resistance levels over several orders of magnitude, allowing for multibit operation.[1] The influence of fabrication techniques on the switching behavior is also discussed. Overall, these findings provide a solid foundation for further exploration on devices with complex configurations such as multi-bridges, as will be the topic of Chapter 5 and Chapter 6.

4.1 Introduction

In the previous chapter, the film growth of VO_2 using PLD has been discussed. The substrate-induced strain reduces the T_{IMT}, which facilitates it to be triggered with external electrical stimuli at room-temperature operation. For example, in previous work of our group, Rana et al. observed multiple stable resistive states between the insulating and metallic states in VO_2 films by tailored temperature sweeps or external electrical stimuli[31], following earlier work by e.g., Driscoll et al.[121]. The coexistence of both the metallic and insulating phases within the hysteresis span of the IMT results in intermediate resistive states[78]. The existence of the intermediate resistive states is quite unique and particularly attractive for reconfigurable electronic circuitry.

In this chapter, we investigated the resistive switching behavior and realized multi-states in the defined devices, scaling them down to microscale bridges from the whole film. By applying voltage sweeps, which create Joule heating in the device and triggers the IMT, repeatable switching behavior with a correlation between the switching power and device dimensions is observed. It shows a combination of digital- and analog-like switching[55] and the reset happens gradually with steps, resulting in stable intermediate resistive states between the HRS and LRS. By tuning the applied voltage bias, multistate memory within one VO_2-based memory cell (in our demonstration 3 bits per cell) and reliable multilevel operation is achieved. Additionally, the impact of different etching techniques on device topography, temperature-dependent IMT, and resistive switching features is investigated to determine a reliable method for future fabrication and exploration.

4.2 Device design and fabrication

In this thesis, to utilize the substrate-induced strain, we focus on the two-terminal planar device. The design consideration is to create bridges with varying dimensions from the VO$_2$ film and two contact pads for each device to perform electrical measurements.

Figure 4.1 The schematic designs of VO$_2$-based single bridge device (top view) with (a) straight bridge and square electrode pads, and (b) straight bridge and narrower contact close to the bridge. The width, W, and length, L, of the devices are labeled.

Figure 4.1 shows two designs of single-bridge devices, of which Figure 4.1(a) represents the typical geometry mostly employed in this thesis. The device length, denoted by L in the figure, represents the spacing between the contact pads and ranges from 10 μm to 50 μm. To allow for some misalignment, the VO$_2$ bridges are fabricated longer than L and extend under the gold contacts. The bridge width, represented by W, is 5 μm. The size of the electrodes is 150 μm×80 μm. In addition to the square electrodes, pads with narrower contacts closer to the bridges are designed (Figure 4.1(b)). However practical measurements show these devices are more likely to burn out than the ones with square electrodes, possibly because of the higher current density and contact resistance at the interface of the VO$_2$ bridge and electrode, resulting in increased Joule heating. Thus, the design shown in Figure 4.1(a) is preferred for this thesis and used unless otherwise mentioned.

Figure 4.2 summarizes the general process flow of the fabrication. The fabrication of bridge devices from as-deposited VO$_2$ films involves two primary steps: etching the film to form the desired structures and depositing metal contacts, along with the lithography process. To shape the films in the desired structures, an Ultraviolet (UV) lithography process was used. Positive OLIN 907-12 photoresist was spincoated on top of the sample at 6000 rpm for 45 s and successively baked for 1 min on a hot plate at 100 °C. The sample was then placed in a Suss

MA56 mask aligner and aligned with a designed UV lithography mask. Exposure was done by the UV light with $\lambda = 365$ nm at 10 mW/cm^2 for 7 s. The illuminated parts of the resist were dissolved in OPD4262 developer, after which the development was stopped by soaking the sample in deionized (DI) water twice for 30 s. The sample was dried with a nitrogen gun before further processing.
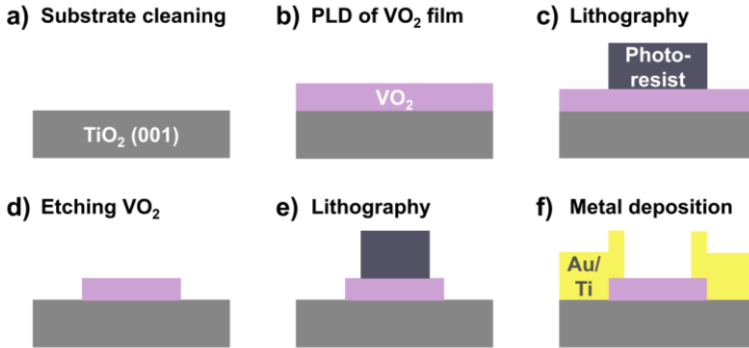

Figure 4.2 Fabrication process of the VO$_2$ single-bridge device (side view). The as-deposited VO$_2$ film is etched by Ar ion beam etching or a diluted nitric acid solution into single bridge structures and the Au electrodes are deposited using sputtering. Lithography is used for the patterns.

Etching the unwanted parts of the VO$_2$ film and maintaining the bridge structures can be done by either wet etching or Ar ion milling. Wet etching typically involves a diluted nitric acid solution[122]. To prepare the etchant, the 69% mass fraction HNO$_3$ was diluted in a 1:1 volume ratio with DI water. The sample was put in the acid for 30 s and then soaked in the DI water for 1 minute to stop the etching. Wet etching can typically remove the 11-nm films, but it can sometimes result in over etching. In contrast, Ar ion milling is more controllable and reproducible. It was done in an Ar ion etcher with the settings listed in Table 4.1. The Ar ions, whose energies are determined by the beam voltage, were generated by a discharge voltage between cathode and anode. They were accelerated towards the sample by an accelerator voltage, and before hitting the sample, their charge was compensated by a neutralizer filament. The sample surface was at an angle of 45° to the ion beam. The sample stage was cooled by cooling water and rotated at 4 rpm during the process. After 3 minutes of etching, 11 nm of the VO$_2$ plus 2 ~ 3 nm of the TiO$_2$ substrate has been etched away.

Parameter:	
Background pressure	4×10^{-4} mbar
Ion beam dose[2]	2.58×10^{15} ions/cm^2
Beam voltage	500 V
Beam current	50 mA
Etching angle	45º
Stage rotation speed	4 rpm
Etching time	3 min

Table 4.1 Ar ion milling parameters for VO$_2$ bridge devices.

The final step is to deposit the metal contacts using RF sputtering (Perkin-Elmer model 2400). The process pressure of the chamber was 2×10^{-2} mbar. After pre-sputtering of a Ti target to clean its oxidized surface, a 5-nm layer of Ti was deposited first as an adhesion layer, followed by the deposition of a 50-nm Au layer. The parameters are listed in Table 4.2. After sputtering, the lift-off of the electrodes was done in an acetone bath overnight to remove the unexposed photoresist and the metal layers on top of it.

Process	RF power	Self bias	Time
Ti clean	250 W	-900 V	2 min
Ti deposition	150 W	-700 V	1 min
Au deposition	500 V	-900 V	3 min

Table 4.2 Sputtering parameters for VO$_2$ bridge devices.

Figure 4.3 shows the outcome of the fabrication process. A wet-etched device with $W = 5$ μm and $L = 15$ μm, following the design presented in Figure 4.1(a), is shown as an example. The

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[2] The ion beam dose is defined as the density of Ar ion per square centimeter. This value is obtained by dividing the beam current multiplied by Coulombs by the surface area of the beam. The diameter of the beam in the Ar etcher is 11 cm.

device was observed by optical microscopy and scanning electron microscopy (SEM), which shows the bridge structure has been effectively etched. This has been further validated by AFM, which reveals that the height of the VO$_2$ bridge is approximately 12 nm.
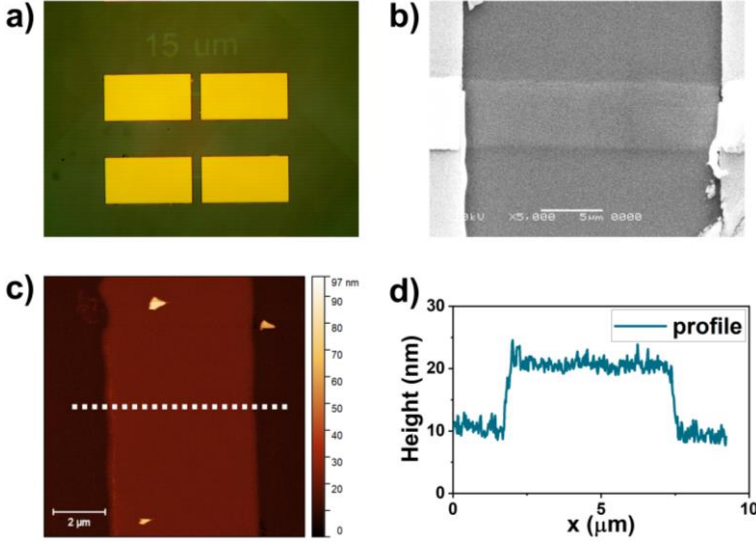

Figure 4.3 The as-fabricated VO$_2$ single-bridge ($W = 5$ µm, $L = 15$ µm). (a) Optical photo under a microscope. (b) SEM image. (c) Surface topography map of the VO$_2$ single bridge. (d) Height profile of the white dashed line in (c).

4.3 Electrical characterization

4.3.1 Electrical characterization setup

The electrical characterization of the VO$_2$-based resistive switching devices was performed in a Janis cryogenic probe station with a Keithley 4200A-SCS parameter analyzer. The stage of the probe station can be heated up to 375 K. Most of the measurements in this thesis were done at room temperature (295 K) unless otherwise stated.

Figure 4.4(a) shows the schematic circuit design of the equipment. Using gold-plated tungsten needles, one terminal of the device under test (DUT) was connected to the source measurement unit (SMU) 4200 whereas the other terminal was grounded. The SMU is essentially a voltage or current source in series with a current meter, connected in parallel

with a voltage meter. It can simultaneously source a voltage and measure the current, or source a current and measure simultaneously the voltage. The source range is up to $\pm$ 210 V and $\pm$ 100 mA with a high current resolution of 100 fA (without preamplifier) or 100 aA (with preamplifier). Normally, during measurements, a fixed sense range of the current (with a maximum 10 mA) was used to avoid voltage spikes during internal change of measurement range by the SMU (that appear each decade of current). Moreover, a programmed compliance was used to prevent damaging the device in events of highly nonlinear *I-V* characteristics such as forming and switching. Since the current compliance has got an intrinsic delay time in a microsecond regime, short but significant current overshoots are to be expected.
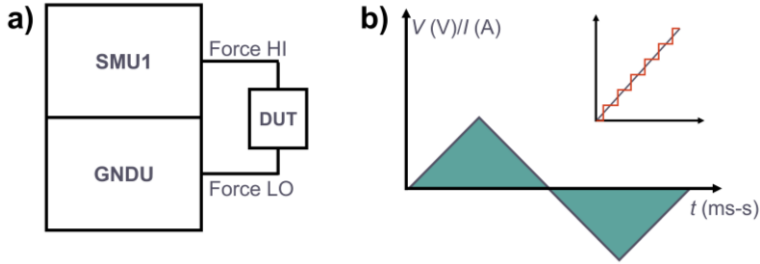

Figure 4.4 (a) Schematic circuit design for electrical measurements with a Keithley 4200 source measurement unit. (b) Time dependence of quasi-static voltage/current sweeps. Inset: Voltage/Current step function in detail.

The electrically induced IMT of VO$_2$ bridges and their switching features were investigated by quasi-static sweeps (Figure 4.4(b)). In this chapter, voltage-controlled measurements are mostly used, whereas in later chapters the current-controlled ones provide more information on the switching dynamics. Generally, an electrical measurement can be regarded as quasi-static if electrical (and thermal) mechanisms equilibrate on a much faster time scale than the time span of the voltage/current steps, which is valid for the present time scale of the steps. By using a low step size, the step function can be approximated as a quasi-continuous sweep. The measurements presented below were typically conducted with step sizes of 50 mV, although they can be adjusted based on the measurement range.

4.3.2   Resistive switching behavior of VO$_2$ single-bridge devices

Figure 4.5 shows the results of the electrical characterization of VO$_2$ single-bridge devices, mainly the voltage-controlled *I-V* curves. All the measured devices show typical volatile switching behavior, as the VO$_2$ bridges spontaneously return from the LRS to the HRS after the removal of the applied voltage. For the set process, the current of the device increases abruptly when the applied voltage surpasses the threshold value (V_s). For the reset process, the current first drops gradually with a decreasing applied voltage, followed by a sudden drop when the applied voltage is smaller than the hold voltage (V_h). So, within one VO$_2$ bridge, there are both fast digital switching and continuous analog-like switching features, which provides possibilities to control the resistive states.

As shown in Figure 4.5(a), the device requires more voltage and power to switch for the first cycle than all the subsequent cycles. This forming process leads to a decrease of the HRS, making the device easier to switch with lower power. All other resistive switching characteristics reported later were measured after the forming cycle. The effect of this forming will be discussed in Section 4.3.3. Figure 4.5(b) shows the *I-V* curve of the voltage sweeps for both positive and negative bias. The symmetrical curve indicates the switching is independent of bias polarity, as expected from a Joule heating-based mechanism. A current compliance (I_{CC}) should be set to protect the devices. It plays an important role in the switching behavior and the control of resistive states since it maximizes the Joule heating generated inside the VO$_2$ bridges. Therefore, the *I-V* characteristics have been measured with different applied I_{CC} (Figure 4.5(c)). Surprisingly, an intermediate step occurs during the reset process when a higher I_{CC} is used. Also, it is shown in Figure 4.5(d) that this behavior is repeatable and stable for up to 100 cycles. It indicates that there are intermediate states between the LRS and HRS and it is possible to stabilize them by tuning the applied voltage and the current compliance.
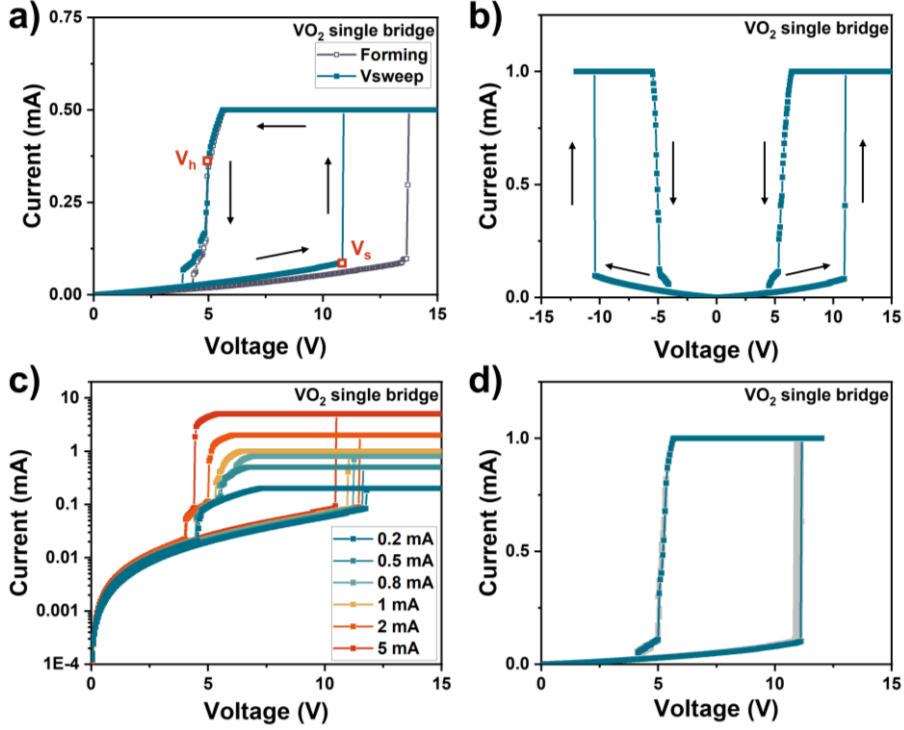
Figure 4.5 Electrical characterization of a VO$_2$-based single-bridge device (W = 5 μm, L = 20 μm). (a) *I-V* characteristics including the forming cycle. I_{CC} = 0.5 mA. The terminology of set voltage (V_s) and hold voltage (V_h) are indicated in (a). (b) *I-V* characteristics in the positive and negative bias. I_{CC} = 1 mA. (c) *I-V* characteristics with varying I_{CC} ranging from 0.2 mA up to 5 mA. The plots are in logarithmic scale for the *y*-axis. (d) *I-V* characteristics for 100 cycles. I_{CC} = 1 mA, the forming step is not shown here.

The correlation between the switching parameters and device length are displayed in Figure 4.6. The set voltage and power both scale with device length. Shorter devices require a lower voltage and power to switch since they have lower resistance and more Joule heating at a given voltage. Also, for longer devices, the window between set and hold is wider. To be noted that P_h is larger than P_s, as P_h is defined at the point when the device is switched from the LRS to the intermediate state, rather than when it is switched back to the HRS.
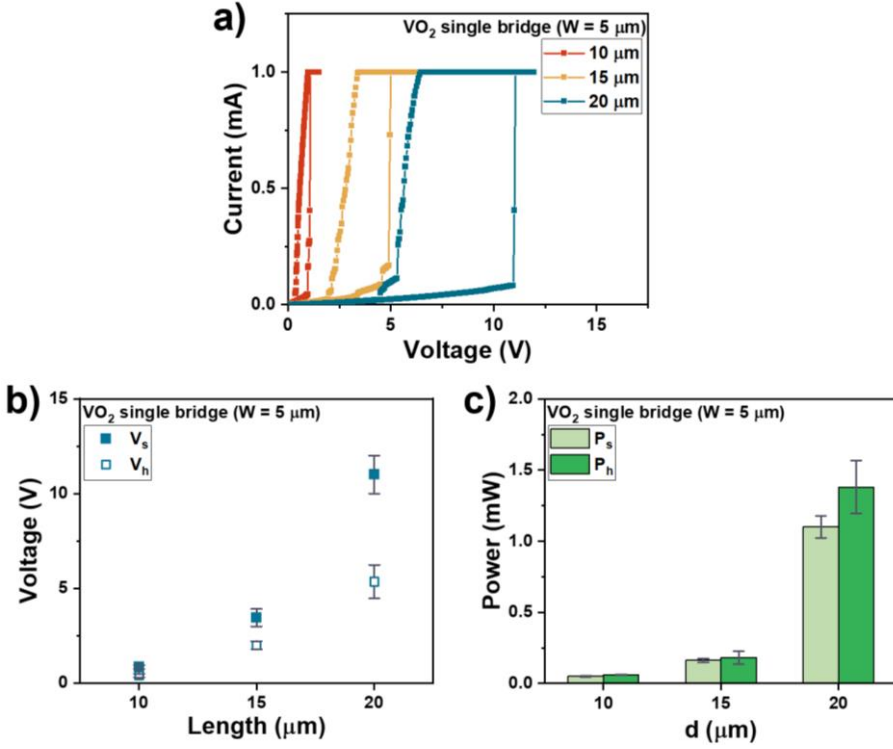
Figure 4.6 (a) *I-V* characteristics of three VO$_2$-based single bridge devices (W = 5 µm) with different bridge lengths. I_{CC} = 1 mA. (b) Set voltage (V_s) and hold voltage (V_h) as a function of the device length (c) Calculated set power (P_s) and hold power (P_h) as a function of length for these devices.

To map out the hysteresis loops for different intermediate resistive states, voltage segment-sweeps were performed. The philosophy is to locate the intermediate resistive states using several intermediate voltages (V_{inter}). The sweep function can be seen in Figure 4.7(a). The voltage is swept from 0 V to the maximum value (V_{max}) and then is swept back and turned at V_{inter} to return to V_{max}, and finally swept all the way back to 0 V. The results are plotted in Figure 4.7(b), showing that multiple resistance states can be achieved when voltage sweeps are reversed at different intermediate voltages during the reset process. Similar to the temperature-dependent measurements reported by Rana et al., the hysteresis loop contains several tunable intermediate resistive states[31].
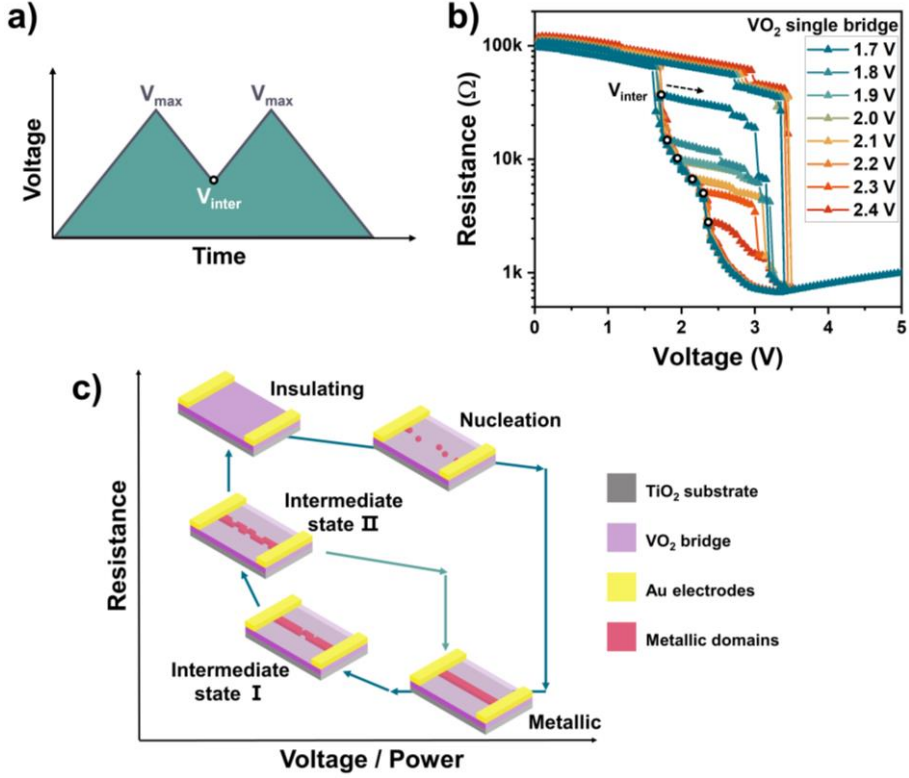
Figure 4.7 (a) The applied voltage during segment-sweep measurements as a function of time. (b) Device resistance as a function of the voltage for the VO$_2$-based single-bridge device during segment-sweeps. $I_{CC} = 5$ mA. The turning points at V_{inter} are indicated by the opened black dots. (c) Suggested schematics of the filament formation in VO$_2$-based single-bridge devices, displayed in the device resistance versus voltage/power curves. The schematics show the status of the filament in the VO$_2$ bridge under different conditions, including the insulating state, the nucleation phase, the metallic state, and two intermediate resistive states (I and II).

The switching mechanism of the VO$_2$-based resistive switching devices has been discussed in Chapter 2, which is based on the conducting filament formation triggered by Joule heating. The set process is on a time scale of nanoseconds[25], while the reset is on a time scale of milliseconds[26]. During the reset process, the metallic domains inside the filament relax to the insulating state at different speeds due to inhomogeneity[26,92]. The filament becomes partially metallic and partially insulating and this intermediate state can be held with a small external stimulus since the residual metallic domains can attract the current and maintain the IMT. When the device is set to different intermediate resistive states, the ratio between the metallic

domains and insulating domains is being tuned. Figure 4.7(c) schematically shows the suggested filament status for the whole process of nucleation, formation, partial retention, and rupture. There are two intermediate states shown, intermediate state I with more metallic domains and intermediate state II with fewer metallic residues. To switch from I to II, the applied voltage can be decreased so that the metallic domains that remained will further become insulating. However, switching from II to I requires the device to be fully set again and then the applied voltage can be decreased to the right value. If the applied voltage simply increases, the device will undergo the complete IMT with a lower power instead of going to a lower intermediate resistive state since the filament formation is ultrafast.
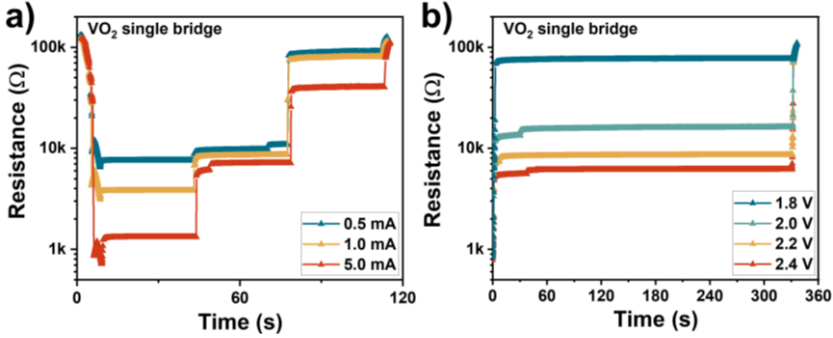

Figure 4.8 (a) Different resistance states obtained for three different applied voltage values (2, 2.5 and 2.8 V) in a VO$_2$-based single-bridge device ($W = 5$ μm, $L = 15$ μm) for three different values of I_{CC}. (b) Time evolution of the resistance of the same device as in (a) under four different applied voltage values after an initial IMT step. The voltage was held for 5 min. $I_{CC} = 1$ mA.

In addition to voltage sweeps, static voltages have also been applied during the reset process to study the stability over time of these intermediate states. For this, the device is first set to the LRS, then the voltage is swept back and maintained steady at a certain intermediate value (2, 2.5 or 2.8 V in Figure 4.8(a)). As can be seen in Figure 4.8(a), varying intermediate resistive states are stabilized. Moreover, the current compliance is still important to control the resistance value of the intermediate state. With a lower I_{CC} (like < 0.5 mA), the LRS is still fairly high, and the controllable range of resistive states is correspondingly small. However, with a higher I_{CC} (like > 5 mA), the LRS is very low which raises the risk for

irreversible breakdown of the device. Therefore, it is better to pick a medium value, such as 1 mA, as in done in the following measurements. To check the stability of the intermediate resistive states, the static intermediate voltages have been held for over 5 min (Figure 4.8(b)), without a noticeable change of resistance after some initial stabilization.

Figure 4.9(a) and (b) shows that within one VO$_2$-based memory cell, straightforwardly over 8 separable levels of states could be achieved, corresponding to 3 bits per cell. The intermediate levels spread in a 1-order-of-magnitude range, and they are reproducible and repeatable. In Figure 4.9(a) the states are accessed in consecutive ascending order, from lower resistive states to higher ones, while Figure 4.9(b) shows the reverse process from higher resistive states to lower ones.
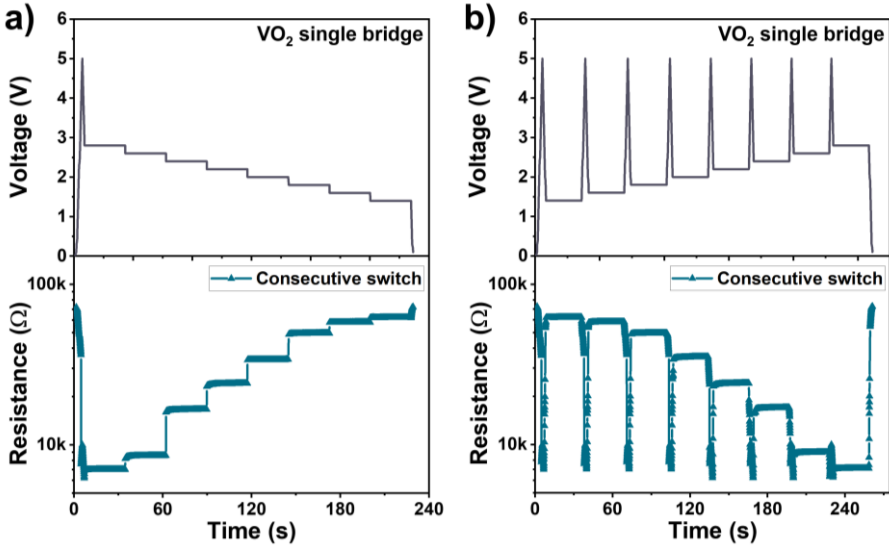
Figure 4.9 Multilevel operation of a VO$_2$-based single-bridge device ($W = 5$ μm, $L = 15$ μm). Eight distinguishable states are accessible in (a) consecutive ascending order or (b) consecutive descending order by adjusting the intermediate voltage value. The upper panels show the applied voltage plotted as a function of time and lower panels are the resistance as a function of time. $I_{CC} = 1$ mA.

Moreover, as shown in Figure 4.10, the individual intermediate states can be reached independently and randomly. When accessing the states in consecutive descending order, under voltage-bias, the device is first set to the LRS before the resistance is fixed on the return to the lower intermediate resistance states. This is because set processes to the low resistance states are too abrupt to stabilize under voltage bias.
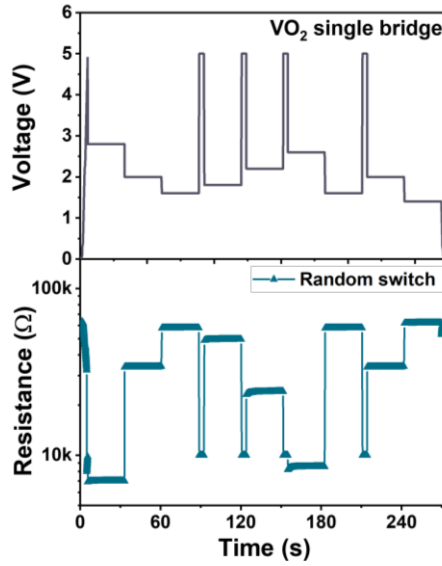

Figure 4.10 Multilevel operation of a VO$_2$-based single-bridge device ($W = 5$ μm, $L = 15$ μm). Eight distinguishable states can be independently reached. The upper panels show the applied voltage plotted as a function of time and lower panels are the resistance as a function of time. $I_{CC} = 1$ mA.

4.3.3   Effect of different etching techniques on VO$_2$ bridges

The previous section shows the promising data of VO$_2$ single-bridge devices fabricated via wet etching. However, subsequent experiments have revealed that the wet etching process can be challenging to control and may occasionally result in over-etching. To fully harness the potential of VO$_2$ bridges, it is essential to understand how different etching techniques affect their properties, especially the IMT and resistive switching features.
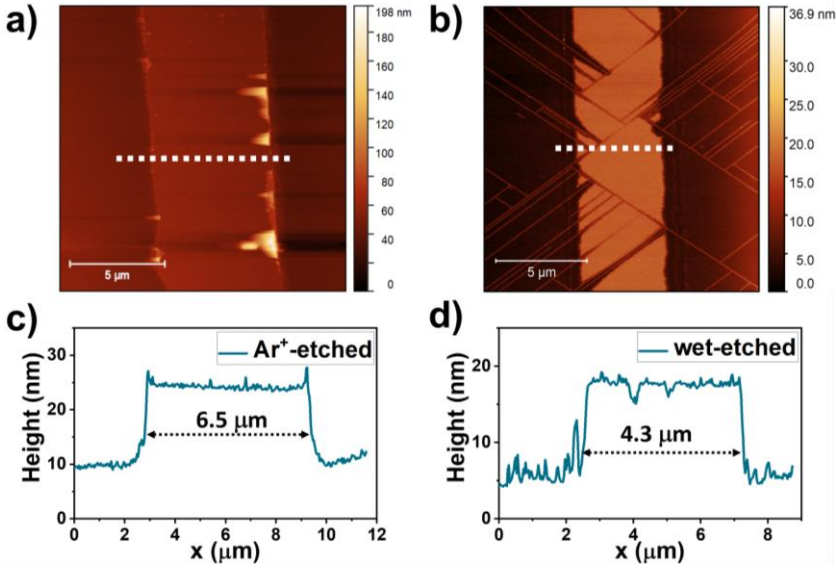
Figure 4.11 Surface topography map of VO$_2$ bridges using different etching techniques: (a) Ar ion milling and (b) wet etching. (c) (d) Height profile of the white dashed lines in (a) and (b), respectively. The bridges were designed to be 5-μm wide.

Based on the VO$_2$ films with the same deposition settings, two samples were fabricated using Ar ion milling (etching time = 3 min) and wet etching (etching time = 40 s), respectively. The AFM images in Figure 4.11 were taken on as-etched bridges, showing that the Ar$^+$-etched bridge contains sharp edges despite some considerable 'ears', while the wet-etched bridge contains more irregular edges and disconnections. The height profiles of the bridges reveal that even though being designed to be 5-μm wide, they differ in size, with the Ar$^+$-etched bridge measuring 6.5 μm and the wet-etched bridge measuring 4.3 μm. These differences can be caused by the 45-degree angle of the Ar$^+$ beam used in Ar$^+$ etching and the over-etching that occurred during wet etching. Another interesting pattern that occurs during the wet etching is that parallel strips emerge and cross over each other on the substrate, and even extend into the bridge (Figure 4.11(b)). The lines are about 6 nm high on average and some form rectangular shapes, similar to the cracks on thicker VO$_2$ films as discussed in Section 3.4. Therefore, during the wet etching, the strain appears to be relaxed. It does not directly result in cracks, but the areas of weaker strain between the domains lead to over etching along

the straight boundaries[122]. While it is uncertain whether the materials along the lines are monoclinic, they still cause the bridge to become discontinuous and non-reproducible, ultimately resulting in switching failure.
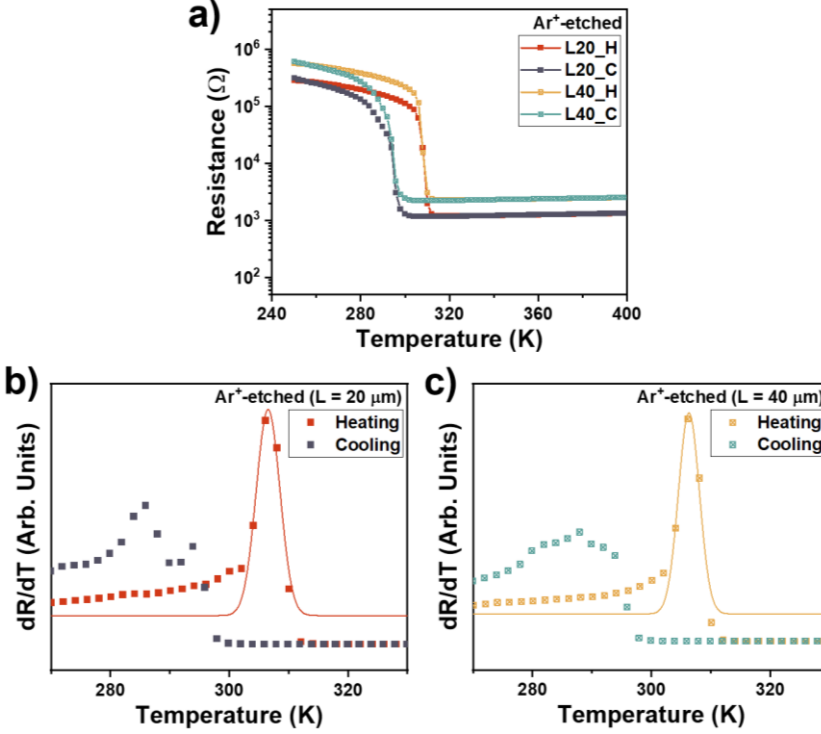
Figure 4.12 (a) Temperature dependence of the resistance of the Ar$^+$-etched VO$_2$ bridges (W= 5 µm, L = 20 and 40 µm). The *dR/dT* plots of the heating and cooling processes for device with length of (b) L = 20 µm and (c) L = 40 µm. The data of the heating branch are fitted using the Gaussian function.

L	20 µm	40 µm
$R_{\text{insulating}}$	86.8 kΩ	170.2 kΩ
R_{metallic}	1.29 kΩ	2.45 kΩ
T_{IMT}	306.5 K	306.3 K
T_{MIT}	285.9 K	287.9 K

Table 4.3 Resistance and transition temperature of Ar$^+$-etched bridges.

Except for the difference in device structure, the two etching techniques also impact the IMT of the devices, as measured by the temperature-dependent resistance (two-point resistance). Figure 4.12 shows the results of two Ar$^+$-etched bridges with length of 20 μm and 40 μm. The dR/dT for both heating and cooling cycle are calculated, and the heating branches are fitted with the Gaussian function. The resistance values of insulating state ($R_{\text{insulating}}$) and metallic state (R_{metallic}) and the transition temperatures are listed in Table 4.3. The resistances of the Ar$^+$-etched bridges scale with device length, while the T_{IMT} remains constant.

Similar measurements and calculations have been done for wet-etched bridges with length of 25 μm and 50 μm. Figure 4.13 shows the results which are completely different as compared to Ar$^+$-etched bridges. The R-T curves in Figure 4.13(a) display two distinct switching steps for both the heating and cooling branches, each of which corresponds to a peak in the dR/dT curves. It should be mentioned that the second peak is considerably smaller than the first, and the range has been adjusted in Figures 4.13(c) and (e) to enhance the visibility of the peaks. The resistance values of each state ($R_{\text{insulating}}$, R_{inter}, and R_{metallic}) and the transition temperatures are listed in Table 4.4. It is surprising to see the resistances of wet-etched bridges do not scale with the device length, which may result from the irregular discontinuous lines in the bridges. Additionally, the transition temperatures for the first switching are comparable, but differ for the second one. The R_{metallic} is much lower than the ones of Ar$^+$-etched bridges. However, the cause for this difference is still unclear. One possible explanation is that the materials surrounding the lines are of monoclinic phase and exhibits IMT accompanied with structural transformation leading to lower resistivity at higher transition temperatures.
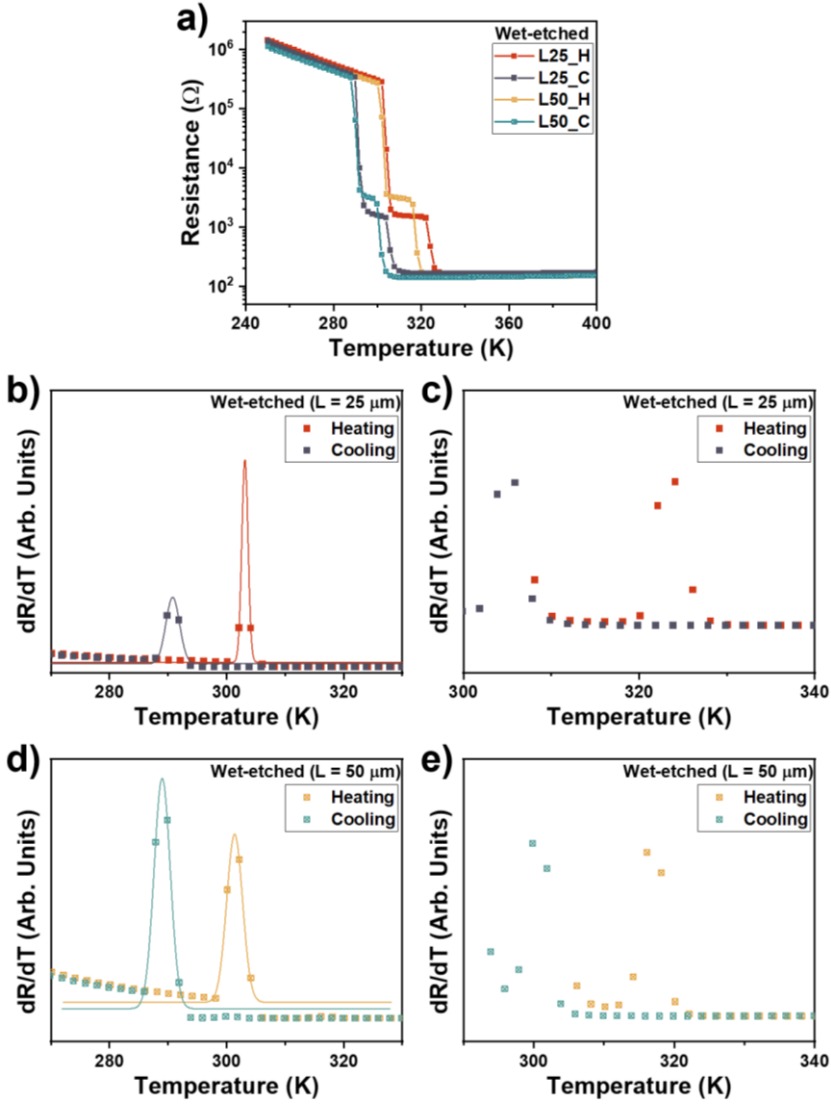
Figure 4.13 (a) Temperature dependence of the resistance of the wet-etched VO$_2$ bridges (W= 5 μm, L = 25 and 50 μm). The dR/dT plots of the heating and cooling processes for device with length of (b) L = 25 μm and (d) L = 50 μm. The data of the heating branch are fitted using the Gaussian function. (c) and (e) is the zoom-in range for temperatures above 290 K in (b) and (d), respectively.

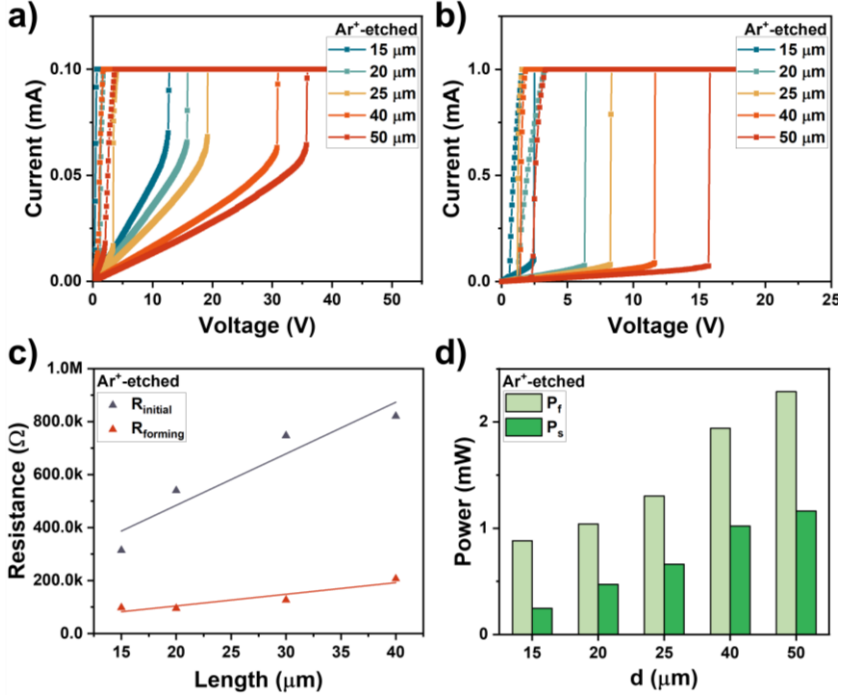| L	25 µm	50 µm
$R_{\text{insulating}}$	362.5 kΩ	302 kΩ
R_{inter}	1.49 kΩ	2.82 kΩ
R_{metallic}	0.18 kΩ	0.16 kΩ
T_{IMT1}	303 K	301.4 K
T_{MIT1}	290.8 K	289 K
T_{IMT2}	324.2 K	316.1 K
T_{MIT2}	305.8 K	299.9 K

Table 4.4 Resistance and transition temperature of wet-etched bridges.

Figure 4.14 Electrical characterization of Ar⁺-etched VO₂ bridges (W= 5 µm, L = 15, 20, 25, 40, and 50 µm). (a) I-V curves of the forming cycle. I_{CC} = 0.1 mA. (b) I-V curves of the subsequent cycle. I_{CC} = 1 mA. (c) Initial resistance and resistance after forming for Ar⁺-etched VO₂ bridges as a function of length. The data are fitted with a linear function. (d) Calculated forming power (P_{f}) and set power (P_{s}) as a function of length for devices.

	Initial	After forming
R_c	47.63 kΩ	8.34 kΩ
R_{sh}	97.25 kΩ/sq	21.75 kΩ/sq

Table 4.4 Contact resistance and sheet resistance of Ar[+]-etched devices before and after forming.

The electrically driven IMT and switching behaviors of the two samples were also studied. Figure 4.14 exhibits the *I-V* characteristics of Ar[+]-etched bridges with varying *L*, including the forming cycles in Figure 4.14(a) and the subsequent voltage sweep cycles in Figure 4.14(b). The devices show the same volatile switching behavior and forming effect as discussed in previous section. The initial resistances and the resistances after the forming cycle are plotted as a function of device length and fitted with a linear function in Figure 4.14(c). According to the transfer length method (TLM)[123], ignoring the resistance of electrode pads, the vertical axis intercept gives an estimate of twice the device contact resistance ($2R_c$), and the slope gives an estimate for sheet resistance (R_{sh}). The values obtain from the linear fit are listed in Table 4.5. After forming, both R_c and R_{sh} decrease dramatically, leading to the decrease of switching power (Figure 4.14(d)). Therefore, the forming effect happens both at the interface of the electrodes and VO$_2$ bridge, as well as within the bridge itself. Bohaichuk et al. referred to the forming at the interface as a burn-in effect which may be caused by the heat from current overshoot at the moment of switching[124]. Due to the presence of the adhesive Ti layer, there will be a very thin TiO$_x$ layer at the interface of the bridge and electrodes. During the forming cycle, the native oxide layer is broken through, making it easier to repeat switching later. As for the resistivity change within the bridge, it results from the long-persisted metallic domains that can be maintained without external bias[92,125]. The forming is not permanent and devices normally recover in one or two days, which is consistent with previously reported data[124].

On the other hand, some of the wet-etched devices were not able to be switched even with a voltage up to 50 V at room temperature (295 K), due to the large initial resistance and transition temperature. The forming cycles were measured at 300 K and the subsequent sweeps were performed at 295 K. The resistance and switching power before and after

forming are not comparable in this case. The *I-V* curves in Figure 4.15 demonstrate that the switching behaviors of the devices vary, and no clear trend can be observed with respect to the device length. This phenomenon is typically caused by the over-etching effect, creating unpredictable disconnected lines within the bridge.
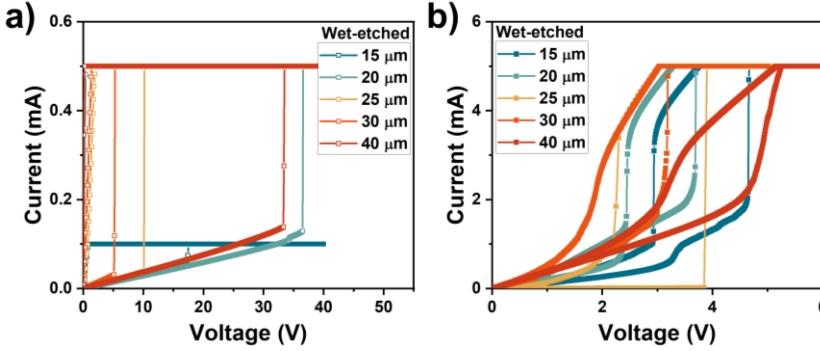

Figure 4.15 Electrical characterization of wet-etched VO$_2$ bridges (*W* = 5 μm, *L* = 15, 20, 25, 30, and 40 μm). (a) *I-V* curves of the forming cycle at 300 K. (b) *I-V* curves of the subsequent cycle at 295 K. I_{CC} = 5 mA.

The bridge topography, temperature-dependent resistance and switching behaviors of the Ar$^+$-etched devices and wet-etched devices are investigated and compared. The Ar ion milling with an etching angle of 45° results in wider bridges, showing typical IMT with constant T_{IMT} as the VO$_2$ film (Section 3.3), and predictable switching features. Nevertheless, wet etching is challenging as it poses a risk of size and continuity loss due to over-etching. Though we have obtained several samples with wet etching successfully[3], the IMT and switching behaviors of some of the samples are different and intractable. Therefore, for further exploration, the more reproducible and controllable etching technique, namely Ar ion milling, is preferred.

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[3] The samples measured for Section 4.3.2 were fabricated with wet etching. The size and continuity of the bridges were carefully checked to ensure that they were suitable for the systematical switching characterization.

4.4 Conclusion

Two-terminal resistive switching devices based on VO_2 single bridges were successfully fabricated and characterized. The VO_2 single-bridge devices show typical volatile switching behavior, which is achieved by applying electrical bias to create Joule heating in the device and trigger the IMT. By tuning the applied voltage or current, we realized multistate memory within one VO_2-based memory cell and reliable multilevel operation at room temperature. This multi-level operation of the VO_2-bridge devices results from the exploiting sub-hysteresis loops by Joule heating, which provides opportunities for novel neuromorphic electronics or other applications of tunable resistors.

Additionally, the reliability of the different etching techniques was investigated. The influences of Ar ion milling and wet etching on the bridge topography, temperature-dependent resistance and switching behaviors of the devices were compared. In conclusion, the Ar ion milling is more reproducible and controllable, making it suitable for further exploration.

In summary, the findings in this chapter demonstrate the switching principles and mechanism of VO_2-based single-bridge devices, serving as a starting point for the development of novel neuromorphic electronic devices based on VO_2 bridges.

Chapter 5.

Enhancing control on multiple resistive states in VO$_2$ double-bridge devices

The VO$_2$ single-bridge devices described in Chapter 4 show volatile resistive switching behavior and reliable multilevel operation. A higher degree of control for the multistate can be achieved by assembling single bridges in parallel configuration, starting with double bridges. As one more switching element is added, the switching behaviors are influenced by the intrinsic IMT of individual bridges and the thermal interaction among them. Due to the complexity of the switching dynamics, nanoscale thermal mapping of in-operando devices has been carried out using scanning thermal microscopy, which gives us a straightforward indication of the current distribution among the bridges. By understanding the switching principles of VO$_2$ double-bridge devices, novel circuit elements can be obtained through structural manipulation of devices assembled from individual switching elements.[1]

5.1 Introduction

To overcome the limitation of the computing system based on the Von Neumann architectures, neuromorphic computing systems which mimic the function of neurons and synapses are of particular interest[14,126]. As previously discussed, VO_2 becomes an attractive candidate since the electrical conductivity and thermal conductivity are highly temperature-dependent, leading to the potential nonlinear dynamics based on the electrothermal feedback loop[30,31]. Furthermore, the tunable multilevel resistive states have been achieved in a single VO_2 bridge as reported in Chapter 4.

In this chapter, we continued to build up planar devices with VO_2 double bridges to obtain better control over the resistive states. To characterize the switching behaviors, both voltage-controlled and current-controlled measurements are performed, which result in totally different *I-V* characteristics. Due to the additional switching elements, the switching behaviors are determined by the intrinsic IMT of individual bridges and the thermal interaction among them. Therefore, the spacing between bridges plays an important role in determining the number of switches and the power required for the subsequent switches.

Furthermore, scanning thermal microscopy (SThM) is used to understand the current distribution in the devices straightforwardly. It uses a special thermo-resistive probe that enables the characterization of thermal phenomena on the sample surface[127,128]. For VO_2 bridges, the local heating generated is directly linked to the current flow, due to Joule heating[25,93]. Assuming that the voltage is equal across both bridges and decreases linearly along the device, the current can be determined from the Joule heating. Therefore, a qualitative picture of the resistive switching dynamics in devices can be drawn by measuring the thermal signals with SThM.

5.2 Device design and fabrication

Based on single-bridges devices, the double-bridge devices are created by adding an additional parallel bridge between the two electrodes. The design, illustrated in Figure 5.1(a), shows the two bridges are of the same shape and size, with the distance (d) between them being a variable.

The fabrication of VO$_2$ double-bridge devices follows the same procedure outlined in Chapter 4, with the bridges being etched by Ar ion milling. Figure 5.1(b) and (c) show an example of the as-fabricated device observed by microscope and AFM, respectively. The bridges have been effectively etched as the AFM profile (Figure 5.1(d)) indicating a step height of 15 nm, including approximately 11 nm of VO$_2$ film and 4 nm of TiO$_2$ substrate.
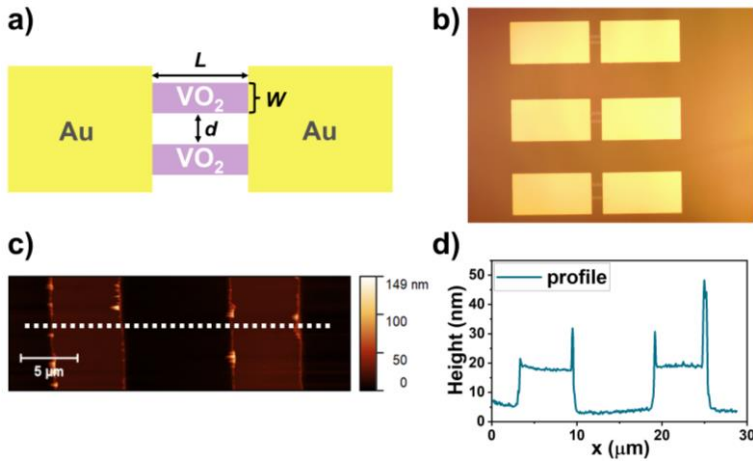

Figure 5.1 (a) The schematic design of VO$_2$-based double-bridge device (top view). (b) Optical photo of as-fabricated devices under a microscope. (c) Surface topography map of a VO$_2$ double-bridge device ($W = 5$ μm, $L = 15$ μm, $d = 10$ μm). (d) Height profile of the white dashed line in (c).

5.3 Electrical characterization

The electrical properties of the VO_2 double-bridge devices are investigated with the same setup used for single-bridge devices. Figure 5.2 shows the *I-V* characteristics of three devices with varying *d* measured with voltage-controlled and current-controlled sweeps. To be noted, all resistive switching characteristics reported are measured after the initial forming, described for single bridges in Chapter 4. Consistent with the single-bridge devices, the double-bridge devices also show volatile resistive switching behavior in both cases. Moreover, the current-controlled curves provide more information which is hidden from the abrupt resistance change in the voltage-controlled measurements. As for voltage sweep, the heating generated at the switching point increases abruptly while for the current sweep the heating increases gradually and can be stabilized. For the device with a smaller spacing (*d* = 5 μm in Figure 5.2(a)), the current-sweep curve also displays a single set as the voltage-sweep one, whereas there are two turns during the reset. On the other hand, the device with a larger spacing (*d* = 30 μm in Figure 5.2(b)) exhibits two switches, including a first set to an intermediate resistive state and a secondary set to the LRS at a higher current value. A critical spacing value has been observed, in this experiment *d* = 20 μm. As shown in Figure 5.2(c), the device shows either a single set or two sets during current sweeps randomly.

Figure 5.3 schematically shows the switching status of the double bridges corresponding to different resistive states. In the beginning, both of the bridges are OFF and the overall device shows HRS. Once the current is applied, due to the intrinsic inhomogeneity, one bridge will switch to ON state first, therefore the device shows the intermediate state. Finally, the other bridge will also switch ON with increased current and the device shows LRS. As one more VO_2 bridge is added, the thermal interaction between the two Joule heating-induced switching elements plays an important role in the number of switches. For smaller-spacing devices, the bridges are switched simultaneously from HRS to LRS due to the strong thermal crosstalk effect. If the bridges are farther apart, the thermal interaction weakens, and bridges can be switched individually giving a chance for the emergence of the intermediate state.
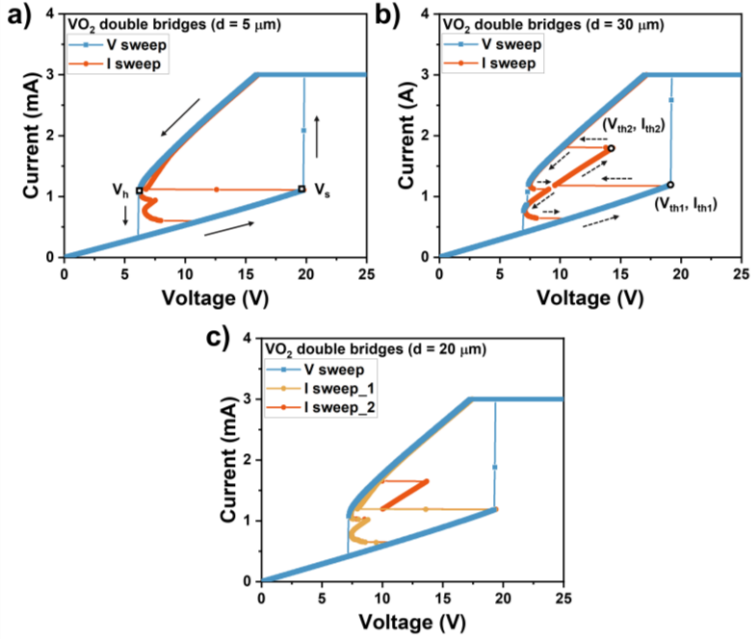
Figure 5.2 Voltage-controlled (direction indicated with solid arrows) and current-controlled (direction indicated with dashed arrows) *I-V* characteristics of double-bridge devices (*W* = 5 μm) with different *d*: (a) 5 μm, (b) 30 μm and (c) 20 μm. I_{CC} = 3 mA. The terminology of set voltage (V_s) and hold voltage (V_h) for voltage sweep are indicated in (a). The terminology of threshold voltages (V_{th}) and currents (I_{th}) for current sweep are indicated in (c). Subscripts 1 and 2 stand for the first snapback and the second snapback, respectively.
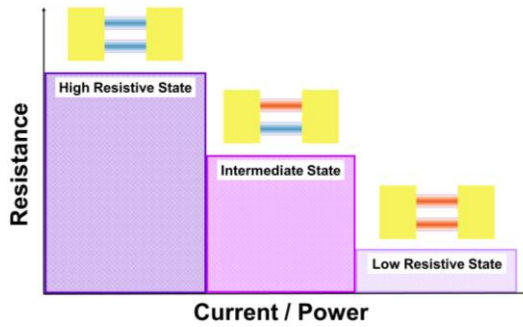

Figure 5.3 Schematics of VO$_2$-based double-bridge devices to show the switching status of bridges corresponding to different resistive states. The color codes assigned to the bridges denote their status, with red indicating that the bridge is ON while blue represents that the bridge is OFF.

More interestingly, there are several negative differential resistance (NDR) regions in the current-sweep curves, where the differential resistance (dV/dI) of the device is negative. NDR can be found in materials that form higher current density channels relative to the rest of the material under the electrical stimuli[129]. There are two types of NDR, the S-type NDR refers to a smooth transition from positive to negative differential resistance, and the snapback NDR refers to a discontinuous characteristic[28,130]. Both and sometimes even more complex combinations of them have been observed in our devices. The dynamical instabilities associated with NDR are of great interest due to the potential applications, including selectors, threshold switches, amplifiers, and chaotic oscillators[28]. For the thermally activated oxides like VO_2, the dynamics and instabilities result from the electrothermal feedback loop, as the electrical and thermal properties are highly temperature-dependent[15]. Based on the model reported by Nandi et al., the snapback NDR is a generic response of materials with a strong temperature dependent conductivity, and the S-type NDR can emergence by tuning the material conductivity, device area or ambient temperature[130]. In our devices, the snapback NDR is usually observed during the set process due to the sharp transition from low conductivity to high conductivity, while the S-type NDR is observed during the reset where the VO_2 bridges are experiencing a relatively slow transition[26,92].

From the current-controlled *I-V* characteristics in Figure 5.2, the differential conductance (dI/dV) of the measured devices is calculated and plotted as a function of applied current in Figure 5.4. The dI/dV values near the switching points diverge to large positive and negative values. When the device resistance settles, the dI/dV should scale with the number of conductance paths available for the current[131]. For the device with a smaller d (Figure 5.4(a)), there is only one step for the set representing the simultaneous switching, while for the device with a larger d (Figure 5.4(c)), there are two steps representing the individual switching. Notably, the height of the two steps is equal and half that of the one step, as evident in Figure 5.4(b). The dI/dV of the reset process contains two steps and the plateau values match with the ones of the set, suggesting the bridges are switched to HRS individually in all cases.
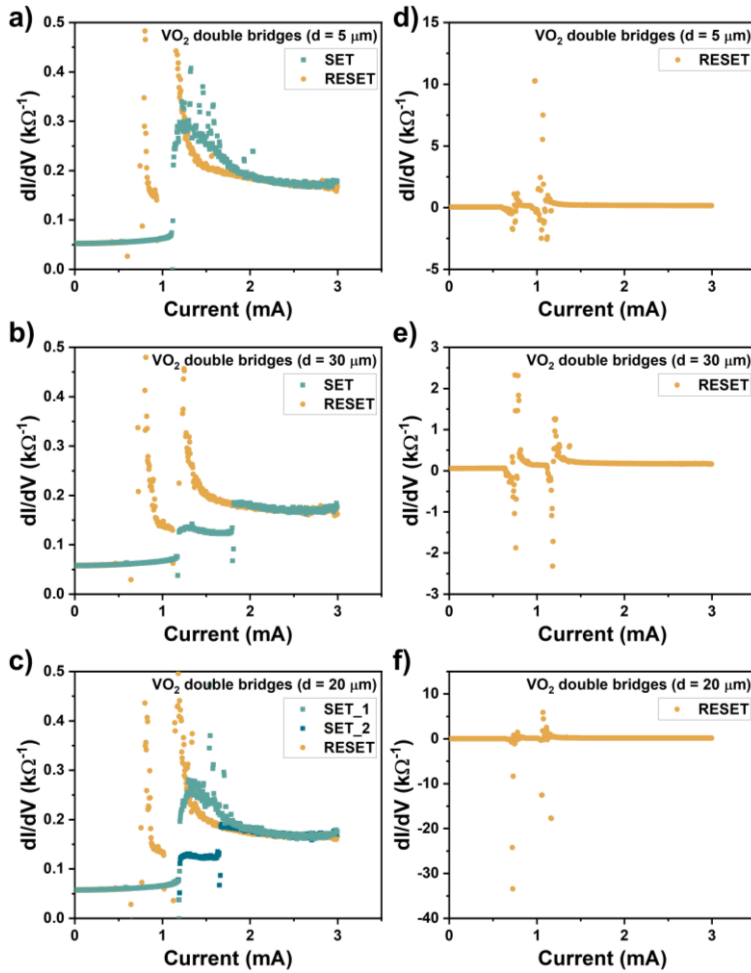
Figure 5.4 Differential conductance (*dI/dV*) as a function of applied current during the set and reset process for the devices measured in Figure 5.3: (a) *d* = 5 μm, (b) *d* = 20 μm, (c) *d* = 30 μm. The range is adjusted clearly in visible steps. (d-f) The full range of *dI/dV* during reset process.
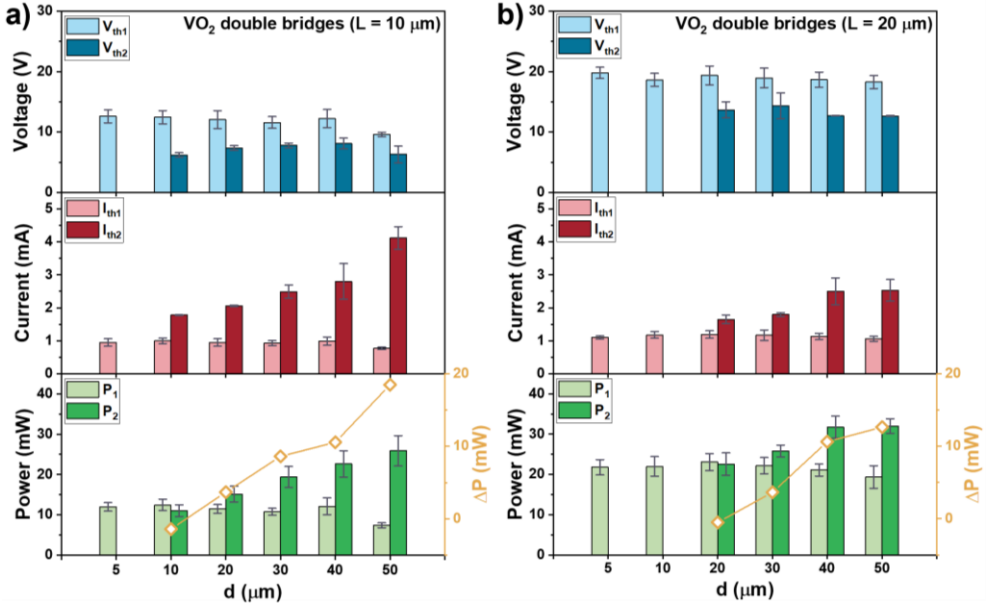
Figure 5.5 Switching parameters of current-controlled measurements as a function of the bridge spacing for VO$_2$-based double-bridge devices: (a) $L = 10$ μm, $W = 5$ μm and (b) $L = 20$ μm, $W = 5$ μm. The top panel shows the threshold voltage (V_{th}). The middle panel shows the threshold current (I_{th}). The bottom panel shows the calculated switching power (P) and the power difference (ΔP) between the first and the second snapback. Subscripts 1 and 2 stand for the first snapback and the second snapback, respectively.

Figure 5.5 shows the correlation between the current-controlled switching parameters and d for two devices with different L (10 μm and 20 μm), respectively. The threshold voltage (V_{th}) and power (P) both scale with L, while the current (I_{th}) does not. The shorter bridges ($L = 10$ μm) can be switched individually at a smaller spacing compared to the longer bridges ($L = 20$ μm), which is beneficial for down scaling the device further. The power needed for the first snapback (P_1) is not strongly dependent on d while the power required for the second one (P_2) is correlated with d. At the critical point, $d = 10$ μm in Figure 5.5(a) and $d = 20$ μm in Figure 5.5(b), P_1 is already enough for both bridges to be switched. However, due to the fluctuation of the heating, there is also potential individual switching within the device and sometimes it dominates the switching behavior. The power difference (ΔP) between P_2 and P_1 scales with d, in line with the consideration that more power is required for the secondary switch when the thermal crosstalk becomes less significant.
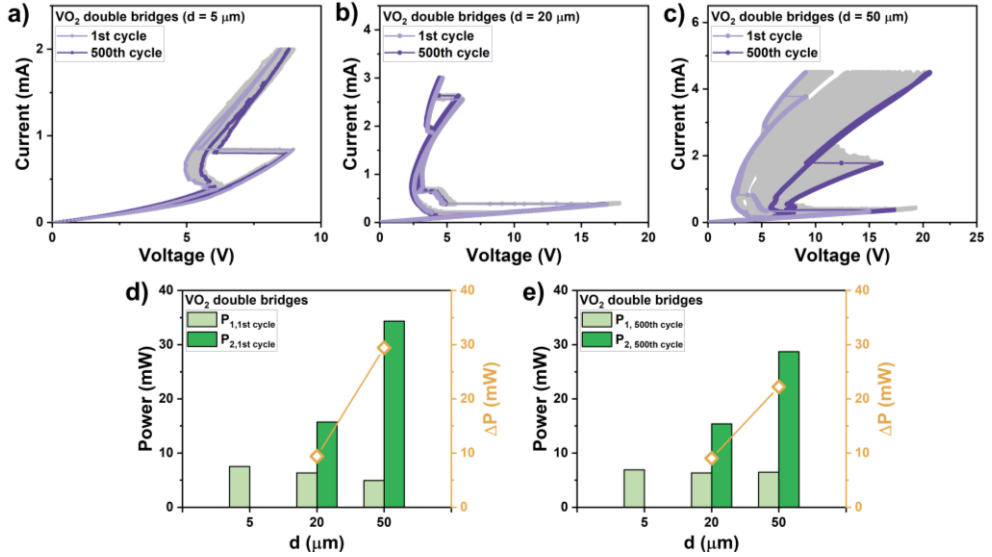
Figure 5.6 Current-controlled *I-V* characteristics of double-bridge devices ($W = 5$ μm) with different *d* for 500 cycles: (a) 5 μm, (b) 20 μm and (c) 50 μm. *P* and ΔP of the three devices for (d) the 1st cycle and (e) the 500th cycle.

To check the repeatability, the current sweeps were performed for 500 cycles for devices with varying *d*. The *I-V* curves plotted in Figure 5.6 show that both simultaneous switching and individual switching behaviors are reproducible and stable over 500 cycles. However, for the device with an extremely large *d*, in this experiment $d = 50$ μm (Figure 5.6(c)), there are some variations after the first 100 cycles. During the first switch, the S-type NDR disappears, and the sharp snapback dominates. The second switch happens at a higher voltage but lower current. The calculated P_1, P_2 and ΔP of the 1st and 500th cycles are plotted in Figure 5.6(d) and (e). After the cycling, the values for the 5 μm-spaced and 20 μm-spaced bridges remain constant. For the 50 μm-spaced bridges, P_1 increases by 0.7 mW while P_2 and ΔP decrease by approximately 7 mW. The variation in the large-spaced bridges results from the continuous operation with high power (30 to 35 mW). Therefore, it is essential to restrict the spacing between the bridges within a specific range to maintain the switching behavior reproducible.
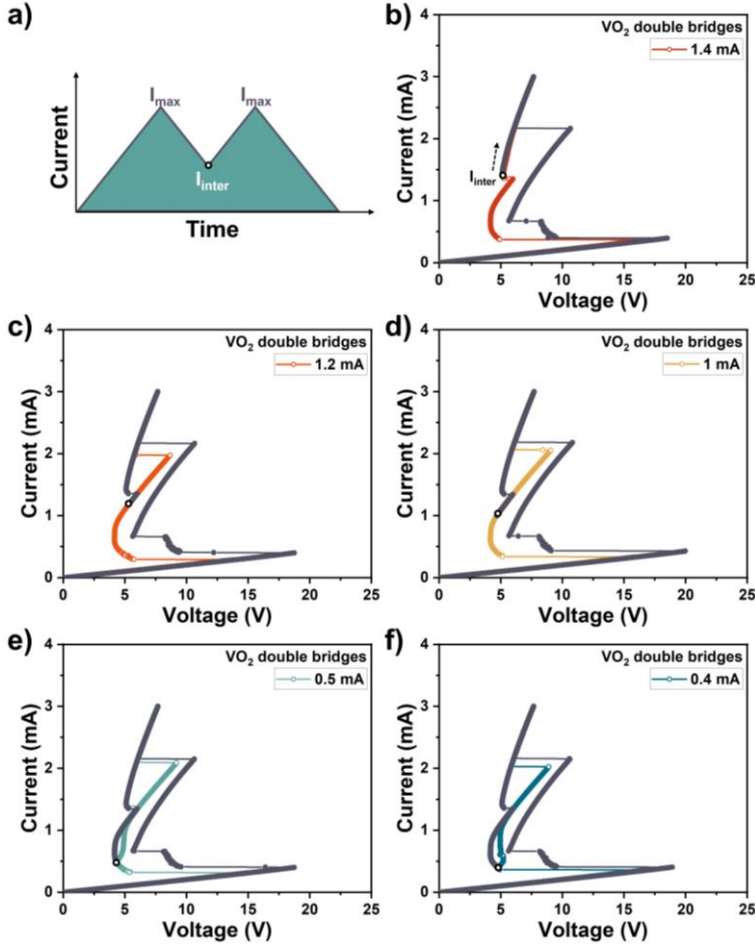
Figure 5.7 (a) The applied current during segment sweep measurements as a function of time. *I-V* curves of the segment sweeps for a double-bridge device with different I_{inter}: (b) 0.4 mA, (c) 0.5 mA, (d) 1 mA, (e) 1.2 mA, and (f) 1.4 mA. The turning points are indicated by the opened black dot.

Similar to the voltage segment sweeps performed on single-bridge devices, the current segment-sweeps were also performed on double-bridge devices to study the resistive states of the reset process. The sweep function can be seen in Figure 5.7(a). The current is swept from 0 A to the maximum value (I_{max}) and then is swept back and turned at I_{inter} to return to I_{max}, and finally swept all the way back to 0 A. The results for different I_{inter} values are plotted in Figure 5.7(b-f). There are two situations where I_{inter} occurs: before the first turn of the reset, and before the second turn of the reset. Figure 5.7(b) shows an example of I_{inter} = 1.4 mA,

where both bridges are still ON. Therefore, once the current is turned at 1.4 mA, the device remains in LRS and follows the same *I-V* curve. Regarding the region between the first reset and the second reset, one bridge is OFF, and the other is still ON. If the I_{inter} is in the linear region, as shown in Figure5.7(c) and (d), the device initially follows the reset branch of the *I-V* curve and then is switched to LRS at a lower P_2. However, if the I_{inter} is in the NDR (Figure 5.7(e) and (f)), the device undergoes multiple intermediate states before tracking the reset branch, which results from the instability in the NRD.

According to the current segment-sweeps, there are two possible scenarios for the double-bridge device to switch from having one ON-state bridge and one OFF-state bridge to both bridges being ON-state, which are following either the set branch or reset branch. It is further confirmed that the resistive state of the device with one ON-state bridge and one OFF-state bridge depends on the switching history it experiences. As noted in Figure 5.8(a), during the multilevel operation on the double-bridge device, several resistive states can be probed in the whole set and reset cycle, including the HRS (A), the NDR state during set (B), the intermediate state during set (C), the LRS (D), the intermediate state during reset (E) and the NDR state during reset (F). These states can be tuned consecutively or randomly as shown in Figure 5.8(b) and (c). The HRS (A) and LRS (D) values are constant regardless of the switching history, while the NDR states (B and F) are similar but may have slight variations. However, the resistances of the intermediate states C and E are different, despite both representing the device with an ON-state bridge and an OFF-state bridge. When switched from two OFF-state bridges (A), the transition of the VO$_2$ bridge follows the heating branch of the hysteresis IMT loop. On the other hand, when switched from two ON-state bridges (E), the VO$_2$ bridge undergoes a transition following the cooling branch. Thus, the resistance of the OFF bridge during reset is lower than during set, resulting in a smaller intermediate state.
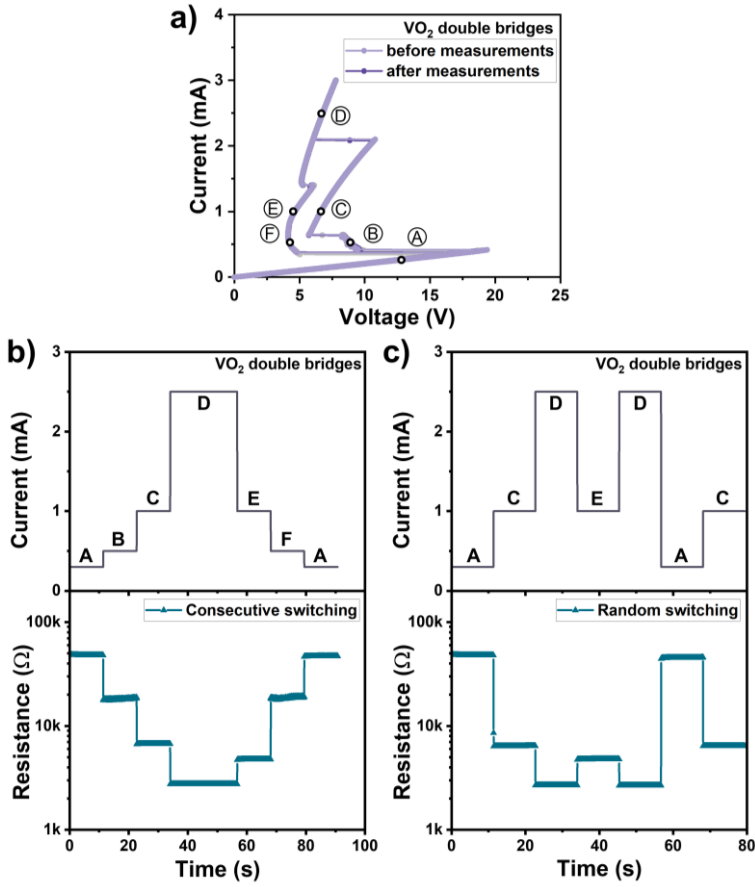
Figure 5.8 (a) Current-controlled *I-V* characteristics of VO$_2$-based double-bridge devices ($W = 5$ µm, $L = 15$ µm, $d = 30$ µm) before and after the multilevel operation. The points where the resistive states were probed are labeled by letters (A: 0.3 mA, B: 0.5 mA, C: 1 mA, D: 2.5 mA, E: 1 mA, F: 0.5 mA). Multiple resistive states are accessible in (b) consecutively and (c) randomly. The upper panels are the applied voltage as a function of time and the lower panels are the resistance as a function of time.

Moreover, temperature-dependent resistive switching features were investigated. Both the voltage-sweep and current-sweep curves are displayed in Figure 5.9 and the related switching parameters are plotted in Figure 5.10. With increasing operating temperature, V_s, V_h and the hysteresis window between them for the voltage-controlled measurements reduce. For the current-controlled measurements of the device with large d (30 µm), I_{th}, P and ΔP also decrease with increasing temperature. Interestingly, the device with smaller d (5 µm) starts to show individual switching when temperature increases. The critical temperature is 300 K where the device shows a secondary switch after the NDR region. When operating the device closer to the transition temperature, the required power for switching becomes lower, therefore the thermal cross talk also decreases.
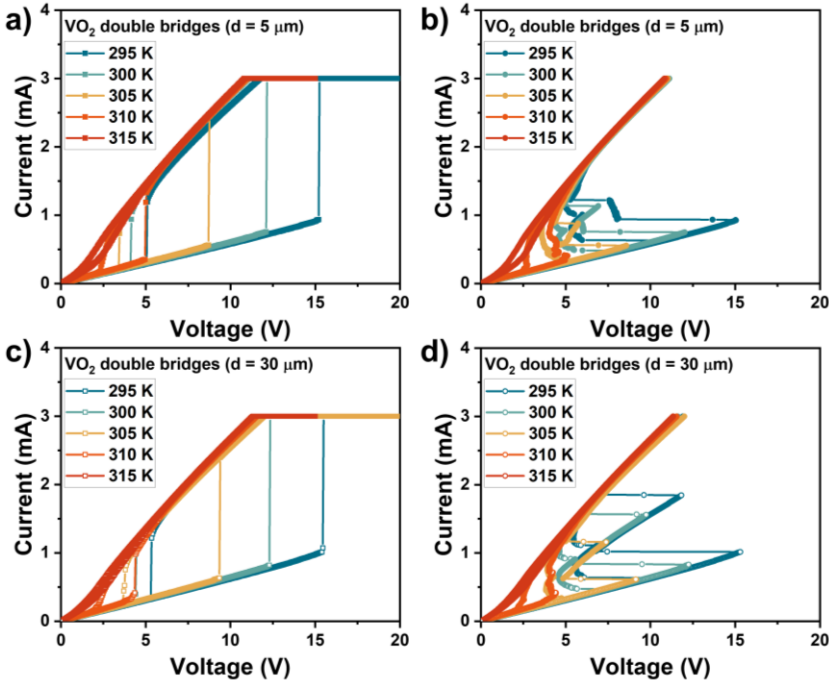
Figure 5.9 Temperature-dependent measurements of VO$_2$-based double-bridge devices ($L = 15$ µm, $W = 5$ µm) with different d. The temperature increased from 295 K to 315 K with an incremental step of 5 K. (a) Voltage-controlled *I-V* characteristics, (b) current-controlled *I-V* characteristics for the device with $d = 5$ µm. (c) Voltage-controlled *I-V* characteristics, (d) current-controlled *I-V* characteristics for the device with $d = 30$ µm.

Figure 5.10 (a) Temperature-dependence of V_s and V_h of voltage-controlled measurements and (b) P and ΔP of current-controlled measurements for the 5 µm-spacing device. (c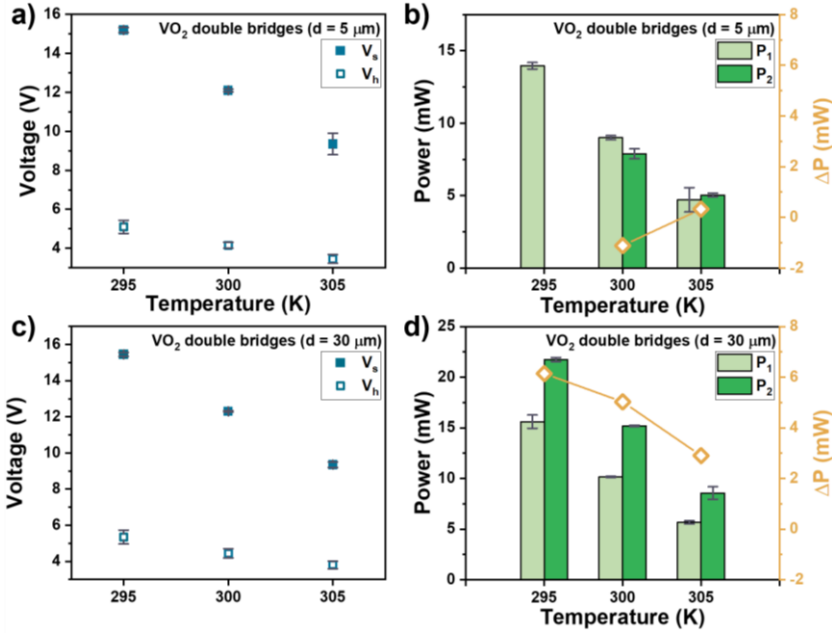) Temperature-dependence of V_s and V_h of voltage-controlled measurements and (d) P and ΔP of current-controlled measurements for the 30 µm-spacing device.

5.4 Switching dynamics

5.4.1 Scanning thermal microscopy

Scanning thermal microscopy (SThM) is one of the scanning probe techniques for imaging the topography and heating features on the device surface simultaneously. It uses a special thermo-resistive probe with high thermal sensitivity (< 1 K) that enables the characterization of thermal phenomena on the sample surface with nanoscale spatial resolution (<50 nm)[127,128]. SThM is performed using an Asylum AFM and a SThM thermo-resistive probe from Bruker. The SEM image[132] in Figure 5.11(a) shows that the tip of the SiN probe is coated by Pd, which can correlate changes in its electrical resistance with temperature variations in the tip ($R_{probe} \propto T_{probe}$)[132]. The SThM probe is electrically connected to an external Wheatstone bridge (Figure 5.11(b)) consisting of two fixed resistances (1 kΩ each), a potentiometer (R_{pot}), and the resistance of the probe (R_{probe}). When operating the SThM, a voltage bias (V_{source}) is

applied to the Wheatstone bridge to induce an electrical current. The electrical current leads to an increment of the temperature of the probe originated by self-heating, which consequently results in an increase of its electrical resistance. For thermal sensing, this current must be as low as possible to track changes in the probe resistance when scanning the surface of a sample but avoiding as much self-heating as possible. Therefore, the SThM measurements are performed in passive mode, with a 0.5 V set point and a 0.5 V tip bias. The potential measured across the bridge (V_{SThM}) allows to determine accurately the changes of the electrical resistance of the probe and hence, temperature variations on the surface of the device.
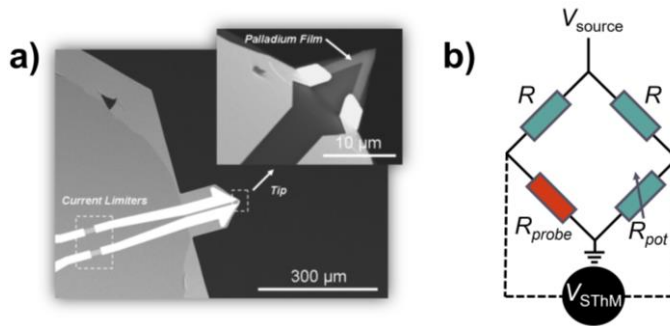

Figure 5.11 (a) SEM image of the SThM probe. (b) The schematics of the Wheatstone bridge which consists of four resistors: two having fixed resistances R, a potentiometer R_{pot} and the resistance of the probe R_{probe}. A voltage with variable magnitude is applied between V_{source} and the ground during the measurements. Figure (a) is reproduced from [132].

During the SThM scans, the device is biased at constant current bias values when the resistance is settled. The current is ramped up towards a maximum at which the entire device is fully switched to the LRS. Afterwards the current is ramped down back to 0 mA to reset the device. To probe the amount and variation of the thermal background noise, a scan with zero bias current is always performed prior to the first biased SThM scan and after the last. To be noted, the thermal signal measured from SThM cannot be directly related to the surface temperature without certain calibration steps but serves as a qualitative indication of the current distribution among the bridges[128].

The measured samples were coated with a 90 nm-thick PMMA-A2 layer for the SThM scans, in order to protect the SThM tip from electrical discharges while biasing the devices. The PMMA layer was spincoated at 2000 rpm for 2 min and successively baked for 5 min on a hot plate at 180 °C.

5.4.2 Thermal maps of VO$_2$ double-bridge devices

The electrical measurements show signs of bridges individually being switched ON and OFF during the current sweep. However, this is not a direct verification until the individual switch is imaged using SThM, which can sense the heat dissipation over a surface topography with a thermo-resistive tip (Figure 5.12(a)).

During the SThM scans, the device was set to stable intermediate resistive states by biasing at constant current values as labeled in the current-sweep curve (Figure 5.12(b)). Three resistive states were chosen for the scans during both the set and reset processes, as depicted in Figure 5.12(c). The thermal maps obtained during these processes are shown in Figure 5.12(d) and (e).

By increasing the bias current from zero to a value below the threshold current for switching I_{th}, the current distributes evenly over the two bridges (scan A). When one of the bridges switches, the heating is redistributed indicating that almost all the current flows through the bridge that has switched ON (scan B). By further increasing the bias current, there will be an increase in the current flowing through both bridges according to their differences in resistance and, potentially supported by heat transferred from the bridge with the highest current, also the remaining bridge switches to the LRS (scan C). The reset process is basically the inverse process of the set behavior, but follows a different trace, due to the hysteretic resistance versus temperature characteristics of the VO$_2$. Starting with two bridges in the LRS (scan D), the right bridge is switched OFF when the current decreases (scan E), and finally the remaining bridge is also switched to the HRS and the current is almost evenly distributed over both bridges again (scan F). While in principle the switching sequence between the two bridges for the set and reset process could be different, we see in Figure 5.12 as well as in all our other measurements thus far, that the order of switching back to the HRS is the reverse

of the switching events to the LRS. Possible contributors for the fixed switching order are the intrinsic differences between the two bridges, including slight variations in geometry, dimensions, material composition, and local defects. The effects may have been amplified during the initial forming step, which could have defined the overall behavior of the bridges.
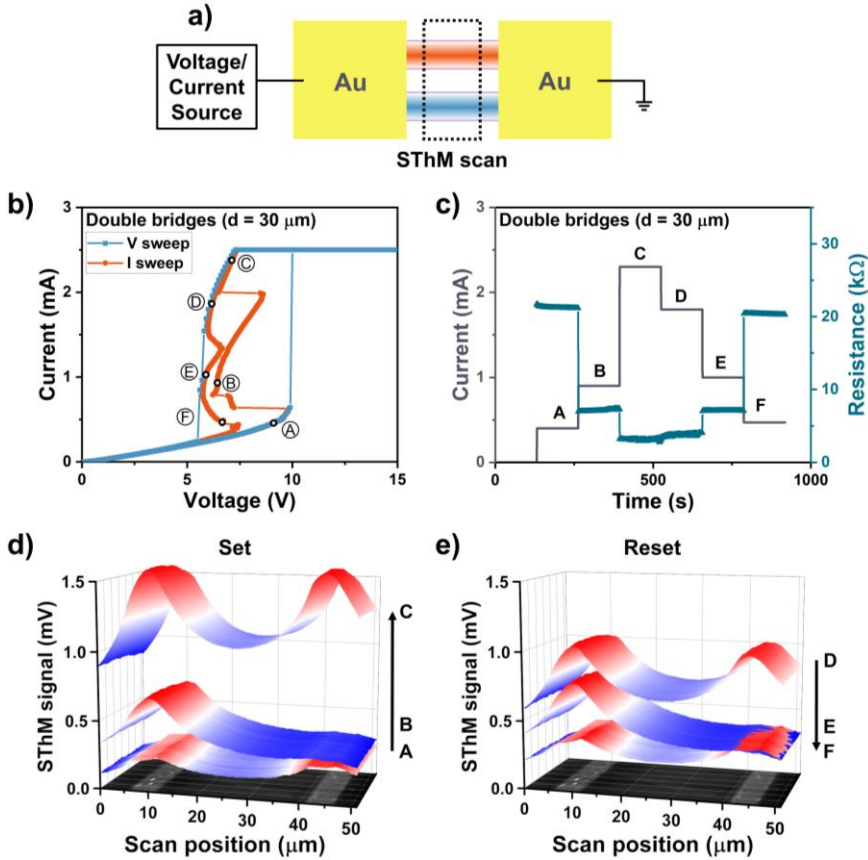

Figure 5.12 (a) Schematic of the simplified SThM measurement setup. The black dash line box is the scan area. (b) Voltage-controlled and current controlled *I-V* characteristics of a VO$_2$-based double-bridge device ($L = 20$ μm, $W = 5$ μm, $d = 30$ μm). $I_{CC} = 2.5$ mA. The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 0.9 mA, C: 2.3 mA, D: 1.8 mA, E: 1 mA, F: 0.47 mA (c) Current applied and resistance measured during SThM measurements. 3D SThM thermal maps during the d) set and e) reset process. The points where the scans were taken are indicated beside their respective maps and the arrow shows the order of the scans. 2D Surface topography images at the bottom are obtained using the SThM tip and shown as a guide for the position of the bridges in the device.

The SThM scans on VO_2 double-bridge devices with varying d were performed to image the switching during the set process and further confirm the dynamics. As can be seen in Figure 5.13, only one wide heating path covering both bridges appears for the smaller-spacing device ($d = 5$ μm) while there are two separate heating paths for larger-spacing devices ($d = 20$ and 50 μm). The straightforward visualization of the current paths further verifies the switching dynamics in the double-bridge devices as illustrated in Figure 5.3.
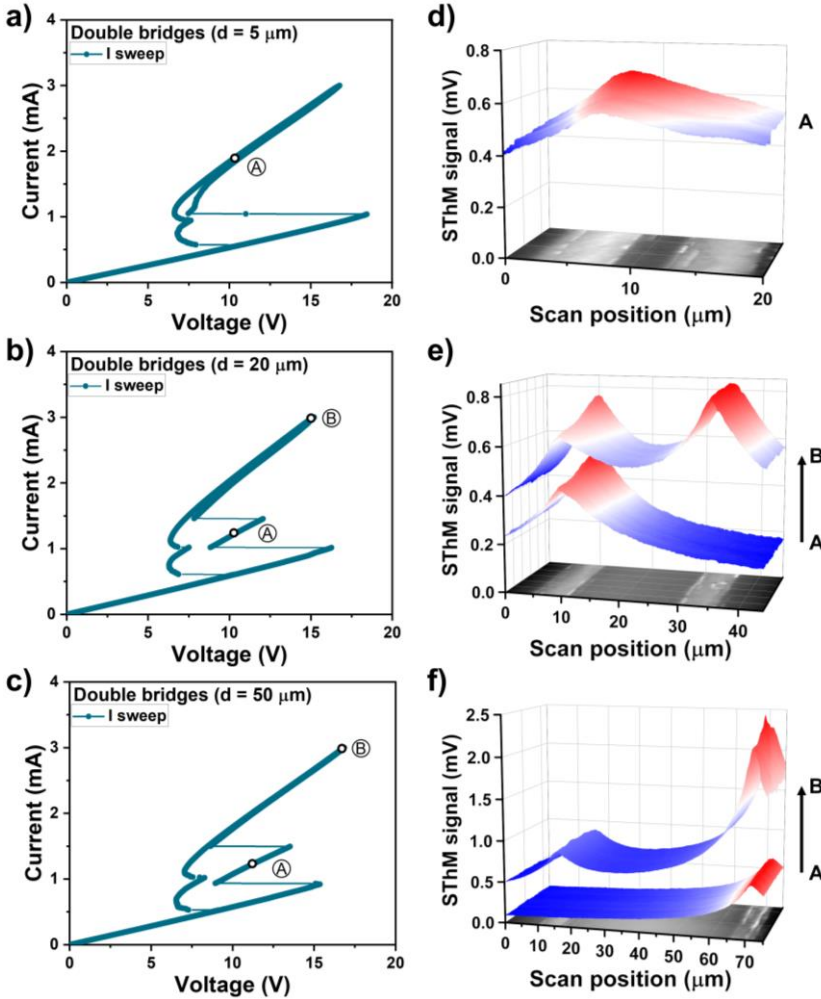

Figure 5.13 Current-controlled *I-V* characteristics of VO_2-based double-bridge devices ($L = 20$ μm, $W = 5$ μm) with different d: a) 5 μm, b) 20 μm, c) 50 μm. The points where SThM measurements were taken are labeled. 3D SThM thermal maps of the corresponding devices: d) $d = 5$ μm, e) $d = 20$ μm, f) $d = 50$ μm.

5.5 Conclusion

Two-terminal resistive switching devices based on VO$_2$ double bridges have been successfully fabricated and characterized. The switching principle of single-bridge devices can be extended to double-bridge devices, including the repeatable volatile switching behavior and the switching power scale with the bridge length. The current-controlled measurements allow a higher degree of control over the resistive states compared to the voltage-controlled ones. The current-controlled switching behaviors are influenced by the intrinsic switching properties of the bridges and the thermal interaction among them.

As the number of the Joule heating-induced switching element increases, the thermal interaction among them will greatly influence the switching behavior, which is a double-sided sword. On the one hand, when the bridges are placed in closer proximity to each other, the thermal crosstalk effect dominates, leading to simultaneous switching. On the other hand, it plays a role in assisting the subsequent switches with lower power. By increasing the spacing within a certain range, the bridges can be switched independently, and the power of the subsequent switches can be reduced, allowing the full potential of the double-bridge devices to be exploited.

In summary, the results stand that VO$_2$ double-bridge devices are promising and have the potential to be developed further into novel circuit elements with more tunable multistate and unique switching behaviors.

Chapter 6.

Extension towards VO₂ multi-bridge devices

Based on the systematic study on VO_2 single-bridge and double-bridge devices, we further extend the device configuration to multiple bridges. Several factors at a device level can be tuned to manipulate the resistive switching behaviors, including the number of bridges, the spacing between bridges and the geometries of the bridges. Devices with additional bridges, such as triple-bridge and quintuple-bridge devices, as well as the devices with multi-width bridges are investigated. Despite the rising complexity in the device configuration, there are some basic trends. The addition of extra bridges will introduce the potential for more switching events and resistive states. The spacing between bridges affects the number of switches and the potential switching bridge. Our findings provide insights into the switching principles of VO_2 multi-bridge devices, which can be used to obtain novel circuit elements through structural manipulation of devices assembled from individual switching elements.[1]

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[1] Parts of this chapter was published as: X. Gao, T. J. Roskamp, T. Swoboda, C. M. M. Rosário, S. Smink, M. Muñoz Rojo, H. Hilgenkamp, Multibridge VO_2-Based Resistive Switching Devices in a Two-Terminal Configuration, Advanced Electronic Materials (2023), in press.

6.1 Introduction

In the previous chapter, it is shown that VO_2 double-bridge devices not only exhibit volatile switching behavior but also possess additional intermediate resistive states. This raises the intriguing question whether we can expand the device configuration while maintaining the fundamental switching principles. Two avenues are explored to achieve this: adding extra bridges to achieve more resistive states and placing bridges with varying widths to gain better control over the switching behavior. The situations for triple-bridge devices, quintuple-bridge devices, and multi-width bridge devices are discussed in this chapter. The growing complexity of the configuration makes it challenging to interpret the switching dynamics from the *I-V* characteristics, therefore, we employ SThM as a powerful tool to visualize the current paths. Multi-bridge devices can be assembled using VO_2 single bridges as building blocks, which are promising for novel circuit elements with more tunable multistate and novel switching behaviors.

6.2 Device design and fabrication

Based on the systematic studies on double-bridge devices, we further expand the device configuration to multiple bridges to investigate whether the switching behavior and principles of single- and double-bridge devices can be maintained. Figure 6.1 displays the designs of the multi-bridge devices, which are created with two considerations. The first is to add additional bridges of the same shape and size in a symmetrical configuration, such as the triple bridges shown in Figure 6.1(a) and quintuple bridges shown in Figure 6.1(b). The second is to place bridges with different geometries (varying widths) into a single device. These devices contain bridges with identical length and spacing but varying widths and order, with the wider bridge placed at the edge of Device I (Figure 6.1(c)) and in the middle of Device II (Figure 6.1(d)).
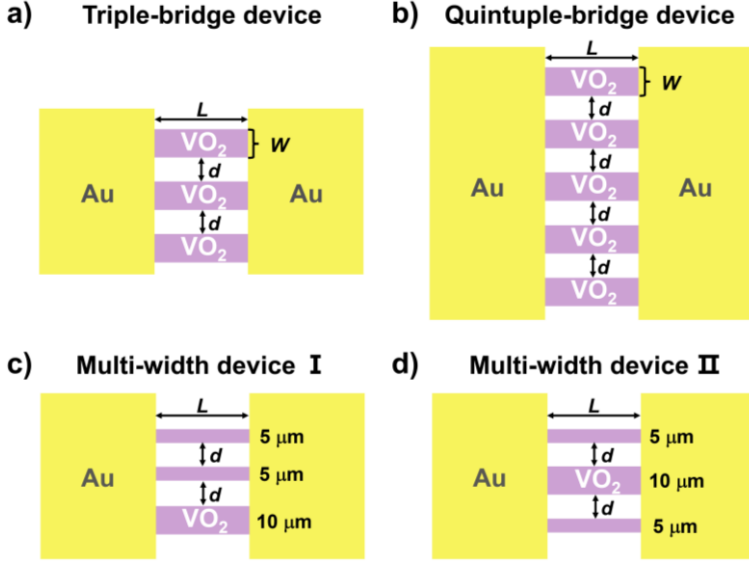
Figure 6.1 The schematic design of VO$_2$-based multi-bridge device (top view). (a) Triple-bridge devices. (b) Quintuple-bridge devices. (c) Multi-width bridge device I and (d) multi-width bridge device II. The width, W, length, L, and spacing d of the devices are as labeled.
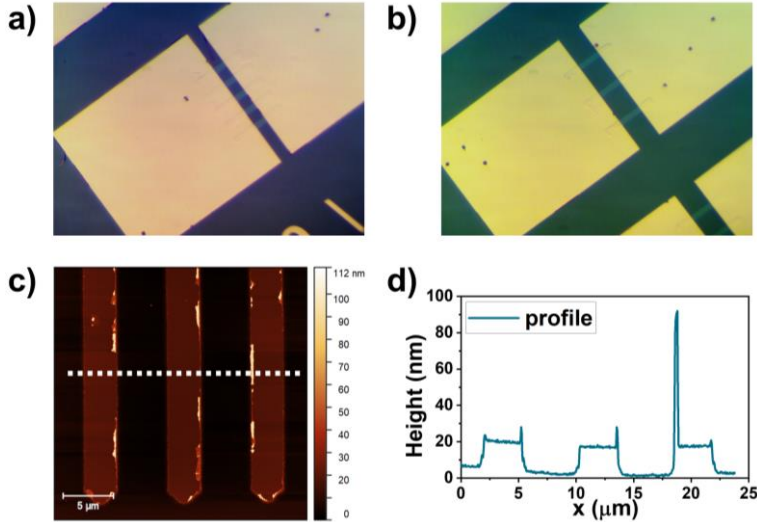

Figure 6.2 The as-fabricated VO$_2$ multi-bridge devices. (a) Optical photo of a quintuple-bridge device. (b) Optical photo of a triple-bridge device. (c) Surface topography map of a triple-bridge device ($W = 3$ μm, $L = 15$ μm, $d = 5$ μm). (d) Height profile of the white dashed line in (c).

The VO$_2$ multi-bridge devices were fabricated using the same procedure described in Chapter 4, with the bridges being etched by Ar ion milling. Microscope images of the as-fabricated quintuple-bridge and triple-bridge devices are displayed in Figure 6.2(a) and (b), respectively. The bridges have been effectively etched as the AFM line profile of a triple-bridge device (Figure 5.1(c) and (d)) indicating a step height of 15 nm, including approximately 11 nm of VO$_2$ film and 4 nm of TiO$_2$ substrate. The presence of large ears on some parts of the bridge edge results from the material redeposition during the Ar ion etching.

6.3 Electrical characterization

6.3.1   Devices with additional bridges

The addition of extra bridges will provide the potential for more switches and resistive states. Figure 6.3 shows the electrical characterization of triple-bridge devices with different d. The voltage-sweep curves are presented to demonstrate their close agreement with the current-sweep curves during the reset process. The primary focus is on the current-sweep curves, as in both Figure 6.3(a) and (b) these curves show three distinct snapbacks during the set process with a maximum of four stable resistive states. These states are reproducible over multiple cycles, as illustrated in Figure 6.3(c). However, in contrast to the *I-V* curves for double-bridge devices in the previous chapter, which exhibit sharp snapbacks for the set and distinct turns for the reset, the *I-V* curves for these triple-bridge devices show more nonlinear behavior at low currents during the set and vague turns during the reset. This is a result of growing competition among bridges, and its implications are further discussed in this chapter.

The switching power for each snapback and the power difference have been calculated and plotted in Figure 6.3(d). P_1 has been found to be independent of d while P_2 and P_3 increase with d, showing the same trend as for double-bridge devices. The required power for the second snapback (ΔP_{12}) also correlates with d, resulting from the weakened thermal crosstalk effect as the spacing between the bridges increased. An interesting phenomenon occurs when calculating the power for the third snapback (ΔP_{23}). For bridges with small d (5, 10, and 15 μm), ΔP_{23} followed the same trend as ΔP_{12}. However, for bridges with large d (20 and 30

μm), ΔP_{23} deviates from the trend and begins to decrease. Therefore, the actual situation for the third switch remains unclear, especially for the large-spacing bridges. A better understanding will be achieved once we perform SThM scans to visualize the switching dynamics.
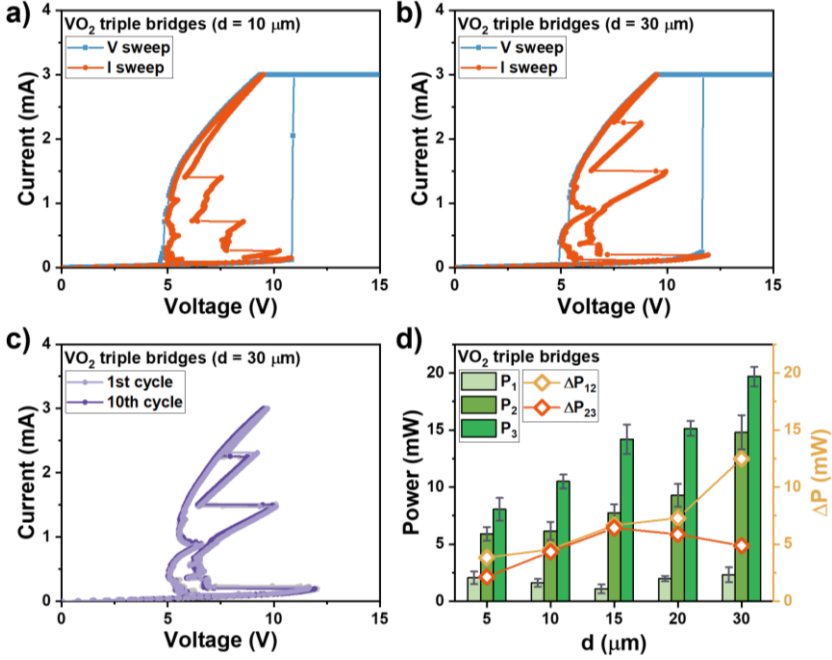

Figure 6.3 Voltage-controlled and current-controlled *I-V* characteristics of triple-bridge devices ($W = 5$ μm, $L = 20$ μm) with different d: (a) 10 μm and (b) 30 μm. $I_{CC} = 3$ mA. (c) Current-controlled *I-V* characteristics of triple-bridge device ($W = 5$ μm, $L = 20$ μm, $d = 30$ μm) for 10 cycles. (d) Switching power (P) and power differences (ΔP) of current-controlled measurements as a function of d. Subscripts 1, 2 and 3 stand for the first, the second and the third snapback, respectively. $\Delta P_{12} = P_2\text{-}P_1$, $\Delta P_{23} = P_3\text{-}P_2$.

To achieve even more switches within a single device, two more bridges are incorporated based on the triple-bridge device, creating a quintuple-bridge configuration. Figure 6.4(a) and (b) show the *I-V* curves for a quintuple-bridge device ($W = 5$ μm, $L = 20$ μm, $d = 20$ μm), which exhibits reproducible five distinct snapbacks during the set process with the NDR after the first switch, yielding a maximum of six stable resistive states. Figure 6.4(c) displays the switching power for each snapback (P_1, P_2, P_3, P_4 and P_5). The power values for the first

three snapbacks (P_1, P_2 and P_3) are found to be independent of the spacing, while P_4 and P_5 show a correlation with the spacing. Once again, there is no clear trend regarding the required power for subsequent switches (ΔP_{12}, ΔP_{23}, ΔP_{34}, ΔP_{45}) as the number of bridges increases, resulting in more possible combinations of ON-state and OFF-state bridges. Therefore, the bridge status and switching features are not as straightforward as illustrated in Figure 5.3.
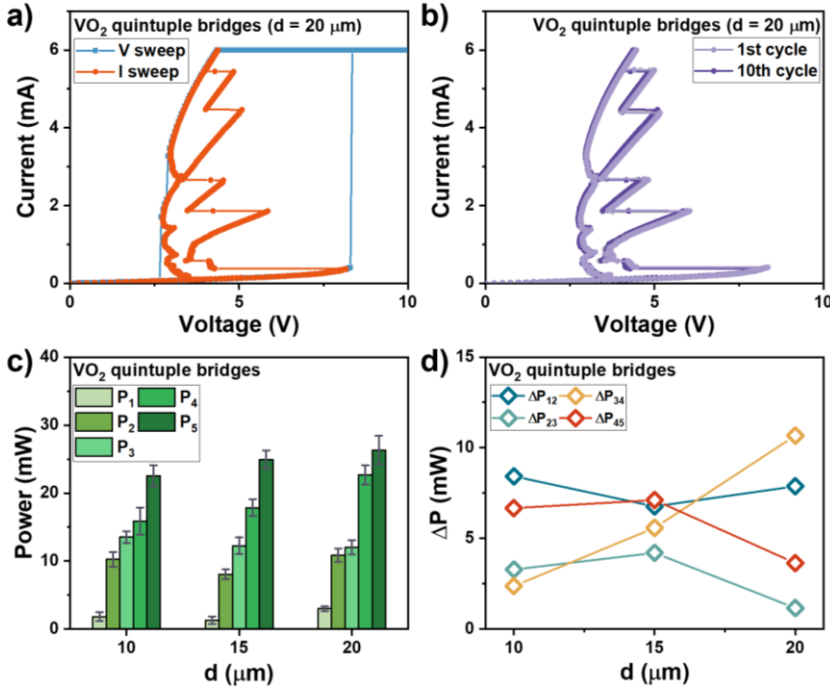

Figure 6.4 (a) Voltage-controlled and current-controlled *I-V* characteristics and (b) current-controlled *I-V* characteristics for 10 cycles of quintuple-bridge devices ($W = 5$ μm, $L = 20$ μm, $d = 20$ μm). $I_{CC} = 6$ mA. (c) Switching power (P) of current-controlled measurements as a function of spacing (d). Footnotes 1 to 5 stand for the first to the fifth snapback, respectively. (d) Power differences (ΔP) of current-controlled measurements as a function of spacing (d). $\Delta P_{12} = P_2\text{-}P_1$, $\Delta P_{23} = P_3\text{-}P_2$, $\Delta P_{34} = P_4\text{-}P_3$, $\Delta P_{45} = P_5\text{-}P_4$.
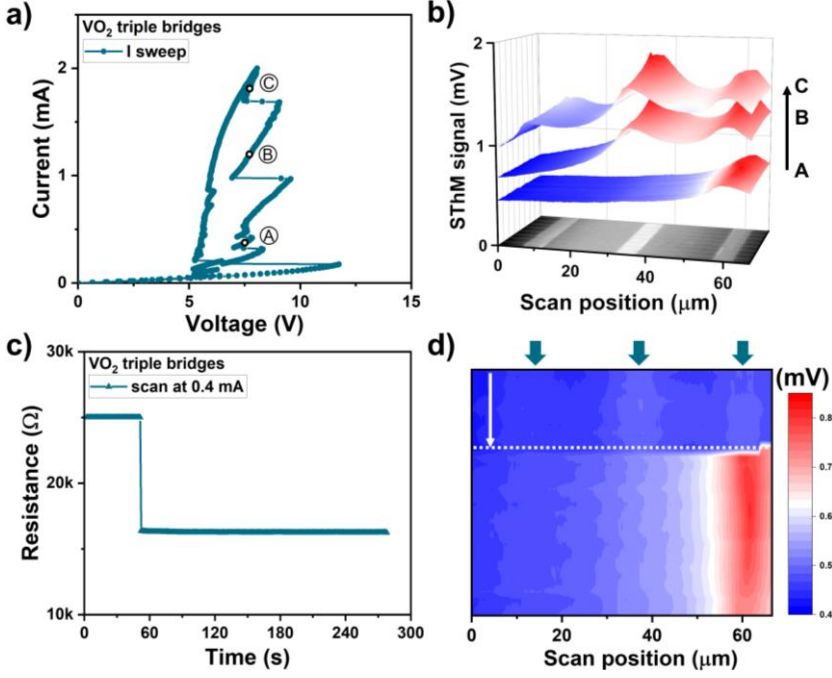
Figure 6.5 (a) Current controlled *I-V* characteristics and (b) 3D SThM thermal maps of a VO$_2$-based triple-bridge device ($L = 20$ µm, $W = 5$ µm, $d = 20$ µm). The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1.2 mA, C: 1.8 mA. (c) Resistance plots of the device during the SThM scan at 0.4 mA. (d) 2D SThM thermal map of the scan at 0.4 mA. The green arrows show the bridge position. The white arrow indicates the scan direction, and the white dashed line indicates the switching point of the resistance.

To gain more insight on the switching dynamics, SThM thermal maps were measured for each resistive state in several triple-bridge devices and quintuple-bridge devices. Figure 6.5(a) and (b) show the results for a triple-bridge device ($L = 20$ µm, $W = 5$ µm, $d = 20$ µm). It is observed that the bridges are switched in a sequential order, from right bridge (scan A) to the central bridge (scan B) and finally to the left (scan C) as the applied current increases, corresponding to the individual snapbacks in the *I-V* curve. Additional attention has been paid to the low current range as there are several small switches before reaching a stable resistance. Prior to scan A with a current bias of 0.4 mA, an SThM scan was taken using the same current bias. The resistance of the device suddenly drops from 25 kΩ to 16 kΩ and then stabilizes during the scan (Figure 6.5(c)). The resulting heating map is shown in Figure 6.5(d), with the

white arrow indicating the scan direction and the white dashed line indicating the switching point of the resistance. Heating paths were observed in the central and right bridges until the white dashed line, after which the right bridge dominates the current and produces a significant amount of heat. Consequently, the nonlinear behavior at low currents is caused by competition among the bridges.
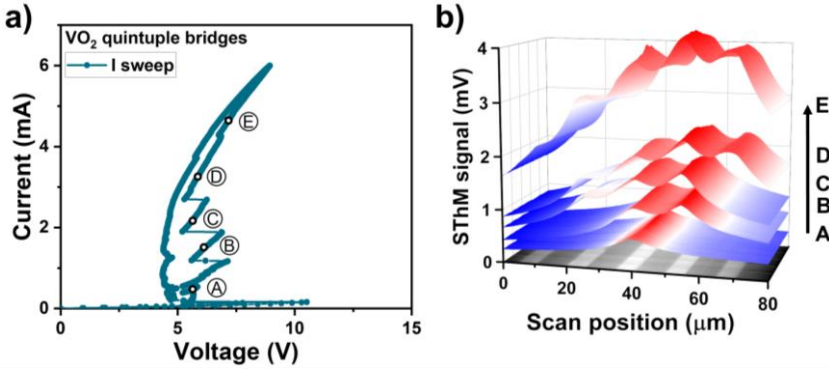

Figure 6.6 (a) Current controlled *I-V* characteristics and (b) 3D SThM thermal maps of a VO$_2$-based quintuple-bridge device ($L = 15$ μm, $W = 5$ μm, $d = 10$ μm). The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1.4 mA, C: 2.2 mA, D: 3.3 mA: E: 4.9 mA.

Figure 6.6(b) illustrates the SThM thermal maps for each resistive state (marked in Figure 6.6(a)) in a quintuple-bridge device ($L = 15$ μm, $W = 5$ μm, $d = 10$ μm). In this case, the bridges are switched individually in a different order. Since the bridges are closer than the previous triple-bridge device, the central bridge receives most heating from its neighbors and is switched first (scan A). Subsequently, its neighboring bridges to the right and left are switched (scan B and C), followed by the bridges at the edges (scan D and E). In scan E, the thermal peak on the left edge bridge is less pronounced than the previous scans because most of the current is already dominated by the ON-state bridges at this point.

To be noted, for both triple- and quintuple-bridge devices, the subsequent switch is highly likely to occur in the neighboring bridge of the ON-state bridge when $L > d$. While for $L <\sim d$, stochasticity can be induced and will be further discussed. This observation provides proof that thermal crosstalk is the main influential factor for the sequential switching process.
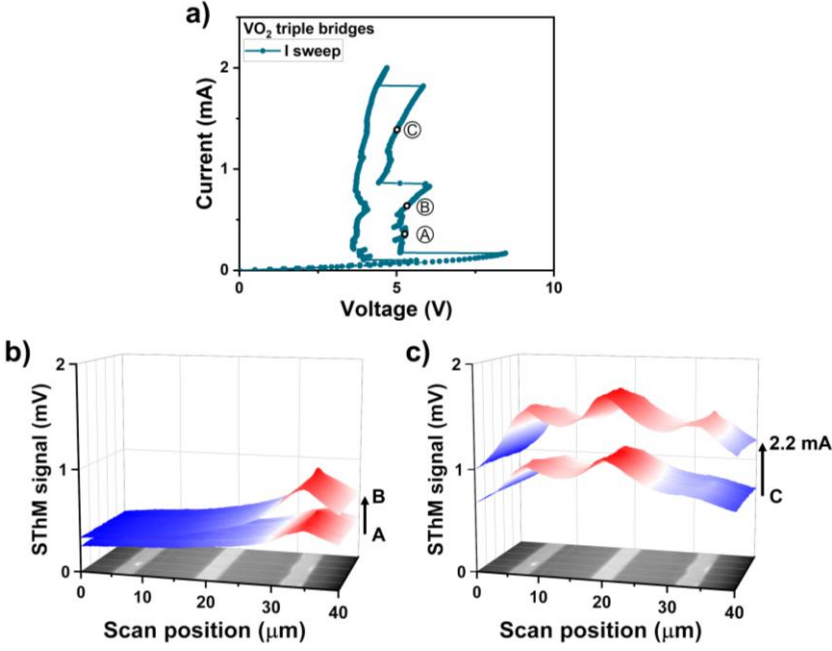
Figure 6.7 (a) Current-controlled *I-V* characteristics and (b)(c) 3D SThM thermal maps during the set process of a VO$_2$-based triple-bridge devices ($L = 10$ μm, $W = 3$ μm, $d = 10$ μm). The points where SThM measurements were taken are labeled as follows; A: 0.35 mA, B: 0.65 mA, C: 1.4 mA, and 2.2 mA.

Increasing the number of switching elements in the device presents a promising opportunity to achieve more resistive states while maintaining the switching principles. However, the growing number of VO$_2$ bridges also raises complexity and uncertainty. As can be seen in the *I-V* characteristics of the multi-bridge devices, there is nucleation within individual bridges and competition among bridges leading to chaotic behaviors in the low current range prior to achieving the first stable intermediate state. Moreover, revealed by the SThM scans, the switching behavior after the first switch is also complicated. For example, though the current-sweep *I-V* curve for a triple-bridge device ($L = 10$ μm, $W = 3$ μm, $d = 10$ μm) in Figure 6.7(a) also shows three distinct snapbacks, while the order of the switching bridge is completely different from the one in Figure 6.5(a). As shown in Figure 6.7(b) and (c), the right bridge is set first (scan A and B), then for the second snapback, the other two OFF-state bridges are switched ON simultaneously while the right bridge is switched OFF, surprisingly (scan C). Finally, the right bridge is switched ON again creating the third snapback (scan at 2.2 mA).
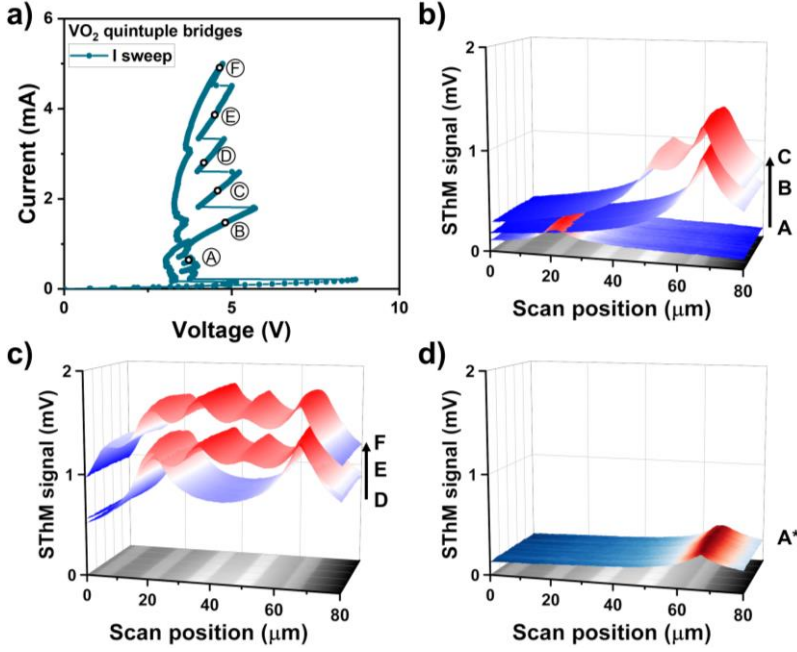
Figure 6.8 (a) Current-controlled *I-V* characteristics and (b)(c)(d) 3D SThM thermal maps during the set process of a VO$_2$-based quintuple-bridge devices (*L* = 10 μm, *W* = 5 μm, *d* = 10 μm). The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1.4 mA, C: 2.2 mA, D: 2.8 mA, E: 3.7 mA, F: 4.9 mA. The SThM scan A* in d) was taken after scan F, at 0.4 mA. A different color scheme is employed in d) to distinguish scan A* from the previous round of scans.

A more complex phenomenon is observed in a quintuple-bridge device (*L* = 10 μm, *W* = 5 μm, *d* = 10 μm) with distinct five snapbacks in the *I-V* curve (Figure 6.8(a)). The SThM thermal maps in Figure 6.8(b) and (c) show that the second bridge from the left is set first (scan A), but during reaching a stable resistive state, it loses the competition to the fifth bridge (scan B). Then the fourth bridge is triggered due to the thermal assistance of the ON-state fifth bridge (scan C). However, for the third snapback, the fourth bridge is switched OFF whereas the second bridge is switched ON again at the same time (scan D). Subsequently, the two bridges in between the second and fifth ones are triggered with the same current (scan E) as they both receive heating from their neighbors. Finally, the last remaining bridge on the left is also switched ON with increasing current. To investigate the repeatability of the behavior in the low current range, an additional round of SThM scan is performed after scan

F (Figure 6.8(d)). This time the fifth bridge is set first without competing with the second one (scan A*) and the scans at higher currents stay the same. The first switched bridge can be different during cycling. We remark that this phenomenon is not seen in many devices, as it can already be induced in the initial forming.

As discussed above, due to the additional complexity, the intrinsic switching behavior is not always as straightforward as the current-controlled *I-V* characteristic would indicate. The competition among the nominally identical bridges for the first switch makes the set process in the low current range chaotic, leading to the unpredictable first switched bridge. Furthermore, more than one bridge can be switched ON simultaneously, sometimes accompanied by an ON-state bridge back to the OFF state. The surprising observation of an apparently stochastic order of switching when $L <\sim d$ cannot be explained fully by thermal crosstalk between steady-state bridges. We theorize that local thermal fluctuations could drive the observed stochasticity, which will be the subject of further research. This complexity may be further optimized and utilized in applications, for example in finite-state machine devices[133].

6.3.2   Devices with multi-width bridges

So far, all the bridges in one device have been identical in terms of their dimensions, including length, width and spacing. However, as mentioned in the previous section, competition between identical bridges can severely lead to unpredictable inherent switching behavior. The geometry of bridges highly influences the switching behavior, as it affects the initial resistance, the required switching power, and the generated heating of the bridges. Therefore, placing bridges with different widths into a single device allows for a higher degree of control over the switching behavior, especially for the first switch.
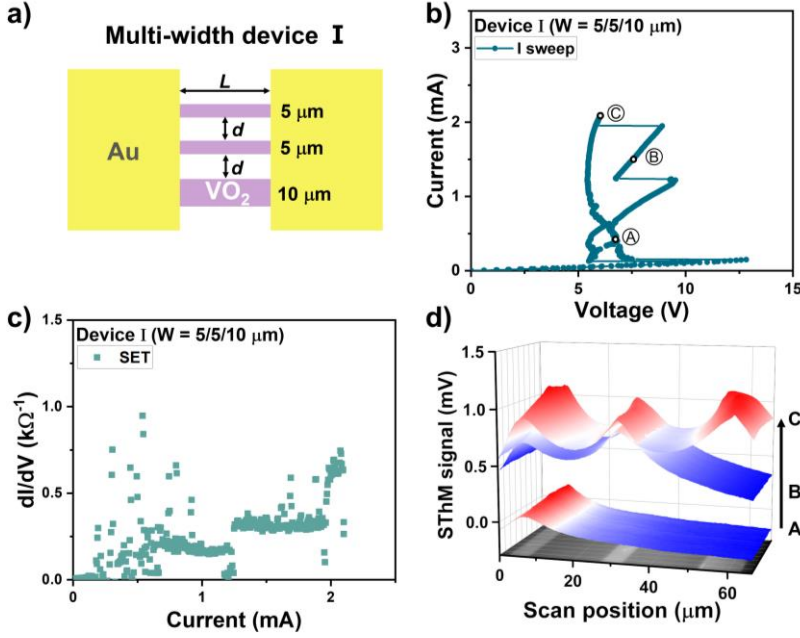
Figure 6.9 (a) Schematic of Device I ($L = 20$ μm, $W = 5/5/10$ μm, $d = 20$ μm) (top view). (b) Current-controlled *I-V* characteristics and (c) *dI/dV* plots of Device I. (d) 3D SThM thermal maps during the set process for Device I. The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1.5 mA, C: 2.2 mA.

The electrical measurements and SThM scans were carried out on mainly two types of multi-width triple-bridge devices. These devices contain bridges with the same *L* (20 μm) and *d* (20 μm), but different *W* and placing order. The wider bridge is placed at the edge of Device I (Figure 6.9(a)) while in the middle of Device II (Figure 6.10(a)). During the current-controlled measurements, they both show three snapbacks, though the trend of the curves differs. The third snapback of Device I (Figure 6.9(b)) is more intense and occurs at a lower current compared to Device II (Figure 6.10(b)). The *dI/dV* plots of the set process in Figure 6.9(c) contains three steps, representing three available current paths in Device I. The first two steps are of equal height while the third step is twice as high, suggesting the two 5 μm-wide bridges are switched first followed by the 10 μm-wide bridge. The SThM thermal maps in Figure 6.9(d) confirmed this switching sequence, from the narrow bridge on the left (scan A) to the narrow bridge in the middle (scan B) and finally the wide bridge on the right (scan C). In contrast, the *dI/dV* plots of Device II in Figure 6.10(c) are more scattered and there are

only two steps with different height. The SThM measurements in Figure 6.10(d) reveal its switching dynamics. The left 5 μm-wide bridge is triggered first (scan A) and maintained ON with increasing current until the device reaches a steady resistive state (scan B). However, for the second snapback, the left bridge is switched OFF and at the same time the 10 μm-wide one in the middle is triggered (scan C). Increasing the current further, the left 5 μm-wide bridge is switched ON again while the right one remains OFF (scan at 3.5 mA). Both devices show an intriguing phenomenon where the 10 μm-wide, once set, becomes the primary pathway for most of the current flow due to its lower resistance.
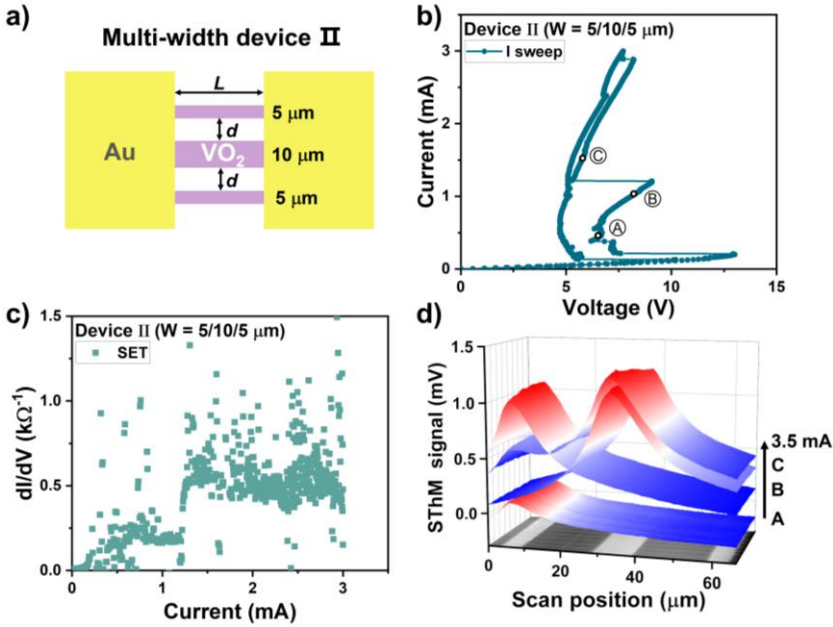
Figure 6.10 (a) Schematic of Device II ($L = 20$ μm, $W = 5/10/5$ μm, d = 20 μm) (top view). (b) Current-controlled *I-V* characteristics and (c) *dI/dV* plots of Device II. (d) 3D SThM thermal maps during the set process for Device II. The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1 mA, C: 1.5 mA, and 3.5 mA.

Figure 6.11 (a) Schematic of Device I (L = 20 μm, W = 5/5/10 μm, d = 5 μm) (top view). (b) Current-controlled *I-V* characteristics and (c) 3D SThM thermal maps during the set process for D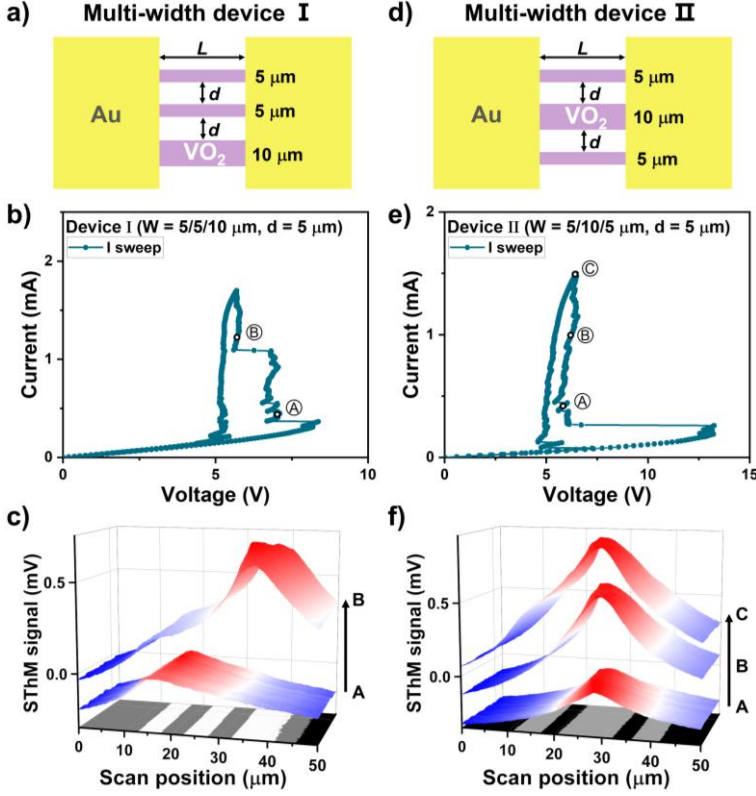evice I. The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1.2 mA. (d) Schematic of Device II (L = 20 μm, W = 5/10/5 μm, d = 5 μm) (top view). (e) Current-controlled *I-V* characteristics and (f) 3D SThM thermal maps during the set process for Device II. The points where SThM measurements were taken are labeled as follows; A: 0.4 mA, B: 1 mA, C: 1.5 mA.

Moreover, in the case of multi-width bridge devices, the spacing between the bridges still plays an important role. To investigate this further, two more devices with the same bridge arrangement as in Device I and Device II, but with a smaller d (5 μm), were fabricated and subjected to measurements. The current-sweep *I-V* curves in Figure 6.11(b) and (e) exhibit fewer snapbacks for both devices, indicating that there is simultaneous switching among the bridges due to the significant thermal crosstalk effect, as expected. The SThM thermal maps in Figure 6.11(c) illustrate the switching dynamics of Device I, where both 5 μm-wide bridges

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are switched simultaneously for the first snapback (scan A), and for the second snapback, the 10 µm-wide bridge is switched and takes over most of the current (scan B). On the other hand, the SThM thermal maps of Device II (Figure 6.11(f)) reveal that the major snapback in the *I-V* curve is contributed by the 10 µm-wide bridge located in the middle, as it receives thermal assistance from both neighboring bridges. When the current increases further, the 5 µm-wide bridge on the left is also switched, but it only results in a small pump in the heating profile. Although measurements were not conducted, it is anticipated that the remaining 5 µm-wide bridge will switch with higher currents due to thermal assistance from the 10 µm-wide bridge. However, the resulting change in resistance is likely to be insignificant.

6.3.3   Influential Factors of the Resistive Switching Behaviors

In the parallel-bridge devices, there are several variables to manipulate the switching behaviors, including the intrinsic IMT properties of the VO₂ bridges, the configuration of the devices, and the operating temperature. There is also an interplay between these factors, as was shown in Section 5.3. The intrinsic IMT determines the required switching power and the resistive states of the device. However, by tuning the operating temperature, the switching characteristic and critical spacing for synchronized/sequential switching in multi-bridge devices can be changed. In this chapter, we focus on the structural manipulation at the device level so the configuration of the devices will be mainly discussed.

First, the number of the VO₂ bridge determines the maximum number of switches and resistive states. From single bridge to double bridges and further to quintuple bridges, by simply adding the switching elements, the device gains the potential for more resistive states. The principles for single-bridge devices can be extended to double-bridge and multiple-bridge devices. However, there is a limitation of the bridge amount due to the device-area efficiency and energy efficiency, which can be improved by shrinking the bridge to the nanoscale.

Moreover, as the number of the Joule heating-induced switching element increases, their thermal interaction becomes a significant factor influencing the switching behavior. Similar to the discussion in Chapter 5 for double-bridge devices, when the thermal crosstalk effect

dominates, simultaneous switching occurs. By increasing the spacing within a certain range, the bridges can be switched independently, allowing the full potential of the device to be exploited. The correlation between device length and spacing also impacts the switching behavior. As we observed, when $L <\sim d$, stochastic behavior can emerge, resulting in the required power of the subsequent switches appearing independent from the spacing. In contrast, when $L > d$, the thermal crosstalk effect causes subsequent switches to preferentially occur in the neighboring bridge of the ON-state bridge. Therefore, the bridge spacing determines the number of switching events and the potential switching bridge.

Finally, the geometry of bridges highly influences the switching behavior, as it affects the initial resistance, the required switching power, and the generated heating of the bridges. Although only two configurations have been investigated in this chapter, certain common trends have been observed. In the devices, narrow bridges tend to win the competition in the low current range and can be triggered first. This may be due to two possible reasons. First, they produce more Joule heating because of their large initial resistance. Second, the metallic domains in narrow bridges coalesce into a conducting path more easily. Additionally, once the wide bridges are switched ON, they dominate most of the current flowing through the device due to their low resistance at the LRS. However, this also raises the risk that the narrow bridges may not be able to maintain the ON state or may not be switched at all. Therefore, placing the wide bridge at the edge, as in Device I, may be a wise strategy.

6.4 Conclusion

In conclusion, the resistive switching behaviors of VO$_2$-based multi-bridge devices were investigated. The switching principle of single-bridge devices and double-bridge devices can be extended to multiple-bridge devices. The switching behavior can be manipulated at the device level by adjusting several key factors, including bridge numbers, bridge spacing and bridge geometry, which also interact with each other. With more bridges, there is potential to achieve more switches and resistive states. The spacing between bridges affects the number of switches and the potential switching bridge. Additionally, narrower bridges with higher initial resistance tend to be switched first while wider bridges with lower resistance dominate current flow once they are switched. Therefore, by assembling the VO$_2$ bridges and modifying the device configuration, novel switching behaviors and more controllable resistive states can be achieved in a two-terminal device, offering new possibilities for innovative electronics.

Chapter 7.

Miniaturizing to VO$_2$ nano-bridge devices

Based on the systematic study on microscale VO$_2$ parallel-bridge devices, we further miniaturize the bridges to several hundreds of nanometers in order to reduce the device dimensions and switching powers. The results show that the observed switching principles in microscale bridges are still applicable in the nanoscale devices, including single-bridge, double-bridge, and multi-bridge devices. A 'waterfall-like' multi-bridge configuration has been proposed to achieve more controllable switches in two-terminal electronics.

7.1 Introduction

In previous chapters, different device configurations were explored by adjusting the length, width, and spacing of microscale bridges. However, for the devices assembled by microscale bridges, the device dimensions and required switching power keep increasing in order to achieve more switches. Downsizing to the nanoscale can reduce these limitations, and the behavior of single-bridge, double-bridge, and multi-bridge devices at the nanoscale is discussed in this chapter.

Building on the results of the multi-width triple-bridge discussed in Chapter 6, a 'waterfall-like' multi-bridge configuration with bridges of varying widths arranged in a sequence from narrow to wide is proposed. It is expected that these devices could display a 'waterfall switching' from the narrowest bridge to the widest.

7.2 Device design and fabrication

After etching out microscale parallel bridges from the film, we continued to scale down the bridge size to a few micrometers or hundreds of nanometers, which included the single-bridge, double-bridge, and multi-bridge configurations. Figure 7.1 displays the designs of the multi-bridge devices, which are created with two considerations. The first one is to continue the study of multi-width triple-bridge devices. These devices contain bridges with identical L and d but varying W and different placing order, with the widest bridge placed at the edge of Device I (Figure 7.1(a)) and in the middle of Device II (Figure 7.1(b)). Another consideration is to create multiple-bridge devices containing bridges of different W, growing from one side to the other, such as the quintuple-bridge device in Figure 7.1(c) and the septuple-bridge device in Figure 7.1(d).
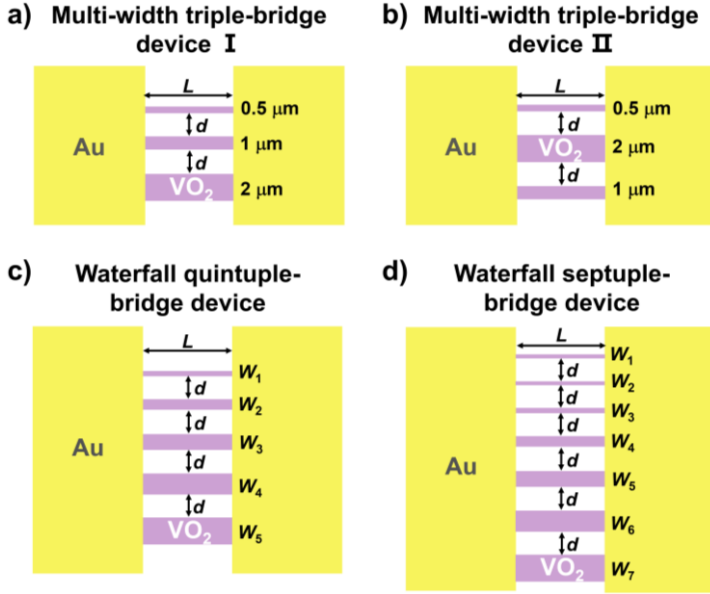
Figure 7.1 The schematic design of VO₂-based nano-bridge device (top view). (a) Multi-width triple-bridge device I, (b) multi-width triple-bridge device II, (c) waterfall quintuple-bridge device and (d) waterfall septuple-bridge device. The width, *W*, length, *L*, and spacing *d* of the devices are as labeled.

The fabrication process of the VO₂ nano-bridge devices followed a similar procedure as described in Chapter 4. To obtain features smaller than 1 μm, the electron beam lithography (EBL) technique was utilized to shape the film instead of the UV lithography. In the EBL process, positive PMMA-A4 950 photoresist was spincoated on top of the sample at 4000 rpm for 60 s and successively baked for 5 min on a hot plate at 160 °C. Afterwards, a conducting layer, AR-PC 5090.02, was coated on top of the sample at 2000 rpm for 45 s and successively baked for 2 min on a hot plate at 90 °C to prevent the insulating substrate from charging during the EBL process. The sample was then loaded into the Raith Electron Beam Pattern Generator (EBPG) 5150 machine and exposed to the electron beam accelerated by 100 kV voltage with a beam current of 2 nA and dose of 400 μC/cm². After the exposure, we first remove the conducting layer by bathing the sample in DI water for 60 s. The resist was developed in diluted MIBK solution (MIBK:IPA 1:3) for 45 s and subsequently cleaned in DI water for 30 s.

With the typical recipe for microscale bridges (Table 4.1), the etching rate of VO₂ film is

approximately 4 nm/min. However, if the same parameters are used the PMMA resist would be hardbaked and impossible to be removed due to the amount of heat generated during the bombardment. Therefore, in order to avoid this issue, a low-energy Ar ion milling was utilized for etching the nanoscale bridges. The settings for this process are listed in Table 7.1, where both the ion beam dose and the beam energy were reduced. However, there is still a risk of hardbaking the PMMA layer if the beam is applied continuously for 20 minutes. Instead, the beam was applied for 1 minute at a time and repeated 20 times, with 3-5 min in between to allow for heat dissipation, to fully etch away the unwanted VO_2 without burning the PMMA.

Parameter:	
Background pressure	4×10^{-4} mbar
Ion beam dose[1]	1.29×10^{15} ions/cm^2
Beam voltage	150 V
Beam current	25 mA
Etching angle	45º
Stage rotation speed	4 rpm
Etching time	20×1 min

Table 7.1 Ar ion milling parameters for VO_2 nano-bridge devices.

In Figure 7.2(a), an example of an as-fabricated single-bridge device (W = 0.15 μm, L = 5 μm) is shown. Similarly, in Figure 7.2(c), an example of a double-bridge device (W = 0.5 μm, L = 5 μm, d = 1 μm) is displayed. The bridges have been effectively etched as the AFM line profile indicating a step height of 15 nm for single bridge (Figure 7.2(b)) and 25 nm for double bridges (Figure 7.2(d)), including approximately 11 nm of VO_2 film and few

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[1] The ion beam dose is defined as the density of Ar ions per square centimeter for the operating duration. This value is obtained by dividing the beam current multiplied by Coulombs by the surface area of the beam. The diameter of the beam in the Ar etcher is 11 cm.
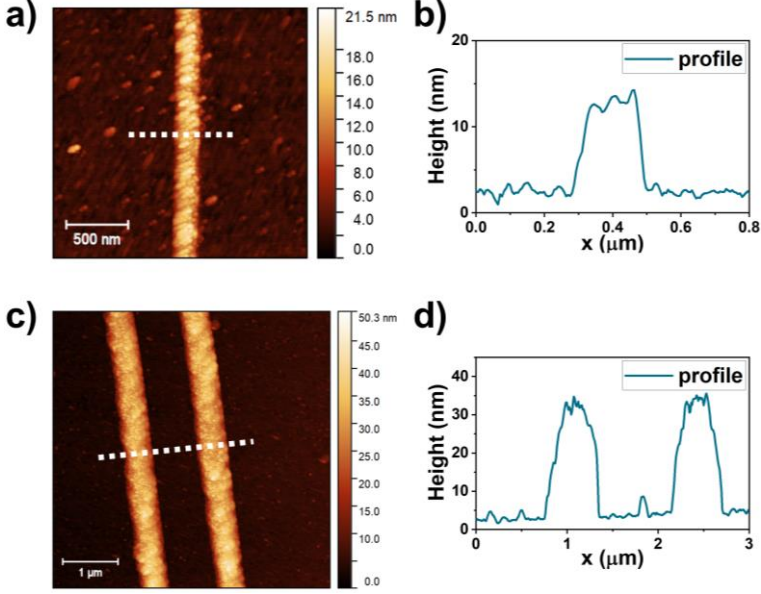
nanometers of TiO_2 substrate.

Figure 7.2 The as-fabricated VO_2 nano-bridge devices. (a) Surface topography map of a single-bridge device ($W = 0.15$ μm, $L = 5$ μm). (b) Height profile of the white dashed line in (a). (c) Surface topography map of a double-bridge device ($W = 0.5$ μm, $L = 5$ μm, $d = 1$ μm). (d) Height profile of the white dashed line in (c).

The multi-bridge devices were also fabricated well, for example, Figure 7.3 shows the AFM image of a septuple-bridge device ($W_1 = 0.2$ μm, $W_2 = 0.4$ μm, $W_3 = 0.6$ μm, $W_4 = 0.8$ μm, $W_5 = 1$ μm, $W_6 = 1.2$ μm, $W_7 = 1.4$ μm, $L = 5$ μm, $d = 0.5$ μm). The line-scan profile confirms that most bridges (indicated by the black dashed arrows) have been etched well with a height of approximately 12 nm, although the narrowest bridge on the right is not continuous or sufficient in height.
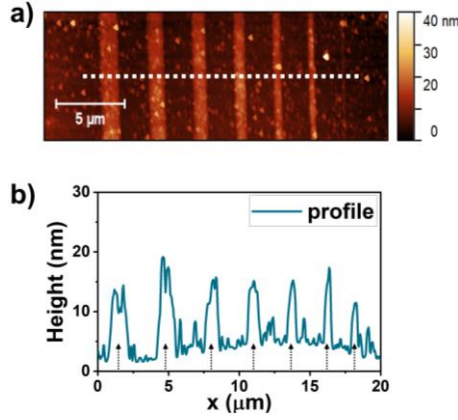
Figure 7.3 (a) Surface topography map of a septuple-bridge device ($W_1 = 0.2$ μm, $W_2 = 0.4$ μm, $W_3 = 0.6$ μm, $W_4 = 0.8$ μm, $W_5 = 1$ μm, $W_6 = 1.2$ μm, $W_7 = 1.4$ μm, $L = 5$ μm, $d = 0.5$ μm). (b) Height profile of the white dashed line in (a). The positions of the bridges are indicated by the black dashed arrows.

7.3 Electrical characterization

7.3.1 Temperature-dependent measurements

The temperature-dependent resistance (two-point resistance) of the nano-bridge devices has been measured using PPMS. Figure 7.4 shows the results of two single-bridge devices with L of 2 μm and 1 μm. The dR/dT for both heating and cooling cycle are calculated, and the heating branches are fitted with the Gaussian function. $R_{insulating}$ and $R_{metallic}$ and the transition temperatures are listed in Table 7.2. The transition of the devices is sharp with a resistance change of 2 orders of magnitude. The resistances of the single-bridge device scale with L, while the T_{IMT} and T_{MIT} remain constant.
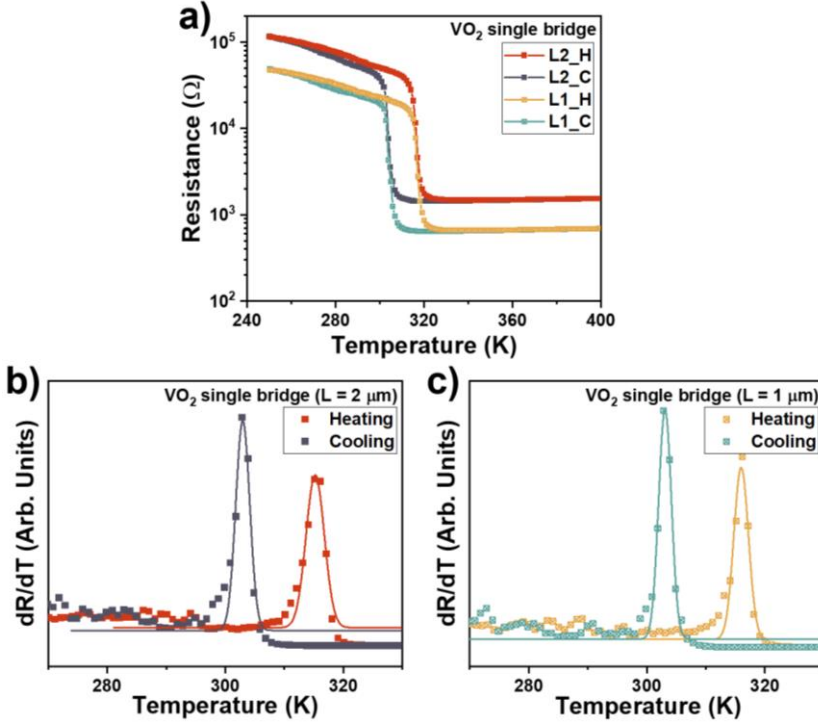
Figure 7.4 (a) Temperature dependence of the resistance of two nanoscale single-bridge devices (W= 1 μm, L = 2 and 1 μm). The dR/dT plots of the heating and cooling processes for device with L of (b) 2 μm and (c) 1 μm. The data of the heating branch are fitted using the Gaussian function.

L	2 μm	1 μm
$R_{\text{insulating}}$	105.9 kΩ	49.6 kΩ
R_{metallic}	1.5 kΩ	0.76 kΩ
T_{IMT}	315.9 K	315.2 K
T_{MIT}	302.9 K	303.1 K

Table 7.2 Resistance and transition temperature of the nanoscale single-bridge devices.

7.3.2   Resistive switching characterization

Electrical characterization was carried out on nanoscale single-bridge devices, double-bridge devices, and multi-bridge devices using voltage-controlled and current-controlled measurements. The nanoscale VO₂ bridges exhibit volatile switching behavior same as the

microscale bridges, and the switching principles are maintained such as the length-dependent switching power and the interaction among bridges, which will be elaborated further.
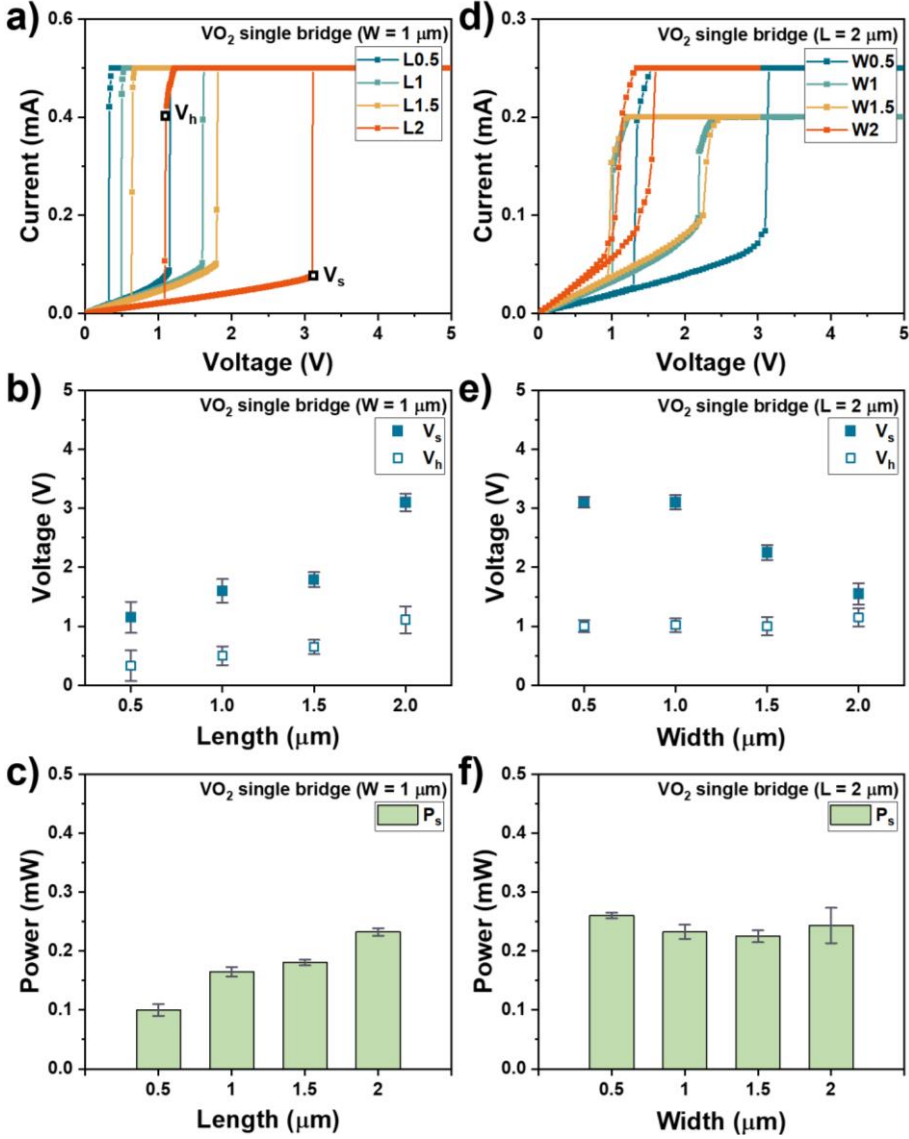
Figure 7.5 (a) *I-V* characteristics of four VO$_2$-based single-bridge devices ($W = 1$ μm) with different *L*. $I_{CC} = 0.5$ mA. (b) Set voltage (V_s) and hold voltage (V_h) as a function of *L* (c) Calculated set power (P_s) as a function of *L*. (d) *I-V* characteristics of four VO$_2$-based single-bridge devices ($L = 2$ μm) with different *W*. $I_{CC} = 0.2$ mA or $I_{CC} = 0.25$ mA. (e) V_s and V_h as a function of *W* (f) Calculated P_s as a function of *W*.

The switching behavior and the formed conducting channel in the bridge is dependent on the bridge geometry. Figure 7.5 displays the voltage-sweep *I-V* curves for single-bridge devices and the setting parameters extracted from the curves. The curves in Figure 7.5(a) were obtained on the devices with identical W (1 μm) but varying L (0.5, 1, 1.5, 2 μm). As illustrated in Figure 7.5(b) and (c), V_s and P increase with L. A longer device corresponds to a higher initial resistance; hence, more power is required for the switch. The *I-V* curves of devices with same L (2 μm) but varying W (0.5, 1, 1.5, 2 μm) were also measured and plotted in Figure 7.5(d). V_s reduces as W increases while the overall P remains constant irrespective of W. The results are in accordance with the previous findings of Yoon et al., who reported a linear relationship between device length and the conductive channel size, but no significant correlation between device width and the conductive channel size[134,135].

The switching behavior and the retention of the conducting channel is also influenced by the applied current bias. Figure 7.6 shows both the voltage-sweep and current-sweep the *I-V* curves of a single-bridge device (W = 0.8 μm, L = 2 μm). When a low I_{CC} is applied for the voltage sweep, the device is reset to HRS immediately after the voltage drops below V_s, and there is almost no hysteresis window. However, the current-sweep curve exhibits different behavior. After the snapback, the device enters an NDR range, which is reproducible for 100 cycles as shown in Figure 7.6(b). Once the I_{CC} increases to 0.3 mA, the voltage-sweep curve contains a larger hysteresis span, and V_h is much lower than V_s. For the current-controlled measurements, the *I-V* curves exhibit a large NDR region after the snapback, and the curves show cycle-to-cycle variation as shown in Figure 7.6(d). With lower current, the conductive channel in the bridge is narrow and can easily break once the power is reduced. When a higher current is applied, the conductive channel grows wider, leading to the slow relaxation process that produces hysteresis *I-V* curves. It is surprising that the nonlinear properties, such as the NDR regions during and set and reset process, are more pronounced for nanoscale bridges than for microscale bridges. One possible reason could be that the reduced dimensions amplify the effect of switching, so that even one domain switches will cause significant change of the electrical and thermal conductivity. Additionally, the instability of the conductive channel can enhance the nonlinear behavior.
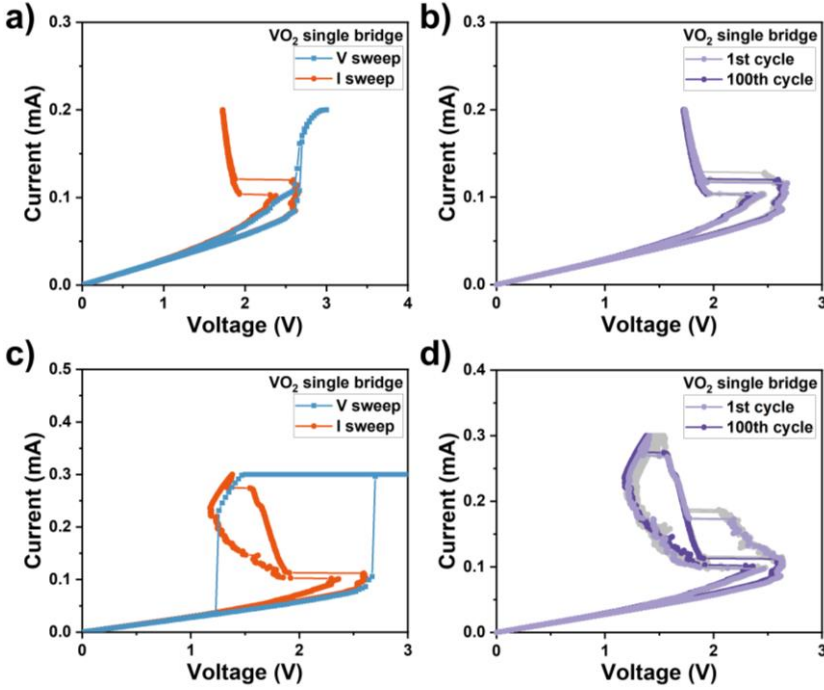
Figure 7.6 (a) Voltage-controlled and current-controlled *I-V* characteristics of a single-bridge device ($W = 0.8$ μm, $L = 2$ μm) with a current limitation of 0.2 mA. (b) Current-controlled measurement for 100 cycles. (c) Voltage-controlled and current-controlled *I-V* characteristics of the same device with a current limitation of 0.3 mA. (b) Current-controlled measurement for 100 cycles.

Similar to the double-bridge devices at the microscale level, the thermal interaction between the nanoscale bridges has been investigated. Two nanoscale double-bridge devices with different d were measured with voltage sweep and current sweep, and the resulting *I-V* curves are shown in Figure 7.7. For the device with $d = 0.2$ μm, the current-sweep curve exhibits a significant NDR region followed by one snapback, indicating that the bridges are in great competition and interact with each other, leading to the simultaneous switching. As d is increased to 1 μm, the bridges are switched individually, with several NDR regions during the first snapback, before and after the second snapback. Figure 7.7(c) shows the correlation between the switching power and the d. It is observed that P_1 is not strongly affected by d while P_2 is correlated with d and is larger than P_1. Moreover, ΔP is proportional to d, suggesting that more power is required for the secondary switch when the spacing increases

due to reduced thermal crosstalk effect. It should be noted that the switching power of nanoscale double-bridge devices has decreased by two orders of magnitude compared to that of microscale devices.
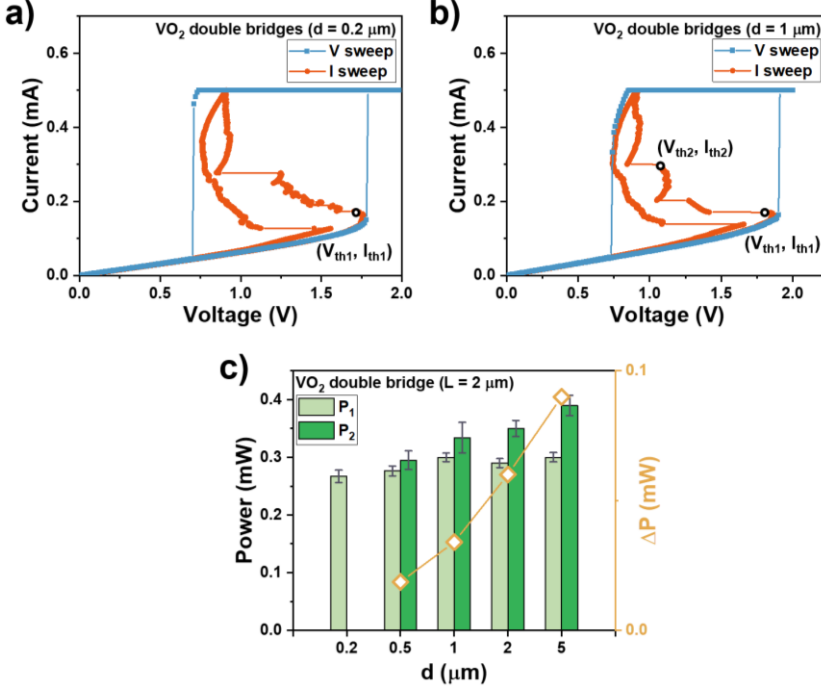

Figure 7.7 Voltage-controlled and current-controlled I-V characteristics of double-bridge devices ($W = 0.5$ μm, $L = 2$ μm) with different d: (a) 0.2 μm and (b) 1 μm. $I_{CC} = 0.5$ mA. (c) The calculated switching power (P) and the power difference (ΔP) between the first and the second snapback. Subscripts 1 and 2 stand for the first snapback and the second snapback, respectively.

Similar to microscale devices, two types of multi-width triple-bridge devices were fabricated. These devices contain bridges with the same L (10 μm) and d (10 μm), but different W and order. The widest bridge is placed at the edge of Device I (Figure 7.8(a)) while in the middle of Device II (Figure 7.8(d)). Voltage-controlled and current-controlled measurements were performed on both devices. During the voltage sweep, they show two jumps during the set process, however, the second switch of Device I (Figure 7.8(b)) occurs at a higher voltage compared to Device II (Figure 7.8(b)). Furthermore, the reset branch of Device I shows more intermediate resistive states than that of Device II.
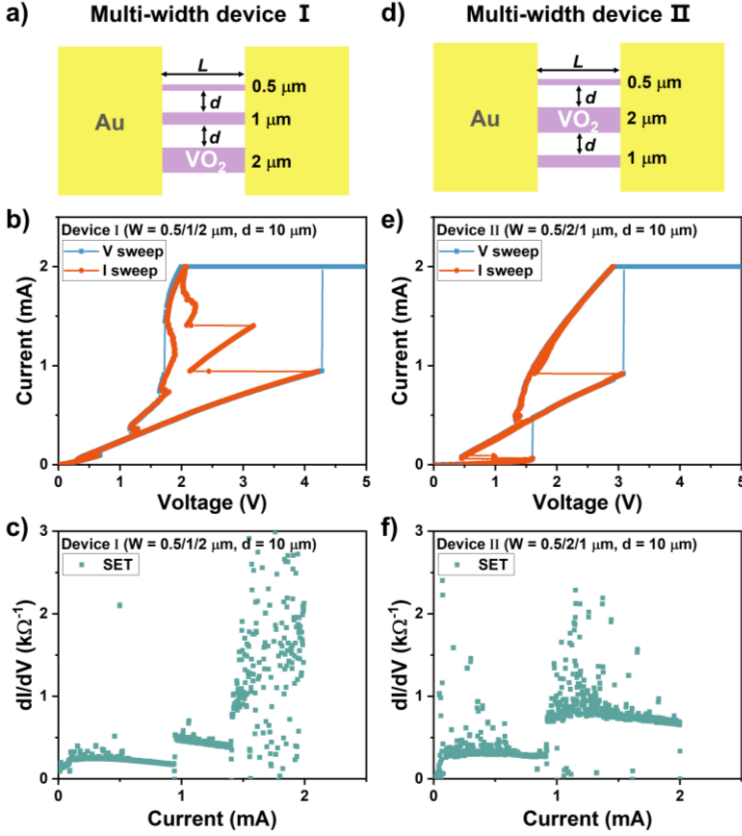
Figure 7.8 (a) Schematic of Device I ($L = 10$ μm, $W = 0.5/1/2$ μm, $d = 10$ μm) (top view). (b) Voltage-controlled and current-controlled I-V characteristics and (c) dI/dV plots of the set process for Device I. (d) Schematic of Device II ($L = 10$ μm, $W = 0.5/2/1$ μm, $d = 10$ μm) (top view). (e) Voltage-controlled and current-controlled *I-V* characteristics and (f) dI/dV plots of the set process for Device II.

In terms of the current-sweep curves, the primary difference is that Device I shows three snapbacks, while Device II only shows two. The dI/dV plots of the set process in Figure 7.8(c) contains three steps, though the third step is very scattered due to the NDR region in curve, representing three available current paths in Device I. The height of each step is double the height of the previous one, which is consistent with the width difference of Device I, indicating that the bridges are switched from the narrowest one to the widest one. In contrast, the dI/dV plots of the set process for Device II in Figure 7.8(f) contains two steps, where the second step has a height that is three times greater than the first one. The height difference in

the *dI/dV* plots can be interpreted in two ways with respect to the switching dynamics. One is the 0.5-µm bridge is switched first followed by the 2-µm bridge, which dominates the current flow, and at the same time the narrowest bridge returns to the OFF state. The second interpretation proposes that the 1-µm bridge is switched first, followed by the 2-µm bridge, and the 0.5-µm bridge remains in the OFF state. Though the switching dynamics of Device II is not yet fully understood, it is evident that once the widest bridge is switched, it will become the primary pathway for the current flow, which could impede the subsequent bridge from switching.

Figure 7.9 (a) Voltage-controlled and current-controlled *I-V* characteristics (b) current-sweep curves for 100 cycles and (c) *dI/dV* plots of Device I with *d* = 1 µm.

Thermal interaction also has a significant impact on the number of switches in multi-width triple-bridge devices. To investigate it, Device I with a smaller *d* (1 µm) was fabricated and measured. As shown in Figure 7.9(a), the voltage-sweep curve already exhibits several small jumps during the set process and intermediate resistive states during the reset process. As for the current-sweep curves in Figure 7.9(b), there are two major switches with few small

snapbacks during the set process. It is more obvious in the *dI/dV* plots shown in Figure 7.9(c), that there are two major steps, with the first one being a gradual increase and the second one being a sharp jump. This indicates that the bridges are highly interacting with each other due the strong thermal cross talk effect, leading to the chaotic nucleation process in the low current range and simultaneous switching behavior.
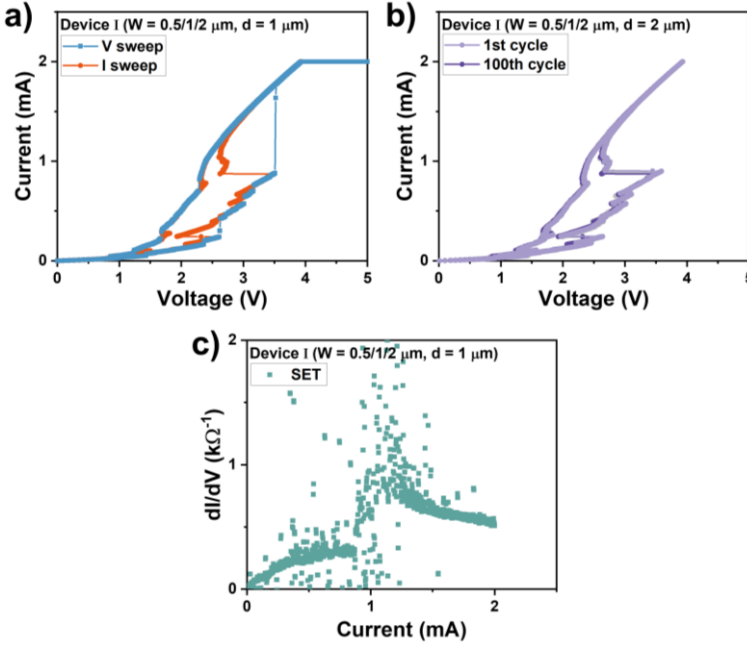

Figure 7.10 (a) Voltage-controlled and current-controlled *I-V* characteristics (b) current-sweep curves for 100 cycles and (c) *dI/dV* plots of a waterfall quintuple-bridge device (W = 0.5/1/1.5/2/4 µm, L = 10 µm, d = 5 µm).

To investigate the feasibility of manipulating the switching behavior of VO_2 parallel-bridge devices through device configuration, nanoscale 'waterfall-like' multi-bridge devices were fabricated and measured. Anticipated behavior of these devices is that they may exhibit a sequential switching from the narrowest bridge to the widest, resembling a 'waterfall switching'.

Figure 7.10 shows an example of a 'waterfall-like' quintuple-bridge device with a W series of 0.5, 1, 1.5, 2, and 4 µm. The voltage-sweep curve in Figure 7.10(a) contains four jumps during the set process and three intermediate resistive states during the reset process. As for

the current-sweep curves, there are five distinct switches and six stable resistive states that remain reproducible for over 100 cycles (Figure 7.10(b)). Moreover, the dI/dV plots in Figure 7.10(c) contains five steps and the height of each step (0.45, 0.9, 1.35, 1.8, and 3.6) is proportional to the bridge width, indicating sequential switching from the narrowest to the widest bridge.
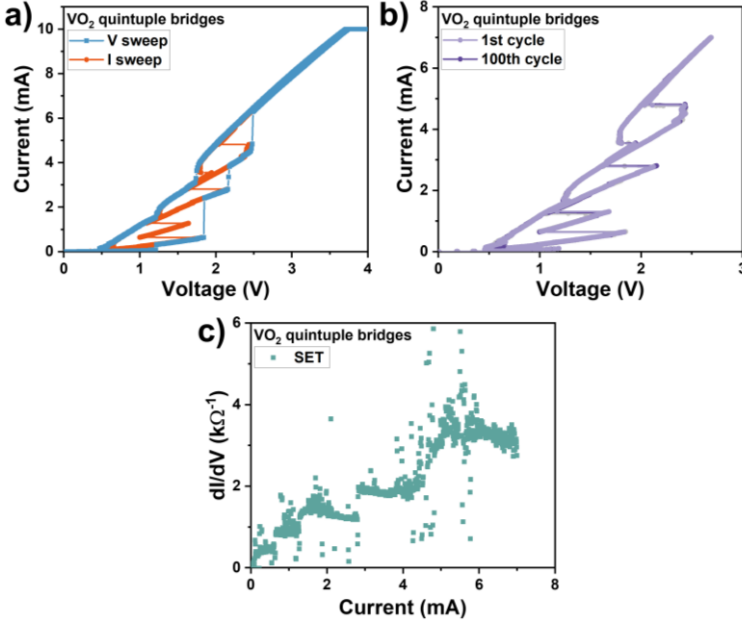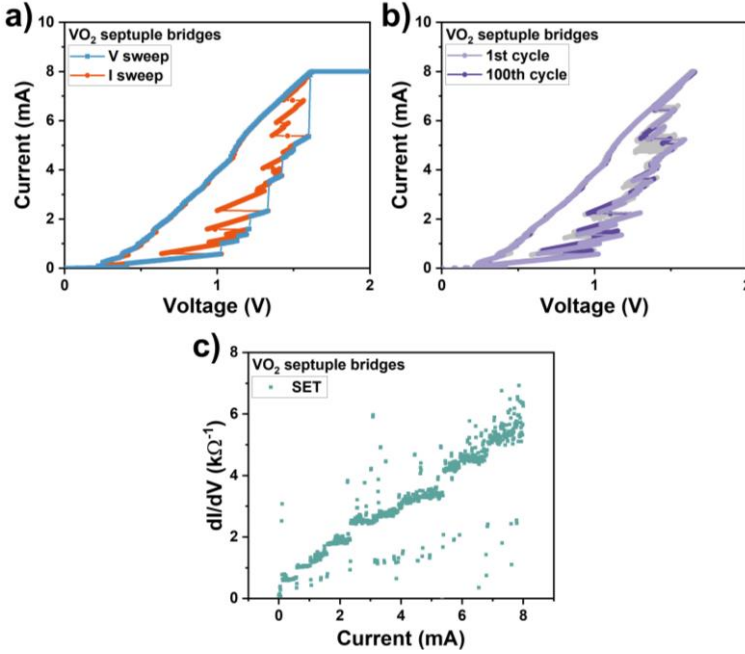

Figure 7.11 (a) Voltage-controlled and current-controlled I-V characteristics (b) current-sweep curves for 100 cycles and (c) dI/dV plots of a waterfall septuple-bridge device (W = 0.2/0.4/0.6/0.8/1/1.2/1.4 μm, L = 5 μm, d = 1 μm).

With the optimism of achieving more controllable switches in the VO₂ parallel-bridge devices, we have extended the number of bridges to 7 and created a septuple-bridge device with a W series of 0.2, 0.4, 0.6, 0.8, 1, 1.2, and 4 μm. The measured voltage-sweep and current-sweep curves in Figure 7.11(a) exhibit numerous small switches, and there is significant cycle-to-cycle variation during the current-controlled measurements, as seen in Figure 7.11(b). Moreover, the dI/dV plots in Figure 7.12(c) are very scattered with many small steps, including the gradual ones and sharp ones. As a result, it is challenging to determine the exact number of switches present and the actual switching dynamics. The small width difference

of 0.2 μm might lead to significant competition among the bridges, hindering the bridges from dominating the current flow. Additionally, the small spacing between the bridges would lead to strong thermal interactions, resulting in simultaneous switching behavior.

7.4 Conclusion

In conclusion, the resistive switching behaviors of VO_2-based parallel-bridge devices at the nanoscale has been investigated, including the single-bridge, double-bridge, and multi-bridge devices. The switching principles observed in microscale bridges can be maintained for nanoscale devices, with significantly reduced switching power. The geometry of single bridges, thermal interaction among the bridges, and the geometry of the bridges still have great effects on the switching behavior. The use of a 'waterfall-like' multi-bridge configuration has been proposed to achieve more controllable switches. Although there is still a lot of room for improving the device performance, two examples are presented in this chapter to demonstrate the potential of this approach for achieving multiple switches and controllable resistive states in two-terminal electronics.

Chapter 8.

Conclusions and perspectives

In this thesis, we have focused on constructing devices by assembling VO_2 single and multiple bridge structures in two-terminal configurations and fine-tuning their switching behavior at the device level. This chapter serves to summarize the findings of the presented experiments. Additionally, we will discuss potential directions for future research on a broader scale.

8.1 Conclusions

At the beginning of this thesis, we contemplated a path to overcome the bottlenecks and limitations of current computing architecture, which is developing the brain-inspired neuromorphic computing system. Neuromorphic computing circuitry requires novel circuit elements with tunable resistance states, nonlinear response functions and adaptable dynamic behavior for the case of spiking neuromorphic circuitry. VO_2 is an attractive candidate material to fulfill some of these roles, since it exhibits a near-room-temperature, hysteretic IMT with resistivity changes of several orders of magnitude. To utilize the IMT for novel switching electronics, we systematically investigated the resistive switching behavior of VO_2-based devices with various configurations, starting from the thin film growth to the fabrication of the bridges, further to the electrical characterizations, as detailed in this thesis. VO_2 thin films were grown epitaxially on (001)-oriented TiO_2 substrates using PLD. If the thickness of the films is below the critical value (12 nm), they are fully strained and exhibit the IMT at a lower temperature, making them suitable for room temperature applications. Making use of the reduced transition temperature of strained films, we fabricated planar devices by etching the film into bridge structures. We explored the reliability of various etching techniques and found that Ar ion milling is more reproducible and controllable than wet-chemical etching, making it suitable for further fabrication. Reliable fabrication procedures for microscale and nanoscale devices have been described.

Two-terminal resistive switching devices based on VO_2 parallel bridges have been successfully fabricated and characterized. The VO_2 parallel-bridge devices show typical volatile switching behavior, which is achieved by applying electrical bias to create Joule heating in the device and trigger the IMT. The current-controlled measurements offer better control over the generated Joule heating than voltage-controlled measurements, enabling more detailed information about the switching dynamics. The temperature-dependent electrical and thermal properties of VO_2 contribute to the instability and nonlinearity of the switching behavior, such as the sharp threshold switch and NDR regions. Moreover, the hysteresis nature of the resistivity makes the set and reset process of VO_2 bridges follow

different traces and provide room for multilevel operation within one single switching element.

In the parallel-bridge devices, there are several variables to manipulate the switching behaviors. To manipulate the resistive switching behavior on a device level, there are several key factors that have been tuned, including bridge number, bridge spacing and bridge geometry.

First, the number of VO_2 bridges determines the maximum number of switches and resistive states. From single bridge to double bridges and further to quintuple bridges, by simply adding switching elements, the device gains the potential for more resistive states. Moreover, scaling down the bridge to the nanoscale allows more bridges to be placed in one device.

As the number of the Joule heating-induced switching elements increases, the thermal interaction among them will greatly influence the switching behavior, which is a double-sided sword. On the one hand, when the bridges are placed in closer proximity to each other, the thermal crosstalk effect dominates, leading to simultaneous switching. On the other hand, it plays a role in assisting the subsequent switches with lower power. By increasing the spacing within a certain range, the bridges can be switched independently, and the power of the subsequent switches can be reduced, allowing the full potential of the double-bridge devices to be exploited.

The correlation between device length and spacing also impacts the switching behavior. Stochastic behavior can emerge when $L <\sim d$, resulting in unpredictable subsequent switching. In contrast, when $L > d$, the thermal crosstalk effect causes subsequent switches to preferentially occur in the neighboring bridge of the ON-state bridge. Therefore, the bridge spacing determines the number of measured switches and the potential switching bridge.

Additionally, the geometry of bridges highly influences the switching behavior, as it affects the initial resistance, the required switching power, and the generated heating of the bridges. Despite the limited number of devices investigated in this thesis, certain common trends have been observed. First, narrow bridges tend to win the competition in the low current range and can be triggered first. Second, once the wide bridges are switched ON, they dominate most of the current flowing through the device due to their low resistance. However, this also can

lead to the situation that the narrow bridges do not maintain the ON state or may not be switched at all.

Finally, the size of the bridges has been reduced to the nanoscale. The switching principles observed in microscale bridges are maintained for nanoscale devices, with significantly reduced switching power and more pronounced nonlinear properties. A 'waterfall-like' multi-bridge configuration has been proposed to achieve multiple switches and controllable resistive states in two-terminal electronics.

Compared to the current VO_2-based devices, which only consist of a single switching element, the VO_2-based parallel-bridge devices exhibit controllable switching behaviors, such as highly nonlinear responses, multiple switches, tunable intermediate resistive states, and history-based resistive states. Moreover, the concept of interacting switching bridges in a two-terminal device, rather than connecting them in series[136], effectively utilizes thermal crosstalk and enhances energy efficiency. This capability to control the novel switching behaviors at a device level assembled by single bridges may result in the development of novel circuit elements and broaden the application of neuromorphic computing.

8.2 Perspectives

The exploration of novel circuit elements utilizing the IMT of VO_2 for neuromorphic computing is a lively field of research. Here, we discuss a few perspectives in this field for future experiments.

In this thesis, we already discussed the tunable knobs at a device level to obtain novel switching behaviors and multiple resistive states. However, there is still room for further understanding of the switching behavior and improvement of device performance. For microscale devices, the switching dynamics can be interpreted by analyzing the change of differential conductance (dI/dV) and validating them with the qualitative current distribution maps obtained through SThM measurements. On the other hand, in the case of nanoscale devices, the discussion on how the bridges switch relies primarily on the observation of dI/dV plots and the assumption that the thermal interaction between bridges remains consistent with microscale bridges. Therefore, it would be beneficial to visualize the switching dynamics

using SThM scans as well. However, there are challenges in accurately resolving the less prominent heating paths with nanoscale proximity in these devices. Scanning over the nano-bridges that produce less Joule heating with nanoscale spacing usually results in a heating envelope covering the bridges. Two possible solutions can be considered. One is to reduce the thickness of the capping layer in order to improve the resolution of the SThM scan. The other is to image the current paths on each bridge individually instead of scanning the whole device area. This can be achieved by placing the SThM tip on top of each bridge, biasing the device to go through all the resistive states and monitoring the state of each bridge. Although this approach may be time-consuming for devices with numerous bridges, it can provide straightforward evidence of the switching dynamics.

By gaining a deeper understanding of the switching behavior, we can explore the assembly of VO$_2$ bridges in various configurations. As we proposed, the 'waterfall-like' multi-bridge configuration with different widths is promising for controllable sequential switching. Except for varying width, the length and spacing of the bridges can also be adjusted. This opens up possibilities for investigating more diverse and complex configurations. Therefore, it is urgent to establish a model to guide the design of the devices.

The primary goal of the model is to simulate the switching behavior of a given device configuration. This can be done by setting up a finite element model using COMSOL Multiphysics, which self-consistently considers electrical and thermal effects. An electrical model is used to calculate the voltage and current distribution in the device using Equation 8.1, while a thermal model based on Fourier's law of heat conduction in steady state (Equation 8.2) is used to determine the local temperature. In this, k is the thermal conductivity, and σ is the temperature-dependent electrical conductivity of VO$_2$. These two equations are coupled together via $J \cdot E$ as a Joule heating source term, with J being the local current density and E the local electric field.

$$\nabla \cdot (\sigma(x, y, z, T)\nabla V) = 0 \tag{8.1}$$

$$\nabla \cdot (k(\nabla T)) + J \cdot E = 0 \tag{8.2}$$

By calculating the resistive states of VO$_2$ bridges and considering the thermal interaction among them, it is possible to simulate the overall switching behavior and visualize the heating

path. This provides an efficient means to test various device configurations and optimize bridge geometry without the need to actually fabricate every possible option, saving time and effort.

Ultimately, the objective of the model is to act as a guide for assembling the VO_2 bridges or other potential switching elements, providing the possible configuration based on the desired switching properties. This model necessitates extensive calculations. Nevertheless, with the development in current generative AI models and the accumulation of a larger dataset from experiments, it is foreseeable that such a model may become feasible soon.

In addition to investigating device performance and principles, the application of these novel switching devices presents an intriguing research avenue. The VO_2-based devices, with sharp threshold switching and volatile behavior, hold potential for creating neuronal spiking behaviors when combined with other simple circuit components like capacitors and resistors. Moreover, the utilization of VO_2-based switching devices holds promise in establishing oscillatory neural networks as an alternative to the conventional convolutional computing layer for image processing operations[137]. While progress has been made using devices with a single switching element[97,138] or several coupled devices[29,139], the utilization of devices with multiple interacting switching elements remains largely unexplored. It is anticipated that such devices can offer more diverse spiking behavior. For instance, whereas a single switching element produces a monotonic spike frequency, multiple correlated switching elements can enable tuning of the frequency within a fixed circuitry.

Furthermore, the integration of VO_2-based devices with other non-volatile switching devices offers the potential to emulate both neurons and synapses. In an ideal scenario, this emulation could be achieved entirely within the VO_2 material itself. Through specific material engineering approaches, such as Ar ion beam bombardment or utilizing IL gating to create movable defects, the VO_2 bridges can exhibit non-volatile switching behavior. Consequently, the connection of VO_2 'neurons' can be realized through the VO_2 'synapses' with tunable states. Ultimately, this research is aimed to contribute to new directions for energy-efficient, brain-inspired information technologies. The work presented in this thesis illustrates and analyses the potential of utilizing VO_2 for its unique switching behavior in various configurations.

Towards technology, this can be further extended into e.g., multiterminal devices, oscillatory networks and other functional circuits, with energy-efficiency as a central design parameter.

Summary

This thesis is related to overcoming the bottlenecks and limitations of current computing architectures by developing brain-inspired computing systems. This thesis aims to contribute to the development of neuromorphic computing by exploring devices based on VO_2 with unique switching characteristics. In **Chapter 2**, we reviewed recent advancements in utilizing VO_2 for neuromorphic computing circuits and discussed the motivation behind this research. We focused on hardware aspects of neuromorphic computing systems and introduced a key building block; the memristor. We discussed the physical principles of the memristive phenomena, with a specific focus on the insulator-metal transition (IMT) of VO_2 and its driving force. Utilizing the electrically induced IMT of VO_2, we have proposed strategies to establish a two-terminal device with novel switching behaviors, including multi-switches, multi-level operation, highly nonlinear responses, etc.

The resistive switching behavior of the VO_2 bridge devices is not only influenced by the intrinsic material properties but can also be tuned on a device level. Therefore, we have systematically investigated the resistive switching behavior of VO_2-based devices with various configurations, starting from the thin film growth to the fabrication of the bridges, further to the electrical characterizations.

Chapter 3 focused on the thin film fabrication of VO_2 through pulsed laser deposition (PLD) and the subsequent characterization of the deposited films. The impact of substrate-induced strain on the films was explored, and the importance of avoiding crack formation by maintaining a thickness below the critical value (~12 nm) was emphasized.

We fabricated planar devices by etching the film into bridge structures, taking advantage of the reduced transition temperature of the film due to the epitaxial strain. In **Chapter 4**, we explored the reliability of various etching techniques and found that Ar ion milling is more reproducible and controllable than wet etching, making it suitable for further fabrication. Two-terminal resistive switching devices based on VO_2 parallel bridges have been

successfully fabricated and characterized, starting with the single-bridge devices. The VO_2 single-bridge devices show typical volatile switching behavior, which is achieved by applying electrical bias to create Joule heating in the device and trigger the IMT. The temperature-dependent electrical and thermal properties of VO_2 contribute to the instability and nonlinearity of the switching behavior, such as the sharp threshold switching. Moreover, the hysteresis nature of the resistivity makes the set and reset process of VO_2 bridges follow different traces and provide room for multilevel operation within one single switching element. Controllable switching behavior is demonstrated between multiple resistance levels over several orders of magnitude, allowing for multibit operation.

Based on the findings in Chapter 4, we explore devices with more complex configurations, such as double bridges in **Chapter 5**. By assembling single bridges in a parallel configuration, we can achieve a higher degree of control for multistate characteristics. We studied switching dynamics and the effect of thermal crosstalk using current-controlled measurements and in-operando scanning thermal microscopy (SThM). As a result, the thermal interaction between bridges will greatly influence the switching behavior, which is a double-sided sword. On the one hand, when the bridges are placed in closer proximity to each other, the thermal crosstalk effect dominates, leading to simultaneous switching. On the other hand, it plays a role in assisting the subsequent switches with lower power. By increasing the spacing within a certain range, the bridges can be switched independently, and the power of the subsequent switches can be reduced, allowing the full potential of the double-bridge devices to be exploited.

In **Chapter 6**, the device configuration was further extended to include multiple bridges. We examined the effect of several factors at a device level, such as the number of bridges, spacing between bridges, and geometries of bridges. We fabricated and measured devices with additional bridges, such as triple-bridge and quintuple-bridge devices, as well as devices with multi-width bridges.

First, the number of the VO_2 bridge determines the maximum number of switches and resistive states. From single bridge to double bridges and further to quintuple bridges, by simply adding the switching elements, the device gains the potential for more resistive states.

Similar to the double-bridge devices, the bridge spacing influences the thermal interaction significantly. Moreover, the correlation between device length (L) and spacing (d) also impacts the switching behavior. Stochastic behavior can emerge when $L <\sim d$, resulting in the subsequent switches unpredictable. In contrast, when $L > d$, the thermal crosstalk effect causes subsequent switches to preferentially occur in the neighboring bridge of the ON-state bridge. Therefore, the inter-bridge spacing determines the number of measured switches and the potential switching bridge. Additionally, the geometry of bridges highly influences the switching behavior, as it affects the initial resistance, the required switching power, and the generated heating of the bridges. Despite the limited number of devices investigated in this thesis, certain common trends have been observed. First, narrow bridges tend to win the competition in the low current range and can be triggered first. Second, once the wide bridges are switched ON, they dominate most of the current flowing through the device due to their low resistance. However, this also raises the risk that the narrow bridges may not be able to maintain the ON state or may not be switched at all.

Finally, in **Chapter 7**, the size of the bridges has been shrunk to nanoscale. We reported on the resistive switching behaviors of single-bridge, double-bridge, and multi-bridge devices in the nano-scale range. The switching principles observed in microscale bridges were maintained for nanoscale devices, with significantly reduced switching power and more pronounced nonlinear properties. A 'waterfall-like' multi-bridge configuration has been proposed to achieve multiple switches and controllable resistive states in two-terminal electronics.

In this thesis, VO_2-based thin film structures with unique switching characteristics have been investigated. The study spans from thin film fabrication to the characterization and understanding of various device configurations. The ability to control the novel switching behaviors at a device level, through variation of multi-bridge configurations, provides a route to the development of novel circuit elements for neuromorphic computing.

Samenvatting

Dit proefschrift is gerelateerd aan het overwinnen van de beperkingen en belemmeringen van huidige computerarchitecturen door de ontwikkeling van neuromorfe computing systemen, geïnspireerd door de hersenen. Het doel van dit proefschrift is bij te dragen aan de ontwikkeling van neuromorfe computing door het onderzoeken van elektronische teststructuren met unieke schakelkarakteristieken, gebaseerd op vanadium-dioxide (VO_2). In **Hoofdstuk 2** bespreken we recente ontwikkelingen in het gebruik van VO_2 voor neuromorfe computing circuits en geven we de motivatie achter dit onderzoek. We richten ons op de hardware-aspecten van neuromorfe computing systemen en introduceren een belangrijke bouwsteen: de *memristor*. We bespreken de fysische principes van de memristieve fenomenen, met speciale aandacht voor de isolator-metaal overgang van VO_2 en de drijvende kracht erachter. Op basis van de elektrisch geïnduceerde isolator-metaal overgang van VO_2 stellen we strategieën voor om een tweepoorts-structuur met nieuw schakelgedrag te realiseren, waaronder meervoudige schakelingen, meervoudige toestanden, sterk niet-lineaire reacties, enzovoort.

Het weerstandsschakelende gedrag van de VO_2 structuren wordt niet alleen bepaald door de intrinsieke materiaaleigenschappen, maar kan ook extern worden beïnvloed. Daarom hebben we systematisch VO_2-structuren met verschillende configuraties onderzocht, te beginnen met de dunnelaag-groei tot aan de structuring en vervolgens de elektrische karakterisering.

Hoofdstuk 3 richt zich op de dunnelaag-fabricage van VO_2 door middel van gepulsde laserdepositie en de daaropvolgende karakterisering van de gedeponeerde films. Het effect van door het substraat geïnduceerde epitaxiale rek op de lagen is onderzocht, en het belang van het vermijden van fase-veranderingen door de dikte onder een kritische waarde (~12 nm) te behouden, wordt benadrukt.

We fabriceren planaire meet-objecten, door de films te etsen in de vorm van brug-structuren, waarbij gebruik wordt gemaakt van de verlaagde transitietemperatuur van de films ten

gevolge van epitaxiale rek. In **Hoofdstuk 4** onderzoeken we de betrouwbaarheid van verschillende etsmethodes en ontdekken we dat argon-ionen etsen reproduceerbaarder en controleerbaarder is dan nat-chemische technieken. Tweepoorts-weerstandsschakelende structuren gebaseerd op enkele of parallelle VO_2-bruggen zijn succesvol gefabriceerd en gekarakteriseerd, beginnend met de enkele brugstructuren. De enkele VO_2-brugstructuren vertonen typisch niet-permanent schakelgedrag, dat wordt bereikt door elektrische spanning aan te leggen om Joule-verwarming in het materiaal te induceren en de isolator-metaal overgang te activeren. De temperatuurafhankelijke elektrische en thermische eigenschappen van VO_2 dragen bij aan de instabiliteit en niet-lineariteit van het schakelgedrag, zoals een scherpe drempelwaarde voor de schakeling. Bovendien maakt de hysterese van de weerstand het mogelijk dat het aan- en uitschakelen van de lage weerstands toestand in de VO_2-bruggen bij verschillen aangelegde spanningen geschieden, hetgeen de mogelijkheid biedt voor de realisatie van meervoudige toestanden binnen één enkel schakelend element. Controleerbaar schakelgedrag wordt gedemonstreerd tussen meerdere weerstandsniveaus over verschillende ordes van grootte, waardoor multibit-operatie mogelijk is.

Op basis van de bevindingen in Hoofdstuk 4 onderzoeken we in **Hoofdstuk 5** structuren met complexere configuraties, zoals dubbele bruggen. Door enkele bruggen in een parallelle configuratie samen te stellen, kunnen we een hogere mate van controle bereiken met meerdere toestanden. We bestuderen de schakeldynamiek en het effect van thermische overspraak met behulp van stroomgestuurde metingen en in-operando raster thermische microscopie ('*Scanning Thermal Microscopy*'). De resultaten laten zien dat de thermische interactie tussen bruggen sterk het schakelgedrag beïnvloedt, wat een tweezijdig effect heeft. Enerzijds, wanneer de bruggen dichter bij elkaar geplaatst zijn, domineert het effect van thermische overspraak en schakelen de bruggen gelijktijdig. Anderzijds speelt het een rol bij het ondersteunen van de daaropvolgende schakelingen met minder vermogen. Door de afstand te vergroten, kunnen de bruggen onafhankelijk van elkaar worden geschakeld en kan het vermogen van de daaropvolgende schakelingen worden verminderd, waardoor het volledige potentieel van de dubbele-brugstructuren kan worden benut.

In **Hoofdstuk 6** wordt de configuratie verder uitgebreid door toevoeging van meerdere

bruggen. We onderzoeken het effect van verschillende factoren, zoals: het aantal bruggen, de afstand tussen bruggen en de geometrie van de bruggen. We fabriceren en meten structuren met extra bruggen, zoals drievoudige- en vijfvoudige bruggen, evenals structuren met bruggen van verschillende breedtes.

Ten eerste bepaalt het aantal VO_2-bruggen het maximaal aantal weerstandsschakelingen en -toestanden. Van enkele bruggen tot dubbele bruggen en verder tot vijfvoudige bruggen; door eenvoudig de schakelelementen toe te voegen, krijgt het systeem de mogelijkheid voor meer weerstandstoestanden. Net als bij de dubbele-brugstructuren heeft de afstand tussen bruggen een aanzienlijke invloed op de thermische interactie. Bovendien beïnvloedt de correlatie tussen de lengte (L) van de brug en de afstand (d) ook het schakelgedrag. Stochastisch gedrag kan optreden wanneer $L <\sim d$, hetgeen resulteert in onvoorspelbare schakelingen. Daarentegen veroorzaakt het effect van thermische overspraak bij $L > d$ dat de daaropvolgende schakelingen bij voorkeur plaatsvinden in de naburige brug van de brug die al in de lage weerstandstoestand is. Daarom bepaalt de onderlinge brugafstand het aantal waargenomen schakelingen en de potentieel schakelende brug.

Daarnaast beïnvloedt de geometrie van de bruggen sterk het schakelgedrag, omdat het de initiële weerstand, het benodigde schakelvermogen en de gegenereerde warmte van de bruggen beïnvloedt. Ondanks het beperkte aantal onderzochte apparaten in dit proefschrift zijn bepaalde gemeenschappelijke trends waargenomen. Ten eerste hebben smalle bruggen de neiging om te domineren in het lage stroomgebied en kunnen ze als eerste worden geactiveerd. Ten tweede, zodra de brede bruggen zijn ingeschakeld, domineren zij het grootste deel van de stroom die door het apparaat stroomt vanwege hun lage weerstand. Dit kan er ook toe leiden dat de smalle bruggen mogelijk niet in de lage weerstandstoestand kunnen blijven of helemaal niet worden geschakeld.

Tot slot, in **Hoofdstuk 7** is de grootte van de bruggen verkleind tot de nanoschaal. We doen verslag van het weerstandsschakelende gedrag van enkele bruggen, dubbele bruggen en multi-bruggen op de nanoschaal. De schakelprincipes die worden waargenomen bij bruggen op de microschaal blijven behouden voor de nanoschaal, met aanzienlijk verminderd schakelvermogen en meer uitgesproken niet-lineaire eigenschappen. Een 'watervalachtige'

multi-brugconfiguratie is voorgesteld om meerdere schakelingen en controleerbare weerstandstoestanden te bereiken in tweepoorts-elektronica.

In dit proefschrift zijn VO$_2$-gebaseerde dunne laag structuren met unieke schakelkarakteristieken onderzocht. Het onderzoek strekt zich uit van dunnelaag-fabricage tot de karakterisering en het begrijpen van verschillende configuraties. Het vermogen om de nieuwe schakelgedragingen te controleren, door variatie van multibrug-configuraties, biedt een route tot de ontwikkeling van nieuwe schakelelementen voor neuromorfe computing.

全文总结

本论文的研究旨在通过开发神经形态计算系统，克服当前冯诺依曼计算架构的能耗瓶颈和计算速度限制。我们聚焦于二氧化钒（VO_2）这种具有相变特性的金属氧化物，探索基于 VO_2 的电子器件独特的开关特性，为神经形态计算电路带来可观的应用前景。

在**第二章**中，我们介绍了当前基于 VO_2 的开关元件在神经形态计算电路方面的研究进展，并讨论了本论文的研究目的。我们着重探索神经形态计算系统的硬件方面，其中关键的基本元件是有记忆功能的非线性电阻——记忆电阻器。我们详细探讨了当前记忆电阻器的物理原理，特别是着重介绍了 VO_2 所具有的绝缘体—金属相变（IMT）及其相变机理。电场诱导的 VO_2 相变器件具有简单的结构和广阔的应用前景。在此基础上，我们建立了具有新型开关行为的 VO_2 两端桥型器件，其中包括多阻态、多级操作、显著的非线性响应等特性。

首先，我们利用脉冲激光沉积（PLD）方法制备了 VO_2 薄膜。为了充分利用应变薄膜所具备的较低相变温度特性，我们将 VO_2 薄膜蚀刻成桥型结构，并制备成平面两端器件，并对其电学性质进行了详细表征。VO_2 两端桥型器件的电学性质不仅受到其固有材料特性的影响，还可以通过调节器件结构来实现。因此，我们对器件在各种结构下的开关行为进行了系统研究。

第三章介绍了 PLD 方法，并对制备的 VO_2 薄膜进行了一系列表征。我们研究了衬底诱导的应变对 VO_2 薄膜表面形貌和相变特性的影响。我们发现，当 VO_2 薄膜的厚度高于临界值（约 12 纳米）时，薄膜中的应变会松弛，从而导致裂纹的形成。因此，我们需要将 VO_2 薄膜厚度控制在临界值以下，以获得均匀可靠的薄膜并进一步制备器件。

在**第四章**中，我们详细介绍了制备 VO_2 两端桥型器件的方法，并对各种蚀刻技术的可靠性进行了研究。我们发现，氩离子束刻蚀的方法更为可控，可用于器件的制备。在电学测试中，VO_2 单桥器件表现出典型的易失性开关行为。通过在器件两端施加电压，VO_2 单桥中产生的焦耳热触发了 IMT，实现了电阻率的改变，使器件呈现出阈值

开关特性。此外，电阻率的滞后性使得 VO_2 桥型器件的触发和复位过程遵循不同的轨迹，为单个开关元件内的多级操作提供了可能。我们可以通过控制外加电压，在 VO_2 单桥器件实现多个电阻态之间的切换。

在**第五章**中，我们研究了具有更复杂结构的器件，如双桥结构。通过将两个单桥并联在一个器件中，我们可以实现更高程度的多阻态控制。我们利用电学测试和原位扫描热显微镜（SThM）研究了器件的开关特性和桥之间的热相互作用。结果表明，桥之间的热相互作用将极大地影响开关行为。这是一个双刃剑：一方面，当桥彼此靠近时，热相互作用占主导地位，导致双桥同时被触发；另一方面，通过在一定范围内增加桥间距，双桥可以被独立触发，并且触发后续桥的功率明显降低。

在**第六章**中，我们进一步扩展了器件结构至多桥结构。我们系统研究了多个可控参数对器件开关特性的影响，例如桥的数量、桥的间距和桥的几何形状。我们成功制备和表征了三桥器件、五桥器件，以及具有不同宽度桥的器件。

我们发现，首先，VO_2 桥的数量决定了最大开关数和电阻态数。从单桥到双桥再到五桥，通过简单地添加桥的数量，器件可以在更多的电阻态之间切换。与双桥器件类似，桥的间距显著影响热相互作用。此外，桥的长度和间距之间的大小关系也影响着器件的开关特性。当长度小于间距或与之相近时，器件的开关特性会出现随机行为，导致后续被触发的桥是不可预测的。相反，当长度大于间距时，热相互作用导致后续被触发的桥更倾向于发生在已被触发的桥的相邻桥中。因此，桥间距影响了可以测量到的开关数和被触发的桥的位置。此外，桥的几何形状也极大地影响开关行为，因为它影响每个桥的初始电阻、所需触发功率和产生的焦耳热。尽管本论文中研究的器件数量有限，但我们观察到了某些普适的特性。首先，在低电流范围内，较窄的桥可以被首先触发。其次，一旦较宽的桥被触发切换到低电阻态，由于其较低的电阻，它们将主导器件中大部分电流。然而，这也使得较窄的桥无法维持低电阻态，或者无法被进一步触发。

最后，在**第七章**中，我们将 VO_2 桥的尺寸缩小到了纳米尺度。我们研究了纳米尺寸的单桥、双桥和多桥器件的电学特性。我们观察到，应用于微米尺寸器件的电学特性和原理在纳米尺寸器件中仍然适用，并且纳米尺寸器件具有低的开关功耗和更加显著的非线性特性。基于实验结果，我们提出了一种"瀑布式"多桥结构器件，其中桥的尺寸由小到大逐渐增加。具有这种结构的器件可以更好地实现多重开关和可控多电阻

态特性。

  在本论文中，我们研究了具有独特开关特性的 VO_2 两端桥型器件。研究涵盖了从薄膜生长到各种器件结构的制备和表征。通过改变器件中桥的数量和结构，能够在器件级别控制其开关行为，实现可控的多阻态特性，为神经形态计算的新型电路元件的发展提供了途径。

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