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Robust Spiking Attractor Networks with a Hard Winner-Take-All Neuron Circuit

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Abstract-Attractor networks are widely understood to be a reoccurring primitive that underlies cognitive function. Stabilising activity in spiking attractor networks however remains a difficult task, especially when implemented in analog integrated circuits (aIC). We introduce here a novel circuit implementation of a hard Winner-Take-All (hWTA) mechanism, in which competing neurons' refractory circuits are coupled together, and thus their spiking is forced to be mutually exclusive. We demonstrate stable persistent-firing attractor dynamics in a small on-chip network consisting of hWTA-connected neurons and excitatory recurrent synapses. Its utility within larger networks is demonstrated in simulation, and shown to support overlapping attractors and be robust to synaptic weight mismatch. The realised hWTA mechanism is thus useful for stabilising activity in spiking networks composed of unreliable components, without the need for careful parameter tuning.

Index Terms—Attractor network, spiking neurons, neuromorphic engineering, analog CMOS, working memory, winner-takeall.

I. INTRODUCTION

The human brain exhibits remarkable information processing capabilities while consuming approximately only 20 W of power [1]. In comparison, modern deep learning accelerators, which aim to perform only a subset of possible cognitive tasks, have power consumptions which are several orders of magnitudes greater. One major culprit of this disparity in power consumption is the so-called Von-Neumann bottleneck, wherein conventional computer architectures spend much time and energy ferrying data between storage units and computational units [2]. This is in stark contrast to biology, where there is no such clear distinction between areas dedicated to storage and those dedicated to computation. Neuromorphic

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Author Contribution: M.C., and E.C. conceived the experiments. M.C., O.R., M.M., H.G., E.J. and W.S.G. designed the circuits and chip. M.C., M.M. and E.J. built the periphery. M.C., H.G. did the chip measurements. Circuit design and chip measurement was done under the supervision of O.R. and E.C. with M.M. as project coordinator. M.Z. and E.C. jointly supervised the research. All authors contributed to the manuscript. The authors would like to acknowledge Philipp Klein for soldering the PCBs and Ton Juny Pina for his help with chip testing.

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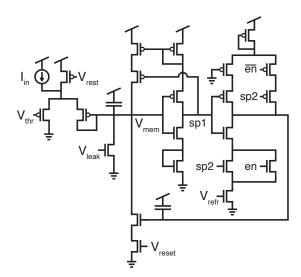
engineering aims to close this gap by exploring massively parallel brain-inspired computation schemes, where memory and computation are co-located. One such biologically and physically inspired model is the attractor network, wherein the dynamics of a recurrently connected population of neurons can be described by a set of fixed-point attractor states, to which the neural activity converges in the absence of input [3-7]. Such networks are remarkably robust, remaining stable and functional in the face of noisy inputs, asynchronous updates, and imperfections in their implementation (e.g. weight mismatch). As such, they are suitable for implementation in both biological networks as well as in analog Integrated Circuits (aIC) [8-10]. They are theoretically well understood, and the same network topology can be trained to perform a variety of tasks simultaneously, e.g. pattern completion [3, 11, 12], separation [13], correction [14, 15], and classification [16], as well as being capable constraint satisfaction and optimisation task solvers [17-20].

Implementing attractor networks in spiking neuromorphic hardware, where biological neural and synaptic dynamics are emulated by ultra-low power analog CMOS circuits, promises further gains in efficiency [21, 22]. Ensuring attractor stability in neuromorphic aIC poses a unique challenge however, as the combination of unreliable devices and positive feedback due to recurrent dynamics means that careful consideration must be made to ensure the recurrent excitation is simultaneously strong enough to sustain spiking activity, but not so strong that runaway excitation causes the network to enter a state of all neurons firing continuously [23]. Most aIC Spiking Neural Networks (SNN) therefore restrict the attractor states



Fig. 1. Photograph of the realised "Cognigr1" ASIC. Within the small white rectangle are the analog synapses and competitive hWTA neuron circuits, while the larger white rectangle includes the on-chip DAC and supporting I/O circuitry.

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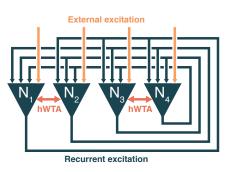


Fig. 3. A high level diagram of the SNN implemented on the Cognigr1 ASIC, comprised of 4 ExLIF neurons (denoted $N_{1:4}$), where neurons are hWTA connected to each-other as depicted. Excluding self connections, between every ordered pair of neurons there is an excitatory DPI synapse [38] with an individually configurable weight (12 recurrent synapses), and additionally each neuron has a non-recurrent excitatory DPI synapse which receives input from off-chip.

Fig. 2. The circuit of a single neuron with the hWTA mechanism. The capacitor voltage V_{mem} is the neuron's dynamic membrane voltage, while all other signals denoted V_{label} are subthreshold voltage parameters generated by the on-chip DAC. The digital signal "spl" is the low-active spike output of the neuron, while "sp2" is the spiking output of a competing neuron. The digital signal "en" allows the hWTA functionality to be disabled. The hWTA behaviour is accomplished by the added branch in the refractory circuit, such that the refractory circuits of the two competing neurons become coupled.

to be population-based and non-overlapping, such that one attractor's firing may not accidentally excite another [24-26]. This drastically reduces the number of storable attractor states, and is at odds with conventional attractor theory, where attractor states are usually independently generated and so may have an arbitrary degree of overlap [4]. Possible resolutions include adding a homeostatic mechanism to ensure a certain mean activity level [27, 28], a soft Winner-Take-All (sWTA) mechanism between attractor populations [26, 29, 30], or careful control of the relative strengths of inhibitory and excitatory recurrent connectivity [31]. Nonetheless, each have their drawbacks in either the need for careful parameter tuning or orthogonal pattern representations.

We here propose a spiking neuron circuit with a local pairwise hard Winner-Take-All (hWTA) [32-35] mechanism which overcomes many of these problems and achieves stableyet-switchable attractor dynamics, with arbitrary overlapping patterns, which is robust, scalable, and does not require extensive parameter tuning. Furthermore, the model does not require that trainable weights may be negative, and so is highly suitable for implementation with dense memristive crossbars [36, 37].

II. METHODS

We designed a composite neuron circuit, where each composite consists of two Exponential Leaky Integrate and Fire (ExLIF) neurons, whose competition is enforced by the coupling of their refractory circuits. The neuron design is based on the Differential Pair Integrator (DPI) neuron introduced in [39], and the reader is directed to [21] for a more thorough discussion of the neuron's membrane dynamics. The circuit of a single neuron is shown in Figure 2. A composite neuron circuit consists of 2 of these, with their spike signals sp1/sp2 connected accordingly. The main alteration to the standard DPI neuron circuit is that the neuron's refractory circuit may now be charged not only by its neuron spiking, but also by a competing neuron's spikes, similar to the spike-triggered global reset signal in [32]. Thus, if one neuron spikes, its competitor is forced into a refractory state without being given a chance to spike, realising the hWTA behaviour. The refractory capacitors then begin discharging only once both neurons have reached a refractory state, i.e. V_{mem} has been brought below the switching voltage of the first inverter. A current-limiting transistor was added to the refractory pull-down branch on the membrane capacitor, to ensure that the refractory capacitors have sufficient time to charge before V_{mem} is brought below the spike threshold. Without this transistor, we cannot ensure that both neurons will have the same refractory period $\tau_{\rm refr}$, and so competition for the next spike would be distorted. To the same end, the ground-connected PMOS in the pull-up branch of the refractory circuit was added to ensure further symmetry between competing neurons. The diode-connected transistor at the top of the refractory pull-up branch slows the switching of the second inverter, and prevents unwanted oscillations at spike time. A small network of 4 neurons $N_{1:4}$ was created, where neurons are pairwise hWTA-connected as shown in Figure 3. This network was fabricated in X-FAB's XP018 180 nm technology, as part of the Cognigr1 aIC. The network also consists of 16 excitatory DPI synapses [38], 12 of which were recurrently connected (all-to-all connectivity, no self connections), with the remaining 4 dedicated to external spike input. A diagram of the realised network is shown in Figure 3. Supporting the neural circuitry was also a 12-bit DAC to supply the necessary subthreshold voltage parameters, as well as 4 analog voltage multiplexers for monitoring. A photograph of the realised ASIC is shown in Figure 1. After verification of the desired behaviour of the neural circuitry, as well as small-scale tests of attractor dynamics, a large-scale simulation of ExLIF neurons using the hWTA mechanism was created in the Brian 2 SNN simulator [40], and was verified to support multiple overlapping attractor states despite considerable mismatch being imposed upon the network's connectivity matrix.

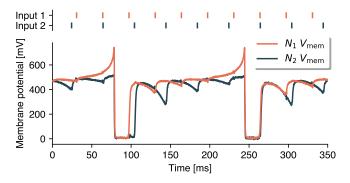


Fig. 4. Measurements from two neurons N_1 and N_2 exhibiting competitive hWTA behaviour. Each neuron receives 200 µs input voltage spikes at a rate of 30 Hz and 25 Hz respectively (shown above) from an off-chip function generator. Below are the membrane potentials $V_{\rm mem}$ of the two neurons, explicitly showing their integrative and leaky temporal dynamics in response to input. Since N_1 is receiving spikes at a higher frequency than N_2 , and thus has a larger synaptic input current, it reaches the spiking threshold first. The hWTA mechanism then forces both N_1 and N_2 into a refractory state, despite the fact that N_2 did not spike. This decisiveness allows a network of these neurons to reach a stable neural representation for arbitrarily strong input.

III. RESULTS AND DISCUSSION

We first verified that the hWTA mechanism was functioning on-chip as intended. The neurons and external synapses were given voltage parameters such that spiking could be triggered by 3-5 input spikes in quick succession, set by programming the on-chip DAC's FIFO storage with an external digital function generator. Recurrent synapses were disabled. Two hWTAconnected neurons N_1 and N_2 were then given input periodic spike trains of different frequencies but identical pulse widths and synaptic weights. In Figure 4 the membrane potentials of the competing neurons are shown. Despite both neurons receiving sufficient input to be able to spike in isolation, since N_1 receives input of a higher frequency (30 Hz) than N_2 (25 Hz) it reaches its spiking threshold first, and the hWTA mechanism forces both neurons into a refractory state, preventing N_2 from spiking.

The joint firing rate function of the two hWTA neurons was then investigated across a 2D sweep of input strengths. Input spike frequencies to the two neurons were thus varied independently. For each pair of input frequencies the neurons were allotted 500 ms (far larger than any circuit time constants) to reach a steady state and ensure that there were no residual dynamics from the previous frequency run. Spike output from the neurons was then recorded for one second. Output firing rates were then estimated via $f_{\text{out}} = [N_{\text{spikes}} - 1] / [t_{\text{last}}^{\text{spk}} - t_{\text{first}}^{\text{spk}}]$, and neurons with fewer than 2 spikes were assigned a firing rate of 0 Hz. Figure 5 shows the results of this 2D input sweep. We see that while there is mutual exclusivity in their spiking, for similar input spike frequencies it is not always the neuron with the greater input frequency which spikes first. That perfect competition does not hold is expected, as due to non-idealities such as transistor mismatch, one neuron will always have a slight advantage over the other. Assuming that a neuron spikes first, its dynamics are otherwise independent of the competing neuron, and so its firing rate curve is identical to that of a single neuron in isolation. Figure 6 shows a finer-

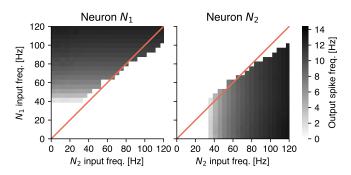


Fig. 5. Measurement data of the joint spike frequency response of a pair of hWTA-connected neurons N_1 and N_2 as the frequencies of spikes input to the two neurons are varied. The hWTA mechanism ensures that only the neuron receiving the strongest input is able to spike, and that if a neuron is the "winner" of the competition, then its single-neuron firing rate curve is otherwise independent of its competitor, and is typical of a single ExLIF neuron (Figure 6). Although ideally the two neurons should be identical in their behaviour and thus the data symmetric around the line y = x (shown in red), due to non-idealities such as device mismatch the data is not perfectly symmetric, and so one neuron has a slight advantage over the other at different firing rates.

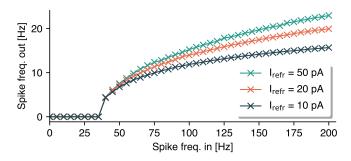


Fig. 6. Measurement data of the firing rate curve for a single neuron. This is equivalent to the firing rate curve for any neuron in Figure 5, assuming that the neuron spikes before its competitor. The three curves shown are for neurons with different refractory periods τ_{refr} , set by altering the refractory current parameter I_{refr} (and thus V_{refr} as in Figure 2). The firing rate characteristics are as expected from ExLIF neurons [21], with a reduction in τ_{refr} resulting in an increase in the spike rate that the neuron approaches for very strong input currents.

grained 1D sweep of a single winning neuron, and is typical of a single DPI ExLIF neuron. Altogether, as long as the neurons receive sufficient input to trigger spiking, the hWTAimplemented mutual exclusivity in neuron activity, combined with the asymptotic bounding of the DPI neuron's firing rate function means a network of these neurons may easily reach a nontrivial and stable firing rate configuration without careful regard for the strength of recurrent connectivity.

We next demonstrated the stability of small-scale on-chip attractor dynamics. The two attractor states to be implemented were the "1-3" and "2-4" states, represented by neurons (N_1 and N_3) or (N_2 and N_4) firing persistently in the absence of external input, respectively. This was achieved by setting the weight of recurrent synapses between neurons which should cooperate to a high, potentiated value, and all others to a lower, depressed value. Figure 7 shows the measured membrane traces and attractor dynamics, as a sequence of external inputs is given. The network is first initialised to be in the "1-3" state. For 1 s afterwards, no input is given, and the attractor exhibits stable sustained firing. At t = 1 s, a very strong

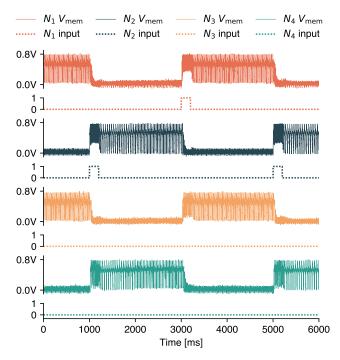


Fig. 7. Measurement data of on-chip bistable attractor dynamics. The inputs shown are the digital spike inputs to the external synapses. The recurrent weights are set to support the two attractors "1-3" and "2-4", where the corresponding neurons fire simultaneously and cooperatively to sustain spiking activity over a time period longer than any circuit time constants. The network is initialised in the "1-3" attractor state, and exhibits stable sustained activity. A strong excitatory input is then provided to N_2 only, causing it to spike faster than its hWTA-connected competitor N_1 , overpowering it and providing enough recurrent stimulus for the network to switch to the "2-4" attractor state, which then persists stably.

external input is given to N_2 for 200 ms. Consequently N_2 is driven to spike faster than N_1 , overriding the on-chip dynamics and preventing N_1 from spiking. The recurrent excitation from N_2 is then enough to excite N_4 to spike before N_3 , and the network switches to sustained firing of the "2-4" attractor. Thus, given a strong input corresponding to an incomplete stored pattern, the network switches to the corresponding completed pattern. The same procedure is repeated twice afterwards, switching again between the attractor states. The sustained firing of the final "2-4" state then remained stable for at least 30 minutes thereafter.

Since the on-chip network was too small to explicitly show overlapping attractor capabilities, we ran a larger simulation model in the Brian 2 SNN [40] simulator of 512 ExLIFhWTA neurons with the same connectivity as in Figure 3. Sixteen patterns $\{\vec{x}^p\}_{p=1}^{P=16}$ were stored as attractors in the network, of which 14 were randomly generated from the subset of $\{0, 1\}^{512}$ which obey the aforementioned pairwise mutual exclusivity. The remaining 2 patterns, denoted \vec{x}^1 and \vec{x}^2 , were manually chosen for the sake of visual clarity (see Figure 8). All patterns were approximately 50% overlapping with all other patterns. In contrast to gradient-based training methods, the excitatory recurrent weights were then set according to the Hebbian outer product rule

$$w_{ij} \propto |\chi_{ij}| + \frac{1}{\sqrt{\alpha}} \max\left(0, \sum_{\text{pattern } p}^{P} \left[x_i^p - \frac{1}{2}\right] \left[x_j^p - \frac{1}{2}\right]\right) \quad (1)$$

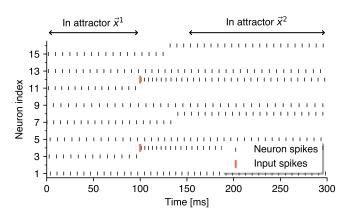


Fig. 8. Spike data from a Brian 2 simulation of a network of 512 ExLIFhWTA neurons with the same connectivity scheme as in Figure 3 and as implemented on-chip. The first 16 neurons are shown here, and are representative of the other neurons' behaviour. The recurrent excitatory weights were constructed to store 16 patterns as attractors, and then random noise of similar magnitude was added to emulate weight mismatch as per Equation 1. The network is initialised in a pattern \vec{x}^1 that was chosen w.l.o.g. to be $(1, 0, 1, 0, \ldots)$. A second pattern \vec{x}^2 was chosen to be $(1, 0, 0, 1, \ldots)$. At t = 100 ms a strong external input spike is sent to a subset of the neurons active in \vec{x}^2 . As in the on-chip experiments (Figure 7), this strong input overrides the recurrent dynamics, and the network switches to stably representing the second attractor.

where $w_{ij} \in \mathbb{R}_{\geq 0}$ is the weight from N_j to N_i , P the number of stored attractors, $\chi_{ij} \in \mathbb{R}$ are standard normally distributed random noise terms, and $\alpha = \frac{P}{16} \left[1 - \frac{1}{\pi}\right]$ is a scale constant to keep the summation term of unit standard deviation. The magnitude of weight mismatch noise is thus comparable to that of the deterministic addition. The network is initialised in the \vec{x}^{1} attractor state. Similar to the on-chip experiments, we then provide a strong excitatory input to a subset (25 %) of neurons which are active in \vec{x}^{2} , causing the network to switch to representing attractor \vec{x}^{2} (Figure 8). Although the simulation includes only non-idealities in the synaptic weights, its validity is supported by the robustness of the dynamics realised onchip, which can be scaled up via standard techniques [41, 42].

IV. CONCLUSION

We presented a neuron model and CMOS circuit with a novel hWTA implementation which enforces mutual exclusivity in spiking activity by coupling the refractory circuits of competing neurons. We taped out a small network of these neurons connected recurrently by excitatory DPI synapses. The connectivity thus consisted of fixed strong inhibitory connections between pairs of neurons, with only the excitatory connections being adjustable, a motif which is thought to be a principle of robust yet flexible cortical working memory maintenance [43]. On-chip measurement data verified the correct functioning of the hWTA mechanism, and we demonstrated stable-yet-switchable attractor dynamics in a small network with minimal required parameter tuning. In simulation the hWTA mechanism enabled overlapping attractor dynamics in a larger network, and was shown to be highly robust to synaptic weight mismatch. The fixed hWTA connectivity thus enables considerable stability properties in spiking attractor networks, and could represent a useful building block in spiking aICs where individual components are unreliable, but stable nontrivial neural representations are desired.

REFERENCES

- [1] C. W. Kuzawa, H. T. Chugani, L. I. Grossman, L. Lipovich, O. Muzik, P. R. Hof, D. E. Wildman, C. C. Sherwood, W. R. Leonard, and N. Lange, "Metabolic costs and evolutionary implications of human brain development," *Proceedings of the National Academy of Sciences* of the United States of America, vol. 111, no. 36, pp. 13010–13015, Sep. 2014.
- [2] G. Indiveri and S.-C. Liu, "Memory and Information Processing in Neuromorphic Systems," *Proceedings of the IEEE*, vol. 103, no. 8, pp. 1379–1397, Aug. 2015.
- [3] J. J. Hopfield, "Neural networks and physical systems with emergent collective computational abilities," *Proceedings of the National Academy* of Sciences, vol. 79, no. 8, pp. 2554–2558, Apr. 1982.
- [4] D. Amit, "Modeling Brain Function: The World of Attractor Neural Networks, 1st Edition," 1989.
- [5] D. Holcman and M. Tsodyks, "The Emergence of Up and Down States in Cortical Networks," *PLOS Computational Biology*, vol. 2, no. 3, p. e23, Mar. 2006.
- [6] Y. Shu, A. Hasenstaub, and D. A. McCormick, "Turning on and off recurrent balanced cortical activity," *Nature*, vol. 423, no. 6937, pp. 288–293, May 2003.
- [7] W. A. Little, "The existence of persistent states in the brain," *Mathe-matical Biosciences*, vol. 19, no. 1, pp. 101–120, Feb. 1974.
- [8] M. Verleysen and P. Jespers, "An analog VLSI implementation of Hopfield's neural network," *IEEE Micro*, vol. 9, no. 6, pp. 46–55, Dec. 1989.
- [9] C. Mead and L. Conway, *Introduction to VLSI Systems*, ser. Addison-Wesley series in computer science and information processing. Addison-Wesley, 1980.
- [10] R. Howard, D. Schwartz, J. Denker, R. Epworth, H. Graf, W. Hubbard, L. Jackel, B. Straughn, and D. Tennant, "An associative memory based on an electronic neural network architecture," *IEEE Transactions on Electron Devices*, vol. 34, no. 7, pp. 1553–1556, Jul. 1987.
- [11] H. Tang, M. Schrimpf, W. Lotter, C. Moerman, A. Paredes, J. Ortega Caro, W. Hardesty, D. Cox, and G. Kreiman, "Recurrent computations for visual pattern completion," *Proceedings of the National Academy of Sciences*, vol. 115, no. 35, pp. 8835–8840, Aug. 2018.
- [12] J.-H. Li, A. Michel, and W. Porod, "Analysis and synthesis of a class of neural networks: linear systems operating on a closed hypercube," *IEEE Transactions on Circuits and Systems*, vol. 36, no. 11, pp. 1405–1422, Nov. 1989.
- [13] E. Rolls, "The mechanisms for pattern completion and pattern separation in the hippocampus," *Frontiers in systems neuroscience*, vol. 7, p. 74, Oct. 2013.
- [14] N. Sourlas, "Spin-glass models as error-correcting codes," *Nature*, vol. 339, no. 6227, pp. 693–695, Jun. 1989.
- [15] J. J. Knierim and J. P. Neunuebel, "Tracking the flow of hippocampal computation: Pattern separation, pattern completion, and attractor dynamics," *Neurobiology of Learning and Memory*, vol. 129, pp. 38–49, Mar. 2016.
- [16] S. Wang, "Classification with incomplete survey data: a Hopfield neural network approach," *Computers & Operations Research*, vol. 32, no. 10, pp. 2583–2594, Oct. 2005.
- [17] G. E. Hinton, T. J. Sejnowski, and D. H. Ackley, *Boltzmann machines: Constraint satisfaction networks that learn*. Carnegie-Mellon University, Department of Computer Science Pittsburgh, PA, 1984.
- [18] Z. Jonke, S. Habenschuss, and W. Maass, "Solving Constraint Satisfaction Problems with Networks of Spiking Neurons," *Frontiers in Neuroscience*, vol. 10, 2016.
- [19] A. Likas, G. Papageorgiou, and A. Stafylopatis, "A Connectionist Approach for Solving Large Constraint Satisfaction Problems," *Applied Intelligence*, vol. 7, no. 3, pp. 215–225, Jul. 1997.
- [20] A. Srinivasulu, "Digital very-large-scale integration (VLSI) Hopfield neural network implementation on field programmable gate arrays (FPGA) for solving constraint satisfaction problems," *Journal of Engineering and Technology Research*, vol. 4, no. 1, pp. 11–21, Jan. 2012.
- [21] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, "Neuromorphic Electronic Circuits for Building Autonomous Cognitive Systems," *Proceedings of the IEEE*, vol. 102, no. 9, pp. 1367–1388, Sep. 2014.
- [22] G. Indiveri, B. Linares-Barranco, T. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbruck, S.-C. Liu, P. Dudek, P. Häfliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna, F. Folowosele, S. Saïghi, T. Serrano-Gotarredona, J. Wijekoon, Y. Wang,

and K. Boahen, "Neuromorphic Silicon Neuron Circuits," Frontiers in Neuroscience, vol. 5, 2011.

- [23] J. Tegnér, A. Compte, and X.-J. Wang, "The dynamical stability of reverberatory neural circuits," *Biological Cybernetics*, vol. 87, no. 5-6, pp. 471–481, Dec. 2002.
- [24] M. Giulioni, P. Camilleri, M. Mattia, V. Dante, J. Braun, and P. Del Giudice, "Robust Working Memory in an Asynchronously Spiking Neural Network Realized with Neuromorphic VLSI," *Frontiers in Neuroscience*, vol. 5, 2012.
- [25] M. Giulioni, F. Corradi, V. Dante, and P. del Giudice, "Real time unsupervised learning of visual stimuli in neuromorphic VLSI systems," *Scientific Reports*, vol. 5, no. 1, p. 14730, Oct. 2015.
- [26] D. Liang and G. Indiveri, "Robust state-dependent computation in neuromorphic electronic systems," in 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), Oct. 2017, pp. 1–4.
- [27] C. Bartolozzi and G. Indiveri, "Global scaling of synaptic efficacy: Homeostasis in silicon synapses," *Neurocomputing*, vol. 72, no. 4, pp. 726–731, Jan. 2009.
- [28] N. Qiao, C. Bartolozzi, and G. Indiveri, "An Ultralow Leakage Synaptic Scaling Homeostatic Plasticity Circuit With Configurable Time Scales up to 100 ks," *IEEE transactions on biomedical circuits and systems*, vol. 11, no. 6, pp. 1271–1277, Dec. 2017.
- [29] U. Rutishauser, R. Douglas, and J.-J. Slotine, "Collective Stability of Networks of Winner-Take-All Circuits," *Neural computation*, vol. 23, Dec. 2010.
- [30] D. Corneil, D. Sonnleithner, E. Neftci, E. Chicca, M. Cook, G. Indiveri, and R. Douglas, "Real-time inference in a VLSI spiking neural network," in 2012 IEEE International Symposium on Circuits and Systems (ISCAS), May 2012, pp. 2425–2428.
- [31] R. H. R. Hahnloser, R. Sarpeshkar, M. A. Mahowald, R. J. Douglas, and H. S. Seung, "Digital selection and analogue amplification coexist in a cortex-inspired silicon circuit," *Nature*, vol. 405, no. 6789, pp. 947–951, Jun. 2000.
- [32] J. Abrahamsen, P. Hafliger, and T. Lande, "A time domain winner-takeall network of integrate-and-fire neurons," in 2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512), vol. 5, May 2004.
- [33] S.-C. Liu and M. Oster, "Feature competition in a spike-based winnertake-all VLSI network," in 2006 IEEE International Symposium on Circuits and Systems (ISCAS), May 2006, pp. 4 pp.–3637.
- [34] D. Hernández García, S. Adams, A. Rast, T. Wennekers, S. Furber, and A. Cangelosi, "Visual attention and object naming in humanoid robots using a bio-inspired spiking neural network," *Robotics and Autonomous Systems*, vol. 104, pp. 56–71, Jun. 2018.
- [35] Y. Bethi, Y. Xu, G. Cohen, A. van Schaik, and S. Afshar, "An optimised deep spiking neural network architecture without gradients," *IEEE Access*, vol. 10, pp. 97912–97929, 2022.
- [36] Q. Xia and J. J. Yang, "Memristive crossbar arrays for brain-inspired computing," *Nature Materials*, vol. 18, no. 4, pp. 309–323, Apr. 2019.
- [37] Y. Zhang, Z. Wang, J. Zhu, Y. Yang, M. Rao, W. Song, Y. Zhuo, X. Zhang, M. Cui, L. Shen, R. Huang, and J. Joshua Yang, "Braininspired computing with memristors: Challenges in devices, circuits, and systems," *Applied Physics Reviews*, vol. 7, no. 1, p. 011308, Jan. 2020.
- [38] C. Bartolozzi and G. Indiveri, "Synaptic Dynamics in Analog VLSI," *Neural Computation*, vol. 19, no. 10, pp. 2581–2603, Oct. 2007.
- [39] P. Livi and G. Indiveri, "A current-mode conductance-based silicon neuron for address-event neuromorphic systems," in 2009 IEEE International Symposium on Circuits and Systems, May 2009, pp. 2898–2901.
- [40] M. Stimberg, R. Brette, and D. F. Goodman, "Brian 2, an intuitive and efficient neural simulator," *eLife*, vol. 8, p. e47314, Aug. 2019.
- [41] B. V. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A. R. Chandrasekaran, J.-M. Bussat, R. Alvarez-Icaza, J. V. Arthur, P. A. Merolla, and K. Boahen, "Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations," *Proceedings of the IEEE*, vol. 102, no. 5, pp. 699–716, 2014.
- [42] N. Qiao, H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawska, and G. Indiveri, "A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128k synapses," *Frontiers in neuroscience*, vol. 9, p. 141, 2015.
- [43] R. Kim and T. J. Sejnowski, "Strong inhibitory signaling underlies stable temporal dynamics and working memory in spiking neural networks," *Nature Neuroscience*, vol. 24, no. 1, pp. 129–139, Jan. 2021.