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Modulation bandwidth improvement of III-V/Si hybrid MOS optical modulator by reducing parasitic capacitance

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Abstract: In this work, we numerically and experimentally examined the impact of parasitic capacitance on the modulation bandwidth of a III-V/Si hybrid metal-oxide-semiconductor (MOS) optical modulator. The numerical analysis revealed that the parasitic capacitance between the III-V membrane and the Si slab should be considered to achieve high-speed modulation, particularly in the case of a thick gate oxide. We also fabricated a high-speed InGaAsP/Si hybrid MOS optical modulator with a low capacitance using a SiO_2-embedded Si waveguide. The fabricated device exhibited a modulation efficiency of 0.245 Vcm and a 3 dB bandwidth of up to 10 GHz. Clear eye patterns with 25 Gbps non-return-to-zero (NRZ) modulation and 40 Gbps 4-level pulse amplitude modulation (PAM-4) were obtained without pre-emphasis.

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1. Introduction

The increasing data traffic in data centers [1] and high-performance computing clusters [2] is driving the development of optical interconnection solutions up to several terabits per second. It is widely agreed that silicon (Si) photonics is the most promising technology for next-generation optical communication systems [3]. An efficient and large-bandwidth optical modulator is the component pivotal to realize the electro-optical (EO) conversion function. The free-carrier dispersion effect in Si is widely adopted in the conventional Si optical modulators. In particular, a metal-oxide-semiconductor (MOS) optical modulator provides a higher modulation efficiency because of its high capacitance over the carrier-depletion optical modulator [4]. However, the trade-off between modulation efficiency and modulation bandwidth in a Si MOS optical modulator limits the overall performance. Various approaches to improve the performance of Si MOS optical modulators were proposed. But they had a considerable increase in fabrication complexity [5–7]. To break the performance limit of a Si MOS optical modulator, the heterogeneous integration of III-V semiconductors on a Si photonics platform brings new opportunities [8,9].

In previous studies, an InGaAsP/Si hybrid MOS optical modulator was proposed [10,11], in which an n-type poly-Si layer in a conventional Si MOS optical modulator was substituted with a bonded n-type InGaAsP membrane. Owing to the greater electron-induced refractive index change in InGaAsP than in Si, the modulation efficiency is increased by a factor of 5 and the optical loss is suppressed by 10 times compared with all-Si MOS optical modulators. With the

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InGaAsP/Si hybrid MOS optical modulator, it is expected that a large modulation bandwidth and a high modulation efficiency can be achieved simultaneously [12]. However, owing to the high parasitic capacitance in our previous studies [10,13], the modulation bandwidth is limited below 1 GHz.

In this paper, we numerically and experimentally studied the impact of the parasitic capacitance in an InGaAsP/Si hybrid MOS structure on the modulation bandwidth. The numerical analysis revealed that the reduction in the parasitic capacitance between the Si slab and the III-V membrane is important for high-speed modulation. The Mach–Zehnder modulator (MZM) with an improved design for a low parasitic capacitance shows a 3 dB EO bandwidth of 10 GHz and a $V_{\pi}L$ of 0.245 Vcm. As a result, a 25 Gbps non-return-to-zero (NRZ) modulation and a 40 Gbps 4-level pules amplitude modulation (PAM-4) were obtained.

2. Numerical analysis

The schematic of the InGaAsP/Si hybrid MOS optical phase modulator reported in [10] is shown in Fig. 1. An n-type InGaAsP layer bonded onto a p-type Si waveguide with an Al_2O_3 gate dielectric forms a MOS capacitor. Upon applying a positive gate voltage to the hybrid MOS capacitor, electrons and holes accumulate at the InGaAsP/Al_2O_3 and Si/Al_2O_3 interfaces, respectively. As a result, the effective refractive index of the optical mode is modulated owing to the free-carrier effect. Since the electron-induced refractive index change in InGaAsP is more than 10 times greater than that in Si, the efficient optical phase modulation is achievable by using the hybrid MOS capacitor. When applying a negative votlage, the phase modulation can be achieved with the free-carrier effect and Franz–Keldysh effect in the depletion region at the MOS interface [14]. Note that carrier inversion with a large negative voltage may saturate the optical phase shift. In our previous work [10], the modulation bandwidth of the InGaAsP/Si hybrid MOS phase shifter is limited by the resistor–capacitor (RC) bandwidth owing to the large parasitic capacitance between the InGaAsP membrane and the supporting Si terraces, as shown in Fig. 1. In addition, the waveguide width, equivalent oxide thickness (EOT), and the doping profiles in the Si and III-V layers were not optimized to further reduce the RC constant.

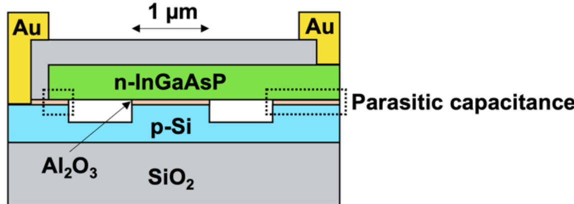

Fig. 1. Schematic of InGaAsP/Si hybrid MOS phase modulator in our previous work [10].

The parasitic capacitance between the III-V membrane and the Si terraces can be eliminated using a SiO_2-embedded Si waveguide. Because of the planarization of the SiO_2 cladding by chemical mechanical polishing, Si terraces are no longer required for the bonding of the III-V membrane [15]. However, a parasitic capacitance remains between the III-V membrane and the Si slabs. In [16], the authors showed that the capacitance changes with the overlap between the n-InP membrane and the p-Si slab, whereas the effect of this parasitic capacitance on modulation bandwidth has not been studied yet. To numerically investigate the impact of this parasitic capacitance, we considered two device structures shown in Fig. 2. The InGaAsP membrane is bonded to the SiO_2 cladding in both structures, to eliminate the parasitic capacitance from the Si terraces shown in Fig. 1. However, in Fig. 2(a), the Si slabs remain on both sides of the Si waveguide mesa. Therefore, the impact on the parasitic capacitance between the III-V membrane and the Si slab (C_{slab}) can be analyzed by comparing the capacitances of structure A

shown in Fig. 2(a) (C_{dev} + C_{slab}) and structure B shown in Fig. 2(b) (C_{dev}). Since there are no air gaps on both sides of the Si waveguide, the width of the Si waveguide is no longer limited for wafer bonding. Thus, the waveguide width in Fig. 2 is assumed to be 0.4 μm to reduce C_{dev} further. The III-V membrane is assumed to be 0.2-μm-thick $In_{0.97}Ga_{0.21}As_{0.46}P_{0.54}$ with a bandgap wavelength of 1.19 μm, which is transparent for an operating wavelength of 1.31 μm. The doping concentration of the n-InGaAsP layer is assumed to be 2×10^{18} cm^{-3}. A heavily doped n^+-InGaAs layer (1×10^{19} cm^{-3}) is also assumed for a low-resistive metal contact. The gap between the InGaAs layer and the edge of the Si waveguide is 1.0 μm. In structure A, the InGaAsP layer protrudes 0.5 μm from the Si edge due to the concern of overlay accuracy in fabrication. The thickness of the Si layer is 0.22 μm, and the doping concentrations are 1×10^{18} cm^{-3} for p-Si and 1×10^{20} cm^{-3} for p^+-Si. To prevent the free-carrier absorption from the p^+-Si layer, a 0.4 μm gap is assumed from the waveguide edge to the p^+-Si layer. The gate dielectric for the hybrid MOS capacitor is SiO_2, and the EOT of the hybrid MOS capacitor is varied from 5 nm to 40 nm. Here, we performed numerical analysis using Ansys Lumerical DEVICE and MODE simulators.

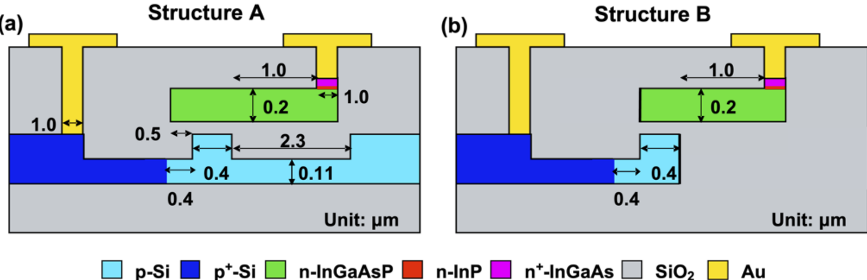

Fig. 2. Schematics of (a) InGaAsP/Si hybrid MOS phase modulator with overlap between InGaAsP and Si slab as structure A and (b) ideal InGaAsP/Si hybrid MOS phase modulator with no overlap as structure B.

First, we analyzed the phase modulation efficiency of the hybrid MOS phase shifter for a fundamental transverse-electric (TE) mode operating at a 1.31 μm wavelength. In Fig. 3(a), we show the carrier-induced phase shift with different EOTs from 5 nm to 40 nm in the structure A and B. The two structures show similar phase modulations with minor disparity stemming from the different mode distributions. As EOT increases, the phase shift decreases with both positive (accumulation) and negative (depletion) gate voltages. The nonlinear phase shift in small EOT is owing to the different free-carrier effect in depletion and inversion region [14]. When EOT increases, the inversion does not occur in the simulated bias range, leading to a relatively linear phase shift. The $V_\pi L$ is extracted from the accumulation region. The result is shown in Fig. 3(b). With EOT increasing from 5 nm to 40 nm, the $V_\pi L$ increases from 0.06 Vcm to 0.43 Vcm in both structures, independent of the slab overlap. This indicates that the parasitic capacitance between the III-V membrane and the Si slab (C_{slab}) has no contribution to the phase modulation. The simulated optical loss induced by the doping profile is 4.5 dB/mm.

Then, the capacitances of the hybrid MOS phase modulators were calculated by small-signal AC analysis. we show the potential distributions in Fig. 4(a) of the structures A and B shown in Fig. 2 when the devices are biased with 3 V for carrier accumulation. The potential drop between the III-V membrane and the Si slab is clearly observed with the structure A in Fig. 2(a), resulting in the additional slab capacitance (C_{slab}). The equivalent circuit models of the cross sections are shown on the right side of Fig. 4(a) correspondingly. The capacitance – gate voltage curves of C_{dev} and C_{slab} are shown in Fig. 4(b) for the EOT of 5 nm. While C_{dev} shows a strong dependence on gate voltage owing to the carrier depletion near the MOS interfaces, C_{slab} remains

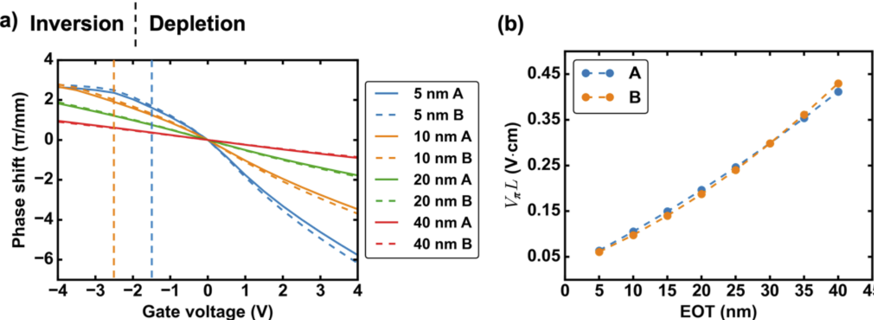

Fig. 3. (a) Simulated phase shift in InGaAsP/Si hybrid MOS phase modulators in structure A and B with different EOTs. (b) $V_\pi L$ extracted from the simulated phase shift of structure A and B with the gate voltage in the range of 0.5 V to 1.5 V.

constant with gating due to the smaller carrier response stemming from thick SiO_2 layer between the InGaAsP membrane and the Si slab region. The result in Fig. 4(b) also indicates that the negative gate bias cannot effectively reduce the total capacitance because of the existence of C_{slab}. Figure 4(c) shows C_{dev} and extracted C_{slab} as a function of EOT for the gate voltage of 6 V. Owing to EOT near zero, C_{dev} is sensitive to the change in EOT. Meanwhile, due to the addition of the slab thickness, C_{slab} is insensitive to the change in EOT. As a result, C_{dev} can be greater than C_{slab} when EOT is thin. In contrast, the simulation shows that C_{slab} becomes the dominant part in the total device capacitance when EOT is larger than 25 nm and leads to the RC bottleneck.

Next, we evaluated the effect of C_{slab} on the RC bandwidth using the equivalent circuit of the InGaAsP/Si hybrid MOS optical modulator with a lumped electrode as shown in Fig. 5(a). V_i is the output voltage of a driver. R_i is the output impedance of the driver fixed at 50 Ω. C_{pad} of 1 fF is the parasitic capacitance between the two metal contact vias calculated using the parallel plate model [17]. R_{slab} is the slab resistance in InGaAsP and Si from the contact to the junction region, which is calculated to be 6 Ω. C_{MOS} is the capacitance of the MOS optical phase modulator, i.e., $C_{MOS} = C_{dev} + C_{slab}$ for the structure A in Fig. 2(a) or $C_{MOS} = C_{dev}$ for that in structure B. The 3 dB RC bandwidths of a 120-μm-long phase shifter at accumulation (4 V) and depletion (−4 V) modes are shown in Figs. 5(b) and 5(c), respectively. As shown in these figures, the RC bandwidth increases with increasing EOT. When EOT is 40 nm, the RC bandwidth exceeds 50 GHz when there is no C_{slab}. Since the capacitance can be reduced in the depletion mode as shown in Fig. 4(b), the RC bandwidth is greater in the depletion mode than in the accumulation mode. In particular, the improvement of the RC bandwidth in the depletion mode is remarkable when EOT is small. When C_{slab} is taken into account, the RC bandwidth decreases considerably because the total capacitance is dominated by C_{slab} regardless of the bias conditions for the accumulation and depletion modes. As a result, the RC bandwidth is limited to approximately 20 GHz even with an EOT of 40 nm. In the case of the structure B in Fig. 2(b), the RC bandwidth increases linearly with EOT. As predicted by the capacitance simulation, the RC bandwidth decreases considerably at a thick EOT when considering C_{slab} in both accumulation and depletion mode. When EOT is small l, compared to the C_{slab}, the C_{dev} is large in accumulation modes and small in the depletion mode. Thus, the effect of C_{slab} is severer in the depletion mode than in the accumulation mode.

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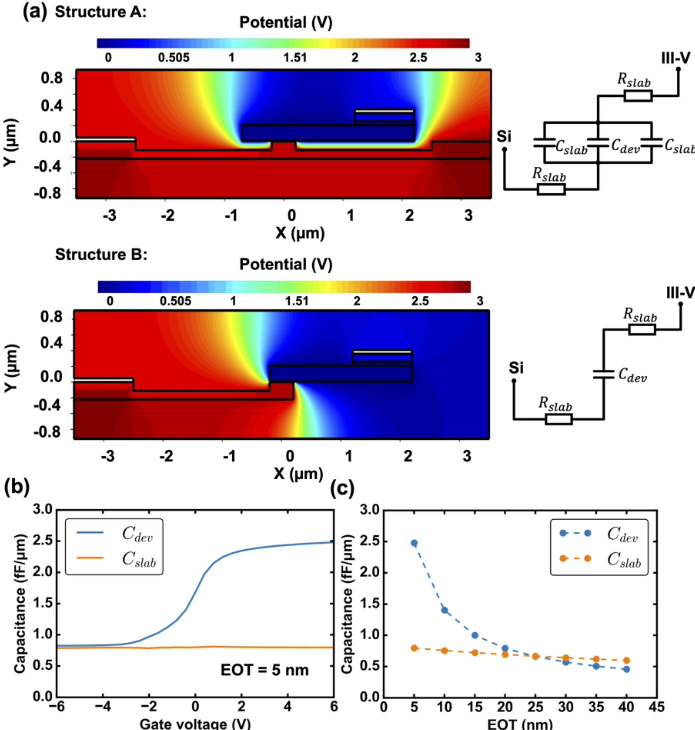

Fig. 4. (a) Potential distributions of the simulated structure A and B shown in Fig. 2 under 3 V bias for carrier accumulation. The equivalent circuits are shown along right side. (b) Device capacitance (C_{dev}) and slab capacitance (C_{slab}) as functions of gate voltage for EOT of 5 nm (c) Device capacitance (C_{dev}) and slab capacitance (C_{slab}) as functions of EOT for a gate voltage of 6 V.

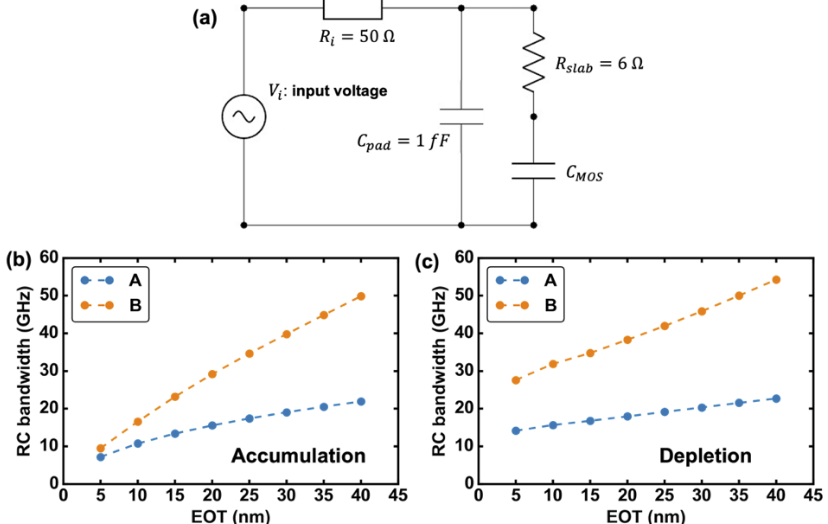

Fig. 5. (a) Equivalent circuit model of InGaAsP/Si hybrid MOS phase modulator with a lumped electrode for RC bandwidth calculation. 3 dB RC bandwidth of phase modulator in (b) accumulation mode and (c) depletion mode.

3. Fabrication process

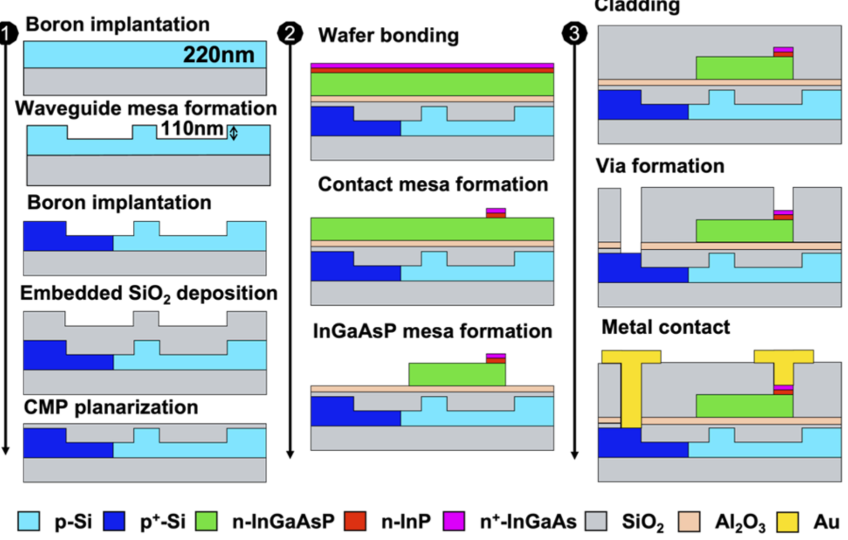

Fig. 6. Fabrication process flow of InGaAsP/Si hybrid MOS phase modulator.

To partially demonstrate the device, we used the Si waveguide in structure A of Fig. 2(a) which was originally used in [15,18]. Figure 6 shows the fabrication process flow. We started from a standard Si-on-insulator (SOI) wafer with a 220-nm-thick Si layer and a 2-µm-thick buried oxide (BOX). Firstly, we implanted boron to form the p-Si doping region. After activation annealing, the Si waveguide was defined by lithography and reactive-ion etching (RIE). High-dose boron was implanted to form the p^+-Si doping region in the Si/metal contact. The doping concentrations of the p-Si and p^+-Si regions were 1×10^{18} cm^{-3} and 1×10^{20} cm^{-3}, respectively. After activation, a thermal oxidation over 1000 °C was carried out to form a thin SiO_2 film with a thickness of 3 to 5 nm for good interface quality. Then, a thick SiO_2 layer was deposited by tetraethoxysilane (TEOS) based plasma-enhanced chemical vapor deposition (PECVD) to fill in the etched region. After planarization by chemical mechanical polishing (CMP), the thickness of SiO_2 remaining on the waveguide is approximately 10 ± 5 nm. We also grew 200-nm-thick n-$In_{0.97}Ga_{0.21}As_{0.46}P_{0.54}$ (2×10^{18} cm^{-3}), 50-nm-thick n-InP (2×10^{18} cm^{-3}), 100-nm-thick n^+-InGaAs (1×10^{19} cm^{-3}) and etch-stop layers on an InP substrate. Then, 10-nm-thick Al_2O_3 was formed on the top of the Si waveguide and InGaAsP surface by atomic layer deposition (ALD) at 200 °C as the bonding interface. Prebonding annealing for 40 min was carried out in a vacuum at 700 °C for the Si wafer and 200 °C for the InP wafer separately to suppress the void generation after bonding [19]. The Si and InP wafers were cleaned in mega sonic water and manually bonded together. The bonded wafer was annealed at a temperature of 200 °C for 1 h in vaccum, with a pressure of 0.625 MPa The InP substrate was removed with HCl solution. The etch-stop layers consisting of InGaAs and InP layers were etched with $H_3PO_4 : H_2O_2 : H_2O = 1 : 1 : 7$ and $H_3PO_4 : HCl = 4 : 1$. The InGaAs mesa for contact was defined by electron beam (EB) lithography and wet etching. The InGaAsP mesa was defined by EB lithography and RIE. Then, a 300-nm-thick SiO_2 cladding was formed by PECVD. The via for contact was opened by BHF wet etching. However, the etching speed of the Al_2O_3 layer on the Si contact region is slow compared to the SiO_2 cladding. Therefore, after SiO_2 etching by BHF, the Al_2O_3 layer was selectively etched with 2.38% tetramethylammonium hydroxide (TMAH) at 40 °C to avoid side-wall etching of

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the contact via. Finally, the Ni (50 nm)/Au (500 nm) metal stack was deposited using the EB evaporator and patterned by the lift-off process.

The plan-view scanning electron microscopy (SEM) images of the fabricated device are shown in Figs. 7(a) and 7(b). The GSGSG electrode was formed for RF measurement as shown in Fig. 7(a). From Fig. 7(b), we confirmed a smooth adiabatic InGaAsP taper which is required to suppress the mode mismatch between the Si waveguide and hybrid waveguide. Figures 7(c) and 7(d) are the cross-sectional transmission electron microscopy (TEM) images of the fabricated device. As shown in Fig. 7(c) that the InGaAs membrane is well bonded to the planarized Si waveguide. From the magnified TEM image of the bonded MOS interface shown in Fig. 7(d), the thicknesses of the Al_2O_3 and SiO_2 layers on the Si waveguide are found to be 20.5 nm and 4.5 nm, respectively. We measured the dielectric constant of Al_2O_3 with a separate capacitor and calculated the EOT to be 20.5 nm using the thicknesses of the Al_2O_3 and SiO_2 obtained by the TEM image.

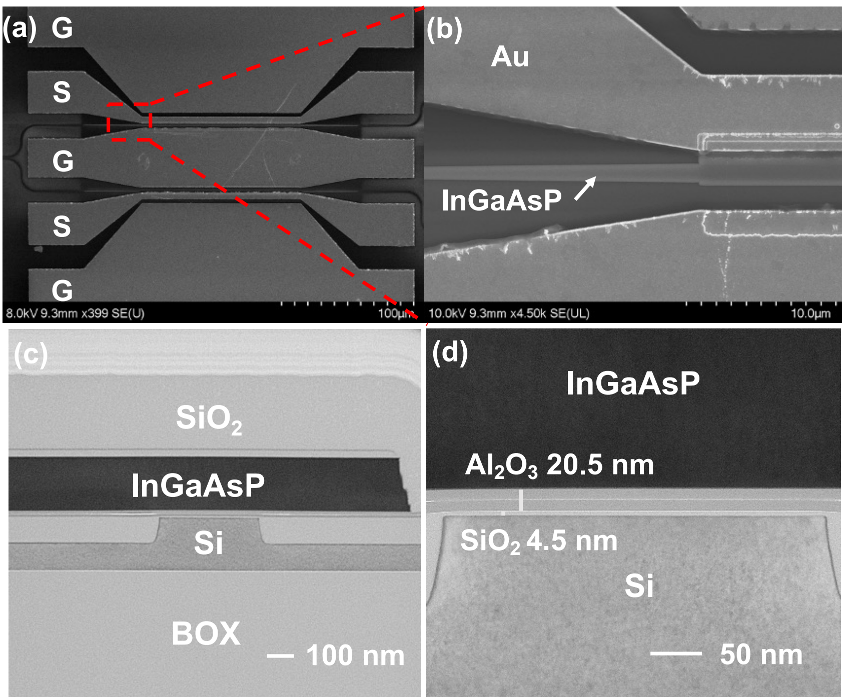

Fig. 7. (a)-(b) Plan-view SEM images of fabricated InGaAsP/Si hybrid MOS asymmetric MZM and (c)-(d) cross-sectional TEM images of InGaAsP/Si hybrid MOS optical phase modulator.

4. Measurement results

4.1. DC measurements

We measured the transmission spectra of the fabricated asymmetric MZM with an imbalanced length of 10 µm. The length of the hybrid MOS phase shifter was 120 µm. The length of the tapers at input and output ends of the hybrid MOS phase shifter was 40 µm. We chose the spectrum of O band and swept the gate voltage from -2 V (depletion) to 4 V (accumulation), as shown in Fig. 8(a). The MZM was driven with single-ended signal. The light from a tunable laser was coupled into the cleaved edge of the Si waveguide through a lensed single-mode optical fiber. The polarization was tuned to the TE mode of the Si waveguide. The output from the edge

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of the Si waveguide was coupled again into an optical fiber through an objective lens. Then, the output power was measured using an InGaAs optical power meter. The spectrum was normalized to optical source power and the maximum transmission was −14 dB, which includes the coupling loss of approximately −6 dB per facet of the edge coupler, the insertion of the phase shifter (−0.54 dB), and the loss of the Si passive waveguide (−1.46 dB). The measured spectrum shows an extinction ratio (ER) up to 30 dB. With forward bias up to 4 V on the single arm, the ER shows no obvious decreasing trend, indicating the small loss induced by phase modulation. We extract the phase shift from the resonance wavelength peak shift from the spectra and calculated $V_\pi L$ to be 0.245 Vcm as shown in Fig. 8(b), which is higher than the simulated $V_\pi L$ with 20 nm EOT (~0.2 Vcm). The slightly higher measured $V_\pi L$ than the simulated value and phase shift saturation at the accumulation region may originate from the Fermi level pinning due to interface traps at the MOS interfaces [20,21]. The device capacitance was measured at 1 MHz as shown in Fig. 8(c). When a gate voltage is swept from 4 V to -2 V, the capacitance decreases owing to carrier depletion at the MOS interface. The measured capacitance is 2.5 fF/µm in the accumulation mode (4 V), which is larger than the simulated value of the same structure with a 20-nm EOT (1.48 fF/µm). The extra parasitic capacitance has two sources. Firstly, the metal pad for InGaAsP has an overlap on the Si slab with a width of approximately 4 µm. The 300-nm-thick SiO_2 cladding between the pad and the Si slab leads to an extra parasitic capacitance of 0.46 fF/µm. Secondly, according to [6], the parasitic capacitance formed between metal vias and pads leads to extra 0.7 fF/µm increase in total capacitance. Considering these two extra parasitic capacitances, our measurement result matches well with the simulation result.

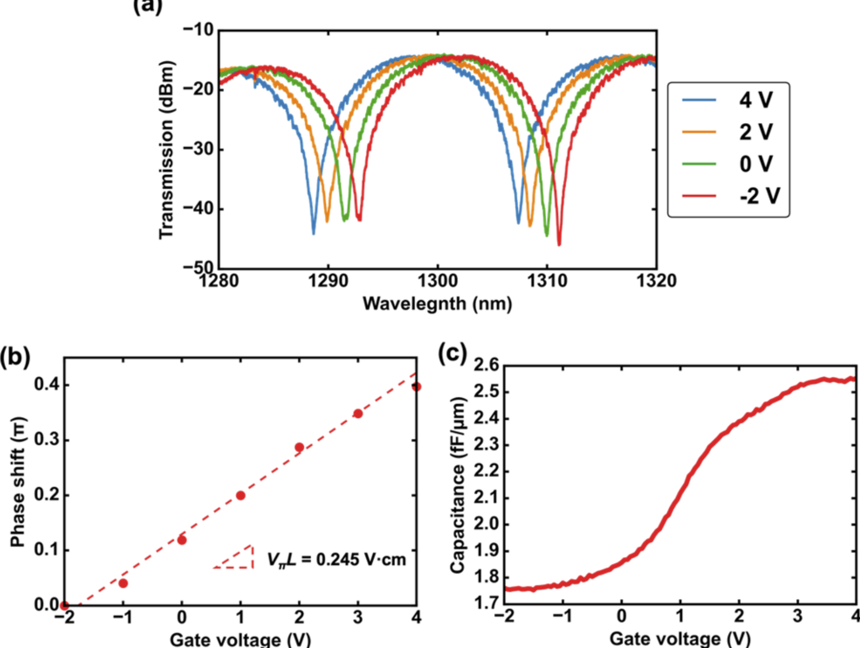

Fig. 8. (a) Measured transmission spectrum of the InGaAsP/Si hybrid MOS MZI modulator under different gate biases. (b) Phase shift as a function of gate bias. (c) Device capacitance measured at 1 MHz.

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4.2. Dynamic measurements

Figure 9(a) shows the measured EO frequency response of the 240-µm-long modulator with different DC biases. When biased at -2 V, the 3 dB bandwidth is around 10 GHz. With forward bias, the 3 dB bandwidth drops to 6 GHz owing to the increase in the capacitance at the accumulation region. In the simulation result in Fig. 5, the 3 dB RC bandwidth are 17 GHz and 15 GHz for −2 V and 2 V gate voltages, respectively. We fitted the measured bandwidth at −2 V with RC model shown in Fig. 5(a) and found that difference between the measured and simulated 3 dB bandwidth can be attributed to the extra parasitic capacitance of 0.47 fF/µm and a contact resistance of 2.34 Ω·mm. Figure 9(b) shows the measured eye pattern with a 25 Gbps 2^{31}-1 pseudo-random binary sequence (PRBS-31) electrical modulation. The test device is driven with Vpp = 5 V and a −2 V DC bias at −3 dB point using differential drive signal. The lower half of the eye pattern becomes blurred owing to the smaller bandwidth at the accumulation region as shown in Fig. 9(a). Figure 9(c) shows the 40 Gbps eye pattern of PAM-4 measured at $V_{pp} = 5$ V. We obtained a clear eye opening without any pre-emphasis driving schemes.

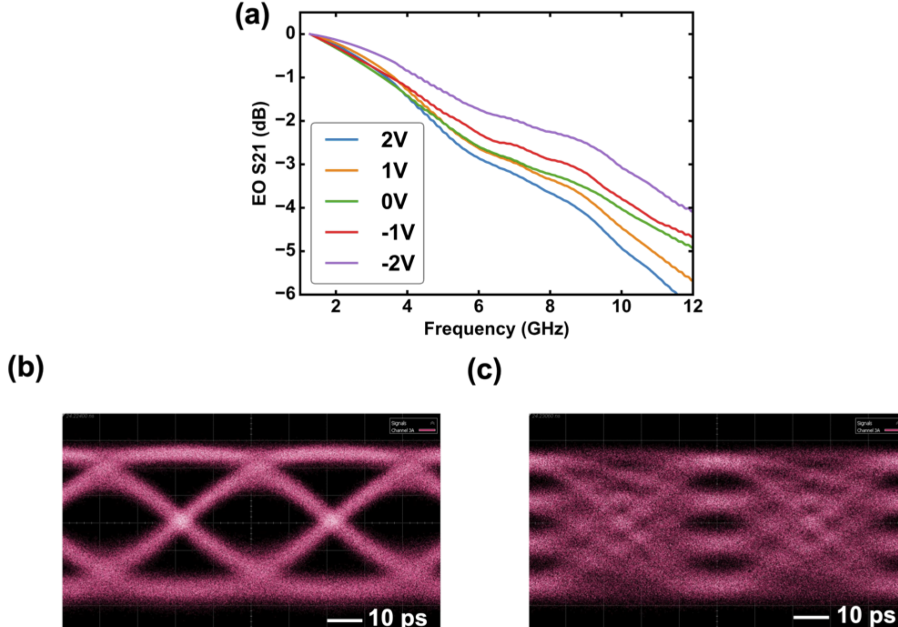

Fig. 9. (a) Measured EO frequency response of the 240-µm-long modulator with different biases. (b) Eye pattern modulated with 25 Gbps NRZ signal. (c) Eye pattern modulated with 40 Gbps (20 Gbaud) PAM-4 signal without pre-emphasis. The bias voltage is -2 V and V_{pp} is 5 V.

4.3. Benchmark and discussion

For benchmark, we compared the lumped InGaAsP/Si MOS, InP/Si MOS [16,22] GaAs/Si MOS [23], III-V/Si PN [24] and Si/Si MOS [18,25,26] modulators with modulation efficiency in terms of $V_{\pi}L$ and bit rate with NRZ modulation, as shown in Fig. 10.

For simulation results and references results with only frequency response, we convert the 3 dB bandwidth to NRZ bit rate with a factor of 2. The benchmark shows that, as compared with InP/Si and Si/Si MOS modulators, the InGaAsP/Si MOS modulator can achieve a similar bit rate but with a better modulation efficiency owing to the stronger free-carrier effect in n-type

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InGaAsP [10]. To consider the achievable bit rate of the InGaAsP/Si device, the simulated curves of the structures shown in Fig. 2(a) and 2(b) are respectively plotted as dashed and solid lines in Fig. 10. The result exhibits that the trade-off between the modulation efficiency and modulation bandwidth exists in lumped hybrid MOS optical phase shifter. Our experimental result is close to the simulation prediction with C_{slab} considered. The difference stems from extra parasitic capacitance and the contact resistance shown in Section 4.2, which can be optimized through fine tune of design and process. To further improve the trade-off between modulation efficiency and modulation bandwidth, the parasitic capacitance can be reduced by using the asymmetric Si waveguide as shown in Fig. 2(b) to shrink the overlap between the InGaAsP membrane and the Si slab, and by optimizing the shape of electrode pads. As the output impedance in the driver is the dominant resistance component, a smaller device length with a low capacitance is favorable for the lumped design. With ring resonators, we can obtain an adequate extinction ratio with a smaller phase shift and a smaller device length [27–29]. Another approach is the traveling-wave design. The simulation result of the traveling-wave InGaAsP/Si hybrid MOS modulator in the depletion mode is also included in Fig. 10 [30]. With a traveling-wave design, the modulation is no longer limited by the RC constant in an equivalent circuit, and by a careful design for velocity and impedance matching, the travelling-wave device can achieve over 100 GHz bandwidth.

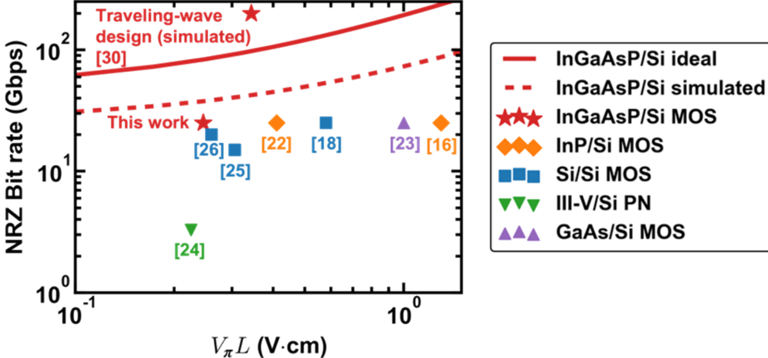

Fig. 10. Benchmark of InGaAsP/Si, InP/Si, III-V/Si PN and Si/Si MOS modulators with modulation efficiency ($V_\pi L$) and NRZ bit rate.

5. Conclusion

In this paper, the impact of the parasitic capacitance in the InGaAsP/Si hybrid MOS optical modulator on the modulation bandwidth was investigated. The numerical analysis revealed that the parasitic capacitance between the InGaAsP membrane and Si slab should be removed to improve the RC time constant. The fabricated InGaAsP/Si hybrid MOS optical modulator exhibited a 10 GHz 3 dB EO bandwidth with a $V_\pi L$ of 0.245 Vcm. We successfully obtained a clear eye opening with 25 Gbps NRZ and 40 Gbps PAM-4 signals. From the comparison with the numerical analysis, the modulation bandwidth can be increased further by removing the parasitic capacitance between the InGaAsP membrane and the Si slab. Moreover, it is also effective for higher bandwidths to introduce a ring resonator or a traveling-wave design for the next generation of integrated optical communication systems.

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Disclosures. The authors declare that there are no conflicts of interest related to this article.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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