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Novel high-speed monolithic silicon detector for particle physics

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Abstract: This contribution presents simulation results, implementation, and first tests of a monolithic detector developed at KIT. It consists of a sensor diode tightly integrated with an analogue front-end based on SiGe (Silicon-Germanium) SG13G2 130 nm BiCMOS technology produced at the Leibniz Institute for High Performance Microelectronics (IHP). The pixel size is 100 µm × 100 µm, and the nwell charge collection node dimensions were reduced to 10 µm × 10 µm. We investigate the influence of this approach on sensor performance, spatial resolution via charge sharing and timing behaviour.

Keywords: Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc); Front-end electronics for detector readout; Solid state detectors

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1 Introduction

Monolithic pixel sensors are used in high-energy physics (HEP) due to their high spatial resolution and small thicknesses, which gives significant advantages in detecting and tracking of charged particles. The most common form of monolithic pixel sensor implements Complementary Metal Oxid Semiconductor (CMOS) electronics on the same silicon die as the sensor diode. This technology offers micrometre spatial resolution, low material budget, low power consumption, and high scalability, even though some parameters such as signal-to-noise ratio, time resolution, and radiation tolerance are still prerogative of hybrid sensors [1].

To improve the signal-to-noise ratio, time, and spatial resolution, we have investigated the possibility of implementing a monolithic pixel sensor with SG13G2 130 nm BiCMOS technology from the Leibniz Institute for High Performance Microelectronics (IHP).[1] SiGe BiCMOS technology offers a standard silicon CMOS process with the addition of a high-performance SiGe Hetero-junction Bipolar Transistor (HBT). This technology has already been proven as a base for ultra-fast, low-power silicon pixel sensors. Moreover, it shows prominent time resolution results [2].

This sensor diode is the main component of a monolithic active pixel sensor (MAPS), the pixel size is 100 µm × 100 µm, and the nwell charge collection node is reduced to 10 µm × 10 µm.

2 Monolithic silicon detector design

The sensor structure and the size of the nwell sensor node have been simulated and optimised using Technology Computer-Aided Design (TCAD). The BiCMOS process allows the usage of both CMOS and bipolar transistors. The on-chip signal processing chain consists of a pre-amplifier and an output stage.

[1] https://www.ihp-microelectronics.com/.

2.1 Silicon sensor optimisation using TCAD

As a tool for simulation, TCAD by Synopsys was used.[2] It allows users to develop and optimise semiconductor process technologies and devices. Working on the sensor design, two primary TCAD tools were used: Sentaurus Structure Editor (SDE) for structure simulation and Sentaurus Device (SDEVICE) for device simulation.

The total sensor thickness is 50 µm with a p-type substrate. Pixel pitch was simulated in a range between 50 µm and 200 µm. The pixel pitch of 100 µm was found as an optimal value. At this pitch, the electric field is not distorted, causing premature breakdown between the nwell and the p-stops, and it is sufficiently small to grant total lateral depletion. This common depletion region enables the sensor's spatial resolution to benefit from charge sharing, by creating a signal not only in one but in several readout points. The size of the collection node is suitable for the placement of electronics in IHP SG13G2 technology. Figure 1 shows the electric field and depletion regions for different pixel pitch designs.

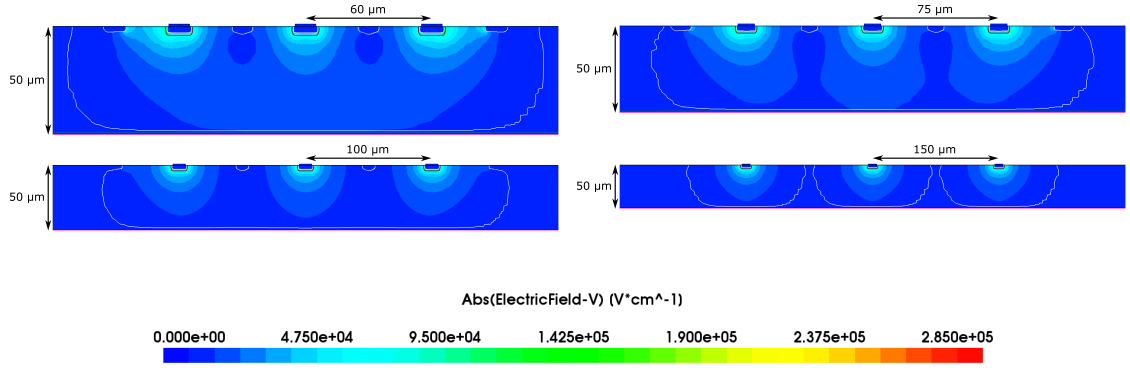

Figure 1. Electric field distribution for sensors with different pixel pitch. Colour gradient shows electric field with applied backplane voltage V = −100 V. White lines show depletion region.

To estimate charge sharing after the impact of a charged particle, the "Heavy Ion", "deep-level defects", and "interface defects" models were used [3, 4]. The "Heavy Ion" model is used to estimate charge distribution at different positions within the structure. A Minimum Ionising Particle (MIP) can be simulated with the Heavy Ion function of the Synopsys Sentaurus TCAD toolkit, with a Linear Energy Transfer function $\mathrm{LET}_f = 1.282 \times 10^{-5}\,\mathrm{pC} \cdot \mu\mathrm{m}^{-1}$, corresponding to an average of 80 $e - h$ pairs per micrometre [3]. Impact ionisation effects are considered using the avalanche model from the University of Bologna with electron/hole driving force. "Deep-level defects" includes radiation damage effects in silicon bulk. In this simulation "Hamburg Penta Trap Model" was applied. Interface properties such as silicon dioxide surface charge are defined as $N_{\mathrm{ox}} = 1 \times 10^{11}\,\mathrm{cm}^{-2}$ for non-irradiated and as $N_{\mathrm{ox}} = 3 \times 10^{12}\,\mathrm{cm}^{-2}$ for irradiated silicon [4]. The simulation result of a MIP particle impacting at a 45-degree angle on the sensor biased to −100 V is shown in figure 2. The charge carrier density before impact is shown in (a), where all equilibrium charge is evenly distributed between pixels. At the moment of impact (b), MIP goes through the centre pixel and creates a charge cloud in the active volume of the sensor. At a timestamp of 2 ns (c), this generated charge drifts mainly to the hit pixel but also to the neighbouring one. This illustrates possibility for

[2] https://www.synopsys.com/silicon/tcad.html.

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charge sharing effect. Also, the reset time for the detector can be estimated using the MIP simulation, where 4 ns after impact (d), the charge carrier density matches its initial state.

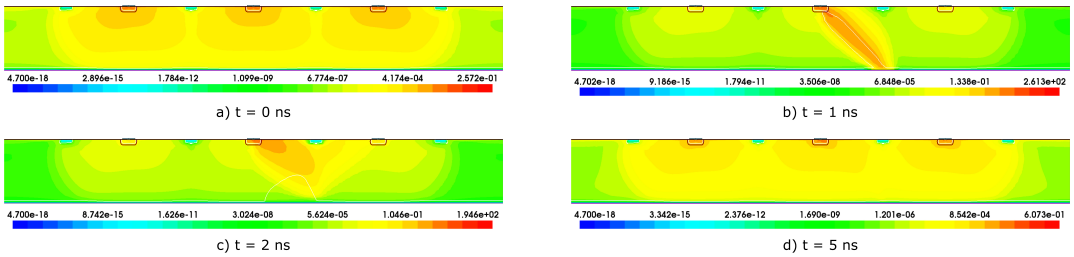

Figure 2. Charge sharing visualisation with MIP impact for 100 µm pixel pitch sensor.

2.2 Readout electronic design in SiGe BiCMOS technology

The schematic of chip electronics is presented in figure 3 (left). The sensor diode inside the pixel is biased by a PMOS transistor, which has a source and a gate connected to bond pads. This allows influencing the shape of the sensor signal, for example, the discharging time of the detector capacitance, by controlling applied voltages. A transconductance amplifier based on an HBT is placed inside the pixel. At the periphery of the chip, it is connected to a transimpedance amplifier by common base architecture. This architecture provides a low-impedance signal between the pixel and the periphery and allows high-speed signal transmission over long high-capacitance connection lines with relatively low power consumption.

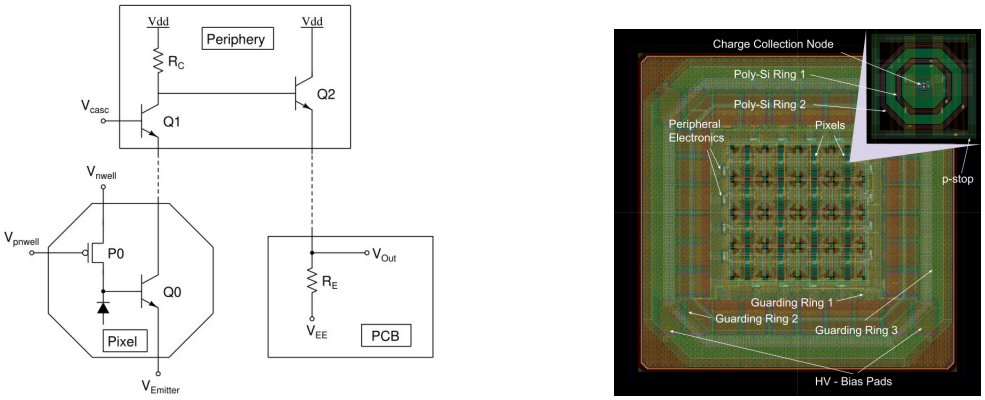

Figure 3. Schematic of readout electronics for one pixel (left) and layout of the sensor chip with pixel matrix, periphery and guard rings (right).

The emitter of the in-pixel HBT is also connected to bond pads in order to set the amplifiers and the pixel in operating mode. Since no digital readout is provided in this prototype, the analogue signal should be recorded by an oscilloscope. This is achieved by a PECL-based output buffer, where the analogue and a single-ended signal are transmitted.

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3 Implementation

The layout of the detector prototype is presented in figure 3 (right), including pixel layout. The pixel size is 100 µm × 100 µm. The 10 µm × 10 µm nwell collection node is surrounded by two poly-silicon rings. The pixel matrix comprises 4 × 4 pixels, each pixel separated by a p-stop. The total chip area is 1 mm × 1 mm.

Three guarding rings are implemented around the whole matrix, where the closest one is grounded and used as periphery placement for electronics. The other two additional guarding rings have individual pads, which create the opportunity of maintaining the electric field underneath by applying individual negative voltages. During the measurements, the rings were left floating. Four pads are implemented on the corners of the chip to bias the substrate with negative bias voltage.

This design has been produced and tested on two different substrates: a standard substrate of 50 Ωcm resistivity and an epitaxial substrate. The performance of both will be compared in the next section.

4 Primary measurements

High sensor currents, which are including dark- and photo-currents, significantly contribute to the detector's power consumption and sensor noise. The breakdown voltage defines the operational range of the sensor. We measured the sensor current over bias voltage for several sensors implemented on both standard and epitaxial substrates until the breakdown voltage was reached.

The breakdown voltages of all tested sensors are in the range of −70 V to −80 V for both substrates. The dark current of the chips of either substrate at a bias voltage of −50 V is in the order of 7 nA. Being exposed to daylight, the sensor current of the standard substrate increases to approximately 30 nA and the sensor current of the epitaxial substrate remains at 7 nA. Total noise is expected to be low due to decreased contribution of shot noise, which is related to low leakage current.

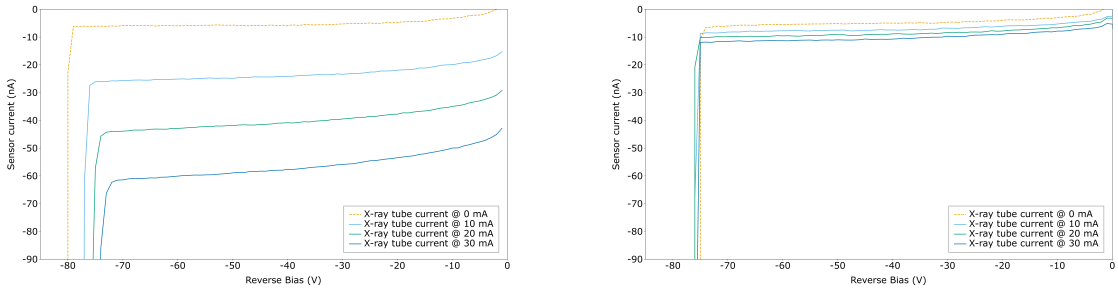

Figure 4. Sensor current for 50 Ωcm resistivity substrate (left) and epitaxial substrate (right).

The sensor was exposed to a steady X-rays beam for performance investigation. The used Tungsten X-ray tube setup has been described in [5]. The operation voltage is V_{max} = 60 kV and tube current can vary from 0 mA to 33 mA. In figure 4, IV-measurements of two chips with different substrates are presented. Breakdown voltage for 50 Ωcm resistivity substrate increases with dose rate and is in the range from −75 V to −80 V. The chip on epitaxial substrate shows dose rate independent behaviour and has a static breakdown voltage equal to −75 V. The sensor current of both substrate types increases with increasing dose rate.

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Table 1 shows the sensor current of both standard and epitaxial substrates for different dose rates, extracted from figure 4. It increases linearly with dose rate, approximately 5 times faster in case of standard than epitaxial substrate.

Table 1. Sensor current of the sensors at different X-ray tube settings at a bias voltage of −50 V.

X-ray dose rate	Standard substrate	Epitaxial substrate
0 Gy/h	5.7 nA	5.1 nA
24 Gy/h	25 nA	7.6 nA
48 Gy/h	42 nA	9.2 nA
73 Gy/h	59 nA	11 nA

For sensor illumination with electrons, we used encapsulated Strontium-90, which is a common source for MIP-like particles [6]. A centre pixel was connected to the oscilloscope to monitor the sensor's response to these particles. One of the observed waveforms is plotted in figure 5. The signal rise-time is in the order of 4 ns which agrees with simulations.

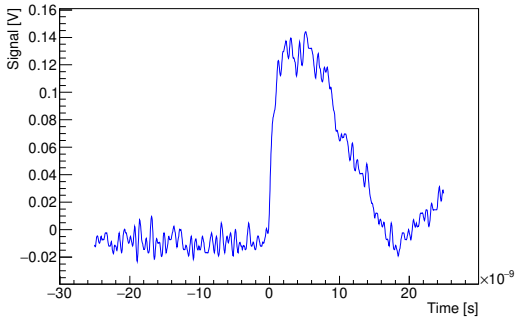

Figure 5. Waveform caused by a ^{90}Sr electron for 50 Ωcm resistivity substrate.

5 Conclusion

In this article, we have investigated the possibility of implementing a monolithic pixel sensor with high time and spatial resolution in SiGe BiCMOS technology of IHP. Our first prototype has 16 active pixels with 100 µm pitch and 10 µm × 10 µm n-type collection node. Simple pixel electronics that contain one SiGe bipolar transistor for amplification and one PMOS transistor for sensor bias are implemented inside the collection node. The rest of the readout chain is located in the chip's periphery.

This design has also been studied using TCAD simulations with different pixel geometries. Those simulations have indicated the capability of the sensor to share the charge between adjacent pixels, which will be the subject of upcoming tests. The first results prove that the sensor can detect MIP-like beta particles from a ^{90}Sr-source. The output signal has a fast rise time in the order of a few nanoseconds. Further measurements are needed to estimate the detection efficiency, spatial, and time resolution.

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References

[1] I. Perić, *A novel monolithic pixel detector implemented in high-voltage CMOS technology*, in the proceedings of the *2007 IEEE Nuclear Science Symposium and Medical Imaging Conference*, p. 1033–1039 [DOI:10.1109/NSSMIC.2007.4437188].

[2] G. Iacobucci et al., *A 50 ps resolution monolithic active pixel sensor without internal gain in SiGe BiCMOS technology*, 2019 *JINST* **14** P11008 [arXiv:1908.09709].

[3] G.-F. Dalla Betta et al., *Simulation of 3D pixel sensors cells*, AIDA-2020-D7.1 [https://aida2020.web.cern.ch/aida2020/].

[4] J. Schwandt et al., *A new model for the TCAD simulation of the silicon damage by high fluence proton irradiation*, in the proceedings of the *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference*, (2018) [DOI:10.1109/NSSMIC.2018.8824412] [arXiv:1904.10234].

[5] J.-O. Müller-Gosewisch, *Investigation of Radiation Damage in Silicon Sensors for the Phase-2 Upgrade of the CMS Outer Tracker*, Ph.D. Thesis, KIT, Karlsruhe, ETP (2021).

[6] A. Chilingarov, *Recommendations towards a standardisation of the macroscopic parameter measurements — Part II: MIP CCE measurements*, (2004), http://rd50.web.cern.ch/rd50/doc/Internal/rd50_2004_001.doc.

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