UNIVERSIDAD COMPLUTENSE DE MADRID

FACULTAD DE CIENCIAS FÍSICAS
DEPARTAMENTO DE FÍSICA APLICADA III
(ELECTRICIDAD Y ELECTRÓNICA)

TESIS DOCTORAL

Growth of high permittivity dielectrics by high pressure sputtering from metallic targets

Crecimiento de dieléctricos de alta permitividad mediante pulverización catódica de alta presión a partir de blancos metálicos

MEMORIA PARA OPTAR AL GRADO DE DOCTORA

PRESENTADA POR

María Ángela Pampillón Arce

DIRECTOR

Enrique San Andrés Serrano

Madrid, 2017

© María Ángela Pampillón Arce, 2016

UNIVERSIDAD COMPLUTENSE DE MADRID

FACULTAD DE CIENCIAS FÍSICAS

Departamento de Física Aplicada III (Electricidad y Electrónica)

Growth of high permittivity dielectrics by high pressure sputtering from metallic targets

Crecimiento de dieléctricos de alta permitividad mediante pulverización catódica de alta presión a partir de blancos metálicos

A dissertation submitted in partial fulfillment of the requirements for the degree of **Doctor in Physics** by:

Ms. María Ángela Pampillón Arce

Supervisor:

Prof. Enrique San Andrés Serrano

Madrid, 2016

A mis padres

AGRADECIMIENTOS / ACKNOWLEGDMENTS

En primer lugar, me gustaría agradecer a mi director de tesis, Prof. Enrique San Andrés Serrano, la oportunidad que me ha brindado permitiéndome realizar este trabajo durante estos años. Gracias por todo su esfuerzo, dedicación, confianza y por todas sus enseñanzas. Su labor ha sido mucho más que la de un director. Muchísimas gracias por todo.

Querría también agradecer a todos los miembros del grupo de *Láminas delgadas y microelectrónica* por aceptarme desde el primer momento como una más. Gracias al Prof. Germán González Díaz, al Prof. Ignacio Mártil de la Plaza, a la Profa. María Luisa Lucía Mulas, a la Profa. Margarita Sánchez Balmaseda y al Prof. Álvaro del Prado Millán. Gracias a la Dra. María Toledano Luque, al Dr. David Pastor Pastor, al Dr. Javier Olea Ariza, al Dr. Eric García Hemme, a D. Rodrigo García Hernansanz y a D. Daniel Montero Álvarez. Unas gracias especiales al Dr. Pedro Carlos Feijoo Guerro por ayudarme desde el primer momento y por su simpatía. Gracias a todos por sus enseñanzas, por las charlas, por su dedicación, por su disposición siempre, por su generosidad y por las risas. He sido tremendamente afortunada de haber podido realizar mi tesis con todos ellos. Gracias por enseñarme tanto.

Gracias a los miembros del departamento de *Física Aplicada III* por el buen ambiente. Gracias en especial a Dña. Mar Gálvez Díez por toda su ayuda administrativa y por su buena energía por las mañanas.

Gracias a Dña. Rosa Cimas Cuevas y D. Pablo Fernández Sáez del *C.A.I. de Técnicas Físicas* por su ayuda y asistencia en la fabricación de muestras y por sus charlas. También gracias a la magia de D. Fernando Herrera Fernández y D. Antonio Paz López.

Este trabajo no hubiera sido posible sin la ayuda del Dr. José Emilio Fernández Rubio del *C.A.I. de Espectroscopía* por las medidas de FTIR; de D. Ignacio Carabias Sánchez del *C.A.I. de Difracción de Rayos X* por el GIXRD; del Dr. Nevenko Biskup y del Dr. Adrián Gómez Herrero del *Centro Nacional de Microscopía Electrónica* por la fabricación de las muestras de TEM y el análisis de las mismas; del Prof. José Luis

García Fierro del *Instituto de Catálisis y Petroleoquímica* por los análisis de XPS; de Dña. Laura Casado Zueras, del Dr. Alfonso Ibarra Galián y del Dr. Rodrigo Fernández-Pacheco Chicón del *Instituto de Nanocienca de Aragón* por la fabricación y análisis de TEM.

Gracias al *Grupo de Caracterización de Materiales y Dispositivos Electrónicos* de la Universidad de Valladolid, en especial a la Profa. Helena Castán Lanaspa, al Prof. Salvador Dueñas Carazo y al Prof. Héctor García García por las medidas eléctricas y la ayuda en la compresión del análisis de los resultados.

Thank you very much to all the people of the PGI-9 at *Forschungszentrum Jülich* to accept me during six months. It was a real pleasure to be with you those months, learning and sharing talks. I will never forget those lunches at 11:00 am. Mahlzeit! Vielen Dank!

No puedo olvidarme tampoco de mi "familia española" durante mi estancia en Jülih. Hicistéis que esos meses lejos de casa fueran especiales e inolvidables. ¡Gracias!

Quisiera agradecer de manera muy especial a mi familia: mis padres, Maique y Fernando, por permitirme hacer lo que he querido siempre y por todo su apoyo. Sin duda, no hubiera llegado a esto sin ellos. También a mis hermanos, Fernando y Joaquín, a mi cuñada Almudena y al pequeño de la familia (por el momento), Yago. Son la familia que me ha tocado, pero me siento muy afortunada por ello.

Por último, gracias a todos mis amigos, por ser la familia que se puede elegir. Y gracias a esas personas que se han ido cruzando en mi camino, porque de una manera u otra, habéis hecho que sea también la persona que soy y que haya llegado hasta aquí.

Y gracias también a todas esas personas que están por llegar...

Marián Pampillón Arce

TABLE OF CONTENTS

Agradecimientos / Acknowlegdments i

Table of contents iii

List of figures vii

List of tables xvii

List of abbreviations xix

List of symbols xxi

Summary xxv

Resumen xxix

Chapter I: INTRODUCTION 1

I.1.- Historical evolution 2

I.2.- CMOS devices scaling 3

I.3.- High κ dielectrics 5

3.1.- Gadolinium oxide 9

3.2.- Scandium oxide 10

3.3.- Gadolinium scandate 10

I.4.- Metal gate electrodes 11

4.1.- Scavenging effect 11

I.5.- Alternative substrates 13

I.6.- High pressure sputtering (HPS) 13

I.7.- Alternative structures 15

I.8.- Outline of the thesis 16

References 17

Chapter II: FABRICATION TECHNIQUES 27

II.1.- High pressure sputtering (HPS) 28

II.2.- Glow discharge optical spectroscopy (GDOS) 31

2.1.- System I (monocromator) 32

2.2.- System II (spectrometer) 33

II.3.- Electron beam (e-beam) evaporation 34

3.1.- SiO_x acting as field oxide 37

3.2.- Metallic electrodes 37

II.4.- Lithography process 37
4.1.- Positive photoresist 38
4.2.- Negative photoresist.. 39
II.5.- Rapid thermal annealing (RTA) 40
II.6.- MIS fabrication.. 41
6.1.- Process without field oxide (FOX) 41
6.2.- Process with FOX 43
II.7.- Substrates.. 45
7.1.- Semiconductor materials.. 45
7.1.A.- Si wafers.. 45
7.1.B.- InP substrates.. 46
7.2.- Substrate surface cleaning.. 46
7.2.A.- Si wafers.. 46
7.2.B.- InP wafers.. 47
References 48
Chapter III: CHARACTERIZATION TECHNIQUES 51
III.1.- Structural characterization techniques 52
1.1.- Fourier transform infrared spectroscopy (FTIR).. 52
1.2.- Grazing incidence X ray diffraction (GIXRD) 56
1.3.- X ray reflectometry (XRR) 58
1.4.- X ray photoelectron spectroscopy (XPS).. 58
1.5.- Transmission electron microscopy (TEM).. 60
III.2.- Electrical characterization techniques.. 61
2.1.- MIS capacitors 62
2.1.A.- Ideal MIS capacitor in equilibrium 62
2.1.B.- Ideal MIS capacitor under bias.. 62
2.1.C.- Real MIS structure.. 64
2.2.- Capacitive behavior of MIS devices: C-V_{gate} characterization 64
2.2.A.- Effects of Q_{INS} in the C-V_{gate} characteristics.. 67
2.2.B.- Effects of D_{it} in the C-V_{gate} characteristics 67
2.2.C.- Effects of the oxide trapped charge in the C-V_{gate} characteristics 70
2.3.- Interfacial state density (D_{it}) determination 70
2.3.A.- Conductance method.. 70

2.3.B.- Deep level transient spectroscopy (DLTS) 72
2.4.- Leakage current density measurements 73
References 74
Chapter IV: THERMAL OXIDATION OF Gd_2O_3 79
IV.1.- Experimental method 80
IV.2.- Results and discussion 81
2.1. Plasma characterization of metallic Gd sputtered in Ar 81
2.2. Physical characterization of the thermally oxidized GdO_x films 83
2.3. Electrical characterization of MIS devices with thermally oxidized Gd_2O_3 ... 88
2.4. TEM analysis of MIS devices 91
IV.3.- Summary and conclusions 94
References 94
Chapter V: PLASMA OXIDATION OF Gd_2O_3 AND Sc_2O_3 97
V.1.- Experimental method 98
V.2.- Results and discussion 98
2.1.- Feasibility of the two-step deposition process for Gd_2O_3 and Sc_2O_3 98
2.1.A.- Plasma characterization of metallic Gd sputtered in Ar/O_2 atmosphere 98
2.1.B.- Plasma characterization of metallic Sc sputtered in pure Ar and mixed Ar/O_2 atmospheres 102
2.1.C.- Structural characterization of the plasma oxidized Gd_2O_3 films 103
2.1.D.- Structural characterization of the plasma oxidized Sc_2O_3 films 106
2.1.E.- Electrical characterization of MIS devices with plasma oxidized Gd_2O_3 and Sc_2O_3 106
2.2.- Optimization of the two-step deposition process for Gd_2O_3 109
2.2.A.- Oxidation power effect 110
2.2.B.- Initial metal deposition time influence 113
2.2.C.- Oxidation time 117
2.3.- Effect of FGA temperature on optimized MIS devices with plasma oxidized Gd_2O_3 123
2.4.- Electrical characterization of optimized MIS devices with plasma oxidized Sc_2O_3 130
V.3.- Summary and conclusions 134
References 135

Chapter VI: GADOLINIUM SCANDATE **141**
VI.1.- Experimental method 142
VI.2.- Results and discussion 143
2.1.- Plasma characterization 143
2.2.- Physical characterization 145
2.3.- Electrical characterization 150
VI.3.- Summary and conclusions 158
References 158
Chapter VII: INTERFACE SCAVENGING **161**
VII.1.- Experimental method 162
VII.2.- Results and discussion 162
2.1.- Thick Ti layers as top electrode with Gd_2O_3 162
2.2.- Optimization of the scavenging effect for plasma oxidized Gd_2O_3 165
2.3.- Scavenging effect for plasma oxidized Sc_2O_3 173
2.4.- Scavenging effect for plasma oxidized $Gd_{0.9}Sc_{1.1}O_3$ 176
VII.3.- Summary and conclusions 179
References 179
Chapter VIII: Gd_2O_3 ON InP SUBSTRATES **183**
VIII.1.- Experimental method 184
VIII.2.- Results and discussion 184
2.1.- Feasibility of plasma oxidized Gd_2O_3 deposited on InP substrates 184
2.2.- Optimized devices with Gd_2O_3 on InP 188
2.3.- Interface scavenging with InP 193
VIII.3.- Summary and conclusions 196
References 196
Chapter IX: CONCLUSIONS AND FUTURE WORK **201**
IX.1.- Conclusions 202
IX.2.- Future work 204
LIST OF PUBLICATIONS **205**
Journal papers 205
Conference contributions 207
Patent 211

LIST OF FIGURES

Figure I.1: Cross sectional sketch of a traditional n-MOSFET. The MOS structure is marked in this figure 2

Figure I.2: Leakage current density as a function of gate voltage for different SiO_2 thicknesses. Data are extracted from Taur *et al.*[16] 5

Figure I.3: Data and predicted data of the EOT as a function of the year. Provided by the 2013 edition of ITRS 7

Figure I.4: Bandgap as a function of the κ value for different dielectric materials. In dotted line is shown the inverse dependence. Data have been extracted from several references. In diamond symbols are represented the data of the materials used along this thesis. 8

Figure I.5: Schema of the scavenging process: the oxygen of the IL diffused through the high κ material and is dissolved by Ti, while the Si atoms are reincorporated to the substrate. 12

Figure I.6: Schema of a tridimensional tri-gate transistor from *Intel.*[121] 15

Figure II.1: Picture of the high pressure sputtering used for high κ materials deposition. 28

Figure II.2: Scheme of the high pressure sputtering used. 29

Figure II.3: Scheme of the glow discharge optical spectroscopy system I (monocromator) 32

Figure II.4: Scheme of the system II (spectrometer) to analyze the GDOS 33

Figure II.5: GDOS emission spectrum of a target sputtered in Ar during the conditioning process. H_2O band and N_2 peaks are marked in the figure. The remaining peaks are related to Ar I and Ar II 34

Figure II.6: Image of the e-beam evaporation system used in this thesis 35

Figure II.7: Scheme of the electron beam evaporation system 36

Figure II.8: Image of the *Headway Research* spinner (in the left hand side) and the *MJB3 UV400* alignment system (in the right hand side), used for the lithography process 38

Figure II.9: Image of the RTA system 40

Figure II.10: Dice of the lithography mask of the process without field oxide to define the top electrodes 41

Figure II.11: J-V_{gate} characteristics for the same sample measured applying more or less pressure to the needles 42

Figure II.12: Lithography mask used for the process with field oxide. In the left hand side is the mask used for opening the SiO_x windows and in the right hand side is for defining the top contacts. A pad and a device are marked in the figure 44

Figure II.13: Cross-section of MIS devices (a) without FOX and (b) with FOX (and pad) fabricated following the steps from subsection 6.1 and 6.2, respectively 45

Figure III.1: Schematic image of a Fourier transform infrared spectrometer 52

Figure III.2: FTIR spectra for (a) Si substrate with HF clean used for corrections, (b) as deposited Gd_2O_3 film (without the contribution of the Si substrate) and (c) Gd_2O_3 powder 55

Figure III.3: Schema of the GIXRD system used: β is a fixed angle while the detector performs a scan in 2θ 56

Figure III.4: GIXRD spectra of a Si substrate sputtered with Gd in an Ar/O_2 atmosphere. The observed diffraction peaks have been identified as monoclinic gadolinium oxide and are marked with black solid lines. Also, a Si substrate contribution is observed and is indicated with a grey dashed line 57

Figure III.5: Schematic of the XPS system used 59

Figure III.6: XPS wide scan or survey spectrum of $Gd_{0.9}Sc_{1.1}O_3$ sample. The identified peaks are related to Gd, C, Sc and O and are marked in the figure 60

Figure III.7: Schematic of the transmission electron microscope 61

Figure III.8: Band diagram of an ideal MIS structure in equilibrium 62

Figure III.9: Band diagram (and charge concentration) of an ideal MIS structure under bias. The accumulation (in the left hand side), depletion (in the center) and inversion (in the right hand side) situations are presented 63

Figure III.10: C-V_{gate} curves for low and high frequencies. In the figure are marked the four different situations of the MIS structure depending on the applied gate voltage ... 66

Figure III.11: Shift produced in the C-V_{gate} characteristics of a MIS structure as a consequence of the presence of $Q_{INS} > 0$ 67

Figure III.12: Interface states charge changes depending on the applied voltage to the MIS structure. A0 and D0 are neutral acceptors and donors, A− are the negatively charged acceptor states and D+ are the positive charged donor states 68

Figure III.13: Stretch-out of the C-V_{gate} curve as a consequence of the presence of a D_{it}. 69

Figure III.14: (a) Small signal equivalent circuit of a MIS device for conductance measurements and (b) measured circuit 71

Figure III.15: J-V_{gate} characteristic of a MIS device measured from inversion (negative voltages) to accumulation (positive voltages) 74

Figure IV.1: Simulation of the SiO_x thickness regrowth as a function of the oxidation temperature for bare-Si substrate implementing the Massoud oxidation model 80

Figure IV.2: Optical emission spectra of metallic Gd sputtered in an Ar plasma at room temperature with (a) *rf* power variation (from 10 to 30 W) and (b) an Ar pressure dependence (0.25-1.0 mbar). The ranges with the most important lines for Ar I, Ar II, Gd I and Gd II are indicated in the figure.. 82

Figure IV.3: Grazing incidence X-ray diffraction patterns of thick Gd layers (a) as-deposited and (b)-(f) oxidized at several temperatures (from 250 to 750 ºC). The observed diffraction peaks have been identified as hexagonal metallic gadolinium (dashed lines), monoclinic gadolinium oxide (solid lines) or cubic gadolinium oxide (dotted lines) 84

Figure IV.4: (a)-(d) GIXRD patterns of thin Gd films oxidized at several temperatures (from 350 to 750 ºC). The observed diffraction peaks have been identified as monoclinic gadolinium oxide (solid lines). The cubic gadolinium oxide is also shown (dotted lines) 85

Figure IV.5: X-ray reflection measurements of the Gd film oxidized at 750 ºC (solid line), and fit to a $Gd_2O_3/SiO_2/Si$ model (dashed line) 86

Figure IV.6: Thickness result of the XRR simulations to a $Gd_2O_3/SiO_2/Si$ bilayer model: Gd_2O_3 thickness (open symbols) and SiO_2 thickness (closed symbols). The uncertainty of these values can be estimated as ± 1.0 nm 87

Figure IV.7: FTIR spectra of thin Gd layers oxidized at several temperatures (from 350 to 750 ºC). The wavenumber of thermal SiO_2 stretching is marked by the dashed line 88

Figure IV.8: (a) Representative normalized capacitance curves as function of gate voltage of the $Al/Gd_2O_3/SiO_2/Si$ devices measured at 10 kHz for different oxidation temperatures (500-750 ºC) and FGA temperatures (300 ºC (with dashed lines) and 450 ºC (solid lines)). (b) Gate current density as a function of gate voltage for the same samples 90

Figure IV.9: D_{it} values as a function of different oxidation temperatures for FGA at 300 ºC (square symbols) and FGA at 450 ºC (circle symbols) 91

Figure IV.10: (a) and (b) Cross-sectional TEM images of the Gd_2O_3 films oxidized at 750 ºC. (c) and (d) Images of the films oxidized at 500 ºC. (a) and (c) high magnification images, used to measure Gd_2O_3 and SiO_x thickness and (b) and (d) low magnification images, where the density of domes can be observed. Samples were covered by Pt for protection during FIB sample preparation 93

Figure V.1: GDOS spectra of metallic Gd sputtered in an Ar/O_2 atmosphere at 0.50 mbar and at room temperature with different oxygen concentration (from 0 to 20%) at 30 W. The ranges with the most important lines for Ar I, Ar II, Gd I and Gd II are marked in the figure 99

Figure V.2: GDOS spectra of metallic Gd sputtered in a 95% Ar and 5% O_2 atmosphere at 0.50 mbar and at room temperature with different *rf* power varying from 30 to 50 W. The ranges with the most important lines for Ar I, Ar II, Gd I, Gd II and the most intense peak of O I are marked in the figure 100

Figure V.3: Cross-sectional TEM image of a bare Si substrate exposed to an Ar/O_2 plasma with 30 W and 0.50 mbar during 5 min at room temperature 101

Figure V.4: GDOS spectra of metallic Sc sputtered at 0.50 mbar and at room temperature for different *rf* powers in (a) a pure Ar atmosphere and (b) a 95% / 5% Ar/O_2 plasma. The most intense Sc I peaks are marked in the figure with dashed lines. In the inset of (a), an enlargement is made for the *rf* power of 30 W to observe the Ar I and Ar II peaks 102

Figure V.5: GIXRD spectra of bare Si substrates sputtered in Ar/O_2 atmosphere with Gd target and at different *rf* powers (from 30 to 50 W). The observed diffraction peaks have been identified as monoclinic gadolinium oxide and are marked with solid lines. 104

Figure V.6: Gd 4d doublet (left) and O 1s (right) core-level peaks and their fits taken from the surface of a ~3 nm thick film of Gd_2O_3 grown with a two-step method from a Gd target 105

Figure V.7: GIXRD spectra of bare Si substrates sputtered in Ar/O_2 atmosphere with Sc target and at different *rf* powers: 30, 40 and 50 W. The most intense peaks in the Sc_2O_3 cubic phase are marked in solid lines 106

Figure V.8: C-V_{gate} curves of MIS devices using (a) Gd_2O_3 and (b) Sc_2O_3 as dielectric with two metallic gates: Al in dashed lines and Pt/Al in solid lines. The capacitors were measured at 10 kHz and after a FGA at 300 ºC for 20 min 107

Figure V.9: Cross-sectional TEM images of the Gd_2O_3 films after a FGA at 300 ºC using (a) Al and (b) Pt/Al gate stack 109

Figure V.10: FTIR spectra for Gd_2O_3 samples with different oxidation *rf* power: 10, 20 and 30 W. Inset: SiO_x peak area as a function of the *rf* power for the same samples .. 110

Figure V.11: Normalized capacitance as a function of gate voltage before and after the FGA at 300 ºC for samples with different *rf* oxidation power: 10, 20 and 30 W......... 111

Figure V.12: Cross-sectional TEM images of the Gd_2O_3 films with 80 s of Gd and 300 s of plasma oxidation at (a) 30 W and (b) 20 W after a FGA at 300 ºC using Pt/Al gate stack 112

Figure V.13: FTIR spectra for Gd_2O_3 samples with different metal deposition time: 80, 120 and 160 s. Inset: SiO_x area as a function of the metal deposition duration for the same samples 114

Figure V.14: C-V_{gate} characteristics for samples with different initial Gd deposition time (varied between 80 to 160 s) before and after the FGA at 300 ºC 115

Figure V.15: HRTEM image of the Gd_2O_3 film with 160 s of Gd and 300 s of plasma oxidation at 30 W after a FGA at 300 ºC using Pt/Al gate stack 116

Figure V.16: FTIR spectra for Gd_2O_3 samples with different oxidation time: 150, 225 and 300 s. Inset: SiO_x area as a function of the oxidation time for the same samples . 118

Figure V.17: C-V_{gate} before and after the FGA at 300 ºC for samples with different oxidation duration: 150, 225 and 300 s 118

Figure V.18: Cross-sectional HRTEM image of the Gd_2O_3 film with 80 s of Gd and 150 s of plasma oxidation at 30 W after a FGA at 300 ºC using Pt/Al gate stack 119

Figure V.19: FTIR spectra for Gd_2O_3 samples with 120 s of Gd and different duration of the plasma oxidation: 100 and 300 s 120

Figure V.20: C-V_{gate} and G-V_{gate} curves measured at 10 kHz and after the FGA at 300 ºC for samples with 120 s of Gd and 100 (solid lines) and 300 s (dashed lines) of plasma oxidation at 20 W 121

Figure V.21: J-V_{gate} characteristic after FGA at 300 ºC for samples with Gd deposition during 120 s and a plasma oxidation of 100 (solid lines) and 300 s (dashed lines). In grey is represented the sample with 120 s of Gd oxidized during 300 s at 30 W fabricated without FOX as a comparison 122

Figure V.22: Normalized C-V_{gate} curves measured at 10 kHz before and after the FGA at representative temperatures for samples with (a) 80 s and (b) 120 s of Gd with a plasma oxidation during 100 s 124

Figure V.23: EOT (left) and D_{it} (right) as a function of the annealing temperature for samples with 80 s (squares) and 120 s (circles) of Gd oxidized for 100 s 125

Figure V.24: Interface trap density obtained by DLTS for sample with 80 s of Gd and 100 s oxidation measured after the FGA at 400 ºC 126

Figure V.25: J-V_{gate} characteristics before and after FGA at representative temperatures for (a) 80 s and (b) 120 s deposited Gd with a 100 s plasma oxidation 126

Figure V.26: J-V_{gate} curves for the sample with 80 s of Gd and 100 s of oxidation after FGA at 400 ºC, measured in several devices to observe breakdown events and reproducibility 127

Figure V.27: J-V_{gate} characteristics measured at different temperatures (from 100 to 300 K) for the sample with 80 S of Gd and 100 s oxidation after the FGA at 300 ºC. In the inset, the exponential slope of J at $V_{gate} > 1.3$ V as a function of the temperature is represented 128

Figure V.28: C-V_{gate} hysteresis curves for (a) 80 s of Gd sample and (b) 120 s of Gd with 100 s of plasma oxidation at 10 kHz after FGA at 400 ºC 128

Figure V.29: C-V_{gate} and G-V_{gate} curves measured at different frequencies after FGA at 400 ºC for the sample with 80 s of Gd oxidized during 100 s with 20 W of *rf* power. 129

Figure V.30: FTIR absorbance spectra for samples with 80 s of Sc and plasma oxidation duration of 100 and 300 s before the FGA 130

Figure V.31: FTIR spectra of the Sc_2O_3 sample oxidized during 100 s before and after the FGA at 300 and 450 ºC. Inset: SiO_x band area as a function of the FGA 131

Figure V.32: Cross-sectional HRTEM images of the ScO_x samples with 80 s of Sc and plasma oxidation carried out during (a) 100 s and (b) 300 s after FGA at 450 ºC....... 132

Figure V.33: C and G as a function of V_{gate} for samples with 80 s of Sc and an oxidation of 100 s before (dashed lines) and after the FGA at 300 ºC (solid lines)..... 133

Figure V.34: J vs V_{gate} for the samples with Sc deposited for 80 s and a plasma oxidation for 100 and 300 s before and after the FGA at 300 ºC 134

Figure VI.1: GDOS emission spectra of sputtered Gd in an Ar plasma at 30 W when the Sc *rf* power is (a) switched off and (b) on. The range where the most important lines of Gd I and Gd II are located is marked in the figure... 143

Figure VI.2: GDOS emission spectra of sputtered Sc in an Ar atmosphere at 30 W when the Gd *rf* power is (a) switched off and (b) on. Sc I and Sc II lines are marked in the figure with dashed and dotted lines, respectively. The rest of the peaks presented in the spectra are related to Ar I and Ar II.. 144

Figure VI.3: XPS wide scan or survey spectra of Gd_2O_3, $Gd_{2-x}Sc_xO_3$ and Sc_2O_3 samples after a FGA at 600 ºC. Gd $4d_{5/2}$, Sc $2p_{3/2}$ and O 1s peaks are marked in the figure.. 145

Figure VI.4: High resolution XPS spectrum for $Gd_{2-x}Sc_xO_3$ sample after a FGA at 600 ºC: Gd 4d (left) and Sc 2p (center) doublets and O 1s (right) together with their fits. 146

Figure VI.5: FTIR absorbance spectra for the as deposited Gd_2O_3, $Gd_{0.9}Sc_{1.1}O_3$ and Sc_2O_3 samples.. 147

Figure VI.6: FTIR spectra for the $Gd_{0.9}Sc_{1.1}O_3$ film before and after different FGAs.148

Figure VI.7: Grazing incident XRD spectra of $Gd_{0.9}Sc_{1.1}O_3$ film after a FGA at 600 ºC was performed. No diffraction peaks are observed 149

Figure VI.8: HRTEM cross-sectional image of $Gd_{0.9}Sc_{1.1}O_3$ sample obtained after the FGA at 600 ºC 149

Figure VI.9: Area normalized C and G as a function of V_{gate} characteristics for the $Gd_{0.9}Sc_{1.1}O_3$ sample before and after several FGAs at different temperatures............ 151

Figure VI.10: EOT (left) and D_{it} (right) values as a function of the annealing temperature for the sample fabricated with $Gd_{0.9}Sc_{1.1}O_3$ as dielectric 152

Figure VI.11: Hysteresis C-V_{gate} characteristics measured from inversion to accumulation and back again for the $Gd_{0.9}Sc_{1.1}O_3$ sample after several FGAs at different temperatures.. 154

Figure VI.12: Flatband voltage shift as a function of the annealing temperature for the $Gd_{0.9}Sc_{1.1}O_3$ sample 154

Figure VI.13: C-V_{gate} and G-V_{gate} curves measured at different frequencies for the $Gd_{0.9}Sc_{1.1}O_3$ sample after FGA at 600 ºC 155

Figure VI.14: J-V_{gate} characteristics for the $Gd_{0.9}Sc_{1.1}O_3$ sample before and after different FGAs 156

Figure VI.15: J-V_{gate} curves for the $Gd_{0.9}Sc_{1.1}O_3$ sample after an FGA at 600 ºC, measured in several devices to observe breakdown events and reproducibility 157

Figure VII.1: C-V_{gate} curves for the sample with 80 s of Gd and a 300 s plasma oxidation at 30 W measured before (dashed lines) and after the FGA at 300 ºC (solid lines) for two different top contacts: Pt/Al (as a reference) and thick Ti/Al 163

Figure VII.2: HRTEM images for the samples with long oxidation (300 s at 30 W) with two metallic contacts: (a) Pt (as a reference) and (b) thick Ti.................................... 165

Figure VII.3: C-V_{gate} curves for the sample with 80 s of Gd and an 100 s plasma oxidation at 20 W measured before and after several FGAs with different thickness of Ti layers: (a) 2.5 nm, (b) 5 nm and (c) 17 nm 166

Figure VII.4: EOT (left) and D_{it} (right) values as a function of the annealing temperature for the samples fabricated with different Ti thicknesses: 2.5, 5 and 17 nm. 167

Figure VII.5: J-V_{gate} curves for the sample with 80 s of Gd and 100 s plasma oxidation at 20 W measured before and after several FGAs with different thickness of Ti layers: (a) 2.5 nm, (b) 5 nm and (c) 17 nm 169

Figure VII.6: Interface trap density obtained by DLTS for sample with 80 s of Gd and 100 s oxidation at 20 W with 5 nm of Ti measured after the FGA at 400 ºC 170

Figure VII.7: (a) J-V_{gate} characteristics measured at different temperatures (from 100 K to 300 K) and (b) current electric field dependency fitting following the Poole-Frenkel model at several temperatures for the Si sample with 5 nm of Ti and after the FGA at 400 °C. The β_{PF} parameter is shown in the figure.. 171

Figure VII.8: C-V_{gate} frequency dispersion curves measured from 1 kHz to 1 MHz (left) and hysteresis measured at 10 kHz (right) for the sample fabricated with 5 nm of Ti and after the FGA at 400 ºC.. 172

Figure VII.9: C-V_{gate} curves for the sample with 80 s of Sc and 100 s plasma oxidation at 20 W measured before (left) and after the FGA at 300 ºC (right) for two different electrodes: 5 nm of Ti capped with Pt (in black) and Pt (in grey as a reference)......... 174

Figure VII.10: J-V_{gate} characteristics for the Sc_2O_3 sample (80 s of Sc and 100 s oxidation at 20 W) measured before (solid lines) and after the FGA at 300 ºC (dashed lines) for 5 nm of Ti capped with Pt (in black). As a reference, the Pt sample is represented in grey.. 175

Figure VII.11: C-V_{gate} characteristics of capacitors with $Gd_{0.9}Sc_{1.1}O_3$ formed after a FGA at 600 ºC using Ti as top electrode (in black) before (solid line) and after a second FGA at 300 ºC (dashed line). The same dielectric with Pt is represented as a reference in grey 177

Figure VII.12: J-V_{gate} curves for the $Gd_{0.9}Sc_{1.1}O_3$ sample formed after a FGA at 600 ºC measured before (solid line) and after a second FGA at 300 ºC (dashed line) with 5 nm of Ti capped with Pt (in black). As a reference, the Pt sample is represented in grey . 178

Figure VIII.1: Normalized C-V_{gate} and G-V_{gate} curves measured at 10 kHz before (dashed lines) and after the FGA at 400 ºC (solid lines). In black is represented the InP sample with 120 s of Gd and 200 s of plasma oxidation (performed at 20 W) with Pt/Al. Also, Si sample as a reference is depicted in the figure in grey 185

Figure VIII.2: High resolution TEM image of a MIS device with 120 s of Gd and plasma oxidized during 200 s after the annealing at 400 ºC 186

Figure VIII.3: Depth profile of a MIS device (120 s of Gd and 200 s plasma oxidation) with Pt/Al electrode after FGA at 400 ºC obtained from the EELS spectra during STEM measurements. Each emission line was normalized to its maximum value 187

Figure VIII.4: Gate leakage as a function of gate voltage of the InP devices with pure Pt gate electrode and different Gd sputtering times before (dashed lines) and after the FGA at 325 ºC (solid line) 189

Figure VIII.5: Gate normalized capacitance (left) and conductance (right) vs gate voltage of the devices with 120 s of Gd and a plasma oxidation of 100 s (at 20 W) with pure Pt electrode measured before and after the FGA at 325 ºC................................ 190

Figure VIII.6: Frequency dispersion C-V_{gate} curves measured from 100 Hz to 10 MHz for the InP sample with 120 s of Gd and 100 s oxidation after a FGA at 325 °C for 30 min 191

Figure VIII.7: Experimental data for V_{FB} as a function of the frequency measured for the InP sample with 120 s of Gd and a plasma oxidation of 100 s with Pt after the FGA at 325 °C and its linear fit... 192

Figure VIII.8: Normalized C-V_{gate} characteristics for the InP sample with 120 s of Gd and 100 s of plasma oxidation at 20 W measured at 10 kHz with 5 nm of Ti before and after the FGA at 325 ºC. The Pt sample is also shown as a reference in grey.............. 193

Figure VIII.9: C-V_{gate} curves measured at several frequencies (from 100 Hz to 10 MHz) for the InP sample with Ti after the FGA at 325 ºC 194

Figure VIII.10: Leakage current density as a function of V_{gate} for the Ti sample with GdO_x measured before and after the FGA at 325 ºC.. 195

LIST OF TABLES

Table IV.1: EOT values extracted from electrical measurements after FGA at 450 ºC and κ_{GdO} obtained from XRR and TEM thicknesses 89

Table V.1: EOT and D_{it} values extracted from electrical measurements after the FGA at 300 ºC for samples with different dielectrics obtained with the two-step method (Gd_2O_3 and Sc_2O_3) and two metallic contacts: Al and Pt/Al 108

Table V.2: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with different oxidation power. "---" means that the D_{it} value is under the detection limit of the method 111

Table V.3: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with different metal deposition duration. "---" means that the D_{it} value is under the detection limit of the method 115

Table V.4: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with different oxidation duration step. "---" means that the D_{it} value is under the detection limit of the method 118

Table V.5: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with 120 s of Gd and different plasma oxidation duration. 122

Table VII.1: EOT and D_{it} values extracted from electrical measurements before and after the FGA at 300 ºC for samples with 80 s of Gd and a plasma oxidation of 300 s (at 30 W) with two different top electrodes: Pt/Al and thick Ti/Al. "---" means that the D_{it} value is under the detection limit of the method 164

Table VII.2: EOT and D_{it} values extracted from electrical measurements before and after the FGA at 300 ºC for samples with 80 s of Sc and a plasma oxidation of 100 s (at 20 W) with two different top electrodes: 5 nm of Ti capped with Pt and Pt layers 175

LIST OF ABBREVIATIONS

Abbreviation	Meaning
ALD	Atomic layer deposition
BOE	Buffer oxide etching
CCD	Charge coupled device
CMOS	Complementary metal-oxide-semiconductor
CZ	Czochralski
DI	Deionized
DLTS	Deep level transient spectroscopy
DMSO	Dimethyl sulfoxide
DSP	Double side polished
e-beam	Electron beam
EDX	Energy dispersive X ray spectroscopy
EELS	Electron energy loss spectroscopy
FGA	Forming gas anneal
FIB	Focused ion beam
FOX	Field oxide
FTIR	Fourier transform infrared spectroscopy
FZ	Float zone
GDOS	Glow discharge optical spectroscopy
GIXRD	Grazing incidence x ray diffraction
HPS	High pressure sputtering
HRTEM	High resolution transmission electron microscopy
IC	Integrated circuit
IL	Interlayer
IPA	Isopropyl alcohol

ITRS	International Technology Roadmap for Semiconductors
MBE	Molecular beam epitaxy
MFC	Mass flow controller
MIS	Metal-insulator-semiconductor
MOCVD	Metal-organic chemical vapor deposition
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
PLD	Pulsed laser deposition
PVD	Physical vapor deposition
RCA	Radio Corporation of America
rf	Radiofrequency
RTA	Rapid thermal annealing
SC	Standard clean
SMU	Source measuring unit
SSP	Single side polished
STEM	Scanning transmission electron microscopy
TCAD	Technology computer aided design
TEM	Transmission electron microscopy
ULSI	Ultra large-scale integration
USB	Universal serial bus
VLSI	Very large-scale integration
XPS	X ray photoelectron spectroscopy
XRD	X ray diffraction
XRR	X ray reflectivity

LIST OF SYMBOLS

Symbol	Unit	Description
$\alpha(\omega)$	m^{-1}	Absorbance in FTIR
β	deg or rad	Incident angle in GIXRD
β_{PF}	$eVm^{1/2}/V^{1/2}$	Poole-Frenkel coefficient
ΔC	C	Capacitance difference
ΔG	J/mol	Change in the Gibbs energy
ΔV_{FB}	V	Flatband voltage shift
ε_0	F/m^2	Permittivity of free space
θ_{hkl}	deg or rad	Diffracted angle in GIXRD
2θ	deg or rad	Angle of the scan in GIXRD
κ	Adim.	Relative permittivity
κ_{eff}	Adim.	Effective relative permittivity
κ_s	Adim.	Semiconductor relative permittivity
$\kappa_{high\ \kappa}$	Adim.	Relative permittivity of the high κ material
κ_{SiO}	Adim.	Relative permittivity of SiO_2
λ	m	Wavelength
μ	m^2/Vs	Mobility
ν	m^{-1}	Wavenumber
τ_e	s	Emission time constant in DLTS
Φ_{MS}	eV	Work function differences between the metal and the semiconductor
ω	rad/s	Angular frequency
BE	eV	Binding energy
c	m/s	Light velocity

C	$\mu F/cm^2$	Capacitance per area unit
C	F	Capacitance
C_0	F	Capacitance at t = 0
C_{accum}	$\mu F/cm^2$	Measured accumulation capacitance per unit area
C_{HF}	F	High frequency capacitance
C_{INS}	F	Insulator capacitance
C_{it}	F	Interface capacitance
C_{LF}	F	Low frequency capacitance
C_m	F	Measured capacitance
$C_{m,a}$	F	Measured capacitance in accumulation
$C_{m,corr}$	F	Corrected measured capacitance
C_{ox}	$\mu F/cm^2$	Oxide capacitance density
C_s	F	Semiconductor capacitance
CET	nm	Capacitance equivalent thickness
d_{hkl}	m	Interplanar distance
D_{it}	$eV^{-1}m^{-2}$	Interface trap state density
E	V/m	Electric field (Poole-Frenkel equation)
E_C	eV	Conduction band energy
E_{Fi}	eV	Intrinsic Fermi level
E_{Fm}	eV	Metal Fermi level
E_{Fs}	eV	Semiconductor Fermi level
E_g	eV	Bandgap energy
E_k	eV	Kinetic energy
E_V	eV	Valence band energy
EOT	nm	Equivalent oxide thickness

$EOT_{high\ \kappa}$	nm	EOT related to the high κ
EOT_{IL}	nm	EOT related to the IL
f	Hz	Frequency
F_{ox}	V/m	Electric field oxide
G	S	Conductance
G/A	S/cm^2	Conductance per area unit
G_m	S	Measured conductance
$G_{m,a}$	S	Measured conductance in accumulation
$G_{m,corr}$	S	Corrected measured conductance
G_p	S	Parallel conductance
hv	eV	Incident beam energy
I	W	Resultant beam intensity in FTIR
I	A	Current
I_0	W	Initial beam intensity in FTIR
I_0	A	Pre-exponential factor in the Poole-Frenkel equation
I_D	A	Drain current
$I_{D,sat}$	A	Saturation drain current
I_t	W	Transmitted beam intensity in FTIR
$I(\infty)$	Adim.	Integration constant in FTIR
J	A/cm^2	Gate leakage current density
k	eV/K	Boltzmann's constant
L	m	Channel length
n	Adim.	Positive integer in GIXRD
N_D	cm^{-3}	Donor doping concentration
$n_T(0)$	cm^{-3}	Electron trapped concentration at t = 0

p	mbar	Pressure
P	W	Power
q	C	Electron charge
Q	C	Charge
Q_f	C	Fixed oxide charge
Q_{gate}	C	Gate charge
Q_{INS}	C	Insulator charge
Q_{it}	C	Interface charge
Q_{ot}	C	Oxide trapped charge
Q_s	C	Semiconductor charge
R_s	Ω	Series resistance
t	m	Insulator thickness
$t_{high\ \kappa}$	m	High κ material thickness
t_{IL}	m	Interlayer thickness
t	s	Time
t_i	s	Specific time in DLTS (i = 1,2)
T	ºC or K	Temperature
$T(\omega)$	Arb. Units	Transmittance in FTIR
V_D	V	Drain voltage
V_{FB}	V	Flatband voltage
V_{gate}	V	Gate voltage
V_T	V	Threshold voltage
W	m	Channel width
x	m	Position of the mobile mirror in FTIR

SUMMARY

The integrated circuit based on complementary metal-oxide-semiconductor (CMOS) devices is currently the dominant technology in the microelectronic industry. Their success is based on their low static power consumption and their high integration density. The metal-oxide-semiconductor field effect transistors (MOSFETs) are the main component of this technology. Their dimensions have been decreasing during the last years following the Moore's law. This downscaling has made possible their continuous performance improvement.

However, the size shrinking produced an excessive increase in the leakage current density that made this technology to face several challenges. The introduction of high permittivity (κ) dielectrics permits the use of a thicker insulator film (thus, reducing the leakage current) but with a lower equivalent SiO_2 thickness (EOT). Besides, the introduction of these materials also required a change in the poly-Si electrode, that became a pure metal.

The main objective of this thesis was the fabrication of metal-insulator-semiconductor (MIS) structures using high κ dielectrics grown from metallic targets. This was performed by means of high pressure sputtering (HPS). The advantage introduced by this system is that, due to the high working pressure, the particles suffer many collisions (because their mean free path is much lower than the target-substrate distance) and get thermalized before reaching the substrate in a pure diffusion process. This way, the semiconductor surface damage is preserved. The key novelty of this work consisted on the fabrication process using metallic targets. A two-step deposition process was developed: first, a thin metallic film is sputtered in an Ar atmosphere and, afterwards, this film was *in situ* oxidized.

The main objective was the fabrication of $GdScO_3$ (a high κ dielectric that presents interesting and promising properties) from metallic Gd and Sc targets. Since co-sputtering is not possible, a nanolaminate of these materials was necessary. With the aim of determining the growth properties and the interfacial quality of the binary oxides (Gd_2O_3 and Sc_2O_3), an initial study of those materials was performed.

For the characterization of the dielectric films and their interfaces between the insulator and the semiconductor, different techniques were used: Fourier transform infrared spectroscopy (FTIR), grazing incident X ray diffraction (GIXRD), X ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). In the other hand, for the electrical characterization, capacitance as a function of gate voltage (C-V_{gate}) and leakage current density vs gate voltage (J-V_{gate}) measurements were performed.

The *in situ* thermal oxidation of the Gd layer to obtain Gd_2O_3 did not provide an appropriate effective κ value, due to adhesion problems at the interface. For that reason, a different process was studied: the *in situ* plasma oxidation of the metallic layer in a mixed Ar/O_2 atmosphere. Using this two-step fabrication process, amorphous and stoichiometric Gd_2O_3 layers were obtained. With a shorter oxidation performed at 20 W, MIS devices were fabricated with an EOT of 2.2 nm showing good electrical behavior. The effective κ value was 11, due to a $GdSiO_x$ interfacial layer formation after the forming gas anneal (FGA).

For the Sc_2O_3 case, MIS devices with reasonable electrical characteristics and with 1.6 nm of EOT were obtained. The κ was 9, again related to a silicate formation at the interface.

Once these binary oxides were analyzed, $Gd_{0.9}Sc_{1.1}O_3$ films were fabricated. After a FGA at 600 ºC, amorphous and homogeneous layers were obtained, as demonstrated by TEM. However, MIS devices presented better leakage current density and lower hysteresis after a FGA at 500 ºC. The permittivity value obtained was 32, very promising for future CMOS generations.

During this work, it was also studied the effect of using different gate electrodes, studying Al (a material that reacts with the dielectric, increasing the EOT and, thus, reducing the κ value), Pt (a noble metal which does not react and it was used to study the bare properties of the insulator) and Ti (that is an oxygen scavenger which reduces the interlayer thickness and, therefore, permits achieving a lower EOT). In this thesis it was demonstrated the compatibility of the scavenging effect of the Ti electrodes with the three analyzed dielectrics. A reduction in the EOT value was observed for all the samples with Ti (as compared with Pt). Besides, it was found that an appropriate choice

of the Ti thickness and the FGA temperature were key parameters to achieve a controlled scavenging, that decreases the interlayer thickness without compromising the interfacial state density, D_{it}, and without degrading the dielectric.

Finally, MIS capacitors were fabricated on a high electron mobility semiconductor, such as InP. This way, it would be possible to increase the n-MOSFET current. The MIS devices grown with Gd_2O_3 as dielectric showed a full accumulation-depletion-inversion sweep even before the FGA and without surface passivation treatments. This implied an unpinned Fermi level. However, a high D_{it} was obtained, which indicated the necessity of a surface passivation treatment performed before the high κ dielectric deposition. Besides, the scavenging effect with this semiconductor was also demonstrated.

RESUMEN

Los circuitos integrados basados en los dispositivos CMOS (*complementary metal-oxide-semiconductor*) son en la actualidad la tecnología dominante de la industria microelectrónica. Su éxito se basa en su bajo consumo de potencia estática y en su alta capacidad de integración. Esto ha hecho que las dimensiones de los transistores de efecto campo metal-óxido-semiconductor (MOSFET, *metal-oxide-semiconductor field effect transistor*), que es el dispositivo principal de dicha tecnología, se hayan ido reduciendo durante los últimos años de acuerdo a la ley de Moore. A medida que los tamaños se fueron reduciendo, proceso habitualmente denominado escalado, las prestaciones de los transistores mejoraban.

Sin embargo, esta continua reducción de los transistores lleva asociada una excesiva corriente de fugas que hace que los transistores dejen de funcionar de una manera óptima. Por tanto, los dieléctricos de alta permitividad (κ) se introdujeron para permitir emplear aislantes de mayor espesor físico (y así reducir las fugas), pero con un menor espesor de óxido de silicio equivalente (EOT, *equivalent oxide thickness*). El cambio en el material aislante de la puerta lleva asociado también un cambio en el electrodo metálico.

El principal objetivo de esta tesis ha sido la fabricación de estructuras MIS (*metal-insulator-semiconductor*) empleando dieléctricos de alta κ a partir de blancos metálicos. Para su fabricación se empleó la técnica de pulverización catódica (*sputtering*) a alta presión. La ventaja que introduce la alta presión de trabajo es que las partículas sufren muchas colisiones (su recorrido libre medio es mucho menor que la distancia que hay entre el blanco y el sustrato), termalizándose y llegando al sustrato por un mecanismo de difusión, evitándose, de esta forma, un dañado de la superficie del semiconductor. La novedad de este trabajo ha estado en el proceso de fabricación, ya que se parte de blancos metálicos. Se ha desarrollado un proceso en dos pasos: primero se deposita una capa metálica en una atmósfera no reactiva de Ar y posteriormente se realiza una oxidación *in situ*.

El objetivo principal consistía en la fabricación de $GdScO_3$ (un dieléctrico de alta permitividad que presenta interesantes y prometedoras propiedades) a partir de blancos metálicos de Gd y Sc. Para ello, dado que el co-*sputtering* no es posible, se requirió el depósito inicial de un nanolaminado de dichos materiales. Con el fin de conocer las propiedades de crecimiento y la calidad de la intercara de los óxidos binarios que lo forman (Gd_2O_3 y Sc_2O_3), se realizó un estudio inicial de dichos materiales.

Para caracterizar el dieléctrico y la intercara entre el aislante y el semiconductor, se emplearon diversas técnicas: la espectroscopía infrarroja por transformada de Fourier (FTIR), la difracción de rayos X en incidencia rasante (GIXRD), la espectroscopía de fotoelectrones emitidos por rayos X (XPS) y la microscopía de trasmisión electrónica (TEM). Por otro lado, para la caracterización eléctrica se realizaron medidas de capacidad frente al voltaje de puerta ($C\text{-}V_{gate}$) y de corriente de fugas frente al voltaje de puerta ($J\text{-}V_{gate}$).

Dado que con la oxidación térmica *in situ* de una película de Gd para producir Gd_2O_3 no se obtuvo un valor adecuado de la permitividad efectiva, por problemas de adherencia en la intercara, se empleó un proceso diferente: la oxidación por plasma en atmósfera de Ar y O_2. Con este procedimiento, se obtuvieron películas de Gd_2O_3 amorfas y estequiométricas. Mediante una oxidación con menor duración y realizada a 20 W, se fabricaron dispositivos MIS con buena respuesta eléctrica, obteniéndose un EOT de 2.2 nm. El valor efectivo de la permitividad fue de solamente 11, debido a la formación de una capa de $GdSiO_x$ después del aleado en *forming gas*.

En el caso del Sc_2O_3, se fabricaron dispositivos con un EOT de 1.6 nm con características eléctricas razonables. La permitividad obtenida fue de 9, también relacionada con la formación de un silicato en la intercara.

Una vez analizados los óxidos binarios, se fabricó $Gd_{0.9}Sc_{1.1}O_3$. Después de un tratamiento térmico a 600 ºC, se obtuvieron películas amorfas y homogéneas. Sin embargo, las estructuras MIS analizadas presentaban mejores valores de la densidad de corriente y menor histéresis para un aleado a 500 ºC. Se pudo determinar que la permitividad era 32, muy prometedora para generaciones CMOS futuras.

En este trabajo, se ha analizado también el efecto de la composición del electrodo de puerta, estudiando el Al (que es un material que reacciona con el dieléctrico,

aumentando el EOT y, por tanto, reduciendo la permitividad), el Pt (metal noble que no reacciona y que sirve para analizar las propiedades de los aislantes) y el Ti (que es un material capaz de disolver oxígeno y reducir la intercara, obteniendo un EOT menor). Se ha demostrado, además, la compatibilidad del efecto carroñero (*scavenging*) del Ti con los tres dieléctricos analizados. Se obtuvo una reducción del EOT para todas las muestras estudiadas con Ti con respecto a las de Pt. También se comprobó que era crítica la elección del espesor de Ti y de la temperatura del tratamiento térmico posterior para conseguir un *scavenging* controlado, que redujera el espesor de la intercara sin comprometer seriamente la densidad de estados de la intercara, D_{it}, y sin degradar el dieléctrico.

Por último, se realizaron dispositivos MIS sobre un semiconductor por mayor movilidad de electrones, como el InP. De esta forma, es posible aumentar la corriente de los transistores. Los dispositivos MIS con Gd_2O_3 sobre InP presentaron un compartimiento eléctrico razonable, con curvas C-V_{gate} que mostraban un barrido completo acumulación-vaciamento-inversión, incluso antes de los tratamientos térmicos y sin realizar ningún tratamiento previo de pasivación de la intercara. Sin embargo, el alto valor de la D_{it} obtenido demuestra que es necesario un proceso previo de pasivación de los defectos de la superficie. También se ha demostrado que el proceso de *scavenging* es aplicable a estos semiconductores.

Chapter I:

Introduction

The integrated circuits (ICs) based on complementary metal-oxide-semiconductor (CMOS) devices are currently the dominant technology in the microelectronic industry. Its success is based on the low static power consumption and its high integration density.

During some decades, shrinking of these devices has been the key approach for the performance improvements of the metal-oxide-semiconductor field effect transistors (MOSFETs), following the Moore's law. However, the continuation of this trend faced several technological challenges. The materials typically used for these transistors (silicon, silicon dioxide and polysilicon) had to be replaced to continue with this tendency.

The first approach was the introduction of the high permittivity (high κ) dielectrics to replace SiO_2. Many materials were studied for this purpose. The replacement of the polysilicon used as the gate electrode by a metal gate came together with the dielectric change.

Besides, for the forthcoming years, the introduction of high mobility substrates, such as III-V semiconductors, will be a fundamental step to continue with the MOSFET size downscaling without losing the benefits of the high integration density.

In this thesis, different high κ dielectrics were studied: Gd_2O_3, Sc_2O_3 and $GdScO_3$. Besides, several top metal electrodes were analyzed in order to find the advantages and drawbacks of each material. Finally, the introduction of a high mobility substrate such as InP was also investigated.

I.1.- HISTORICAL EVOLUTION

The metal-oxide-semiconductor field effect transistors (MOSFETs) were patented by J. E. Lilienfeld in 1926.[1,2] Their basic principle was that the current flow between two terminals, source and drain, could be controlled by the voltage applied to a third one, the gate. However, several technological issues made not possible the practical development of these devices until some years later.

In 1947, while working in the characterization of semiconductor surface defects, J. Bardeem, W. Brattain and W. Shockley invented the germanium junction transistors at *AT&T's Bell Labs*.[3,4]

It was not until 1960 when the fabrication of the first MOSFET was possible. M. M. Atalla and D. Kahng, working at *Bell Labs*, overcame the technological challenges for this milestone.[5,6] This first transistor consisted on the growth of a silicon dioxide layer on a silicon wafer. This way the surface states were passivated and surface conductance modulation was finally achieved.

A MOSFET consists on a metal-oxide-semiconductor (MOS) capacitor, called the gate structure, and two p-n junctions, called source and drain. These transistors are used for amplifying or switching electronic signals and are the key devices of microprocessors and memory devices. During the first decades, the gate capacitor was formed by a SiO_2 layer, thermally grown on a top of a Si substrate. The metallic electrode was polysilicon. In Figure I.1 is represented the cross sectional image of a traditional n-MOSFET.

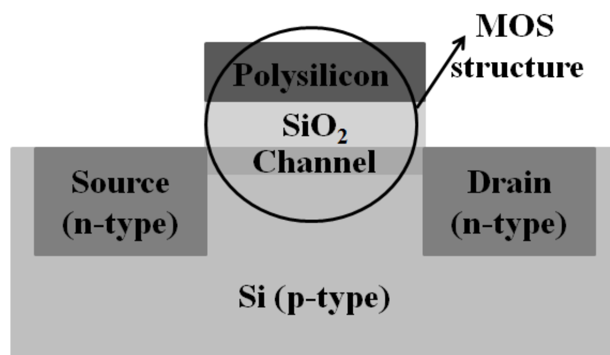

Figure I.1: Cross sectional sketch of a traditional n-MOSFET. The MOS structure is marked in this figure.

With the aim of improving the benefits of the discrete transistors, the IC was invented. The idea behind this concept was that when all the electronic devices of a circuit were fabricated monolithically in a small surface of a semiconductor material, the probability of obtaining a functioning circuit was similar to the probability of having just one working discrete device. This way, a huge reduction in cost and size could be achieved. The first developments were done in 1949 by W. Jacobi at *Siemens AG*.7 Some years later, J. Kilby working at *Texas Instruments* solved technological problems and patented the principle of integration.8 K. Lehovec, at *Sprague Electric Company* developed a method to isolate different components on a chip.9 Finally, R. N. Noice of *Fairchild Semiconductor* invented a way to interconnect the IC components[10] that improved the J. Hoerni version laying the foundations of the planar technology.[11]

I.2.- CMOS DEVICES SCALING

G. Moore, in 1965, predicted that the number of transistors in an IC would double every year.[12] Later, he revised his prediction: the doubling would occur every two years.[13] This statement became to be known as Moore's law.

In 1963, F. M. Wanlass working at *Fairchild Semiconductor* patented the CMOS technology.[14] This used complementary pairs of p-type and n-type MOSFETs. The benefits of this technology were its simplicity, in addition to the high integration density and the lower static power consumption compared to other technologies. This technology was first implemented in 1968 by *Radio Corporation of America* (RCA) in their 4000 series, and since then still remains as the workhorse of the IC industry, due to the continue demand for increasing the performance of the devices while decreasing the power consumption.

As it was mentioned in the former section, during some decades, MOSFETs used SiO_2 as the dielectric layer. The advantages of using this material are several. First, SiO_2 can be thermally grown on Si, and it grows in an amorphous phase. This native layer is thermodynamically stable on Si. Second, the Si/SiO_2 structure presents a high quality interface, with an interfacial state density (D_{it}) in the order of 10^{10} $eV^{-1}cm^{-2}$ (as a reference, the silicon (100) plane has an atomic density of 6.78×10^{14} atoms/cm^2). Finally, SiO_2 acts as a good electrical insulator with a wide bandgap (E_g) around 9 eV.

In order to reduce the dimensions of these transistors to improve the integration density and the operation speed, the thickness of this oxide film had to be decreased. Otherwise, short channel effects would make apparition (in other words, the gate would lose control of the channel conductance).

The drain current of these transistors can be expressed as:

$$I_D = \frac{W}{L}\mu C_{ox}\left(V_{gate} - V_T - \frac{V_D}{2}\right)V_D \qquad \textbf{(I.1)}$$

where *W* and *L* are the channel width and length, respectively, μ is the substrate carrier mobility, C_{ox} is the oxide capacitance density, V_{gate} it the gate voltage, V_T, the threshold voltage and V_D, the drain voltage. This equation is valid for $V_D < V_{gate} - V_T$.

As it can be seen, I_D increases linearly with V_D, until it saturates, reaching a maximum when $V_D = V_{gate} - V_T$. In this situation, the saturation drain current is given by:

$$I_{D,sat} = \frac{W}{L}\mu C_{ox}\frac{\left(V_{gate} - V_T\right)^2}{2} \qquad \textbf{(I.2)}$$

Therefore, this value can be increased by either reducing *L* or increasing C_{ox}. Besides, an increase in μ by changing the semiconductor material would increase this value. In section I.5 other alternative semiconductors with high mobility will be studied. The rest of the parameters cannot be easily modified.

Focusing on C_{ox}, this value can be expressed by:

$$C_{ox} = \frac{\varepsilon_0 \kappa}{t} \qquad \textbf{(I.3)}$$

being ε_0 the permittivity of free space (8.85×10^{-14} F/cm^2), κ, the dielectric constant of the insulator material (the relative permittivity) and *t* is the dielectric thickness.

Hence, one way for improving this oxide capacitance density (and, consequently, increase the drain current) is to reduce the oxide thickness and, the other, is to increase the permittivity value.

The SiO_2 thickness has been continuously reduced during some decades. For $t < 1.5$ nm, the leakage current density through the insulator due to tunneling is extremely high and the power consumption is unacceptable.[15] In Figure I.2, the leakage current density, J, as a function of the gate voltage is represented for several SiO_2

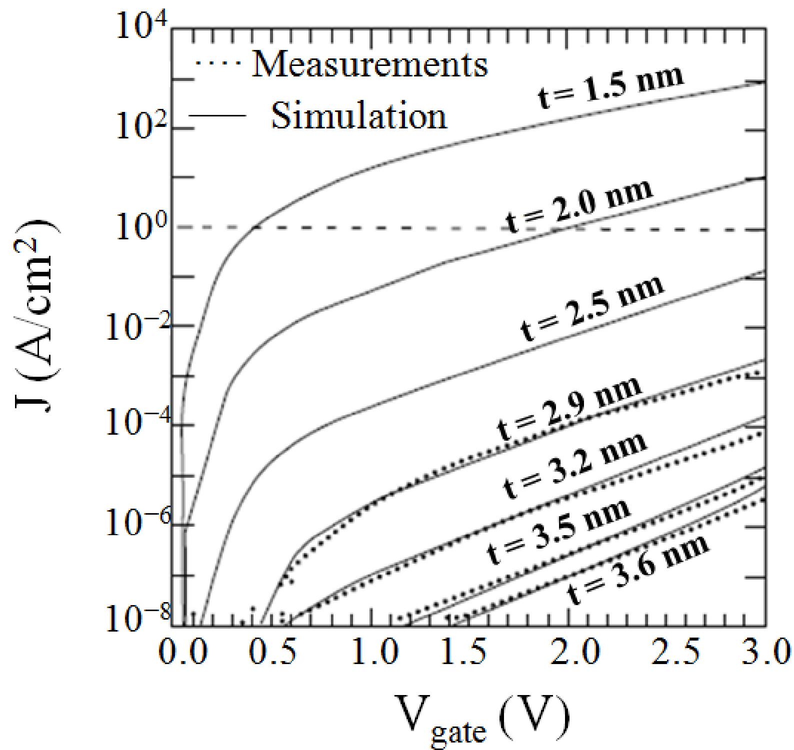

Figure I.2: Leakage current density as a function of gate voltage for different SiO_2 thicknesses. Data are extracted from Taur *et al.*[16]

thicknesses. These data are obtained from Y. Taur *et al.*[16] There, it can be observed a great increase in the leakage current while the oxide thickness is reduced, being $J \sim 100$ A/cm^2 for $V_{gate} = 1.5$ V when $t = 1.5$ nm. Thus, this material has reached its thickness limit. For this reason, the introduction of alternative insulator materials with a higher κ value than SiO_2 is required in order to keep on with the device downscaling.

I.3.- HIGH κ DIELECTRICS

The main advantage of introducing these high κ materials in the MOS structures (also called metal-insulator-semiconductor (MIS) devices) is the possibility of having a thicker dielectric film, with the aim of reducing the leakage current, while maintaining the oxide capacitance value.

The equivalent oxide thickness (EOT) of a high κ dielectric film can be defined as the thickness of the SiO_2 layer that would be required to achieve the same capacitance behavior of the structure using a thicker high κ dielectric layer. It can be estimated by:

$$EOT = \frac{\kappa_{SiO}}{\kappa_{high\ \kappa}} t_{high\ \kappa} \tag{I.4}$$

where κ_{SiO} and $\kappa_{high\ \kappa}$ are the dielectric constant of SiO_2 (with a value of 3.9) and the high κ material, respectively, and $t_{high\ \kappa}$, the thickness of this dielectric film.

To obtain the EOT, it is necessary to fit the capacitance-voltage ($C\text{-}V_{gate}$) curve taking into account quantum corrections. If the semiconductor is Si, there are many well characterized algorithms[17] that can be employed and obtaining this value is quite straightforward. During this thesis, to obtain the EOT value, we have used the CVC algorithm developed by J. R. Hausser and K. Ahmed.[18] However, with alternative substrates, using these algorithms is not direct and thus, as a simple alternative, the capacitance equivalent thickness (CET) is typically used, which is defined with the next equation:

$$CET = \frac{\varepsilon_0 \kappa_{SiO}}{C_{accum}} \tag{I.5}$$

being ε_0, the permittivity of free space (8.85×10^{-14} F/cm^2) and C_{accum} is the measured accumulation capacitance per unit area extracted from the $C\text{-}V_{gate}$ curves. The difference with EOT is that no quantum corrections due to the surface accumulation layer are taken into account, therefore the EOT is lower than the CET. As an approximation of EOT, many groups make the following approximation: EOT = CET – 0.7. In other words, they assume that the accumulation capacitance contributes with a capacitance equivalent to 0.7 nm of SiO_2.

The *International Technology Roadmap for Semiconductors* (ITRS) predicts the trend that should follow the EOT as a function of the year. In Figure I.3 it is presented the tendency since 2000 and the prediction made by ITRS from 2013.[19] There, it can be observed a severe reduction in the EOT, which should achieve a value of 0.5 nm in 2024. For that reason, controlling this parameter is critical for the technology and to allow a good scaling of MOSFETs in the years to come.

To determine the best candidate as high κ material, several woks have been done.[15,20-22] These dielectrics have to meet certain requirements to be suitable for replacing SiO_2.[15,20,23,24] The most important ones are listed below:

a) A κ value higher than SiO_2 is required. Nowadays, it should be higher than 20 to allow the scalability during a reasonable number of year, but lower than 30 to avoid fringe effects.[25]

b) The conduction and valence band offsets from the semiconductor to the high κ material should be, at least, 1 eV to avoid Schottky emission and to minimize the leakage current. For this reason, a bandgap larger than 5 eV is also essential, due to band misalignments.

c) These materials are desirable to be amorphous and must maintain this phase along the fabrication process. The grain boundaries tend to increase the leakage current and changes in the grain structure could impact the κ value over the film, leading to variable electrical characteristics.

d) A high quality interface is mandatory to avoid the degradation of the carrier mobility. This implies a low D_{it} (in the order of 10^{11} $eV^{-1}cm^{-2}$ or lower).

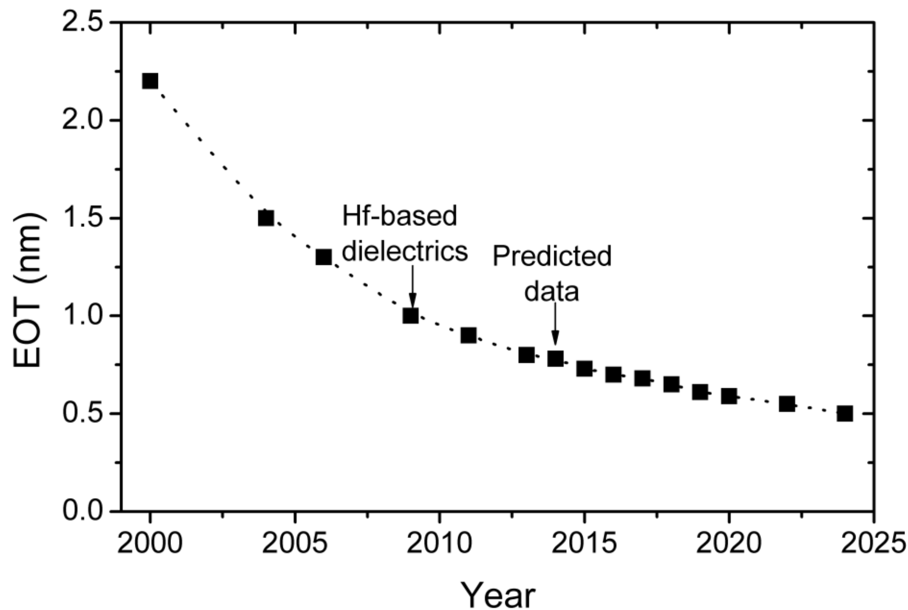

Figure I.3: Data and predicted data of the EOT as a function of the year. Provided by the 2013 edition of ITRS.

e) All the structure must be chemically and thermodynamically stable. This involves avoiding the formation of undesirable layers between the semiconductor and the high κ and between this dielectric material and the metal. Also, these materials must withstand all the processes and manufacturing temperatures.

The two first parameters are related: the bandgap value has an inverse dependence on the κ value[26] as it is presented in Figure I.4. There, it can be observed that it is important to have a trade-off between the bandgap and the permittivity value. This limits the number of possibly candidates that could be used to replace SiO_2.

According the last point, the formation of an interlayer (IL) between the high κ dielectric and the semiconductor would increase the total EOT. In this case, the gate stack is equivalent to two capacitors connected in series. For this reason, the total EOT can be expressed as:

$$EOT = EOT_{IL} + EOT_{high\,\kappa} \quad \textbf{(I.6)}$$

being $EOT_{high\,\kappa}$ and EOT_{IL}, the EOT related to the high κ and the IL, respectively.

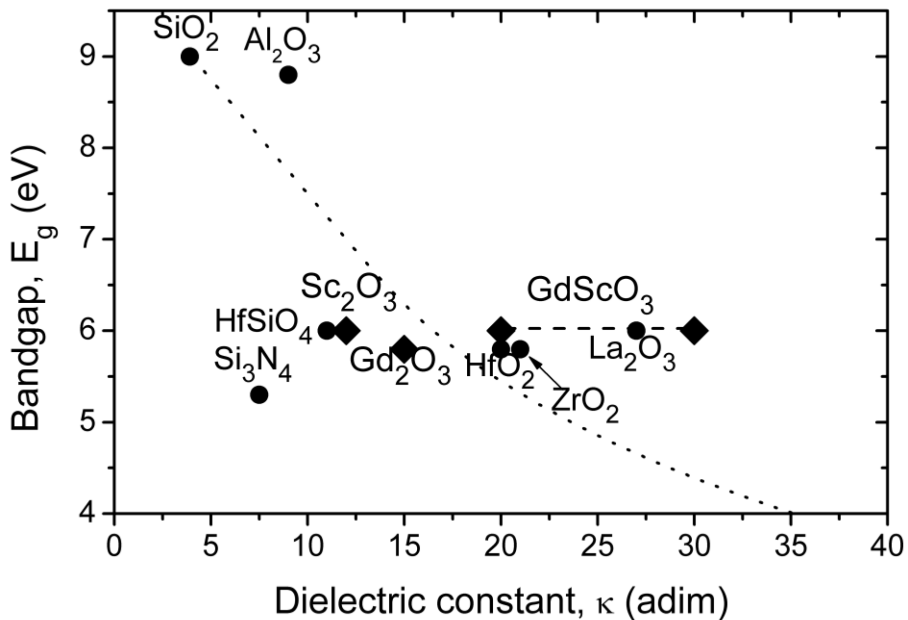

Figure I.4: Bandgap as a function of the κ value for different dielectric materials. In dotted line is shown the inverse dependence. Data have been extracted from several references. In diamond symbols are represented the data of the materials used along this thesis.

Therefore, reducing EOT_{IL} (or increasing the κ value of this layer) is necessary if a minimum EOT is desired. In subsection 4.1, this will be further explored.

In 2007, *Intel* announced the introduction of hafnium-based oxides in the 45 nm fabrication route.[27] At the same time, *IBM* manifested the necessity to the transition to these high κ materials.[28] The reason of using Hf-based dielectrics was due to its interesting properties[29]: a κ value ~20, a bandgap around 6 eV with large conduction and valence band offsets[30] and a good thermodynamic stability in contact with silicon.[31,32] The main drawback of this material is the low crystallization temperature (around 500 ºC).[33] To solve this, HfO_2 was alloyed with Si or Al, but at the expense of a decrease of the κ value.[34] Thus, other alternatives should be explored.

In this work, we have studied different candidates as high κ dielectrics for replacing HfO_2 on high performance MOSFETs: gadolinium oxide, scandium oxide and gadolinium scandate. Due to the better properties of $GdScO_3$, one of the main objectives of this thesis is to grow MIS devices with this material. The novelty of this work consists on the deposition of these films from pure metallic Gd and Sc targets by sputtering at high pressure, followed by an oxidation. This technique is a non-conventional method for high κ dielectric fabrication. In section I.6 the high pressure sputtering system will be introduced.

For this reason, it is also important to analyze first the growing properties of both binary oxides: Gd_2O_3 and Sc_2O_3.

3.1.- Gadolinium oxide

Gd_2O_3 is a rare earth oxide that has potential interest in a wide range of technological applications, such as optical,[35] magnetic[36] and microelectronic devices. In this last field, the applications of Gd_2O_3 are focused on memory devices[37,38] and as alternative high κ dielectric in MOS capacitors.[39-42]

The interest of this material is due to its promising properties: its relatively high permittivity value (κ ~ 15-17),[41,43] large bandgap (E_g ~ 6 eV)[43] with a proper band alignment[20] and chemical stability in contact with Si.[43-44] Besides, its compatibility with III-V semiconductor has been proved.[45-48] This is an interesting result in order to fabricate MOSFETs with high mobility substrates and good electrical performance.

Gd_2O_3 has been grown using different techniques: atomic layer deposition (ALD),[41,49] electron beam evaporation,[40,45] molecular beam epitaxy (MBE)[42] or radiofrequency, *rf*, sputtering from Gd_2O_3 target in Ar atmosphere and also from Gd target in a mixed Ar/O_2 plasma.[37-39]

3.2.- Scandium oxide

Sc_2O_3 has been also studied as high κ material.[50] Its permittivity value is around 13,[51,52] E_g ~ 6 eV[53] and, besides, it presents a conduction band offset to Si of 2 eV.[20] Additionally, a previous work predicted a good thermodynamic stability with Si.[31]

In principle, the κ value of this material is not very promising to replace HfO_2. However, the most interesting property of Sc_2O_3 is the possibility of mixing this material with rare earth oxides, such as Gd_2O_3, La_2O_3, Dy_2O_3, etc., to obtain ternary scandate materials, with higher κ values than those of its constituents oxides.[32,43,54]

3.3.- Gadolinium scandate

$GdScO_3$ belongs to the ternary rare earth scandate family. The rare earth scandate materials were introduced as high κ dielectrics for microelectronic applications some years ago because of their promising properties, such as high permittivity values, large bandgaps, an amorphous character and a good band alignment.[55-59]

Among them, $GdScO_3$ presents favorable characteristics for replacing Hf-based oxides.[60-62] It presents an outstanding thermodynamic stability with Si (for temperatures up to 1000 ºC it maintains its amorphous phase)[57,63] in addition to a higher κ value (between 20 and 30)[64], an E_g around 6 eV[55,56,59] with conduction and valence band offsets to Si around 2-2.5 eV.[56]

This material has been prepared using ALD,[54,61] electron beam evaporation,[58,60,63] pulsed laser deposition (PLD),[58,62] or metal-organic chemical vapor deposition (MOCVD).[64]

In addition, several $GdScO_3$ MOSFETs fabricated on different substrates (strained Si on insulator, SiGe or InAlN/AlN/GaN heterostructure, for instance) have been

reported with well behaved characteristics.[60,65,66] Besides, this material has been investigated as potential candidate for NAND flash memory.[43,54]

I.4.- METAL GATE ELECTRODES

The introduction of high κ dielectrics in the gate stack structure made also necessary the replacement of the top metallic electrode.[15,24] During some decades, polysilicon (polycrystalline silicon doped up to degeneration to reduce the resistance) was the material employed for the gate contacts. The main advantages were that the work function could be modulated by the doping, enabling the threshold voltage tuning of the transistors, and this material can withstand high processing temperatures in contact with SiO_2 without intermixing. The principal drawback was that, since it is a semiconductor, the charge is not confined in the poly-Si/SiO_2 interface. This space charge effect contributes typically around 0.5 nm[67] to the total EOT of the structure. When a low EOT is desired, this depletion width is unacceptable. Thus, to continue with the shrinking of the MOSFETs sizes, a metal gate electrode is required.

The benefits of using metal electrodes are several: the minimization of the depletion region, the reduction of the electrical resistance and it is not necessary to activate the gate dopants and, therefore, the thermal budget can be reduced. However, this replacement also faces several challenges, such as the modulation of the work functions and the thermal and chemical stability with the dielectric.

During some years, several metallic materials have been studied for this purpose: Al,[68,69] Pt,[70,71] TiN,[61,72] TaN,[72,73] W,[73] Ti,[74,75] etc. Among them, in this work, only three of them were studied: Al, Pt and Ti. In the following chapters, the reason of using these metals will be commented.

4.1.- <u>Scavenging effect</u>

In 2004, Kim *et al.*[74] explored the scavenging effect for the first time as a method to reduce the interfacial SiO_x layer that regrowths at the interface between the high κ material and the silicon. This IL scavenging is the chemical decomposition of the SiO_x induced by a reactive layer that can dissolve large amount of oxygen, such as Ti, deposited on top of the high κ dielectric. Silicon atoms are incorporated to the

semiconductor[74,76] while the oxygen atoms, to the Ti overlayer.[77] The high κ material would have a high permeability for O_2 in order to allow the diffusion through it.[74] In Figure I.5 is presented a schema of this process.

This SiO_x decomposition follows the next chemical reaction:

$$SiO_x + M \rightarrow Si + MO_x \qquad \textbf{(I.7)}$$

where M is the scavenging metal layer. This reaction will be spontaneous if the change in the Gibbs energy (ΔG) is negative. If the Gibbs energy of formation of MO_x is lower than the SiO_x one then, the more likely is the reduction of this SiO_x by the oxidation of M to form MO_x.[78-80] This way, the IL is scavenged. The decrease of the SiO_x thickness, which is a low κ material, reduces the total EOT of the structure, according equation (I.6), which enables obtaining a minimal EOT. Because of this, scavenging represents another approach to continue with MOSFETs downscaling.[26]

Nevertheless, this EOT reduction is typically accompanied by an interface degradation, with an intense negative impact in device performance and reliability due to a generation of defects produced by the interfacial dangling bonds.[81] Therefore, this implies that for device integration, Ti electrode should be removed after EOT optimization and the structure should be annealed afterwards to passivate defects, in a gate-last approach.[82]

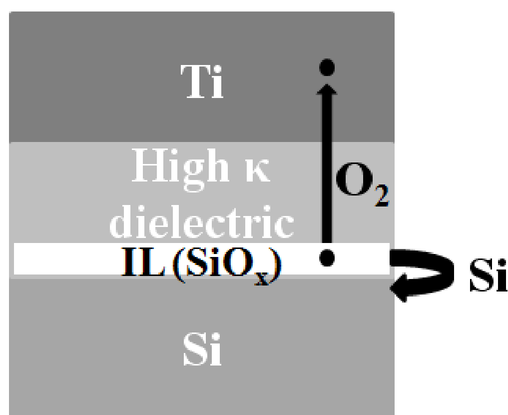

Figure I.5: Schema of the scavenging process: the oxygen of the IL diffused through the high κ material and is dissolved by Ti, while the Si atoms are reincorporated to the substrate.

I.5.- ALTERNATIVE SUBSTRATES

Silicon is the most important semiconductor material for the microelectronic industry. It is an abundant material (the second in the Earth's crust after oxygen) and its manufacturing processes are highly developed and are well known. For these reasons, its fabrication costs are reduced and it has been the microelectronic workhorse for the last decades. The main drawback of this material is that the carrier mobility for both electrons and holes is lower compared to other semiconductors.

As it was commented before, Si is reaching its scaling limits. Thus, in order to continue with transistor scaling, high mobility channels should be integrated with high κ dielectrics.[83] As it was stated in equation (I.2), a higher mobility would increase the drain current. For p-MOSFETs the main channel candidate is Ge,[84,85] while for n-MOSFETs, there is still a debate on the material of choice, like GaAs,[86,87] $In_xGa_{1-x}As$[88] or InP.[89-91] For these semiconductors the challenge is to obtain well behaved high κ/III-V semiconductor interfaces with a low D_{it} to prevent Fermi level pinning.[24,83] The principal disadvantage of these materials is that they do not possess a high quality native oxide, as in the Si case.[83,92]

InP is a potential candidate as a barrier layer in MOSFETs.[93,94] It is used in high power and high frequency applications due to its high electron mobility (~5400 cm^2/Vs) and for having a great ability to dissipate the power. For these reasons, in this thesis is also analyzed the electrical characteristics of MIS devices grown on InP.

I.6.- HIGH PRESSURE SPUTTERING (HPS)

This system was used during the thesis for the deposition of high κ materials. Sputtering is included within the physical vapor deposition (PVD) techniques. Its mechanism is to generate a plasma and to direct the ions towards the target (by the application of a voltage between the target and the substrate). The atoms from the target are ejected and transported to the substrate, where they are deposited forming a thin film.[95]

Sputtering is used for depositing metallic films in VLSI (very large-scale integration) and ULSI (ultra large-scale integration) fabrication, such as Al alloys, Ti,

Ta, Co, etc.[96,97] The typical working pressure of these systems is around 10^{-2}-10^{-3} mbar, so the mean free path of the species is in the order of some centimeters.[98] This could produce a degradation of the semiconductor surface because of the high energy of the particles that arrive to the substrate, and has prevented the use of conventional sputtering for the deposition of gate dielectrics.

HPS is a promising alternative to reduce this plasma damage, due to the high working pressure (in the mbar range, two or three orders of magnitude higher than conventional sputtering systems). This deposition technique was developed by Dr. Poppe's research group at Forschungszentrum Jülich (Germany), in origin for the growth of epitaxial high temperature superconductors based on metal oxides.[99-101] The system used in this thesis was adapted by the *Thin Film and Microelectronic Group*,[102-104] where this thesis is developed. Different types of high κ materials were deposited using dielectric targets, such as TiO_2,[105,106] HfO_2,[107,108] Sc_2O_3,[109,110] Gd_2O_3[111] and also the ternary $GdScO_3$ from a stoichiometric target or a nanolaminate of Gd_2O_3 and Sc_2O_3.[112,113] In this thesis, the deposition was carried out from metallic targets.

In HPS systems, the mean free path of the plasma ions is around 10^{-2} cm and, thus, the energetic sputtered species from the target suffer many collisions and get thermalized within a short distance, and then they move by a pure diffusion process and reach the substrate with low energy. Thus, the semiconductor surface is preserved. Besides, a compact design (therefore, a low volume vacuum chamber) can be achieved, increasing the wafer throughput. Finally, due to the high working pressure, the conformality of the films is expected to be better than conventional sputtering systems, because the deposition is less directional.

In addition, sputtering presents other advantages. For instance, since the target is made of pure material and the sputtering gas is usually inert, the film contamination can be minimal. Besides, complex material can be deposited as long as a composite target can be fabricated,[114] since the sputtering yields of most materials are in the same order of magnitude. Concerning the growth rate, it is fairly constant and since the chemisorption on the surface is not needed, it is possible to deposit on many starting surfaces. Also, the target material use efficiency is much better and, thus, from an economic point of view, this can be relevant for expensive materials. Finally, the

deposition temperature can be lower than in other techniques, so, the undesirable SiO_x regrowth between the high κ dielectric and the semiconductor can be minimized.

In the next chapter, a complete description of this system will be done.

I.7.- ALTERNATIVES STRUCTURES

The continue MOSFET dimensions shrinking brings different issues which affect its performance, such as the short-channel effects.[115] To avoid these, several companies and research groups have worked in the development of a tridimensional architecture, called multigate MOSFETs or FinFETs, because of the fin shape of the channel.[116-120] The main advantage of these transistors is that they present a better electrical control over the channel, reducing the leakage current density and thus, the power consumption, while increasing the switching performance.

In 2012, *Intel* launched the *Ivy-Bridge* microprocessors based on the 22 nm tri-gate transistors.[121,122] In Figure I.6 is represented a schema of this tri-gate transistor that is in essence a MOSFET which form a conduction channel on the three sides of the vertical fin structure. These transistors can be fabricated with several fins, in order to increase the current flow between the source and the drain.

Similar transistors grown on III-V semiconductors have also been reported in different works,[123,124] allowing a way to improve CMOS devices.

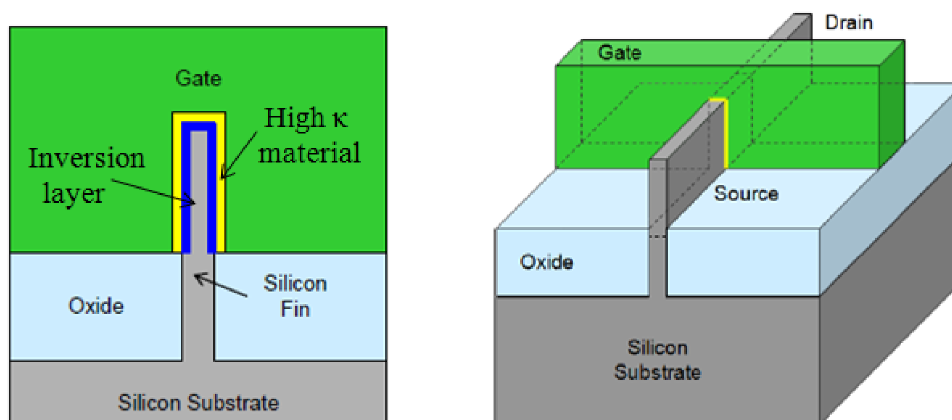

Figure I.6: Schema of a tridimensional tri-gate transistor from *Intel*.[121]

I.8.- OUTLINE OF THE THESIS

After the introduction made in the present chapter, in chapter II, the different fabrication techniques used during this thesis are briefly reviewed. The fabrication of MIS devices is the core of this thesis and, for this reason, all the techniques used for this purpose are described there. Besides, the steps followed during the different processes are listed, in addition to the substrates used and their preparation before deposition.

Chapter III presents the structural and electrical characterization techniques employed for the analysis of the high κ films and also of the interfacial layer that grows between the dielectric and the semiconductor.

In chapter IV, the thermal oxidation of metallic Gd layers to obtain Gd_2O_3 is explored. After the deposition of a thin Gd film, different oxidation temperatures are analyzed in order to obtain a good dielectric material with acceptable electrical properties.

Chapter V studies the results of the plasma oxidation of Gd_2O_3 and Sc_2O_3 films. First, a thin metallic layer is deposited and afterwards, a plasma oxidation is carried out using different conditions. A complete structural characterization is performed to these dielectric films. Besides, an analysis of the interlayer grown between the high κ materials and the Si depending on the deposition conditions is accomplished. Finally, the electrical results of Gd_2O_3 and Sc_2O_3 MOS capacitors are presented in this chapter.

Chapter VI shows the results of the $GdScO_3$ used as high κ dielectric. This material is deposited from Gd and Sc targets. A nanolaminate of these metallic layers is deposited followed by a plasma oxidation. The structural and the electrical characterizations of this film are analyzed.

In chapter VII, the scavenging effect of Ti electrodes is studied for different high κ materials and using several Ti thickness. The influence of the overlayer thickness and the annealing temperatures is analyzed in order to achieve a low EOT without degrading the dielectric films.

Chapter VIII explores the MIS devices fabricated using InP as substrate and Gd_2O_3 as dielectric. The two-step deposition process developed in the other chapters, allows to fabricate MIS capacitors without a special surface treatment.

Finally, in chapter IX, the main conclusions obtained during this thesis are summarized. Besides, the future work is also presented.

REFERENCES

[1] J. E. Lilienfeld. "*Method and apparatus for controlling electric currents*". US Patent 1745175 A (1930).

[2] J. E. Lilienfeld. "*Device for controlling electric current*". US Patent 1900018 A (1933).

[3] J. Bardeen, W. H. Brattain. "*Three-electrode circuit element utilizing semiconductive materials*". US Patent 2524035 A (1950).

[4] W. Shockley. "*The path to the conception of the junction transistor*". IEEE Trans. Electron Devices, 23, 597 (1976).

[5] M. M. Atalla. "*Semiconductor devices having dielectric coatings*". US Patent 3206670 A (1965).

[6] D. Kahng. "*Electric field controlled semiconductor device*". US Patent 3102230 A (1963).

[7] W. Jacobi. "Halbleiterverstärker". DE Patent 833366 C (1952).

[8] J. S. Kilby. "*Miniaturized electronic circuits*". US Patent 3138743 A (1964).

[9] K. Lehovec. "*Multiple semiconductor assembly*". US Patent 3029366 A (1962).

[10] R. N. Noyce. "*Semiconductor device-and-lead structure*". US Patent 2981877 A (1961).

[11] J. A. Hoerni. "*Method of manufacturing semiconductor devices*". US Patent 3025589 A (1962).

[12] G. Moore. "*Cramming more components onto integrated circuits*". Electronics, 38, 114 (1965).

[13] G. Moore. "*Progress in digital integrated electronics*". IEEE International Electron Device Meeting (IEDM), 21, 11 (1975).

[14] F. M. Wanlass. "*Low stand-by power complementary field effect circuitry*". US Patent 3356858 A (1967).

[15] G. D. Wilk, R. M. Wallace, J. M. Anthony. "*High-κ gate dielectrics: Current status and materials properties considerations*". J. Appl. Phys., 89, 5243 (2001).

[16] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, L. O. Shih-Hsien, G. A. Sai-Halasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind, H. S. Wong. "*CMOS scaling into the nanometer regime*". Proc. IEEE, 85, 486 (1997).

[17] C. A. Richter, A. R. Hefner, E. M. Vogel. "*A comparison of quantum-mechanical capacitance-voltage simulators*". IEEE Electron Dev. Lett., 22, 35 (2001).

[18] J. R. Hauser, K. Ahmed. "*Characterization of ultra-thin oxides using electrical C-V and I-V* measurements". AIP Conf. Proc. 449, 235 (1998).

[19] International Technology Roadmap for Semiconductors (ITRS): <www.itrs.net>.

[20] J. Robertson, "*High dielectric constant gate oxides for metal oxide Si transistors*". Rep. Prog. Phys., 69, 327 (2006).

[21] M. Houssa, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gent, G. Groeseneken, M. M. Heyns. "*Electrical properties of high-κ gate dielectrics: challenges, current issues, and possible solutions*". Mater. Sci. Eng. R, 51, 37 (2006).

[22] H. Wong, H. Iwai. "*On the scaling of subnanometer EOT gate dielectrics for ultimate nano CMOS technology*". Microelectron. Eng., 138, 57 (2015).

[23] H. Wong, H. Iwai. "*On the scaling issues and high-κ replacement of ultrathin gate dielectrics for nanoscale MOS transistors*". Microelectron. Eng., 83, 1867 (2006).

[24] G. He, L. Zhu, Z. Sun. Q. Wan, L. Zhang. "*Integrations and challenges of novel high-k gate stacks in advanced CMOS technology*". Prog. Mater. Sci., 56, 475 (2011).

[25] D. J. Frank, Y. Taur, H. S. P. Wong. "*Generalized scale length for two-dimensional effects in MOSFETs*". IEEE Electron Dev. Lett., 19, 385 (1998).

[26] T. Ando. "*Ultimate scaling of high-κ gate dielectrics: higher-κ of interfacial layer scavenging?*". Materials, 5, 478 (2012).

[27] C. Auth, M. Buehler, A. Cappellani, C. H. Choi, G. Ding, W. Han, S. Joshi, B. McIntyre, M. Prince, P. Ranade, J. Sandford, C. Thomas. "*45 nm high-k + metal gate strain-enhanced transistors*". Intel Technology Journal, 12, 77 (2008).

[28] E. P. Gusev, V. Narayanan, M. M. Frank. "*Advanced high-κ dielectric stacks with polySi and metal gates: Recent progress and current challenges*". IBM J. Res. & Dev., 50, 387 (2006).

[29] G. He, L. D. Zhang. "*Current progress of Hf (Zr)-based high-k gate dielectric thin films*". J. Mater. Sci. Technol., 23, 433 (2007).

[30] J. Robertson. "*Band offsets of wide-band-gap oxides and implications for future electronic devices*". J. Vac. Sci. Technol. B, 18, 1785 (2000).

[31] K. J. Hubbard, D. G. Schlom. "*Thermodynamic stability of binary oxides in contact with silicon*". J. Mater. Res., 11, 2757 (1996).

[32] D. G. Schlom, J. H. Haeni. "*A thermodynamic approach to selecting alternative gate dielectrics*". MRS Bull, 27, 198 (2002).

[33] M. H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, S. W. Nahm, D. H. Ko, J. H. Lee, N. I. Lee, K. Fujihara. "*Thermal stability and structural characteristics of HfO_2 films on Si (100) grown by atomic-layer deposition*". Appl. Phys. Lett., 81, 472 (2002).

[34] S. Hall, O. Buiu, I. Z. Mitrovic, Y. Lu, W. M. Davey. "*Review and perspective*

of high-k dielectrics on silicon". Journal of Telecommunications and Information Technology, 2, 33 (2007).

[35] J. C. G. Bünzli, C. Piguet. "*Taking advantage of luminescent lanthanide ions*". Chem. Soc. Rev., 34, 1048 (2005).

[36] M. Gasgnier. "*Rare-earth elements in permanent magnets and superconducting compounds and alloys (except new high T_c ceramics) as thin films, thin crystals and thinned bulk materials*". J. Mater. Sci., 26, 1989 (1991).

[37] J. Pu, S. J. Kim, Y. S. Kim, B. J. Choc. "*Evaluation of gadolinium oxide as a blocking layer of charge-trap flash memory cell*". Electrochem. Solid St., 11, H252 (2008).

[38] J. C. Wang, C. T. Lin, P. C. Chou, C. S. Lai. "*Gadolinium-based metal oxide for nonvolatile memory applications*". Microelectron. Reliab., 52, 635 (2012).

[39] T. M. Pan, C. S. Liao, H. H. Hsu, C. L. Chen, J. D. Lee, K. T. Wang, J. C. Wang. "*Excellent frequency dispersion of thin gadolinium oxide high-k gate dielectrics*". Appl. Phys. Lett., 87, 262908 (2005).

[40] M. Czernohorsky, E. Bugiel, H. J. Osten, A. Fissel, O. Kirfel. "*Impact of oxygen supply during growth on the electrical properties of crystalline Gd2O3 thin films on Si(001)*". Appl. Phys. Lett., 88, 152905 (2006).

[41] K. Xu, R. Ranjith, A. Laha, H. Parala, A. P. Milanov, R. A. Fischer, E. Bugiel, J. Feydt, S. Irsen, T. Toader, C. Bock, D. Rogalla, H. J. Osten, U. Kunze, A. Devi. "*Atomic layer deposition of Gd_2O_3 and Dy_2O_3: a study of the ALD characteristics and structural and electrical properties*". Chem. Mater., 24, 651 (2012).

[42] P. Shekhter, A. R. Chaudhuri, A. Laha, S. Yehezkel, A. Shriki, H. J. Osten, M. Eizenberg. "*The influence of carbon doping on the performance of Gd_2O_3 as high-k gate dielectric*". Appl. Phys. Lett., 105, 262901 (2014).

[43] J. A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang, C. Adelmann, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V. V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervost, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M. Jurczak, J. Van Houdt, D. J. Wouters. "*High-k dielectrics for future generation memory devices*". Microelectron. Eng., 86¸ 1789 (2009).

[44] J. Kwo, M. Hong, A. R. Kortan, K. L. Queeney, Y. J. Chabal, R. L. Opila Jr., D. A. Muller, S. N. G. Chu, B. J. Sapjeta, T. S. Lay, J. P. Mannaerts, T. Boone, H. W. Krautter, J. J. Krajewski, A. M. Sergnt, J. M. Rosamilia. "*Properties of high k gate dielectrics Gd_2O_3 and Y_2O_3 for Si*". J. Appl. Phys., 89, 3929 (2001).

[45] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, A. M. Sergent. "*Epitaxial cubic gadolinium oxide as a dielectric for gallium arsenide passivation*". Science, 283, 1897 (1999).

[46] J. Kwo, D. W. Murphy, M. Hong, J. P. Mannaerts, R. L. Opila, R. L. Masaitis, A. M. Sergent. "*Passivation of GaAs using gallium-gadolinium oxides*". J. Vac. Sci. Technol. B, 17, 1294 (1999).

[47] M. Hong, J. Kwo, S. N. G. Chu, J. P. Mannaerts, A. R. Kortan, H. M. Ng, A. Y. Cho, K. A. Anselm, C. M. Lee, J. I Chyi. "*Single-crystal GaN/Gd_2O_3/GaN heterostructure*". J. Vac. Sci. Technol. B, 20, 1274 (2002).

[48] W. H. Chang, C. H. Lee, P. Chang, Y. C. Chang, Y. J. Lee, J. Kwo, C. C. Tsai, J. M. Hong, C. H. Hsu, M. Hong "*High κ dielectric single-crystal monoclinic Gd_2O_3 on GaN with excellent thermal, structural, and electrical properties*". J. Crystal Growth, 311, 2183 (2009).

[49] A. P. Milanov, K. Xu, A. Laha, E. Bugiel, R. Ranjith, D. Schwendt, H. J. Osten, H. Parala, R. A. Fischer, A. Devi. "*Growth of crystalline Gd_2O_3 thin films with a high-quality interface on Si(100) by low-temperature H_2O-assisted atomic layer deposition". J. Am. Chem. Soc., 132, 36 (2010).*

[50] D. O. Klenov, L. F. Edge, D. G. Schlom, S. Stemmer. "*Extended defects in epitaxial Sc_2O_3 films grown on (111) Si*". Appl. Phys. Lett., 86, 051901 (2006).

[51] R. D. Shannon. "*Dielectric polarizabilities of ions in oxides and fluorides*". J. Appl. Phys., 73, 348 (1993).

[52] P. de Rouffignac, A. P. Yousef, K. H. Kim, R. G. Gordon. "*ALD of scandium oxide from scandium Tris(N,N'-diisopropylacetamidinate) and water*". Electrochem. Solid-State Lett., 9, F45 (2006).

[53] V. V. Afanas'ev, S. Shamuilia, M. Badylevich, A. Stesmans, L. F. Edge, W. Tian, D. G. Schlom, J. M. J. Lopes, M. Roeckerath, J. Schubert. "*Electronic structure of silicon interfaces with amorphous and epitaxial insulating oxides: Sc_2O_3, Lu_2O_3, $LaLuO_3$*". Microelectron. Eng., 84, 2278 (2007).

[54] L. Nyns, J. G. Lisoni, G. Van den Bosch, S. Van Elshocht, J. Van Houdt. "*Atomic layer deposition of scandium-based oxides*". Phys. Status Solidi A, 211, 409 (2014).

[55] S. G. Lim, S. Kriventsov, T. N. Jackson, J. H. Haeni, D. G. Schlom, A. M. Balbashov, R. Uecker, P. Reiche, J. L. Freeouf, G. Lucovsky. "*Dielectric functions and optical bandgaps of high-K dielectrics for metal-oxide-semiconductor field-effect transistors by far ultraviolet spectroscopic ellipsometry*". J. Appl. Phys., 91, 4500 (2002).

[56] V. V. Afanas'ev, A. Stesmans, C. Zhao, M. Caymax, T. Heeg, J. Schubert, Y. Jia, D. G. Schlom, G. Lucovsky. "*Band alignment between (100)Si and complex rare earth/transition metal oxides*". Appl. Phys. Lett., 85, 5917 (2004).

[57] C. Zhao, T. Witters, B. Brijs, H. Bender, O. Richards, M. Caymax, T. Heeg, J. Schubert, V. V. Afanas'ev, A. Stesmans, D. G. Schlom. "*Ternary rare-earth metal oxide high-k layers on silicon oxide*". Appl. Phys. Lett., 86, 132903 (2005).

[58] J. M. J. Lopes, E. Durgun Ozben, M. Roeckerath, U. Littmark, R. Luptak, St. Lenk, M. Luysberg, A. Besmehn, U. Breuer, J. Schubert, S. Mantl. "*Amorphous ternary rare-earth gate oxides for future integration in MOSFETs*". Microelectron. Eng., 86, 1646 (2009).

[59] C. Derks, K. Kuepper, M. Raekers, A. V. Postnikov, R. Uecker, W. L. Yang, M. Neumann. "*Band-gap variation in $RScO_3$ (R = Pr, Nd, Sm, Eu, Gd, Tb, and Dy): X-ray absorption and O K-edge X-ray emission spectroscopies*" Physical Rev. B, 86, 155124 (2012).

[60] M. Roeckerath, J. M. J. Lopes, E. Durgun Ozben, C. Sandow, S. Lenk, T. Heeg, J. Schubert, S. Mantl. "*Gadolinium scandate as an alternative gate dielectric in field effect transistors on conventional and strained silicon*". Appl. Phys. A, 94, 521 (2009).

[61] J G. Lisoni, L. Breuil, L. Nyns, P. Blomme, G. Van den Bosch, J. Van Houdt. "*High-k gadolinium and aluminum scandates for hybrid floating gate NAND flash*". Microelectron. Eng., 109, 220 (2013).

[62] A. Schäfer, K. Rahmanizadeh, G. Bihlmayer, M. Luysberg, F. Wendt, A. Besmehng, A. Fox, M. Schnee, G. Niu, T. Schroeder, S. Mantl, H. Hardtdegen, M. Mikulics, J. Schubert. "*Polymorphous $GdScO_3$ as high permittivity dielectric*". J. Alloys Compd., 651, 514 (2015).

[63] M. Wagner, T. Heeg, J. Schubert, St. Lenk, S. Mantl, C. Zhao, M. Caymax, S. De Gent. "*Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation*". Appl. Phys. Lett., 88, 172901 (2006).

[64] K. Fröhlich, J. Fedor, I. Kostic, J. Manka, P. Ballo. "*Gadolinium scandate: next candidate for alternative gate dielectric in CMOS technology?*". J. of Elect. Eng., 62, 54 (2011).

[65] R. A. Minamisawa, M. Schmidt, E. Durgun Özben, J. M. J. Lopes, J. M. Hartmann, K. K. Bourdelle, J. Schubert, Q. T. Zhao, D. Buca, S. Mantl. "High mobility strained $Si_{0.5}Ge_{0.5}$/SSOI short channel field effect transistors with TiN/$GdScO_3$ gate stack". Microelectron. Eng., 88, 2955 (2011).

[66] K. Cico, K. Huseková, M. Tapajna, D. Gregusová, R. Stoklas, J. Kuzmík, J. F. Carlin, N. Grandjean, D. Pogany, K. Fröhlich. "*Electrical properties of InAlN/GaN high electron mobility transistor with Al_2O_3, ZrO_2, and $GdScO_3$ gate dielectrics*". J. Vac. Sci. Technol. B, 29, 01A808 (2011).

[67] E. Josse, T. Skotnicki. "*Polysilicon gate with depletion- or metallic-gate with buried channel: what evil worse?*". IEEE International Electron Device Meeting (IEDM), 661 (1999).

[68] B. Yao, Z. B. Fang, Y. Y. Zhu, T. Ji, G. He. "*A model for the frequency dispersion of the high-k metal-oxide-semiconductor capacitance in accumulation*". Appl. Phys. Lett., 100, 222903 (2012).

[69] S. Kaya. E. Yilmaz. "*A comprehensive study of the frequency-dependent electrical characteristics of Sm2O3 MOS capacitors*". IEEE Trans. Electron Devices, 62, 980 (2015).

[70] K. Xu, R. Ranjith, A. Laha, H. Parala, A. P. Milanov, R. A. Fischer, E. Bugiel, J. Feydt, S. Irsen, T. Toader, C. Bock, D. Rogalla, H. J. Osten, U. Kunze, A. Devi. "*Atomic layer deposition of Gd_2O_3 and Dy_2O_3: a study of the ALD characteristics and structural and electrical properties*". Chem. Mater., 24, 651 (2012).

[71] L. Nyns, J. G. Lisoni, G. Van den Bosch, S. Van Elshocht, J. Van Houdt. "*Atomic layer deposition of scandium-based oxides*". Phys. Status Solidi A, 211, 409 (2014).

[72] L. Å. Ragnarsson, T. Chiarella, M. Togo, T. Schram, P. Absil, T. Hoffmann. "*Ultrathin EOT high-j/metal gate devices for future technologies: Challenges, achievements and perspectives (invited)*". Microelectron. Eng., 88, 1317 (2011).

[73] V. Narayanan, K. Maitra, B. P. Linder, V. K. Paruchuri, E. P. Gusev, P. Jamison, M. M. Frank, M. L. Steen, D. La Tulipe, J. Arnold, R. Carruthers, D. L. Lacey, E. Cartier. "*Process optimization for high electron mobility in nMOSFETs with aggressively scaled HfO_2/metal stacks*". IEEE Electron Devices Lett., 27, 591 (2006).

[74] H. Kim, P. C. McIntryre, C. O. Chui, K. C. Saraswat, S. Stemmer. "*Engineering chemically abrupt high-k metal oxide/silicon interfaces using an oxygen-gettering metal overlayer*". J. Appl. Phys., 96, 3467 (2004).

[75] C. Choi, J. C. Lee. "*Scaling equivalent oxide thickness with flat band voltage (V_{FB}) modulation using in situ Ti and Hf interposed in a metal/high-k gate stack*". J. Appl. Phys., 108, 064107 (2010).

[76] K. I. Seo, D. I. Lee, P. Pianetta, H. Kim, K. C. Saraswat, P. C. McIntyre. "*Chemical states and electrical properties of a high-k metal oxide/silicon interface with oxygen-gettering titanium-metal-overlayer*". Appl. Phys. Lett. 89, 142912 (2006).

[77] K. Nakajima, A. Fujiyoshi, Z. Ming, M. Suzuki, K. Kimura. "*In situ observation of oxygen gettering by titanium overlayer on $HfO_2/SiO_2/Si$ using high-resolution Rutherford backscattering spectroscopy*". J. Appl. Phys., 102, 064507 (2007).

[78] T. Ando, M. M. Frank, K. Choi. C. Choi, J. Bruley, M. Hopstaken, R. Haignt, M. Copel, H. Arimura, H. Watanabe, V. Narayanan. "*Ultimate EOT scaling (< 5 Å) using Hf-based high-κ gate dielectrics and impact on carrier mobility*". ECS Trans., 28, 115 (2010).

[79] T. Ando, C. Choi, M. M. Frank, V. Narayanan. "*Scavenging metal stack for a high-k gate dielectric*". US Patent 7989902 B2 (2011).

[80] A. Nichau, A. Schäfer, L. Knoll, S. Wirths, T. Schram, L. Å. Ragnarsson, J. Schubert, P. Bernardy, M. Luysberg, A. Besmehn, U. Breuer, D. Buca, S. Mantl. "*Reduction of silicon dioxide interfacial layer to 4.6 Å EOT by Al remote scavenging in high-κ/metal gate stacks on Si*". Microelectron. Eng., 109, 109 (2013).

[81] F. Cerbu, A. P. D. Nguyen, J. Kepa, V. V. Afanas'ev, A. Stesmans. "*Generation of Si dangling bond defects at Si/insultator interfaces induced by oxygen scavenging*". Phys. Status Solidi B, 251, 2193 (2014).

[82] T. Y. Hoffman. "*Integrating high-k/metal gates: gate-first or gate-last?*" Solid State Technology, 53, 20 (2010).

[83] J. A. del Alamo. "*Nanometre-scale electronics with III-V compound semiconductors*". Nature, 479, 317 (2011).

[84] C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi. "*Record-high electron mobility in Ge n-MOSFETs exceeding Si universality*". IEEE International Electron Device Meeting (IEDM), 457 (2009).

[85] R. Xie, T. H. Phung, W. He, M. Yu, C. Zhu. "*Interface-engineered high-mobility high-k/Ge pMOSFETs with 1-nm equivalent oxide thickness*". IEEE Trans. Electron Devices, 56, 1330 (2009).

[86] Y. C. Byun, C. H. An, J. Y. Choi, C. Y. Kim, M. H. Cho, H. Kim. "*Interfacial self-cleaning during PEALD HfO_2 process on GaAs using $TDMAH/O_2$ with different $(NH_4)_2S$ cleaning time*". J. Electrochem. Soc., 158, G141 (2011).

[87] T. Das, C. Mahata, C. K. Maiti, G. K. Dalapati, C. K. Chia, D. Z. Chi, S. Y. Chiam, H. L. Seng, C. C. Tan, H. K. Hui, G. Sutradhar, P. K. Bose. "*Sputter-deposited La_2O_3 on p-GaAs for gate dielectric applications*". J. Electrochem. Soc., 159, G15 (2012).

[88] Y. C. Lin, M. L. Huang, C. Y. Chen, M. K. Chen, H. T. Lin, P. Y. Tsai, C. H. Lin, H. C. Chang, T. L. Lee, C. C. Lo, S. M. Jang, C. H. Diaz, H. Y. Hwang, Y. C. Sun, E. Y. Chang. "*Low interface trap density Al2O3/In0.53Ga0.47As MOS capacitor fabricated on MOCVD-grown InGaAs epitaxial layer on Si substrate*". Appl. Phys. Express, 7, 041202 (2014).

[89] Y. Q. Wu, Y. Xuan, T. Shen, P. D. Ye, Z. Cheng, A. Lochtefeld. "*Enhancement-mode InP n-channel metal-oxide-semiconductor field effect transistors with atomic-layer-deposited Al_2O_3 dielectrics*". Appl. Phys. Lett., 91, 022108 (2007).

[90] H. S. Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. C. Lee, P. Majhi. "*HfO_2-based InP n-channel metal-oxide-semiconductor field-effect transistors and metal-oxide-semiconductor capacitors using a germanium interfacial passivation layer*". Appl. Phys. Lett., 93, 102906 (2008).

[91] H. Dong, W. Cabrera, X. Qin, B. Brennan, D. Zhernokletov, C. L. Hinkle, J. Kim, Y. J. Chabal, R. M. Wallace. "*Silicon interfacial passivation layer chemistry for high-k/InP interfaces*". ACS Appl. Mater. Interfaces, 6, 7340 (2014).

[92] R. Engel-Herbert, Y. Hwang, S. Stemmer. "*Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces*". J. Appl. Phys., 108, 124101 (2010).

[93] M. Radosavljevic, G. Dewey, J. M. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, R. Chau. "*Non-planar, multi-gate InGaAs quantum well field effect transistors with high-K gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications*". IEEE Int. Electron Devices Meet. (IEDM), 126 (2010).

[94] J. Lin, T. W. Kim, D. A. Antoniadis, J. A. Del Alamo. "*A self-aligned InGaAs quantum-well metal-oxide-semiconductor field-effect transistors fabricated through a liftoff-free front-end process*". Appl. Phys. Express, 5, 064002 (2012).

[95] S. Kar. "High permittivity gate dielectric materials". Springer. Heidelberg, 2013.

[96] S. M. Rossnagel, J. J. Cuomo, W. D. Westwood. "Handbook of plasma processing technology: Fundamentals, etching, deposition, and surface interactions". Noyes Publications. Mill Road, Park Ridge, New Jersey, 1990.

[97] S. Wolf. "Microchip manufacturing". Lattice Press. Sunset Beach, California, 2004.

[98] W. Umrath. "Fundamentals of vacuum technology". Leybold. Cologne, 1998.

[99] U. Poppe, J. Schubert, R. R. Arons, W. Evers, C. H. Freiburg, W. Reichert, K. Schmidt, W. Sybertz, K. Urban. "*Direct production of crystalline superconducting thin films of $YBa_2Cu_3O_7$ by high-pressure oxygen sputtering*". Solid State Comm., 66, 661 (1988).

[100] U. Poppe, P. Prieto, J. Schubert, H. Soltner, K. Urban. "*Epitaxial multilayers of $YBa_2Cu_3O_7$ and $PrBa_2Cu_3O_7$ as a possible basis for superconducting electronic devices*". Solid State Comm., 71, 569 (1989).

[101] U. Poppe, N. Klein, U. Dähne, H. Soltner, C. L. Jia, B. Kabius, K. Urban, A. Lubig, K. Schmidt, S. Hensen, S. Orbach, G. Müller, H. Piel. "*Low-resistivity epitaxial $YBa_2Cu_3O_7$ thin films with improved microstructure and reduced microwave losses*". J. Appl. Phys., 71, 5572 (1992).

[102] E. San Andrés Serrano. "*Fabricación y caracterización de dieléctricos de alta permitividad para su aplicación como aislantes de puerta en dispositivos MIS*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2004).

[103] M. Toledano-Luque. "*Growth and characterization of high-k dielectrics for field effect devices*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2008).

[104] P. C. Feijoo Guerro. "*High permittivity dielectrics for next generatios of integrated circuits*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2013).

[105] E. San Andrés, M. Toledano-Luque, A. del Prado, M. A. Navacerrada, I. Mártil, G. González-Díaz, W. Bohne, J. Röhrich. "*Physical properties of high pressure reactively sputtered TiO_2*". J. Vac. Sci. Technol. A, 23, 1253 (2005).

[106] S. Dueñas, H. Castán, H. García, E. San Andrés, M. Toledano-Luque, I. Mártil, G. González-Díaz, K. Kukli, T. Uustare, J. Aarik. "*A comparative study of the electrical properties of TiO_2 films grown by high-pressure reactive sputtering and atomic layer deposition*". Semicond. Sci. Technol., 20, 1044 (2005).

[107] M. Toledano-Luque, M. L. Lucía, A. del Prado, E. San Andrés, I. Mártil, G. González-Díaz. "*Optical spectroscopic study of the SiN/HfO_2 interfacial formation during rf sputtering of HfO_2*". Appl. Phys. Lett., 91, 191502 (2007).

[108] M. Toledano-Luque, E. San Andrés, A. del Prado, I. Mártil, M. L. Lucía, G. González-Díaz, F. L. Martínez, W. Bohne, J. Röhrich, E. Strub. "*High-pressure reactively sputtered HfO_2: Composition, morphology, and optical properties*". J. Appl. Phys., 102, 044106 (2007).

[109] P. C. Feijoo, A. del Prado, M. Toledano-Luque, E. San Andrés, M. L. Lucía. "*Scandium oxide deposited by high-pressure sputtering for memory devices: Physical and interfacial properties*". J. Appl. Phys., 107, 084505 (2010).

[110] P. C. Feijoo, M. A. Pampillón, E. San Andrés, M. L. Lucía. "*Optimization of scandium oxide growth by high pressure sputtering on silicon*". Thin Solid Films, 526, 81 (2012).

[111] P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Optimization of gadolinium oxide growth deposited on Si by high pressure sputtering*". J. Vac. Sci. Technol. B, 31, 01A103 (2013).

[112] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Gadolinium scandate by high-pressure sputtering for future generations of high-κ dielectrics*". Semicond. Sci. Technol., 28, 085004 (2013).

[113] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Nano-laminate vs. direct deposition of high permittivity gadolinium scandate on silicon by high pressure sputtering*". Thin Solid Films, 593, 62 (2015).

[114] V. M. Mukhortov, Y. I. Golovko, G. N. Tolmachev, A. N. Klevtzov. "*The synthesis mechanism of complex oxide films formed in dense rf-plasma by reactive sputtering of stoichiometric targets*". Ferroelectrics, 247, 75 (2000).

[115] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, H. S. P. Wong. "*Device scaling limits of Si MOSFETs and their application dependencies*". Proc. of the IEEE, 89, 259 (2001).

[116] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, C. Hu. "*Sub 50-nm FinFET: PMOS*". IEEE International Electron Devices Meeting (IEDM), 67.(1999).

[117] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor, C. Hu. "*FinFET-a self-aligned double-gate MOSFET scalable to 20 nm*". IEEE Trans. Electron Devices, 47, 2320 (2000).

[118] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C. Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. J. King, J. Bokor, C. Hu, M. R. Lin, D. Kyser. "*FinFET scaling to 10 nm gate length*". IEEE International Electron Devices Meeting (IEDM), 251 (2002).

[119] R. S. Chau, B. S. Doyle, J. Kavalieros, D. Barlage, S. D. Scott, A. Hareland. "*Tri-gate devices and methods of fabrication*". US Patent 6858472 B2 (2005).

[120] I. Ferain, C. A. Colinge, J. P. Colinge. "*Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors*". Nature, 479, 310 (2011).

[121] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, R. Chau. "*High performance fully-depleted tri-gate CMOS transistors*". IEEE Electron Device Lett., 24, 263 (2003).

[122] M. Bohr, K. Mistry. "*Intel's revolutionary 22 nm transistor technology*". Intel (2011).

[123] Y. Q. Wu, M. Xu, R. S. Wang, O. Koybasi, P. D. Ye. "*High performance deep-submicron inversion-mode InGaAsMOSFETs with maximum G_m exceeding 1.1 mS/μm: new HBr pretreatment and channel engineering*". IEEE Internation Electron Devices Meeting (IEDM), 323 (2009).

[124] M. Radosavljevic, G. Dewey, J. M. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, R. Chau. "*Non-planar, multi-gate InGaAs quantum well field-effect transistors with high-κ gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications*". IEEE International Electron Devices Meeting (IEDM), 126 (2010).

Chapter II:
Fabrication techniques

The microelectronic industry uses several fabrication methods in order to deposit layers of dielectric and metallic materials. Besides, lithography processes and temperature treatments are needed to define the active areas and improve the electrical characteristics of the devices.

In this chapter, the different fabrication techniques used during this thesis are described. The core of this thesis was the fabrication of metal-insulator-semiconductor (MIS) capacitors using high κ dielectrics in order to perform structural and electrical characterizations of these materials.

The technique used for the deposition of thin films of high κ materials was high pressure sputtering (HPS). This system was widely studied and here it is described in depth. Glow discharge optical spectroscopy (GDOS) was employed as a tool to study the species presented in the plasma during the deposition.

The metallic electrodes were grown by means of the electron beam (e-beam) evaporation system. This technique was also used for the growth of a thick SiO_x layer that acts as field oxide (FOX).

In order to define the top metal electrodes, two different lithography processes were used, depending on the particular conditions of each MIS device fabrication.

The temperature treatments were carried out in a rapid thermal annealing system (RTA) using a forming gas atmosphere.

Two types of semiconductors (Si and InP) were used to fabricate MIS devices. The characteristics of these substrates and the cleaning procedures are also described at the end of this chapter.

II.1.- HIGH PRESSURE SPUTTERING (HPS)

During this thesis, the system used for the deposition of high κ materials was HPS. As it was commented in the former chapter, this system works with a pressure in the mbar range, which is two or three orders of magnitude higher than conventional sputtering systems. The main advantage is that this high working pressure avoids the degradation of the semiconductor surface because the particles suffer many collisions and get thermalized before reaching the substrate.

The HPS system used in this thesis, and shown in Figure II.1, was initially purchased from Forschungszentrum Jülich (Germany), where it was designed for the deposition of superconducting films[1] and was adapted by the *Thin Film and Microelectronic Group*[2-4] for the deposition of several high κ materials from oxide targets.[5-9]

In Figure II.2, a scheme of the HPS system is presented. The targets used during this thesis are metallic Gd and Sc, with the maximum purity available of 99.9%, purchased from *Kurt J. Lesker*. The diameter of both targets is 2 inches (~5 cm) and the thickness is 1/8 inch (~0.3 cm). Both materials are glued to the cathode of the system with a *Varian* Torr-seal low vapor-pressure epoxy resin. The targets are fixed to a

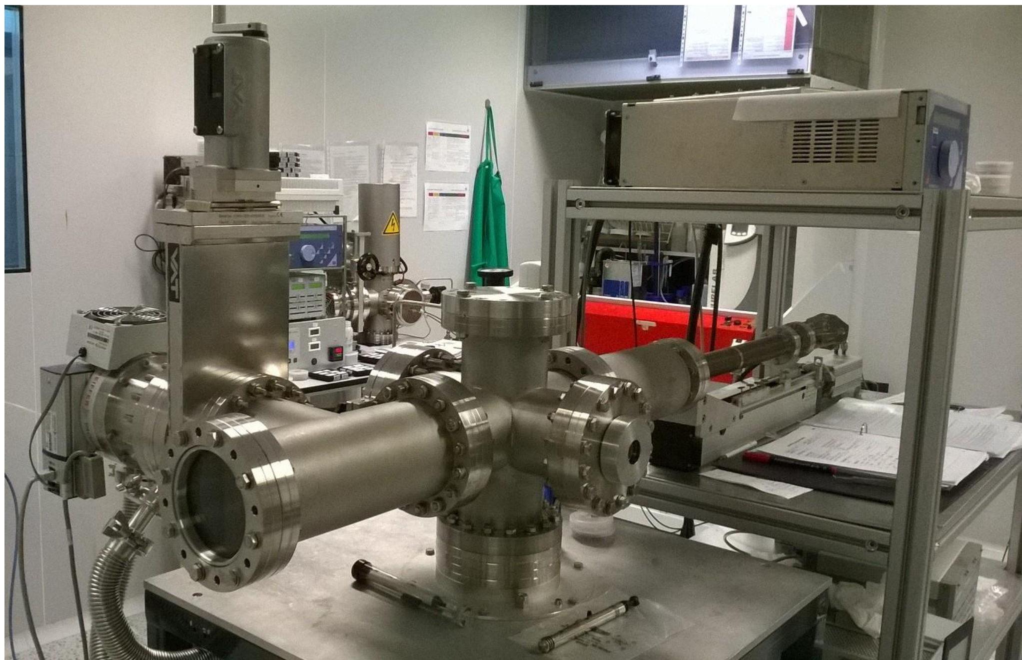

Figure II.1: Picture of the high pressure sputtering used for high κ materials deposition.

mechanical arm that can hold up to three different targets and its movement in one axis is controlled and can be automated using a motorized system from *Isel Automation*. This allows sputtering the target surface away from the substrate (thus, “conditioning” the target), preventing deposition during this process without needing shutters that can become contaminated over time. The mechanized arm also permits nanolaminates deposition[10] and an excellent control of layer thickness by controlling deposition time. To avoid the degradation of the glue, due to the heating of the targets, the system is refrigerated by a water circuit.

The plasma is generated with a radiofrequency (*rf*) source model *PFG 300* from *Hüttinger* at a standard frequency of 13.56 MHz. The connection to the system is made through an impedance matchbox. This matchbox adapts the plasma impedance to the source impedance and it is placed close to the cathode to prevent *rf* losses. It consists in several capacitances in parallel with inductors. Two of the capacitors can be adjusted manually for obtaining the minimum reflected power. The reason of using *rf* and not DC power is because the system is prepared to deposit insulators.2-4 The use of the *rf* signal is mandatory in those materials in order to avoid a charge accumulation on the surface of the target that would switch off the plasma.[11-13] In this work, the targets used

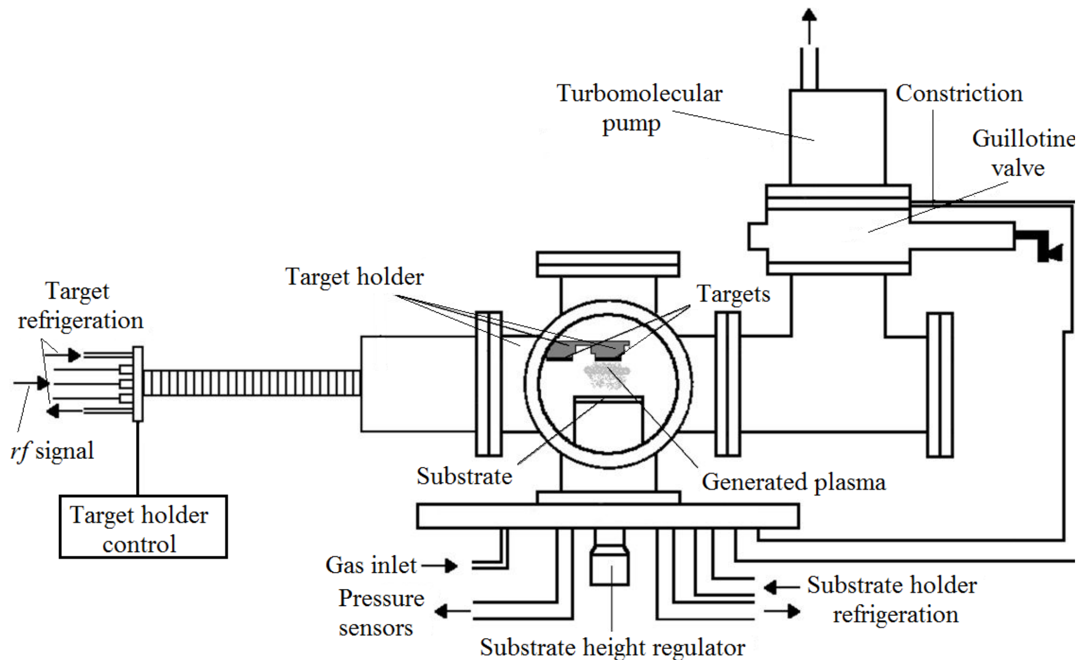

Figure II.2: Scheme of the high pressure sputtering used.

are metallic, so the *rf* signal should not be necessary. But, if the metallic surface of the target would be oxidized (even locally) this could produce high voltage discharges, producing plasma instabilities and possibly damaging the devices. Also, the epoxy used to glue the targets to the cathode is insulating and it would be necessary to use a conducting one. Therefore, in order to keep the know-how of the system operation, achieved in previous works, we decided to stick to the same *rf* system and epoxy glue.

The chamber, that reaches a base pressure in the order of 1.0×10^{-6} mbar, is connected to a *Pfeiffer TMU 261* turbomolecular pump supported with a roughing system. During the first part of this thesis, the support pump was a compact model *Drytel 31* from *Alcatel*, which was replaced afterwards by a modern *Hi Cube* model from *Pfeiffer Vacuum*. Both systems have the same structure: a small turbomolecular pump and a membrane pump. After pump substitution, there were no differences in the system behavior. Between the vacuum system and the chamber, there is a guillotine valve that allows regulating the effective pumping speed. This valve is fully opened when there is no deposition, to achieve the base pressure. However, keeping the valve opened during sputtering would imply excessive gas flow (that would heat the turbomolecular pump to the point of self-stopping to avoid permanent damage). Thus, when the deposition is taking place the position of the guillotine valve is manually regulated, controlling the chamber pressure with a fixed gas flow.

Three different pressure sensors are used to measure the pressure of the chamber. For pressures close to the atmospheric pressure (between 10^{3} to 10 mbar) a *Leybold-Heraeus Kat. Nr. 160 40* sensor is used. For the range between 10^{3} and 10^{-3} mbar, a thermal conductivity based sensor with a constant resistance is utilized. For the medium-high vacuum range (10^{-3}-10^{-9} mbar), a *Balzers IKR 250* cold cathode gauge sensor is used. This way, all the pressure range can be covered, from atmospheric pressure to high-vacuum.

The system allows us working up to three different gases. In this thesis only two of them have been used: Ar and O_2 from *Praxair* with a purity of 99.999%. These gases are introduced using a mass flow controlled (MFC) from *Bronkhorst*. Also, an additional line for dry Ar is available to fill the chamber before breaking its vacuum.

To load and unload the samples into the chamber, it is necessary to open it to the clean room atmosphere. This could produce a contamination of the targets and the chamber. To reduce this contamination, a constant flow of Ar is maintained while the chamber is open, and also the target is conditioned for at least 60 min away of the substrate before the actual deposition processes.

The substrates are placed on a substrate holder that can hold wafers up to 2 inches in diameter. The target to substrate distance is controlled by a micrometric screw. This height has been kept fixed during this thesis, so the distance between the target and the substrate is 2.5 cm. This is much higher than the mean free path of the plasma species (around 5×10^{-2} cm for Sc and Gd or 3×10^{-1} cm for Ar, according some calculations made using references)[14,15] in order to prevent surface damage of the semiconductor. The heater can reach temperatures up to 975 ºC and is controlled by a *Eurotherm 810* automat, which permits programming complex temperature profiles. The temperature is measured with a thermocouple.

The HPS system used for the high κ dielectric deposition is placed inside the clean room of the *Departamento de Física Aplicada III: Electricidad y Electrónica* from *Universidad Complutense de Madrid*.

II.2.- GLOW DISCHARGE OPTICAL SPECTROSCOPY (GDOS)

This technique was used to analyze the emissions of the *rf* plasma in order to choose the optimal working conditions. Using this spectroscopy system, the presence of atoms and molecules of different materials can be identified by observing the wavelengths of the emitted light.

A plasma is a gas containing an equal number of positive and negative particles (such as electrons and ions), usually together with neutral gas-atoms.[12] The neutral density is much higher than the charged density. On average, the plasma is electrically neutral. In the electronic industry, the most common plasma is the glow discharge. This is a weakly ionized plasma that is self-sustaining and emits light. This emitted light is due to the excitation or recombination processes of the electrons of the plasma, atoms, ions or molecules. Since these transitions are between well defined energy levels, depending on the transition and the species, the photon has a particular energy (or

wavelength). Thus, by measuring the wavelengths emitted by the glow discharge, information on the species that compose the plasma can be obtained.

Two different spectroscopy systems were used during this thesis with the purpose of analyzing the light emitted by the plasma inside the HPS system. The light was collected through a sapphire window, which is transparent to the measured wavelengths. These systems are briefly described in the next subsections.

2.1.- System I (monocromator)

In the experimental setup of this first system (shown in Figure II.3), a monocromator (model *Jobin Yvon H-25*) is used. This system was used to measure the wavelengths ranging between 280.0 and 550.0 nm with a resolution of 0.1 nm. This monocromator consists in an input and output slits, a system of collimating lenses and a diffraction grating that permits the selection of a determined wavelength. The photons with that wavelength are directed to the photomultiplier. For each incident photon in the photocathode, an electron is emitted. This electron is directed by an electric field to a dynode (fabricated with a material with a high emission of secondary electrons). Thus,

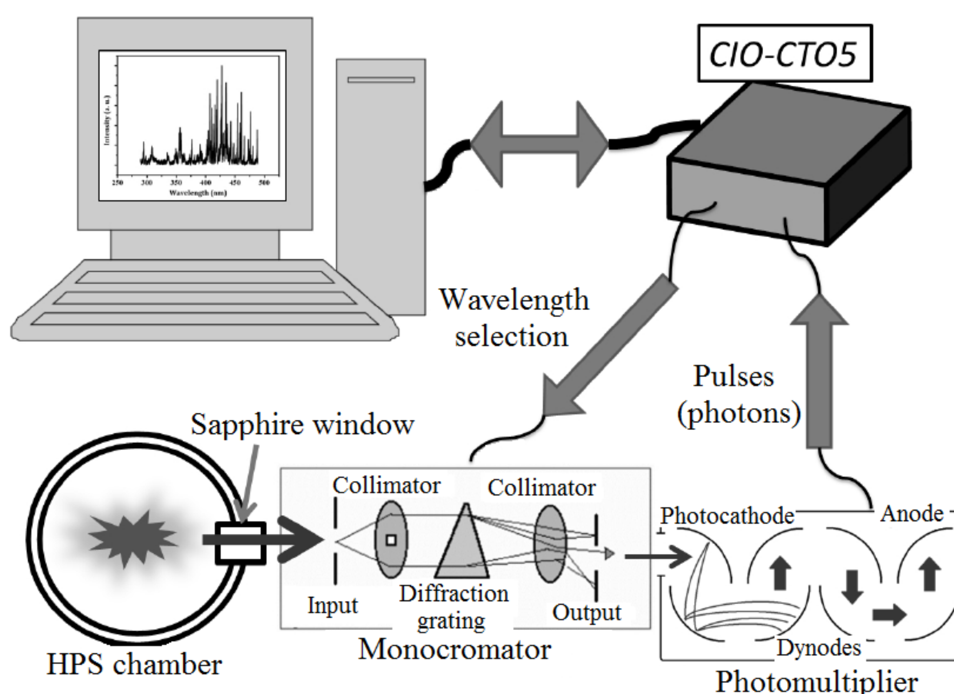

Figure II.3: Scheme of the glow discharge optical spectroscopy system I (monocromator).

for each electron, there are two electrons that are directed to another dynode. These electrons cross several dynodes and, therefore, they are multiplied. In the anode, a pulse signal is generated and, thus, each pulse corresponds to a single photon. This signal is processed by a card *CIO-CTO5* that counts the number of pulses during a determined time. Besides, it sends a signal to the stepper motor that controls the diffraction grating of the monocromator and thus, selects the wavelength. With the help of a *Labview* program designed to control the card, we can determine the wavelength sweep and the scanning results are stored. The typical measurement has a total duration of around 40 min.

2.2.- System II (spectrometer)

In this case, instead of mechanically sweeping the wavelength with a monocromator (that is a slow process), a spectrometer is used to provide an instantaneous spectral image from a highly sensitive charge coupled device (CCD) with 2048 pixels from *StellarNet*. Wavelengths ranging from 200.00 nm to 1000.00 nm can be measured with a resolution of 0.25 nm. The main advantage of this system is that the data can be acquired in ~1 s, thus, a real-time analysis of the spectra can be made.

In Figure II.4 a schematic of this system is presented. An optical fiber directs the emitted light to the CCD, which is protected inside a rugged metal enclosure, together

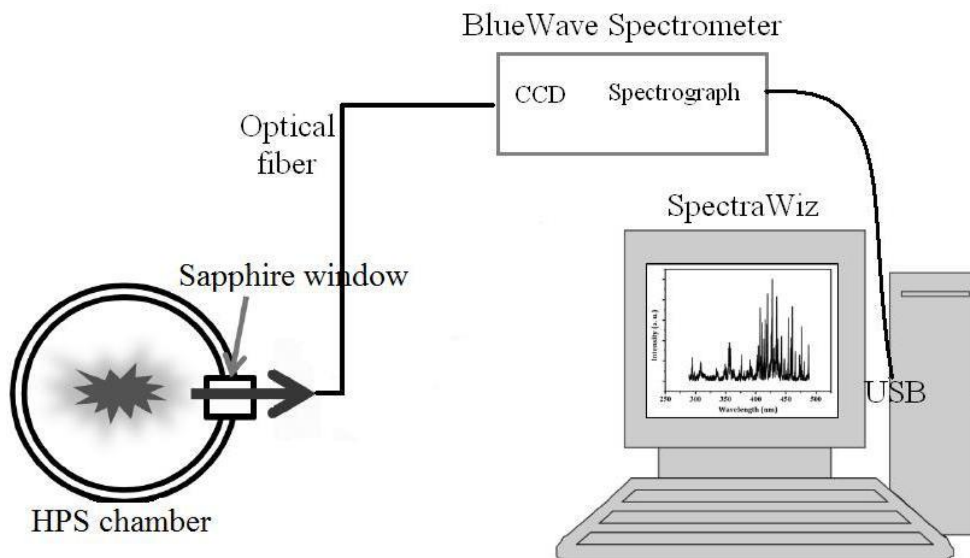

Figure II.4: Scheme of the system II (spectrometer) to analyze the GDOS.

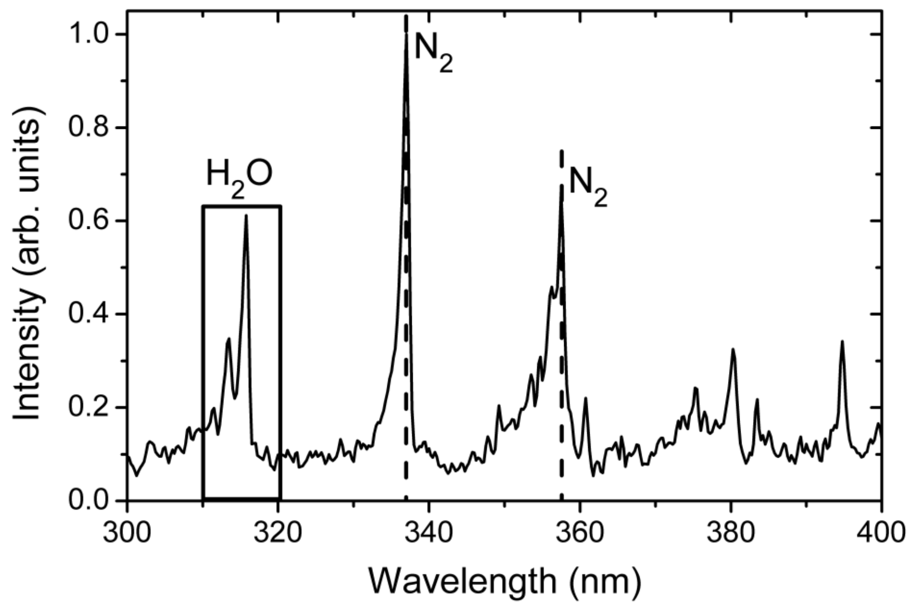

Figure II.5: GDOS emission spectrum of a target sputtered in Ar during the conditioning process. H_2O band and N_2 peaks are marked in the figure. The remaining peaks are related to Ar I and Ar II.

with the spectrograph. This box is connected to the computer via USB. Using the *SpectraWiz* program, the spectrum is obtained and the data can be saved to analyze the emission lines.

Figure II.5 represents a GDOS spectrum obtained with the spectrometer, in which the presence of H_2O (a broad band located at wavelengths ranging from 310 to 320 nm)[16] and also peaks corresponding to N_2 (the main peaks at around 336 and 358 nm)[16] can be observed. In this example, these features indicate that there is contamination in the plasma that might affect the deposited film. This way, GDOS can be used as a deposition quality check. In the following chapters, the shown spectra will not have these contamination bands. Finally, the remaining peaks present in this spectrum are related to Ar I and Ar II.[17,18]

II.3.- ELECTRON BEAM (e-beam) EVAPORATION

This system was used along this thesis for MIS fabrication with two different goals: to deposit SiO_x as field oxide and to evaporate the metallic electrodes, using Al,

Ti or Pt. This technique is another form of PVD, since no chemical reactions are involved. It consists in melting the material to evaporate by the bombardment with a high intensity electron beam. This beam is produced by a heated tungsten filament biased with a high voltage and is directed magnetically to the melt by regulating the current of deflecting coils. Once this beam melts the material, the vapor pressure produces the evaporation of this material.[19] The evaporated atoms travel in straight lines because the system works in high vacuum, until reaching a surface, where they become fixed.

Figure II.6 is a picture of the e-beam evaporation system used during this thesis, while in Figure II.7, a scheme of the system is shown. The samples are glued to the cover upside down with capton film. The chamber reached a base vacuum around 5×10^{-7} mbar due to the help of a turbomolecular pump, *Balzers TPH 330*, supported by a rotary pump, *Balzers DUO 30A*. The tungsten filament, which is protected by a shield, is biased with a high potential of ~6 kV. Regulating the current through this filament, the intensity of the e-beam can be controlled. The magnetic field created by the coils deflects the beam and directs it to the material target, which lies within a crucible. This crucible can hold up to four different materials and it is refrigerated by water in order to

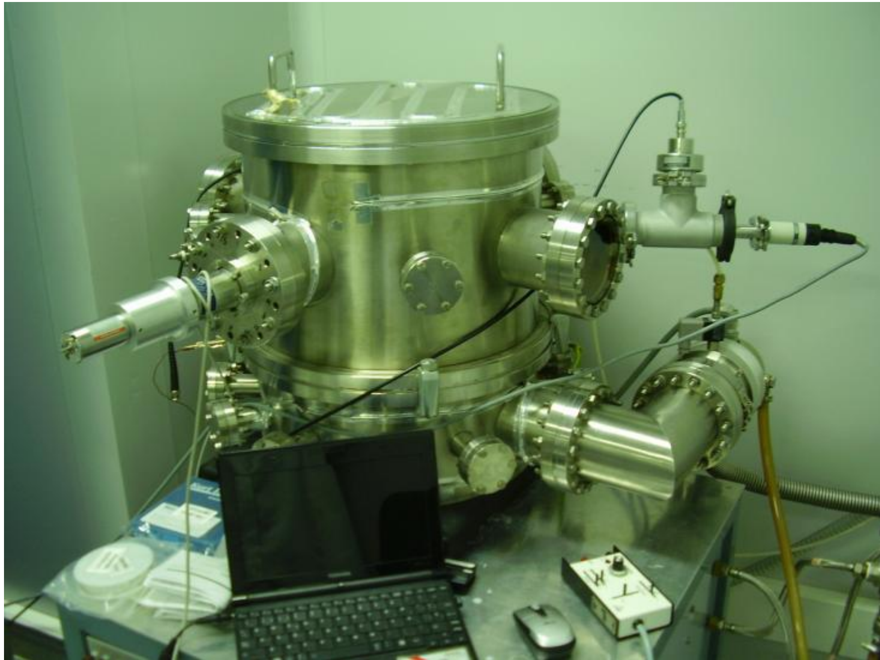

Figure II.6: Image of the e-beam evaporation system used in this thesis.

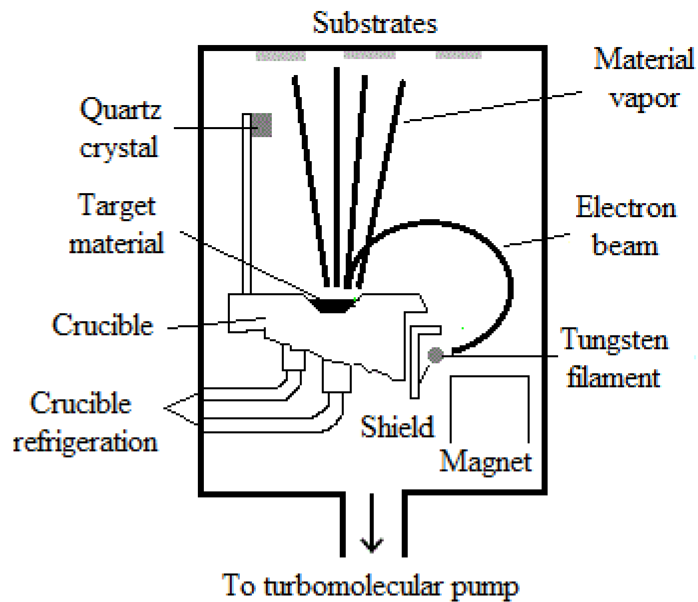

Figure II.7: Scheme of the electron beam evaporation system.

avoid damages. When the material is melted, the atoms are evaporated through the chamber and a thin film is deposited. The thickness of the evaporated layer can be controlled by means of a quartz crystal: the shift of the resonance frequency of this crystal is proportional to the thickness. The growth rate can be controlled with the beam intensity and it is obtained with a program controlled by a computer. The accuracy is 0.1 nm/s.

The distance between the samples and the material which will be evaporated is around 50 cm. The atoms must reach the surface of the wafers without neither colliding nor scattering. Therefore, the mean free path of particles must be larger than the target-substrates distance. To achieve this, a pressure in the order of 10^{-6}-10^{-7} mbar is needed during the evaporation. Thus, the pumps are switched on during this process.

Between the crucible and the samples, there is a shutter that can be opened or closed to permit or block the evaporation of the material to the substrates. This shutter avoided the contamination of the samples in the first stages of the evaporation, when the target melting is performed.

As it was mentioned, two different processes were carried out with the e-beam evaporation system and are listed below.

3.1.- SiO_x acting as field oxide

The reason of performing this process will be further analyzed later in section II.6. It consists in the evaporation on the semiconductor surface of a thick layer of SiO_x (around 200 nm), obtained from a high purity SiO_2 source (99.999%), purchased from *Test Bourne Super Vac*. The evaporation rate of this process was low to avoid adhesion problems.

3.2.- Metallic electrodes

For MIS fabrication, different metallic stacks were used. On the one hand, for the Si bottom contact, the whole backside surface of the wafers was cover with~70 nm of Al or a stack formed with 50 nm of Ti / 100 nm of Al. On the other hand, for InP substrates, the back electrode was 100 nm of AuGe and 100 nm of Au. In both cases, these metals ensure ohmic contact to n-Si and n-InP wafers, respectively.

To define the top contacts, a lithography process was performed and several electrodes were investigated: pure Al gates (with a thickness around 40-70 nm), a stack formed with a thin Pt layer (less than 10 nm in order to avoid adhesion problems due to stress), capped with Al (to ensure a thick contact with the aim of avoiding the perforation of the metal gate when probing), ~25 nm of pure Pt electrodes and different thicknesses of Ti (to explore the scavenging effect) capped with 25 nm of Pt to avoid nitridation or oxidation problems. In the next chapters, the effects of using these different top electrodes will be explained.

The e-beam evaporation system used is placed inside the clean room.

II.4.- LITHOGRAPHY PROCESS

This optical process is used to transfer a mask pattern to the surface of the samples using ultraviolet light.[20] This method was used during this thesis to define the shape and size of the metallic top electrodes. To achieve that transfer, a thin film of photoresist, which is a light sensitive material, must be homogenous deposited over the

Figure II.8: Image of the *Headway Research* spinner (in the left hand side) and the *MJB3 UV400* alignment system (in the right hand side), used for the lithography process.

surface with a spinner (from *Headway Research*). This system is showed in the left hand side of Figure II.8. After a soft bake (that removes almost all of the solvents from the photoresist coating), the mask is aligned to the previous processes, and the photoresist is exposed with high intensity ultraviolet light (produced by a mercury lamp). The system used was a *Karl Suss MJB3 UV400* and it is also presented in Figure II.8. This system allows a maximum resolution of 0.8 μm. Finally, the image is developed. A post exposure bake (or a hard bake) was necessary in order to harden the photoresist and improve the adhesion of this material to the wafer surface. This step was accomplished before or after the development, depending on the type of the photoresist. Due to the strict cleanliness needed, these processes were performed in a class 1000 clean room.

Two different types of photoresist were used and the procedure followed is explained in the next subsections.

4.1.- <u>Positive photoresist</u>

In this type of photoresist, the areas exposed to the light become soluble in the developer. Thus, the pattern of the mask is transferred to the substrate. This process was used to open windows in the field oxide deposited over the semiconductor.

A description of this procedure is shown below:

a) The photoresist used was the *AZ 4533* from *Microchemicals*. The spin coating was performed at 4000 rpm during 30 s. Prior to this photoresist deposition, it was necessary an adhesion promoter: *TI Prime* also from *Microchemicals*, spinned at 6000 rpm for 30 s.

b) The soft bake was carried out at a temperature of 100 ºC for 3 min.

c) A rehydration at room temperature of the photoresist was required in order to allow the photoreaction. The duration of this step was around 30 min.

d) After the ultraviolet exposition with a dose of 6 mW/cm^2, the development was performed for ~3 min. The developer used was *MIF 826*, bought from *Microchemicals.* Afterwards, the wafers were rinsed in deionized (DI) water and blown with nitrogen to dry the water.

e) A hard bake was carried out for 5 min at 130 ºC.

f) In order to remove the SiO_x from the exposed areas, the samples were immersed in a buffered oxide etching (BOE) solution for 2 min.

g) The last step was to remove the photoresist with dimethyl sulfoxide (DMSO) and followed by an isopropyl alcohol (IPA) bath.

BOE, DMSO, and IPA were purchased at *Technic* with the maximum quality available (VLSI grade).

4.2.- Negative photoresist

In this case, the behavior of the photoresist with light is the opposite of the former subsection. Here, the exposition to the light caused that the photoresist becomes polymerized and, therefore, more difficult to dissolve. Thus, the image transferred to the substrate is the negative of the mask image. This process was used to define the metal contacts by a lift-off process.

The steps followed in this process are summarized below:

a) The photoresist was the *AZ nLof 2070* from *Microchemicals*. It was spinned at 3000 rpm during 30 s.

b) The soft bake was carried out for 1 min at 110 ºC.

c) After the ultraviolet exposition using a dose of 8 mW/cm^2, a post exposure bake at 110 ºC during 2 min was performed.

d) The development was carried out for ~3 min followed by a rinse in DI water and a nitrogen blow to dry the samples.

e) After the metal evaporation, the last step was to eliminate the photoresist using DMSO followed by an IPA bath. In this process the metal deposited on the photoresist is lifted-off the surface, leaving only metal on the exposed areas.

II.5.- RAPID THERMAL ANNEALING (RTA)

This system was used for two objectives: to reduce the series resistance associated to the backside contact and to passivate the dangling bonds formed at the interface between the high κ and the semiconductor, thus to reduce the interface trap density. Briefly, a RTA system can increase its temperature within seconds (with a fixed ramp and in a controlled atmosphere) up to around 1000 ºC, and keeps it stable for a certain period, typically seconds or minutes.

An image of the RTA system used is shown in Figure II.9. It is a *RTP-600* model fabricated by *Modular Process Technology*. The maximum achieved temperature is higher than 1000 ºC and it can reach it in only some seconds (less than 1 minute). The

Figure II.9: Image of the RTA system.

heating is carried out with several tungsten halogen lamps and the temperature is controlled by a type *K* thermocouple. The chamber is made of quartz and inside it, a graphite susceptor is placed.[20]

During this thesis, after the top and bottom electrode evaporation, the samples were annealed in the RTA furnace using a forming gas atmosphere (a high-purity mixture of 90% of N_2 and 10% of H_2). This process was usually performed at different temperatures, from 300 to 450 ºC during 20 min. In the following chapters, other temperatures and durations were also used and those details will be mentioned there.

II.6.- MIS FABRICATION

Two different processes were followed to fabricate MIS devices during this thesis. Both fabrication methods are summarized below:

6.1.- Process without field oxide (FOX)

This first procedure was the simplest method to fabricate MIS capacitors. This fabrication method was used to produce devices for process development with minimal

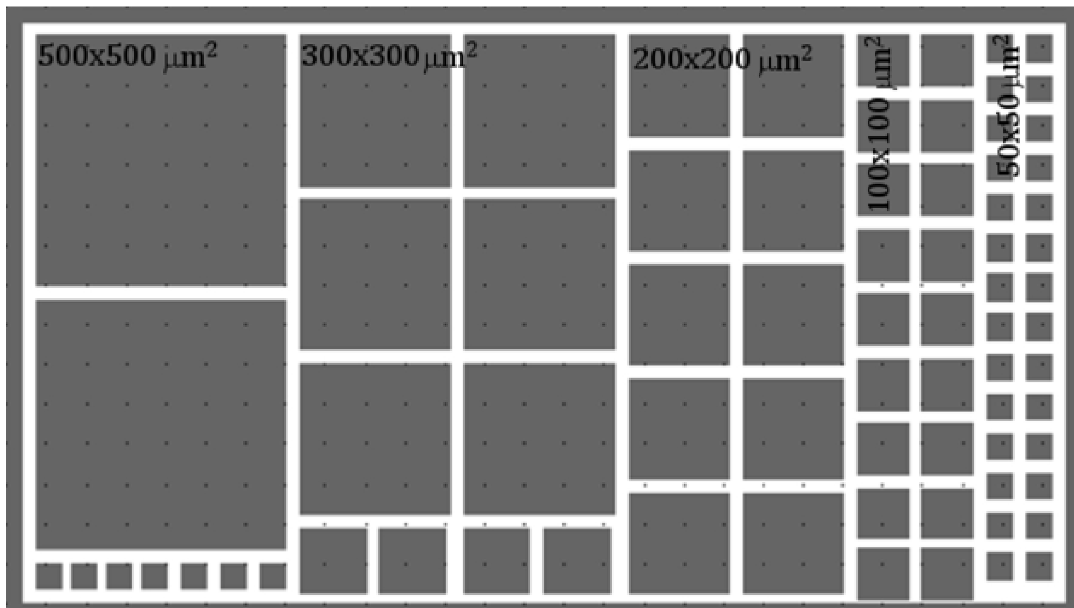

Figure II.10: Dice of the lithography mask of the process without field oxide to define the top electrodes.

manufacturing complexity. It was employed for thick dielectric films were the leakage was not very significant.

The process consisted in the definition of the top metallic electrodes directly on the dielectric (deposited previously by means of HPS) with a negative lithography process (explained in subsection 4.2). After the metal e-beam evaporation and the lift-off of the top electrodes, the devices were finished with the e-beam evaporation of the backside contact. Figure II.10 shows one dice of the lithography mask employed. The complete mask consists in the repetition of the dice several times to cover the complete wafer surface. The defined squares have sizes ranging from 630×630 μm^2 to 50×50 μm^2.

It was observed that, especially for thin dielectrics, the pressure applied by the needles of the probe station on the metallic contacts during the electrical characterization influenced significantly the obtained curves. In many cases, the leakage current density as a function of the gate voltage (J-V_{gate}) measured applying high pressure to the needles was several orders of magnitude higher than the J-V_{gate} curve measured with low pressure. Figure II.11 presents two J-V_{gate} characteristics of the same sample, with the only difference of the applied pressure to the needles during the

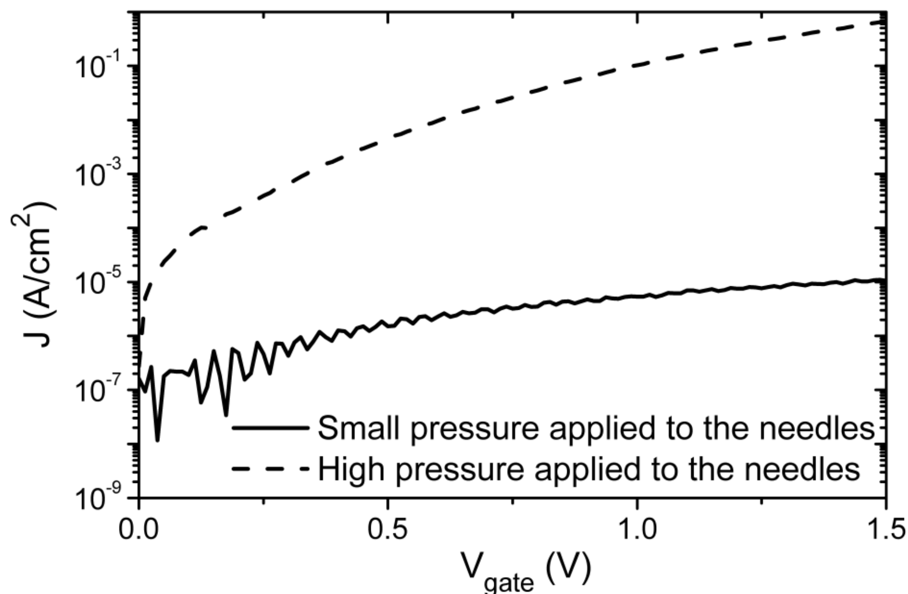

Figure II.11: J-V_{gate} characteristics for the same sample measured applying more or less pressure to the needles.

measurement. More than four orders of magnitude between both measurements could be seen there. This could be explained as follow: due to the small thickness of the dielectric used (around 5-6 nm), if the pressure applied to the needles is high enough to pierce the dielectric, then the dielectric is permanently damaged. However, for moderate leakage, the capacitance measurement is only slightly affected, thus this process can be used for preliminary process assessment. For accurate electrical characterization, other process must be used, more mechanically robust at the cost of process complexity.

6.2.- Process with FOX

This fabrication method was more complex because it included a thick SiO_x film acting as field oxide in order to avoid the degradation observed in the former paragraph. The introduction of contacting pads (little contacts attached to the devices and grown over a thick insulator layer) allows measuring the electrical characteristics without damaging the high κ dielectric with the needles.

In this process, once the wafers were cleaned, a thick SiO_x used as insulator layer was grown with two different methods: SiO_2 obtained with a dry thermal oxidation or SiO_x deposited by e-beam evaporation.

In the first case, the FOX was grown with a dry oxidation process on the Si wafers. The oxidation gas was pure O_2 without H_2O (to guarantee the maximum oxide quality). This dry oxidation was performed at a temperature of 1100 ºC for almost 3 hours, which provided a SiO_2 layer ~200 nm thick. This process was carried out by Prof. Enrique Iborra from the *departamento de Ingeniería Electrónica* of *E.T.S.I. de Telecomunicación* from *Universidad Politécnica de Madrid*. The main advantage of this process is the high quality of the insulator film grown, but it is only possible for Si substrates. However, for the InP wafers, this oxidation process was not possible, thus other alternative must be explored. For that reason, the SiO_x was obtained by e-beam evaporation.

The results obtained by both field oxides were analyzed and no differences were observed between them. Therefore, for simplicity and to reduce thermal budget, most devices were fabricated with evaporated field oxide.

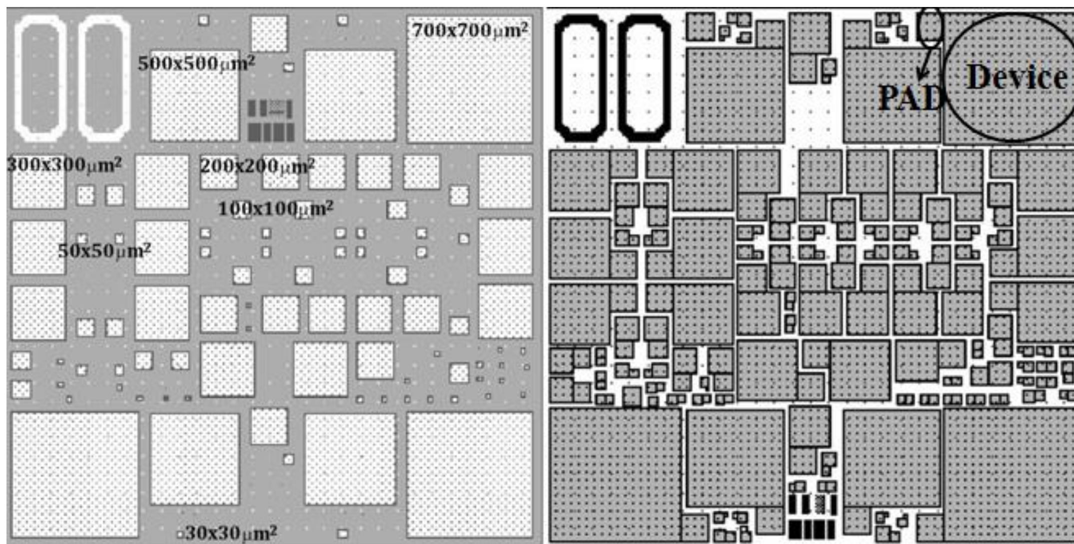

Figure II.12: Lithography mask used for the process with field oxide. In the left hand side is the mask used for opening the SiO_x windows and in the right hand side is for defining the top contacts. A pad and a device are marked in the figure.

To define the SiO_x windows, a positive lithography process (explained in subsection 4.1) was performed, using the mask of the left hand side of Figure II.12. The opened windows had areas from 700×700 μm^2 to 50×50 μm^2. After the HPS deposition, a second lithography process was carried out, in this case, using negative photoresist and the mask presented in the right hand side of Figure II.12. This mask included the pads, little devices placed over the thick SiO_x film with a size ranging from 150×150 μm^2 to 50×50 μm^2. The top metal contacts were e-beam evaporated and, afterwards, the lift-off was performed. MIS devices were finished after the evaporation of the bottom contact in the whole backside of the wafer.

For both processes, a forming gas anneal (FGA) performed in the RTA furnace was carried out to improve the backside electrode and to passivate the interface traps.

In Figure II.13 it is presented the cross-sections of two MIS devices fabricated without FOX and with FOX and pad, following the steps of subsections 6.1 and 6.2, respectively. The total capacitance of the MIS capacitor of Figure II.13(b) is the device capacitance (the same that in Figure II.13(a)) and the pad capacitance. Thus:

$$C_{total} = C_{device} + C_{pad} \quad \textbf{(II.1)}$$

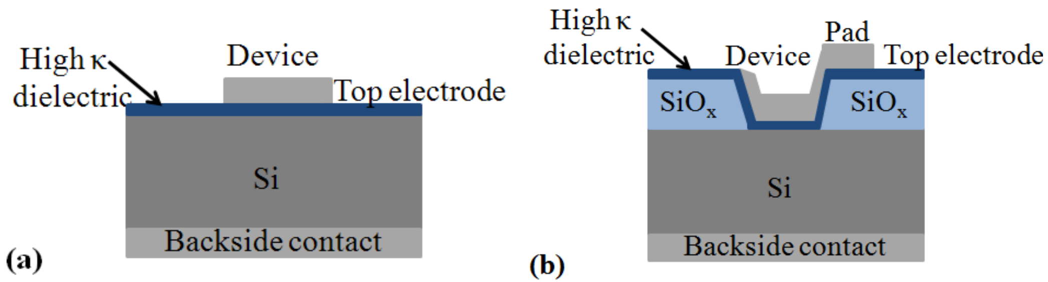

Figure II.13: Cross-section of MIS devices (a) without FOX and (b) with FOX (and pad) fabricated following the steps from subsection 6.1 and 6.2, respectively.

Therefore, the C_{pad} should be much lower than the C_{device} in order to ensure that this contribution does not affect the total capacitance. The C_{pad} is around 9×10^{-12} F, while the measured capacitance is ~4×10^{-10} F, more than two orders of magnitude higher than the C_{pad}. Hence, including the pad produces a small capacitance increase of around 2%, which is irrelevant for device characterization.

II.7.- SUBSTRATES

7.1.- Semiconductor materials

The semiconductor materials used during this thesis for growing the MIS structures were Si and InP wafers. Both kinds of semiconductors were n-type, with a diameter of 2 inches (~5 cm), a thickness of 300 μm and (100) surface orientation. The InP wafers were unintentionally doped but the fabrication process led to n-type behavior.

7.1.A.- Si wafers

For Si, two different types of substrates were selected depending on the characterization technique. On the one hand, for optical measurements, double side polished (DSP) and high resistivity (from 1100 to 3000 Ω·cm) wafers were used. These samples had low doping density with the aim of avoiding the photon absorption by free charge carriers. On the other hand, for electrical characterization, MIS devices were grown on single side polished (SSP) wafers with a resistivity between 1.5 to 5 Ω·cm.

The reason of using these values of the resistivity was to avoid a high series resistance that could cause distortions during the electrical measurements.

Besides, Si wafers used were grown by two different methods: float zone (FZ)[21] that provided a high purity Si with low density of defects and Czochralski (CZ)[22] which is now the most dominant method for growing Si crystals.[23] Both types of substrates were fabricated by the *Institute of Electronic Materials Technology*, *ITME*. MIS devices grown on Si wafers fabricated with the FZ and CZ techniques were measured and no significant differences were obtained in the electrical characteristics.

7.1.B.- InP substrates

In the case of InP, only one kind of wafers were used because only MIS devices were fabricated with this substrate. Thus, SSP samples were utilized with a resistivity ranging from 1 to 5 Ω·cm and fabricated by *InPACT*.

7.2.- Substrate surface cleaning

The electrical properties of the dielectric/semiconductor interface can be strongly affected by the morphological structure and chemical integrity of the semiconductor surface before dielectric deposition.[24] For that reason, prior to the deposition, it was necessary and crucial a proper cleaning of the semiconductor surface in order to remove contamination and defects and to obtain a high quality interface. Since in this thesis Si and InP wafers were used, two different cleaning procedures were carried out for each semiconductor.

7.2.A.- Si wafers

The Si wafers were cleaned following the standard RCA (*Radio Corporation of America*) procedure.[25] The steps for this cleaning method are:

a) An immersion in DMSO followed by an IPA bath. Both processes were carried out at room temperature for some minutes. This step removes the organic contaminants.

b) Standard clean 1 (SC1): the wafers were immersed in a solution of H_2O:H_2O_2:NH_4OH (5:1:1) for 10 min at a temperature between 70-80 ºC. This solution oxidizes the Si surface and dissolves the growing oxide,

removing different organic contaminants and metals such as Na, K, Al and Cu.

c) DI water rinse (with a resistivity of 18.2 MΩ·cm) to reduce wafer temperature and remove residues.

d) HF:H_2O (1:50) dip for 30 s at room temperature to remove the thin native oxide film formed during the SC1 step together with the contaminants trapped.

e) Standard clean 2 (SC2): samples were immersed in a dissolution of H_2O:H_2O_2:HCl (6:1:1) at 70-80 ºC for 10 min. Again, this solution forms a native oxide by the oxidation of the Si surface and traps the remaining heavy metallic (ionic) contaminants.

f) The last step consists on dipping the wafers in DI water and a nitrogen blow.

Just before loading the samples into the chamber, the Si substrates were immersed in an H_2O:HF (1:50) solution for 30 s, in order to remove the native oxide grown during the SC2 process, and then a DI water dip. This step provided a Si surface with a hydrogen passivation (and the surface becomes hydrophobic). It is important to perform this step as fast as possible to minimize the time that the sample is exposed to the atmosphere. Additionally, once the samples were inside the HPS system, the substrates were heated at 500 ºC for 5 min in vacuum with the aim of surface desorption and to improve the cleaning of the chamber after exposing it to the atmosphere.

7.2.B.- InP wafers

These type of substrates were cleaned with a 10% diluted iodic acid solution (HIO_3:H_2O) during 1 min and followed by a dip in DI water for rinsing.[26,27] With this step, the first InP layers were removed and, therefore, the surface contamination was eliminated.[28]

Besides, before the introduction of these samples into the HPS system, the same cleaning carried out for the Si wafers (HF-cleaning) were performed for 30 s in order to remove the native oxides and then the samples were washed in DI water. In this case, no heating of the samples in vacuum was carried out to avoid In diffusion and surface degradation.

REFERENCES

[1] U. Poppe, J. Schubert, R. R. Arons, W. Evers, C. H. Freiburg, W. Reichert, K. Schmidt, W. Sybertz, K. Urban. "*Direct production of crystalline superconducting thin films of* $YBa_2Cu_3O_7$ *by high-pressure oxygen sputtering*". Solid State Comm., 66, 661 (1988).

[2] E. San Andrés Serrano. "*Fabricación y caracterización de dieléctricos de alta permitividad para su aplicación como aislantes de puerta en dispositivos MIS*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2004).

[3] M. Toledano-Luque. "*Growth and characterization of high-k dielectrics for field effect devices*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2008).

[4] P. C. Feijoo Guerro. "*High permittivity dielectrics for next generatios of integrated circuits*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2013).

[5] E. San Andrés, M. Toledano-Luque, A. del Prado, M. A. Navacerrada, I. Mártil, G. González-Díaz, W. Bohne, J. Röhrich. "*Physical properties of high pressure reactively sputtered* TiO_2". J. Vac. Sci. Technol. A, 23, 1253 (2005).

[6] M. Toledano-Luque, E. San Andrés, A. del Prado, I. Mártil, M. L. Lucía, G. González-Díaz, F. L. Martínez, W. Bohne, J. Röhrich, E. Strub. "*High-pressure reactively sputtered* HfO_2*: Composition, morphology, and optical properties*". J. Appl. Phys., 102, 044106 (2007).

[7] P. C. Feijoo, M. A. Pampillón, E. San Andrés, M. L. Lucía. "*Optimization of scandium oxide growth by high pressure sputtering on silicon*". Thin Solid Films, 526, 81 (2012).

[8] P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Optimization of gadolinium oxide growth deposited on Si by high pressure sputtering*". J. Vac. Sci. Technol. B, 31, 01A103 (2013).

[9] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Nano-laminate vs. direct deposition of high permittivity gadolinium scandate on silicon by high pressure sputtering*". Thin Solid Films, 593, 62 (2015).

[10] C. R. Aita. "*Reactive sputter deposition of metal oxide nanolaminates*". J. Phys.: Condens. Matter., 20, 264006 (2008).

[11] S. M. Rossnagel, J. J. Cuomo, W. D. Westwood. "Handbook of plasma processing technology: Fundamentals, etching, deposition, and surface interactions". Noyes Publications. Mill Road, Park Ridge, New Jersey, 1990.

[12] S. Wolf. "Microchip manufacturing". Lattice Press. Sunset Beach, California, 2004.

[13] S. Wolf, R. N. Tauber. "Silicon Processing for the VLSI Era. Volume 1: Process Technology". Lattice Press. Sunset Beach, California, 1986.

[14] A. Gras-Marti, J. A. Valles-Abarca. "*Slowing down and thermalization of sputtered particle fluxes: energy distributions*". J. Appl. Phys., 54, 1071 (1983).

[15] J. A. Valles-Abarca, A. Gras-Marti. "*Evolutions towards thermalization and diffusion of sputtered particle fluxes: spatial profile*". J. Appl. Phys., 55, 1370 (1984).

[16] R. W. B. Pearse, A. G Gaydon. "*The identification of molecular spectra*". 4th edition. John Wiley & Sons, Inc., New York (1976).

[17] G. Norlén. "*Wavelengths and energy levels of Ar I and Ar II based on new interferometric measurements in the region 3400-9800 Å*". Phys. Scr. 8, 249 (1973).

[18] B. Wende, "*Optical transition probabilities of the configurations $3p^5 4s$-$3p^5 5p$ of Argon I,*" Zeitschrift für Physik 213, 341 (1968).

[19] S. A. Campbell. "The science and engineering of microelectronic fabrication". Oxford University Press. Oxford, New York, 2001.

[20] R. Doering, Y. Nishi. "Handbook of semiconductor manufacturing technology". CRC Press. Boca Raton, Florida, 2008.

[21] H. C. Theuerer. "*Method of processing semiconductive materials*". US Patent 3060123 (1962).

[22] J. Czochralski. "*Ein neues Yerfahren zur Messung des Kristallisationsgeschwidig- keit der Metalle [A new method for the measurement of crystallization rate of metals]*". Zeitschrift für physikalische Chemie, 92, 219 (1918).

[23] Q. Chen, Y. Jiang, J. Yan, M. Qin. "*Progress in modeling of fluid flows in crystal growth processes*". Prog. Nat. Sci., 18, 1465 (2008).

[24] T. Ohmi, M. Miyashita, M. Itano, T. Imaoka, I. Kawanabe. "*Dependence of thin-oxide films quality on surface microroughness*". IEEE Trans. Electron Dev., 39, 537 (1992).

[25] W. Kern, D. A. Puotinen. "*Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology*". RCA Rev., 31, 187 (1970).

[26] E. Redondo Romero. "*Realización de transistores MISFET sobre semiconductores compuestos del grupo III-V*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2001).

[27] E. Redondo, I. Mártil, G. González-Díaz, P. Fernández, R. Cimas. "*Improvement of SiN_x:H/InP gate structures for the fabrication of metal-insulator-semiconductor field-effect transistors*". Semicond. Sci. Technol., 17, 672 (2002).

[28] S. K. Krawczyk, G. Hollinger. "*Photoluminescence and x-ray photoelectron spectroscopy measurements of InP surface treated by acid and base solutions*". Appl. Phys. Lett., 45, 870 (1984).

Chapter III:

Characterization techniques

The study of the semiconductor/high κ interface and the properties of the dielectric film, grown using the fabrication techniques described in the former chapter, are one of the main objectives of this thesis. For this reason, several characterization techniques were used and they are described along this chapter.

The present chapter is divided in two sections: firstly, the structural and physical characterizations are described. With these methods, it can be obtained the thickness, composition and crystallinity for the gate stack, composed of the high κ material and an interfacial layer that grows between the semiconductor and the dielectric film. In this section, the Fourier transform infrared spectroscopy (FTIR), grazing incident X ray diffraction (GIXRD), X ray reflectivity (XRR), X ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) techniques are briefly introduced.

Afterwards, the electrical characterization techniques are presented. The description and the study of the electrical behavior of metal-insulator-semiconductor (MIS) devices is a key part of this thesis. For that reason, it is introduced the physics of these capacitors. For this electrical characterization, the capacitance per unit area (C) and conductance (G) as a function of gate voltage (V_{gate}) curves have to be measured. For these characteristics, we obtain the equivalent oxide thickness (EOT), the interfacial traps density (D_{it}), the frequency dispersion and the hysteresis cycle.

Besides, the study of the gate leakage current density (J) as a function of V_{gate} is also described at the end of the chapter, in order to understand the conduction mechanisms presented in the MIS devices fabricated.

III.1.- STRUCTURAL CHARACTERIZATION TECHNIQUES

1.1.- Fourier transform infrared spectroscopy (FTIR)

FTIR is a non destructive technique that measures the absorbance for infrared wavelengths of the grown films. This method permits to get information on which molecules are present in a sample and their concentration,[1] together with qualitative and quantitative chemical information such as the bonding structure, the vibration modes2 or the chemical neighborhood.3 In this case, this information is obtained not only from the high κ layer but also from the interlayer formed between the dielectric material and the semiconductor substrate.

In Figure III.1, a schematic image of a FTIR spectrometer is presented. A light source (assumed monochromatic for this description) emits a beam of intensity I_0 directed to a beam splitter that reflects the 50% to a fixed mirror and transmits the other 50% to a mobile mirror. The reflected beams are merged again in the beam splitter and an interference is observed due to the difference of path lengths introduced by the position of the mobile mirror. The resultant beam intensity, I, is given by:[4,]5

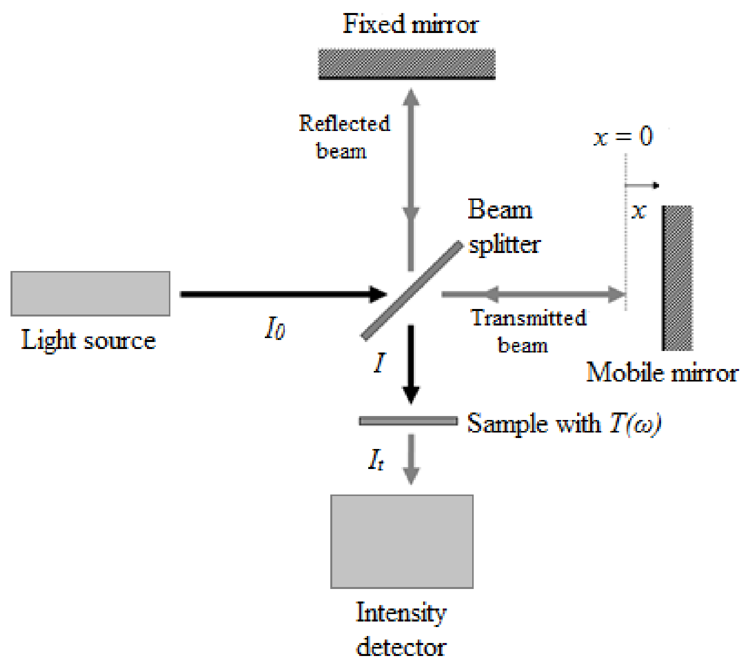

Figure III.1: Schematic image of a Fourier transform infrared spectrometer.

$$I = I_0 cos\left(\frac{2\omega x}{c}\right) \qquad \textbf{(III.1)}$$

where, I_0 is the initial beam intensity, ω is the frequency of the beam, x is the position of the mobile mirror ($x = 0$ when both mirrors are at the same distance of the beam splitter) and c is the light velocity. This beam passes through the sample with transmittance $T(\omega)$ and the transmitted beam intensity is then:

$$I_t = T(\omega) I_0 cos\left(\frac{2\omega x}{c}\right) \qquad \textbf{(III.2)}$$

If the light source is not monochromatic, the reasoning is similar but the integration for all the frequencies has to be made. In this case, the detected intensity as a function of the mobile mirror position is:

$$I_t(x) = I(\infty) + \int_{-\infty}^{\infty} T(\omega) I_0 cos\left(\frac{2\omega x}{c}\right) d\omega \qquad \textbf{(III.3)}$$

being $I(\infty)$ an integration constant. The second term represents the Fourier transform of the transmittance of the sample, $T(\omega)$. Thus, if the inverse Fourier transform of the $I_t(x)$ is calculated, $T(\omega)$ is obtained.

As a first approach, if the sample thickness, t, is known, the absorption coefficient, $\alpha(\omega)$, is related to $T(\omega)$ by the following equation:

$$T(\omega) = e^{-\alpha(\omega)t} \quad \Rightarrow \quad \alpha(\omega) = -\frac{1}{t} lnT(\omega) \qquad \textbf{(III.4)}$$

Since this model does not take into account the multiple reflections at the interfaces, the result of equation III.4 is only an approximation of the absorption coefficient, and is denoted as normalized absorbance. In a FTIR spectrum, the absorbance is obtained as a function of the wavenumber, v, which is the inverse of the wavelength, λ, and is expressed in cm^{-1}.

FTIR measurements were obtained in the *CAI de Espectroscopía* of the *Universidad Complutense de Madrid* using a *FT-IR Nicolet Magna 750 series II* spectrometer working in the transmission mode. The results were measured in the mid-infrared range (between 4000 to 400 cm^{-1}) with an *everGlo* infrared light source and a deuterated tri-glycine sulfate window and a KBr detector. The spectra were taken with a resolution of 16 cm^{-1}.

The interest of obtaining the absorbance in the region of this mid-infrared range is that most of the molecular groups have the bonding resonance frequencies in this zone of the electromagnetic spectrum.6

The obtained spectra correspond to the deposited film and the substrate (in this thesis, double side polished silicon wafers were used for these measurements). Therefore, for the analysis of the grown layer, the contribution of the semiconductor has to be removed. So, the experimental procedure followed was to measure a Si wafer of the same lot, etched with HF just before FTIR measurements, in order to minimize the native oxide contribution. This spectrum was used to correct the sample substrate absorbance. However, this approach has two drawbacks: slight differences in wafer thicknesses yield residual Si peaks in the spectra and some native oxide growth is unavoidable because after HF etching the substrate is transferred to the FTIR system in an uncontrolled atmosphere. It is noteworthy to point out that the backside of these high κ samples is bare Si, so a fraction of the measured SiO_x signal might be due to the backside native oxide. Nevertheless, since all samples followed similar processing after deposition, the differences in backside oxidation should be minimal and FTIR results can be used, at least, to give qualitative information about interfacial SiO_x thickness.

In Figure III.2(a) is presented the FTIR spectrum of a Si substrate (etched with HF) used for the substrate correction. Only the range between 1200 and 400 cm^{-1} is shown due to the absence of relevant peaks in the remaining part of the spectrum. The peak located at 610 cm^{-1} is attributed to a Si phonon absorption,[7] while the peak around 667 cm^{-1} is due to the presence of CO_2 in the FTIR chamber during the measurement.8 The rest of the observed peaks are due to the Si substrate. All these mentioned peaks will appear in the measured spectra of the analyzed samples. To remove the Si substrate contribution, the spectrum of the bare substrate will be subtracted from the measured spectrum, and thus, the contribution of the thin film and the interlayer can be analyzed.

Figure III.2(b) shows the absorbance of a Gd_2O_3 film after the Si substrate correction. The peak at 610 cm^{-1} is observed downwards due to slight wafer thickness variations between the sample and the reference Si. On the other hand, the peak located at 667 cm^{-1} is seen upwards, indicating a higher amount of residual CO_2 in the chamber

during this measurement as compared to the Si reference case. Therefore, these peaks are not related to the high κ and will not be further discussed.

The band associated to the Si-O stretching vibration mode is observed at around 1070 cm^{-1}, as it is referenced in many works.[9-11] This peak shifts to higher or lower wavenumbers with the oxygen content or with the stress of the film.[9,10] If the peak is upwards (as it will be in most cases), it indicates that the SiO_x film is thicker in the sample than in the HF etched Si. However, if it points downwards, it means that the thickness of this oxide at the interface is lower in the sample than in the reference Si (the reference wafer can suffer from atmospheric oxidation during the transfer from the HF bath to the FTIR system). In the case of Figure III.2(b), a very small band is observed pointing upwards at around 1035 cm^{-1}, which can be related to the Si-O presence. This points out to a SiO_x film slightly thicker (but comparable in thickness) than in the HF etched Si.

Concerning Gd_2O_3, due to the high atomic mass of Gd, the vibration of the Gd-O bond would appear at the wavenumber range of 540-370 cm^{-1},[12] as it is observed in Figure III.2(c) for Gd_2O_3 powder. The Gd-O-Si bond would show an absorbance at wavenumbers below 400 cm^{-1}.[13] Due to the measurement range and the low thickness of the deposited films (in the order of 5-10 nm for all the analyzed samples), the presence of Gd-O-Si and Gd-O bonds could not be clearly observed in the FTIR spectra, as Figure III.2(b) shows.

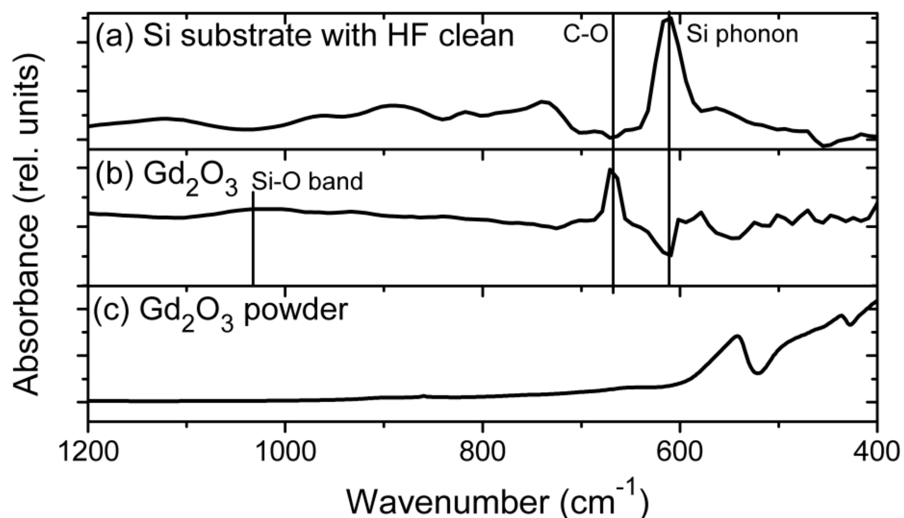

Figure III.2: FTIR spectra for (a) Si substrate with HF clean used for corrections, (b) as deposited Gd_2O_3 film (without the contribution of the Si substrate) and (c) Gd_2O_3 powder.

For the Sc_2O_3 case, no traces of absorbance peaks related to Sc-O bonds were observed in the fabricated samples. Some works reported absorbance for Sc-O at wavenumbers between 600 to 400 cm^{-1}.[14-16] The absence of these peaks in our layers is also due to the thin dielectric thickness.

Therefore, in the results sections of this thesis, we will focus on the 1200-900 cm^{-1} range, in order to determine qualitatively the SiO_x thickness at the interface between the high κ dielectric and the Si substrate.

1.2.- Grazing incidence X ray diffraction (GIXRD)

GIXRD is a non destructive technique that permits to identify, unambiguously, the structure of crystalline and polycrystalline thin films, with a thickness in the order of few nanometers and provides information of the crystal phases.[17,18]

This technique consists on directing an X ray source to the analyzed sample. When the incident beam streaks a crystalline plane with indexes *hkl*, there would be a constructive interference if the diffracted angle, θ_{hkl}, verifies the Bragg law:[19]

$$n\lambda = 2d_{hkl}sin\theta_{hkl} \quad \textbf{(III.5)}$$

being n, a positive integer, λ is the wavelength of the incident beam and d_{hkl}, the interplanar distance. The *hkl* subscripts denote the Miller indices of the planes considered in the diffraction.

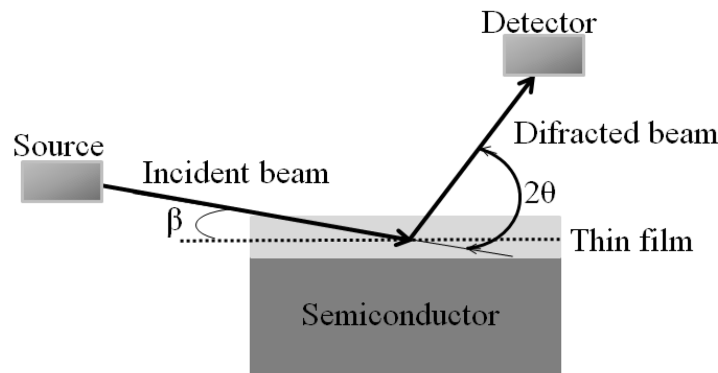

Figure III.3: Schema of the GIXRD system used: β is a fixed angle while the detector performs a scan in 2θ.

In the case of the grazing incidence, the incident angle to the sample, *β*, is fixed and small (= 0.5°) and the detector makes a scan in *2θ*. A schematic of this system is shown in Figure III.3. These analysis were performed using a *PANalytical* diffractometer, model *X'Pert PRO MRD*, with a wavelength of the X ray source of 0.1541 nm, corresponding to the Cu K_{α} line. The measured *2θ* range was between 10º and 70º. The measurements were carried out at the *CAI de Difracción de Rayos X* of the *Universidad Complutense de Madrid*.

In Figure III.4 is presented a complete spectrum of a Si sample with Gd deposited in a mixed Ar/O_2 atmosphere. Three peaks can be clearly observed, thus, the sample shows a polycrystalline structure. The peaks located at 29.3º and 42.3º corresponds to the monoclinic phase of Gd_2O_3.[20] However, the peak at around 56º is observed in all the spectra with the same shape and intensity and corresponds to diffraction patterns of the Si substrate, according the *Inorganic Crystal Structure Database* (*JCPDS* file number *89-5012*) and it was also observed in other works.[21-24] This peak is observed due to the thin thickness of the top layer and no other significant information is obtained.

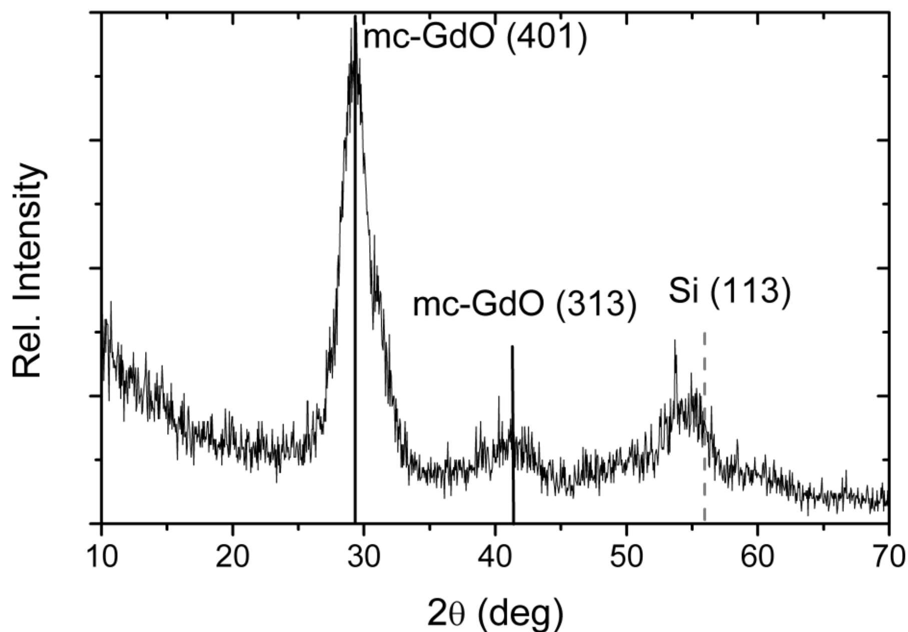

Figure III.4: GIXRD spectra of a Si substrate sputtered with Gd in an Ar/O_2 atmosphere. The observed diffraction peaks have been identified as monoclinic gadolinium oxide and are marked with black solid lines. Also, a Si substrate contribution is observed and is indicated with a grey dashed line.

In the case of Sc_2O_3, the only known stable structure is the cubic bixbyite phase[25] with peaks located at 22º, 31.5º and 43º.

For that reason, the GIXRD spectra that will be presented in the rest of the thesis will be given between 10 and 50º. In this range, all the materials analyzed during this thesis will show diffraction peaks if they would have a polycrystalline character.

1.3.- X ray reflectometry (XRR)

XRR is a non destructive and non contact method to obtain the thickness of thin films with high precision. In addition, this technique is also employed for the determination of density and roughness of films and also multilayers.[26]

With XRR measurements, the thicknesses of thin high κ dielectrics layers can be obtained. Using a bilayer model, it is also possible to determine the thickness of the interlayer between the high κ material and the semiconductor.

For this purpose, the same system used for GIXRD was utilized but sweeping low 2θ angles, typically between 0.2º and 4º. The thicknesses were obtained by fitting the reflection spectra with a segmented algorithm implemented on a proprietary software from *Philips*, using as the fitting parameters the density, thickness and roughness of the films.[27]

1.4.- X ray photoelectron spectroscopy (XPS)

XPS is an analytical technique with sub-monolayer sensitivity that can provide information about the composition and chemical bonding of the surface and near-surface region of thin films.[17,28,29]

The bombardment of materials (placed in an ultra high vacuum chamber) with a low energy and monochromatic X ray source causes photoelectron emission. The incident beam produces the ejection of core-level electrons from the sample atoms. The energy of these photoemitted electrons, detected by an electron energy analyzer, is related to their binding energy and is characteristic of the element. By measuring the kinetic energy of the photoelectrons that reach the detector and its amount, an emission spectrum is obtained. According to the photoelectric effect given by Einstein in 1905, the relationship

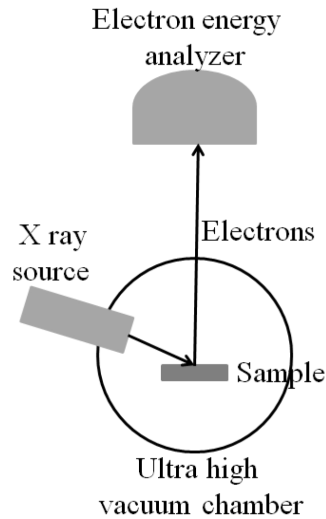

Figure III.5: Schematic of the XPS system used.

between the kinetic energy of the electrons, E_k, and their binding energy, BE, is calculated in accordance with the following equation:

$$E_k = h\nu - BE \quad \textbf{(III.6)}$$

where $h\nu$ is the incident beam energy.

These measurements were carried out using a *VG Escalab 200 R* spectrometer provided with an Al K_α radiation source ($h\nu$ = 1486.6 eV), powered at 120 W and with a hemispherical electron analyzer. The analyses were performed at the *Instituto de Catálisis y Petroleoquímica* of the *Consejo Superior de Investigaciones Científicas*. In Figure III.5 a schematic of this system is presented.

Figure III.6 shows the XPS wide scan or survey spectrum of a $Gd_{0.9}Sc_{1.1}O_3$ sample. Several peaks at different binding energies are observed. These energies are calibrated relative to the C 1s peak located at ~285 eV.[30,31] It is important to highlight that the sample, after the deposition process, is exposed to the atmosphere. Thus, this C 1s peak is due to surface adsorption, but no other significant information can be extracted from it. The O_{KLL} peak represents the energy of the electrons ejected from the atoms due to the filling of the O 1s state (K shell) by an electron from the L shell coupled with the ejection of an electron from an L shell. This peak is located around 745 eV.[32] The rest of the peaks present in the spectrum are related to Gd 4d,[33] Sc 2p[34] and O 1s[35] and will be further analyzed in the following chapters.

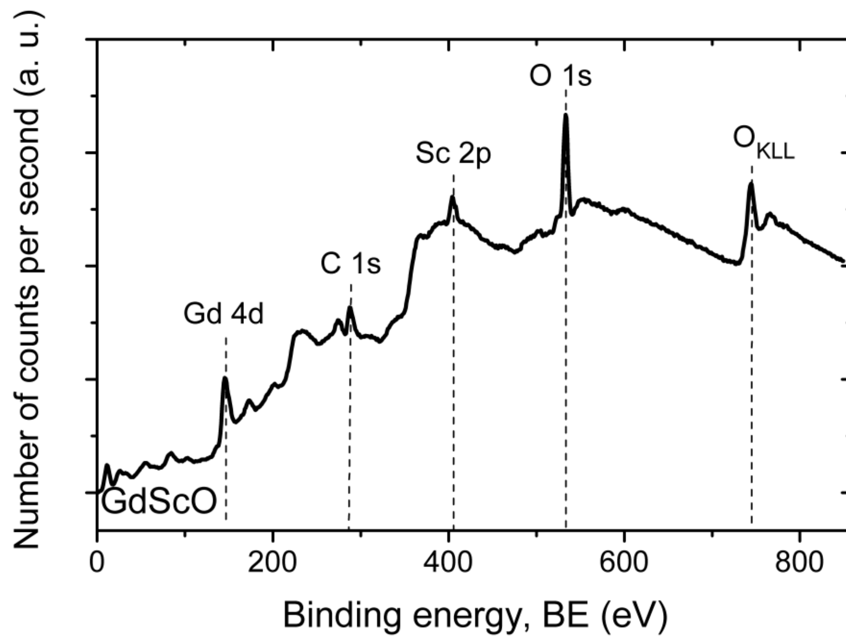

Figure III.6: XPS wide scan or survey spectrum of $Gd_{0.9}Sc_{1.1}O_3$ sample. The identified peaks are related to Gd, C, Sc and O and are marked in the figure.

1.5.- Transmission electron microscopy (TEM)

TEM provides ultrahigh resolution images achieving atomic resolution of thin films. This technique is used routinely to measure the thickness of gate oxides (and also the interface layer) with high accuracy, as well as to visualize materials defects, device geometry and structure. Also, it measures grain size distributions.[17,28,36]

This microscopy technique uses an electron beam that is focused by condenser lenses and is directed to the sample. To produce image, the incident beam must pass through the sample. For that reason, the analyzed sample must be thin enough to avoid excessive absorption, in the order of ten to hundreds of nanometers thick. By the use of several electromagnetic lenses the image is enlarged and is projected to a fluorescent screen. A schematic image of this system is shown in Figure III.7.

Besides, some of the microscopes used can perform analytical measurements by means of energy dispersive X ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS). These techniques allow obtaining chemical analysis of the samples, identifying the elements presented.

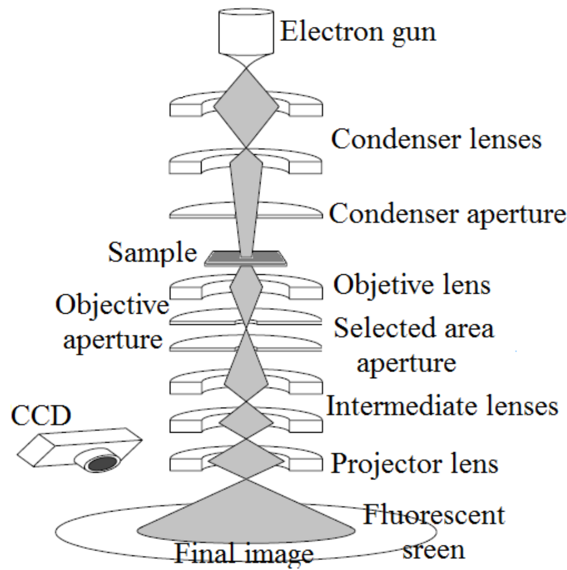

Figure III.7: Schematic of the transmission electron microscope.

During this thesis, two different transmission electron microscopes were use to obtain the high resolution images. One was a *FEI Tecnai T20* belonging to the *Instituto de Nanociencia de Aragón* from the *Universidad de Zaragoza*, operating at 200 kV. The other was a *JEOL JEM 3000F* at 300 kV from *CAI de Microscopía Electrónica* of the *Universidad Complutense de Madrid*.

As it was mentioned before, samples must be thin enough to permit the electron beam to pass through it. For that reason, the preparation of the samples to create a lamellae is an important issue to achieve the desirable thickness. Two different procedures were followed for this purpose: the preparation by *ex situ* lift out technique,[37] where a specific region is milled by focused ion beam (FIB), and a manual preparation.[38] The first method was carried out in the *Instituto de Nanociencia de Aragón*, while the second one was performed at the *CAI de Microscopía Electrónica*.

III.2.- ELECTRICAL CHARACTERIZATION TECHNIQUES

Before describing the electrical characterization techniques used in this thesis, the fundamentals of the metal-insulator-semiconductor (MIS) structure will be briefly described.

2.1.- MIS capacitors

To explain the operation of the MIS structure, an n-type semiconductor will be assumed (for the p-type, the explanation would be analogous).[39,40] First, an ideal MIS capacitor will be considered. In this model the Fermi level of the semiconductor is aligned with the work function of the gate metal, and the oxide is an ideal insulator, without charges or traps. The semiconductor will be assumed to be grounded.

2.1.A.- Ideal MIS capacitor in equilibrium

When a voltage of 0 V is applied to the metal, which is the gate of the device (V_{gate} = 0 V), the metal and the semiconductor Fermi levels, E_{Fm} and E_{Fs}, respectively, are aligned and, as a consequence, the bands are horizontal. In this case, the work function difference between the metal and the semiconductor, ϕ_{MS}, is 0 eV. There is not any net charge accumulation in the structure. This is called the flatband situation and the band diagram is represented in Figure III.8.

2.1.B.- Ideal MIS capacitor under bias

When a voltage is applied to the gate of the MIS structure, three different situations can happen, depending on the applied voltage:

(a) Accumulation: A positive voltage is applied to the gate ($V_{gate} > 0$ V). The electrons, which are the majority carriers of the semiconductor, are attracted to the insulator/semiconductor interface. The oxide blocks these carriers, which cannot reach the gate metal. In this situation, an accumulation of electrons is produced at this interface and thus, this regime is called accumulation.

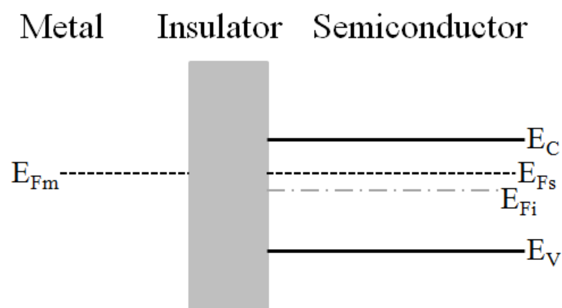

Figure III.8: Band diagram of an ideal MIS structure in equilibrium.

(b) <u>Depletion</u>: Now, a negative voltage is applied to the metal, thus $V_{gate} < 0$ V. The electrons are now repelled away from the semiconductor/insulator interface. Therefore, the region close to the insulator/semiconductor interface is depleted of majority carriers and it is called depletion zone. This zone has a positive charge, due to the ionized donor impurities. Its width increases when the voltage applied to the metal is decreased. This situation is known as depletion.

(c) <u>Inversion</u>: If the applied voltage is more negative, at some point, the minority holes (created by thermal generation) that are attracted to the semiconductor surface exceed the amount of electrons (in other words, the surface Fermi level crosses the intrinsic Fermi level, E_{Fi}). This is the weak inversion situation. Reducing further the voltage eventually produces that the hole concentration at the interface is higher than the electron concentration of the semiconductor. This situation is denoted as strong inversion. In inversion the depletion depth does not increase further, since the higher electric field would be screened by minority charges on the semiconductor surface.

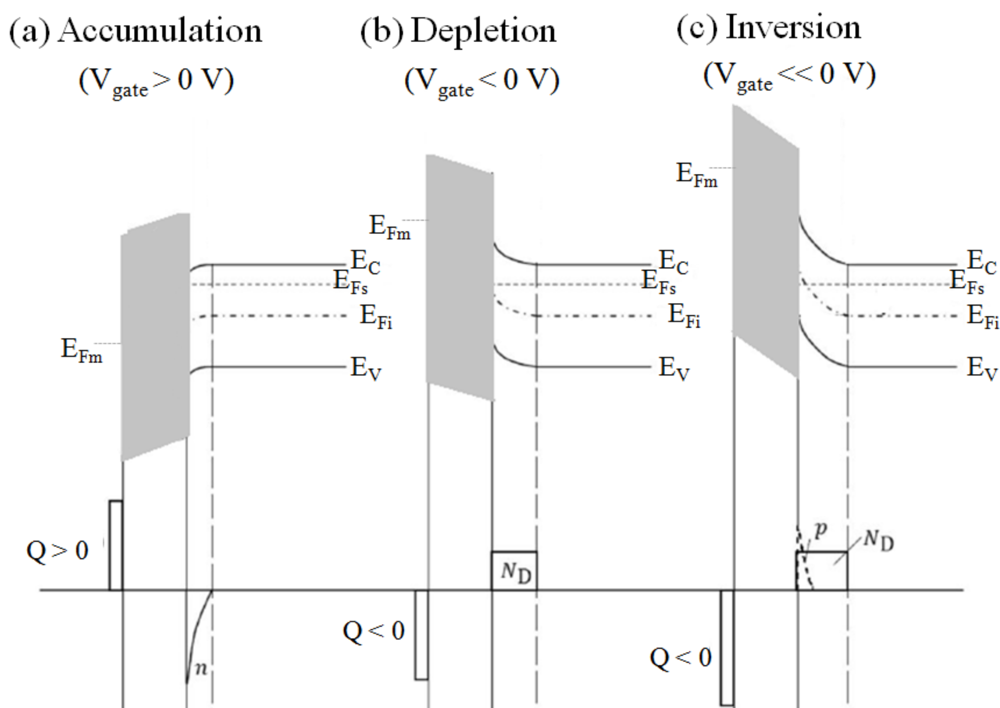

Figure III.9: Band diagram (and charge concentration) of an ideal MIS structure under bias. The accumulation (in the left hand side), depletion (in the center) and inversion (in the

The band diagrams (and the charge concentrations) of these three situations are qualitatively represented in Figure III.9.

2.1.C.- Real MIS structure

In the case of a real MIS capacitor, some particularities are present. The first one is that, in general, the semiconductor work function is different than the metal work function. Thus, $\phi_{MS} \neq 0$ eV. Therefore, some charge accumulation is located at the insulator/semiconductor interface and the bands are bended even in equilibrium. For that reason, to have horizontal bands in the semiconductor and, thus, no charge accumulation, it is necessary to apply a voltage to the gate. This is known as the flatband voltage, V_{FB}. Consequently, to be in the accumulation situation a gate voltage higher that V_{FB} must be applied. For $V_{gate} < V_{FB}$, the structure would be in depletion or in inversion if $V_{gate} << V_{FB}$.

Another important issue is the presence of charges in the insulator, Q_{INS}. These can be fixed charge, trapped charge and mobile charge.[39,41] The fixed charge is a net charge that is produced by the fabrication process. It is located at the insulator/semiconductor interface and it is modeled as a surface charge. The trapped charge is related to trap centers within the insulator, which can capture or emit carriers during device operation. The mobile charge is due to the presence of alkali ions, such as Na^+ or K^+. In the next section, the influence of these charges to the MIS structure will be studied.

Finally, some states or traps exist at the interface between the insulator and the semiconductor. This is known as the interfacial state density, D_{it}. These states are due to dangling bonds from the semiconductor surface.[42] To ensure the proper operation of the MOSFETs, it is necessary to obtain a low D_{it} value, since these charges would impact severely the channel mobility. In the following section, this will be further studied.

2.2.- Capacitive behavior of MIS devices: C-V_{gate} characterization

The capacitance, *C*, of a MIS structure is usually defined as the dynamic capacitance of the structure:

$$C = \frac{dQ_{gate}}{dV_{gate}} = \frac{d(Q_S + Q_{INS})}{dV_{gate}} \quad \textbf{(III.7)}$$

being Q_{gate} and Q_s, the gate and the semiconductor charges.

The capacitance can be modeled by two capacitors in series[39] and thus:

$$\frac{1}{C} = \frac{1}{C_{INS}} + \frac{1}{C_s} \qquad \textbf{(III.8)}$$

where C_{INS} and C_s are the insulator and semiconductor capacitances, respectively.

To measure the capacitance, the MIS device is polarized to a gate voltage, V_{gate}, and a small *ac* signal is superimposed. Depending on the frequency of this signal, the behavior of the MIS capacitor is different. C_{INS} has a fixed value for all the voltages and frequencies while C_s is a variable capacitance, which depends on the applied voltage (that determines the regime of the MIS structure) and, also, the frequency of the *ac* signal (that determines which carriers are able to follow this signal).

Starting from an accumulation situation where the majority carriers are accumulated at the insulator/semiconductor interface in a very thin layer. Thus, $C_s >> C_{INS}$. As a consequence, from equation III.8, the accumulation capacitance is approximately the oxide capacitance. This is observed for both low and high frequencies because the charge variations are due to the majority carriers. When the applied voltage is reduced, the device will enter depletion. In this situation the semiconductor capacitance is determined by the depletion depth and the contribution of C_s becomes relevant. As it was mentioned before, the depletion width increases when the voltage is decreased and, as C_s is inversely proportional to this width, the total capacitance is reduced. Again, the majority carriers are responsible of the charge changes and the low and high frequency curves coincide. Finally, in the inversion case, two different behaviors are observed depending on the measured frequency. Now, the minority carriers are accumulated at the interface between the insulator and the semiconductor. If the frequency is low, the minorities can follow the *ac* signal and, again, $C_s >> C_{INS}$ and therefore, the same capacitance observed in accumulation is measured. However, if the *ac* signal frequency is high, these minority carriers are not able to follow the alternating signal and the total capacitance is determined both by the oxide and the depletion depth. Since the depletion depth in inversion does not increase further, the capacitance remains constant even if the voltage is further reduced.

In Figure III.10, C-V_{gate} characteristics are observed for both low and high frequencies.

During this thesis, only high frequency curves were measured. To obtain reasonable results for the low frequency measurements, a relative thick oxide film (with low leakage current density) has to be used to minimize gate leakage that would make difficult to determine incremental charge. Since that was not the case (because the dielectric layers fabricated during this work were thin), these measurements were not performed.

The C-V_{gate} characteristics were obtained using an *Agilent 4294A* impedance analyzer. This system can measure frequencies ranging from 40 Hz to 100 MHz. The sample is contacted with a probe station placed inside a Faraday box. The contact needles can be positioned using micrometric screws.

The measuring frequency was varied in the 1 kHz-1 MHz range. The optimal signal frequency is as high as possible in order to maximize capacitance signal, but not too high, to avoid capacitance decrease due to the coupled effect of conductance and series resistance.[43]

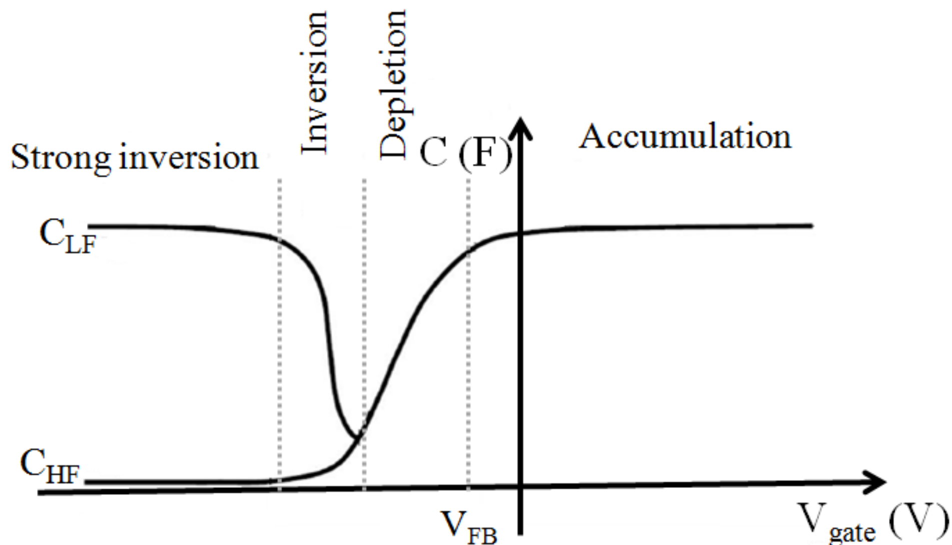

Figure III.10: C-V_{gate} curves for low and high frequencies. In the figure are marked the four different situations of the MIS structure depending on the applied gate voltage.

2.2.A.- Effects of Q_{INS} in the C-V_{gate} characteristics

The presence of Q_{INS} produces some changes to the flatband voltage, which can be expressed by:[39,41]

$$V_{FB} = \phi_{MS} - \frac{Q_{INS}}{C_{INS}} \qquad \textbf{(III.9)}$$

An important characteristic of Q_{INS} is that its value does not depend on the applied voltage. This means that the C-V_{gate} curve would be shifted according equation (III.9), but the shape will not change. In Figure III.11, the C-V_{gate} characteristics of a MIS structure without and with $Q_{INS} > 0$ are shown.

2.2.B.- Effects of D_{it} in the C-V_{gate} characteristics

Other important effect produced in the C-V_{gate} curves is due to a high interfacial trap density, D_{it}. These states are located inside the bandgap and they have an associated interface charge, Q_{it}. They have the property of interchanging carriers with the semiconductor and thus, their occupancy state is modified when the Fermi level changes.

The interface states can present donor or acceptor character. Donors are neutral when they are occupied and they can donate an electron, acquiring positive charge.

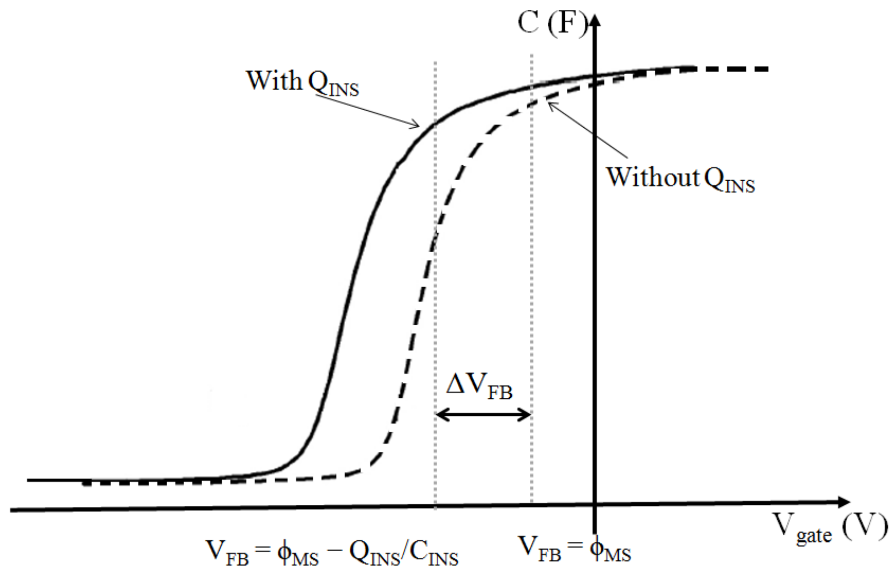

Figure III.11: Shift produced in the C-V_{gate} characteristics of a MIS structure as a consequence of the presence of $Q_{INS} > 0$.

Conversely, acceptors are neutral when they have a hole and they become negative after trapping an electron. The donor states with an energy lower than the Fermi level (they are occupied) are neutral and those with a higher energy have a positive charge. The acceptor states with an energy higher than the Fermi level are neutral (they are unoccupied) and those with lower energy have a negative charge.

When the MIS structure is under bias, a modification of E_{Fs} will be produced and the occupancy of the interface states will change.

When $V_{gate} = V_{FB}$, we can assume a distribution of D_{it} with all the interface states neutral (thus, $Q_{it} = 0$). In this case, the states with an energy lower than the Fermi level are donors and those with higher energy are acceptors. This situation is presented in Figure III.12(a).

Now, $V_{gate} > V_{FB}$ and the bands are bended downwards. E_{Fs} gets closer to the conduction band and some acceptor states become negatively charged. Generally, a decrease in Q_{it} is produced. This situation is shown in Figure III.12(b).

If $V_{gate} < V_{FB}$ (represented in Figure III.12(c)), the bands are bended upwards and E_{Fs} is closer to the valence band. For that reason, some donor states lose one electron, becoming positively charged. In this case, an increase in Q_{it} occurs.

It is important to highlight that the variation of Q_{it} does not depend on the type of states that are above or below the Fermi level. When the applied voltage is higher than

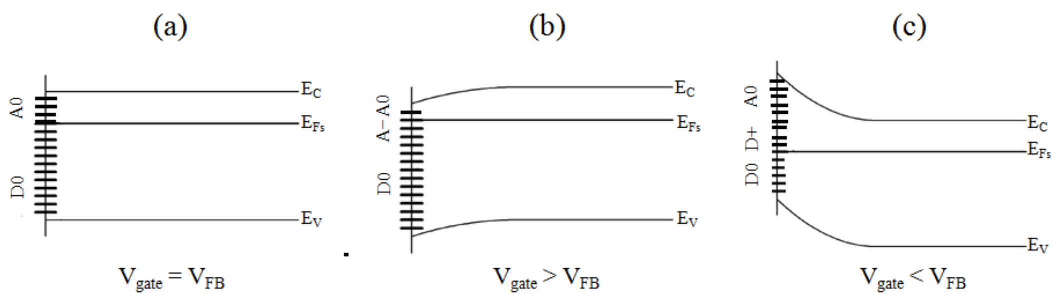

Figure III.12: Interface states charge changes depending on the applied voltage to the MIS structure. A0 and D0 are neutral acceptors and donors, A− are the negatively charged acceptor states and D+ are the positive charged donor states.

V_{FB}, either type of state will be occupied and Q_{it} will decrease. This means that either the neutral acceptor states become negative or the positive charged donor states become neutral. The reasoning is analogous in the $V_{gate} < V_{FB}$ case.

Since this Q_{it} is located in the semiconductor surface, it can be added to Q_s. Therefore, the total capacitance can be modeled as a C_{INS} in series with C_s and C_{it} in parallel.

The effect of D_{it} in the C-V_{gate} characteristics measured at high frequency is a stretch-out of the curves: due to the interfacial charge field screening, the C-V_{gate} curve stretches out to negative voltages for $V_{gate} < V_{FB}$ and to positives voltages for $V_{gate} > V_{FB}$. In Figure III.13 is presented this effect in the C-V_{gate} curve of a MIS device.

Besides, a high D_{it} value can produce the appearance of a hump in depletion. This hump is reduced (it can even disappear) when the measuring frequency increases, depending on the characteristic trap response: once charged, the traps can emit the charge in phase with the *ac* signal (contributing to the measured conductance) or out of phase (contributing to the capacitance, producing the hump in depletion).[44]

Along this thesis, a temperature annealing at 300-450 ºC in a forming gas atmosphere was performed to the samples in order to reduce the D_{it} value, as it was mentioned in the former chapter.

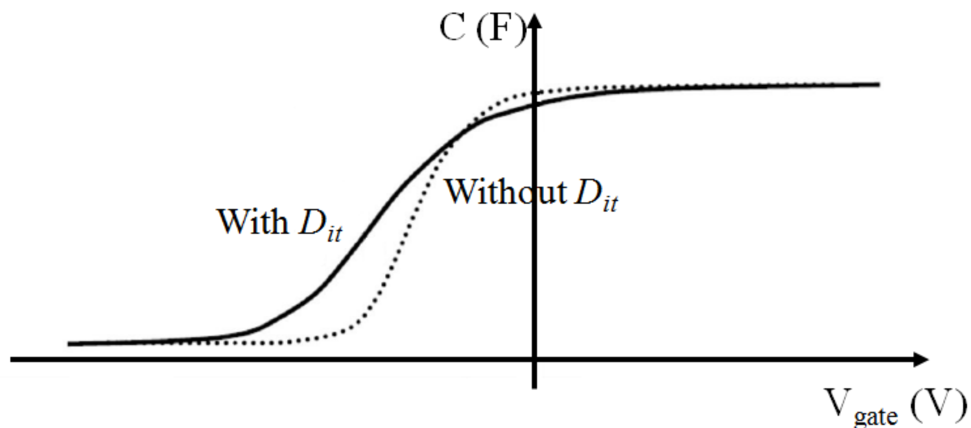

Figure III.13: Stretch-out of the C-V_{gate} curve as a consequence of the presence of a D_{it}.

2.2.C.- Effects of the oxide trapped charge in the C-V_{gate} characteristics

As it was mentioned before, the variation of trapped charge within the insulator is due to the fabrication process or to hot carriers (high energy carriers). Carriers with low energy are not able to surpass the energy barrier, and thus are not injected to the insulator. The injected carriers are electrons if the applied gate voltage is positive or holes in the opposite case.[39,45] Once injected, they can be captured by a trap. When the carriers are trapped inside the insulator, they produce a change in Q_{INS}. In agreement with former discussion, this trapped charge shifts V_{FB}. To empty these traps, a high voltage of the opposite polarity is needed. When the C-V_{gate} curves are measured from accumulation to inversion and back again, a hysteresis cycle is produced due to this electron charge trapping.

The oxide trapped charge, Q_{ot}, can be obtained using the following expression:[41]

$$Q_{ot} = -\Delta V_{FB} C_{INS} \qquad \textbf{(III.10)}$$

where ΔV_{FB} is the flatband voltage shift: the flatband voltage of the positive to negative curve minus the flatband voltage of the negative to positive curve. Therefore, the sign and absolute value of ΔV_{FB} determines the properties of the oxide traps.

2.3.- Interfacial state density (D_{it}) determination

Obtaining the value of this magnitude is very important to know the possibility of using the high κ materials in MOSFETs applications.

Two different methods were used during this thesis to determine the D_{it} value. In the following subsections these methods are explained.

2.3.A.- Conductance method

This method is considered to be the most sensitive to determine the D_{it}. It was proposed by Nicollian and Goetzberger.[46,47] It is also the most complete method because it obtains the D_{it} in the depletion and weak inversion polarizations, among other parameters. The conductance method determines the D_{it} by extracting this value from the conductance measured in depletion as a function of V_{gate} and the *ac* signal frequency, *f*.[39,41] The conductance represents the loss mechanism due to interface trap capture and emission of carriers.

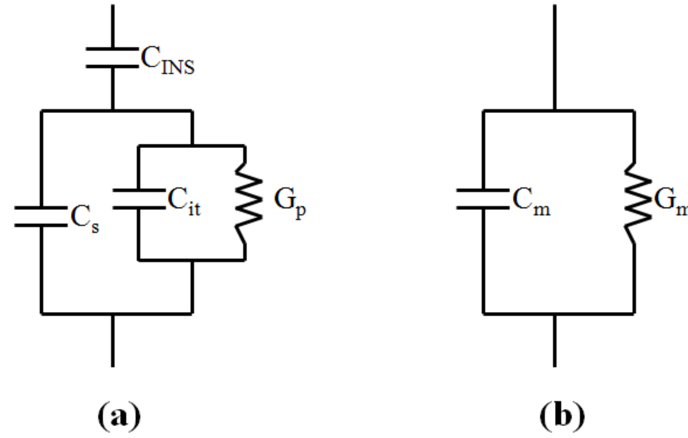

Figure III.14: (a) Small signal equivalent circuit of a MIS device for conductance measurements and (b) measured circuit.

The simplified equivalent circuit of a MIS device is shown in Figure III.14(a). Measuring the capacitance and the conductance, C_m and G_m (presented in Figure III.14(b)), the parallel conductance, G_p can be obtained by:

$$\frac{G_p}{\omega} = \frac{\omega {C_{INS}}^2 G_m}{{G_m}^2 + \omega^2 (C_{ins} - C_m)^2} \quad \textbf{(III.11)}$$

being $\omega = 2\pi f$.

The D_{it} can be determined using the following equation:

$$D_{it} = \frac{2.5}{q} \left[\frac{G_p}{\omega}\right]_{max} \quad \textbf{(III.12)}$$

where q is the electron charge.

W. A. Hill and C. C. Coleman[48] proposed a simplification where only the measurement of the curves at one frequency was enough for having a D_{it} estimation.

One parameter that is very important and has to be taken in consideration is the series resistance, R_s.[40] This parameter can cause a large distortion when measuring the C-V_{gate} curves. The strong accumulation polarizations are more affected by this parameter. Therefore, ignoring this resistance induces inaccuracies in the parallel conductance, because, according equation (III.11), this is determined from C_{INS}, which is the capacitance in accumulation. Thus, the D_{it} value can also be estimated with

inaccuracies. For this reason, it is important to obtain the R_s and correct the C_m and G_m magnitudes using the following equations:

$$R_s = \frac{G_{m,a}}{G_{m,a}^2 + \omega^2 C_{m,a}^2} \qquad \textbf{(III.13)}$$

$$C_{m,cor} = \frac{G_m^2 + \omega^2 C_m^2}{a^2 + \omega^2 C_m^2} C_m \qquad \textbf{(III.14)}$$

$$G_{m,cor} = \frac{G_m^2 + \omega^2 C_m^2}{a^2 + \omega^2 C_m^2} a \qquad \textbf{(III.15)}$$

where $a = G_m - R_s(G_m^2 + \omega^2 C_m^2)$, $G_{m,a}$ and $C_{m,a}$ are the measured conductance and capacitance in accumulation and $C_{m,corr}$ and $G_{m,cor}$, the corrected C_m and G_m, respectively.

2.3.B.- Deep level transient spectroscopy (DLTS)

DLTS is a technique normally used to analyze deep level defects but, in this case, it was used to evaluate the traps at the interface between the high κ dielectric and the semiconductor.

This technique was developed by C. T. Sah[49,50] and improved by D. V. Lang with the rate window concept.[51] This method consists in the combination of capacitance transient measurements with a temperature sweep. From these transients at different temperatures, the capacitance difference for two times (t_1 and t_2 that defined the rate window) can be expressed as follow:

$$\Delta C = C(t_1) - C(t_2) = \frac{C_0 n_T(0)}{2N_D}\left[exp\left(-\frac{t_2}{\tau_e}\right) - exp\left(-\frac{t_1}{\tau_e}\right)\right] \qquad \textbf{(III.16)}$$

being C_0 and $n_T(0)$, the capacitance and the trapped electron concentration at t = 0, N_D, the donor doping concentration and τ_e, the emission time constant.

It was demonstrated by N. M. Johnson and K. Yamasaki *et al.*[52,53] that for a MOS capacitors with $C_{it} = qD_{it} << C_{INS}$ and $\Delta C << C_{HF}$, the capacitance difference is:

$$\Delta C \approx -\frac{C_{HF}^3}{\kappa_S \varepsilon_0 N_D C_{INS}} ln\left(\frac{t_2}{t_1}\right) kTD_{it} \qquad \textbf{(III.17)}$$

where C_{HF} is the high frequency capacitance, κ_s, the semiconductor relative permittivity, k is the Boltzmann's constant (with a value of 8.617×10^{-5} eV/K) and T, the temperature.

Therefore, from this last equation, the D_{it} can be obtained, using DLTS, as:

$$D_{it} = -\frac{\kappa_S \varepsilon_0 N_D}{kTln(t_2/t_1)} \cdot \frac{C_{INS}}{{C_{HF}}^3} \cdot \Delta C \qquad \textbf{(III.18)}$$

These measurements and the analyses of the results were done in the *Grupo de caracterización de materiales y dispositivos electrónicos* of the *Departamento de Electricidad y Electrónica* of the *E.T.S.I de Telecomunicación* from *Universidad de Valladolid*. The sample is placed inside an *Oxford DM1710* cryostat, used to cool down the temperature from room temperature to 77 K. The measurements were carried with a *Boonton 72B* capacitance meter, an *HP54501* digital oscilloscope to record the capacitance transients and an *HP81104* pulse generator to apply the filling pulses.

2.4.- Leakage current density measurements

In an ideal MIS structure, the current that pass through the dielectric layer is zero. But, in practice, the insulators are not ideal and when gate voltage is applied, some current crosses through it.

The gate leakage current density, J, is a critical parameter for MOSFET operation. As it was commented in the introduction, the reason of studying high κ materials is the possibility to obtain thicker layers without reducing capacitance while minimizing the leakage current due to the tunneling effect.[54]

Different conduction mechanisms exist depending on the applied gate voltage and also the temperature.[55,56] The most common mechanisms are the tunneling effect conduction, which can be direct or indirect (also called Fowler-Nordheim),[57] the ohmic mechanism[58] and the Poole-Frenkel transport.[59] The tunneling effect mechanism is produced by carriers that cross the dielectric by quantum tunneling. Thus, it is especially relevant for high electric field oxide, F_{ox} (high V_{gate}), and also for thin insulator layers. This conduction mechanism is highly dependent on F_{ox} and temperature independent. The ohmic conduction appears at low F_{ox} and it is due to the thermally excited carriers present at localized states inside the insulator. Finally, the Poole-Frenkel conduction mechanism appears at moderate F_{ox} and it is related to electrons placed in traps inside the insulator, which can jump between traps by thermal excitation.

During this thesis, the J-V_{gate} measurements were carried out with a source measuring unit (SMU) from *Keithley* model *2636A*. This probe station was placed within

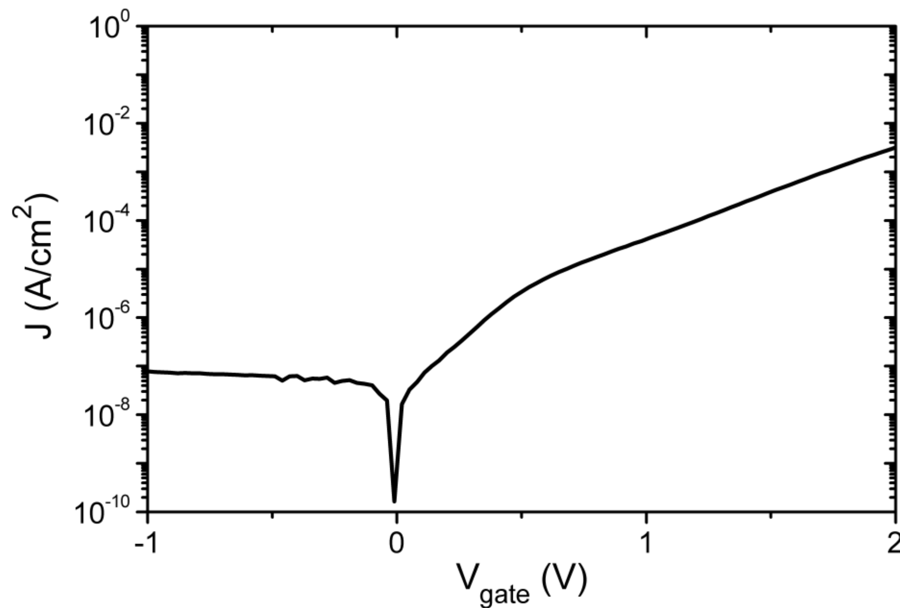

Figure III.15: J-V_{gate} characteristic of a MIS device measured from inversion (negative voltages) to accumulation (positive voltages).

a Faraday box. Besides, the J-V_{gate} curves obtained at variable temperatures were acquired with a *Keithley 6517A* programmable electrometer and using an *Oxford DM1710* cryostat. These last measurements were done in the *Grupo de caracterización de materiales y dispositivos electrónicos* of the *Universidad de Valladolid*.

The J-V_{gate} characteristics were typically measured in the accumulation region (for $V_{gate} > 0$ V) because this is the region where leakage is determined by the dielectric layer. In inversion and depletion polarizations, the depletion zone is present, limiting leakage. Figure III.15 presents a complete accumulation-depletion-inversion J-V_{gate} curve for a MIS device, where it can be observed that the inversion leakage current density (for negative voltages) is much lower than the current density in accumulation (positive V_{gate}).

REFERENCES

[1] B. C. Smith. "Fundamentals of Fourier Transform Infrared Spectroscopy". CRC Press. Boca Raton, Florida, 2011.

[2] M. Zacharias, D. DimovaMalinovska, M. Stutzmann. "*Properties of hydrogenated amorphous silicon suboxide alloys with visible room-temperature photoluminescence*". Philos. Mag. B. 73, 799 (1996).

[3] G. Lucovsky, J. Yang, S. S. Chao, J. E. Tyler, W. Czubatyj. "*Oxygen-bonding environments in glow-discharge-deposited amorphous silicon-hydrogen alloy films*". Phys. Rev. B 28, 3225 (1983).

[4] E. D. Palik. "Handbook of optical constant of solids". Academic Press. Orlando, Florida, 1985.

[5] H. Ibach, H. Lüth. "Solid state physics. An introduction to theory and experiment". Springer Verlag, Berlin, 1993.

[6] S. Perkowitz. "Optical Characterization of Semiconductors: Infrared, Raman and Photoluminescence Spectroscopy". Academic Press Limited. London, 1993.

[7] M. M. Frank, S. Sayan, S. Dörmann, T. J. Emge, L. S. Wielunckі, E. Garfunkel, Y. J. Chabal. "*Hafnium oxide gate dielectrics grown from an alkoxide precursor: structure and defects*". Mater. Sci. Eng. B 109, 6 (2004).

[8] C. N. Harward, R. R. Patty. "*Low-Resolution Determination of the Strength of the 667-cm^{-1} CO_2 Band*". J. Opt. Soc. Am. 58, 188 (1968).

[9] P. G. Pai, S. S. Chao, V. Takagi, G. Lucovsky. "*Infrared spectroscopic study of SiO_x films produced by plasma enhanced chemical vapor deposition*". J. Vac. Sci. Technol. A, 4, 689 (1986).

[10] R. A. B. Devine. "*Structural nature of the Si/SiO_2 interface through infrared spectroscopy*". Appl. Phys. Lett., 68, 3108 (1996).

[11] A. Hardy, C. Adelmann, S. Van Elshocht, H. Van den Rusl, M. K. Van Bael, S. De Gent, M. D'Olieslaeger, M. Heyns, J. A. Kittl, J. Mullens. "*Study of interfacial reactions and phase stabilization of mixed Sc, Dy, Hf high-k oxides by attenuated total reflectance infrared spectroscopy*". Appl. Surf. Sci., 255, 7812 (2009).

[12] A. García-Murillo, C. Le Luyer, C. Garapon, C. Dujardin, E. Bernstein, C. Pedrini, J. Mugnier. "*Optical properties of europium-doped Gd_2O_3 waveguiding thin films prepared by the sol-gel method*". Opt. Mat. 19, 161 (2002).

[13] G. Liu, G. Hong, D. Sun. "*Synthesis and characterization of SiO_2/Gd_2O_3:Eu core-shell luminescent materials*". J. Colloid Interface Sci. 278, 133 (2004).

[14] N. T. McDevitt, W. L. Baun. "*Infrared absorption study of metal oxides in the low frequency region (700-240 cm^{-1})*". Spectrochimica Acta, 20, 799 (1964).

[15] C. Jones, T. J. Leedham, H. O. Davies, K. A. Fleeting, P. O'Brien, M. J. Crosbie, P. J. Wright, D. J. Williams, P. A. Lane. "*Metal-organic chemical vapour deposition of lead scandium tantalate: chemical issues and precursor selection*". Polyhedron 19, 351 (2000).

[16] P. C. Feijoo, M. A. Pampillón, E. San Andrés, M. L. Lucía. "*Optimization of scandium oxide growth by high pressure sputtering on silicon*". Thin Solid Films, 526, 81 (2012).

[17] R. Doering, Y. Nishi. "Handbook of semiconductor manufacturing technology". CRC Press. Boca Raton, Florida, 2008.

[18] E. D. Specht, C. J. Sparks, C. J. McHargue. "*Determination of residual stress in Cr-implanted Al_2O_3 by glancing angle x-ray diffraction*". Appl. Phys. Lett., 60, 2216 (1992).

[19] B. E. Warren. "X-ray diffraction". Addison-Wesley. Reading, Massachusetts, 1969.

[20] M. P. Singh, C. S. Thakur, K. Shalini, S. Banerjee, N. Bhat, S. A. Shivashankar. "*Structural, optical and electrical characterization of gadolinium oxide films deposited by low-pressure metalorganic chemical vapor* deposition". J. Appl. Phys., 96, 5631 (2004).

[21] J. Olea, M. Toledano-Luque, D. Pastor, G. González-Díaz, I. Mártil. "*Titanium doped silicon layers with very high concentration*". J. Appl. Phys., 104, 016105 (2008).

[22] J. Olea, M. Toledano-Luque, D. Pastor, E. San-Andrés, I. Mártil, G. González-Díaz. "*High quality Ti-implanted Si layers above the Mott limit*". J. Appl. Phys., 107, 103524 (2010).

[23] D. D. Zhao, Z. Yang, E. S. W. Kong, C. L. Xu, Y. F. Zhang. "*Carbon nanotube arrays supported manganese oxide and its application in electrochemical capacitors*". J. Solid State Electrochem. 15, 1235 (2010).

[24] P. Jennings, Z. T. Jiang, N. M. W. Wyatt, D. Parlevliet, C. Creagh, C. Y. Yin, H. Widjaja, N. Mondinos. "*Characterization of silicon nanowires grown on silicon, stainless steel and indium tin oxide substrates*". Appl. Phys. A 3, 723 (2013).

[25] S. J. Schneider, J. L. Waring. "*Phase equilibrium relations in the* Sc_2O_3-Ga_2O_3 *system*". J. Res. Natl. Stand. Sec. A, 67A, 19 (1963).

[26] M. Yasaka. "*X-ray thin-film measurements techniques*". The Rigaku Journal, 26, 1 (2010).

[27] L. G. Parratt. "*Surface studies of solids by total reflection of X-rays*". Phys. Rev. 95, 359 (1954).

[28] S. Wolf. "Microchip manufacturing". Lattice Press. Sunset Beach, California, 2004.

[29] R Jenkins, R. W. Gould, D. Gedke. "Quantitative x ray spectrometry". Marcel Dekker, New York, 1997.

[30] S. T. Jackson, R. G Nuzzo. "*Determining hybridization differences for amorphous carbon from the XPS C 1s envelope*". Appl. Surf. Sci., 90, 195 (1995).

[31] P. Mérel, M. Tabbal, M. Chaker, S. Moisa, J. Margot. "*Direct evaluation of the* sp^3 *content in diamond-like-carbon films by XPS*". Appl. Surf. Sci., 136, 105 (1998).

[32] G. Hollinger, Y. Jugnet, P. Pertosa, T. M. Duc. "*X-ray photoelectron spectroscopy of thermally grown silicon dioxide films on silicon*". Chem. Phys. Lett., 36, 441 (1975).

[33] Y. Uwamino, Y. Ishizuka, H. Yamatera. "*X-ray photoelectron spectroscopy of rare-earth compounds*". J. Electron Spectrosc. Relat. Phenom., 34, 67 (1984).

[34] A. D. Hamer, D. G. Tisley, R. A. Walton. "*The X-ray photoelectron spectra of inorganic molecules-VIII[1,2]: Compounds of scandium(III), scandium (III) oxide and complexes with organic oxygen donor molecules*". J. Inorg. Nucl. Chem., 36, 1771 (1974).

[35] P. Raghy, N. Rana, C. Yim, E. Shero, F. Shadman. "*Adsorption of moisture and organic contamintants on hafnium oxide, zirconium oxide and silicon oxide gate dielectrics*". J. Electrochem. Soc., 150, F186 (2003).

[36] D. B. Williams, C. B. Carter. "Transmission electron microscopy". Plenum Press, New York, 1996.

[37] J. Mayer, L. A. Giannuzzi, T. Kamino, J. Michael. "*TEM sample preparation and FIB-induced damage*". MRS Bull., 32, 400 (2007).

[38] M. Toledano-Luque. "*Growth and characterization of high-k dielectrics for field effect devices*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2008).

[39] E. H. Nicollian, J. R. Brews. "MOS (Metal Oxide Semiconductor): Physics and Technology". John Wiley & Sons. New York, 1982.

[40] S. M. Sze. "Semiconductor devices: Physics and Technology". John Wiley & Sons. Singapore, 1985.

[41] D. K. Schroder. "Semiconductor material and device characterization". John Wiley & Sons. New York, 1990.

[42] R. M. Warner Jr., B. L. Grung. "Transistors: fundamentals for the integrated-circuit engineer". John Wiley & Sons. New York, 1983.

[43] E. San Andrés, L. Pantisano, J. Ramos, P. J. Roussel, B. J. O'Sullivan, M. Toledano-Luque, S. De Gendt, G. Groeseneken. "*Accurate gate impedance determination on ultraleaky MOSFETs by fitting to a three-lumped-parameter model at frequencies from DC to RF*". IEEE. Trans. Elect. Dev. 54, 1705 (2007).

[44] E. M. Vogel, G. A. Brown. "*Challenges of electrical measurements of advanced gate dielectrics in metal-oxide-semiconductor devices*". Characterization and Metrology of VLSI Technology: International Conference, 771 (2003).

[45] B. E. Deal, P. J. Fleming, P. L. Castro. "*Electrical properties of vapor-deposited silicon nitride and silicon oxide films on silicon*". J. Electrochem. Soc., 115, 300 (1968).

[46] E. H. Nicollian, A. Goetzberger. "*MOS conductance technique for measuring surface state parameters*". Appl. Phys. Lett., 7, 216 (1965).

[47] E. H. Nicollian, A. Goetzberger. "*The Si-SiO$_2$ interface – electrical properties as determined by the metal-insulator-silicon conductance technique*". Bell Syst. Tech. J., 46, 1055 (1967).

[48] W. A. Hill, C. C. Coleman. "*A single-frequency approximation for interface-state density determination*". Solid-State Electron., 23, 987 (1980).

[49] C. T. Sah, L. Forbes, L. L. Rosier, A. F. Tasch Jr. "*Thermal and optical emission and capture rates and cross sections of electrons and holes at imperfection centers in semiconductor from photo and dark junction current and capacitance experiments*". Solid-State Electron., 13, 759 (1970).

[50] C. T. Sah. "*Bulk and interface imperfections in semiconductors*". Solid-State Electron., 19, 975 (1976).

[51] D. V. Lang. "*Deep level transient spectroscopy: A new method to characterize traps in semiconductors*". J. Appl. Phys., 45, 3023 (1974).

[52] N. M. Johnson. "*Measurement of semiconductor-insulator interface states by constant-capacitance, deep level transient spectroscopy*". J. Vac. Sci. Technol., 21, 303 (1982).

[53] K. Yamasaki, M. Yoshida, T. Sugano. "*Deep level transient spectroscopy of bulk traps and interface states in Si MOS diodes*". Jnp. J. Appl. Phys., 18, 113 (1979).

[54] International Technology Roadmap for Semiconductor (ITRS). http://www.itrs2.net/.

[55] F. C. Chiu. "*A review on conduction mechanisms in dielectric films*". Advances in Materials Science and Engineering, 2014, 578168 (2014).

[56] A Gómez Bravo. "*Caracterización de dieléctricos de alta permitividad para su aplicación en tecnologías nanométricas*". Ph. D. dissertation, Universidad de Valladolid, Valladolid (2015).

[57] M. Depas, B. Vermeire, P. W. Mertens, R. L. Van Meirhaeghe, M. M. Heyns. "*Determination of tunneling parameters in ultra-thin oxide layer poly-Si/SiO_2/Si structures*". Solid-State Electron., 38, 1465 (1995).

[58] D. G. Park, M. Tao, E. Botchkarev, Z. Fan, Z. Wang, S. N. Mohammad, A. R. Heyd, S. A. Alterovitz. "*Gate quality Si_3N_4 prepared by low temperature remote plasma enhanced chemical vapor deposition for III-V semiconductor-based metal-insulator-semiconductor devices*". J. Vac. Sci. Technol. B, 14, 2674 (1996).

[59] J. Frenkel. "*On pre-breakdown phenomena in insulators and electronic semiconductors*". Physical Review, 54, 647 (1938).

Chapter IV:

Thermal oxidation of Gd_2O_3

A straightforward method to deposit gadolinium oxide is reactive sputtering from a metallic Gd target using a mixed Ar/O_2 atmosphere.1 The drawback of this approach is that the highly reactive excited oxygen molecules presented in the plasma can oxidize the substrate during the first stages of dielectric growth.2 This may impose a lower limit on the lowest EOT achievable, restricting device scaling. In order to explore processing alternatives to this conventional approach, another Gd_2O_3 growth route aiming to the minimization of interface regrowth is presented in this chapter. This approach is inspired on previous works by Hayashi and Yamamoto *et al.* that studied several Hf oxidation routes.3-5

Therefore, in this chapter, metallic gadolinium layers were deposited by HPS in a pure Ar atmosphere. Subsequently, without extracting the sample from the chamber, the system was filled with O_2 up to atmospheric pressure and an *in situ* thermal oxidation was performed at temperatures ranging from 150 to 750 ºC. The goal was to determine if there is an oxidation temperature high enough to fully oxidize the Gd layer but without affecting the underlying Si substrate (in other words, without the regrowth of the interfacial SiO_x).

First, plasma conditions (pressure and radiofrequency (*rf*) power) were studied with the aim of obtaining the optimal Gd sputtering parameters by means of GDOS. Then, the films were structurally characterized by GIXRD, XRR, FTIR and TEM. The electrical study was carried out by the fabrication of MIS devices with Al as gate electrode.

IV.1.- EXPERIMENTAL METHOD

After the metallic Gd thin film sputtered (with deposition time from 90 s to 30 min) at room temperature and without exposing the sample to the atmosphere, all pumping ports were closed, leaving the chamber sealed. Then, the chamber was immediately filled with high purity O_2 up to a pressure of 1 bar, and the substrate holder temperature was ramped at 50 ºC/min up to the oxidation temperature (temperatures between 250 and 750 ºC were studied). This temperature was kept for 60 min. Then the substrates were cooled down to room temperature and subsequently removed from the chamber. The maximum temperature of 750 ºC was chosen with the aid of Technology Computer Aided Design (TCAD) simulations which implement the Massoud oxidation model.6 These simulations are presented in Figure IV.1 and show that annealing bare-Si up to 650 ºC in O_2 atmosphere did not cause any significant SiO_x regrowth. Also, oxidation at 750 ºC only caused around 1 nm increase in thickness. In any case, these simulations were only used as a first crude approach for selecting the temperature range, since it is not known beforehand whether covering Si with metallic Gd inhibits or catalyzes SiO_x regrowth.

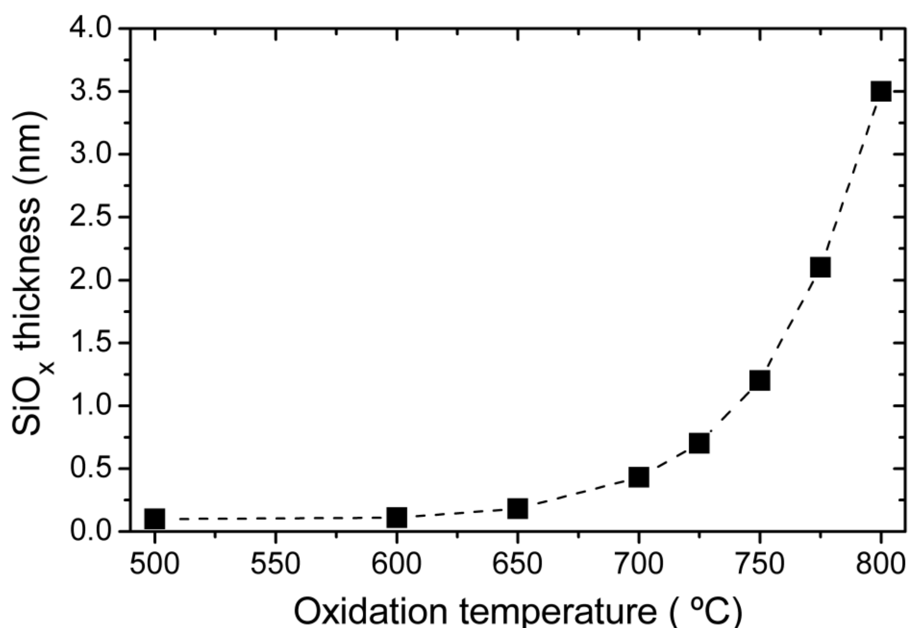

Figure IV.1: Simulation of the SiO_x thickness regrowth as a function of the oxidation temperature for bare-Si substrate implementing the Massoud oxidation model.

IV.2.- RESULTS AND DISCUSSION

2.1. Plasma characterization of metallic Gd sputtered in Ar

The first objective was to select the optimal metallic Gd sputtering conditions by means of studying the GDOS spectrum of the plasma. It was measured with the monocromator system and between 280 and 520 nm, because in that range there are the most relevant peaks. To decide the optimal working *rf* power, it was varied between 10 and 30 W while setting the pressure at 0.50 mbar. The results are shown in Figure IV.2(a). As expected, it is observed that increasing the power results in enhanced plasma activity. Also, no features related to H_2O (typically a broad band between 310 and 320 nm),[7] nor N_2 peaks (the main peaks located at 336 and 358 nm)7 are observed, as it was pointed out in chapter II. This indicates that the chamber was correctly sealed, which is critical in order to ensure that no oxidation occurs during the Gd pulverization. The 10 W spectrum shows only neutral Ar peaks (Ar I) between 400 and 450 nm8[,9] with a low intensity. This signifies that at this low power there are no ionized species, which are needed for the sputtering to take place.[10] Increasing the power to 20 W, increments the Ar I intensity, and also many peaks make apparition: ionized Ar (Ar II) is found in the 450-500 nm range,[8] some Gd I peaks (the most intense one located at 422.5 nm)[11] and also many Gd II emission lines (in the 290-390 nm range).[11] The effect of further increasing the power to 30 W is a rise on peak intensities, more relevant for the Gd II case, but no new peaks appear. Thus, it was selected 30 W as working *rf* power, in order to avoid being close to the extraction threshold power (which lay between 10 and 20 W, as it was found) and also to ensure a high deposition rate.

In order to determine the optimal working pressure, the plasma emission was measured at pressures of 0.25, 0.50, 0.75 and 1.0 mbar, and the obtained spectra are shown in Figure IV.2(b). The highest measured pressure of 1.0 mbar was fixed because for pressures above this value, plasma instabilities are produced, which could promote a lack of reproducibility in the sample fabrication. From the Figure IV.2(b) it is clear that at a pressure of 0.25 mbar, the plasma does not present Ar II, thus there is no Gd extraction. For higher pressures there is Gd extraction, so any value in this range could be reasonable. It was decided to focus on the lowest pressure that shows Gd extraction, since lower pressures produce less confined plasma and therefore, higher deposition

rate. Besides the Gd *versus* Ar intensity ratio is higher for a pressure of 0.50 mbar, which indicates a more efficient extraction. Thus this pressure, 0.50 mbar, was chosen as the working pressure.

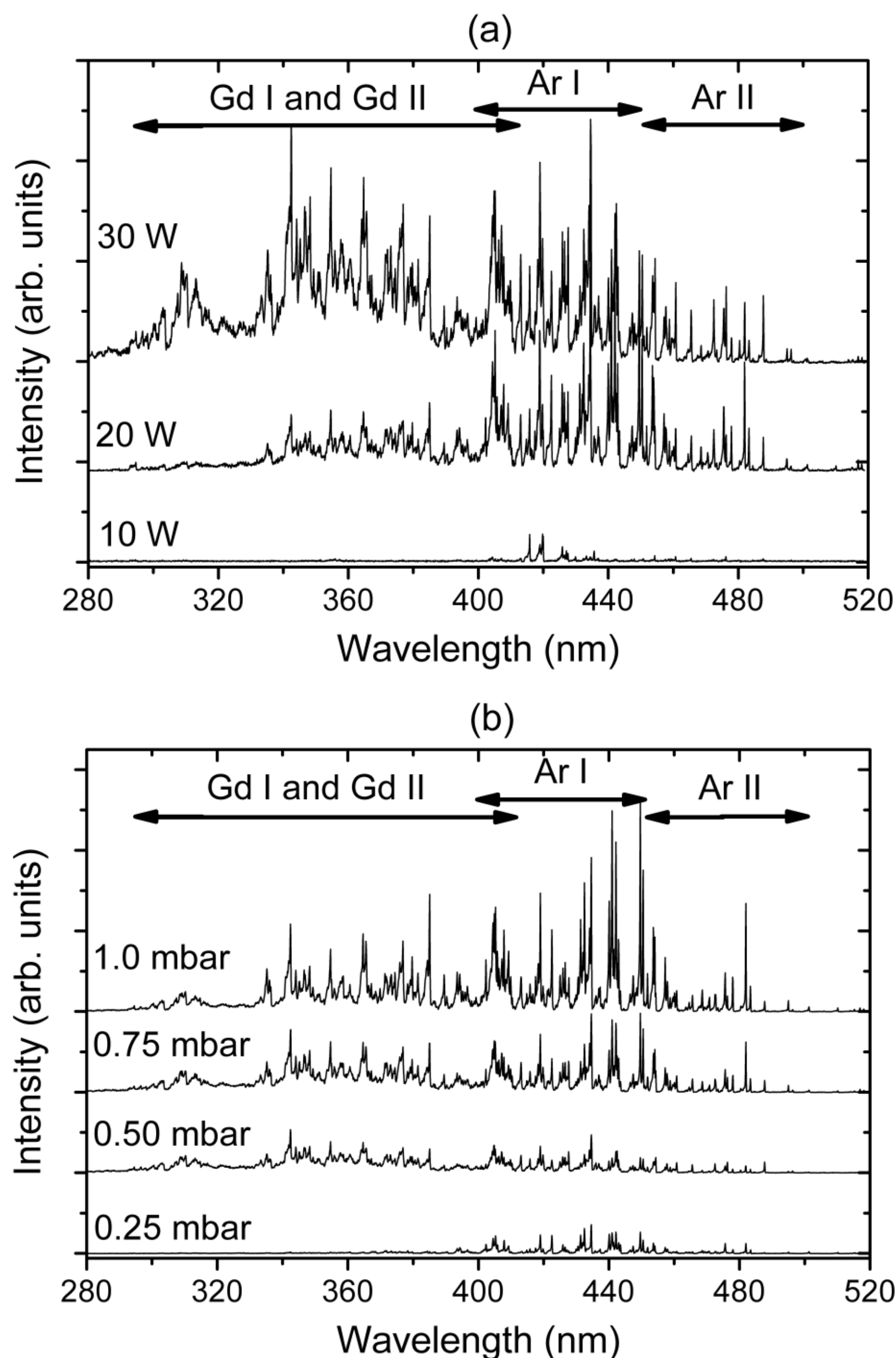

Figure IV.2: Optical emission spectra of metallic Gd sputtered in an Ar plasma at room temperature with (a) *rf* power variation (from 10 to 30 W) and (b) an Ar pressure dependence (0.25-1.0 mbar). The ranges with the most important lines for Ar I, Ar II, Gd I and Gd II are indicated in the figure.

2.2. Physical characterization of the thermally oxidized GdO_x films

Once the metallic deposition conditions were fixed, the Gd films were thermally oxidized inside the chamber. As a fast screening procedure, the oxidation degree of the metallic films was studied by 4-point sheet resistance measurements,[12] in order to obtain the onset oxidation temperature. It was performed consecutive annealing treatments at increasing temperature, and it was found that under 350 ºC, the sheet resistance was finite with an ohmic behavior. On the other hand, for higher temperatures, the resistance was too large to be measured. This was a first indication that full oxidation was not achieved for temperatures under 350 ºC.

Thick Gd films (around 200 nm) were deposited and oxidized at temperatures between 250 and 750 ºC in order to study the crystalline structure of the thermally oxidized GdO_x films. Thick layers were used in order to obtain intense diffraction peaks. The GIXRD diffraction patterns of the as-deposited metallic Gd sample and of the oxidized films at different temperatures are shown in Figure IV.3.

As-deposited metallic Gd film (Figure IV.3(a)) has the expected hexagonal structure (dashed lines in Figure IV.3), with the main diffraction peaks for planes (100) at 28.3º and (101) at 32.3º.[13] Besides, other peaks with lower intensity (42.2º and 50.1º related to the hexagonal Gd structure) can also be observed in Figure IV.3. For an oxidation temperature of 250 ºC, there are still traces of hexagonal Gd peak located at 32.3º (Figure IV.3(b)). This residual metallic peak disappears for higher temperatures as it can be seen in Figure IV.3(c)-(f). Also, after oxidation at low temperature many peaks make apparition. The most intense peak is located at 29.3º, and its height is directly correlated to another peak at 26.1º. These are the main diffractions of the monoclinic structure of Gd_2O_3.[14] As it is shown, most peaks can be directly related to this crystalline structure (solid lines in Figure IV.3). After oxidation at 350 ºC, metallic Gd peaks disappear and the only phase presented is monoclinic Gd_2O_3, as it is shown in Figure IV.3(c). At 500 ºC and above, two more peaks appear located at 20.1º and 28.6º (Figure IV.3(d)-(f)). The intensity of these peaks is 2 to 3 times lower and they are the most intense peaks of the cubic Gd_2O_3 structure.[14] Their associated diffraction angles are marked with dotted lines in Figure IV.3.

These results confirm the resistivity measurements commented before that pointed to a minimum oxidation temperature of 350 ºC to achieve a complete oxidation. Also, it can be concluded that oxidation at low temperature produces a polycrystalline monoclinic Gd_2O_3. On the other hand, oxidation at temperatures above 500 ºC yields a monoclinic-cubic phase mixture, but the monoclinic phase dominates. This behavior is contrary to thermodynamic studies and the results of other groups,[14,15] which found the opposite trend: the cubic phase was favored at low temperature, while annealing at higher temperatures promoted the transition to the monoclinic phase. It is noteworthy that the reported κ value of the monoclinic phase is significantly lower than the cubic phase, so if the device processing requires high temperatures this anomalous behavior might be useful. Also, in Figure IV.3 there are some peaks that were not identified.

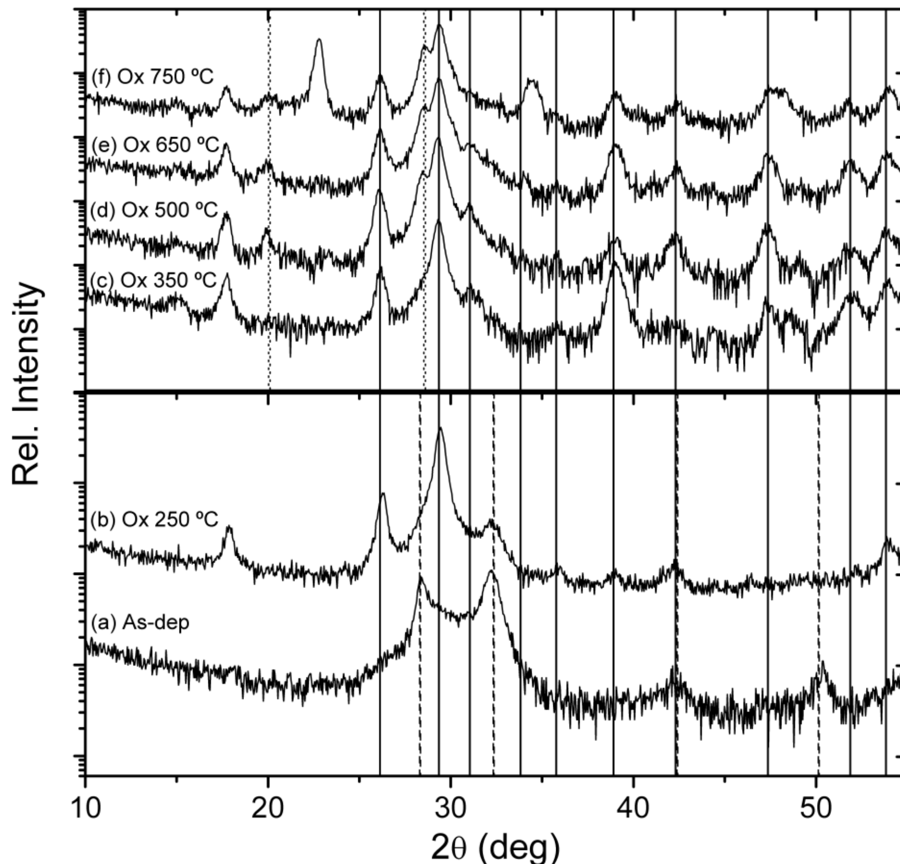

Figure IV.3: Grazing incidence X-ray diffraction patterns of thick Gd layers (a) as-deposited and (b)-(f) oxidized at several temperatures (from 250 to 750 ºC). The observed diffraction peaks have been identified as hexagonal metallic gadolinium (dashed lines), monoclinic gadolinium oxide (solid lines) or cubic gadolinium oxide (dotted lines).

They could not be related to Gd_2O_3, to Si or to a mixture of them according to the bibliography found.

In order to check if these conclusions can be extended to thin films, ~15 nm-thick films were also studied by GIXRD. The results are shown in Figure IV.4. As expected, the measurements are much noisier and the strongest observed diffraction is the most intense monoclinic Gd_2O_3 (111) peak at 29.3º. However, in these thin films there are not clear traces of the cubic Gd_2O_3 structure for temperatures above 500 ºC (Figure IV.4(b)-(d)), as it was observed for the thicker films (shown in Figure IV.3). This could be explained due to the low diffraction patterns observed for the cubic structure in the thicker films, thus, those peaks would be less clear for the thinner samples. In both cases, the monoclinic Gd_2O_3 structure is predominant. Besides, since the surface of these films is closer to the Si substrate, the GIXRD would show silicate diffraction peaks if there were gadolinium silicate formation close to the interface. Since the only diffractions found are related to the monoclinic structure of Gd_2O_3, it can be concluded that even at high oxidation temperatures of 750 ºC there is no relevant silicate formation.

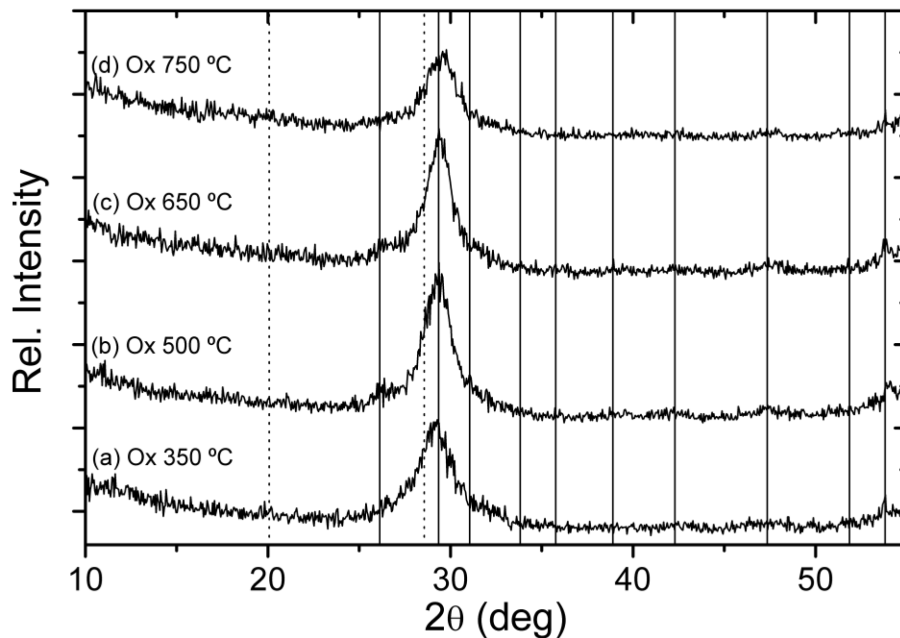

Figure IV.4: (a)-(d) GIXRD patterns of thin Gd films oxidized at several temperatures (from 350 to 750 ºC). The observed diffraction peaks have been identified as monoclinic gadolinium oxide (solid lines). The cubic gadolinium oxide is also shown (dotted lines).

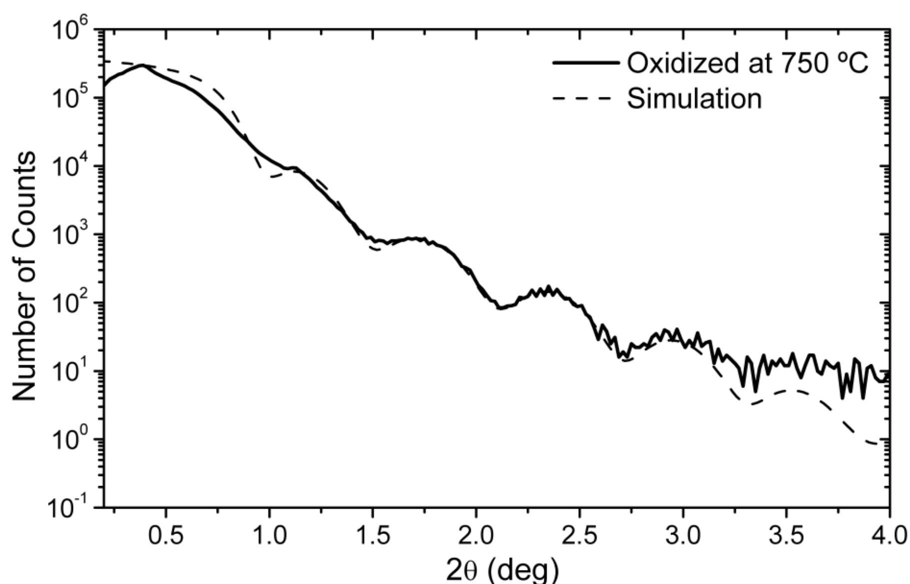

Figure IV.5: X-ray reflection measurements of the Gd film oxidized at 750 ºC (solid line), and fit to a $Gd_2O_3/SiO_2/Si$ model (dashed line).

With the aim of obtaining the thickness of the Gd_2O_3 layers, XRR measurements were also performed. The results were fitted with a segmented algorithm to a $Gd_2O_3/SiO_2/Si$ bilayer model, using density, thickness and roughness as parameters.[16] As an example, Figure IV.5 shows the measurements for the film oxidized at 750 ºC and the fitting results. There is an excellent agreement between measurements and simulation, as it can be seen in this figure.

The thickness values obtained from the fitting are shown in Figure IV.6. The uncertainty of these values can be estimated as ± 1.0 nm. This absolute uncertainty is relatively small compared to the Gd_2O_3 thickness. It can be observed that there is a thickness increase when annealing above 350 ºC (the temperature where the cubic phase appears). For temperatures above 500 ºC (cubic + monoclinic phase), there are no relevant changes on Gd_2O_3 thickness, with a mean value of 13.6 nm. On the other hand, the relatively uncertainty on SiO_2 thickness is too high to obtain accurate quantitative information. The only trend that is clear is that above 350 ºC, there is an increase of the interfacial SiO_2 thickness.

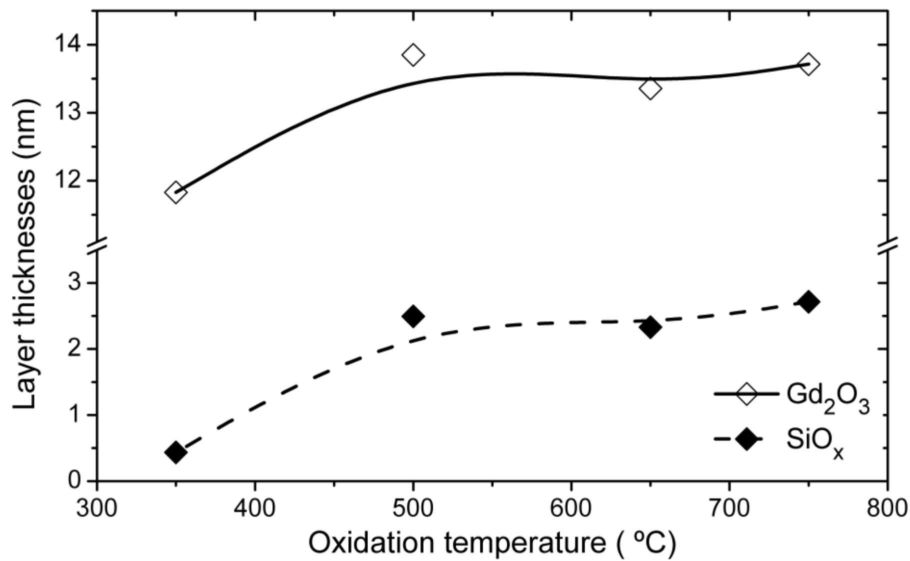

Figure IV.6: Thickness result of the XRR simulations to a $Gd_2O_3/SiO_2/Si$ bilayer model: Gd_2O_3 thickness (open symbols) and SiO_2 thickness (closed symbols). The uncertainty of these values can be estimated as ± 1.0 nm.

Since one of the goals of this work is trying to minimize SiO_2 regrowth, the transmission FTIR spectroscopy is used as a fast and more reliable technique than XRR to study the SiO_2 presence on the samples. Figure IV.7 shows the absorbance in the 1200-900 cm^{-1} range. The feature observed at around 1060 cm^{-1}, which shows a clear increase in absorption with increasing oxidation temperature, is due to the SiO_x that is usually present at the high κ/Si interface. Unstressed thermal SiO_2 has its most intense stretching absorption at around 1075 cm^{-1}.[17,18] Besides, in Si-rich SiO_x this absorption shifts towards lower wavenumbers with increasing Si content.[17] In these oxidized Gd samples, it can be observed that at an oxidation temperature of 350 ºC there is a peak downwards, at 500 ºC there is no peak and at higher temperatures the peak grows in intensity (at 750 ºC the peak is located at 1065 cm^{-1} and its intensity is comparable to the intensity presented by a RCA cleaned substrate, which is covered by a 1-2 nm thick SiO_2 layer).[17] The interpretation is quite straightforward: at 350 ºC there is even less interfacial SiO_x than native SiO_2 on the surface of the HF cleaned substrate (during the reference substrate measurement the native oxide regrowth is unavoidable). For higher temperatures, the thickness of the interfacial layer grows but it is difficult to quantify

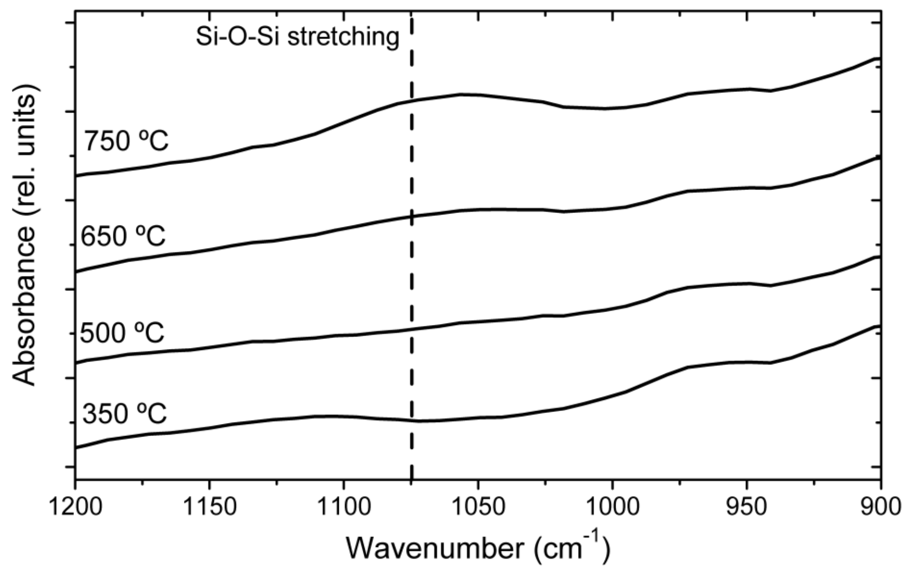

Figure IV.7: FTIR spectra of thin Gd layers oxidized at several temperatures (from 350 to 750 ºC). The wavenumber of thermal SiO_2 stretching is marked by the dashed line.

numerically this regrowth. The shift of the peak to lower wavenumbers suggests a Si-rich SiO_x interlayer formation that grows with the oxidation temperature.

2.3. Electrical characterization of MIS devices with thermally oxidized Gd_2O_3

For the electrical measurements, MIS devices were fabricated with ~15 nm of Gd_2O_3 and using ~70 nm of Al for the top and bottom contacts. These samples did not have field oxide (FOX). Due to the use of thick Gd_2O_3 films, the absence of this FOX should not represent any problem for the electrical characterization.

The electrical results of the MIS devices are shown in Figure IV.8, where it is presented representative normalized capacitance, C, and leakage current density, J, as a function of gate voltage, V_{gate}, characteristics for three oxidation temperatures (500, 650 and 750 ºC) and after the FGA at 300 and 450 ºC for 20 min. The samples oxidized at 350 ºC presented very poor electrical characteristics due to high gate leakage and are not shown. The devices were measured at 10 and 100 kHz to avoid capacitance decrease (due to the coupled effect of conductance and series resistance).[19] No relevant

differences were found, therefore here it is only shown the 10 kHz curves. The spread in accumulation capacitance within each sample was about 5-10%.

In Figure IV.8(a) it can be seen that the maximum accumulation capacitance increases ~50% when the oxidation temperature increases from 500 to 650 ºC, but higher temperatures do not increase the capacitance (in fact, there is a slight capacitance decrease). This is an indication that further increasing oxidation temperature is not a good path to improve device characteristics. Also for FGA at 450 ºC the C-V_{gate} curves are free of humps in the depletion region, which is characteristic of a low density of interface states. This is not the case when the FGA is performed at 300 ºC. For that temperature, the curves are displaced towards positive voltages, and also show a hump in the depletion region, due to interface defects. This last fact indicates that performing a FGA at temperature above 300 ºC is mandatory to improve the devices performance.

The EOT of the devices was obtained from the fit of the C-V_{gate} FGA at 450 ºC with the CVC algorithm,[20] and the results are summarized on table IV.1. The fit of the samples with FGA at 300 ºC is less reliable due to the big D_{it} hump, but the resulting values are the same within ± 0.5 nm, which shows that FGA temperature does not affect SiO_x regrowth or Gd_2O_3 permittivity. From these EOTs and using the XRR thicknesses for Gd_2O_3 and SiO_2 at each temperature, the permittivity of the Gd_2O_3 film can be calculated with a two capacitors in series model. As it is also presented in Table IV.1, the maximum κ_{GdO} value of ~7.4 is obtained at oxidation temperatures above 650 ºC. Unfortunately, this value is way too low for high performance applications. The origin of this extremely low permittivity will be studied by TEM.

Oxidation temperature (ºC)	EOT (nm)	κ_{GdO} (XRR thickness)	κ_{GdO} (TEM thickness)
500	14.4	4.5	4.8
600	9.8	7.0	7.4
750	10.0	7.4	7.3

Table IV.1: EOT values extracted from electrical measurements after FGA at 450 ºC and κ_{GdO} obtained from XRR and TEM thicknesses.

Concerning the gate leakage, it is clear that the oxidation at higher temperatures reduces leakage current by several orders of magnitude, as Figure IV.8(b) shows.

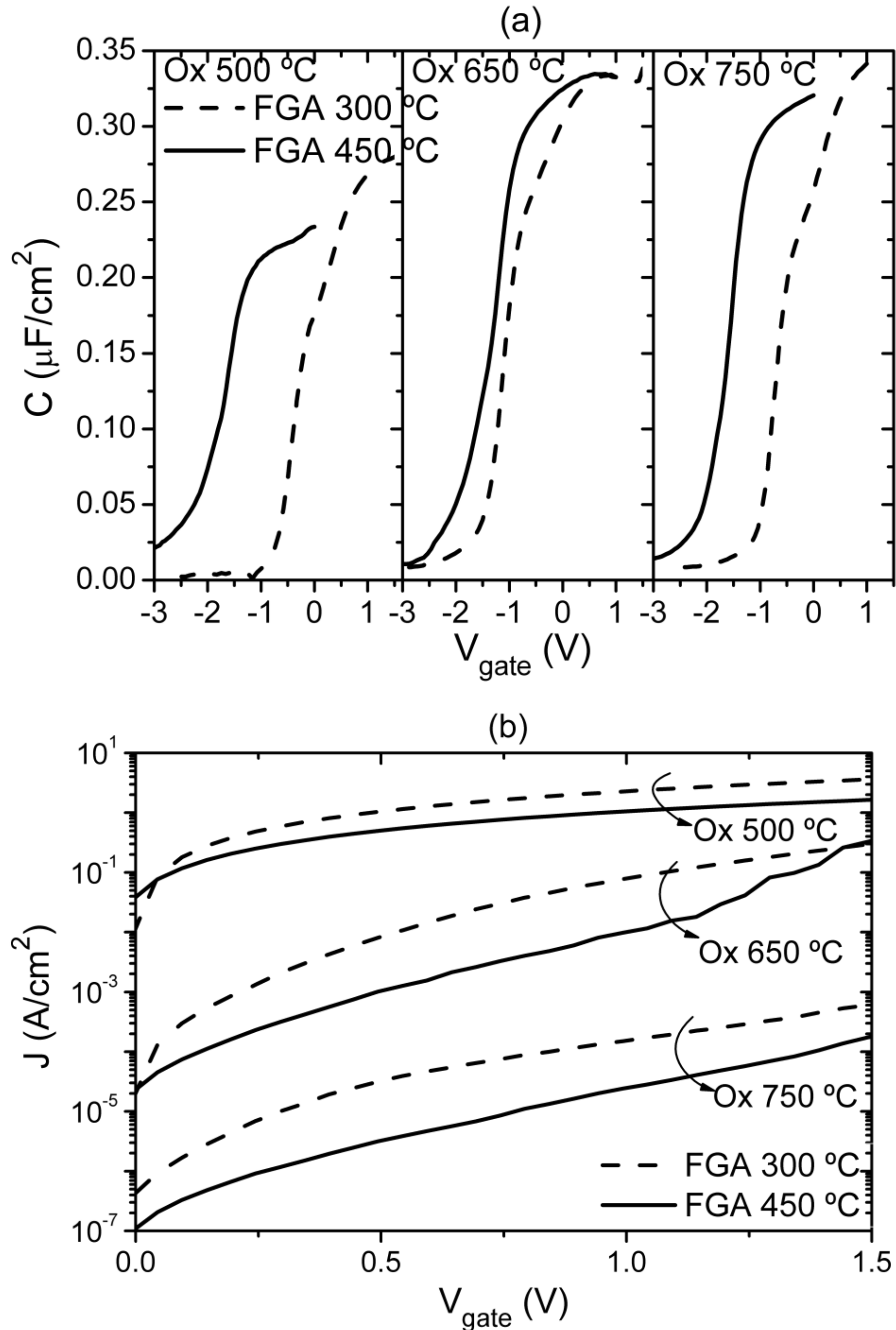

Figure IV.8: (a) Representative normalized capacitance curves as function of gate voltage of the $Al/Gd_2O_3/SiO_2/Si$ devices measured at 10 kHz for different oxidation temperatures (500-750 ºC) and FGA temperatures (300 ºC (with dashed lines) and 450 ºC (solid lines)). (b) Gate current density as a function of gate voltage for the same samples.

Besides, FGA at 450 ºC also reduces leakage by an order of magnitude as compared to FGA at 300 ºC. This reduction can be attributed to an improvement of the quality of the Gd_2O_3 layer, probably due to grain size growth and to the densification/relaxation/defect passivation of the SiO_x interfacial layer.

Another improvement that happens with oxidation temperature is also evident when extracting the D_{it} from the electrical measurements by the conductance method.[21] The results for 10 kHz are presented in Figure IV.9, both for FGA at 300 and 450 ºC. There it can be seen that a FGA at 300 ºC is ineffective in passivating interface defects, with D_{it} values above 10^{12} $eV^{-1}cm^{-2}$ for all the oxidation temperatures. On the other hand, by annealing at 450 ºC, the interface presents a very low trap density for the highest oxidation temperature (~4×10^{10} $eV^{-1}cm^{-2}$), comparable to thermal SiO_2.

2.4. TEM analysis of MIS devices

The main drawback that it has been found is the very low permittivity value obtained for these thermal oxidized samples. The origin of this low permittivity could be extrinsic (a measuring problem, such a miscalculation of the thicknesses obtained from XRR) or intrinsic (silicate formation or low permittivity of the dominant monoclinic phase). In order to clarify this question, cross-sectional TEM samples of the

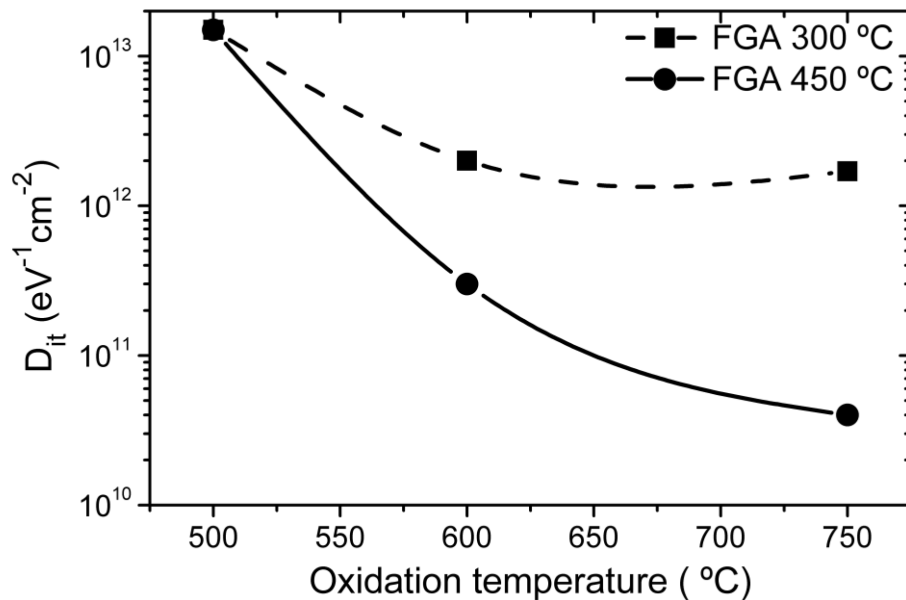

Figure IV.9: D_{it} values as a function of different oxidation temperatures for FGA at 300 ºC (square symbols) and FGA at 450 ºC (circle symbols).

films oxidized at 500 and 750 ºC were prepared. The results for theses samples are shown in Figure IV.10 before the FGA.

In Figure IV.10(a) and (c) it can be seen that the thicknesses calculated from XRR are very close to the actual thicknesses, since for oxidation at 750 ºC, the Gd_2O_3 film is 15.2 ± 0.2 nm thick, and the SiO_x interface is 1.6 ± 0.1 nm (for 500 ºC the thicknesses are 15.0 ± 0.2 nm and 1.4 ± 0.1 nm, respectively). If the Gd_2O_3 permittivity is calculated using these thicknesses, very similar values are found (they are also represented in Table IV.1). Besides, a thin film of around 2 nm is observed between the Gd_2O_3 and the Al top contact pointing to a formation of an aluminate due to a temperature reaction during the Al e-beam evaporation. But the small thickness of this film suggests that this is not the responsible of the low permittivity Gd_2O_3 value obtained.

However, there are other regions on the surface where the film presents "bumps" (Figure IV.10(b) and (d) show the same devices for both analyzed temperatures with less magnification). Also, the TEM images of these bumps suggest a "dome" (or igloo) structure. In other words, there seems to be a less dense space between the Gd_2O_3 and the Si. The origin of these bumps is unclear: they might be due to Si-Gd intermixing (in other words, the formation of gadolinium silicate), but the flatness of the Si surface and the previous GIXRD results rule out this possibility. Furthermore, no significant differences in EOT were found for the two FGA temperatures studied, so a thermally activated reaction can be discarded. On reference,[22] Mólnar *et al.* found that when annealing Gd on Si, even at low temperatures (320 ºC), due to the Gibbs free energy of the system, an "explosive" reaction between Si and Gd happened, starting on the weak SiO_2 spots. At these spots, gadolinium silicide flakes made apparition with a fractal structure. On these samples a similar effect might be the origin of the bumps: during oxidation, first the chamber is filled with O_2 and then there is a temperature increase. The oxygen comes to the film from the top Gd surface, while heat flows from the Si substrate so, in the first stages of the oxidation, some explosive Gd-Si flakes could be produced at the Si interface that, afterwards, become oxidized and give rise to the bumps. Another possibility is that it is a stress or adhesion problem during the warm up or cool down processes.

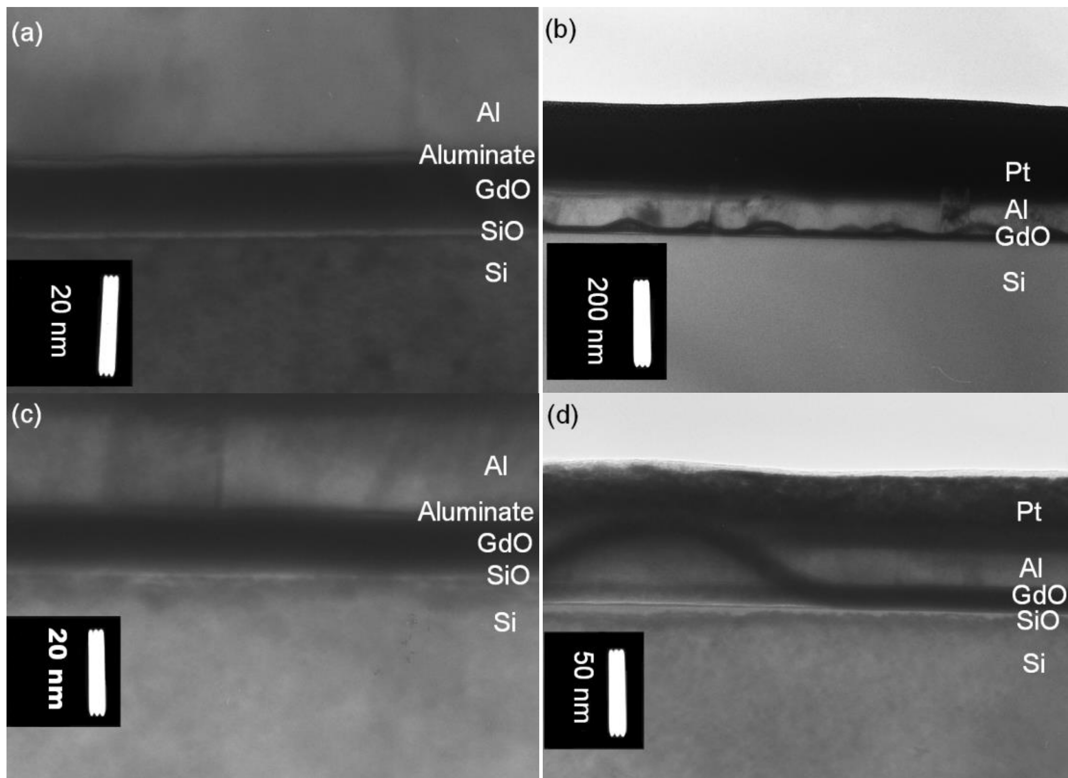

Figure IV.10: (a) and (b) Cross-sectional TEM images of the Gd_2O_3 films oxidized at 750 ºC. (c) and (d) Images of the films oxidized at 500 ºC. (a) and (c) high magnification images, used to measure Gd_2O_3 and SiO_x thickness and (b) and (d) low magnification images, where the density of domes can be observed. Samples were covered by Pt for protection during FIB sample preparation.

In any case, independently on the origin of the bumps, they are clearly at the origin of the low effective permittivity calculated: even if the permittivity were the same as Gd_2O_3, since they are 2-3 times thicker and occupy a big portion of the MIS surface, they produce a severe decrease on capacitance. This decrease would be even more exacerbated if the dome explanation is correct, since in that case, the capacity of the bump is the Gd_2O_3 capacity in series with the vacuum capacity, which has a relative permittivity of 1.

As a consequence of this problem, even after the low D_{it} values found, it can be concluded that pure thermal oxidation of metallic Gd does not meet the requirements for future high κ dielectrics, and this path is discarded. Thus, following a similar approach as the works on HfO_2 of Hoshino and Yamamoto *et al.*,[23,24] the next step was to study the low temperature plasma oxidation of metallic Gd layers.

IV.3.- SUMMARY AND CONCLUSIONS

In this chapter the thermal oxidation of metallic Gd films was explored in order to obtain high κ Gd_2O_3 on Si with minimal SiO_x regrowth. The GIXRD results showed that full oxidation of the metallic Gd films was obtained at temperature higher than 350 ºC. At an oxidation temperature of 500 ºC (and above) the films showed a transition from monoclinic structure to a mixture of monoclinic and cubic phases. The regrowth of interfacial SiO_x is observed as the temperature is increased, up to 1.6 nm for a 750 ºC oxidation. The leakage current and interface trap density decreased with oxidation temperature, being minimal after the oxidation at 750 ºC and after performing a FGA at 450 ºC (with values of ~10^{-4} A/cm^2 and 4×10^{10} eV^{-1}cm^{-2}, respectively). However, a low effective permittivity of the MIS device was found (~7.4) due to the formation of domes at the Gd_2O_3/Si interface. These bumps increased the average thickness, thus reduced the capacitance and therefore the calculated permittivity. So the advantage of the high κ Gd_2O_3 was lost using this thermal oxidation process. For that reason, the exploration of other processing approaches is needed in order to obtain device quality high κ Gd_2O_3.

REFERENCES

[1] J. Pu, S.-J. Kim, Y.-S. Kim, B. J. Cho. "*Evaluation of gadolinium oxide as a blocking layer of charge-trap flash memory cell*". Electrochem. Solid-State Lett. 11, H252 (2008).

[2] M. Toledano-Luque, M. L. Lucía, A. del Prado, E. San Andrés, I. Mártil, G. González-Díaz. "*Optical spectroscopic study of the SiN/HfO_2 interfacial formation during rf sputtering of HfO_2*". Appl. Phys. Lett. 91, 191502 (2007).

[3] S. Hayashi, K. Yamamoto, Y. Harada, R. Mitsuhashi, K. Eriguchi, M. Kubota, M. Niwa. "*Comparison of thermal and plasma oxidations for HfO_2/Si interface*". Appl. Surf. Sci. 216, 228 (2003).

[4] K. Yamamoto, S. Hayashi, M. Niwa, M. Asai, S. Horii, H. Miya. "*Electrical and physical properties of HfO_2 films prepared by remote plasma oxidation of Hf metal*". Appl. Phys. Lett. 83, 2229 (2003).

[5] K. Yamamoto, W. Deweerd, M. Aoulaiche, M. Houssa, S. De Gendt, S. Horii, M. Asai, A. Sano, S. Hayashi, M. Niwa. "*Electrical and physical characterization of remote plasma oxidized HfO_2 gate dielectrics*". IEEE Trans. Electron Devices 53, 1153 (2006).

[6] H. Z. Massoud, J. D. Plummer, E. A. Irene, "*Thermal oxidation of silicon in dry oxygen: accurate determination of the kinetic rate constants*". J. Electrochem. Soc. 132, 1746 (1985).

[7] R. W. B. Pearse, A. G Gaydon. "*The identification of molecular spectra*". 4th edition. John Wiley & Sons, Inc., New York (1976).

[8] G. Norlén. "*Wavelengths and energy levels of Ar I and Ar II based on new interferometric measurements in the region 3400-9800 Å*". Phys. Scr. 8, 249 (1973).

[9] B. Wende, "*Optical transition probabilities of the configurations $3p^5 4s$-$3p^5 5p$ of Argon I,*" Zeitschrift für Physik 213, 341 (1968).

[10] S. Wolf. "Microchip manufacturing". Lattice Press. Sunset Beach, California (2004).

[11] W. F. Meggers, C. H. Corliss, B. F. Scribner. "*Tables of spectral-line intensities, Part I - Arranged by elements, Part II – Arranged by wavelengths, Natl. Bur. Stand. Monograph 145*". Natl. Bur. Stand. U.S., 600 (1975).

[12] D. K. Schroder. "Semiconductor material and device characterization". John Willey & Sons, Hoboken, New Jersey, 2006.

[13] R. W. G. Wyckoff. "Crystal Structures". John Wiley & Sons, New York, 1963.

[14] M. P. Singh, C. S. Thakur, K. Shalini, S. Banerjee, N. Bhat, S. A. Shivashankar. "*Structural, optical and electrical characterization of gadolinium oxide films deposited by low-pressure metalorganic chemical vapor* deposition". J. Appl. Phys. 96, 5631 (2004).

[15] Y. Shoujing, W. Feng, W. Yi, Y. Zhimin, T. Hailing, D. Jun. "*Phase control of magnetron sputtering deposited Gd_2O_3 thin films as high-k dielectrics*". J. Rare Earths 26, 371 (2008).

[16] L. G. Parratt. "*Surface studies of solids by total reflection of X-rays*". Phys. Rev. 95, 359 (1954).

[17] P. G. Pai, S. S. Chao, Y. Takagi, G. Lucovsky. "*Infrared spectroscopic study of SiO_x films produced by plasma enhanced chemical vapor deposition*". J. Vac. Sci. Technol. A 4, 689 (1986).

[18] R. A. B. Devine. "*Structural nature of the Si/SiO2 interface through infrared spectroscopy*". Appl. Phys. Lett. 68, 3108 (1996).

[19] E. San Andrés, L. Pantisano, J. Ramos, P. J. Roussel, B. J. O'Sullivan, M. Toledano-Luque, S. De Gendt, G. Groeseneken. "*Accurate gate impedance determination on ultraleaky MOSFETs by fitting to a three-lumped-parameter model at frequencies from DC to RF*". IEEE. Trans. Elect. Dev. 54, 1705 (2007).

[20] J. R. Hauser, K. Ahmed. "*Characterization of ultra-thin oxides using electrical C-V and I-V* measurements". AIP Conf. Proc. 449, 235 (1998).

[21] E. H. Nicollian, A. Goetzberger. "*The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique*". Bell Syst. Tech. J. 46, 1055 (1967).

[22] G. L. Molnár, G. Petö, Z. Vértesy, E. Zsoldos. "*Kinetics shape formation during Gd thin film and Si(100) solid phase reaction*". Appl. Phys. Lett. 74, 1672 (1999).

[23] Y. Hoshino, Y. Kido, K. Yamamoto, S. Hayashi, M. Niwa. "*Characterization and control of the* $HfO_2/Si(001)$ *interfaces*". Appl. Phys. Lett. 81, 2650 (2002).

[24] K. Yamamoto, S. Hayashi, M. Kubota, M. Niwa. "*Effect of Hf metal predeposition on the properties of sputtered* HfO_2/Hf *stacked gate dielectrics*". Appl. Phys. Lett. 81, 2053 (2002).

Chapter V:

Plasma oxidation of Gd_2O_3 and Sc_2O_3

Thermal oxidation of metallic Gd did not produce good results due to the dome-shaped structures that appeared at the interface between the dielectric and the substrate. These reduced the effective permittivity, as it was pointed out in the former chapter. Thus, the study of other alternatives is mandatory in order to obtain, with HPS, a high κ dielectric with good performance from metallic targets. Following different approaches for plasma oxidation of Hf[1-4] and Ti[5] layers, in this chapter a two-step process was studied with the aim of obtaining Gd_2O_3 and Sc_2O_3 from metallic targets using HPS. First, a thin film of Gd or Sc was sputtered in an Ar atmosphere and, afterwards, an *in situ* plasma oxidation was carried out in a mixed Ar/O_2 atmosphere.

In this chapter, Gd_2O_3 is more thoroughly studied than Sc_2O_3. This is due to several reasons, such as the higher permittivity value of Gd_2O_3 (κ~15)[6,7] as compared to Sc_2O_3 (with a κ value around 13)[8] and its compatibility with III-V substrates.[9-11] Besides, using the same HPS system with oxide targets, it was found that the interface thickness regrowth was smaller for Gd_2O_3 in comparison with Sc_2O_3,[12,13] pointing out to a higher chemical stability of Gd_2O_3 in contact with Si.

The Ar/O_2 ratio and the *rf* power of the plasma were studied by means of GDOS with the aim of obtaining the optimal Gd and Sc sputtering parameters. The films were physically characterized by GIXRD, XPS, FTIR and TEM. The electrical study was carried out by the fabrication of MIS devices with Al and Pt as gate electrode. D_{it} was measured with the conductance method[14] and with DLTS.[15]

V.1.- EXPERIMENTAL METHOD

A two-step deposition process was developed with the aim of obtaining Gd_2O_3 and Sc_2O_3 using HPS from metallic Gd and Sc targets, respectively. After the metallic thin film deposition in pure Ar plasma (with a process duration ranging from 60 to 180 s) and without exposing the sample to the atmosphere, a plasma oxidation was carried out with the introduction of a small amount of oxygen into the chamber. Both processes were performed at 0.50 mbar and at room temperature. Several O_2 ratios (from 0 to 20%) and plasma oxidation conditions (*rf* power and oxidation duration) were studied. The plasma oxidation was executed between 100 and 300 s and several *rf* powers were analyzed (from 10 to 50 W). Besides, in some of the samples studied here, an evaporated SiO_x acting as field oxide (FOX) was introduced with the aim of characterizing the leakage current of the MIS capacitors reliably.

V.2.- RESULTS AND DISCUSSION

2.1.- Feasibility of the two-step deposition process for Gd_2O_3 and Sc_2O_3

2.1.A.- Plasma characterization of metallic Gd sputtered in Ar/O_2 atmosphere

In the former chapter, the plasma characterization by means of GDOS was analyzed for metallic Gd sputtered in an Ar atmosphere for different *rf* powers and pressures (figure IV.2). To carry out the *in situ* plasma oxidation of the Gd layer, the introduction of O_2 into the chamber is needed. Oxygen concentration varying between 0 to 20% was studied with an *rf* power of 30 W. In Figure V.1, three different concentration of Ar/O_2 atmospheres are shown, together with the pure Ar spectrum, for comparison purposes. The spectra were measured with the monocromator system and in the range of 290 to 490 nm.

As it can be observed in this figure, no traces of N_2 or H_2O[16] can be detected in any spectrum (they have clear signatures at 310-320 nm and at 336 and 358 nm, respectively, as it was shown in chapter II). Besides, when the plasma atmosphere is pure Ar, there are features due to non ionized and singly ionized Ar and Gd (Ar I, Ar II, Gd I and Gd II), as it was commented in the previous chapter.[17-19]

On the other hand, the introduction of O_2 into the chamber modifies the plasma emission completely: all the Gd peaks located between 300 and 400 nm disappear and also the intensity of the main peak of Gd I (located at 422.5 nm) decreases.[19] Moreover, the peaks corresponding to Ar I and Ar II[17,18] are less significant. In particular, Ar II intensities decrease drastically. It is noteworthy to point out that sputtering theory says that only ionized species can produce sputtering.[20] Also, when the amount of O_2 is increased, all peaks in the spectrum remain present but their intensities are lower. So, the introduction of a small amount of oxygen into the chamber (even only a 5% of O_2) changes the plasma dynamics, reducing the extraction of Gd from the target. The reason of this behavior can be the tendency of O_2 to become negatively ionized.[21] The trapping of secondary electrons by O_2 can decrease the plasma ionization efficiency, thus reducing the amount of ionized Ar and consequently producing a less efficient sputtering.

Besides, in Figure V.1 no oxygen peaks are unambiguously identified in the mixed Ar/O_2 atmosphere. Since they should be present in the 390-470 nm range, they

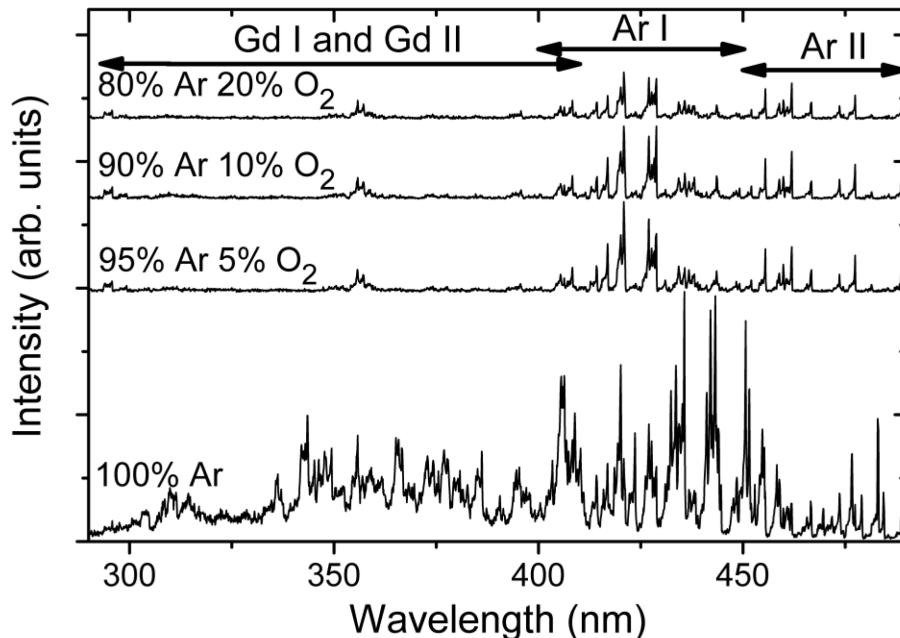

Figure V.1: GDOS spectra of metallic Gd sputtered in an Ar/O_2 atmosphere at 0.50 mbar and at room temperature with different oxygen concentration (from 0 to 20%) at 30 W. The ranges with the most important lines for Ar I, Ar II, Gd I and Gd II are marked in the figure.

might be overshadowed by the Gd and Ar peaks. One of the strongest emission lines of non ionized oxygen (O I) is located at 394.7 nm[22] without any Ar or Gd peak nearby, so it is a perfect region to check oxygen excitation. In this case, a slightly peak located around 395 nm is observed but the intensity is the same for all the O_2 concentrations, even for the 20% oxygen plasma. This fact suggests that some oxygen excitation is taking place. This energetic oxygen can react with the growing film, producing gadolinium oxide and even oxidizing the silicon substrate. To better control the oxidation rate, it was decided to perform the plasma oxidation with the lowest oxygen concentration (95% of Ar and 5% of O_2). This way, the process would be slower and, hence, more easily controlled.

Once the O_2 concentration was fixed, the *rf* power was explored. Thus, it was varied between 30 and 50 W. In Figure V.2 it is shown the GDOS spectra with the variable *rf* power. From the figure it was found that increasing the *rf* power up to 50 W does not produce any new peak. New peaks might be an indication of the apparition in the plasma of new species. The only difference is the increase in the intensity of the Ar peaks, more relevant for Ar II (ionized Ar) than Ar I. This result suggests that when the

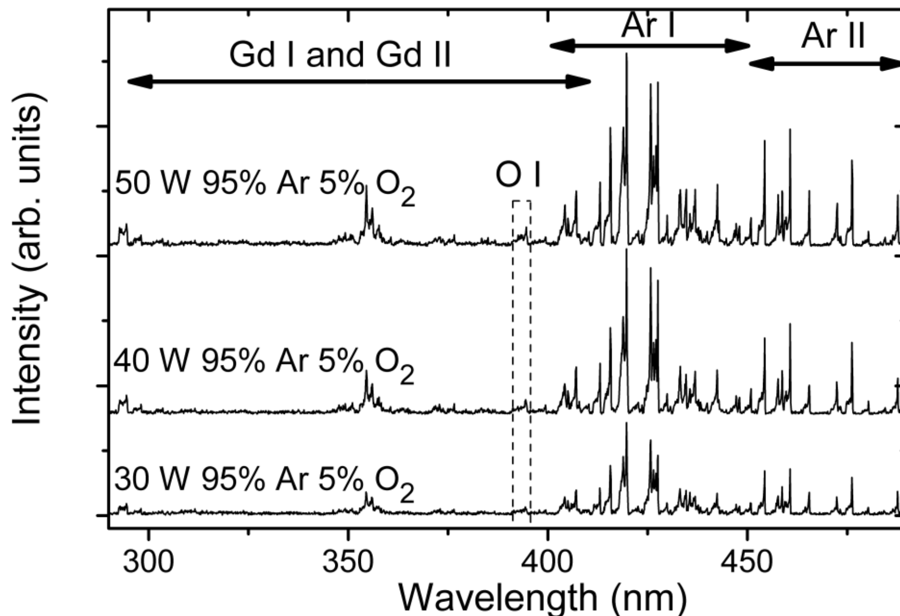

Figure V.2: GDOS spectra of metallic Gd sputtered in a 95% Ar and 5% O_2 atmosphere at 0.50 mbar and at room temperature with different *rf* power varying from 30 to 50 W. The ranges with the most important lines for Ar I, Ar II, Gd I, Gd II and the most intense peak of O I are marked in the figure.

power increases, the sputtering rate accordingly increases. Also, when focusing at 395 nm (wavenumber for the most intense O I emission), there is a weak peak increase with *rf* power, pointing out again to a plasma oxidation, more evident for higher powers.

In order to find out whether when oxygen was introduced only an oxidation process took place or there was also some deposition, Figure V.3 presents the cross-sectional TEM image of a film obtained by sputtering a Gd target during 5 min with an Ar/O_2 plasma (with a ratio of 95/5) at 30 W on a bare Si substrate (without the metallic Gd deposition step). There, it can be observed that no evidence of a Gd_2O_3 layer is found. If it were present, it would appear as a dark film between the glue and the Si. In this figure, only an amorphous bright layer of around 3 nm thick over the Si can be found. Together with the former GDOS results, the most likely explanation could be that at this low *rf* power there is no (or little) Gd extraction. Thereby, the bare Si substrate (that was prepared with an HF-last cleaning before it was loaded into the chamber) was exposed to the excited Ar/O_2 atmosphere, resulting on the oxidation of the substrate and creating a SiO_x film. In other words, when the power is 30 W, there is only a plasma oxidation of the sample, with negligible or no deposition of Gd. This oxidation is effective even at room temperature, as this TEM image proves.

Since the aim is to use a controllable oxidation without Gd deposition, the oxidation conditions chosen were a 95% Ar / 5% O_2 atmosphere with 30 W of *rf* power.

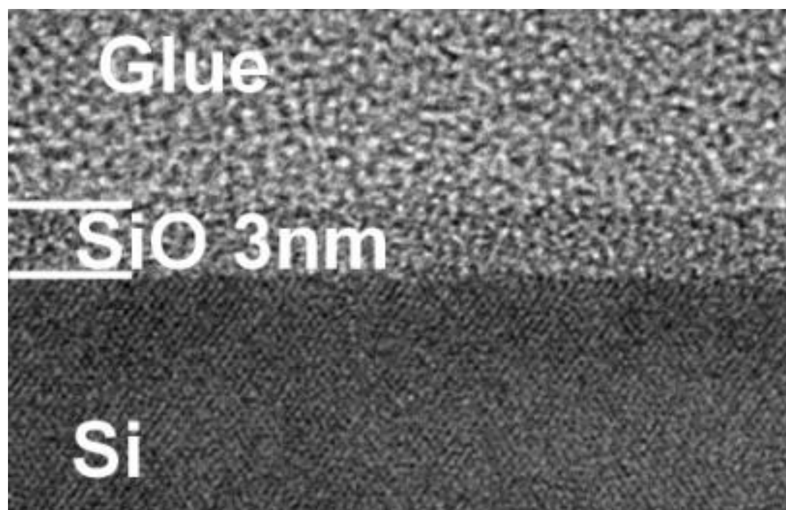

Figure V.3: Cross-sectional TEM image of a bare Si substrate exposed to an Ar/O_2 plasma with 30 W and 0.50 mbar during 5 min at room temperature.

2.1.B.- Plasma characterization of metallic Sc sputtered in pure Ar and mixed Ar/O_2 atmospheres

Now, the optical emissions of the plasma when Sc is sputtered in Ar and Ar/O_2

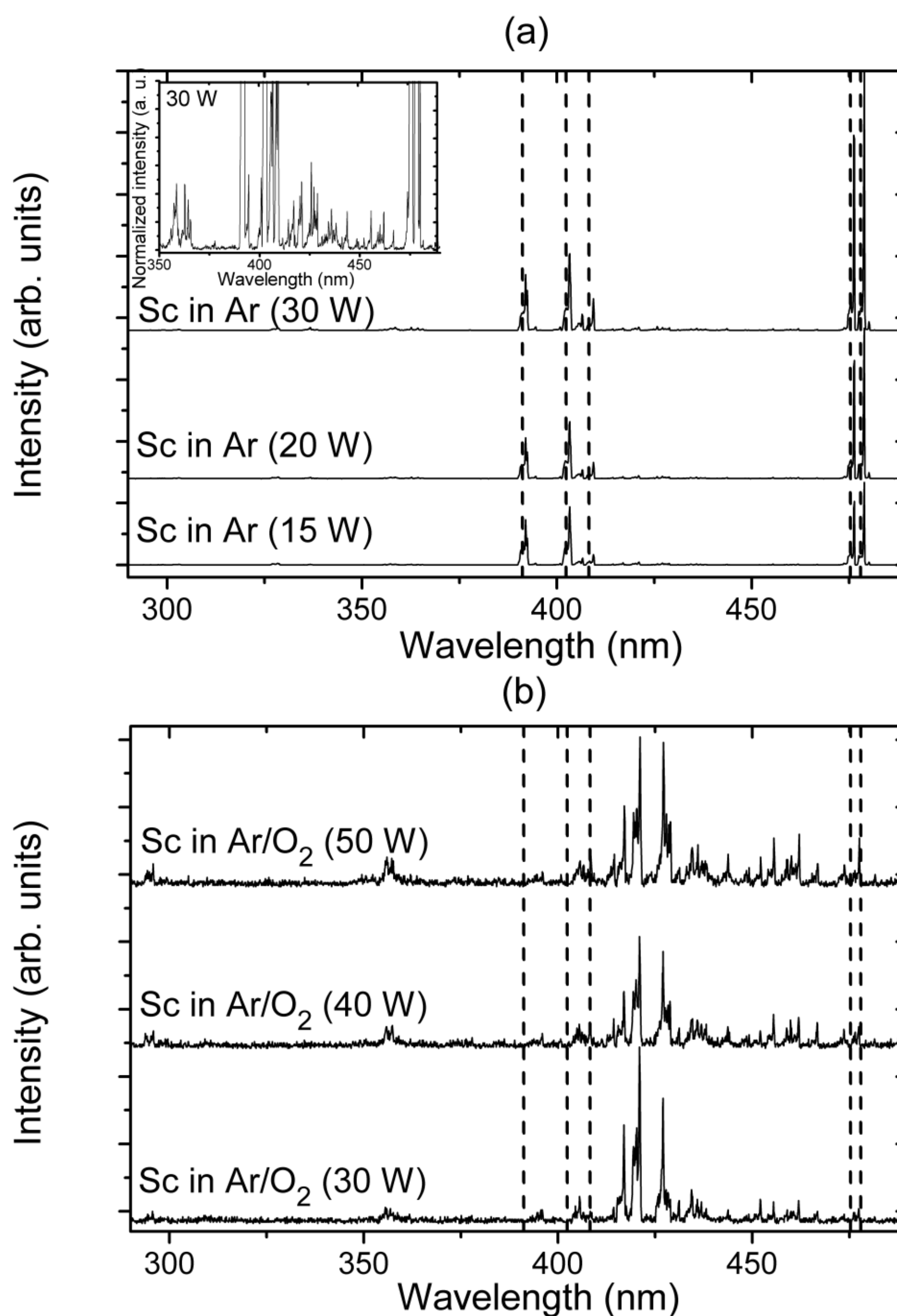

Figure V.4: GDOS spectra of metallic Sc sputtered at 0.50 mbar and at room temperature for different *rf* powers in (a) a pure Ar atmosphere and (b) a 95% / 5% Ar/O_2 plasma. The most intense Sc I peaks are marked in the figure with dashed lines. In the inset of (a), an enlargement is made for the *rf* power of 30 W to observe the Ar I and Ar II peaks.

atmospheres are analyzed. The obtained spectra were also measured between 290 and 490 nm and with the same GDOS system. In Figure V.4(a) is represented the GDOS spectra for different *rf* powers (from 15 to 30 W) when metallic Sc is sputtered in a pure Ar atmosphere. Again, there are not peaks corresponding to H_2O or N_2 in the spectra. Extremely intense peaks located at 391, 402, 408, 475 and 478 nm can be observed in all these spectra. These peaks are related to Sc I[23] and due to their high intensity it seems that no other peaks are found. In the inset of this figure, an enlargement of the 30 W spectrum is shown in order to appreciate the peaks related to Ar I and Ar II,[17,18] necessary for the Sc extraction.

When oxygen is introduced into the chamber, again there is also a complete change in the plasma dynamics as it was observed with the Gd case. As Figure V.4(b) shows for different *rf* powers (from 30 to 50 W) in a mixed Ar/O_2 atmosphere (with a 95%/5% ratio), the intensity of the Sc I peaks decreased dramatically and the Ar I peaks (between 400 and 450 nm) can be appreciated. Besides, a slight peak around 395 nm related to O I is observed. Therefore, the sputtering of Sc in an Ar/O_2 plasma could be explained as in the Gd case: the extraction of Sc is extremely reduced when introducing oxygen into the chamber and an oxidation process is also taking place.

2.1.C.- Structural characterization of the plasma oxidized Gd_2O_3 films

With the aim of further studying the plasma oxidation conditions, some bare Si substrates were sputtered in an Ar/O_2 atmosphere during long times (from 30 to 90 min, in order to obtain thicker films and to minimize signal noise) with different *rf* powers (varying between 30 and 50 W).

The GIXRD results for metallic Gd target are shown in Figure V.5. It is observed there that the substrates sputtered for plasma powers above 40 W present the monoclinic Gd_2O_3 phase,[24] with a clear peak located at 29.3º and a light band around 42.3º, both marked with solid lines in this figure. Nevertheless, at 30 W no peaks are observed in the diffraction spectrum. As it was presented in the former chapter, when Gd is sputtered in a pure Ar atmosphere, the hexagonal structure was obtained (figure IV.3). So, these results could be explained as follows: for the metallic Gd target in an Ar/O_2 plasma and with *rf* power higher or equal than 40 W, there is not only oxidation but also some deposition, producing a film of monoclinic Gd_2O_3. Therefore, for these powers the

Ar II is capable of extracting Gd atoms, even although no Gd is clearly detected in the GDOS spectra (Figure V.2). Since no hexagonal metallic Gd diffractions are present and only Gd_2O_3 peaks are found, this suggests that the oxygen in the plasma is effective in oxidizing completely the growing film. However, at an *rf* power of 30 W, no Gd is deposited in this mixed atmosphere and the growing film is amorphous. Together with the TEM image presented in Figure V.3, it can be concluded that only an oxidation process is taking place at 30 W (even for a long oxidation of 90 min) when the plasma is a mixture of Ar/O_2.

As GIXRD results showed, sputtering Gd in an Ar/O_2 plasma at 40 W and above produces a polycrystalline Gd_2O_3 film. However, obtaining an amorphous layer is desirable for MOSFETs applications,[25,26] because the grain boundaries could be more conductive and thus, the leakage current could be higher. So, a modification on the typical sputtering process was explored in order to use this plasma oxidation effect as an advantage. Thereby, instead of depositing directly Gd_2O_3 on Si from the metallic Gd target (at 40 W and above in the Ar/O_2 atmosphere), a two-step deposition process was implemented. First, a thin metallic Gd film was deposited on the top of the bare Si in a

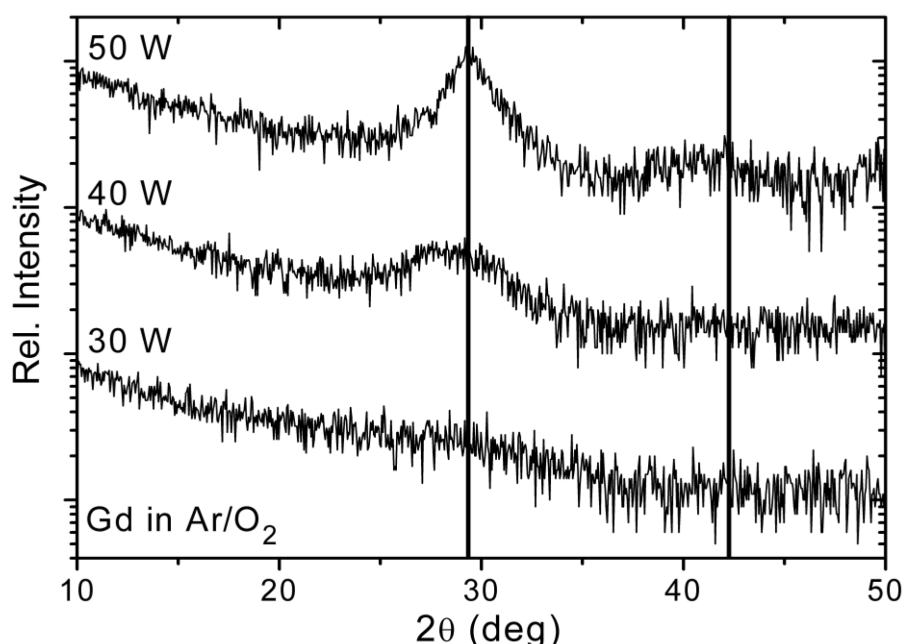

Figure V.5: GIXRD spectra of bare Si substrates sputtered in Ar/O_2 atmosphere with Gd target and at different *rf* powers (from 30 to 50 W). The observed diffraction peaks have been identified as monoclinic gadolinium oxide and are marked with solid lines.

pure Ar atmosphere at 30 W. Afterwards, without extracting the sample to the atmosphere, this metallic layer was *in situ* oxidized by a 30 W Ar/O_2 plasma. This way, when there was excited oxygen in the chamber, the substrate was protected by the Gd film and the regrowth of SiO_x is minimized.

To find out the chemical composition of the GdO_x film obtained with this two-step process, XPS analysis was carried out. Figure V.6 shows the high resolution Gd 4d (left) and O 1s (right) core-level spectra of the top surface of a sample which was obtained at room temperature after 60 s of Gd sputtering and a plasma oxidation of 300 s, both using 30 W as *rf* power and at 0.50 mbar of pressure. Also, the fit of these peaks (obtained by using symmetric Gaussian-Lorentzian functions (90G/10L)) are included. In the left hand side of Figure V.6, the doublet splitting Gd 4d is represented, with two main contributions at around 142.1 and 147.9 eV, which is in agreement with literature reports for stoichiometric Gd_2O_3.[27,28] In the right hand side, the O 1s peak located at a binding energy of ~531.4 eV is slightly sifted to higher energies respect to the Gd-O bond (that is located at ~530 eV) due to the known hygroscopic effect of Gd_2O_3, also reported in the literature.[29,30] From these peaks, the O/Gd arithmetic mean

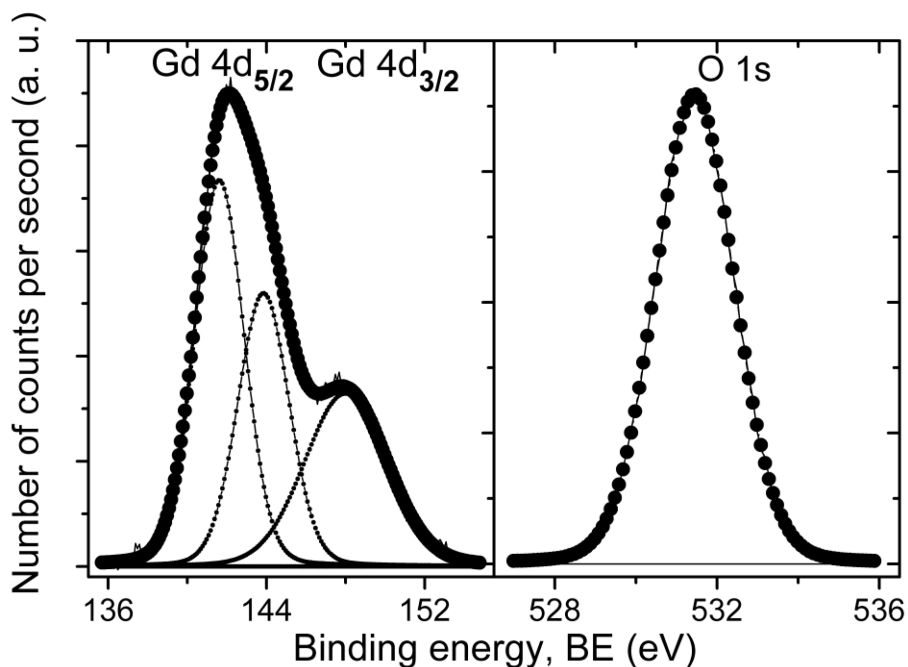

Figure V.6: Gd 4d doublet (left) and O 1s (right) core-level peaks and their fits taken from the surface of a ~3 nm thick film of Gd_2O_3 grown with a two-step method from a Gd target.

ratio obtained is 1.51 ± 0.06. Thus, this plasma oxidation process produced almost stoichiometric Gd_2O_3 films.

2.1.D.- Structural characterization of the plasma oxidized Sc_2O_3 films

For the sputtering of metallic Sc target in Ar/O_2 atmosphere for long times (60 min), no diffraction patterns are observed in the spectra, even at high *rf* power up to 50 W, as it is presented in Figure V.7. The only known Sc_2O_3 stable structure is the cubic bixbyite phase.[31] The absence of diffraction peaks (the most intense are marked in this figure) could mean that either the Sc_2O_3 grown is amorphous or that there is only an oxidation process, even at a high power such as 50 W. Sc_2O_3 deposited by the same HPS using an oxide target was polycrystalline with a non preferential direction growth, with many GIXRD peaks related to this structure.[32] Thus, the most likely explanation in the metallic Sc case is that there is no Sc_2O_3 deposition and only a plasma oxidation is taking place, even at 50 W.

2.1.E.- Electrical characterization of MIS devices with plasma oxidized Gd_2O_3 and Sc_2O_3

With the aim of obtaining the C-V_{gate} curves, two sets of MIS devices were

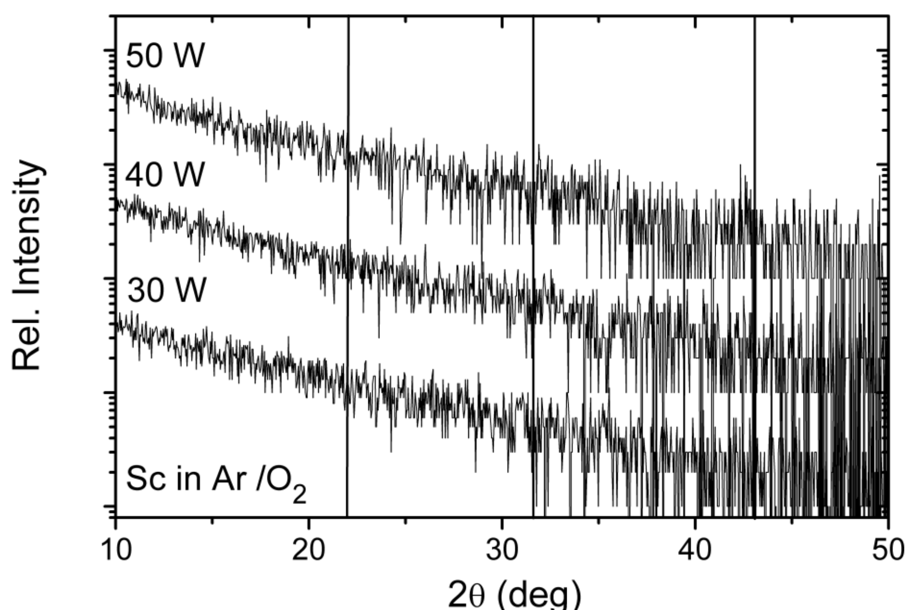

Figure V.7: GIXRD spectra of bare Si substrates sputtered in Ar/O_2 atmosphere with Sc target and at different *rf* powers: 30, 40 and 50 W. The most intense peaks in the Sc_2O_3 cubic phase are marked in solid lines.

fabricated using both targets, Gd and Sc. The process conditions were identical for both sets (60 s of metal deposition and 300 s of plasma oxidation at 30 W and 0.50 mbar) and two different top electrodes were used: ~40 nm of Al and a gate stack formed with ~3 nm of Pt (we used a thin Pt layer in order to avoid adhesion problems due to stress) capped with ~30 nm of Al (with the aim of avoiding the perforation of the metal gate when probing, which can lead to the high κ structural degradation). To ensure that the gate stack was identical for both metallic electrodes, after HPS deposition on bare 2'' Si wafers, samples were cut and then each piece was evaporated with the above mentioned metallic gate. These sets of samples were fabricated without field oxide, so probing was made on top of the gate stack. The backside of the wafers was covered with Ti/Al (50 nm/100 nm), to ensure a good ohmic contact to the n-Si wafer. A forming gas anneal (FGA) was performed at 300 ºC during 20 min.

C-V_{gate} characteristics of MIS devices measured at 10 kHz and after the FGA are represented in Figure V.8 for the two different top metal electrodes studied. Figure V.8(a) shows the results with Gd_2O_3 as dielectric while Figure V.8(b) for the Sc_2O_3 case. The samples evaporated with Al have the lowest accumulation capacitance

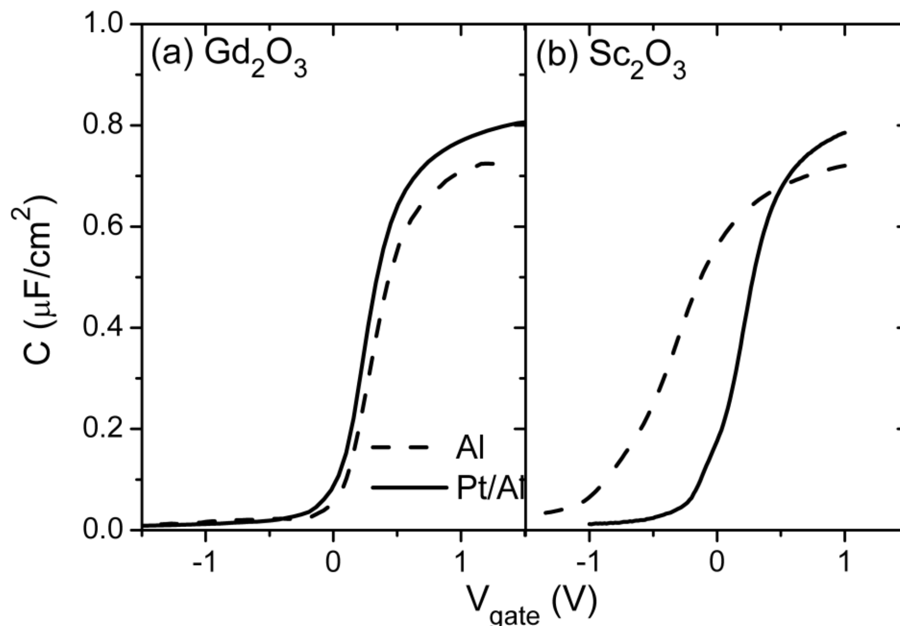

Figure V.8: C-V_{gate} curves of MIS devices using (a) Gd_2O_3 and (b) Sc_2O_3 as dielectric with two metallic gates: Al in dashed lines and Pt/Al in solid lines. The capacitors were measured at 10 kHz and after a FGA at 300 ºC for 20 min.

value (therefore, the highest EOT) for both dielectrics. The EOT values obtained with the CVC algorithm[33] are shown in Table V.1. When Pt is used as top electrode, the EOT is about 0.4-0.5 nm smaller than Al. The explanation of this is that Pt is a noble metal and it does not react with the dielectric. For this reason, Pt is useful to study the bare properties of dielectrics films. On the other hand, when the gate is Al, the metal can react with the high κ film, with the possible outcome of the formation of aluminates, as it was also observed in chapter IV. Besides, the D_{it} value, estimated from the conductance peak in depletion with the conductance method,[14] is also presented in Table V.1.

Sample	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
Gd_2O_3 with Al	4.1	2×10^{11}
Gd_2O_3 with Pt/Al	3.7	1×10^{11}
Sc_2O_3 with Al	4.2	2×10^{12}
Sc_2O_3 with Pt/Al	3.7	3×10^{11}

Table V.1: EOT and D_{it} values extracted from electrical measurements after the FGA at 300 ºC for samples with different dielectrics obtained with the two-step method (Gd_2O_3 and Sc_2O_3) and two metallic contacts: Al and Pt/Al.

To further investigate the differences observed in the capacitance value from Figure V.8, TEM images were obtained for Gd_2O_3 films. On Figure V.9(a), the cross-sectional image of the Al sample is represented. It can be seen that the interfacial SiO_x thickness is about ~1.7 nm under ~3.1 nm of an amorphous Gd_2O_3 layer. Also, an amorphous ~2.7 nm film on top of the dielectric layer is observed. This could be due to the proposed formation of an aluminate-like film at the metal/high κ interface. This interface reaction was also observed in the former chapter (figure IV.10). On the other hand, Figure V.9(b) shows the Pt capped with Al sample. Here, the thicknesses of the SiO_x and Gd_2O_3 films are similar than in the Al case: ~1.8 and ~3.1 nm, respectively. This is an expected result because the dielectric deposition was carried out in the whole wafer and it was cut in pieces before the e-beam evaporation of the different metallic contacts. Besides, no reaction between the Pt and the high κ is observed. Due to the Al

reaction and the formation of the aluminate, in the following experiments, Pt was used as the top electrode in order to study the plain properties of the dielectrics.

The main conclusion of this section was that the two-step process introduced here had been able to grow stoichiometric and amorphous Gd_2O_3 films. Besides, MIS devices with this dielectric film and with Sc_2O_3 had reasonable electrical performance.

2.2.- Optimization of the two-step deposition process for Gd_2O_3

Once the feasibility of this two-step method was demonstrated, it was important to analyze the high κ/Si interface in order to reduce the thickness of the SiO_x that could grow during the plasma oxidation. Besides, the optimization of this process is required for achieving a dielectric film with higher κ value. Thus, FTIR and electrical characterization were used to study this interface for different growing conditions. As it was commented before, we focused on Gd_2O_3 due to its higher interest because of its higher permittivity6[,7] and its compatibility with III-V substrates.9[-11] MIS devices were fabricated without FOX using different thicknesses of Gd_2O_3 (changing the fabrication conditions). The top electrode was ~5 nm of Pt capped with ~20 nm of Al. The bottom one was Ti (50 nm)/Al (100 nm). The effect of three different parameters was explored: oxidation power, initial metal thickness and oxidation time. With the aim of obtaining a thicker Gd_2O_3 film than in the former section, the reference sample was chosen with 80 s of Gd deposition and 300 s of oxidation. Both processes were performed at 30 W, at room temperature and at 0.50 mbar.

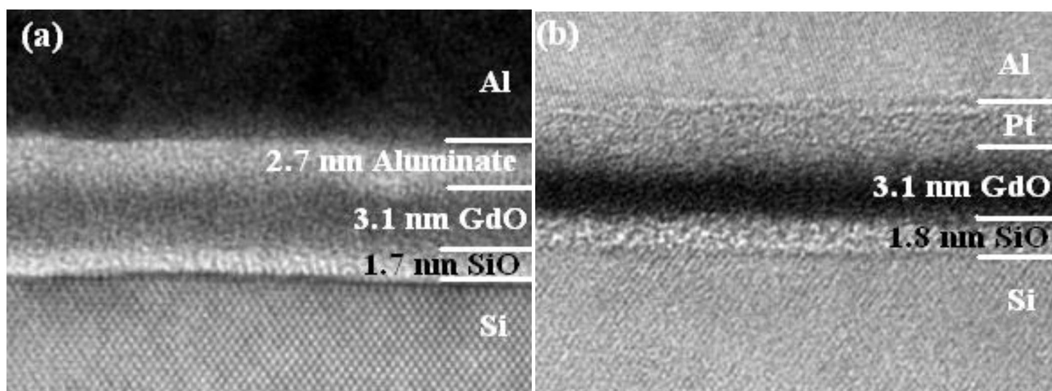

Figure V.9: Cross-sectional TEM images of the Gd_2O_3 films after a FGA at 300 ºC using (a) Al and (b) Pt/Al gate stack.

2.2.A.- Oxidation power effect

In this set of samples the *rf* power of the oxidation step was changed from 10 to 30 W keeping the step duration at 300 s. Figure V.10 presents FTIR absorbance spectra in the range of 1200-900 cm^{-1} for these samples oxidized with different *rf* powers before the FGA. A peak centered at ~1035 cm^{-1} can be observed, which is related to substoichiometric SiO_x[34,35] As it can be seen in this figure, samples oxidized at 10 and 20 W present a SiO_x band that is similar in intensity and shape, but this peak increases for the sample oxidized at 30 W. To minimize the effect of baseline correction, in the inset of this figure the peak area as a function of the oxidation power is shown. Since the area of the peak can be directly related to the SiO_x thickness, these results point to an increase of the SiO_x thickness for 30 W. This is an indication that there is more regrowth of interfacial SiO_x for the highest analyzed power, 30 W, thus higher oxidation powers will not be explored.

Figure V.11 depicts the normalized capacitance, C, of MIS capacitors as a function of the gate voltage, V_{gate}, measured at 10 kHz, for the as deposited devices and after the FGA at 300 ºC for 20 min for the three different oxidation powers studied. Table V.2 summarizes the EOT and D_{it} values obtained for these samples before and after the FGA from the electrical measurements.

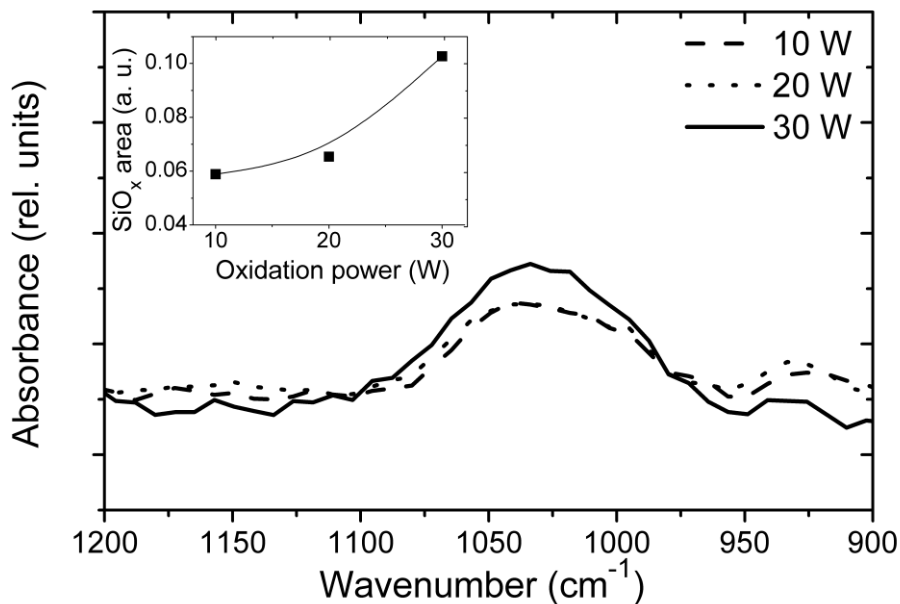

Figure V.10: FTIR spectra for Gd_2O_3 samples with different oxidation *rf* power: 10, 20 and 30 W. Inset: SiO_x peak area as a function of the *rf* power for the same samples.

	Without FGA		FGA 300 ºC	
Oxidation power (W)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
10	4.0	3×10^{12}	4.2	2×10^{11}
20	2.8	2×10^{12}	4.1	1×10^{11}
30	3.8	5×10^{12}	4.0	---

Table V.2: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with different oxidation power. "---" means that the D_{it} value is under the detection limit of the method.

The as grown sample oxidized at 20 W presents the highest value of the accumulation capacitance, with an EOT value of 2.8 nm. These results together with the FTIR spectra observed in the former figure suggest an excessive oxidation (involving an interfacial SiO_x regrowth) at 30 W (the EOT is 1 nm higher than the EOT of the sample oxidized at 20 W), while at 10 W the Gd film is not completely oxidized, yielding a lower κ dielectric film.

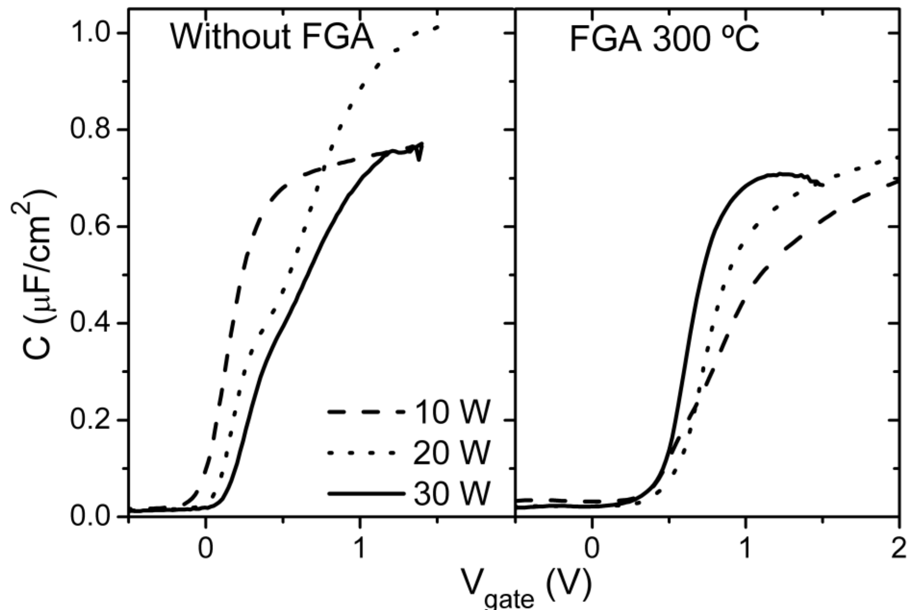

Figure V.11: Normalized capacitance as a function of gate voltage before and after the FGA at 300 ºC for samples with different *rf* oxidation power: 10, 20 and 30 W.

A great reduction of the accumulation capacitance is observed after the FGA for the sample with an oxidation power of 20 W. This could be due to a ~1.3 nm SiO_x growth or to Pt adhesion problems that could reduce the effective electrode area (some bubbling was found in these devices after the FGA treatment).[36] Samples oxidized at 10 and 30 W, present an increase in the EOT of only 0.2 nm. This striking result will be analyzed later with the TEM images.

Additionally, capacitance curves present a slight hump in depletion before the FGA that is reduced after the temperature treatment. D_{it} obtained with the conductance method[14] reaches values of $\sim 10^{11}$ $eV^{-1}cm^{-2}$ after the FGA (also shown in Table V.2), pointing out to an interface improvement. Since no appreciable conductance peak could be observed for the sample oxidized at 30 W after the FGA, it can be concluded that the interfacial states density was under the detection limit of this method, due to the hydrogen passivation during the FGA.

TEM images of samples with a plasma oxidation at 30 and 20 W after a FGA at 300 ºC are presented in Figure V.12. The 30 W oxidized sample shows a ~6.1 nm of amorphous Gd_2O_3 layer over a ~1.8 nm of SiO_x interlayer regrowth. The same values were obtained for the 20 W oxidized sample. This result together with the C-V_{gate} curves obtained in Figure V.11 could be explain as follows: the Gd_2O_3 layers have the same thickness for both samples because the metal deposition time is the same (80 s) and the oxidation processes (during 300 s at 20 and 30 W) produce a complete oxidation of these metallic films. The main difference is that before the FGA, the 20 W oxidized

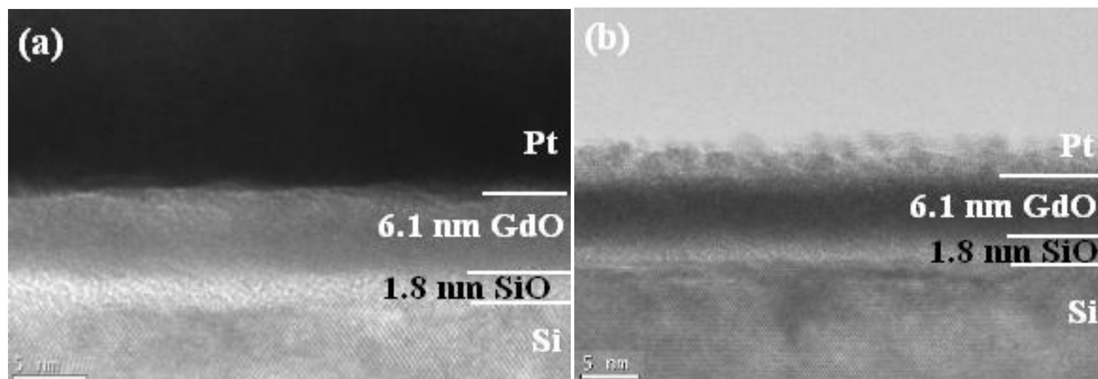

Figure V.12: Cross-sectional TEM images of the Gd_2O_3 films with 80 s of Gd and 300 s of plasma oxidation at (a) 30 W and (b) 20 W after a FGA at 300 ºC using Pt/Al gate stack.

device presents less SiO_x at the interface because the oxidation is softer, as it was pointed out previously with the FTIR and the electrical measurements results. Thus, this capacitor presented the highest accumulation capacitance. During the FGA, a regrowth of this SiO_x film is produced because a reaction between the Si substrate and the Gd_2O_3 dielectric. The total thickness of this interlayer saturates, meaning that when the SiO_x thickness reaches a value around 1.8 nm, the regrowth process does not continue or it is very slow. The final SiO_x thickness is comparable to the 30 W case. On the other hand, for the higher power (30 W) the saturation process could occur during the oxidation step. It was commented before that the oxidation of the Gd film during 300 s at 30 W was long enough to produce the complete oxidation of the dielectric layer and, additionally, oxidize the Si substrate. According to the EOT values for the 30 W device shown in Table V.2, the FGA does not increase this value significatively, supporting this hypothesis. It is interesting to remark that on bare Si the growth of native SiO_2 saturates at a thickness around 2 nm, a similar value that was presented in Figure V.12 and also in Figure V.9.

Finally, 10 W is a power low enough to excite the oxygen and to produce the oxidation. Thus, there is no excess oxygen concentration within the GdO_x film for this power, since it was not completely oxidized. In this case, few oxygen atoms are able to reach the Si surface to produce a significant regrowth of SiO_x during the FGA, since the atmosphere is reducing. The GdO_x does not increase its permittivity being oxygen deficient.

In conclusion, a plasma oxidation step carried out at 20 W, seems to be the best option to control the regrowth of the SiO_x layer for the as deposited samples. It was found an EOT ~1 nm lower as compared with the other *rf* powers.

2.2.B.- Initial metal deposition time influence

The influence of the initial thickness of metallic Gd on the properties of the Gd_2O_3 layer ant its interface with Si obtained after the plasma oxidation is discussed in this subsection. The Gd deposition time was modified between 80 to 160 s in order to achieve thicker films and the oxidation was carried out for 300 s at 30 W.

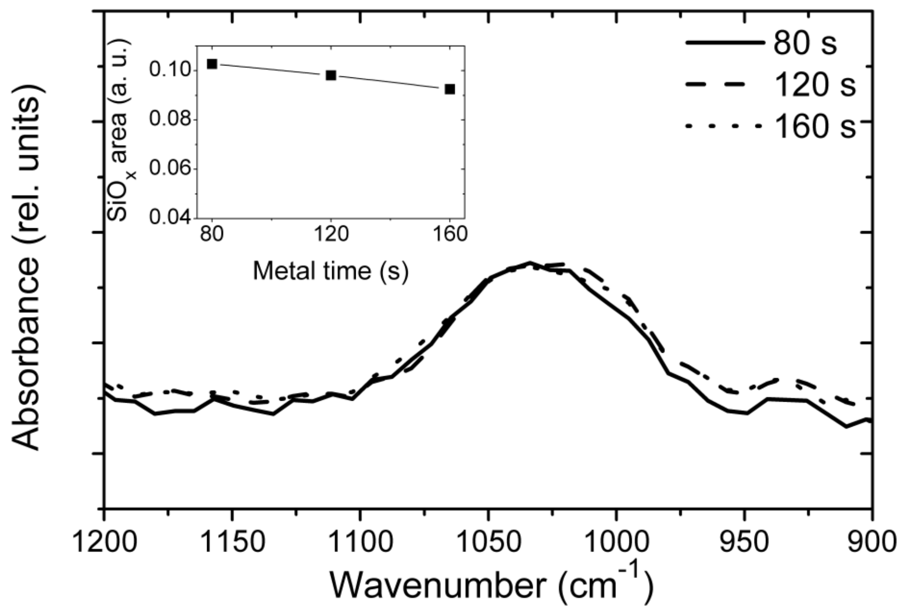

Figure V.13: FTIR spectra for Gd_2O_3 samples with different metal deposition time: 80, 120 and 160 s. Inset: SiO_x area as a function of the metal deposition duration for the same samples.

Figure V.13 shows the FTIR results for the as deposited samples. It can be observed that these samples present a peak centered at ~1035 cm^{-1} related to substoichiometric SiO_x.[34,35] Additionally, the three samples present bands that are similar in shape and area. Nevertheless, the peak area for the 80 s sample is slightly more intense than the others, as it can be seen in the inset of this figure. This means that these thicknesses of the initial Gd layer were not acting as a diffusion barrier for oxygen and a similar SiO_x regrowth is obtained at the interface for the three samples.

In Figure V.14, the electrical behavior for the devices with different metal deposition time is represented. C-V_{gate} curves before the FGA for these capacitors show the expected trend: higher metal deposition time provides lower accumulation capacitance, due to the thicker Gd_2O_3 layer. Thus, the EOT is 3.8, 4.3 and 4.5 nm, as the initial Gd deposition time is increased. However, after the FGA, sample with 160 s presents higher accumulation capacitance (so, lower EOT) than the sample with 120 s (4.3 versus 4.8 nm). This surprising result will be discussed with the aid of TEM images.

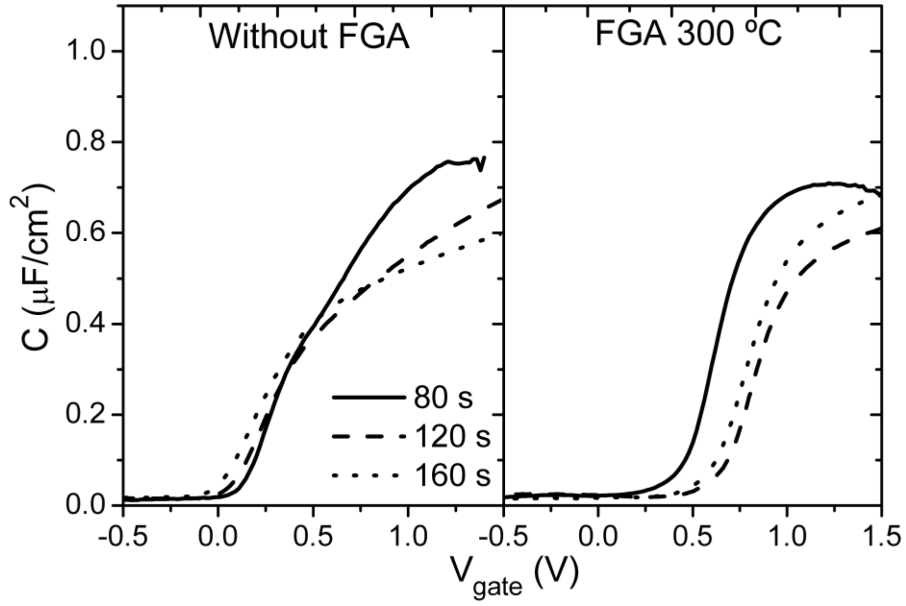

Figure V.14: C-V_{gate} characteristics for samples with different initial Gd deposition time (varied between 80 to 160 s) before and after the FGA at 300 ºC.

FGA for these samples does not produce great changes according to the EOT values. Nevertheless, in agreement with the conductance measurements, the interfacial traps density shows a significant improvement due to hydrogen passivation. D_{it} is reduced more than one order of magnitude after the FGA, reaching a value of ~5×10^{10} $eV^{-1}cm^{-2}$ for the thicker samples (for the 80 s sample, the D_{it} is under the detection limit of the method). Table V.3 summarizes the EOT and D_{it} values for these samples before and after the FGA.

	Without FGA		FGA 300 ºC	
Metal deposition time (s)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
80	3.8	5×10^{12}	4.0	---
120	4.3	1×10^{12}	4.8	5×10^{10}
160	4.5	7×10^{11}	4.3	5×10^{10}

Table V.3: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with different metal deposition duration. "---" means that the D_{it} value is under the detection limit of the method.

Figure V.15 shows a HRTEM image of a device with the thicker Gd film deposited during 160 s and after the FGA. There, it is observed a stacked structure, with a darker layer of ~5 nm on top of a lighter one ~4 nm thick. Both layers are amorphous. The most remarkable result here is the fact that doubling the metal deposition time does not yield a dielectric layer twice as thick. The total thickness for the 160 s sample should be 12 nm instead of 9 nm, because with 80 s of Gd deposition, a layer around 6 nm thick is obtained (Figure V.12(a)). Energy dispersive X ray spectroscopy (EDX) measurements confirmed the Gd and O presence on both layers. The contrast observed can have two different origins: different oxidation degrees of the GdO_x film or the formation of a Gd-Si-O silicate.[13] Since, no evidence of a regrowth of a SiO_x film is observed in this TEM image and the FTIR results showed a band associated to SiO_x before the FGA, this silicate layer could be formed during the FGA by a reaction between the GdO_x layers and the SiO_x that grew during the sputtering process. This result could be due to an oxidation process not long enough for the 160 s of Gd film. During the plasma oxidation the excited oxygen performs the oxidation of the Gd film, starting from the upper layers and then, diffusing deeper. The FTIR results showed that the Gd layer was not acting as an oxygen barrier but HRTEM indicates that if the oxidation time is too short, the complete Gd oxidation is not achieved. Thus, there are

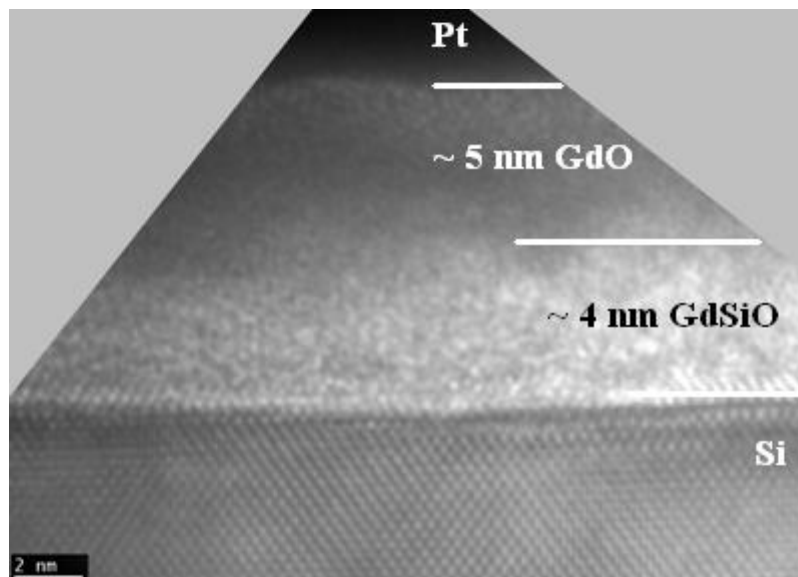

Figure V.15: HRTEM image of the Gd_2O_3 film with 160 s of Gd and 300 s of plasma oxidation at 30 W after a FGA at 300 ºC using Pt/Al gate stack.

many dangling bonds within the GdO_x layer in the region close to the substrate that could react with the SiO_x forming the silicate. However, if this oxidation duration is longer or the Gd thickness is low, a SiO_x layer appears, as it could be noticed in Figure V.12. In this case, the reaction between the Gd_2O_3 layer and the SiO_x is not so likely because the films are stoichiometric and more stable, so intermixing to form the silicate is not that easy. Finally, this uncompleted oxidation for the thicker Gd must be the origin of the anomalous tendency of the accumulation capacitance.

It is important to highlight that the silicate formation observed here had also been reported in other works that used rare earth metal oxides.[37-39] An interesting issue of these silicates is that they do not necessarily rule out the device scaling because subnanometer EOTs can be achieved with good behavior.[40,41]

As a conclusion of this section, it appears that a thicker Gd layer does not prevent the SiO_x regrowth but it is important to optimize plasma conditions to assure a complete Gd oxidation. Thus the oxidation time is an important parameter to be analyzed in order to control the SiO_x formed during the oxidation that could react with the Gd suboxide during the FGA to form a silicate.

2.2.C.- Oxidation time

In this first experiment, after the 80 s of Gd deposition, the time of the oxidation step (carried out at 30 W) was varied between 150 to 300 s.

Firstly, it can be seen that as the oxidation time is increased, the area of the SiO_x band observed in the FTIR spectra clearly increases, as shows Figure V.16. Thus, longer oxidation time increases the SiO_x thickness between the interface of Si and the Gd_2O_3, as the inset of this figure suggests. In any case, the presence of the Si-O stretching band for all three oxidation conditions indicates that some Si-O bonds are present at the interface. In other words, even for the shorter oxidation time (150 s) some oxygen atoms are able to reach the Si substrate.

Normalized capacitance vs V_{gate} for samples oxidized during different times are shown in Figure V.17 before and after the FGA at 300 ºC for 20 min and measured at 10 kHz. In this case, the trend is that, as expected, lower oxidation duration provides higher capacitance values in accumulation. Again in this case, the FGA decreases the

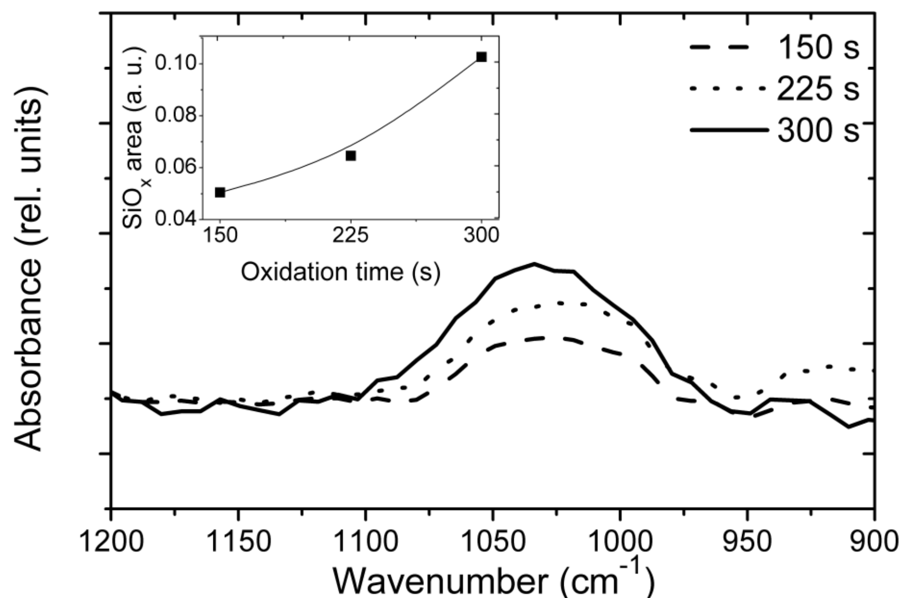

Figure V.16: FTIR spectra for Gd_2O_3 samples with different oxidation time: 150, 225 and 300 s. Inset: SiO_x area as a function of the oxidation time for the same samples.

accumulation capacitance, therefore increases the value of the EOT, and also improves the quality of the interface due to hydrogen passivation, achieving values of the D_{it} below the detection limit. Table V.4 summarizes the EOT and D_{it} values for these samples.

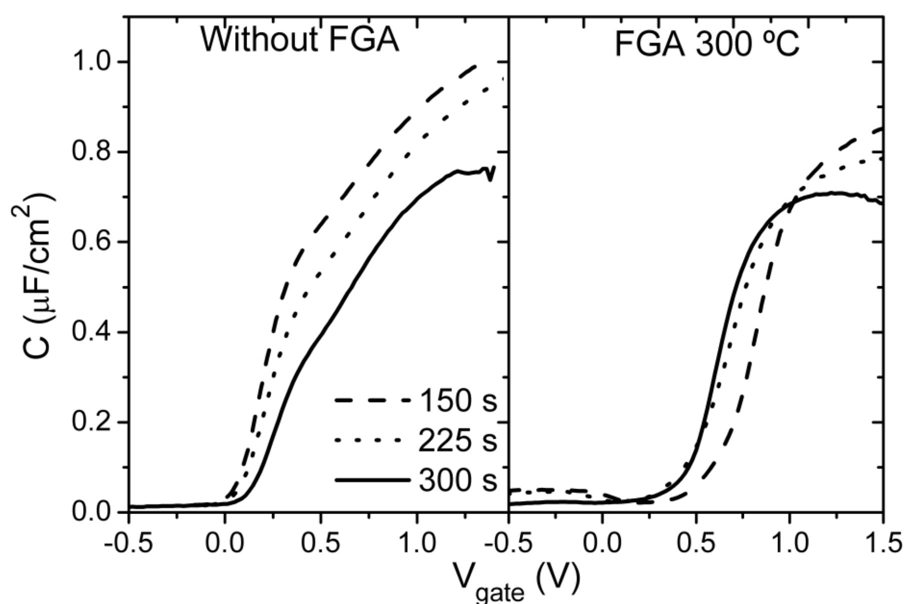

Figure V.17: C-V_{gate} before and after the FGA at 300 ºC for samples with different oxidation duration: 150, 225 and 300 s.

In Figure V.18, the HRTEM image of the sample after FGA with 150 s is presented. There, two layers over the Si can be observed: on top of the Si substrate one brighter film 3 nm thick, and another darker on top, 3.1 nm thick. *In situ* EDX measurements showed qualitatively the presence of Gd and O in both layers. Again, the explanation could be that there exist two different oxidation degrees of the GdO_x film due to the shorter oxidation time, or a formation of a silicate, as it was discussed in the former section. It is important to highlight that in this case, the total thickness of the dielectric film is around 6.1 nm, the expected result because the Gd deposition was carried out during 80 s. Thus, the silicate formation explained in the previous section is likely. The low thickness of the SiO_x layer for the 150 s sample before the FGA (shown in the FTIR results of Figure V.16), could promote the reaction between the dielectric (that is possibly oxygen deficient in the lower region) and the Si substrate. However, for longer oxidation time, this interface is more stable and has less dangling bonds, so the reaction is more difficult. But, in that case, a low κ film appears, as it was shown in Figure V.12.

Summarizing, a plasma oxidation carried out for 150 s (at 30 W) is enough to oxidize the Gd film grown during 80 s of Gd deposition. Besides, a small regrowth of SiO_x appears but, due to its low thickness, a silicate formation occurs after the FGA. This silicate layer should have a higher permittivity than the SiO_x, thus, these conditions seem to be the best to obtain a high κ dielectric film. For that reason, we studied even shorter oxidation times.

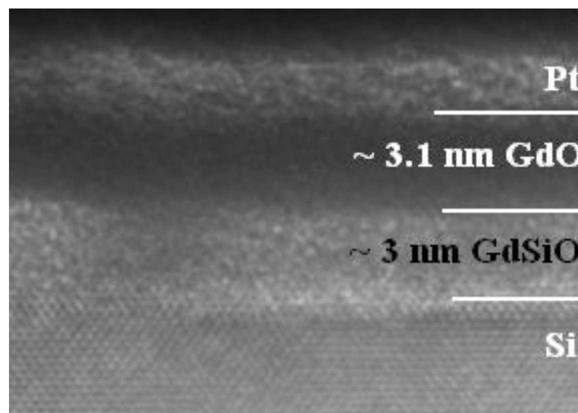

Figure V.18: Cross-sectional HRTEM image of the Gd_2O_3 film with 80 s of Gd and 150 s of plasma oxidation at 30 W after a FGA at 300 ºC using Pt/Al gate stack.

In order to minimize the SiO_x growth during the fabrication process, in a second experiment, thicker samples were fabricated and oxidized during shorter time. Therefore, the metallic Gd deposition was carried out during 120 s (at 30 W and 0.50 mbar). Afterwards, a softer plasma oxidation was performed for 100 s at 20 W and at the same pressure. Besides, a plasma oxidation during 300 s at 20 W was also explored to have a reference. FTIR samples and MIS capacitors (with a stack of 8 nm of Pt capped with 70 nm of Al as top electrode and 50 nm of Ti and 100 nm of Al as the backside) were fabricated. In order to analyze these MIS devices more reliably (with J-V_{gate} characteristics measurements), the fabrication process included the use of ~200 nm of thermal oxidized SiO_x acting as FOX.

Figure V.19 presents the absorbance spectra for these samples with different oxidation duration and before the FGA at 300 ºC in the range of 1200 to 900 cm^{-1}. It can be seen there that the peak located around 1040 cm^{-1}, related to SiO_x, is smaller for the sample with the lower duration (100 s). As this oxidation time is increased, the area of the SiO_x band is also bigger. This result is expected because a longer oxidation leads to a higher regrowth of the interfacial SiO_x during this process, as it was commented before.

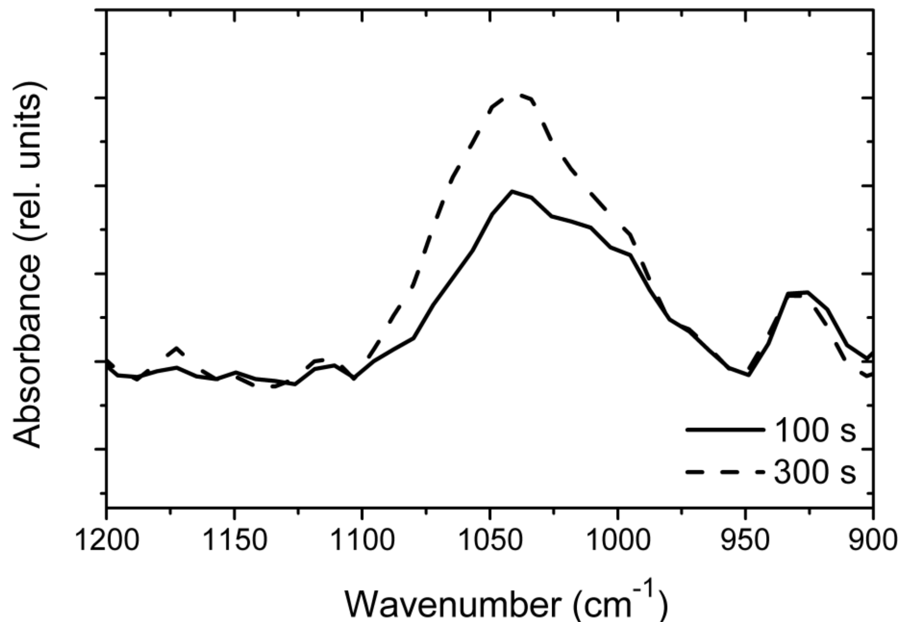

Figure V.19: FTIR spectra for Gd_2O_3 samples with 120 s of Gd and different duration of the plasma oxidation: 100 and 300 s.

C-V_{gate} and G-V_{gate} characteristics for these devices after the FGA at 300 ºC and measured at 10 kHz are shown in Figure V.20. The sample oxidized during 100 s presents the highest value of the capacitance in accumulation, hence, the lowest EOT. EOT values increase around 0.5-0.6 nm after the FGA (thus, there is a reduction in the maximum accumulation capacitance). According to the former results, this implies a formation of $GdSiO_x$ at the interface between the high κ and the Si, being lower, possibly, for the 100 s oxidation sample. The area normalized conductance of these samples has a value of ~10^{-3} S/cm^2 even at 1.5 V. This reduction of conductance is due to the lower leakage of these samples because the introduction of the FOX in the fabrication process.

Table V.5 summarizes the EOT and D_{it} values obtained for these samples before and after the FGA at 300 ºC. The increase of the EOT with the oxidation time is expected according the FTIR results shown in Figure V.19. However, the D_{it} values are reduced after the FGA, pointing out to a better interface passivation after the temperature treatment. The minimum reaches a value of 4×10^{10} $eV^{-1}cm^{-2}$ for the longer oxidation sample and 10^{11} $eV^{-1}cm^{-2}$ for shorter time. Both values are admissible for high κ materials.[42] It is remarkable that the sample with 120 s of Gd deposition and oxidized during 300 s at 30 W presented a similar value of the D_{it} but a higher EOT of

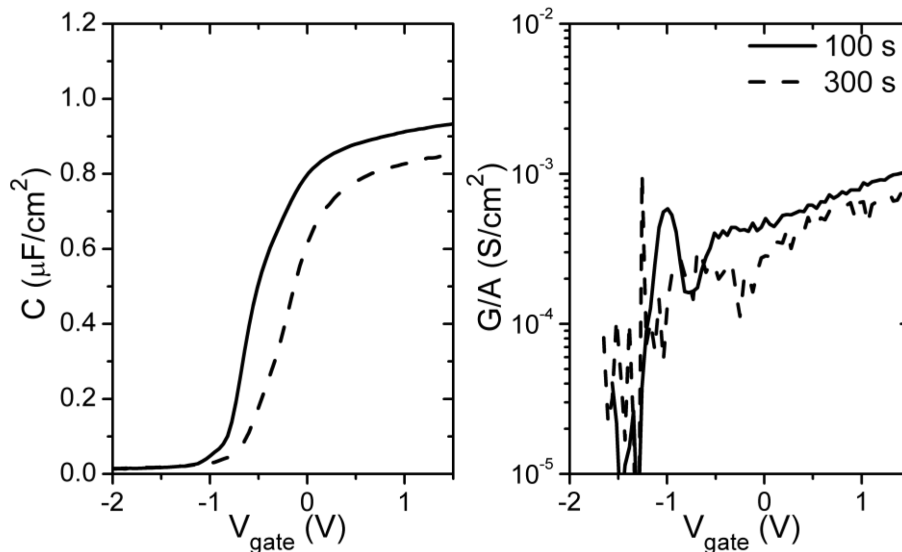

Figure V.20: C-V_{gate} and G-V_{gate} curves measured at 10 kHz and after the FGA at 300 ºC for samples with 120 s of Gd and 100 (solid lines) and 300 s (dashed lines) of plasma oxidation at 20 W.

4.8 nm (see Table V.3). This 1.2 nm reduction of EOT confirms that the oxidation at 20 W is softer while keeping good electric properties.

	Without FGA		FGA 300 ºC	
Oxidation time (s)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
100	2.8	4×10^{11}	3.3	1×10^{11}
300	3.0	3×10^{11}	3.6	4×10^{10}

Table V.5: EOT values and D_{it} extracted from electrical measurements before and after the FGA at 300 ºC for samples with 120 s of Gd and different plasma oxidation duration.

The leakage current curves as a function of the gate voltage of these samples after the FGA at 300 ºC are presented in Figure V.21. The leakage current density at 2 V is below 10^{-5} A/cm^2 for both samples, being slightly lower for the device with 300 s oxidation. This is the expected behavior because of the higher EOT value of this sample. These values are acceptable for low power applications.[25] It is important to

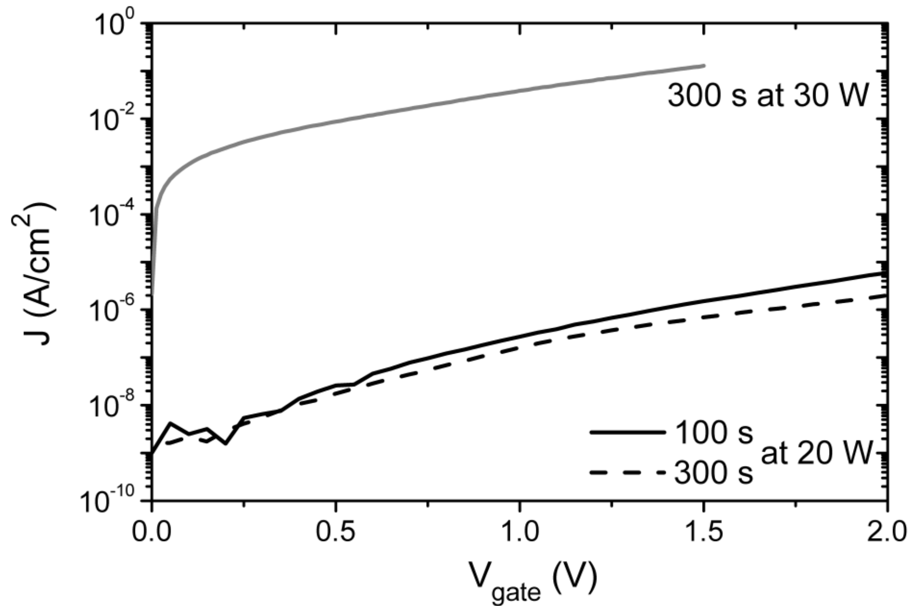

Figure V.21: J-V_{gate} characteristic after FGA at 300 ºC for samples with Gd deposition during 120 s and a plasma oxidation of 100 (solid lines) and 300 s (dashed lines). In grey is represented the sample with 120 s of Gd oxidized during 300 s at 30 W fabricated without FOX as a comparison.

highlight that the grey curve shown in this figure corresponds to the 120 s Gd sample oxidized during 300 s at 30 W fabricated without FOX. As it was commented in chapter II, the introduction of FOX avoided the dielectric damage during probing. Here it was found more than four orders of magnitude of leakage reduction with the field oxide and thus, the leakage through the dielectric can be studied reliably.

In conclusion, shorter oxidation time provided lower EOT with acceptable D_{it} and low leakage current values, even if a weak band associated to SiO_x is observed in FTIR spectra. The formation of $GdSiO_x$ is likely after the temperature anneal because the lower oxygen concentration in the dielectric layer permits the intermixing with the Si substrate, as it was observed in other rare earth metal oxides.[37-39]

2.3.- Effect of FGA temperature on optimized MIS devices with plasma oxidized Gd_2O_3

With the aim of obtaining a complete electrical study including thermal stability of MIS capacitors fabricated with this two-step process and with even lower EOT, the initial thickness of the metallic Gd had to be reduced. Using the best fabrication conditions obtained in the former sections, a set of MIS devices were grown with Gd deposited during 80 s (at 30 W and 0.50 mbar) and, afterwards, a plasma oxidation was performed during 100 s at 20 W and at the same pressure of the 95% Ar / 5% O_2 atmosphere. It was expected that these capacitors present a complete oxidation of the dielectric film with minimal SiO_x growth. Also, samples with 120 s of Gd and the same oxidation conditions were fabricated in order to have a reference with the previous samples. The top electrode was 25 nm of Pt while the backside was 50 nm of Ti and 100 nm of Al. These samples had ~200 nm of evaporated SiO_x as FOX. FGAs at 300 ºC, 350 ºC and 400 ºC were consecutively performed to the samples during 20 min. Samples were electrically measured before and after each FGA.

Figure V.22 represents the area normalized gate capacitance as a function of V_{gate} curves of these samples after representative FGA temperatures measured at 10 kHz. For the thinner sample with 80 s of Gd, the accumulation capacitance values do not present great differences for the as deposited sample and after the FGAs. In fact a small increase is observed, indicating an improvement in the effective κ value. The EOT of these

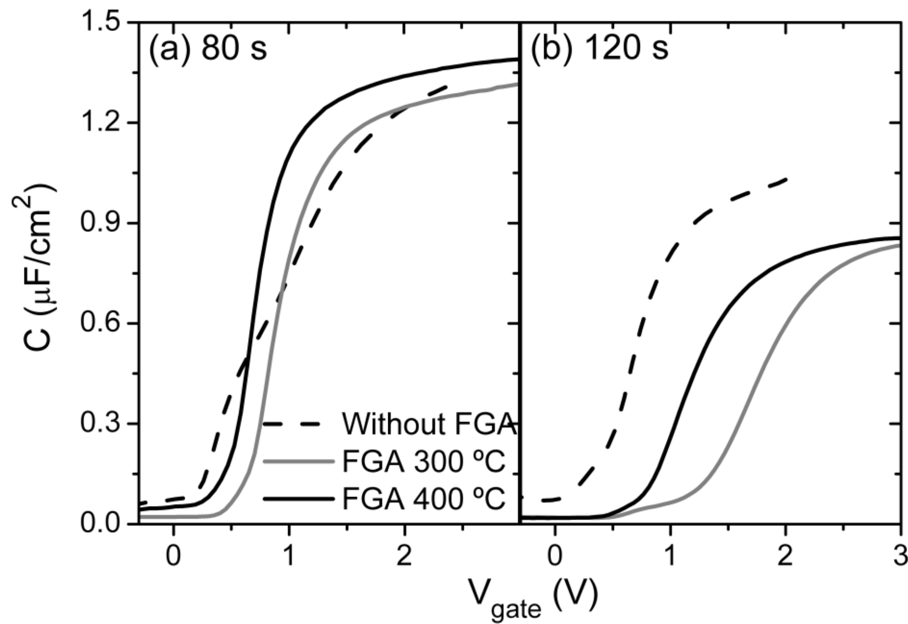

Figure V.22: Normalized C-V_{gate} curves measured at 10 kHz before and after the FGA at representative temperatures for samples with (a) 80 s and (b) 120 s of Gd with a plasma oxidation during 100 s.

samples is around 2.2 nm and it is represented in the left hand side of Figure V.23. Besides, similar flatband voltages (V_{FB}) are obtained for this sample before and after the annealings, indicating a stable dielectric stack.

On the other hand, for the thicker sample with 120 s of Gd deposition, an accumulation capacitance drop and V_{FB} instability with annealing temperature are observed. These effects could be explained by the $GdSiO_x$ formation (as it was commented before) at the interface between the GdO_x and the Si. The V_{FB} variations could be due to the movement of oxygen atoms in the silicate because of the high amount of dangling bonds. The EOT of this sample changes from 2.9 nm before annealing to 3.6 nm after FGA at 400 ºC (also shown in the left hand side of Figure V.23). In the former section, a similar EOT value was obtained. Thus, these electrical results also support the previous conclusion that an oxidation time too short produces a substoichiometric and unstable GdO_x which in contact with the Si substrate formed a $GdSiO_x$ like interface.

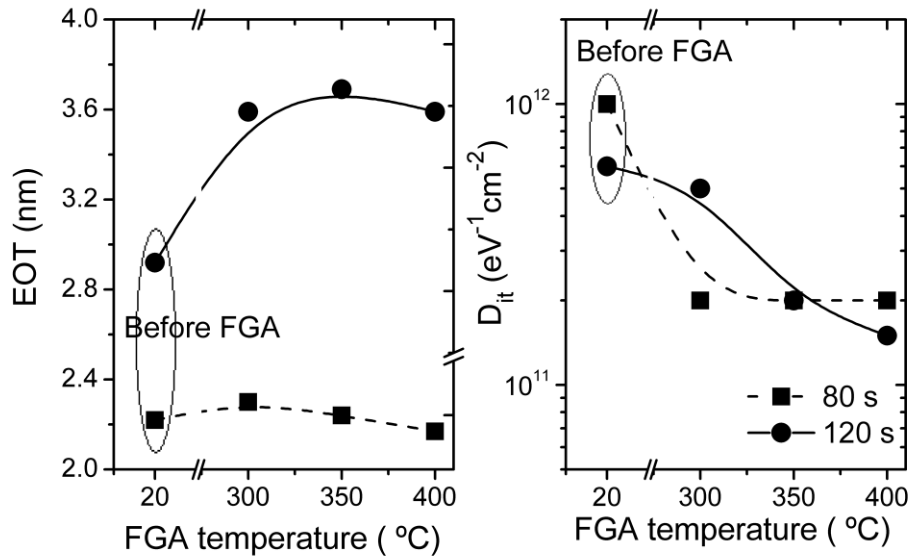

Figure V.23: EOT (left) and D_{it} (right) as a function of the annealing temperature for samples with 80 s (squares) and 120 s (circles) of Gd oxidized for 100 s.

Using the conductance method, the obtained D_{it} value is reduced one order of magnitude after the FGAs for the thinner sample, from ~10^{12} $eV^{-1}cm^{-2}$ to ~2×10^{11} $eV^{-1}cm^{-2}$. For the thicker films the trend is analogous: it is reduced from ~6×10^{11} $eV^{-1}cm^{-2}$ to ~1.5×10^{11} $eV^{-1}cm^{-2}$ after annealings. These values are also represented in the right hand side of Figure V.23. In any case, for both types of samples, the values obtained after the FGA at 400 ºC are lower or comparable to those reported in other works that use different high κ dielectrics.[43-45]

The sample with Gd deposited during 80 s was also measured by DLTS[15] and the D_{it} distribution after the FGA at 400 ºC is shown in Figure V.24. An almost flat distribution was found, with a midgap density around 1.5×10^{11} $eV^{-1}cm^{-2}$, very similar to the value achieved from the conductance method explained in the former paragraph.

In Figure V.25 is represented the gate leakage current density as a function of gate voltage. As it can be seen, these gate current densities are low: ~10^{-3} A/cm^2 for the thinner sample and below 10^{-4} A/cm^2 for the thicker one, even at V_{gate} as high as 3 V. These values are similar to those reported in other works,[44,46] and also those discussed in the former section and represented in Figure V.21. For the thinner sample, the FGA at 300 ºC reduces the leakage current around two orders of magnitude, possibly due to

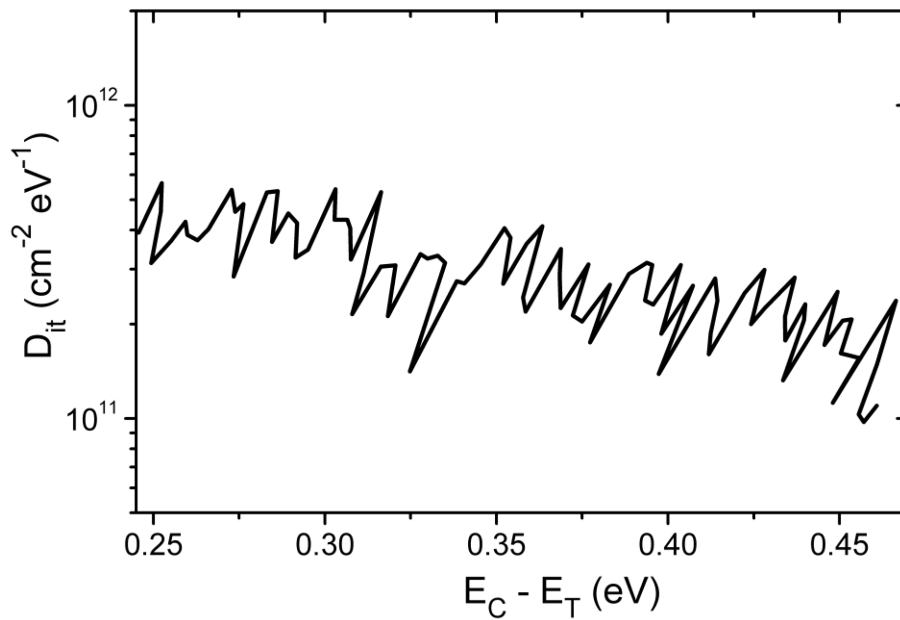

Figure V.24: Interface trap density obtained by DLTS for sample with 80 s of Gd and 100 s oxidation measured after the FGA at 400 ºC.

the hydrogen passivation. Increasing the FGA, increases slightly the current density. In the case of the thicker sample, the leakage is low and it is not affected by the FGA. Taur *et al*.[47] showed the J–V_{gate} curves for different values of the SiO_2 thickness. There it can

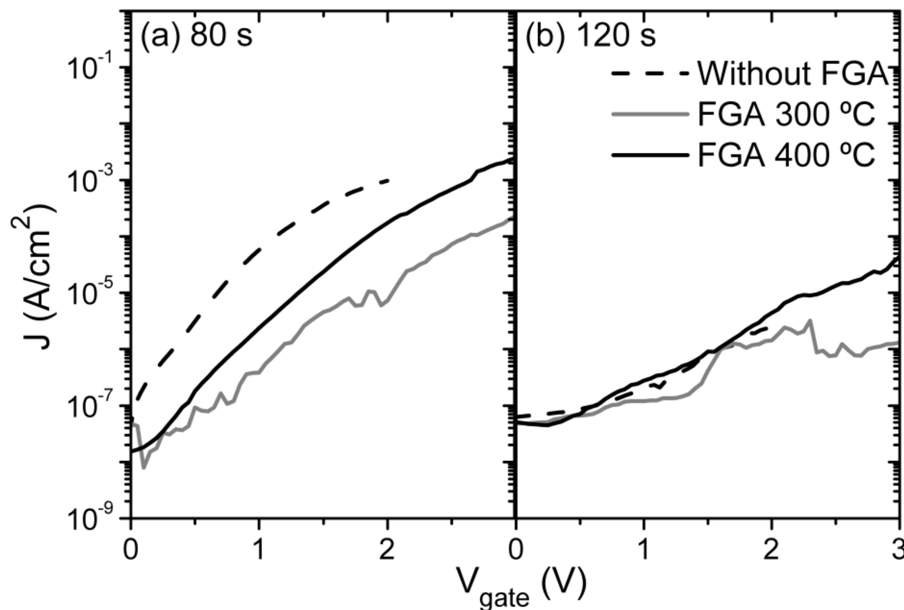

Figure V.25: J-V_{gate} characteristics before and after FGA at representative temperatures for (a) 80 s and (b) 120 s deposited Gd with a 100 s plasma oxidation.

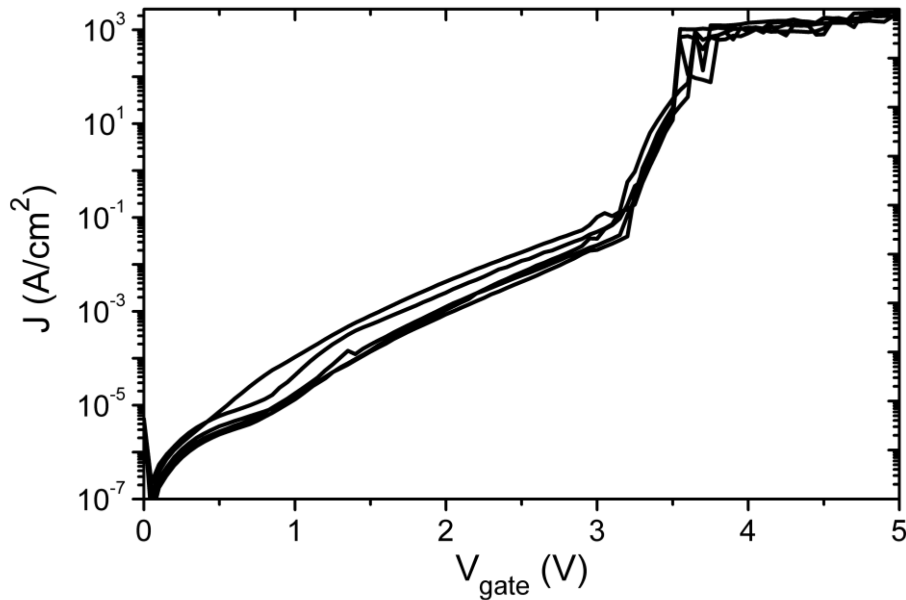

Figure V.26: J-V_{gate} curves for the sample with 80 s of Gd and 100 s of oxidation after FGA at 400 ºC, measured in several devices to observe breakdown events and reproducibility.

be observed that for a sample 2.2 nm thick, the interpolated leakage current at 3 V is around 1 A/cm^2, three orders of magnitude higher than the current obtained in Figure V.25.

Furthermore, in order to check the uniformity of the samples and also to obtain information about the maximum voltage applicable, in Figure V.26 it is shown the J-V_{gate} curves of several devices for the thinner sample (80 s of Gd) annealed at 400 ºC, measured beyond the hard breakdown voltages. There it can be observed that between 3.1 and 3.3 V the devices present an increase of the slope of the leakage current (soft breakdown events). At voltages between 3.5 and 3.7 V all devices show hard breakdown. These voltages are high enough for device applications, and the repeatability indicates a uniform and controlled Gd_2O_3 film.

Additionally, to gain insight of the conduction mechanism, J-V_{gate} curves were obtained at different temperatures (from 100 to 300 K) for the thinner sample and they are represented in Figure V.28. For $V_{gate} > 1.3$ V, the slope of ln(J) is constant and independent of the measured temperature. This points out that the conduction mechanism of this sample is related to a tunnel conduction, which is nearly temperature independent.[48]

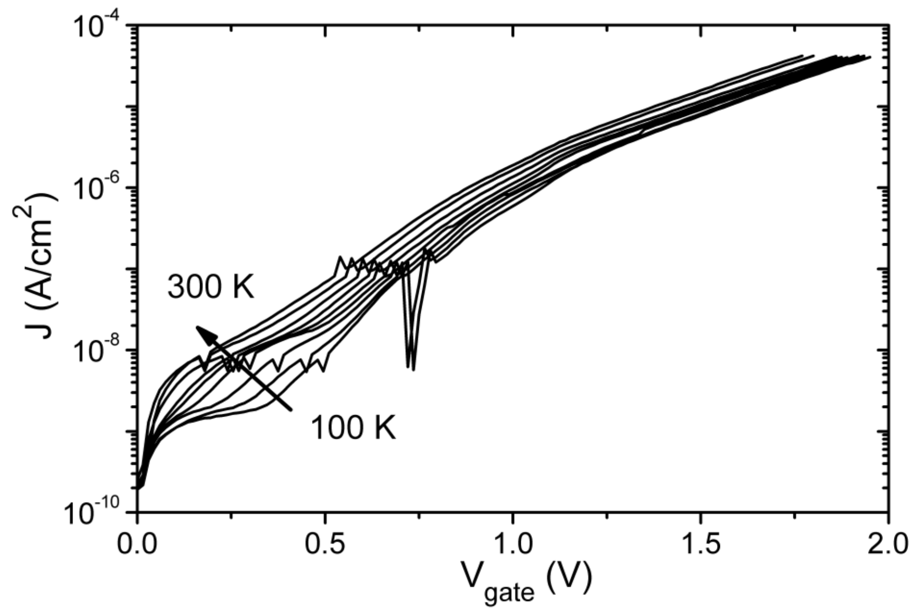

Figure V.28: J-V_{gate} characteristics measured at different temperatures (from 100 to 300 K) for the sample with 80 S of Gd and 100 s oxidation after the FGA at 300 ºC. In the inset, the exponential slope of J at V_{gate} > 1.3 V as a function of the temperature is represented.

The C-V_{gate} hysteresis curves measured at 10 kHz and after the FGA for both types of samples are shown in Figure V.27. The sweep started from accumulation to

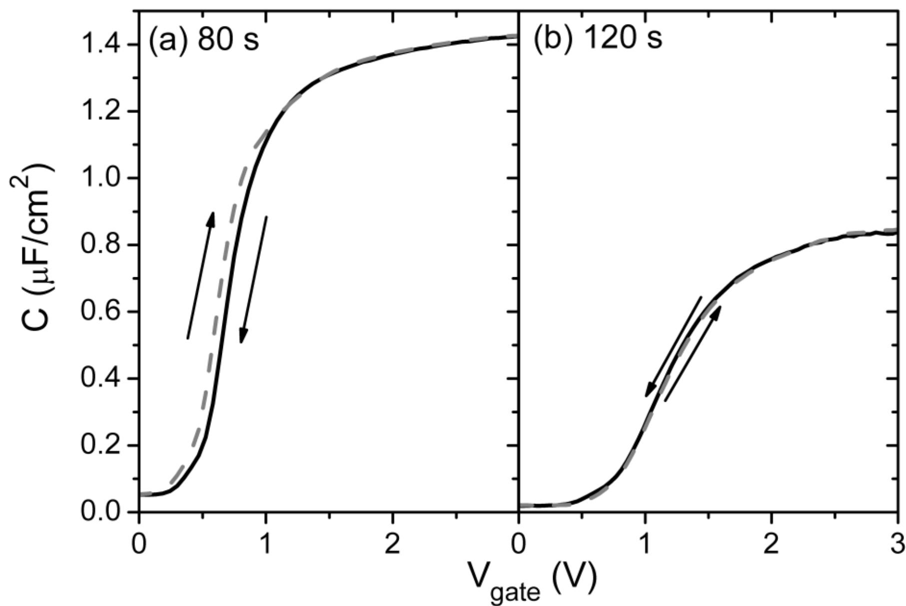

Figure V.27: C-V_{gate} hysteresis curves for (a) 80 s of Gd sample and (b) 120 s of Gd with 100 s of plasma oxidation at 10 kHz after FGA at 400 ºC.

inversion and back again. These characteristics show a small hysteresis of only 80 mV for the 80 s Gd sample (Figure V.27(a)) and an almost negligible value for the 120 s Gd sample (around 15 mV) (Figure V.27(b)). These small values are similar or lower than those reported in other works.[44,49,50] This suggests that either the trap density is low (because the traps were passivated with the FGA) or that the traps remain charged or discharged during the voltage sweep. In any case, this is a positive result for device applications. Besides, for the thinner sample, measurements of conductance and flatband voltage transients were performed in order to characterize possible trapping mechanisms. No transients were observed for both techniques indicating minimal trapping, which is in agreement with the fact that the sample presents such low hysteresis.

Finally, almost no frequency dispersion of the C-V_{gate} characteristics is observed for the thinner sample, as it is represented in left hand side of Figure V.29. These structures only show a small drop in the accumulation capacitance value at 1 MHz, due to the coupled effect of the high conductance (higher than 1 S/cm^2 for V_{gate} equal or higher than 1 V) and the substrate series resistance.[43,50] The capacitance drop could be corrected by using a three-element circuit model.[51] Besides, from the G-V_{gate} curves and using the conductance method, it can be obtained that the D_{it} decreases slightly as the measurement frequency is increased, from 5×10^{11} eV^{-1}cm^{-2} at 1 kHz to

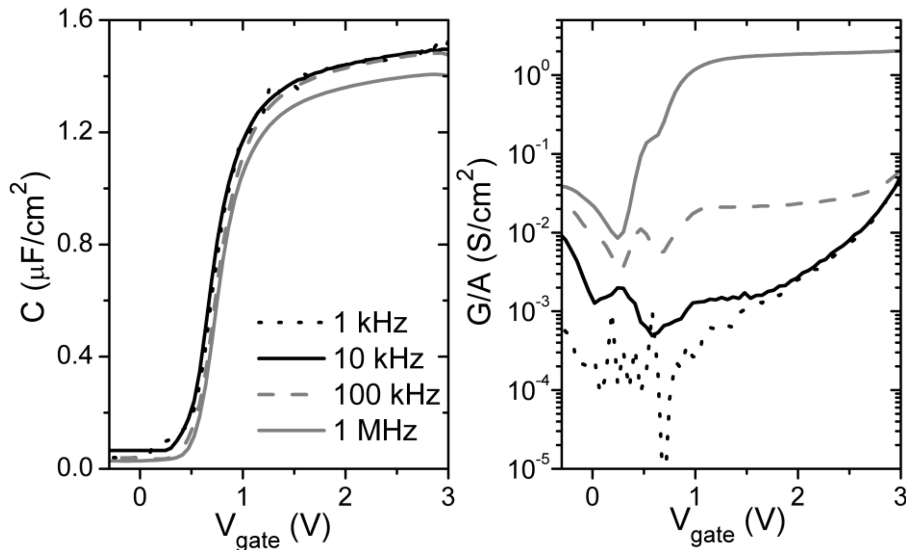

Figure V.29: C-V_{gate} and G-V_{gate} curves measured at different frequencies after FGA at 400 ºC for the sample with 80 s of Gd oxidized during 100 s with 20 W of *rf* power.

3×10^{11} $eV^{-1}cm^{-2}$ at 1 MHz, This means that most interface traps are able to respond even at moderately high frequencies.

From the EOT of the thinner sample (2.2 nm) and assuming a 6.1 nm thick Gd_2O_3 film (the same of the Figure V.12(a) because there is an 80 s of metal deposition) a κ_{eff} of about 11 is obtained. This value is calculated supposing that there is no interfacial layer. This κ value of 11 for Gd_2O_3 is lower than expected, around 15.6'7 But, according the observed $GdSiO_x$ formation due to the intermixing of the oxygen deficient GdO_x and the Si substrate, the κ value of the total gate stack would be lower compared to the binary oxide. In any case, this value confirms that with this two-step method a reasonable Gd_2O_3 (with a silicate--like interfacial layer) can be achieved with good electrical characteristics.

2.4.- Electrical characterization of optimized MIS devices with plasma oxidized Sc_2O_3

In this section, MIS capacitors were fabricated with the evaporated SiO_x as FOX and with Sc_2O_3 as dielectric with the two-step method. Here, only the best conditions obtained for Gd_2O_3 and discussed in former sections were repeated with Sc_2O_3 in order

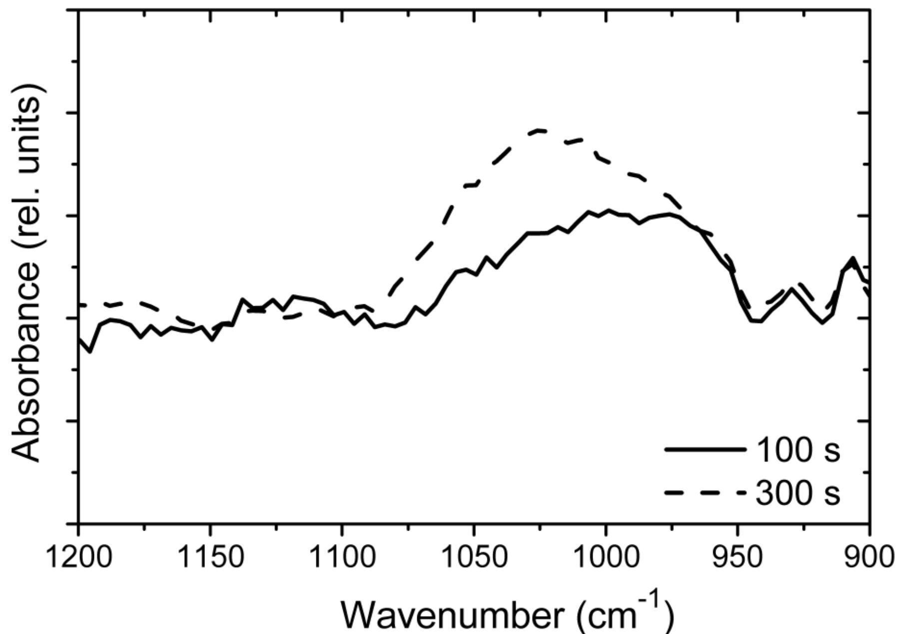

Figure V.30: FTIR absorbance spectra for samples with 80 s of Sc and plasma oxidation duration of 100 and 300 s before the FGA.

to check the possibility of achieving MIS devices with good electrical characteristics using this high κ material. Prior to this MIS capacitors manufacture, FTIR samples were fabricated with different oxidation time aiming to study the interface with Si. Thus, 80 s of Sc was deposited with HPS in an Ar atmosphere (at 30 W and 0.50 mbar). Subsequently, the oxidation was performed during 100 and 300 s at 20 W and 0.50 mbar in an Ar/O_2 plasma. Both processes were carried out at room temperature.

In Figure V.30 is represented the FTIR absorbance spectra in the range of 1200-900 cm^{-1} for the samples with 80 s of Sc oxidized during 100 and 300 s before the FGA. These samples have a band associated to substoichiometric SiO_x located around 1000-1020 cm^{-1}, greater for the sample with higher oxidation time. This points out to a regrowth of SiO_x at the interface between the high κ and the Si during the oxidation process, higher as the oxidation duration is increased. The displacement of the peak as compared with the stoichiometric SiO_2 position (at 1076 cm^{-1}) indicates either a stressed or silicon rich SiO_x (or most likely, both). These results are similar to those obtained for Gd_2O_3 in Figure V.19.

To check the thermal stability of this interface these samples were processed with consecutive FGAs at 300 and 450 ºC for 20 min. After each FGA, samples were measured by FTIR and the spectra are presented in Figure V.31 for the sample with the

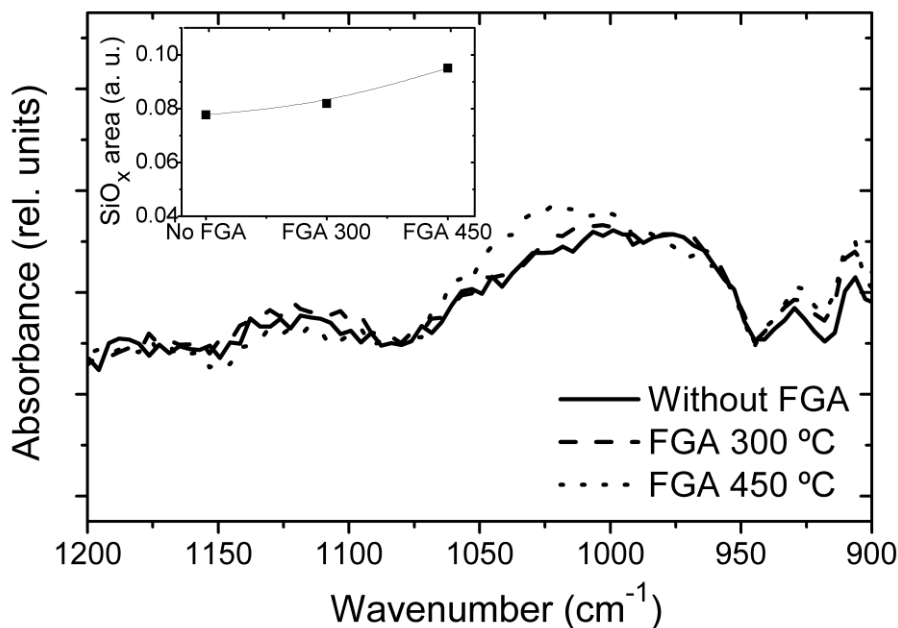

Figure V.31: FTIR spectra of the Sc_2O_3 sample oxidized during 100 s before and after the FGA at 300 and 450 ºC. Inset: SiO_x band area as a function of the FGA.

lower oxidation duration. There, no significant differences can be observed. The SiO_x band increases slightly for the sample with a FGA performed at 450 ºC, as the inset of this figure shows. This indicates that the regrowth of SiO_x at the interface is not excessive after the temperature treatments. Similar results were also obtained for the sample with the longer oxidation time.

HRTEM images for both samples oxidized during different time and after the FGA at 450 ºC are represented in Figure V.32. A two layers stacked structure could be observed for both samples: one lighter over the Si, and a darker one on top. The total thickness is 3.6 nm for both samples. It is important to highlight that for the Gd case, 80 s of deposited Gd provides a 6.1 nm thick GdO_x layer (after oxidation), as it was commented before. In the case of Sc, the thickness is reduced to 3.6 nm, meaning a lower Sc growth rate. Besides, the thicknesses of the interlayer are 1.0 nm and 1.6 nm for the shorter and longer oxidation durations, respectively. As it was explained for the Gd case, the most likely hypothesis is that a silicate formation is also taking place here.

After these FTIR and TEM results, the fabrication of MIS capacitors was carried out with the shorter oxidation time, 100 s, in order to ensure a lower interlayer thickness. 25 nm of Pt were used as the top contact while the bottom one was 50 nm of Ti/100 nm of Al. Around 200 nm of evaporated SiO_x was used as FOX. The sample was measured before and after the FGA at 300 ºC.

The C-V_{gate} curves for the ScO_x devices, measured at 10 kHz and before and after the FGA at 300 ºC, are represented in Figure V.33. The curves show a slight decrease

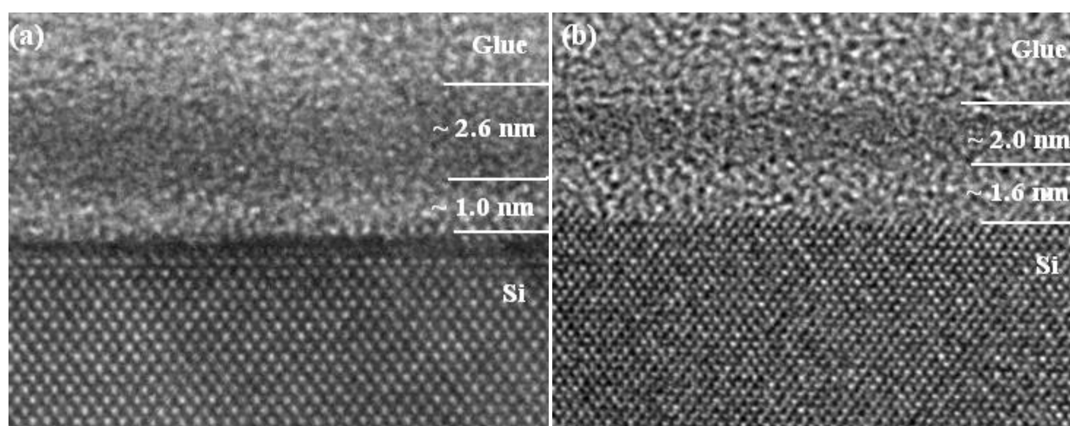

Figure V.32: Cross-sectional HRTEM images of the ScO_x samples with 80 s of Sc and plasma oxidation carried out during (a) 100 s and (b) 300 s after FGA at 450 ºC.

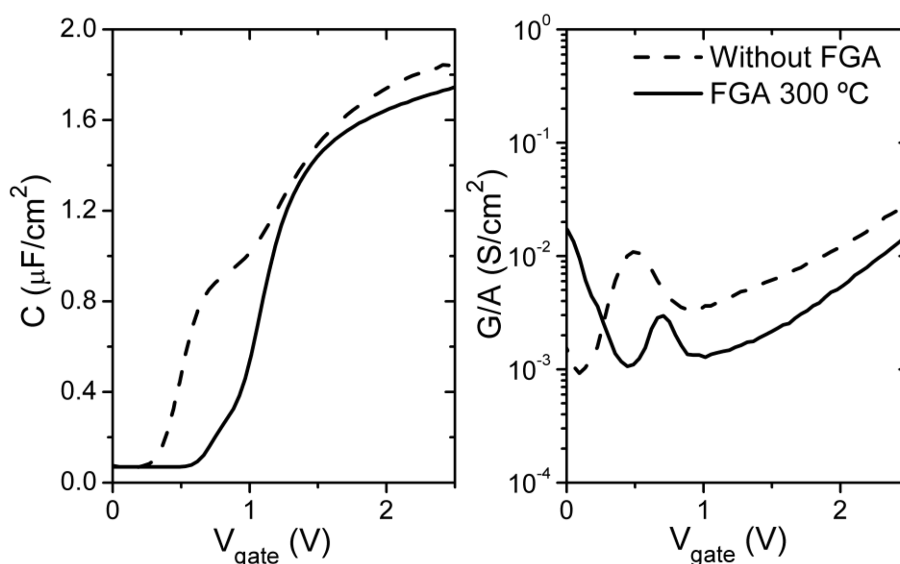

Figure V.33: C and G as a function of V_{gate} for samples with 80 s of Sc and an oxidation of 100 s before (dashed lines) and after the FGA at 300 ºC (solid lines).

for the accumulation capacitance (the EOT is increased from 1.5 to 1.6 nm) after the FGA at 300 ºC. D_{it} value obtained from the conductance method is reduced from ~4×10^{12} $eV^{-1}cm^{-2}$ before the FGA to ~7×10^{11} $eV^{-1}cm^{-2}$ after the temperature annealing. This D_{it} reduction is also explained observing the hump in depletion in the C-V_{gate} characteristic that is greatly reduced after the FGA. This indicates the need of performing the FGA to the Sc_2O_3 samples to improve the interface quality by hydrogen passivation, as it was also observed for the Gd case. Besides, the annealed curve is not displaced in voltage as compared with the unannealed one, thus it can be concluded that this dielectric is stable with the temperature annealing. The same behavior was obtained for Gd_2O_3 grown with the same conditions. Since the EOT is 1.6 nm and given that the film is 3.6 nm thick (obtained with TEM), a κ value of around 9 is obtained. This value is lower than the expected value of Sc_2O_3 (around 13) but it is important to highlight that, again, the presence of the silicate would reduce the effective κ value of the structure. So, this confirms the silicate formation explained before.

Figure V.34 shows the J-V_{gate} characteristics for theSc_2O_3 sample. A value of the leakage current of ~10^{-3} A/cm^2 at a gate voltage of 2 V is obtained before and after the FGA. For a 1.6 nm thick SiO_2 device, the interpolated J at 2 V would be around

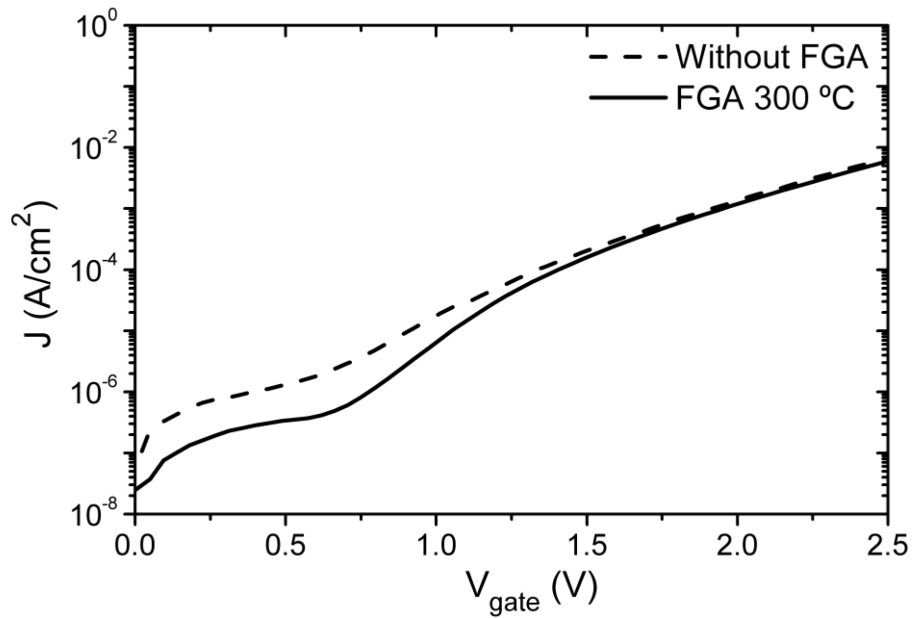

Figure V.34: J vs V_{gate} for the samples with Sc deposited for 80 s and a plasma oxidation for 100 and 300 s before and after the FGA at 300 ºC.

10^2 A/cm^2, according reference,[47] five orders of magnitude higher that the value obtained here. Thus, this density of current is low for a sample with an EOT of ~1.6 nm and acceptable for MOSFETs applications.

Summarizing, Sc_2O_3 MIS devices with an EOT of 1.6 nm, moderate D_{it} and reasonable current density have been fabricated with the two-step method by means of HPS.

V.3.- SUMMARY AND CONCLUSIONS

The two-step method developed in this chapter for obtaining Gd_2O_3 and Sc_2O_3 as high κ dielectric for MIS applications was been successfully demonstrated. For Gd_2O_3, a complete and wide study was carried out, obtaining an amorphous and stoichiometric dielectric film with good electrical characteristics: an EOT of 2.2 nm was obtained with low interface trap density (~2×10^{11} eV^{-1}cm^{-2}), reasonable leakage current density (~10^{-3} A/cm^2), low hysteresis (~80 mV) and almost negligible frequency dispersion. The films that were not completely oxidized presented an interfacial formation of a $GdSiO_x$ after the FGA.

For MIS devices with amorphous Sc_2O_3, a low EOT of only 1.6 nm was achieved, with moderate D_{it} (~7×10^{11} $eV^{-1}cm^{-2}$) and reasonable leakage current (~10^{-3} A/cm^2). As in the Gd case, a silicate formation at the interface between the Sc_2O_3 and the Si was observed.

In both cases, the silicate formation did not seriously compromise the MIS performance.

Therefore, once the binary oxides were studied obtaining good electrical characteristics, we were able to continue with the next step: to fabricate MIS devices with gadolinium scandate from metallic targets. The objective is to use the higher κ value of this material[52-54] as a benefit in the improvement of the capacitors performance.

REFERENCES

[1] K. Yamamoto, S. Hayashi, M. Kubota, M. Niwa. "*Effect of Hf metal predeposition on the properties of sputtered HfO_2/Hf stacked gate dielectrics*". Appl. Phys. Lett., 81, 2053 (2002).

[2] Y. Hoshino, Y. Kido, K. Yamamoto, S. Hayashi, M. Niwa. "*Characterization and control of the HfO_2/Si(001) interfaces*". Appl. Phys. Lett., 81, 2650 (2002).

[3] K. Yamamoto, S. Hayashi, M. Niwa, M. Asai, S. Horii, H. Miya. "*Electrical and physical properties of HfO_2 films prepared by remote plasma oxidation*". Appl. Phys. Lett., 83, 2229 (2003).

[4] G. He, Q. Fang, M. Liu, L. Q. Zhu, L. D. Zhang. "*The structural and interfacial properties of HfO_2/Si by the plasma oxidation of sputtered metallic Hf thin films*". J. Crys. Growth, 268, 155 (2004).

[5] G. He, Q. Fang, L. Zhu, M. Liu, L. Zhang. "*The structure and thermal stability of TiO_2 grown by the plasma oxidation of sputtered metallic Ti thin films*". Chem. Phys. Lett., 395, 259 (2004).

[6] J. A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang, C. Adelmann, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V. V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervost, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M. Jurczak, J. Van Houdt, D. J. Wouters. "*High-k dielectrics for future generation memory devices*". Microelectron. Eng., 86¸ 1789 (2009).

[7] J. Kwo, M. Hong, A. R. Kortan, K. L. Queeney, Y. J. Chabal, R. L. Opila Jr., D. A. Muller, S. N. G. Chu, B. J. Sapjeta, T. S. Lay, J. P. Mannaerts, T. Boone, H. W. Krautter, J. J. Krajewski, A. M. Sergnt, J. M. Rosamilia. "*Properties of high k gate dielectrics Gd_2O_3 and Y_2O_3 for Si*". J. Appl. Phys., 89, 3929 (2001).

[8] R. D. Shannon. "*Dielectric polarizabilities of ions in oxides and fluorides*". J. Appl. Phys., 73, 348 (1993).

[9] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, A. M. Sergent. "*Epitaxial cubic gadolinium oxide as a dielectric for gallium arsenide passivation*". Science, 283, 1897 (1999).

[10] M. Hong, J. Kwo, S. N. G. Chu, J. P. Mannaerts, A. R. Kortan, H. M. Ng, A. Y. Cho, K. A. Anselm, C. M. Lee, J. I Chyi. "*Single-crystal GaN/Gd2O3/GaN heterostructure*". J. Vac. Sci. Technol. B, 20, 1274 (2002).

[11] W. H. Chang, C. H. Lee, P. Chang, Y. C. Chang, Y. J. Lee, J. Kwo, C. C. Tsai, J. M. Hong, C. H. Hsu, M. Hong "*High κ dielectric single-crystal monoclinic Gd_2O_3 on GaN with excellent thermal, structural, and electrical properties*". J. Crystal Growth, 311, 2183 (2009).

[12] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Gadolinium scandate by high-pressure sputtering for future generations of high-k dielectrics*". Semicond. Sci. Technol., 28, 085004 (2013).

[13] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Nano-laminate vs. direct deposition of high permittivity gadolinium scandate on silicon by high pressure sputtering*". Thin Solid Films, 593, 62 (2015).

[14] E. H. Nicollian, A. Goetzberger. "*The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique*". Bell Syst. Tech. J., 46, 1055 (1967).

[15] D. V. Lang. "*Deep level transient spectroscopy: A new method to characterize traps in semiconductors*". J. Appl. Phys., 45, 3023 (1974).

[16] R. W. B. Pearse, A. G Gaydon. "*The identification of molecular spectra*". 4th edition. John Wiley & Sons, Inc., New York (1976).

[17] G. Norlén. "*Wavelengths and energy levels of Ar I and Ar II based on new interferometric measurements in the region 3400-9800 Ǻ*". Phys. Scr., 8, 249 (1973).

[18] B. Wende, "*Optical transition probabilities of the configurations $3p^5 4s$-$3p^5 5p$ of Argon I,*" Zeitschrift für Physik, 213, 341 (1968).

[19] W. F. Meggers, C. H. Corliss, B. F. Scribner. "*Tables of spectral-line intensities, Part I – Arranged by elements, Part II – Arranged by wavelengths, Natl. Bur. Stand. Monograph 145*". Natl. Bur. Stand. U.S., 600 (1975).

[20] S. Wolf. "Microchip manufacturing". Lattice Press. Sunset Beach, California (2004).

[21] S. Wolf, R. N. Tauber. "Silicon processing for the VLSI era. Volume 1: Process technology". Lattice Press. Sunset Beach, California (1986).

[22] C. E. Moore. "*Selected tables of atomic spectra, atomic energy levels and mutilplet tables – O I*". Natl. Bur. Stand., U.S., 33, (1976).

[23] B. Ahmed, J. Verges. "*Extension de l'étude de spectre d'arc de scandium*". Physica, 92C, 113 (1977).

[24] M. P. Singh, C. S. Thakur, K. Shalini, S. Banerjee, N. Bhat, S. A. Shivashankar. "*Structural, optical and electrical characterization of gadolinium oxide films deposited by low-pressure metalorganic chemical vapor* deposition". J. Appl. Phys., 96, 5631 (2004).

[25] G. D. Wilk, R. M. Wallace, J. M. Anthony. "*High-κ gate dielectrics: Current status and materials properties considerations*". J. Appl. Phys., 89, 5243 (2001).

[26] G. He, L. Zhu, Z. Sun. Q. Wan, L. Zhang. "*Integrations and challenges of novel high-k gate stacks in advanced CMOS technology*". Prog. Mater. Sci., 56, 475 (2011).

[27] D. Raiser, J. P. Deville. "*Study of XPS photoemission of some gadolinium compounds*". J. Electron Spectrosc. Relat. Phenom., 57, 91 (1991).

[28] Y. Uwamino, Y. Ishizuka, H. Yamatera. "*X-ray photoelectron spectroscopy of rare-earth compounds*". J. Electron Spectrosc. Relat. Phenom., 34, 67 (1984).

[29] Y. L. Li, N. F. Chen, J. P. Zhou, S. L. Song, L. F. Liu, Z. G. Yin, C. L. Cai. "*Effect of the oxygen concentration on the properties of Gd_2O_3 thin films*". J. Cryst. Growth, 265, 548 (2004).

[30] S. A. Vitale, P. W. Wyatt, C. J. Hodson. "*Plasma-enhanced atomic layer deposition and etching of high-k gadolinium oxide*". J. Vac. Sci. Technol. A, 30, 01A130 (2012).

[31] S. J. Schneider, J. L. Waring. "*Phase equilibrium relations in the Sc_2O_3-Ga_2O_3 system*". J. Res. Natl. Stand. Sec. A, 67A, 19 (1963).

[32] P. C. Feijoo, M. A. Pampillón, E. San Andrés, M. L. Lucía. "*Optimization of scandium oxide growth by high pressure sputtering on silicon*". Thin Solid Films, 526, 81 (2012).

[33] J. R. Hauser, K. Ahmed. "*Characterization of ultra-thin oxides using electrical C-V and I-V measurements*". AIP Conf. Proc., 449, 235 (1998).

[34] P. G. Pai, S. S. Chao, V. Takagi, G. Lucovsky. "*Infrared spectroscopic study of SiO_x films produced by plasma enhanced chemical vapor deposition*". J. Vac. Sci. Technol. A, 4, 689 (1986).

[35] R. A. B. Devine. "*Structural nature of the Si/SiO_2 interface through infrared spectroscopy*". Appl. Phys. Lett., 68, 3108 (1996).

[36] E. Monroy, F. Calle, R. Ranchal, T. Palacios, M. Verdú, F. J. Sánchez, M. T. Montojo, M. Eickhoff, F. Omnè, Z. Bougrioua, I. Moerman. "*Thermal stability of Pt- and Ni-based Schottky contacts on GaN and $Al_{0.31}Ga_{0.69}N$*". Semicond. Sci. Technol., 17, L47 (2002).

[37] H. Ono, T. Katsumata. "*Interfacial reactions between thin rare-earth-metal oxide films and Si substrates*". Appl. Phys. Lett., 78, 1832 (2001).

[38] A. Sakai, S. Sakashita, M. Sahashita, Y. Yasuda, S. Zaima, S. Miyazaki. "*Praseodymium silicate formed by postdeposition high-temperature annealing*". Appl. Phys. Lett., 85, 5322 (2004).

[39] C. J. Choi, M. G. Jang, Y. Y. Kim, M. S. Jun, T. Y. Kim, M. H. Song. "*Electrical and structural properties of high-k Er-silicate gate dielectric formed by interfacial reaction between Er and SiO_2 films*". Appl. Phys. Lett., 91, 012903 (2007).

[40] D. J. Lichtenwalner, J. S. Jur, A. I. Kingon, M. P. Agustin, Y. Yang, S. Stemmer, L. V. Goncharova, T. Gustafsson, E. Garfunkel. "*Lanthanum silicate gate dielectric stacks with subnanometer equivalent oxide thickness utilizing an interfacial silica consumption reactions*". J. Appl. Phys., 98, 024314 (2005).

[41] S. V. Elshocht, C. Adelmann, P. Lehnen, S. De Gent. "*Equivalent oxide thickness reduction for high-k gate stacks by optimized rare-earth silicate reactions*". Electrochem. Solid-State Lett., 12, G17 (2009).

[42] M. Houssa, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, M. M. Heyns. "*Electrical properties of high-κ gate dielectrics: Challenges, current issues, and possible solutions*". Mater. Sci. Eng. R, 51, 37 (2006).

[43] P. M. Tirmali, A. G. Khairnar, B. N. Joshi, A. M. Mahajan. "*Structural and electrical characteristics of RF-sputtered HfO_2 high-k based MOS capacitors*". Solid-State Electron., 62, 44 (2011).

[44] D. Panda, T. Y. Tseng. "*Growth, dielectric properties, and memory device applications of ZrO2 thin films*". Thin Solid Films, 531, 1 (2013).

[45] S. Kaya, E. Yilmaz. "*A comprehensive study on the frequency-dependent electrical characteristics of Sm2O3 MOS capacitors*". IEEE Trans. Electron Devices, 62, 980 (2015).

[46] E. Lipp, H. J. Osten, M. Eizenberg. "*The thermal stability of Pt/epitaxial Gd_2O_3/Si stacks and its dependence on heat treatment ambient*". J. Appl. Phys., 106, 113505 (2009).

[47] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, L. O. Shih-Hsien, G. A. Sai-Halasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind, H. S. Wong. "*CMOS scaling into the nanometer regime*". Proc. IEEE, 85, 486 (1997).

[48] F. C. Chiu. "*A review on conduction mechanisms in dielectric films*". Advances in Materials Science and Engineering, 2014, 578168 (2014).

[49] Q. Q. Sun, A. Laha, S. J. Dong, D. W. Zhang, H. J. Osten, A. Fissel. "*Effective passivation of slow interface states at the interface of single crystalline Gd_2O_3 and Si(100)*". App. Phys. Lett., 92, 152908 (2008).

[50] T. M. Pan, C. S. Liao, H. H. Hsu, C. L. Chen, J. D. Lee, K. T. Wang, J. C. Wang. "*Excellent frequency dispersion of thin gadolinium oxide high-k gate dielectrics*". Appl. Phys. Lett., 87, 262908 (2005).

[51] E. San Andrés, L. Pantisano, J. Ramos, P. J. Roussel, B. J. O'Sullivan, M. Toledano-Luque, S. DeGendt, G. Groeseneken. "*Accurate gate impedance determination on ultraleaky MOSFETs by fitting to a three-lumped-parameter model at frequencies from CD to RF*". IEEE Trans. Electron Devices, 54, 1705 (2007).

[52] C. Zhao, T. Witters, B. Brijs, H. Bender, O. Richards, M. Caymax, T. Heeg, J. Schubert, V. V. Afanas'ev, A. Stesmans, D. G. Schlom. "*Ternary rare-earth metal oxide high-k layers on silicon oxide*". Appl. Phys. Lett., 86, 132903 (2005).

[53] J. M. J. Lopes, E. Durgun Özben, M. Roeckerath, U. Littmark, R. Luptak, St. Lenk, M. Luysberg, A. Besmehn, U. Breuer, J. Schubert, S. Mantl. "*Amorphous ternary rare-earth gate oxide for future integration in MOSFETs*". Microelectron, Eng., 86, 1646 (2009).

[54] K. Fröhlich, J. Fedor, I. Kostic, J. Manka, P. Ballo. "*Gadolinium scandate: next candidate for alternative gate dielectric in CMOS technology?*". J. of Elect. Eng, 62, 54 (2011).

Chapter VI:
Gadolinium scandate

Obtaining a high κ film of $Gd_{2-x}Sc_xO_3$ by means of HPS from metallic Gd and Sc targets was one of the main objectives of this thesis and it is analyzed in this chapter. As stated in the motivation of this thesis, gadolinium scandate is a promising candidate for high κ applications due to its favorable properties, such as a high permittivity value (between 20 and 30, depending on the lattice direction and the composition),[1-3] a large bandgap (higher than 5 eV),[4-6] large conduction and valence band offsets to Si (around 2-2.5 eV)[5] and an excellent thermodynamic stability on Si (up to 1000 ºC).[7,8]

To accomplish the production of $Gd_{2-x}Sc_xO_3$ by HPS from metallic targets, first it was necessary to study the grown properties of Gd_2O_3 and Sc_2O_3 from Gd and Sc and a subsequent plasma oxidation. This was done in the former chapter. Following Feijoo *et al.* works,[9,10] that used these binary oxides to grow a nanolaminate to produce the ternary material after a temperature annealing, in this chapter a similar process was studied. First, a nanolaminate of Gd and Sc was grown in an Ar atmosphere with HPS using the best conditions obtained in chapter V. Afterwards, an *in situ* plasma oxidation was carried out in order to oxidize the metallic nanolaminate film. Finally, a forming gas anneal (FGA) was performed with the aim of producing the intermixing of the nanolaminate and to improve its properties.

GDOS was used to check if having both targets switched on simultaneously affected the plasma, and thus, the growing layer. The films were physically characterized by XPS, FTIR, GIXRD and TEM. MIS devices with field oxide (FOX) and using Pt as gate electrode were fabricated in order to study their electrical characteristics.

VI.1.- EXPERIMENTAL METHOD

$Gd_{2-x}Sc_xO_3$ films were fabricated by means of HPS from metallic Gd and Sc targets. Using the two-step method developed in the last chapter, thin Gd and Sc layers (with a thickness around 0.5 nm) were alternatively deposited in an Ar atmosphere at 30 W. This process was repeated several times in order to obtain thicker films of this nanolaminate of thin Gd and Sc layers. This sequential deposition was achieved without breaking the vacuum of the chamber by means of the mechanized. All targets can be sputtered simultaneously by separate power sources. The moving arm places only one target on top of the sample. Therefore, to obtain compounds from pure targets the only possibility is to produce intermixing of a nanolaminate (in other words, co-sputtering is not possible at the high working pressure of the HPS system). For the depositions of this chapter, two Gd and Sc targets were used, and both were radiofrequency (*rf*) excited continuously during the deposition process. Also, pure Gd and Sc layers were grown to have a comparison. Afterwards, a plasma oxidation was carried out during 100 s in a mixed Ar/O_2 plasma using the Gd target at 20 W for all the samples. The reason of performing the plasma oxidation with the Gd target was because it had been more widely study in chapter V, obtaining good and reliable results. Both processes (the metal deposition and the plasma oxidation) were carried out at 0.50 mbar of pressure and at room temperature. With the aim of modulating the composition of the $Gd_{2-x}Sc_xO_3$ films, the thicknesses of the individual Gd and Sc layers of the nanolaminate were varied by adjusting the sputtering duration for each step. This chapter will be focused on the results obtained from a gadolinium scandate with an intermediate composition.

Besides, in order to produce the ternary material from this nanolaminate and gain insight on the thermal behavior, a temperature annealing was consecutively performed from 300 to 700 ºC in a forming gas atmosphere.

VI.2.- RESULTS AND DISCUSSION

2.1.- Plasma characterization

GDOS emission spectra were measured with the spectrometer system in the range from 200 to 600 nm. Figure VI.1(a) and Figure VI.1(b) present the optical emission spectra of the sputtered Gd in an Ar atmosphere at 30 W and at 0.50 mbar when the Sc *rf* power is switched off and on, respectively. Only wavelengths ranging between 200 to 400 nm are represented here because the main emission lines of Gd I and Gd II are in this range,[11] as it is marked in this figure. Both spectra are similar in the number and intensity of the optical emission lines, regardless of whether the Sc *rf* power is switched off or on. No peaks can be related to Sc even when the power of this target is switched on during the deposition. The same effect was observed in the rest of the range (from 400 to 600 nm), but as no relevant information can be extracted from there, it is not presented. Besides, the presence of the typical contaminants from atmosphere, H_2O (a band located around 310 and 320 nm)[12] or N_2 (the most important lines at 336 and

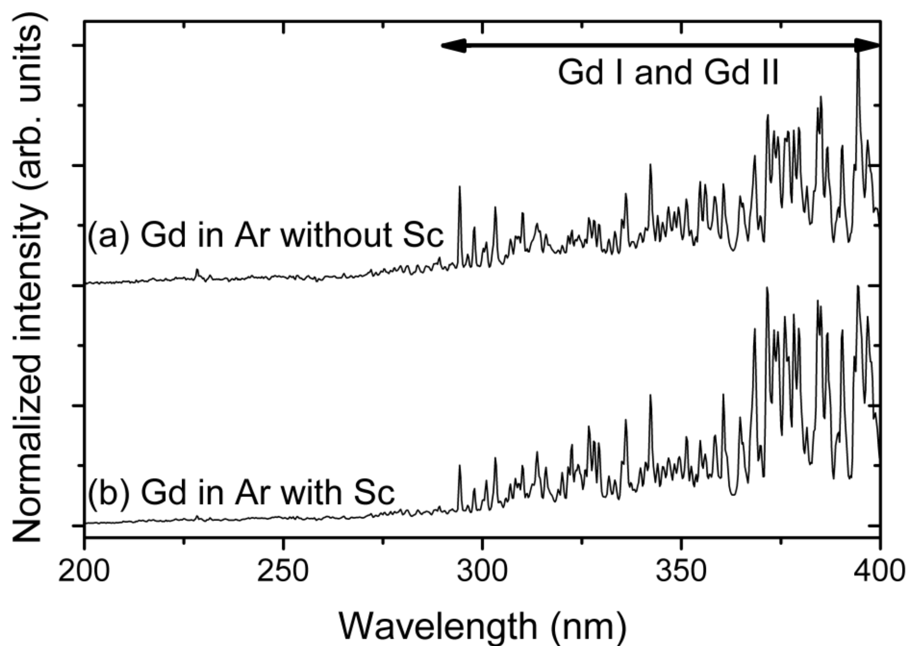

Figure VI.1: GDOS emission spectra of sputtered Gd in an Ar plasma at 30 W when the Sc *rf* power is (a) switched off and (b) on. The range where the most important lines of Gd I and Gd II are located is marked in the figure.

358 nm)[12], are not detected in the plasma, pointing out to a high pureness of the sputtering atmosphere. This is important to achieve a high reproducibility of the processes and a good quality of the growing films. Thus, it can be concluded that there is not appreciable contamination of Sc in the Gd plasma and therefore, the growing film would be almost Sc-free when the Gd is being sputtered, despite both targets were switched on simultaneously during the Gd deposition.

Figure VI.2 presents the plasma spectra of sputtered Sc when the Gd *rf* power is also switched off and on. The same wavelength range is shown in order to emphasize the differences with respect to Figure VI.1. In this range, intense emission lines of non ionized and singly ionized Sc, Sc I and Sc II, respectively, are located.[13-15] These lines are represented in this Figure VI.2 with dashed lines (belonging to Sc I) and dotted lines (related to Sc II). The rest of the lines that appear in these spectra can be associated to Ar I and Ar II,[16,17] necessary for the Sc extraction. Again, no traces of H_2O and N_2 are detected in the plasma, neither Gd emission lines, pointing to a formation of a Gd-free Sc layer.

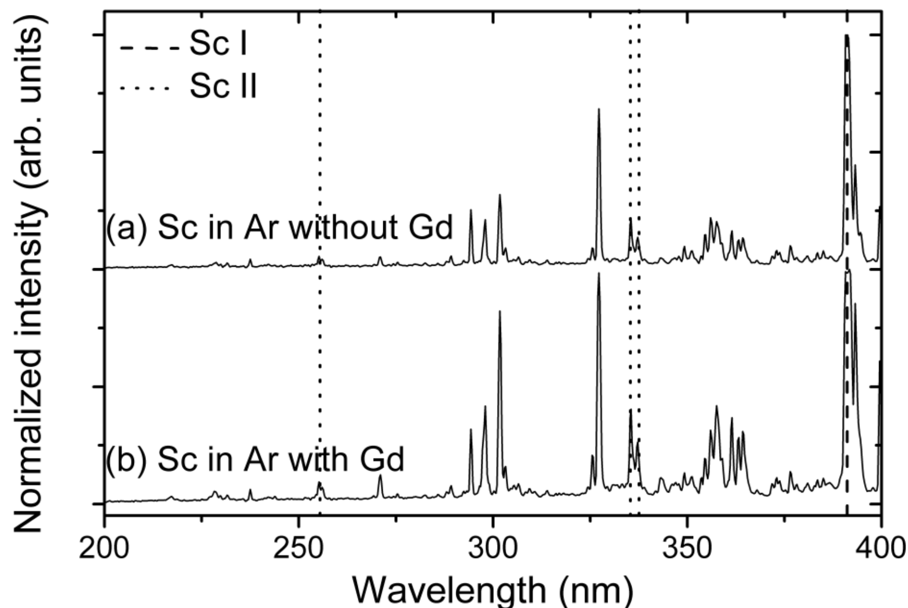

Figure VI.2: GDOS emission spectra of sputtered Sc in an Ar atmosphere at 30 W when the Gd *rf* power is (a) switched off and (b) on. Sc I and Sc II lines are marked in the figure with dashed and dotted lines, respectively. The rest of the peaks presented in the spectra are related to Ar I and Ar II.

Therefore, it is possible to deposit a nanolaminate of metallic Gd and Sc layers in an Ar atmosphere using HPS, and each step is free of contamination from the other target, even when both targets are been sputtered simultaneously.

2.2.- Physical characterization

The chemical composition of the samples was measured by means of XPS. $Gd_{2-x}Sc_xO_3$ (grown to have an intermediate composition) and pure Gd_2O_3 and Sc_2O_3 samples were analyzed after a FGA at 600 ºC. It is important to remember that in this chapter the pure binary oxides films were deposited with both targets switched on simultaneously. Also in both cases, the oxidation was done with the Gd target. The XPS wide scan of survey spectra obtained for these samples are shown in Figure VI.3. There, it can be seen that the pure Gd_2O_3 sample does not present traces of Sc, in agreement with the former GDOS results that pointed out to a Sc-free Gd layer. In the case of pure Sc_2O_3, a slight peak corresponding to Gd is observed, possibly due to the oxidation process that was carried out with the Gd target. XPS detects surface atoms, and some residual Gd can be sputtered during oxidation. In the former chapter, it was concluded

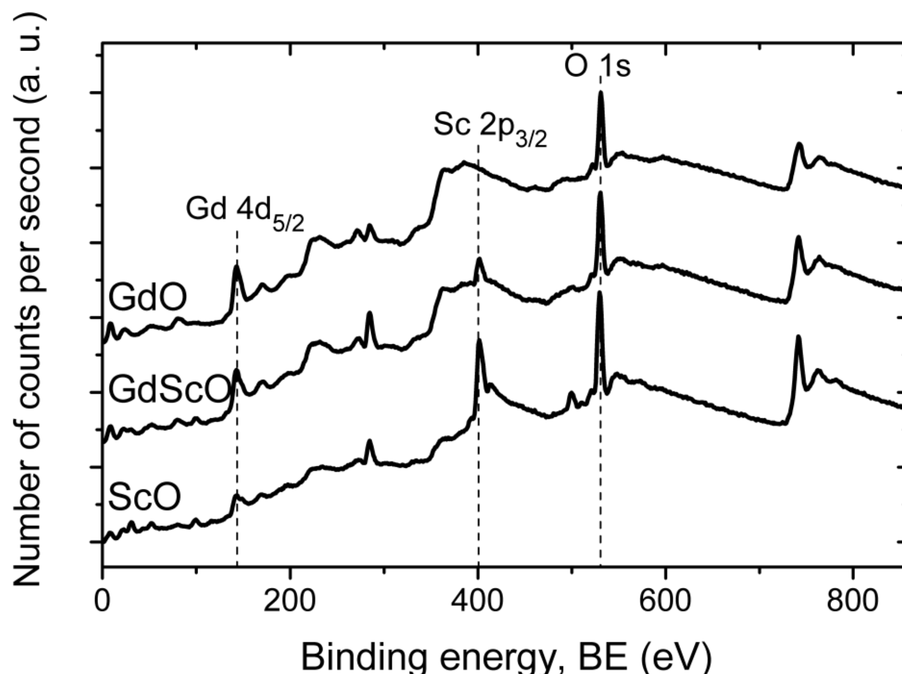

Figure VI.3: XPS wide scan or survey spectra of Gd_2O_3, $Gd_{2-x}Sc_xO_3$ and Sc_2O_3 samples after a FGA at 600 ºC. Gd $4d_{5/2}$, Sc $2p_{3/2}$ and O 1s peaks are marked in the figure.

that the extraction of Gd in a mixed Ar/O_2 atmosphere was small. These XPS results indicate that some Gd is being sputtered, but in a low amount. Focusing on the ternary material, peaks corresponding to Gd and Sc are observed in the grown layer. Besides, all the spectra present a peak related to O 1s.

In order to calculate the chemical bonds and the stoichiometry of the $Gd_{2-x}Sc_xO_3$ layer, high resolution spectrum of the ternary material sample was obtained, as it is presented in Figure VI.4. The spin orbit splitting of the Gd 4d core-level (with components $4d_{5/2}$ and $4d_{3/2}$ located at around 142.2 and 149.1 eV, respectively) are in agreement with reported Gd_2O_3.[18,19] These peaks were similar to those obtained in chapter V. The doublet for the Sc 2p level at about 401.5 eV (for Sc $2p_{3/2}$) and at 406.9 eV (for Sc $2p_{1/2}$) corresponds with Sc_2O_3 as it is stated in other works.[20,21] In the case of O 1s, it is observed an asymmetric peak that is fitted with two components: one lower at 529.6 eV and other higher at 531.5 eV. The first one is related to Sc-O and Gd-O bonds,[20,22] while, the position of the second points to OH^- groups absorbed at the surface of the film. This surface moisture absorption has been also observed in other high κ materials.[23]

This surface related peak makes difficult to determine the oxygen content, hence we will focus on the Sc/Gd ratio and assume that the layer is fully oxidized. The peaks

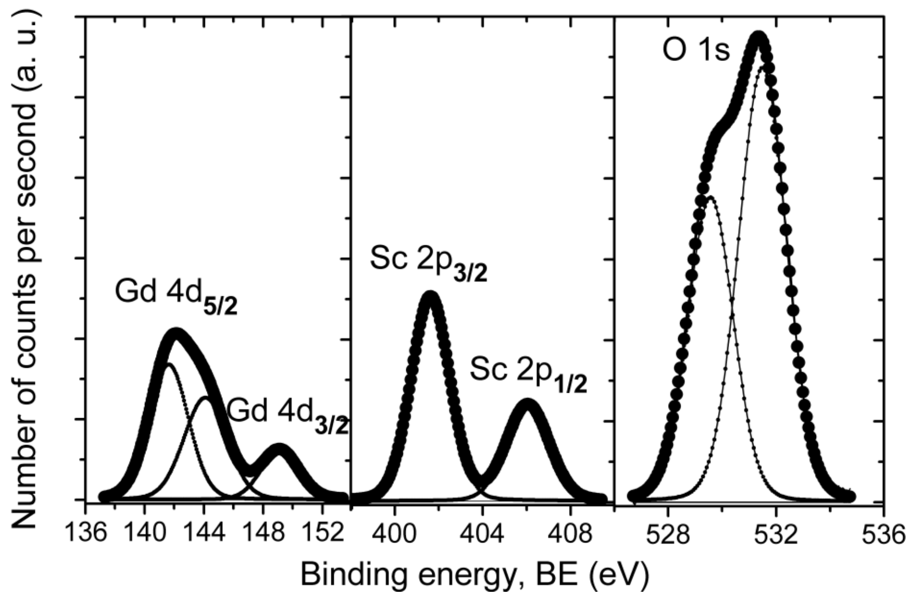

Figure VI.4: High resolution XPS spectrum for $Gd_{2-x}Sc_xO_3$ sample after a FGA at 600 ºC: Gd 4d (left) and Sc 2p (center) doublets and O 1s (right) together with their fits.

used to obtain the composition of the film were Gd 4d and Sc 2p, which produced a Sc/Gd ratio of 1.21 ± 0.03. Therefore, the chemical formula of the intermediate composition layer was $Gd_{0.9}Sc_{1.1}O_3$, gadolinium scandate slightly Sc-rich.

To detect the presence of interfacial SiO_x between the different high κ and the Si substrate it was used FTIR spectroscopy on the as deposited films. In Figure VI.5, it is represented the absorbance spectra from 1200 to 900 cm^{-1} of the $Gd_{0.9}Sc_{1.1}O_3$ film and also the pure binary oxides samples to have a reference. A slight peak centered at around 1040 cm^{-1} and related to substoichiometric SiO_x[24,25] is observed for the pure Gd_2O_3 layer. The area of this peak, which is related to the amount of SiO_x at the interface, is similar to those of the samples analyzed in chapter V. For the pure Sc_2O_3 and the $Gd_{0.9}Sc_{1.1}O_3$ films, there is not a clear peak. In both cases, the band is comparable for these two dielectric layers and is almost negligible and close to the detection limit. In any case, this SiO_x band is slight (if any), meaning that the regrowth of the interfacial oxide is not very significant for the as grown layers.

To study the evolution of the interface with the temperature treatments, in Figure VI.6 is presented the FTIR spectra for the $Gd_{0.9}Sc_{1.1}O_3$ film before and after the FGAs performed at 400 and 600 ºC. In this figure it can be observed a mild increase in

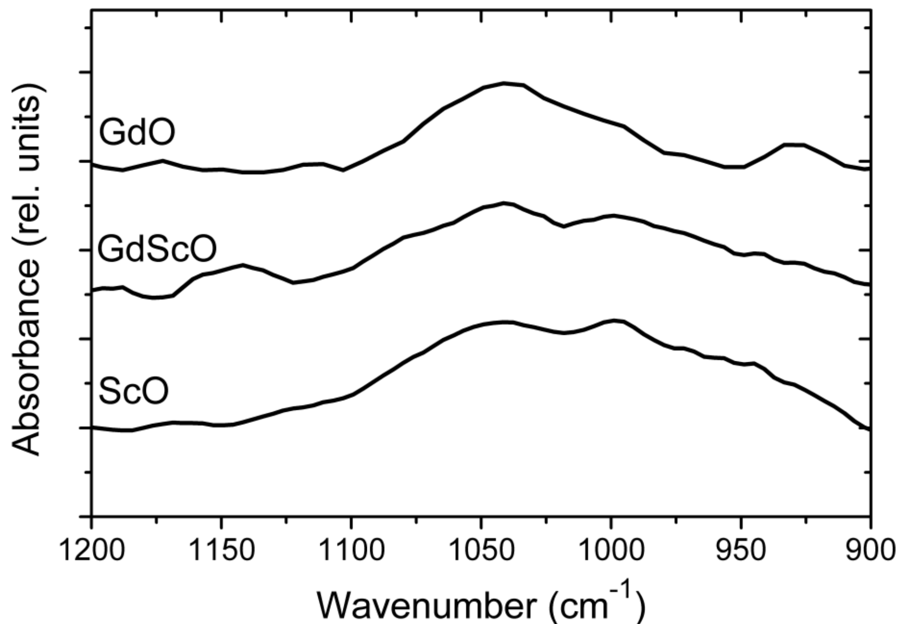

Figure VI.5: FTIR absorbance spectra for the as deposited Gd_2O_3, $Gd_{0.9}Sc_{1.1}O_3$ and Sc_2O_3 samples.

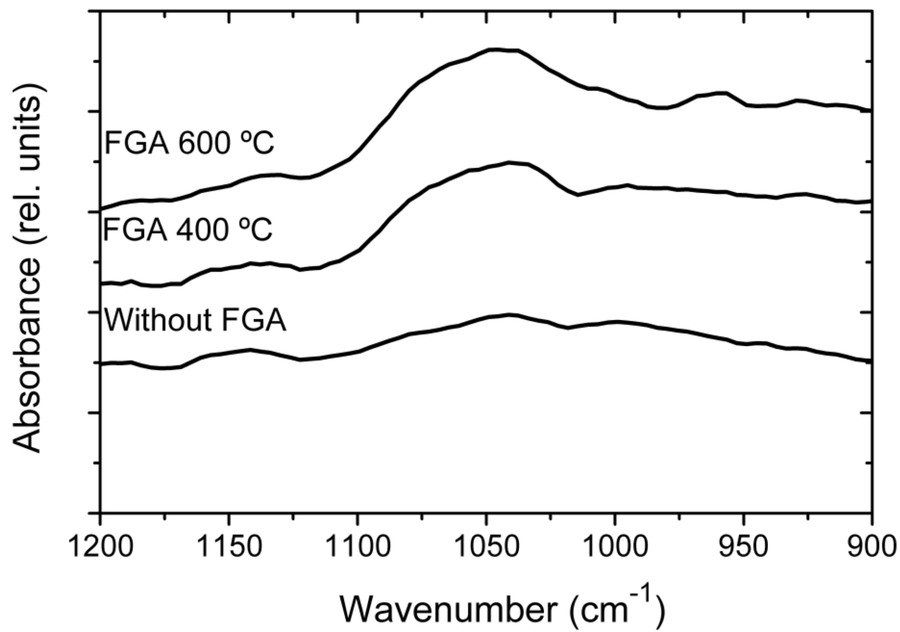

Figure VI.6: FTIR spectra for the $Gd_{0.9}Sc_{1.1}O_3$ film before and after different FGAs.

the area of the band located at ~1040 cm^{-1} and related to SiO_x as the annealing temperature is raised. This points out to a formation of Si-O bonds during the FGA that have the consequence of a slight SiO_x interlayer regrowth.

To find out the atomic arrangement of the $Gd_{0.9}Sc_{1.1}O_3$ film, GIXRD diffraction measurements were performed after the FGA at 600 ºC during 5 min, and the results are represented in Figure VI.7. No diffraction peaks are observed in this figure, pointing out to an amorphous layer, even after the FGA at 600 ºC. Some works3[,8,26] reported a peak located at ~30º due to a Gd-Sc silicate formation for the as deposited samples. In these works, this peak disappeared after an annealing at 1000 ºC. It is interesting to highlight that the sample shown in Figure VI.7 does not present this peak suggesting that there is no appreciable silicate layer or it is amorphous. As it was commented before, the $GdScO_3$ is known to be a material with a good thermodynamic stability with Si up to 1000 ºC. Since a typical microelectronic fabrication process will require low annealing temperatures, the amorphous phase of our $Gd_{0.9}Sc_{1.1}O_3$ film is an interesting property for high κ MIS devices in order to avoid the grain boundaries that are more conductive and increase the leakage current.[27]

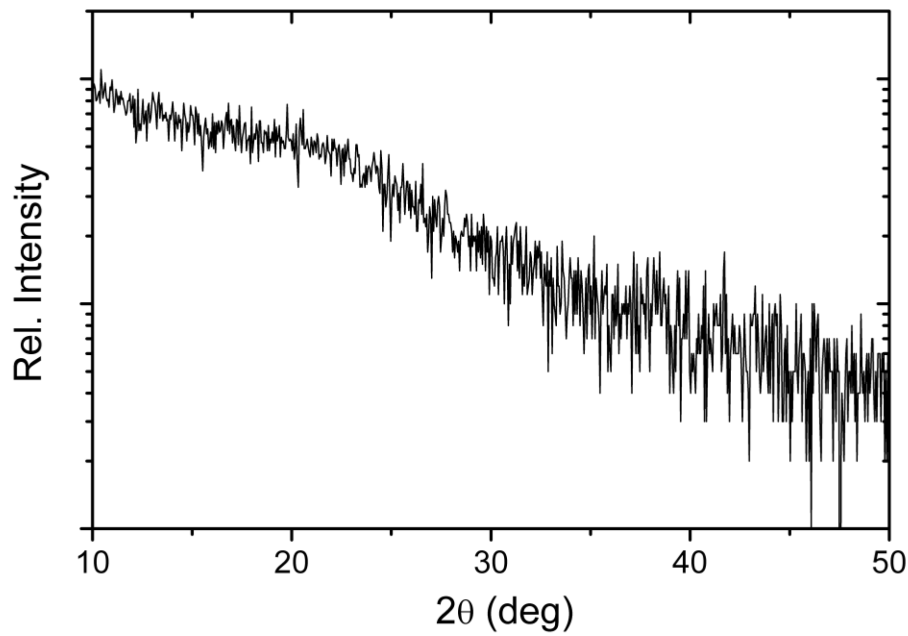

Figure VI.7: Grazing incident XRD spectra of $Gd_{0.9}Sc_{1.1}O_3$ film after a FGA at 600 ºC was performed. No diffraction peaks are observed.

The HRTEM image shown in Figure VI.8 was obtained for the $Gd_{0.9}Sc_{1.1}O_3$ sample after the FGA at 600 ºC. First of all, a stacked structure is observed with two layers over the Si. Both layers are amorphous (as it was shown with the GIXRD results of Figure VI.7) and there are not traces of the presence of a nanolaminate, confirming the intermixing promoted with the temperature explained previously. The lower layer is

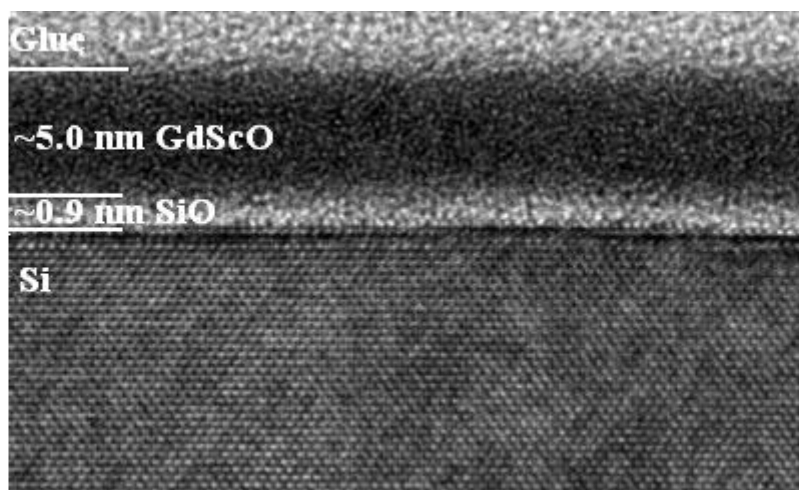

Figure VI.8: HRTEM cross-sectional image of $Gd_{0.9}Sc_{1.1}O_3$ sample obtained after the FGA at 600 ºC.

lighter with a thickness of 0.9 ± 0.1 nm. This is under a darker film 5.0 ± 0.1 nm thick. This top layer is related to amorphous gadolinium scandate formed after the temperature treatment in the forming gas atmosphere. The lower one corresponds to SiO_x, supported by the FTIR results from Figure VI.6 which indicated a slight interlayer regrowth produced after the FGAs. Here, this regrowth can be quantified, and it is only 0.9 nm.

Hence, as a conclusion of this section, a $Gd_{0.9}Sc_{1.1}O_3$ film can be grown with HPS with a low regrowth of interfacial SiO_x layer and in an amorphous phase, even after a FGA at 600 ºC.

2.3.- Electrical characterization

MIS devices with $Gd_{0.9}Sc_{1.1}O_3$ as high κ material were fabricated with evaporated SiO_2 as FOX and using ~25 nm of Pt as gate electrode, in order to avoid the aluminate formation and to study the bare high κ dielectric properties. The backside contact was a stack formed with 50 nm of Ti capped with 100 nm of Al. The capacitors were measured before and after several FGAs at different increasing temperatures from 300 to 700 ºC. The duration of the FGA was 20 min except for the higher temperatures (600 and 700 ºC) that was 5 min.

The area normalized capacitance and conductance measured at 10 kHz as a function of the gate voltage characteristics are depicted in Figure VI.9 before and after representative FGAs. All the $C\text{-}V_{gate}$ curves are free of humps and do not present stretch out, meaning a good quality of the interface.[28] The as deposited sample (in grey solid line) presents the lowest accumulation capacitance. This value increases while the temperature of the FGA is raised (until 600 ºC), as it can be observed in this figure. As the top electrode is Pt, which is a noble metal, this capacitance increase has to be associated to the gadolinium scandate formation. It is important to highlight that this $Gd_{0.9}Sc_{1.1}O_3$ film was obtained from a nanolaminate of metallic Gd and Sc layers followed by a plasma oxidation. Thus, it was necessary to produce the intermixing of those layers to form the high κ gadolinium scandate. According to the $C\text{-}V_{gate}$ results of Figure VI.9, this can be promoted by a low temperature treatment. The same effect was observed in works of Feijoo *et al.*[9,10] that used binary Gd_2O_3 and Sc_2O_3 to form the ternary material after the FGA.

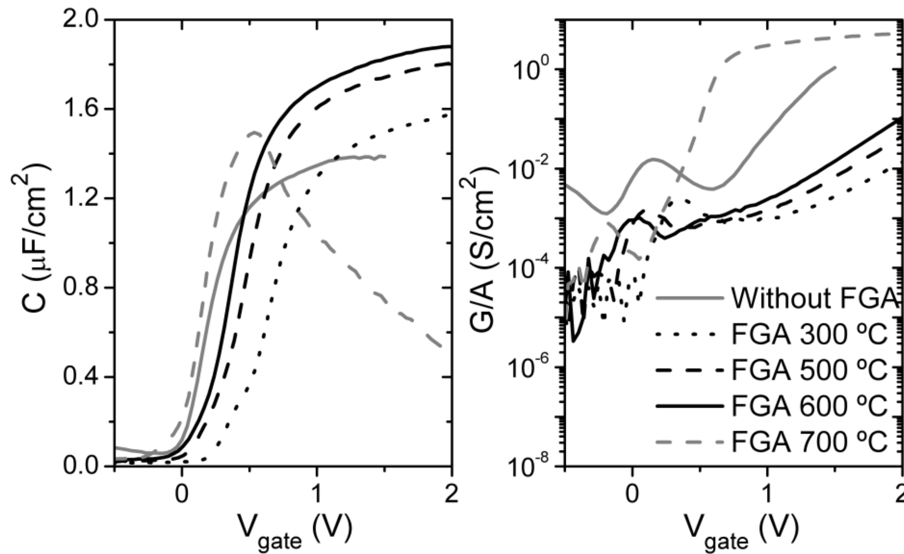

Figure VI.9: Area normalized C and G as a function of V_{gate} characteristics for the $Gd_{0.9}Sc_{1.1}O_3$ sample before and after several FGAs at different temperatures.

The effect of further increasing the FGA temperature up to 700 ºC (presented in Figure VI.9 with grey dashed lines) produces a severe capacitance roll-off due to a high conductance (at 0.5 V, the normalized conductance exceeds 1 S/cm^2). This suggests that the maximum FGA temperature that could be carried out for this sample is 600 ºC.

Referring to the area normalized G-V_{gate} curves of this figure, before the FGA, the conductance is higher than after the FGA up to 600 ºC. This points out that, together with the formation of the gadolinium scandate, leakage paths are passivated. A slight increase in the conductance is observed as the FGA temperature is raised, most likely related to the accumulation capacitance increase commented in the former paragraph.

In terms of the EOT (obtained with a CVC algorithm developed by Hauser *et al.*[29], the as deposited sample has an EOT of ~2.1 nm. This value decreases while the temperature of the FGA is raised. The EOT reaches a minimum value of ~1.5 nm after the FGA at 600 ºC. This decreasing trend is shown in the left hand side of Figure VI.10. This EOT reduction after the FGA was not observed in the binary oxides, as it was pointed out in the former chapter (in fact, an increase in the EOT of around 0.2-0.5 nm for the binary oxides after the FGA was obtained). This is also related to the high κ gadolinium scandate formation.

Additionally, using the conductance method,[30] it was found that the D_{it} has a decreasing tendency with the temperature, as it is shown in the right hand side of Figure VI.10. In other words, the permittivity boost does not compromise the interface quality, which is an excellent result. The D_{it} value is reduced more than one order of magnitude after the FGA (from 8×10^{12} $eV^{-1}cm^{-2}$ for the as deposited sample to 6×10^{11} $eV^{-1}cm^{-2}$ after the FGA at 300 ºC, and then further decreasing with temperature down to 3×10^{11} $eV^{-1}cm^{-2}$ for 600 ºC). This D_{it} value is similar to those reported in other works for $GdScO_3$ grown by electron beam evaporation8 and atomic layer deposition[28] and it is acceptable for high κ dielectrics. Besides, it is noteworthy that even at 600 ºC interface states do not depassivate (in other words, hydrogen remains bonded to defects). At 700 ºC the trap density could not be reliably assessed, but since the conductance peak is similar as the 600 ºC case, no depassivation seems to occur.

It is important to highlight that the SiO_x thickness found by TEM (shown in Figure VI.8) is very close to the EOT (that is 1.5 nm for the sample after the FGA at 600 ºC). Thus, the ± 0.1 nm uncertainty of the SiO_x thickness produce a large disturbance when calculating the permittivity of the dielectric film.

The effective κ value of the dielectric stack can be obtained with the following equation:

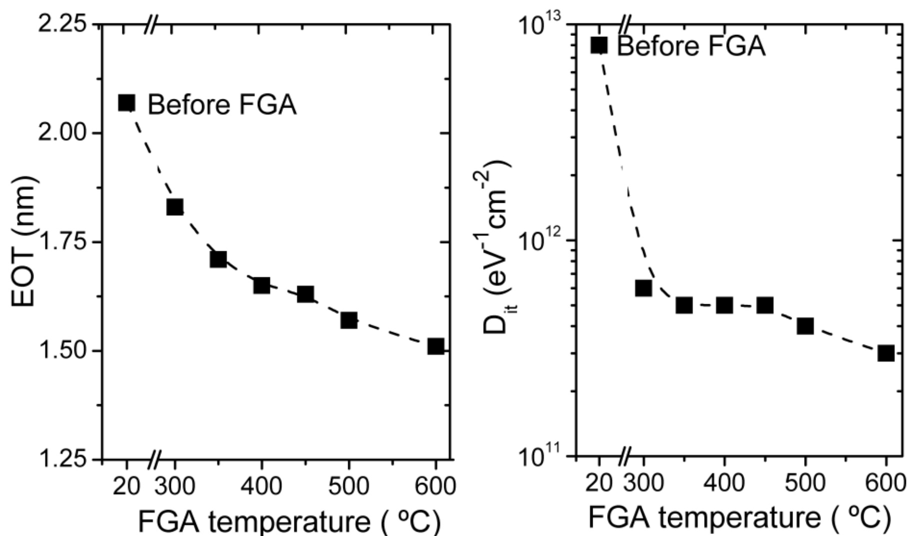

Figure VI.10: EOT (left) and D_{it} (right) values as a function of the annealing temperature for the sample fabricated with $Gd_{0.9}Sc_{1.1}O_3$ as dielectric.

$$\kappa_{eff} = \frac{3.9t}{EOT} \qquad \textbf{(VI.1)}$$

where t is the total dielectric thickness and 3.9 is the dielectric constant for SiO_2.

However, if we want to obtain the permittivity value of the high κ material, the next formula has to be used:

$$\kappa = \frac{3.9t_{high\,\kappa}}{EOT - t_{IL}} \qquad \textbf{(VI.2)}$$

being $t_{high\,\kappa}$, the thickness of the high κ dielectric and t_{IL}, the interlayer thickness.

Therefore, using the thicknesses obtained in Figure VI.8 and with the equation (VI.1), the κ_{eff} of the dielectric stack is higher than 15, a similar value of $HfSiO_4$ reported in other works.[2,31] Nevertheless, by means of equation (VI.2), the permittivity of the $Gd_{0.9}Sc_{1.1}O_3$ film grown by HPS with a two-step method is 32, a value that is in the upper range of the stated values for this material which is between 20 and 30.[1-3] If we take into account in the calculation the uncertainty of the interfacial SiO_x thickness, the $Gd_{0.9}Sc_{1.1}O_3$ permittivity would be 28 (t_{IL} = 0.8 nm) or 39 (t_{IL} = 1.0 nm), in all cases in the upper range of $GdScO_3$ permittivity. This excellent result confirms that the fabrication of MIS devices by means of HPS from metallic targets followed by a plasma oxidation is a very promising alternative for achieving a good performance gadolinium scandate.

To study the presence of slow traps, the hysteresis curves of these devices were measured before and after each FGA, starting the sweep from inversion to accumulation and back again. In Figure VI.11 is represented the hysteresis curves for three different FGAs: 300, 500 and 600 ºC. After the FGA at 300 ºC (in the left hand side of this figure) the flatband voltage shift, ΔV_{FB}, is around 70 mV. This is reduced with annealing temperature, as it can be seen on the sample annealed at 500 ºC, that presents a negligible value (as it is observed in the center of Figure VI.11). Finally, the FGA performed at 600 ºC (and shown in the right hand side of this figure) increases the hysteresis to a negative value (around −150 mV).

Figure VI.12 shows the ΔV_{FB} value for all the annealing temperatures. There it can be appreciated that as deposited devices have an appreciable ΔV_{FB} ~ 150 mV, that

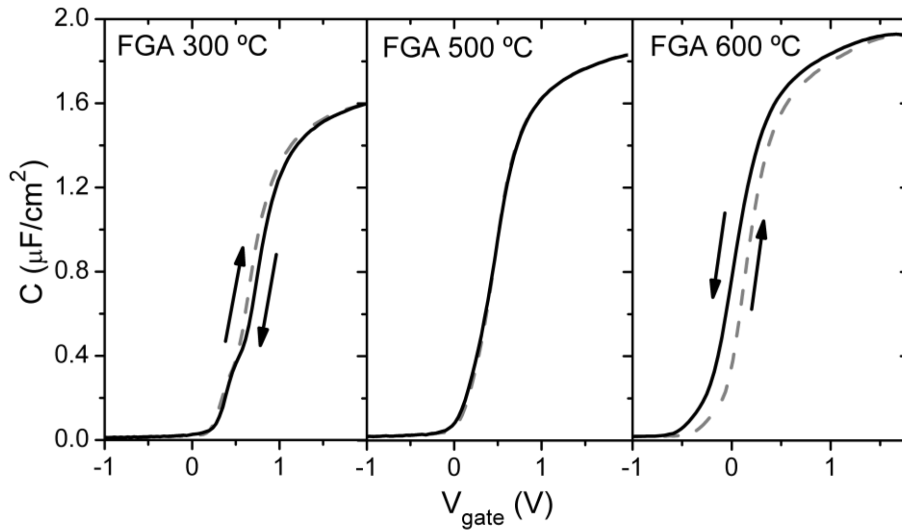

Figure VI.11: Hysteresis C-V_{gate} characteristics measured from inversion to accumulation and back again for the $Gd_{0.9}Sc_{1.1}O_3$ sample after several FGAs at different temperatures.

disappears when annealing at 350 ºC. On the other hand, the V_{FB} shift is noticeable again when annealing at 600 ºC and above, but in this case with a negative value.

To explain this, it is important to remark that the changes in the V_{FB} are due to the variations in charge in the vicinity of the oxide/semiconductor interface during the

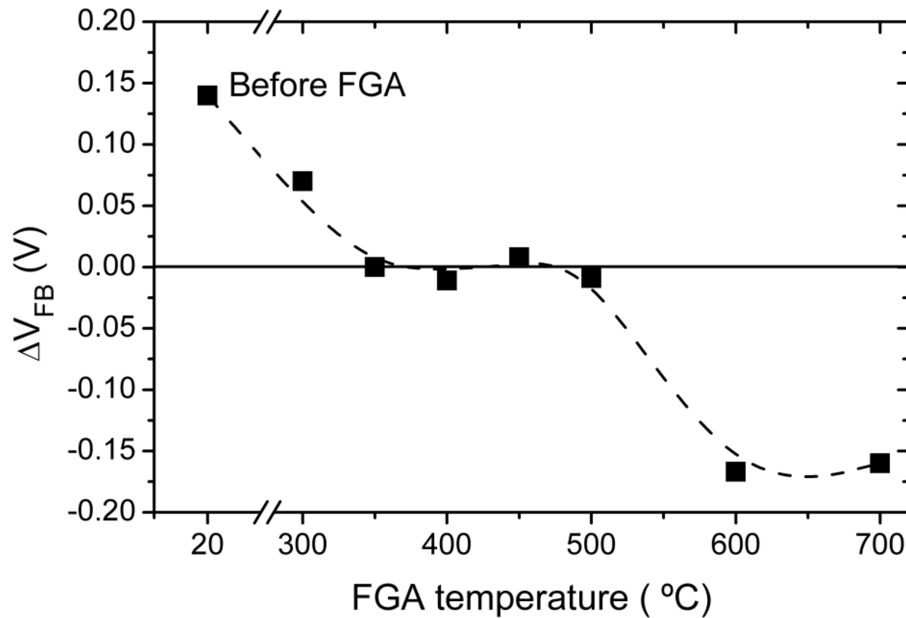

Figure VI.12: Flatband voltage shift as a function of the annealing temperature for the $Gd_{0.9}Sc_{1.1}O_3$ sample.

sweep. This oxide trapped charge, Q_{ot}, can be obtained using the following expression:[32]

$$Q_{ot} = -\Delta V_{FB} C_{ox} \qquad \textbf{(VI.3)}$$

where C_{ox} is the oxide capacitance. The physical origin of this charge variation is either electrons from the semiconductor that are trapped by defects of the dielectric (positive ΔV_{FB}), or mobile positive ions (like sodium, potassium or hydrogen), that are pushed by the electric field from the gate towards the semiconductor (negative ΔV_{FB}). Thus the sign and value of ΔV_{FB} gives insight into the dielectric properties.

The results shown in Figure VI.12 can be interpreted as follows: as deposited $Gd_{0.9}Sc_{1.1}O_3$ film has some dangling bonds that act as electron traps, and thus the positive ΔV_{FB}. These traps are passivated at 350 ºC by the hydrogen from the forming gas atmosphere and as a consequence, no hysteresis is found. At 600 ºC, the negative flatband voltage shift appears, indicating a displacement of positive ions with polarity. Since no mobile ions are present at lower temperatures, K or Na contamination is not likely. Therefore, the most plausible candidate is hydrogen from the forming gas anneal. This means that at 600 ºC and above an excess of hydrogen is accumulated within the dielectric and gives rise to the negative ΔV_{FB}.

The C-V_{gate} and G-V_{gate} frequency dispersion characteristics measured from 1 kHz to 1 MHz are represented in Figure VI.13 for the $Gd_{0.9}Sc_{1.1}O_3$ sample after the FGA at

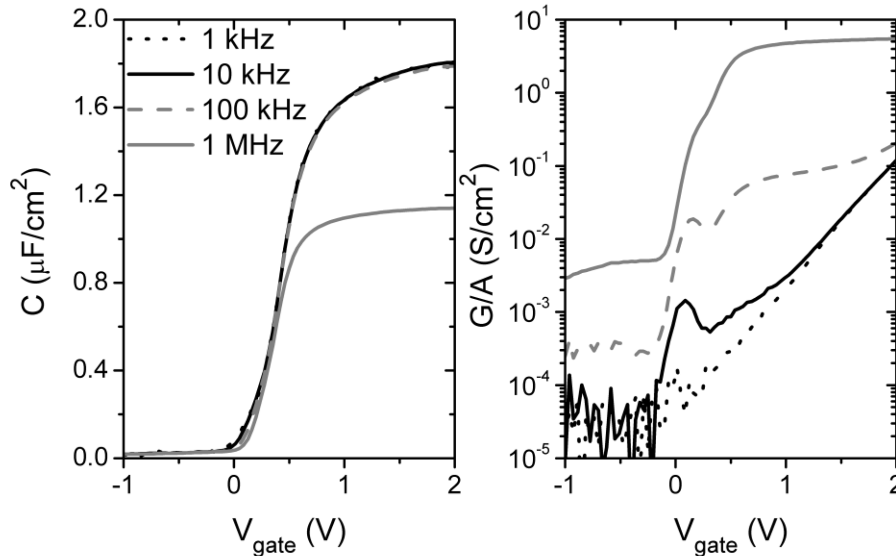

Figure VI.13: C-V_{gate} and G-V_{gate} curves measured at different frequencies for the $Gd_{0.9}Sc_{1.1}O_3$ sample after FGA at 600 ºC.

600 ºC. No frequency dispersion of the flatband voltage is found. The only appreciable effect in the C-V_{gate} curves is a great reduction in the accumulation capacitance measured at 1 MHz, which is originated from high conductance and substrate series resistance. This last parameter mainly affects the high frequency C-V_{gate} curve.[33] The value of the series resistance for the 1 MHz curve is ~170 Ω. From these curves and using the conductance method,[30] the D_{it} is around 3×10^{11} $eV^{-1}cm^{-2}$ for all the frequencies, pointing out that the interfacial traps are fast and can respond even at high frequencies. Analogous results were found for the other annealing temperatures.

The leakage current for the $Gd_{0.9}Sc_{1.1}O_3$ devices measured before and after different FGAs is presented in Figure VI.14 with the J-V_{gate} characteristics. The as grown sample has one order of magnitude higher leakage current than the sample with a FGA at 300 ºC. As it was commented in the C-V_{gate} curves of Figure VI.9, the formation of the gadolinium scandate required a temperature treatment. Here this conclusion is also confirmed: the FGA reduces the current density due to leakage paths passivation when the intermixing of the nanolaminate is taking place. Then, the leakage current is increased as the temperature of the FGA is raised, together with the reduction in the EOT observed before. This points out to a densification of the $Gd_{0.9}Sc_{1.1}O_3$ layer that increases the tunneling current. The current density after the FGA at 600 ºC is low, in

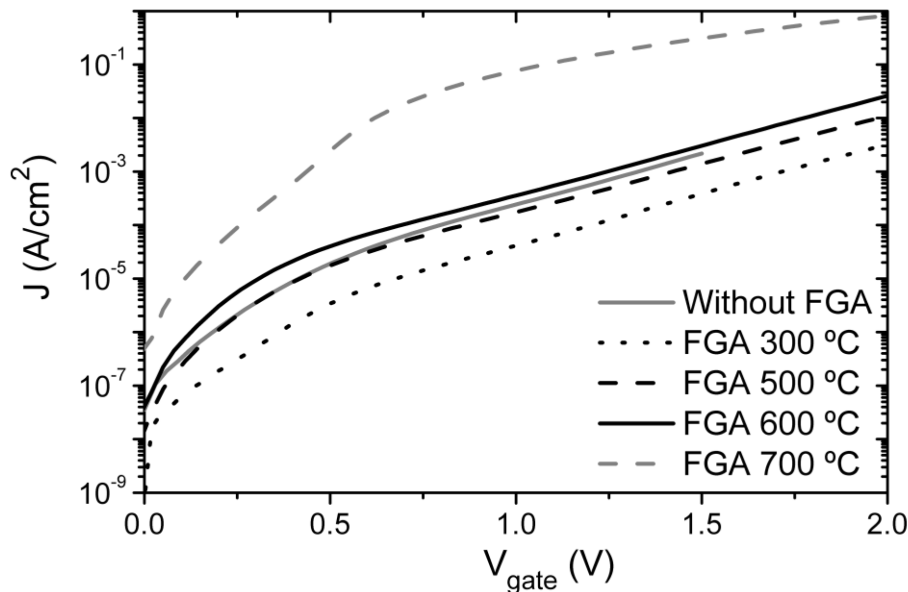

Figure VI.14: J-V_{gate} characteristics for the $Gd_{0.9}Sc_{1.1}O_3$ sample before and after different FGAs.

the ~10^{-3} A/cm^2 range at 1.5 V for an EOT of 1.5 nm. This value is about four orders of magnitude lower compared with the current of a capacitor with an equivalent 1.5 nm SiO_2 layer.[34]

Figure VI.15 shows the J-V_{gate} curves for several devices after the 600 ºC anneal in this case extending the gate voltage to 5 V to check uniformity and dielectric breakdown. The good reproducibility shown there is an indication of the uniformity of the sample. In addition, soft breakdown events are observed at around 2.7 V while hard breakdown events are found at 4.8 V for some samples. These voltages are high enough for MOSFETs applications.

Thus, a conclusion of this subsection is that the fabrication of MIS devices with $Gd_{0.9}Sc_{1.1}O_3$ grown by the two-step method is achieved with good electrical behavior, obtaining an EOT of ~1.5 nm with low interface traps density, hysteresis and leakage current. From the electrical characteristics, an optimal FGA temperature in the 500-600 ºC range is found: 500 ºC is better from a leakage and hysteresis standpoint, but 600 ºC has lower EOT and interface trap density.

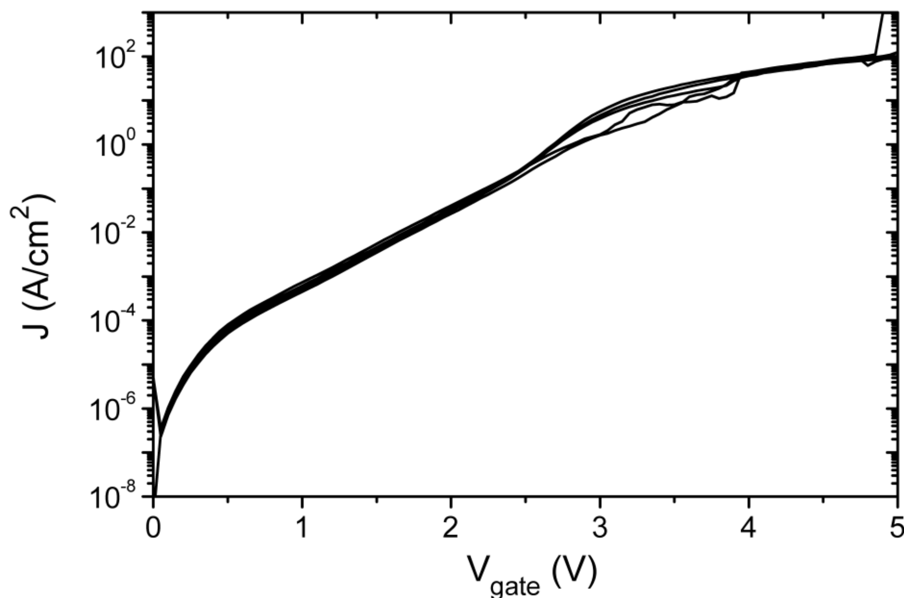

Figure VI.15: J-V_{gate} curves for the $Gd_{0.9}Sc_{1.1}O_3$ sample after an FGA at 600 ºC, measured in several devices to observe breakdown events and reproducibility.

VI.3.- SUMMARY AND CONCLUSIONS

In this chapter, the fabrication of $Gd_{2-x}Sc_xO_3$ film was achieved by means of HPS after a deposition of a nanolaminate of metallic Gd and Sc layer and a subsequently plasma oxidation. A gadolinium scandate with an almost intermediate composition was obtained. This $Gd_{0.9}Sc_{1.1}O_3$ film was amorphous and presented good electrical characteristics: for an EOT of 1.5 nm, the leakage current, the hysteresis and the interfacial trap density were low and similar to other values reported in some works. The κ value of this dielectric film is around 32. Due to the low EOT, that is mostly determined by the IL thickness (1.5 and 0.9 nm, respectively), decreasing this interface is crucial for further EOT scaling. Therefore, the introduction of the scavenging effect[35] is a possible path for improving the reduction in the EOT, which will be explored in the following chapter.

REFERENCES

[1] D. G. Schlom, J. H. Haeni. "*A thermodynamic approach to selecting alternative gate dielectrics*". MRS Bulletin, 27, 198 (2002).

[2] J. A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang, C. Adelmann, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V. V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervost, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M. Jurczak, J. Van Houdt, D. J. Wouters. "*High-k dielectrics for future generation memory devices*". Microelectron. Eng., 86¸ 1789 (2009).

[3] K. Fröhlich, J. Fedor, I. Kostic, J. Manka, P. Ballo. "*Gadolinium scandate: next candidate for alternative gate dielectric in CMOS technology?*". J. of Elect. Eng., 62, 54 (2011).

[4] S. G. Lim, S. Kriventsov, T. H. Jackson, J. H. Haeni, D. G. Schlom, A. M. Balbashov, R. Uecker, P. Reiche, J. L. Freeouf, G. Lucovsky. "*Dielectric functions and optical bandgaps of high-K dielectrics for metal-oxide-semiconductor field-efect transistors by far ultraviolet spectroscopic ellipsometry*". J. Appl. Phys., 91, 4500 (2002).

[5] V. V. Afanas'ev, A. Stesmans, C. Zhao, M. Caymax, T. Heeg, J. Schubert, Y. Jia, D. G. Schlom, G. Lucovsky. "*Band alignment between (100)Si and complex rare earth/transition metal oxides*". Appl. Phys. Lett., 85, 5917 (2004).

[6] C. Derks, K. Kuepper, M. Raekers, A. V. Postnikov, R. Uecker, W. L. Yang, M. Neumann. "*Band-gap variation in $RScO_3$ (R = Pr, Nd, Sm, Eu, Gd, Tb, and Dy): X-ray absorption and O K-edge X-ray emission spectroscopies*" Physical Rev. B, 86, 155124 (2012).

[7] C. Zhao, T. Witters, B. Brijs, H. Bender, O. Richards, M. Caymax, T. Heeg, J. Schubert, V. V. Afanas'ev, A. Stesmans, D. G. Schlom. "*Ternary rare-earth metal oxide high-k layers on silicon oxide*". Appl. Phys. Lett., 86, 132903 (2005).

[8] M. Wagner, T. Heeg, J. Schubert, St. Lenk, S. Mantl, C. Zhao, M. Caymax, S. De Gent. "*Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation*". Appl. Phys. Lett., 88, 172901 (2006).

[9] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Gadolinium scandate by high-pressure sputtering for future generations of high-κ dielectrics*". Semicond. Sci. Technol., 28, 085004 (2013).

[10] P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Nano-laminate vs. direct deposition of high permittivity gadolinium scandate on silicon by high pressure sputtering*". Thin Solid Films, 593, 62 (2015).

[11] W. F. Meggers, C. H. Corliss, B. F. Scribner. "*Tables of spectral-line intensities, Part I – Arranged by elements, Part II – Arranged by wavelengths, Natl. Bur. Stand. Monograph 145*". Natl. Bur. Stand. U.S., 600 (1975).

[12] R. W. B. Pearse, A. G Gaydon. "*The identification of molecular spectra*". 4th edition. John Wiley & Sons, Inc., New York (1976).

[13] J. E. Lawler, J. T. Dakin. "*Absolute transition probabilities in Sc I and Sc II*". J. Opt. Soc. Am. B, 6, 1457 (1989).

[14] B. Ahmed, J. Verges. "*Extension de l'étude de spectre d'arc de scandium*". Physica, 92C, 113 (1977).

[15] S. Johansson, U. Litzén. "*The spectrum of singly ionized scandium, Sc II*". Phys. Scr., 22, 49 (1980).

[16] G. Norlén. "*Wavelengths and energy levels of Ar I and Ar II based on new interferometric measurements in the region 3400-9800 Å*". Phys. Scr. 8, 249 (1973).

[17] B. Wende, "*Optical transition probabilities of the configurations $3p^5 4s$-$3p^5 5p$ of Argon I,*" Zeitschrift für Physik 213, 341 (1968).

[18] D. Raiser, J. P. Deville. "*Study of XPS photoemission of some gadolinium compounds*". J. Electron Spectrosc. Relat. Phenom., 57, 91 (1991).

[19] Y. Uwamino, Y. Ishizuka, H. Yamatera. "*X-ray photoelectron spectroscopy of rare-earth compounds*". J. Electron Spectrosc. Relat. Phenom., 34, 67 (1984).

[20] A. D. Hamer, D. G. Tisley, R. A. Walton. "*The X-ray photoelectron spectra of inorganic molecules-VIII[1,2]: Compounds of scandium(III), scandium (III) oxide and complexes with organic oxygen donor molecules*". J. Inorg. Nucl. Chem., 36, 1771 (1974).

[21] P. C. Feijoo, M. Toledano-Luque, A. del Prado, E. San Andrés, M. L. Lucía, J. L. G. Fierro. "*Electrical and chemical characterization of high pressure sputtered scandium oxide for memory applications*". Conference on Electron Devices (CDE 2011) Conf. Proc., 1-3 (2011).

[22] D. Ferrah, M. El Kazzi, G. Niu, C. Botella, J. Penuelas, Y. Robach, L. Louahadj, R. Bachelet, L. Largeau, G. Saint-Girons, Q. Liu, B. Vilquin, G. Grenet. "*X-ray photoelectron spectroscopy and diffraction investigation of a metal-oxide-semiconductor heterostructure: Pt/Gd_2O_3/Si(111)*". J. Cryst. Growth, 416, 118 (2015).

[23] P. Raghy, N. Rana, C. Yim, E. Shero, F. Shadman. "*Adsorption of moisture and organic contaminants on hafnium oxide, zirconium oxide and silicon oxide gate dielectrics*". J. Electrochem. Soc., 150, F186 (2003).

[24] P. G. Pai, S. S. Chao, V. Takagi, G. Lucovsky. "*Infrared spectroscopic study of SiO_x films produced by plasma enhanced chemical vapor deposition*". J. Vac. Sci. Technol. A, 4, 689 (1986).

[25] R. A. B. Devine. "*Structural nature of the Si/SiO_2 interface through infrared spectroscopy*". Appl. Phys. Lett., 68, 3108 (1996).

[26] K. Huseková, M. Jurkovic, K. Cico, D. Machajdík, E. Dobrocka, R. Lupták, A. Macková, K. Fröhlich. "*Preparation of high permittivity $GdScO_3$ films by liquid injection MOCVD*". ECS Trans., 25, 1061 (2009).

[27] G. D. Wilk, R. M. Wallace, J. M. Anthony. "*High-κ gate dielectrics: Current status and materials properties considerations*". J. Appl. Phys., 89, 5243 (2001).

[28] K. H. Kim, D. B. Farmer, J. S. M. Lehn, P. V. Rao, R. G. Gordon. "*Atomic layer deposition of gadolinium scandate films with high dielectric constant and low leakage current*". Appl. Phys. Lett., 89, 133512 (2006).

[29] J. R. Hauser, K. Ahmed. "*Characterization of ultra-thin oxides using electrical C-V and I-V measurements*". AIP Conf. Proc., 449, 235 (1998).

[30] E. H. Nicollian, A. Goetzberger. "*The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique*". Bell Syst. Tech. J., 46, 1055 (1967).

[31] D. Fischer, A. Kersch. "*Ab initio study of high permittivity phase stabilization in HfSiO*". Microelectron. Eng., 84, 2039 (2007).

[32] D. K. Schroder. "Semiconductor material and device characterization". John Willey & Sons. New York, 1990.

[33] W. H. Wu, B. Y. Tsui, M. C. Chen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, M. S. Liang. "*Spatial an energetic distribution of border traps in the dual layer HfO2/SiO2 high-k gate stack by low-frequency capacitance-voltage measurements*". Appl. Phys. Lett., 89, 162911 (2006).

[34] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, L. O. Shih-Hsien, G. A. Sai-Halasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind, H. S. Wong. "*CMOS scaling into the nanometer regime*". Proc. IEEE, 85, 486 (1997).

[35] H. Kim, P. C. McIntyre, C. O. Chui, K. C. Saraswat, S. Stemmer. "*Engineering chemically abrupt high-k metal oxide/silicon interfaces using an oxygen-gettering metal overlayer*". J. Appl. Phys., 96, 3467 (2004).

Chapter VII:

Interface scavenging

In this chapter, the scavenging concept is analyzed. As it was commented in the introduction, Kim *et al.*[1] explored this effect for the first time with the aim of reducing the SiO_x layer that growth at the high κ/silicon interface. The interlayer (IL) scavenging is produced by the decomposition of the SiO_x.1-3 The reduction in thickness of this SiO_x layer, that is a low κ material, decreases the total EOT.

Several works have studied the scavenging effect using HfO_2 as dielectric.1-8 Also, ZrO_2 was explored.1 However, other than the publications from our group,[9-12] we have not found any reference for scavenging on other alternative high κ dielectrics deposited on Si.

Here, MIS devices using Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ grown by HPS with the two-step method (presented in the last chapters) were fabricated. The top electrode was Ti (capped with Al or Pt in order to avoid oxidation or nitridation). This metal has been reported in several works as an oxygen scavenger.1,6,8 The objective of this chapter is to check if the scavenging effect is compatible with these high κ materials to achieve a reduction in the interfacial SiO_x and thus, obtaining a lower EOT while keeping a reasonable interface trap density and leakage current.

Electrical measurements (C-V_{gate} and J-V_{gate} curves) were performed to the MIS capacitors with Ti as top electrode. These results were compared with the same samples with Pt. HRTEM images were obtained in order to study the thickness of the dielectric and the interfacial layers. The conductance method[13] and DLTS[14] measurements were used to obtain the interfacial trap density, D_{it}.

VII.1.- EXPERIMENTAL METHOD

MIS devices with Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ as dielectrics were fabricated by means of HPS with the two-step method introduced in the former chapters. First of all, thin metallic films of Gd, Sc or a nanolaminate of them were deposited during different times at 30 W in an Ar atmosphere. Afterwards, and without breaking the vacuum, an *in situ* plasma oxidation was performed in an Ar/O_2 ambient in order to oxidize the metallic layer. The *rf* power and the duration of this step were different for each sample. Both processes were carried out, in all the cases, at room temperature and at a pressure of 0.50 mbar.

Various thicknesses of Ti (capped with Al or Pt) were e-beam evaporated as the top electrode. The backside of the wafers was covered with 50 nm of Ti / 100 nm of Al. Several forming gas anneals (FGAs) were performed at different temperatures. Besides, Pt samples were fabricated in order to have a reference and check the differences.

VII.2.- RESULTS AND DISCUSSION

2.1.- Thick Ti layers as top electrode with Gd_2O_3

In this section, the objective was to study the compatibility of the scavenging effect with plasma oxidized Gd_2O_3 films. MIS devices were fabricated without field oxide (FOX) and with 80 s of Gd and a plasma oxidation of 300 s (both processes performed at 30 W). The top electrode was a stacked structure formed of 50 nm of Ti capped with 100 nm of Al in order to avoid titanium surface oxidation or nitridation when annealing in forming gas. This sample was similar to the reference one studied in section 2.2 of chapter V with a metallic gate of Pt and here it was used for comparison. Capacitors were measured before and after a FGA at 300 ºC for 20 min.

The C-V_{gate} characteristics measured at 10 kHz for these devices are presented in Figure VII.1 for the Pt reference sample (in the left hand side) and the Ti gated MIS devices (right hand side) for the as deposited capacitors (in dashed lines) and after the FGA at 300 ºC (in solid lines). The Pt devices present similar values of the accumulation capacitance before and after the FGA (only a slight decrease of this value is observed after the temperature treatment, which corresponds to a 0.2 nm increase in

the EOT obtained with the algorithm developed by Hauser *et al.*[15]). This was due to an oxide regrowth or Pt adhesion problems, as it was commented in chapter V. Additionally, the hump in depletion observed in the as deposited capacitors disappeared after the FGA, pointing out to an interface improvement due to hydrogen passivation.

For the Ti case, a great increase in the accumulation capacitance is observed for the sample after the FGA. In fact, a reduction of ~1.8 nm of EOT is achieved, reaching an EOT value of 1.7 nm. This rise of the accumulation capacitance value for the Ti gated devices is a consequence of the scavenging effect of Ti, which removes oxygen from the interfacial layer of SiO_x. This effect is even observable for the as grown samples and without any temperature treatment. Comparing the Pt and Ti capacitors before the FGA, it is observed a slightly higher accumulation capacitance for the sample with Ti (thus, around 0.3 nm of EOT lower). The explanation could be that during the Ti e-beam evaporation, some heating of the film by infrared radiation is likely. Although this process is performed in vacuum (~10^{-6} mbar) and the sample is separated around 50 cm from the crucible, the melted Ti is at 1200-1500 ºC and this heat could induce interface scavenging. Definitely, this effect is more remarkable when a

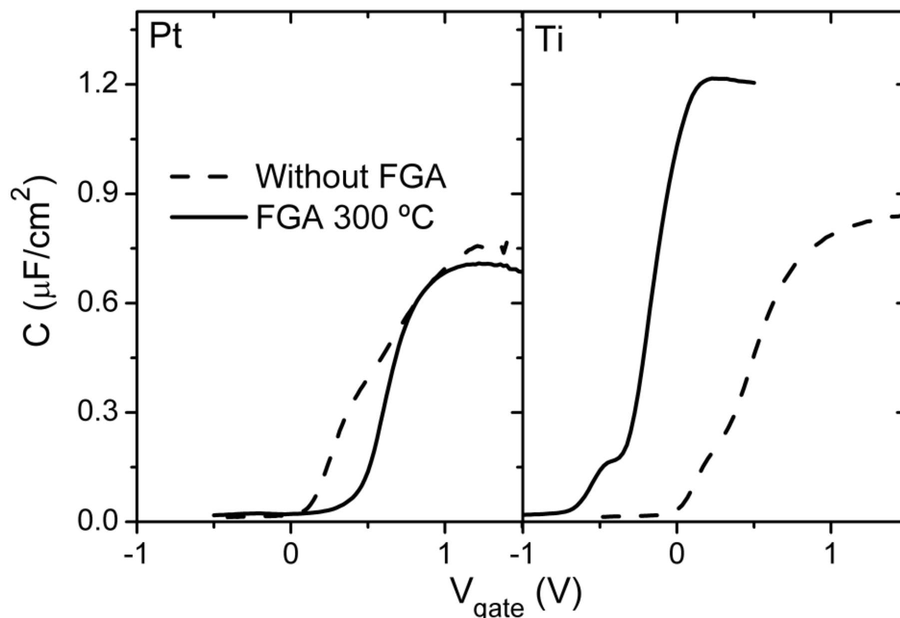

Figure VII.1: C-V_{gate} curves for the sample with 80 s of Gd and a 300 s plasma oxidation at 30 W measured before (dashed lines) and after the FGA at 300 ºC (solid lines) for two different top contacts: Pt/Al (as a reference) and thick Ti/Al.

temperature annealing is performed, as it is observed for the sample after the FGA. This effect was also reported by Nakajima *et al.*3

Besides, capacitance curves present a hump for the Ti devices before and also after the FGA, which is caused by a high D_{it} (~2×10^{12} $eV^{-1}cm^{-2}$, about one or two orders of magnitude higher than the Pt sample). These D_{it} values were extracted from the conductance method.[13] This interface degradation, due to the formation of additional Si dangling bond defects, is related to the scavenging effect as it was pointed out by Cerbu *et al.*[16]

To sum up, the EOT and D_{it} values before and after the FGA for both types of metallic contacts are presented in Table VII.1.

	Without FGA		FGA 300 ºC	
Metallic contact	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
Pt/Al	3.8	5×10^{12}	4.0	---
Ti/Al	3.5	4×10^{12}	1.7	2×10^{12}

Table VII.1: EOT and D_{it} values extracted from electrical measurements before and after the FGA at 300 ºC for samples with 80 s of Gd and a plasma oxidation of 300 s (at 30 W) with two different top electrodes: Pt/Al and thick Ti/Al. "---" means that the D_{it} value is under the detection limit of the method.

The cross-sectional HRTEM images of these samples after the FGA at 300 °C are shown in Figure VII.2 for the two different metal electrodes. Figure VII.2(a) presents the sample with Pt as top metal (as a reference) and Figure VII.2(b), the same dielectric film but with a thick Ti layer. As it was commented in chapter V, the pure Pt sample presents 6.1 nm of an amorphous Gd_2O_3 layer on top of 1.8 nm of interfacial SiO_x, probably grown during the long plasma oxidation. On the other hand, when Ti is used as top metal, no SiO_x interface can be observed. This is due to the scavenging effect of Ti. It is also noticeable, that the thickness of the Gd_2O_3 film is ~2.1 nm lower than in the Pt case. This result points out to an excessive scavenging of the thick Ti layer that not only removes oxygen from the SiO_x interface (~1.8 nm), but also scavenges part of the

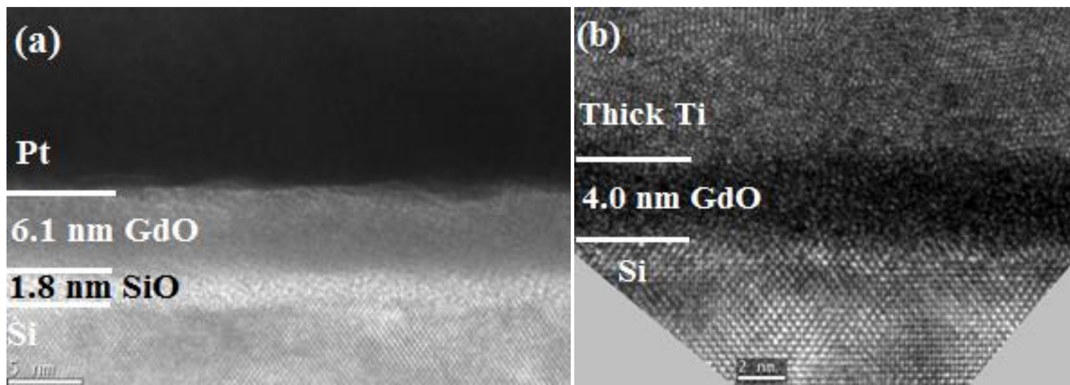

Figure VII.2: HRTEM images for the samples with long oxidation (300 s at 30 W) with two metallic contacts: (a) Pt (as a reference) and (b) thick Ti.

dielectric material (reducing this layer ~2.1 nm). This would produce an increase of the leakage current due to the thinner high κ film, which is not desirable.

Therefore, the main conclusion of this section is that the interface scavenging process works on HPS deposited Gd_2O_3, but needs optimization, since an excessive thickness of the Ti layer, used as top electrode, implies a reduction of the IL but also a degradation of the dielectric film, reducing its thickness after the FGA. Thus, a second set of samples with thinner Ti films was fabricated, with the aim of controlling the scavenging effect produced.

2.2.- Optimization of the scavenging effect for plasma oxidized Gd_2O_3

To optimize the scavenging effect, a second set of samples with a softer oxidation (less duration and lower *rf* power) together with a thinner Ti films was fabricated. MIS capacitors with FOX were grown with 80 s of Gd and a plasma oxidation at 20 W during 100 s. These were the best conditions obtained in chapter V for Gd_2O_3. Since the metallic Gd deposition time is the same as in the first section, it can be assumed that the Gd_2O_3 thickness is similar, around 6.1 nm. On the other hand, it is expected a thinner interface since it was used a less aggressive oxidation. Different thicknesses of Ti were used as top electrode: 2.5, 5 and 17 nm (all capped with 25 nm of Pt). The objective was the decrease of the interfacial SiO_x thickness without degrading the G_2dO_3 layer. Several FGAs at 300, 350 and 400 ºC were performed during 20 min and the devices were measured before and after the different FGAs.

Figure VII.3 depicts the normalized C-V_{gate} characteristics of these samples with different thicknesses of Ti, measured at 10 kHz before and after the FGAs. All the samples present a characteristic hump in depletion in the C-V_{gate} curve before the temperature annealing due to a high D_{it} value. This hump was also observed for the Pt sample used as reference (shown in section 2.3 of chapter V).

For the sample with 2.5 nm of Ti (Figure VII.3(a)) and after the annealings, there is a slight increase of the accumulation capacitance. Besides, there are no relevant differences between the several temperatures of the FGAs. Then, the scavenging effect of the 2.5 nm Ti film is moderate and saturates for an annealing temperature of 300 °C. Furthermore, the FGAs make the C-V_{gate} fall more abruptly and the hump in depletion disappears, which indicates an improvement in the oxide/semiconductor interface.

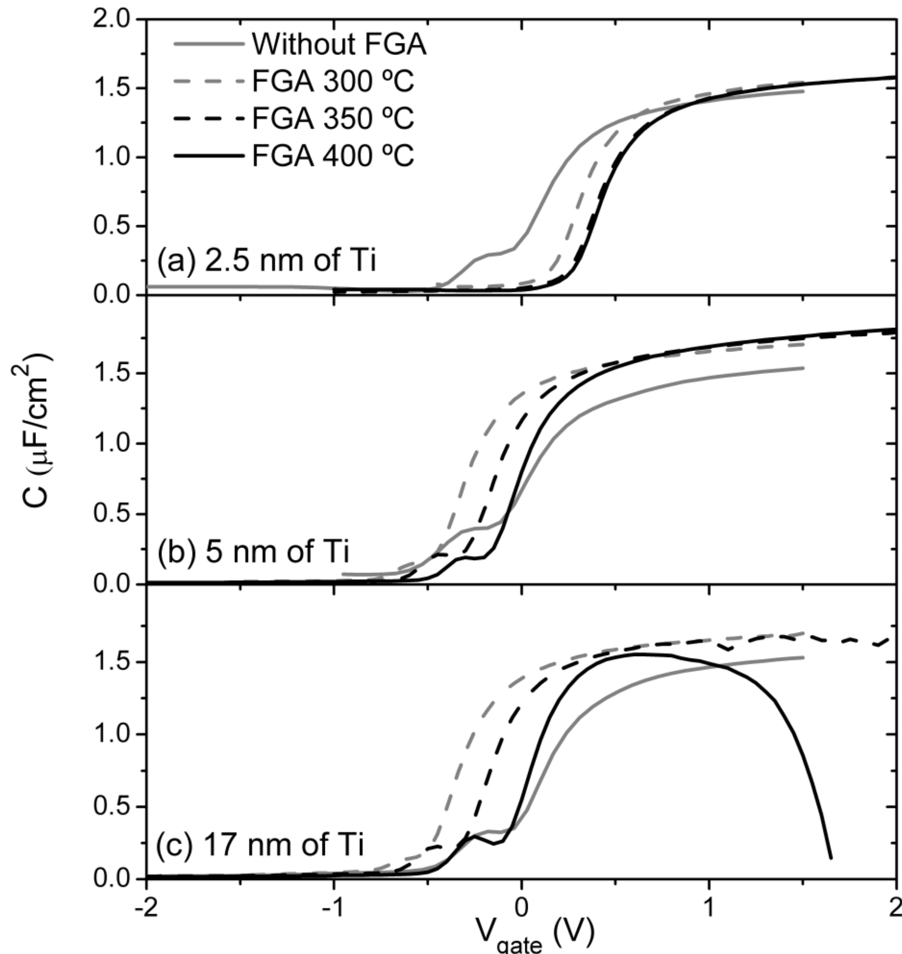

Figure VII.3: C-V_{gate} curves for the sample with 80 s of Gd and an 100 s plasma oxidation at 20 W measured before and after several FGAs with different thickness of Ti layers: (a) 2.5 nm, (b) 5 nm and (c) 17 nm.

For the 5 nm Ti devices (in Figure VII.3(b)), the accumulation capacitance value visibly increases after the FGA at 300 ºC. No significant differences can be noticed for higher FGAs at 350 and 400 °C for this sample. In this case, the scavenging saturation occurs for the FGA at 350 °C. For this Ti thickness, the distortion of the curve in depletion is reduced after annealing, but it is still clearly observed a hump, even after the FGA at 400 ºC. This points out to a high D_{it} due to the scavenging effect, as it was commented in the former section.

For the thicker Ti layer with around 17 nm (Figure VII.3(c)), the behavior of the C-V_{gate} curves is similar to the former sample up to an annealing temperature of 350 °C, but for annealing temperatures above 400 °C, there is a severe accumulation capacitance drop, pointing out to an excessive scavenging effect. The normalized conductance for this sample presents a value over 1 S/cm^2 for gate voltages higher than 1 V, supporting this aggressive scavenging effect.

The left hand side of Figure VII.4 presents the evolution of the EOT value as a function of the annealing temperature for these samples with several Ti thicknesses. It is important to highlight that the Pt sample used as reference, analyzed in chapter V and presented in figure V.23, had an EOT value around 2.2 nm (before and also after the FGAs). For the thinner Ti thickness, there is a hardly noticeable decrease in the EOT

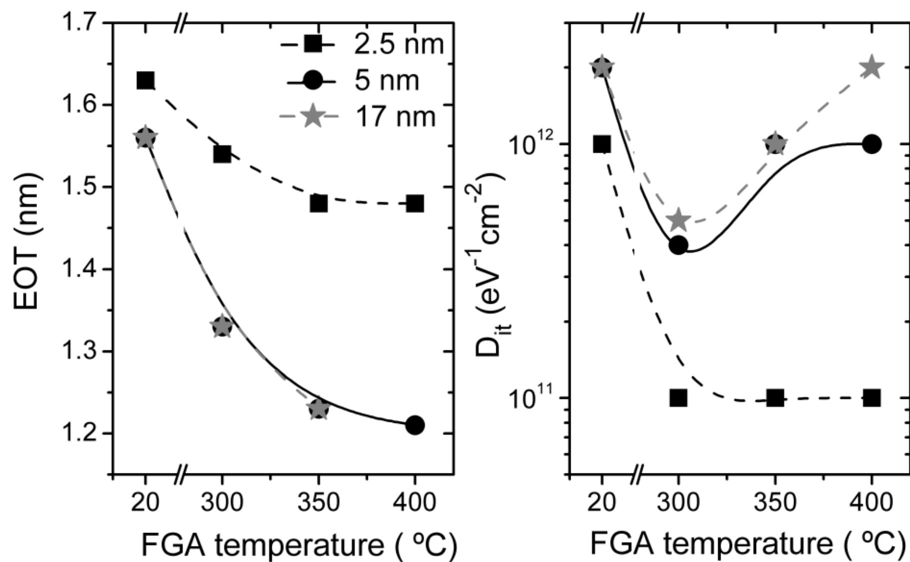

Figure VII.4: EOT (left) and D_{it} (right) values as a function of the annealing temperature for the samples fabricated with different Ti thicknesses: 2.5, 5 and 17 nm.

from a value slightly higher than 1.6 nm (for the as deposited sample) to 1.5 nm (after the FGAs). The saturation effect for this sample discussed before is also noticed in this figure for annealing temperatures above 300 °C. For the sample with 5 nm Ti layer, the EOT reduction goes from a value slightly lower than 1.6 nm (for the as grown sample) to 1.2 nm (after FGA at 400 °C). Finally, for the sample with the thicker Ti top metal layer, the trend in the EOT decrease is the same as the one observed in the previous sample up to the FGA at 350 °C. Due to the capacitance drop observed in Figure VII.3(c) after FGA at 400 °C, it is not possible to obtain the EOT value for this temperature. Besides, from Figure VII.4, it can be observed that the EOT is similar for all the as deposited samples (around 1.6 nm), but this value is slightly lower for samples with higher Ti thickness. When comparing this value with the EOT of the Pt gated device, it can be concluded that some scavenging takes place even during the deposition of the metal contact, as it was also commented it the former section. Besides, the mild EOT reduction when increasing the Ti thickness is also an indication that during the top contact evaporation there is some scavenging in the samples, most likely due to heating by infrared radiation, as it was pointed out before and also was observed in reference.3

Additionally, Figure VII.4 represents, in the right hand side, the evolution of D_{it} as a function of the annealing temperature for the different Ti thicknesses. In the Pt case, it was observed that the D_{it} decreased around one order of magnitude to ~10^{11} $eV^{-1}cm^{-2}$ after the FGAs. In this case, for the sample with 2.5 nm of Ti, the D_{it} achieves a similar value to that obtained for the Pt sample after the FGA at 300 °C, showing an interface improvement, as was also qualitatively observed in the C-V_{gate} of that sample with the disappearance of the hump in depletion. However, thicker Ti layers show a higher value of the D_{it} even before annealing, which is another confirmation of the scavenging effect during evaporation (lower unannealed EOT means more intensive scavenging, which produces more defects). For these samples, the lowest FGA temperature, 300 °C, produces a reduction of the D_{it} up to 4-5×10^{11} $eV^{-1}cm^{-2}$. These values increase again to the ~10^{12} $eV^{-1}cm^{-2}$ range when the annealing temperature is raised. D_{it} degradation is even more noticeable for the sample with 17 nm of Ti after the FGA at 400 °C, suggesting again that, excessive scavenging results in a defective interface. Other works have reported similar values of the D_{it} using ZrO_2,[17] single crystalline Gd_2O_3[18] and polycrystalline Gd_2O_3 with an amorphous GdSiO layer.[19]

In Figure VII.5, the leakage current density is represented as a function of the gate voltage. These results are in agreement with the capacitance measurements (shown in Figure VII.3). The leakage of the sample with 2.5 nm of Ti does not change before and after FGAs, with a value around 10^{-6} A/cm^2 at 1 V (Figure VII.5(a)). This means that only a negligible scavenging is happening. Analogous results were obtained for the reference sample with Pt presented in chapter V. For the sample with 5 nm of Ti, current density increases moderately as the annealing temperature is raised. In any case, leakage current is in the order of 10^{-4} A/cm^2 at 1 V for all the FGAs (Figure VII.5(b)), similar to those reported in previous works.[17,20] On the other hand, for the sample with 17 nm of Ti, the current density reaches a high value over 10^{-1} A/cm^2 at 1 V after the FGA at 350 °C as can be observed in Figure VII.5(c). This confirms, again, that there is

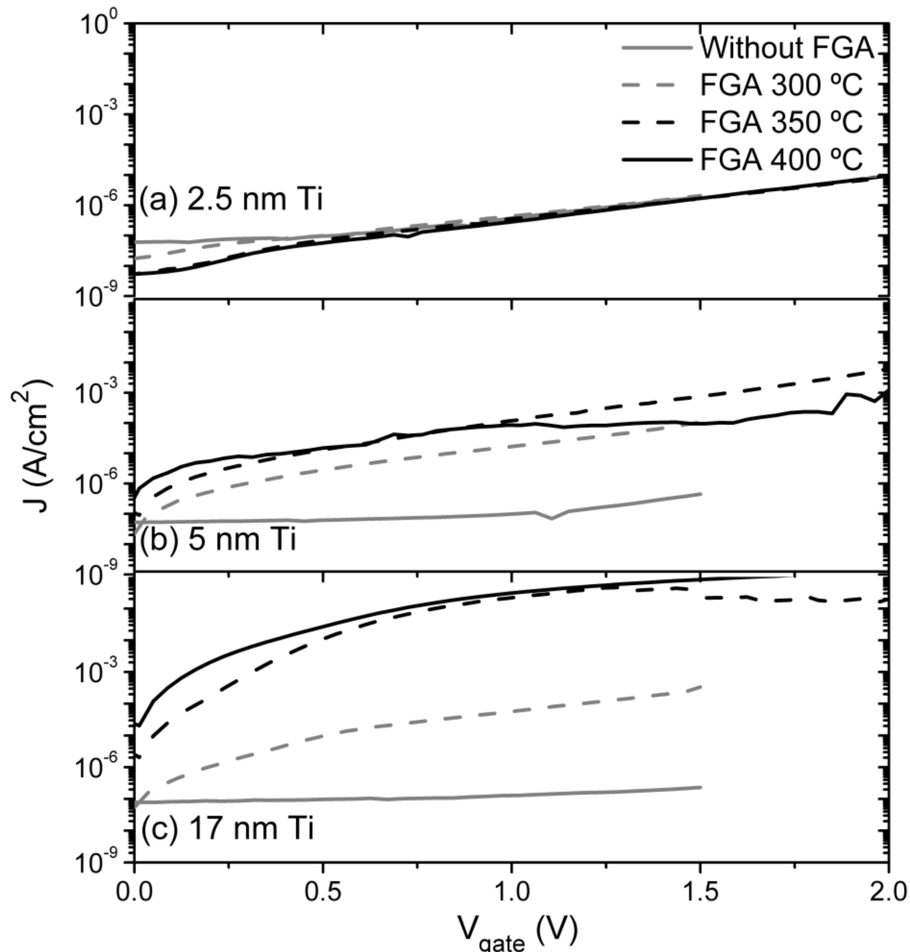

Figure VII.5: J-V_{gate} curves for the sample with 80 s of Gd and 100 s plasma oxidation at 20 W measured before and after several FGAs with different thickness of Ti layers: (a) 2.5 nm, (b) 5 nm and (c) 17 nm.

excessive scavenging in this sample. In any case, when comparing with the same SiO_2 dielectric thickness film of 1.2 nm,[21] much lower values (more than four orders of magnitude lower) were obtained with this Gd_2O_3 layer.

Summarizing these results, 5 nm of Ti together with FGA at 300 °C is the best compromise between scavenging, D_{it} and leakage current. However, more intense scavenging should not be completely discarded, but it would require a metal gate-last process. In other words, after the FGA, the Ti gate should be substituted by a threshold voltage (V_T) control metal followed by an interface improvement process (for instance, FGA at 500 °C during 20 min).

The 5 nm Ti sample after the FGA at 400 ºC was further analyzed. First of all, DLTS measurements give a D_{it} value around 10^{12} $eV^{-1}cm^{-2}$, uniform through the gap (as it is presented in Figure VII.6). These results are in good agreement with the values provided by the conductance method and presented in the right hand side of Figure VII.4.

J-V_{gate} curves at different temperatures are obtained to characterize the leakage current density conduction mechanism. In Figure VII.7(a), two regions can be

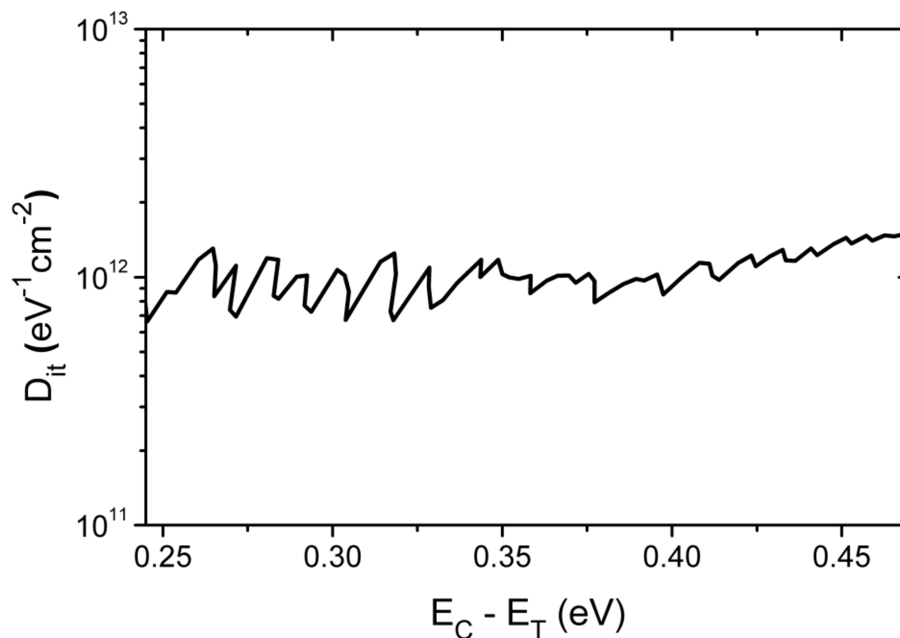

Figure VII.6: Interface trap density obtained by DLTS for sample with 80 s of Gd and 100 s oxidation at 20 W with 5 nm of Ti measured after the FGA at 400 ºC.

distinguished. At low voltages ($V_{gate} < 0.1$ V), current density does not depend on the temperature. Therefore, tunneling is the dominant conduction mechanism in this region.[22] In contrast, for higher voltages, current is thermally activated. This dependency fits well to the Poole-Frenkel effect, that is, trap assisted conduction mechanism is dominant at electric field, E, values higher than 0.7 MV/cm. Figure VII.7(b) shows the plot of J/E (in logarithmic scale) against $E^{1/2}$ at several temperatures, corresponding to this sample with 5 nm of Ti layer and after the FGA at 400 °C. There is a linear dependence in the high-field range, as required by the Poole-Frenkel equation:[23]

$$I = I_0 exp\left(\frac{\beta_{PF}E^{1/2}}{kT}\right)E \qquad \textbf{(VII.1)}$$

where I is the current, I_0, a pre-exponential factor, β_{PF} is the Poole-Frenkel coefficient, E, the applied electric field, k is the Boltzmann's constant and T, the temperature. The obtained value of β_{PF} in the 0.7-1 MV/cm electric field range slightly varies with temperature in the range $(0.7\text{-}1.3)\times10^{-5}$ eVcm$^{1/2}$V$^{-1/2}$. Similar values were obtained in different MIS samples with Gd_2O_3 fabricated with the same method.[24]

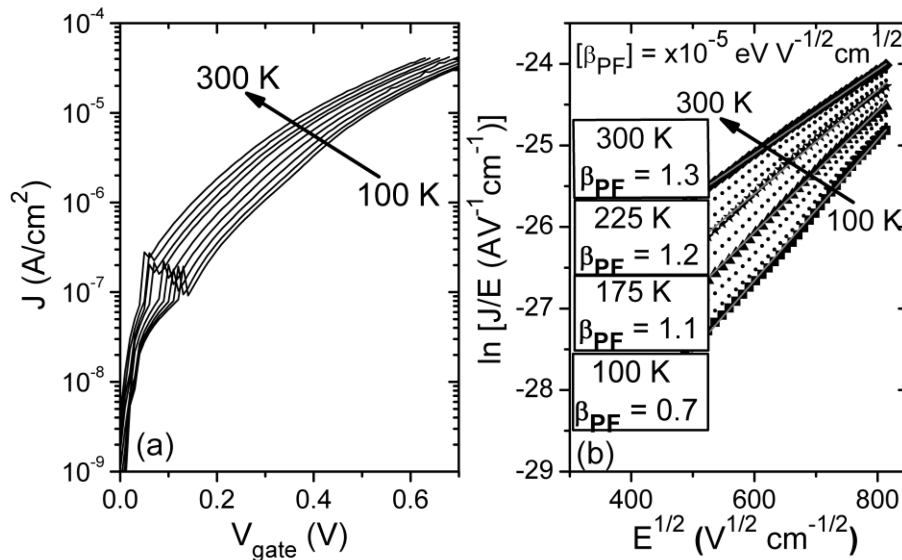

Figure VII.7: (a) J-V_{gate} characteristics measured at different temperatures (from 100 K to 300 K) and (b) current electric field dependency fitting following the Poole-Frenkel model at several temperatures for the Si sample with 5 nm of Ti and after the FGA at 400 °C. The β_{PF} parameter is shown in the figure.

To complete the electrical study, the frequency dispersion of the C-V_{gate} curves for this Ti sample annealing at 400 °C is shown in the left hand side of Figure VII.8. All measured frequencies (from 1 kHz to 1 MHz) present almost the same value of the accumulation capacitance, except the one at 1 MHz, which is around 10% lower than the others. This reduction in the capacitance is due to combined effect of the series resistance with a high conductance (over ~1 S/cm^2 at gate voltages above 0 V) measured at this high frequency. Similar results were obtained for the Pt sample (presented in figure V.29). The hump of the C-V_{gate} curve in depletion due to the interface traps decreases when increasing frequency. The D_{it} values obtained from this figure by using the conductance method decrease almost one order of magnitude as the frequency is increased (from 2×10^{12} to 4×10^{11} eV^{-1}cm^{-2}). This means that most of the traps can follow the *ac* signal even at moderately high frequencies. The same behavior in similar samples but using pure Pt as top metal was observed previously in chapter V. This can be related to the existence of a border trap distribution inside the dielectric. As border traps are located further away from the interface, emission and capture time constants exponentially decrease with the distance from the interface.[25] Therefore, only traps at the interface contribute to conductance values at high frequency.

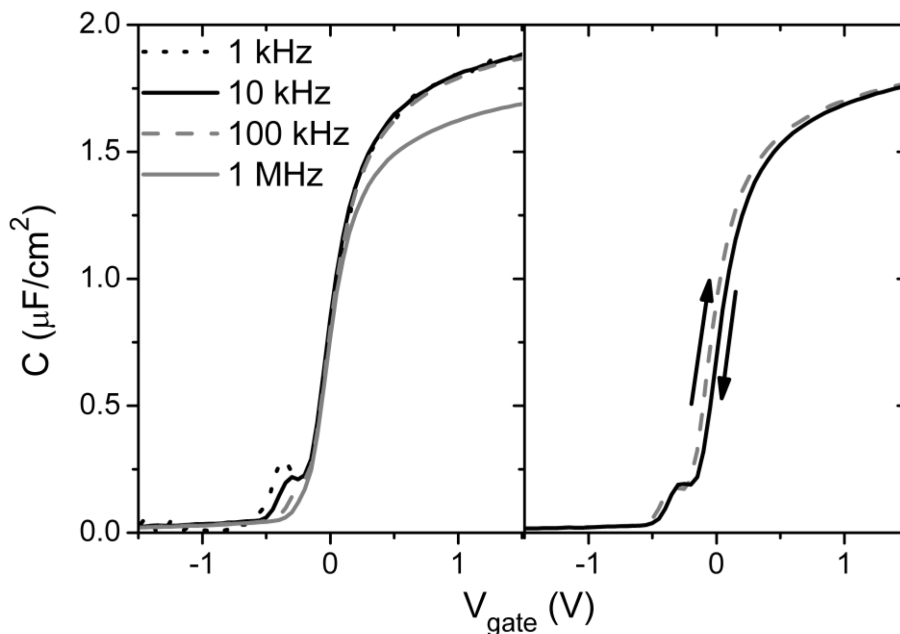

Figure VII.8: C-V_{gate} frequency dispersion curves measured from 1 kHz to 1 MHz (left) and hysteresis measured at 10 kHz (right) for the sample fabricated with 5 nm of Ti and after the FGA at 400 ºC.

The C-V_{gate} hysteresis characteristic measured at 10 kHz is presented in the right hand side of Figure VII.8 after the FGA at 400 °C. The curve is obtained from inversion to accumulation and back again. The flatband voltage (V_{FB}) shift is around 56 mV. These results are similar to other works reported[18,26] and to that obtained for the Pt sample in chapter V (and shown in figure V.28(a)). This indicates that the FGA passivates most of the defects inside the Gd_2O_3 film that act as slow traps.

As a conclusion of this section, the choice of a proper thickness of the Ti layer (5 nm) enables the reduction of the interfacial oxide without compromising the leakage and the performance of the devices. Admissible values for the current density and the D_{it} are achieved for samples with an EOT of around 1.2 nm.

2.3.- Scavenging effect for plasma oxidized Sc_2O_3

Once it has been proved that the scavenging effect was compatible with Gd_2O_3 films and that this effect could be controlled with the thickness of the Ti overlayer and the annealing temperature, in this section, the compatibility of the scavenging effect was studied using MIS devices with Sc_2O_3. These MIS capacitors were fabricated with FOX and with 80 s of Sc and a plasma oxidation of 100 s (performed at 20 W). With these conditions, it was shown (in figure V.32) that the dielectric thickness was around 3.6 nm, much lower than in the Gd case. Therefore, in order to control the scavenging effect, 5 nm of Ti (capped with Pt) was used as top electrode.

Figure VII.9 depicted the area normalized capacitance as a function of the gate voltage for the Sc_2O_3 devices before (left) and after the FGA at 300 ºC (right) for the Ti capacitors (in black). It is also presented the Pt devices (in grey) as a reference. The as deposited capacitors with Ti show an important increase in the accumulation capacitance value compared to the Pt one (from ~1.8 to ~2.4 μF/cm^2), as it can be observed in the left hand side of this figure. Thus, in this case, the scavenging effect produced during the Ti e-beam evaporation is more intense than in the Gd_2O_3 case. After the FGA at 300 ºC, a capacitance roll off is caused due to an aggressive scavenging produced in these samples. This effect is more significant than in the former section with Gd_2O_3. It is important to highlight that the thickness of the Sc_2O_3 film is only 3.6 nm (2.6 nm plus an interlayer of 1.0 nm) and, therefore, the conductance is

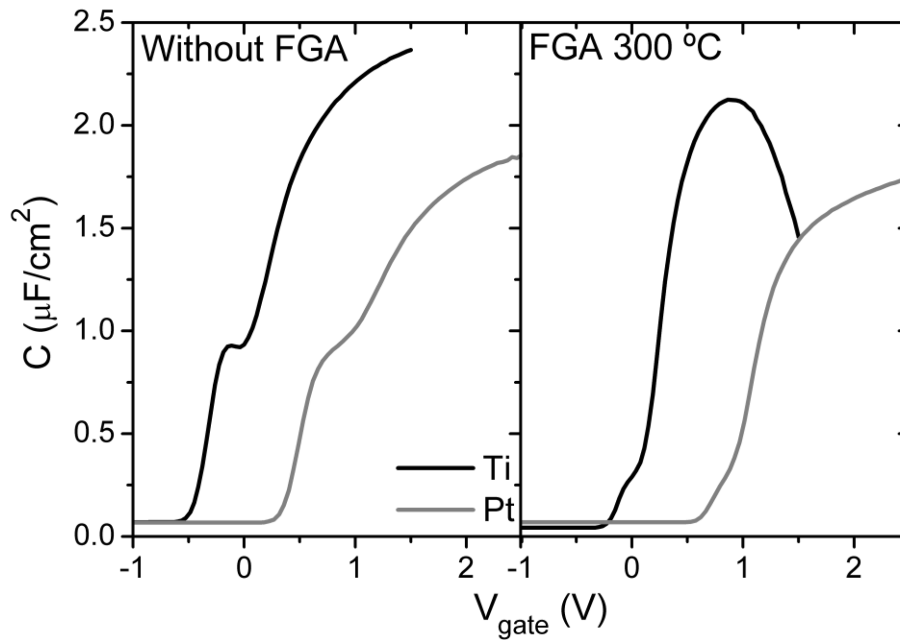

Figure VII.9: C-V_{gate} curves for the sample with 80 s of Sc and 100 s plasma oxidation at 20 W measured before (left) and after the FGA at 300 ºC (right) for two different electrodes: 5 nm of Ti capped with Pt (in black) and Pt (in grey as a reference).

high even for the as deposited sample when using 5 nm of Ti (this value is close to 2×10^{-1} S/cm^2 for V_{gate} higher than 1.5 V, more than one order of magnitude higher compared to the Pt sample, and increases to ~4 S/cm^2 after the FGA at 300 ºC).

Besides, in Figure VII.9, there is a shift of the V_{FB} between the Ti electroded capacitor and the Pt one, before and after the FGA. Ideally, Ti should have a V_{FB} around 1 V lower than Pt,[27] which is in good agreement with the results observed in this figure.

In Table VII.2 is represented the EOT and the D_{it} values for both electrodes before and after the FGA at 300 ºC. The EOT is reduced 0.3 nm only by changing the top electrode from Pt to Ti, reaching a value of 1.2 nm, for the as deposited sample. After the FGA, due to the drop in the accumulation capacitance related to the high conductance, this value could not be obtained using.[15] In the case of the D_{it}, a slight reduction is achieved with the annealing, due to hydrogen passivation.

	Without FGA		FGA 300 ºC	
Metallic contact	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)	EOT (nm)	D_{it} ($eV^{-1}cm^{-2}$)
Ti/Pt	1.2	5×10^{12}	---	1×10^{12}
Pt	1.5	4×10^{12}	1.6	7×10^{11}

Table VII.2: EOT and D_{it} values extracted from electrical measurements before and after the FGA at 300 ºC for samples with 80 s of Sc and a plasma oxidation of 100 s (at 20 W) with two different top electrodes: 5 nm of Ti capped with Pt and Pt layers.

The same effect commented before with the C-V_{gate} characteristics is observed in the current density, presented in Figure VII.10: it increases its value around three orders of magnitude (from 10^{-4} to 10^{-1} A/cm^2 at 1.5 V) when changing the top electrode from Pt to Ti and before the FGA. Besides, the FGA at 300 ºC, increases up this value over 1 A/cm^2. In this case, the EOT of these samples is around (or lower than) 1.2 nm. There is uncertainty due to the capacitance roll off. MOS devices fabricated with this thickness of SiO_2[21] presented values around two or three orders of magnitude higher.

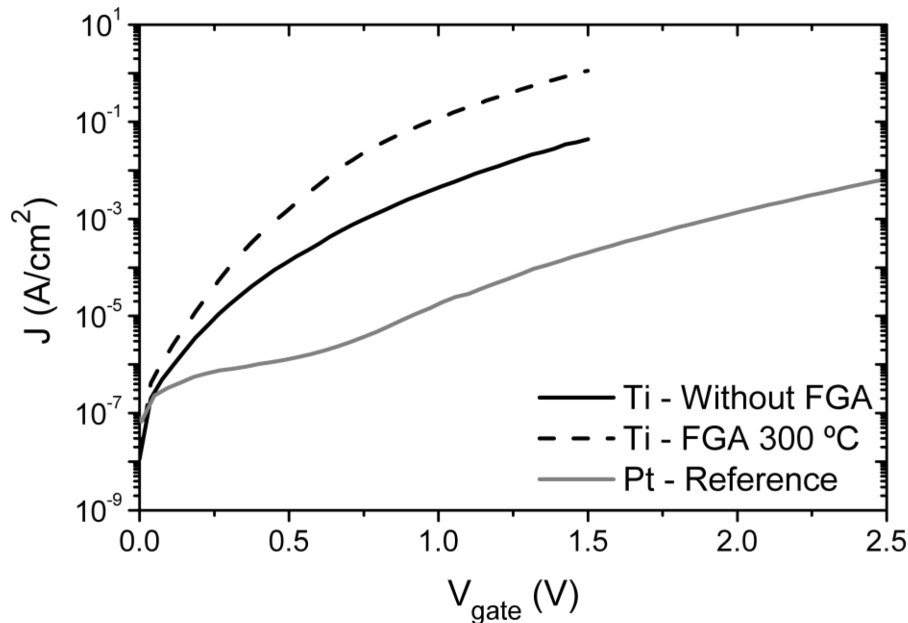

Figure VII.10: J-V_{gate} characteristics for the Sc_2O_3 sample (80 s of Sc and 100 s oxidation at 20 W) measured before (solid lines) and after the FGA at 300 ºC (dashed lines) for 5 nm of Ti capped with Pt (in black). As a reference, the Pt sample is represented in grey.

As a conclusion of this section, it had been proved that the scavenging effect is also compatible with Sc_2O_3 films grown with the two-step method. In fact, for these thin films scavenging was found even before performing the FGA because of the heating during e-beam evaporation. Due to the lower growth rate for this material, the control of the thickness of the Ti layer is very important for the proper device performance in order to have low leakage currents.

2.4.- Scavenging effect for plasma oxidized $Gd_{0.9}Sc_{1.1}O_3$

Finally, the scavenging effect produced by Ti electrodes is studied for MIS devices (with FOX) grown with $Gd_{0.9}Sc_{1.1}O_3$ as dielectric. This high κ material was obtained from a nanolaminate of thin Gd and Sc layers followed by a plasma oxidation (the same samples of chapter VI). As it was commented in the former chapter, the gadolinium scandate need a temperature treatment to mix the nanolaminate and form a homogeneous layer of 5.0 nm thick with 0.9 nm of IL (shown in figure VI.15). Therefore, the Ti layer (with a thickness of 5 nm) was evaporated after a FGA of the $Gd_{0.9}Sc_{1.1}O_3$ at 600 ºC during 5 min, in order to obtain a mixed layer and to ensure the formation of the gadolinium scandate before the scavenging process. After Ti evaporation to improve the metallic contacts and produce scavenging, a FGA at 300 ºC for 20 min was performed. The devices were measured before and after this second FGA.

In Figure VII.11 is represented the area normalized capacitance as a function of the gate voltage for the capacitors with $Gd_{0.9}Sc_{1.1}O_3$ as dielectric. The Ti devices (in black) after the FGA at 600 ºC but before the FGA at 300 ºC (solid line) present a significant increase in the accumulation capacitance compared to the Pt samples after the FGA at 600 ºC (shown as a reference in grey) from 1.9 to ~2.2 $\mu F/cm^2$. Again, this increase is due to the scavenging effect produced during the Ti evaporation, as it was also observed for the other dielectrics analyzed in this chapter. It is important to remember that in these devices, the IL is only 0.9 nm thick and thus, a small reduction in the thickness of this layer would clearly increase the capacitance. Besides, a proper election of the Ti thickness is desirable, aiming of the absence of degradation of the dielectric. Additionally, a slight accumulation capacitance roll off is observed for this Ti

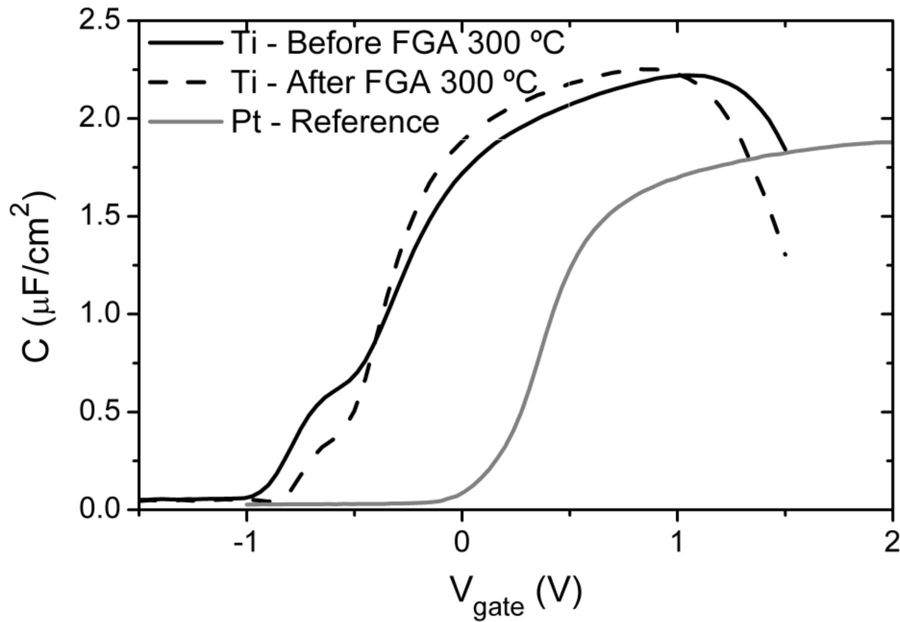

Figure VII.11: C-V_{gate} characteristics of capacitors with $Gd_{0.9}Sc_{1.1}O_3$ formed after a FGA at 600 ºC using Ti as top electrode (in black) before (solid line) and after a second FGA at 300 ºC (dashed line). The same dielectric with Pt is represented as a reference in grey.

sample for $V_{gate} > 1.0$ V, which is related to a high normalized conductance, that is higher than 2×10^{-1} S/cm^2, two orders of magnitude higher than in the Pt case.

Besides, a shift of around 1 V is observed in the V_{FB} for the Pt and Ti samples which is in accordance with the theory.[27]

The impact of performing the second FGA at 300 ºC (represented in black dashed line) does not evidently change the accumulation capacitance. The EOT value is around 1.2 nm for the Ti sample before and after annealing. Due to the capacitance roll off, it is difficult to obtain the value after the FGA. However, it seems that the EOT decreases slightly after the second FGA at 300 ºC due to the scavenging effect. Remember that the Pt sample presented an EOT of 1.5 nm. Thus, the scavenging effect is significant when changing the top electrode.

Furthermore, the D_{it} is high (~10^{13} eV^{-1}cm^{-2}) for the Ti devices before and after the second FGA due to the formation of extra dangling bonds at the dielectric/Si interface, as it was commented before and was also reported in other work[16] related to the scavenging effect. This value is almost two orders of magnitude higher than the Pt

case, which was in the 10^{11} $eV^{-1}cm^{-2}$ range. However, performing the second FGA seems to improve the D_{it}, since the hump in depletion is smaller and the C-V_{gate} curve presents less stretch-out. These two effects are related to a lower D_{it}, as it was stated in chapter III.

Figure VII.12 depicts the leakage current density versus gate voltage characteristics for the devices with $Gd_{0.9}Sc_{1.1}O_3$. The same effects mentioned in the former paragraphs are observed in this figure. The Ti sample before the second FGA increases the leakage current around two orders of magnitude with respect to the Pt device (~6×10^{-1} and ~3×10^{-3} A/cm^2, respectively, at 1.5 V). This is related to the accumulation capacitance increase due to the scavenging effect produced by the Ti evaporation. Performing a second FGA at 300 ºC, slightly increase the current density to a value over 1 A/cm^2, which is a confirmation that there is some further scavenging during this FGA promoted by the temperature. However, comparing these values with 1.2 nm of SiO_2,[21] the leakage current density for this $Gd_{0.9}Sc_{1.1}O_3$ layer is much lower than that obtained for SiO_2.

The main conclusion of this section is that the compatibility of the scavenging effect has been demonstrated with gadolinium scandate formed by our optimized

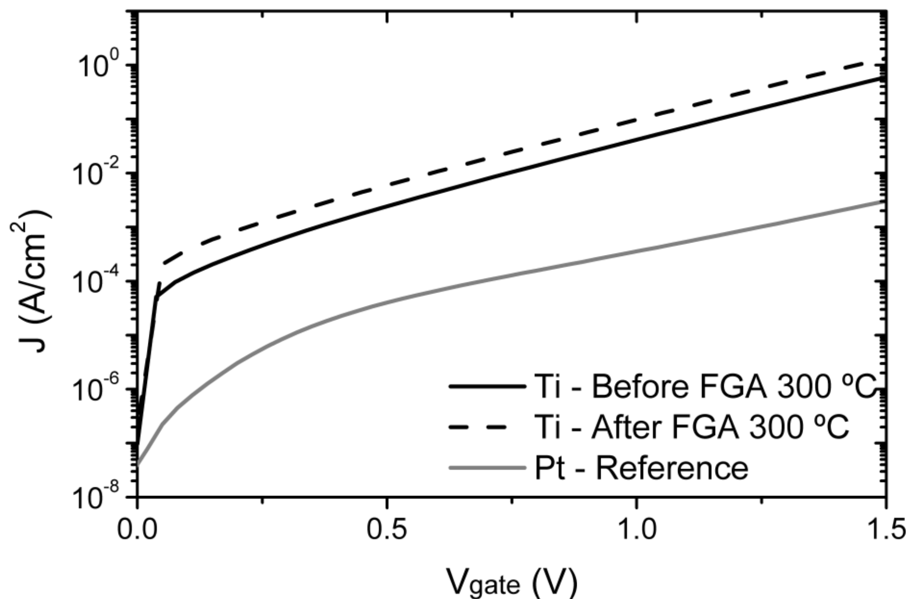

Figure VII.12: J-V_{gate} curves for the $Gd_{0.9}Sc_{1.1}O_3$ sample formed after a FGA at 600 ºC measured before (solid line) and after a second FGA at 300 ºC (dashed line) with 5 nm of Ti capped with Pt (in black). As a reference, the Pt sample is represented in grey.

two-step HPS process. An increase in the accumulation capacitance is achieved after the evaporation of the Ti metallic contact, accompanied by a reduction in the EOT of around 0.3 nm. Due to the lower IL thickness of these samples compared to the Gd_2O_3 devices, the scavenging effect is more significant and a proper election of the Ti thickness is critical to achieve a reduction of the SiO_x layer without compromising the dielectric quality.

VII.3.- SUMMARY AND CONCLUSIONS

In this chapter, the scavenging effect has been proved with MIS capacitors grown with Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ as dielectrics and using Ti as metallic electrode. For these three high κ materials, a clear increase in the accumulation capacitance was achieved. Therefore, a decrease in the EOT value was obtained. This effect was noticeable even before the temperature treatment, due to the infrared radiation produced during the Ti evaporation.

A suitable choice of the Ti overlayer thickness and the FGA temperature is crucial in order to achieve the desirable scavenging effect. This means a decrease of the SiO_x IL, accompanied by a lower EOT value but without degrading the dielectric material or compromising the electrical behavior of the MIS devices.

For the $Gd_{0.9}Sc_{1.1}O_3$ samples, the minimum EOT obtained with Ti is 1.2 nm, 0.3 nm lower than in the Pt case. This reduction is followed by an increase in the D_{it} and in the leakage current density, thus, a moderate degradation of the high κ material. One solution to control this would be to reduce the Ti thickness. In any case, from a production point of view after a controlled scavenging process that optimizes the EOT value, the Ti scavenging gate should be removed and replaced by other metallic stack followed by a FGA to passivate the interfacial defects in a gate-last process.[28]

REFERENCES

[1] H. Kim, P. C. McIntryre, C. O. Chui, K. C. Saraswat, S. Stemmer. "*Engineering chemically abrupt high-k metal oxide/silicon interfaces using an oxygen-gettering metal overlayer*". J. Appl. Phys., 96, 3467 (2004).

[2] K. I. Seo, D. I. Lee, P. Pianetta, H. Kim, K. C. Saraswat, P. C. McIntyre. "*Chemical states and electrical properties of a high-k metal oxide/silicon interface with oxygen-gettering titanium-metal-overlayer*". Appl. Phys. Lett. 89, 142912 (2006).

[3] K. Nakajima, A. Fujiyoshi, Z. Ming, M. Suzuki, K. Kimura. "*In situ observation of oxygen gettering by titanium overlayer on $HfO_2/SiO_2/Si$ using high-resolution Rutherford backscattering spectroscopy*". J. Appl. Phys., 102, 064507 (2007).

[4] L.-Å. Ragnarsson, Z. Li, J. Tseng, T. Schram, E. Rohr, M. J. Cho, T. Kauerauf, T. Conard, Y. Okuno, B. Parvais, P. Absil, S. Biesemans, T. Y. Hoffmann. "*Ultra low-EOT (5 Å) gate-first and gate-last high performance CMOS achieved by gate-electrode optimization*". IEEE International Electron Device Meeting (IEDM) 663, (2009).

[5] T. Ando, M. Copel, J. Bruley, M. M. Frank, H. Watanabe, V. Narayanan. "*Physical origins of mobility degradation in extremely scaled SiO_2/HfO_2 gate stacks with La and Al induced dipoles*". Appl. Phys. Lett., 96, 132904 (2010).

[6] C. Choi, J. C. Lee. "*Scaling equivalent oxide thickness with flat band voltage (V_{FB}) modulation using in situ Ti and Hf interposed in a metal/high-k gate stack*". J. Appl. Phys., 108, 064107 (2010).

[7] L.-Å. Ragnarsson, T. Chiarella, M. Togo, T. Schram, P. Absil, T. Y. Hoffmann. "*Ultrathin EOT high-κ/metal gate devices for future technologies: Challenges, achievements and perspectives (invited)*". Microelectron. Eng., 88, 1317 (2011).

[8] T. Ando. "*Ultimate scaling of high-κ gate dielectrics: higher-κ or interfacial layer scavenging?*". Materials, 5, 478 (2012).

[9] M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. Toledano-Luque, A. del Prado, A. J. Blázquez, M. L. Lucía. "*Towards metal electrode interface scavenging of rare-earth scandates: A Sc_2O_3 and Gd_2O_3 study*". Microelectron. Eng., 88, 1357 (2011).

[10] A. Gómez. H. Castán, H. García, S. Dueñas, L. Bailón, M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Interface quality of Sc_2O_3 and Gd_2O_3 films based metal-insulator-silicon structures using Al, Pt and Ti gates: Effect of buffer layers and scavenging electrodes*". J. Vac. Sci. Technol. B, 31, 01A106 (2013).

[11] M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. L. Lucía. "*Optimization of in situ plasma oxidation of metallic gadolinium thin films deposited by high pressure sputtering on silicon*". J. Vac. Sci. Technol. B, 31, 01A112 (2013).

[12] M. A. Pampillón, P. C. Feijoo, E. San Andrés, H. García, H. Castán, S. Dueñas. "*Scavenging effect on plasma oxidized Gd_2O_3 grown by high pressure sputtering on Si and InP substrates*". Semicond. Sci. Technol., 30, 035023 (2015).

[13] E. H. Nicollian, A. Goetzberger. "*The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique*". Bell Syst. Tech. J., 46, 1055 (1967).

[14] D. V. Lang. "*Deep level transient spectroscopy: A new method to characterize traps in semiconductors*". J. Appl. Phys., 45, 3023 (1974).

[15] J. R. Hauser, K. Ahmed. "*Characterization of ultra-thin oxides using electrical C-V and I-V measurements*". AIP Conf. Proc., 449, 235 (1998).

[16] F. Cerbu, A. P. D. Nguyen, J. Kepa, V. V. Afanas'ev, A. Stesmans. "*Generation of Si dangling bond defects at Si/insulator interfaces induced by oxygen scavenging*". Phys. Status Solidi B, 251, 2193 (2014).

[17] J. J. Huang, L. T. Huang, M. C. Tsai, M. H. Lee, M. J. Chen. "*Enhancenment of electrical characteristics and reliability in crystallized ZrO_2 gate dielectrics treated with in-situ atomic layer doping*". Appl. Surf. Sci., 305, 214 (2014).

[18] Q. Q. Sun, A. Laha, S. J. Ding, D. W. Zhang, H. J. Osten, A. Fissel. "*Effective passivation of slow interface states at the interface of single crystalline Gd_2O_3 and Si(100)*". Appl. Phys. Lett., 92, 152908 (2008).

[19] P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Optimization of gadolinium oxide growth deposited on Si by high pressure sputtering*". J. Vac. Sci. Technol. B, 31, 01A103 (2013).

[20] R. Endres, T. Krauss, F. Wessely, U. Schwalke. "*Damascene TiN-Gd_2O_3-gate stacks: gentle fabrication and electrical properties*". Microelectron. Eng., 88, 3393 (2011).

[21] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, L. O. Shih-Hsien, G. A. Sai-Halasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind, H. S. Wong. "*CMOS scaling into the nanometer regime*". IEEE International Electron Device Meeting (IEDM), 85, 486 (1997).

[22] F. C. Chiu. "*A review on conduction mechanisms in dielectric films*". Advances in Materials Science and Engineering, 2014, 578168 (2014).

[23] J. Frenkel. "*On pre-breakdown phenomena in insulators and electronic semiconductors*". Physical Review, 54, 647 (1938).

[24] A. Gómez, H. Castán, H. García, S. Dueñas, L. Bailón, M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Interface quality of Sc_2O_3 and Gd_2O_3 films based metal-insulator-silicon structures using Al, Pt and Ti gates: Effect of buffer layers and scavenging electrodes*". J. Vac. Sci. Technol. B, 31, 01A106 (2013).

[25] S. Dueñas, R. Peláez, E. Castán, R. Pinacho, L. Quintanilla, J. Barbolla, I. Mártil, G. González-Díaz. "*Experimental observation of conductance transients in Al/SiN_x:H/Si metal-insulator-semiconductor structures*". Appl. Phys. Lett., 71, 826 (1997).

[26] T. M. Pan, C. S. Liao, H. H. Hsu, C. L Chen, J. D. Lee, K. T. Wang. "*Excellent frequency dispersion of thin gadolinium oxide high-k gate dielectric*". Appl. Phys. Lett., 87, 262908 (2005).

[27] E. H. Nicollian and J. R. Brews. "MOS (Metal Oxide Semiconductor): Physics and Technology". John Wiley & Sons. New York, 1982.

[28] T. Y. Hoffman. "*Integrating high-k/metal gates: gate-first or gate-last?*" Solid State Technology, 53, 20 (2010).

Chapter VIII:

Gd_2O_3 on InP substrates

As it was mentioned in the introduction, one possibility to continue with CMOS scaling is the substitution of the Si channel with high mobility semiconductors, such as III-V materials.1 One of the main challenges of these semiconductors is to obtain a good interface with the high κ material, with a low interfacial states density, D_{it}. This means to achieve an unpinned Fermi level with well behaved electrical characteristics.1[,2]

Among all the III-V semiconductors, InP is a potential candidate because it has a high electron mobility and high breakdown field. Some works had reported good electrical characteristics with high κ/InP MOSFETs.3[,4]

In this chapter, MIS devices grown on InP are studied using Gd_2O_3 as the high κ dielectric. The compatibility of this material with III-V substrates had been proved in different works,[5-]8 but only one work used sputtering to deposit the high κ dielectric.9 In this thesis to deposit the high κ material, the two-step procedure developed in former chapters by means of HPS was used.

Electrical measurements (C-V_{gate} and G-V_{gate} measured at different frequencies and also J-V_{gate} curves) were carried out on the MIS devices before and after the forming gas anneal (FGA). Different top electrodes were explored: Pt/Al, pure Pt and also Ti (capped with Pt), in order to check the compatibility with the scavenging effect. HRTEM images and scanning TEM (STEM) analysis were performed for the annealed sample. Together with the STEM imaging, the electron energy loss spectra (EELS) were recorded.

VIII.1.- EXPERIMENTAL METHOD

MIS devices grown on undoped InP wafers (thus, n-type behavior) were fabricated with Gd_2O_3 obtained from the two-step method. In these devices around 200 nm of evaporated SiO_x acting as field oxide (FOX) was introduced for improving the electrical measurements. The capacitance equivalent thickness (CET) downscaling of these high electron mobility substrate devices was not so critical, so, for this study, thicker Gd_2O_3 layers were grown aiming to obtain lower leakage current density. Therefore, in the first experiment, the Gd metallic layers were deposited during 120 s in an Ar atmosphere at 30 W. Afterwards, without breaking the vacuum, these films were *in situ* oxidized in a mixed Ar/O_2 plasma for 200 s at 20 W of *rf* power. Both processes were carried out at room temperature and at 0.50 mbar of pressure. Besides, in the second experiment, in order to optimize the CET, other initial Gd deposition durations were explored: from 60 to 180 s , followed by an oxidation during 100 s at 20 W.

The backside contact was a stack formed with 100 nm of AuGe and 100 nm of Au, which ensures ohmic contact to n-InP wafers.[10]

In this chapter we have used the CET value because we did not have a simulation program for InP substrates.

VIII.2.- RESULTS AND DISCUSSION

2.1.- Feasibility of plasma oxidized Gd_2O_3 deposited on InP substrates

The main objective of this section is to demonstrate the possibility of fabricating MIS devices using InP as substrate and a high κ dielectric deposited by means of HPS with the two-step procedure developed in former chapters. To accomplish this, MIS devices grown on InP substrates were fabricated with a Gd film deposited for 120 s and plasma oxidized during 200 s at 20 W. The top electrode was 8 nm of Pt capped with 50 nm of Al, to ensure a thick metal contact. The capacitors were electrically measured before and after a FGA at 400 ºC for 20 min. To avoid phosphorous loss, the samples were placed upside down on a bare InP wafer used as a holder. Also, Si samples were fabricated in parallel with the same fabrication process to have a reference.

Figure VIII.1 shows the normalized C-V_{gate} and G-V_{gate} characteristics measured at 10 kHz for these InP devices (in black) before (dashed lines) and after annealing at 400 ºC (solid lines). Besides, in grey dashed lines, it is represented the Si sample before the FGA as a reference. First of all, it is observed that the C-V_{gate} of the InP MIS capacitors perform a full accumulation-depletion-inversion sweep, even before the FGA. This indicates an unpinned Fermi level, in other words, a reasonably well behaved interface.[1,2] As it was mentioned, this is one of the main challenges that appears when using III-V substrates. In addition, the accumulation capacitance remains roughly constant before and after the FGA for the InP sample, indicating a negligible interfacial regrowth, with an average value in the order of 0.76 μF/cm^2 (that corresponds to a CET of 4.5 nm). This value is in accordance with those reported in previous works of high κ deposited on high mobility substrates.[9,11,12] For Si devices before the FGA, the accumulation capacitance is around 0.70 μF/cm^2, with a CET value of 4.9 nm, 0.4 nm higher than in the InP case. This CET increase for the Si MIS devices can be attributed to a thicker oxide regrowth at the interface between the dielectric and the semiconductor during the oxidation process, as it was observed in chapter V.

The normalized conductance curves depicted in the right hand side of

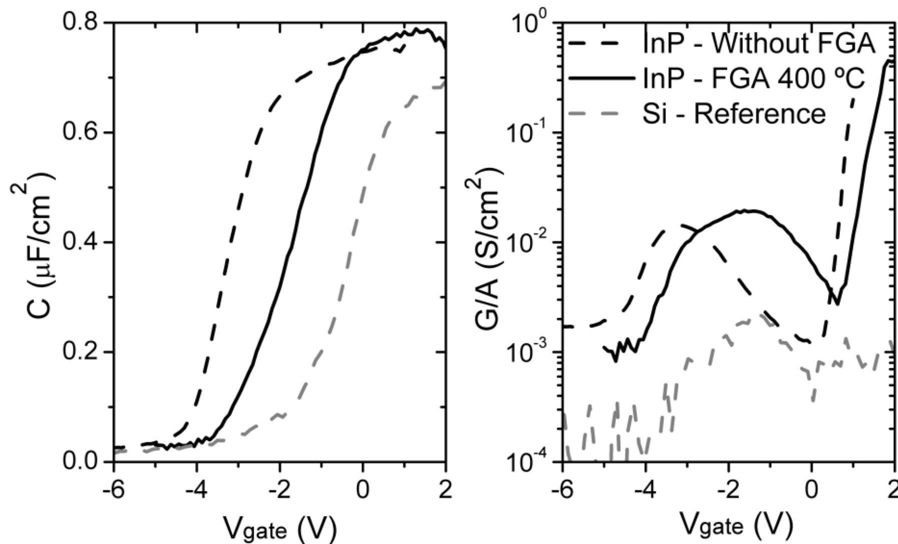

Figure VIII.1: Normalized C-V_{gate} and G-V_{gate} curves measured at 10 kHz before (dashed lines) and after the FGA at 400 ºC (solid lines). In black is represented the InP sample with 120 s of Gd and 200 s of plasma oxidation (performed at 20 W) with Pt/Al. Also, Si sample as a reference is depicted in the figure in grey.

Figure VIII.1 present a well defined peak before and after the temperature anneal. From these curves and using the conductance method[13] a D_{it} value of around 10^{13} $eV^{-1}cm^{-2}$ is obtained for both InP curves. This is similar to other values reported with InP and Al_2O_3 or HfO_2 as dielectrics.[14,15] However, it is important to highlight that in this case, as opposed to most works of high κ on III-V, the surface of the InP was not passivated with any treatment. On the other hand, for the Si case, the D_{it} after the FGA is close to 2-3×10^{11} $eV^{-1}cm^{-2}$.

The HRTEM image of a MIS device grown on InP and annealed at 400 ºC is presented in Figure VIII.2. There, it can be observed that there are not intermediate oxides at the GdO_x/InP interface. This is a very interesting outcome, since this process applied to Si produces a thin SiO_x layer at the interface, around 1–2 nm thick, as it was extensively studied in chapter V. This is in agreement with the higher CET of the Si sample indicated previously. The fact that there is not apparent interlayer between GdO_x and InP, points to a superior oxidation resistance of InP when exposed to the Ar/O_2 plasma and/or in contact with this high κ material. Besides, in this figure, the InP surface seems quite rough, but the origin of this roughness is not clear: it could be an artifact of the image due to the absence of interfacial oxides together with the polycrystalline character of the GdO_x, a reaction of this dielectric with InP or just a

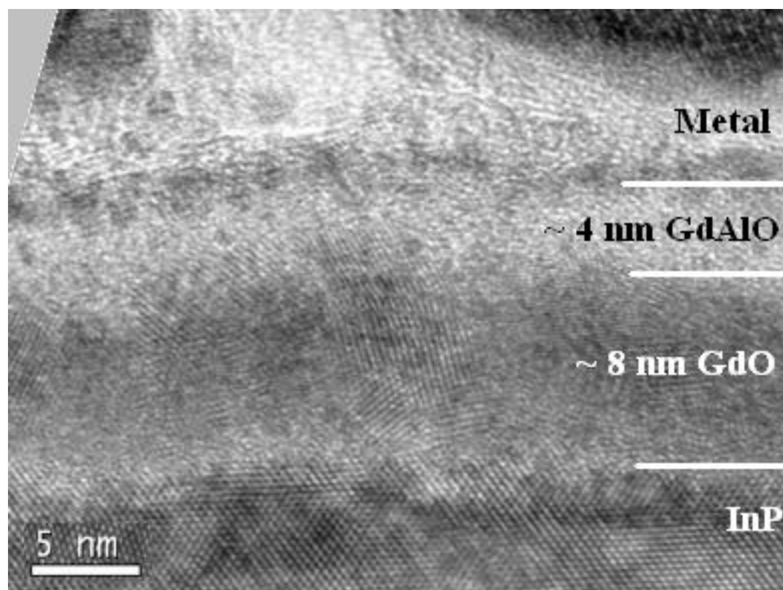

Figure VIII.2: High resolution TEM image of a MIS device with 120 s of Gd and plasma oxidized during 200 s after the annealing at 400 ºC.

rough InP starting surface. As opposed with the Si case, which produces an amorphous Gd_2O_3 (as it was shown in chapter V), here the dielectric presents a polycrystalline character with a thickness of ~8 nm. On top of this layer it is observed a brighter layer ~4 nm thick.

To clarify the composition of these films, in Figure VIII.3 is shown the integrated intensity of the main EELS peaks of each species present in the stack. Concerning the metal gate, it is found that there is an intermixing of the Pt/Al electrode. Furthermore, Al diffuses to the Pt/Gd_2O_3 interface, producing the bright GdAlO layer pointed out in the previous paragraph. A similar Al reaction with GdO_x was found in chapter V (shown in figure V.9(a) for MIS capacitors grown on Si). Since aluminum oxide has a permittivity around 9,[16] it is also expected that the aluminate layer had a smaller permittivity than the pure Gd_2O_3 film. However, the effective κ value of the stack is 12 ± 1, assuming a CET of the semiconductor accumulation layer of 0.7 nm. This value is slightly lower to the reported κ of Gd_2O_3.[16,17] Thus the effect of the aluminate layer is not critical but reduces the permittivity of the high κ material film. The main drawback is that it increases the total thickness of the dielectric stack. This is not desirable for MOSFETs downscaling.

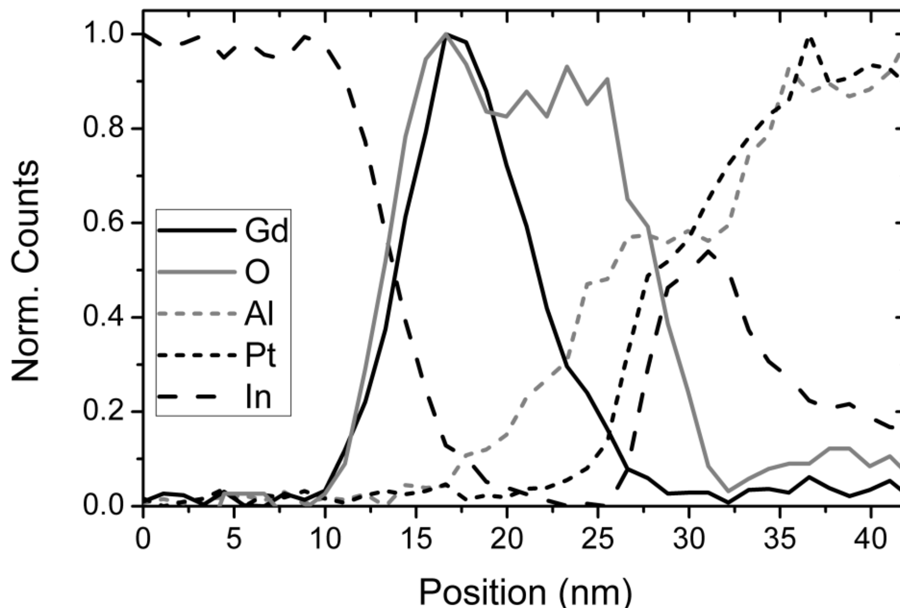

Figure VIII.3: Depth profile of a MIS device (120 s of Gd and 200 s plasma oxidation) with Pt/Al electrode after FGA at 400 ºC obtained from the EELS spectra during STEM measurements. Each emission line was normalized to its maximum value.

Finally, an unexpected feature found is the apparent buildup of indium at the GdAlO/metal interface. Since it was not found any indium peak inside the dielectric layer, it is not likely that the origin of this In is the device substrate, as it was reported for different works using HfO_2 and Al_2O_3.[18-20] As a consequence, this element must be diffusing from the InP wafer which acts as the holder that was in a face-to-face configuration during the FGA. Furthermore, GdO_x seems to be acting as a good In out-diffusion barrier.

As a conclusion of this section, the two-step deposition procedure provides a method to fabricate well behaved MIS devices on InP using Gd_2O_3 as dielectric. However, a reaction observed between the Al electrode and the dielectric was found, which implies a higher CET value. For that reason, to avoid the aluminate formation, the Al electrode should be removed.

2.2.- Optimized devices with Gd_2O_3 on InP

Given the results described in the former section, optimized MIS devices with pure Pt contacts were fabricated in order to improve the CET. The initial Gd thickness was varied by changing the deposition time from 60 to 180 s. The oxidation time was reduced to 100 s for all the thicknesses (carried out at 20 W) to avoid an excessive oxidation of the thinner Gd layer and also to compare the oxidation effect on different Gd thicknesses at the same oxidation conditions.

To minimize phosphorous loss, the FGA temperature of the InP devices was limited to 325 °C. Thus, to ensure a good ohmic contact of the back electrode, the FGA was extended to 30 min. In this case, the annealed was performed for two samples at the same time, placed face-to-face. This way, the In diffusion to the top electrode due to the configuration explained in the former section was avoided.

In Figure VIII.4 it is represented the gate leakage current density of these devices before and after the annealing. Before the FGA (in dashed lines), the leakage is minimal for the devices where the metal was deposited during 120 s, with a value around 10^{-3} A/cm^2 at a V_{gate} of 1 V. This result suggests that the 60 s films were too thin, producing an excessive tunneling current (in the order of 10 A/cm^2 at 1 V), while the 180 s ones are incompletely oxidized, with a worse insulation and a leakage current of

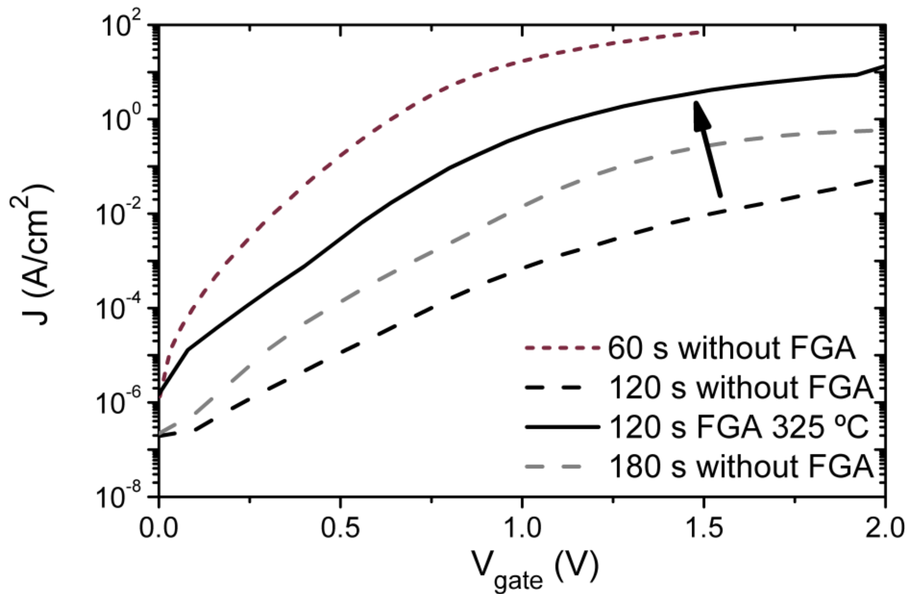

Figure VIII.4: Gate leakage as a function of gate voltage of the InP devices with pure Pt gate electrode and different Gd sputtering times before (dashed lines) and after the FGA at 325 ºC (solid line).

10^{-2} A/cm^2 for the same gate voltage. For that reason, only the sample with 120 s of metal deposition was measured after the FGA (and it is represented in Figure VIII.4 with black solid line). These devices present an increase in the leakage current, around three orders of magnitude, reaching a value close to 1 A/cm^2 at V_{gate} = 1 V. This rise can be associated to a transition from amorphous to polycrystalline, where the leakage current increases because the grain boundaries are more conductive,[21] as it was presented in Figure VIII.2.

Figure VIII.5 shows the normalized C-V_{gate} and G-V_{gate} of the devices with 120 s of Gd deposition time measured at 10 kHz before and after the FGA at 325 ºC. The 60 s devices were too leaky and thus impossible to measure, while the samples with 180 s presented bad insulator properties, possibly due to a non complete oxidation. Therefore, only 120 s devices are shown. It is observed in the left hand side of this figure that the accumulation capacitance remains constant before and after the FGA, with a value slightly lower than 1.4 µF/cm^2. Besides, there are not flatband voltage instabilities. These results indicate that there is not a significative reaction between the semiconductor and the high κ material (as it was also shown in the former section with

the absence of interfacial oxides). The lack of interfacial oxides was also observed in works from other groups using HfO_2 and InP.[18,19,22] This behavior is opposed to the Si case, where the presence of SiO_x at the interface was always found, as it was pointed out in chapter V.

Additionally, it is important to highlight, that this sample has a ~50% higher accumulation capacitance value compared to the devices with Pt/Al electrode shown in the previous section. The CET of this sample is ~2.6 nm (almost 2 nm lower than in the former section). This can be explained by the absence of a GdAlO layer, as expected because, in this case, a pure Pt electrode was used to avoid its reaction with the dielectric. This CET value is similar to other reported in previous works using HfO_2 on InP.[14,22]

According the normalized conductance characteristics shown in the right hand side of Figure VIII.5 and using the conductance method,[13] the D_{it} value obtained is higher than 10^{13} $eV^{-1}cm^{-2}$, both before and after the FGA. This value is similar to that reported in other work using different high κ on InP.[14,15] Also the conductance in accumulation is quite high, due to gate leakage, as it was shown in Figure VIII.4. It is important to highlight that the conductance method is valid to extract the D_{it} on MIS capacitors with relatively low trap densities and with a well passivated surface.[23,24]

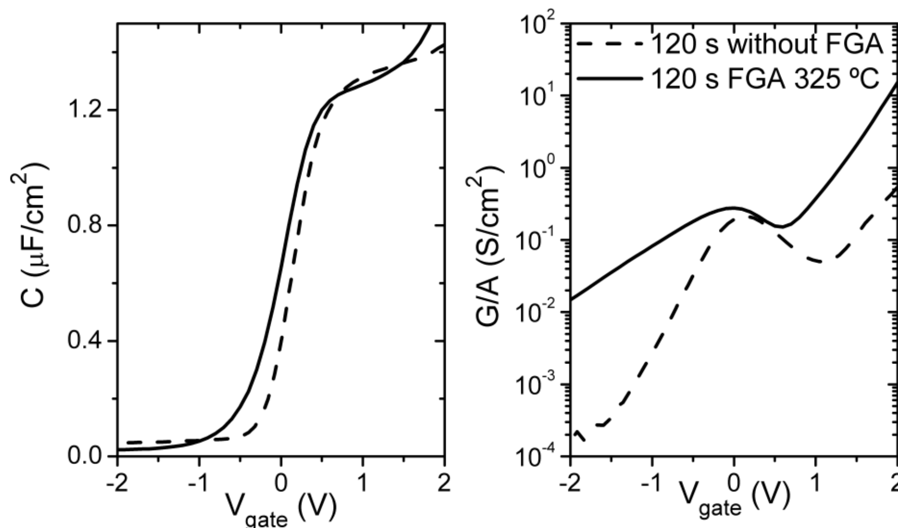

Figure VIII.5: Gate normalized capacitance (left) and conductance (right) vs gate voltage of the devices with 120 s of Gd and a plasma oxidation of 100 s (at 20 W) with pure Pt electrode measured before and after the FGA at 325 ºC.

Additionally, if the oxide capacitance, C_{ox}, is lower than qD_{it}, where q is the electron charge, the conductance method does not provide reliable values.[25] In this case, the InP surface has not been treated with any passivation method, thus, it is expected to obtain a high D_{it}.

Besides, in reference[26] it was shown that the combined effect of series resistance and conductance can produce the incorrect determination of capacitance. Also, a high D_{it} can produce a capacitive signal that could be mistakenly interpreted as gate capacitance.[27] However, these problems can be detected by varying the measuring frequency: if the accumulation capacitance value changes, then the C-V_{gate} curve has to be taken with care. For that reason, in Figure VIII.6 is represented the C-V_{gate} characteristics for the sample with 120 s after the FGA and measured at several frequencies, from 100 Hz to 10 MHz. In this figure, it can be observed that the accumulation capacitance value does not change with frequency. Therefore, we can be quite sure that the measured capacitances are due to the gate dielectric and correctly measured.

Additionally, in Figure VIII.6 is observed a severe V_{FB} shift with the frequency. According to references [28] and [29], the C-V_{gate} frequency dependency can be attributed to

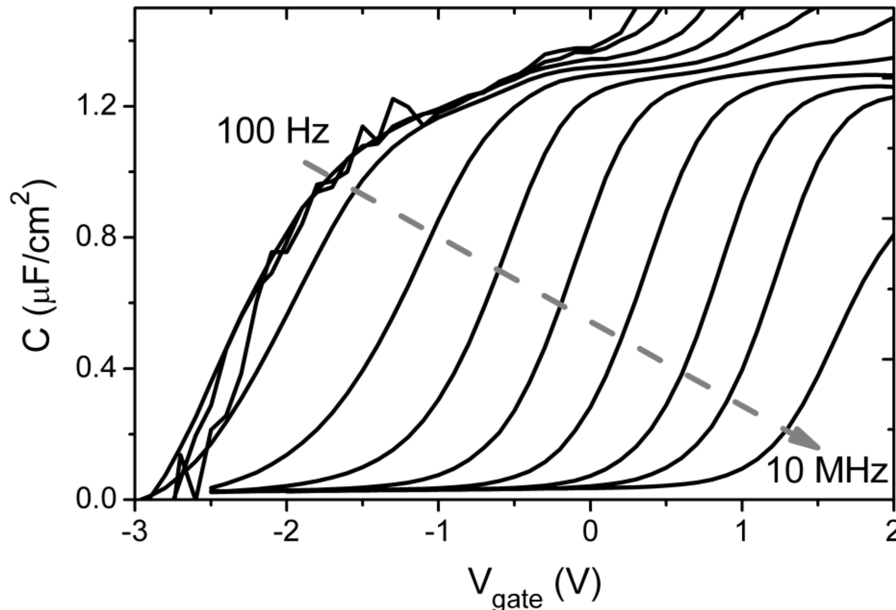

Figure VIII.6: Frequency dispersion C-V_{gate} curves measured from 100 Hz to 10 MHz for the InP sample with 120 s of Gd and 100 s oxidation after a FGA at 325 °C for 30 min.

a high amount of interface traps. Following these references, there is a logarithmic relationship between V_{FB} and frequency, following the next equation:

$$V_{FB}(f) = -\frac{Q_f}{C_{ox}} \mp \frac{kTqD_{it}}{C_{ox}} \mathrm{Ln}\, f \qquad \textbf{(VIII.1)}$$

where Q_f is the fixed oxide charge, k the Boltzmann constant, T the temperature, and f the frequency measured in Hz. C_{ox} is the normalized oxide capacitance and can be extracted from the accumulation value of the capacitance. The ∓ sign stays for acceptor or donor type interface traps, respectively. From this formula, the interface defect density, D_{it}, and the fixed charge, Q_f, can be obtained.

In Figure VIII.7 is represented the V_{FB} data as a function of the measuring frequency. It is observed that under 3 kHz, the flatband voltage remains almost constant, but above this frequency there is a remarkable linear dependence. Halova *et al.*[29] explains this behavior by a characteristic response time of traps, that respond at low frequencies but only partially when the frequency increases. The linear fit for frequencies above 10 kHz is also shown. Using equation (VIII.1), the calculated donor trap density D_{it} is ~10^{14} $eV^{-1}cm^{-2}$, one order of magnitude higher than the value

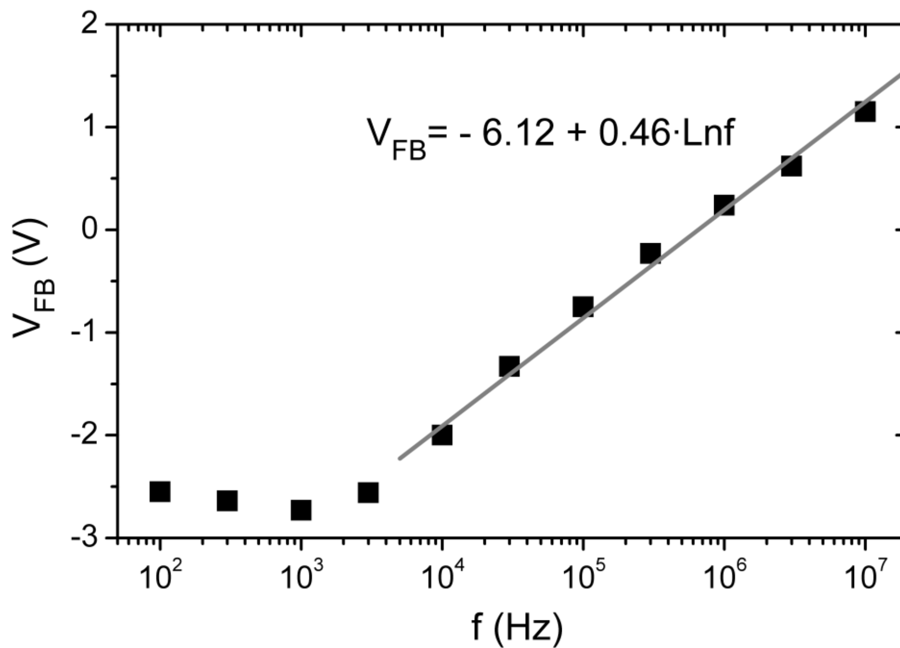

Figure VIII.7: Experimental data for V_{FB} as a function of the frequency measured for the InP sample with 120 s of Gd and a plasma oxidation of 100 s with Pt after the FGA at 325 °C and its linear fit.

obtained by the conductance method. In any case, the D_{it} is too high for MOSFETs applications and a reduction of this value is required. Also, from this fit, the fixed charge obtained is ~$8\cdot10^{-6}$ C/cm^2.

To summarize, the optimized devices with Pt as top electrode achieved a CET of 2.6 nm, thus, an EOT lower than 2.0 nm using InP as substrate. Nevertheless, a passivation treatment is mandatory in order to reduce the high D_{it} value obtained.

2.3.- Interface scavenging with InP

Finally, the scavenging effect using InP as the semiconductor substrate and a stack formed by 5 nm of Ti capped with Pt as metal gate is analyzed. This stack is expected to produce a moderate (and controllable) scavenging effect. In this section, the fabrication process was the same than in the former one: 120 s of Gd and an *in situ* plasma oxidation for 100 s performed at 20 W.

According to the C-V_{gate} curves measured at 10 kHz and depicted in Figure VIII.8, the accumulation capacitance increases clearly after the FGA (from ~1.4 to ~1.75 μF/cm^2). This means a reduction in the CET from 2.5 to 2.0 nm. In the

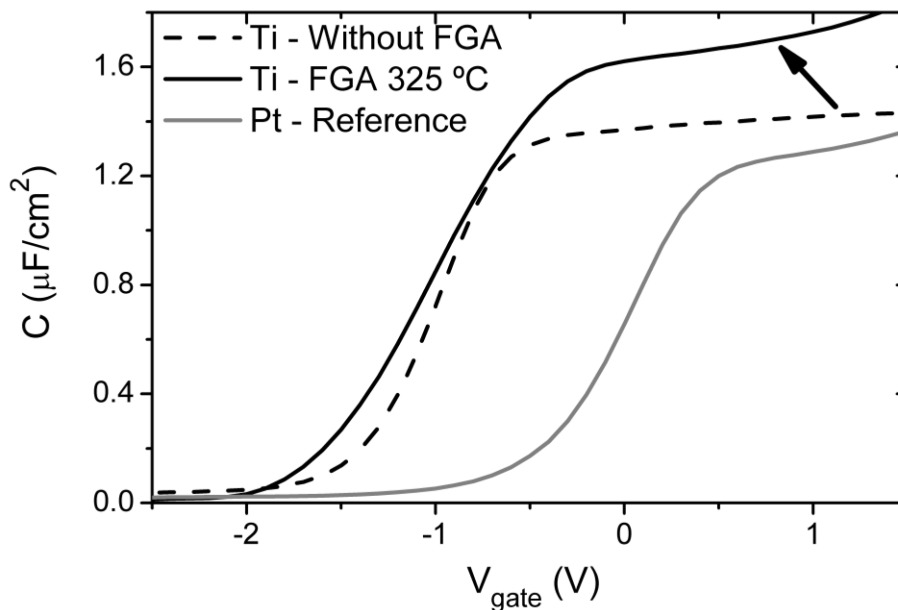

Figure VIII.8: Normalized C-V_{gate} characteristics for the InP sample with 120 s of Gd and 100 s of plasma oxidation at 20 W measured at 10 kHz with 5 nm of Ti before and after the FGA at 325 ºC. The Pt sample is also shown as a reference in grey.

previous section using Pt as top metal and with the same dielectric, the CET was 2.6 nm before and after the FGA. Therefore, the capacitance increase cannot be related to a change in the thickness of the dielectric material or to a permittivity increase.

To be sure that we are measuring correctly the gate capacitance and following the analysis of the former section related to the accumulation capacitance and the flatband voltage shift with the frequency, this sample was measured at several frequencies, from 100 Hz to 10 MHz. The normalized C-V_{gate} curves obtained are represented in Figure VIII.9. Again, the same behavior observed for the Pt sample is seen for these Ti devices: the accumulation capacitance values do not change with the measured frequency. Thus, the accumulation capacitance improvement can be associated to a reduction of the total thickness of the dielectric due to the scavenging effect of Ti in this InP substrate, as it was also found on Si and shown in chapter VII. This effect has been proved in Ge substrates.[30,31] However, at present, this is the first published result on scavenging with high κ on III-V semiconductors.[32]

It is important to remark that, as it was noted for the Si sample, the scavenging effect is even taking place before the FGA due to infrared heating during the Ti evaporation.

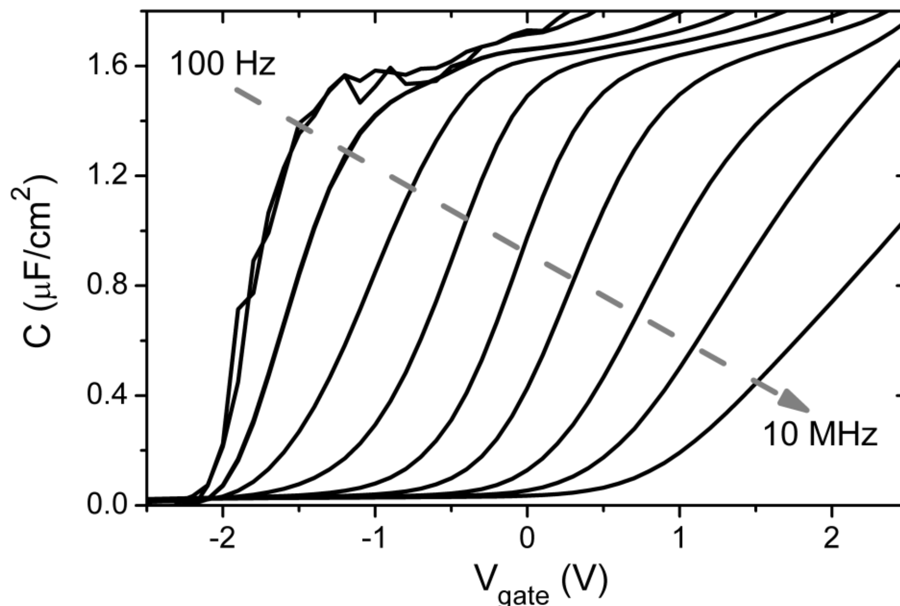

Figure VIII.9: C-V_{gate} curves measured at several frequencies (from 100 Hz to 10 MHz) for the InP sample with Ti after the FGA at 325 ºC.

Representing V_{FB} as a function of the measured frequency, a linear dependence is also observed for frequencies higher than 3 kHz. It is not shown here because it is similar to the Pt case. Using equation (VIII.1), the D_{it} and the Q_f can be obtained. The linear fit in this case is:

$$V_{FB} = -5.05 + 0.37Lnf \qquad \textbf{(VIII.2)}$$

Therefore, the D_{it} is again ~10^{14} $eV^{-1}cm^{-2}$ and Q_f is around $8 \cdot 10^{-6}$ C/cm^2, the same values than for the Pt case. This obtained D_{it} is extremely high and a reduction of this value is mandatory. It is important to remember that these samples have not any passivation treatment. Thus, this could be achieved with surface passivation as it was reported in other works, for instance, nitrogen plasma exposure before HPS process,[33] Si interfacial passivation,[34] a $(NH_4)_2S$ treatment before high κ deposition,[12,22,35-37] *in situ* fluorination,[38] a Ge interlayer,4 etc.

Finally, concerning gate leakage, in Figure VIII.10 is depicted the J-V_{gate} curves for this Ti sample. There, it can be observed a slight increase (less than one order of magnitude) in the current density after the FGA (from 10^{-3} A/cm^2 to less than 10^{-2} A/cm^2 at 1.5 V). This is also consistent with the reduction of the total dielectric thickness due to the scavenging effect.

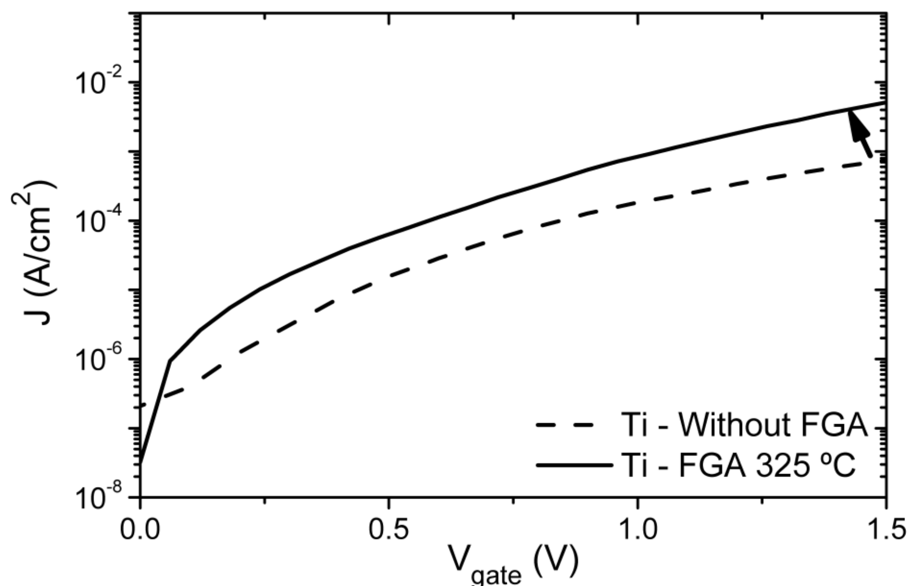

Figure VIII.10: Leakage current density as a function of V_{gate} for the Ti sample with GdO_x measured before and after the FGA at 325 ºC

The main conclusion of this section is the compatibility of the scavenging effect produced by Ti metal layer on InP MIS devices using Gd_2O_3. The CET achieves a value of 2.0 nm, therefore, a very low EOT value of 1.3 nm. Reasonable electrical characteristics were obtained for these capacitors. Moreover, a surface passivation treatment is required aiming with the reduction of the high D_{it} value obtained for these samples.

VIII.3.- SUMMARY AND CONCLUSIONS

In this chapter, the compatibility of the HPS two-step deposition process with high electron mobility substrates is demonstrated. This was achieved by depositing Gd_2O_3 on InP. A full accumulation-depletion-inversion sweep in the C-V_{gate} curves is achieved, meaning an unpinned Fermi level. A reaction observed between the high κ dielectric and the metallic Al contact produced an aluminate formation that increased the total CET of the stack. For that reason, samples with pure Pt gate electrodes were fabricated. For these MIS devices, the CET reached a value of 2.6 nm. Besides, the scavenging effect was also demonstrated for these capacitors. The CET obtained was reduced to 2.0 nm of CET with reasonable electrical characteristics.

Finally, a passivation treatment is required in order to reduce the high D_{it} obtained for these InP devices.

REFERENCES

[1] J. A. del Alamo. "*Nanometre-scale electronics with III-V compound semiconductors*". Nature, 479, 317 (2011).

[2] G. He, L. Zhu, Z. Sun. Q. Wan, L. Zhang. "*Integrations and challenges of novel high-k gate stacks in advanced CMOS technology*". Prog. Mater. Sci., 56, 475 (2011).

[3] I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao. D. Garcia, P. Majhi, N. Goel, W. Tsai. "*Self-aligned n-channel metal-oxide-semiconductor field effect transistor on high indium-content $In_{0.53}Ga_{0.47}As$ and InP using physical vapor deposition HfO_2 and silicon interface passivation layer*". Appl. Phys. Lett., 92, 202903 (2008).

[4] H. S. Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, J. C. Lee, P. Majhi. "*HfO_2-based InP n-channel metal-oxide-semiconductor field-effect transistors and metal-oxide-semiconductor capacitors using a germanium interfacial passivation layer*". Appl. Phys. Lett., 93, 102906 (2008).

[5] M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, A. M. Sergent. "*Epitaxial cubic gadolinium oxide as a dielectric for gallium arsenide passivation*". Science, 283, 1897 (1999).

[6] M. Hong, J. Kwo, S. N. G. Chu, J. P. Mannaerts, A. R. Kortan, H. M. Ng, A. Y. Cho, K. A. Anselm, C. M. Lee, J. I Chyi. "*Single-crystal GaN/Gd_2O_3/GaN heterostructure*". J. Vac. Sci. Technol. B, 20, 1274 (2002).

[7] W. H. Chang, C. H. Lee, P. Chang, Y. C. Chang, Y. J. Lee, J. Kwo, C. C. Tsai, J. M. Hong, C. H. Hsu, M. Hong "*High κ dielectric single-crystal monoclinic Gd_2O_3 on GaN with excellent thermal, structural, and electrical properties*". J. Crystal Growth, 311, 2183 (2009).

[8] W. H. Chan, C. H. Lee, Y. C. Chang, P. Chang, M. L. Huang, Y. J. Lee, C. H. Hsu, J. M. Hong, C. C. Tsai, J. R. Kwo, M. Hong. "*Nanometer-thick single-crystal hexagonal Gd_2O_3 on GaN for advanced complementary metal-oxide-semiconductor technology*". Adv. Mater., 21, 4970 (2009).

[9] T. Das, C. Mahata, C. K. Maiti, G. K. Dalapati, C. K. Chia, D. Z. Chi, S. Y. Chiam, H. L. Seng, C. C. Tan, H. K. Hui, G. Sutradhar, P. K. Bose. "*Sputter-deposited La_2O_3 on p-GaAs for gate dielectric applications*". J. Electrochem. Soc., 159, G15 (2012).

[10] E. Redondo. "*Realización de transistores MISFET sobre semiconductores compuestos del grupo III-V*". Ph. D. dissertation, Universidad Complutense de Madrid, Madrid (2001).

[11] S. Monaghan, E. O'Connor, B. J. Sheenan, K. Cherkaoui, F. Ferdousi, R. Ríos, A. Rahman, K. Kuhn, P. K. Hurley. "*AC level effect on interface state density extractions in high-k/III-V MOSCAPs*". 17th Workshop on Dielectrics in Microelectronics (Wodim), Dresden, Germany (2012).

[12] Y. Q. Wu, Y. Xuan, T. Shen, P. D. Ye, Z. Cheng, A. Lochtefeld. "*Enhancement-mode InP n-channel metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al_2O_3 dielectrics*". Appl. Phys. Lett., 91, 022108 (2007).

[13] E. H. Nicollian, A. Goetzberger. "*The Si-SiO_2 Interface – Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique*". Bell Syst. Tech. J., 46, 1055 (1967).

[14] R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, E. M. Vogel. "*Effect of post deposition anneal on the characteristics of HfO_2/InP metal-oxide-semiconductor capacitors*". Appl. Phys. Lett., 99, 172901 (2011).

[15] R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, E. M. Vogel. "*Electrical and chemical characteristics of Al_2O_3/InP metal-oxide-semiconductor capacitors*". Appl. Phys. Lett., 102, 132903 (2013).

[16] J. A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X. P. Wang, C. Adelmann, M. A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve, M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V. V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J. W. Maes, D. Manger, W. Vandervost, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M. Jurczak, J. Van Houdt, D. J. Wouters. "*High-k dielectrics for future generation memory devices*". Microelectron. Eng., 86¸ 1789 (2009).

[17] J. Kwo, M. Hong, A. R. Kortan, K. L. Queeney, Y. J. Chabal, R. L. Opila Jr., D. A. Muller, S. N. G. Chu, B. J. Sapjeta, T. S. Lay, J. P. Mannaerts, T. Boone, H. W. Krautter, J. J. Krajewski, A. M. Sergnt, J. M. Rosamilia. "*Properties of high k gate dielectrics Gd_2O_3 and Y_2O_3 for Si*". J. Appl. Phys., 89, 3929 (2001).

[18] Y. S. Kang, C. Y. Kim, M. H. Cho, K. B. Chung, C. H. An, H. Kim, H. J. Lee, C. S. Kim, T. G. Lee. "*Thickness dependence on crystalline structure and interfacial reactions in HfO_2 films on InP (001) grown by atomic layer deposition*". Appl. Phys. Lett., 97, 172108 (2010).

[19] C. H. An, Y. C. Byun, M. S. Lee, H. Kim. "*Impact of substrate temperature and film thickness on the interfacial evolution during atomic layer deposition of HfO_2 on InP*". Phys. Status, Solidi RRL, 6, 211 (2012).

[20] H. Dong, W. Cabrera, R. V. Galatage, Santosh KC, B. Brennan, W. Qin, S. McDonnell, D. Zhernokletov, C. L. Hinkle, K. Cho, Y. J. Chabal, R. M. Wallace. "*Indium diffusion through high-k dielectrics in high-k/InP stacks*". Appl. Phys. Lett., 103, 061601 (2013).

[21] G. D. Wilk, R. M. Wallace, J. M. Anthony. "*High-κ gate dielectrics: Current status and materials properties considerations*". J. Appl. Phys., 89, 5243 (2001).

[22] C. H. An, Y. C. Byun, M. S. Lee, H. Kim. "*Therma stabilities of ALD-HfO_2 films on HF-and $(NH_4)_2S$-cleaned InP*". J. Electrochem. Soc., 158, G242 (2011).

[23] H. C. Lin, G. Brammertz, K. Martens, G. de Valicourt, L. Negre, W. E. Wang, W. Tsai, M. Meuris, M. Heyns. "*The Fermi-level efficiency method and its applications on high interface trap density oxide-semiconductor interfaces*". Appl. Phys. Lett., 94, 153508 (2009).

[24] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, G. Groeseneken. "*On the correct extraction of interface trap density of MOS devices with highmobility semiconductor substrates*". IEEE Trans. Electron Devices, 55, 547 (2008).

[25] R. E. Herbert, Y. Hwang, S. Stemmer. "*Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces*". J. Appl. Phys., 108, 124101 (2010).

[26] E. San Andrés, L. Pantisano, J. Ramos, Ph. J. Roussel, B. J. O'Sullivan, M. Toledano Luque, S. DeGendt, G. Groeseneken. "*Accurate gate impedance determination on ultraleaky MOSFETs by fitting to a three-lumped-parameter model at frequencies from DC to RF*". IEEE Trans. Electron. Devices, 54, 1705 (2007).

[27] E. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, P. K. Hurley. "*Temperature and frequency dependent electrical characterization of $HfO_2/In_xGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods*" Appl. Phys. Lett., 94, 102902 (2009).

[28] S. Alexandrova, A. Szekeres, E. Halova. "*Variable frequency C-V analysis for observation of oxide charge in MOS structures with LPCVD-silicon oxynitride film*". Comptes Rendus de l'Academie Bulgare des Sciences, 57, 15 (2004).

[29] E. Halova, S. Alexandrova, A. Szekeres, M. Modreanu. "*LPCVD-silicon oxynitride films: interface properties*". Microlectron. Reliab., 45, 982 (2005).

[30] T. Tabata, C. H. Lee, K. Kita, A. Toriumi. "*Direct $LaLuO_3$/Ge gate stack formation by interface layer scavenging and subsequent low temperature O_2 annealing*". ECS Trans., 33, 375 (2010).

[31] S. Fadida, P. Shekhter, D. Cvetko, L. Floreano, A. Verdini, L. Nyns, S. Van Elshocht, I. Kymissis, M. Eizenberg. "*Direct observation of both contact and remote oxygen scavenging of GeO_2 in a metal-oxide-semiconductor stack*". J. Appl. Phys., 116, 164101 (2014).

[32] M. A. Pampillón, P. C. Feijoo, E. San Andrés, H. García, H. Castán, S. Dueñas. "*Scavenging effect on plasma oxidized Gd2O3 grown by high pressure sputtering on Si and InP substrates*". Semicond. Sci. Technol., 30, 035023 (2015).

[33] E. Redondo, I. Mártil, G. González-Díaz, H. Castán, S. Dueñas. "*Influence of electron cyclotron resonance nitrogen plasma exposure on the electrical characteristics of SiNx:H/InP structures*". J. Vac. Sci. Technol. B, 19, 186 (2001).

[34] H. Dong, W. Cabrera, X. Qin, B. Brennan, D. Zhernokletov, C. L. Hinkle, J. Kim, Y. J. Chabal, R. M. Wallace. "*Silicon interfacial passivation layer chemistry for high-k/InP interfaces*". ACS Appl. Mater. Interfaces, 6, 7340 (2014).

[35] B. Brennan, M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, G. Hughes, R. M. Wallace. "*Optimisation of the ammonium sulphide $(NH_4)_2S$ passivation process on $In_{0.53}Ga_{0.47}As$*". Appl. Surf. Sci., 257, 4082 (2011).

[36] J. J. Gu, A. T. Neal, P. D. Ye. "*Effects of $(NH_4)_2S$ passivation on the off-state performance of 3-dimensional InGaAs metal-oxide-semiconductor field-effect transistors*". Appl. Phys. Lett., 99, 152113 (2011).

[37] Y. C. Byun, C. H. An, J. Y. Choi, C. Y. Kim, M. H. Cho, H. Kim. "*Interfacial self-cleaning during PEALD HfO_2 process on GaAs using TDMAH/O_2 with different $(NH_4)_2S$ cleaning time*". J. Electrochem. Soc., 158, G141 (2011).

[38] M. K. Lee, C. F. Yen, C. H. Cheng, J. C. Lee. "*Characterization of SiON/InP MOS structure with sulfidation, fluorination and hydrogenation*". Appl. Phys. A, 112, 1057 (2013).

Chapter IX:
Conclusions and future work

During this thesis, MIS devices grown with Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ as high κ materials were fabricated on Si wafers. Besides, Gd_2O_3 was deposited on InP substrates. The novelty of this work consists on the dielectric deposition process. A two-step procedure was developed: first, metallic thin films of Gd, Sc and a nanolaminate of them were deposited by means of high pressure sputtering, a non-conventional technique, in an Ar atmosphere from metallic targets. Afterwards and without breaking the vacuum, an *in situ* plasma oxidation was carried out in a mixed Ar/O_2 ambient. Both processes were performed at room temperature and at a pressure of 0.50 mbar. The high working pressure of this system, compared to the conventional sputtering, reduces the damage of the semiconductor surface.

Additionally, the scavenging effect produced by Ti electrodes was explored for the three analyzed high κ materials on Si. This permits a further EOT reduction and, therefore, the CMOS technology downscaling.

Besides, for MIS capacitors with Gd_2O_3 on InP, the scavenging effect has been also demonstrated.

In this chapter, the main conclusions obtained during this work will be addressed. Finally, the future work in this field that will be carried out by the *Thin Films and Microelectronic Group* will be stated.

IX.1.- CONCLUSIONS

The key conclusions of this present work are summarized as follow:

a) The thermal oxidation performed at different temperatures (from 250 to 750 ºC) after the metallic Gd layer deposited on Si using HPS did not meet the requirements for high κ materials. In spite of producing dielectric films with very low D_{it} and acceptable leakage current density, the permittivity value obtained was too low (~7.4). This was produced by the reaction of Gd and Si at the first stages of the oxidation process. After the oxidation, some bumps appeared at the dielectric/semiconductor interface that affected the effective κ value of these MIS devices.

b) The plasma oxidation of Gd_2O_3 and Sc_2O_3 was explored for the fabrication of MIS capacitors with these high κ materials from metallic targets by means of HPS. The two-step procedure produced amorphous and stoichiometric films.

After a complete study of several deposition conditions for Gd_2O_3, it was found that 20 W of *rf* power during the oxidation step performed a less aggressive oxidation with a lower regrowth of interfacial SiO_x. Additionally, the oxidation duration was a key parameter in order to achieve a complete oxidation of the metallic layer without an excessive SiO_x grown at the interface. A shorter oxidation time provided low leakage current density, acceptable D_{it}, small hysteresis and almost no frequency dispersion for an EOT of 2.2 nm. The effective κ value of the dielectric stack was around 11, due to the formation of an interfacial $GdSiO_x$ layer after annealing in forming gas.

For the Sc_2O_3 case, MIS devices with an EOT of 1.6 nm were obtained. These capacitors showed a moderate D_{it} and reasonable current density. The κ value was ~9, again related to an interfacial scandium silicate formation.

c) The fabrication of $Gd_{0.9}Sc_{1.1}O_3$ films from metallic Gd and Sc targets was achieved by depositing a nanolaminate of thin Gd and Sc layers, followed by a plasma oxidation and after a temperature treatment in a forming gas atmosphere. Amorphous and homogeneous layers were obtained after a FGA at 600 ºC. MIS capacitors using this dielectric and Pt as top electrode were fabricated for this slightly Sc-rich gadolinium scandate. From a leakage current density and hysteresis point of view, a FGA at 500 ºC is the best compromise, since increasing the temperature up to 600 ºC reduced the EOT at the expense of an increase of interface trap density. A high permittivity value around 32 was achieved, which is a promising value for CMOS applications.

d) The scavenging effect has been proved in MIS devices with Gd_2O_3, Sc_2O_3 and $Gd_{0.9}Sc_{1.1}O_3$ gates, using Ti in the metallic electrode as scavenging layer. A suitable choice of the Ti thickness and the FGA temperature is critical to obtain a controlled scavenging effect. This means a reduction in the total EOT of the devices but without compromising the electrical behavior of these capacitors (which implies a degradation of the dielectric film, with a reduced thickness, a poor interface quality with a high D_{it} and higher leakage current density).

For Gd_2O_3, it was demonstrated that the best compromise between scavenging, D_{it} and leakage current density was achieved with an electrode of 5 nm of Ti capped with Pt after a FGA at 300 ºC.

For the $Gd_{0.9}Sc_{1.1}O_3$ devices, a decrease in the EOT of 0.3 nm was achieved with the Ti gates, reaching a minimum of 1.2 nm. However, a high D_{it} was obtained for these devices, indicating that a post-scavenging process would be needed to improve the interface.

e) MIS capacitors fabricated on InP semiconductors as substrate and using Gd_2O_3 as high κ material showed a well behaved C-V_{gate} characteristics with a full accumulation-depletion-inversion sweep, meaning an unpinned Fermi level. This was achieved even before the FGA and without a passivation surface treatment before the dielectric deposition. As opposed

to the Si case, interfacial oxides were not found between the high κ material and the InP. Thus, low CET values were obtained for this semiconductor.

The initial metallic Gd thickness and the oxidation time were key parameters in order to obtain MIS devices with low leakage currents. In addition, the top electrode choice was important to obtain capacitors that presented low CET values. In fact, we have also proved the scavenging effect using Ti gates with this semiconductor. The lowest CET achieved was 2.0 nm with reasonable leakage and C-V_{gate} curves.

However, a severe flatband voltage shift with the measured frequency was observed for all these capacitors. This was related to an extremely high D_{it}. This indicates that a surface preparation process prior deposition is mandatory.

IX.2.- FUTURE WORK

The promising results obtained during this present work will be continued in the following years. The main challenge is to obtain subnanometer EOTs. Therefore, the optimization of the scavenging effect for $GdScO_3$ films is required. Besides reducing the EOT, it is necessary to control this effect in order to achieve a good interface with low D_{it} and low leakage current density values.

Additionally, in order to take the advantage of the higher electron mobility of the InP material (and, in extension, of any III-V semiconductor), a study of the compatibility of possible passivation treatments of the surface with the two-step deposition process is required.

Finally, the deposition of $GdScO_3$ layers by HPS on III-V semiconductors is a promising research route that, in the long run, could help to keep up with the continuous MOSFET downscaling.

LIST OF PUBLICATIONS

Journal papers

1. M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. Toledano-Luque, A. del Prado, A. J. Blázquez, M. L. Lucía. "*Towards metal electrode interface scavenging of rare-earth scandates: A Sc_2O_3 and Gd_2O_3 study*". Microelectron. Eng., 88, 1357 (2011).
2. M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. L. Lucía, A. del Prado, M. Toledano-Luque. "*Anomalous thermal oxidation of gadolinium thin films deposited on silicon by high pressure sputtering*". Microelectron. Eng., 88, 2991 (2011).
3. P. C. Feijoo, M. A. Pampillón, E. San Andrés, M. L. Lucía. "*Optimization of scandium oxide growth by high pressure sputtering on silicon*". Thin Solid Films, 526, 81 (2012).
4. P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Optimization of gadolinium oxide growth deposited on Si by high pressure*". J. Vac. Sci. Technol. B, 31, 01A103 (2013).
5. A. Gómez. H. Castán, H. García, S. Dueñas, L. Bailón, M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Interface quality of Sc_2O_3 and Gd_2O_3 films based metal-insulator-silicon structures using Al, Pt and Ti gates: Effect of buffer layers and scavenging electrodes*". J. Vac. Sci. Technol. B, 31, 01A106 (2013).
6. M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. L. Lucía. "*Optimization of in situ plasma oxidation of metallic gadolinium thin films deposited by high pressure sputtering on silicon*". J. Vac. Sci. Technol. B, 31, 01A112 (2013).
7. M. A. Pampillón, C. Cañadilla, P. C. Feijoo, E. San Andrés, A. del Prado. "*High pressure sputtering as a viable technique for future high permittivity on III-V integration: GdO_x on InP demonstration*". J. Vac. Sci. Technol. B, 31, 01A115 (2013).

8. E. San Andrés, M. A. Pampillón, P. C. Feijoo, R. Pérez, C. Cañadilla. "*High permittivity gadolinium oxide deposited on indium phosphide by high-pressure sputtering without interface treatments*". Microelectron. Eng., 109, 223 (2013).

9. M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Electrical characterization of gadolinium oxide deposited by high pressure sputtering with in situ plasma oxidation*". Microelectron. Eng., 109, 236 (2013).

10. P. C. Feijoo, M. A. Pampillón, E. San Andrés, J. L. G. Fierro. "*Gadolinium scandate by high pressure sputtering for future generations of high k dielectrics*". Semicond. Sci. Technol., 28, 085004 (2013).

11. E. San Andrés, P. C. Feijoo, M. A. Pampillón, M. L. Lucía, A. del Prado. "*High pressure sputtering for high-k dielectric deposition. Is it worth trying?*". ECS Trans., 61, 27 (2014).

12. S. Wirths, D. Stange, M. A. Pampillón, A. Tiedemann, G. Mussler, A. Fox, U. Breuer, B. Baert, E. San Andrés, N. Nguyen, J. M. Hartmann, Z. Ikonic, S. Mantl, D. Buca. "*High-k gate stacks on low bandgap tensile strained Ge and GeSn alloys for field effect transistors*". ACS Appl. Mater. Interfaces, 7, 62 (2015).

13. M. A. Pampillón, P. C. Feijoo, E. San Andrés, H. García, H. Castán, S. Dueñas. "*Scavenging effect on plasma oxidized* Gd_2O_3 *grown by high pressure sputtering on Si and InP substrates*". Semicond. Sci. Technol., 30, 035023 (2015).

14. P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Nano-laminate vs direct deposition on silicon of high permittivity gadolinium scandate by high pressure sputtering*". Thin Solid Films, 593, 62 (2015).

15. Z. Gao, M. F. Romero, M. A. Pampillón, E. San Andrés, F. Calle. "*Thermal assessment of AlGaN/GaN MOS-HEMTs on Si substrate using* Gd_2O_3 *as gate dielectric*". IEEE Trans. Electron Dev. (accepted for publication).

Conference contributions

1. E. San Andrés, M. A. Pampillón, M. L. Lucía, P. Feijoo, A. del Prado, M. Toledano-Luque "*Growth of gadolinium oxide by thermal oxidation of thin metallic gadolinium layers*". 11th International Conference on Ultimate Integration on Silicon (ULIS). Glasgow, Scotland. March 2010. Poster.
2. M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. Toledano-Luque, A. del Prado, A. J. Blázquez, M. L. Lucía. "*Interface engineering by metal electrode scavenging of Gd_2O_3 films sputtered on Si*". 8th Spanish Conference on Electron Devices (CDE). Mallorca, Spain. February 2011. Poster.
3. M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. Toledano-Luque, A. del Prado, A. J. Blázquez, M. L. Lucía. "*Towards metal electrode interface scavenging of rare-earth scandates: a Sc_2O_3 and Gd_2O_3 study*". 17th Conference on Insulating Films on Semiconductors (INFOS). Grenoble, France. June 2011. Poster.
4. M. A. Pampillón, C. Cañadilla, P. C. Feijoo, E. San Andrés, A. del Prado. "*High pressure sputtering as a viable technique for future high k on III-V integration: Gd_2O_3 on InP demonstration*". 17th Workshop on Dielectrics in Microelectronics (WoDiM). Dresde, Germany. June 2012. Poster.
5. M. A. Pampillón, P. C. Feijoo, E. San Andrés, M. L. Lucía. "*Optimization of in situ plasma oxidation of Gd metallic thin films deposited by high pressure sputtering on Si*". 17th Workshop on Dielectrics in Microelectronics (WoDiM). Dresde, Germany. June 2012. Poster.
6. P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Optimization of gadolinium oxide growth deposited by high pressure sputtering through scavenging techniques*". 17th Workshop on Dielectrics in Microelectronics (WoDiM). Dresde, Germany. June 2012. Poster.
7. A. Gómez. H. Castán, H. García, S. Dueñas, L. Bailón, M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Interface quality of Sc_2O_3 and Gd_2O_3 films based MIS structures using Al, Pt and Ti gate: effect of buffer layer and scavenging electrodes*". 17th Workshop on Dielectrics in Microelectronics (WoDiM). Dresde, Germany. June 2012. Poster.

8. M. A. Pampillón, P. C. Feijoo, E. San Andrés, J. L. G. Fierro. "*Plasma oxidation of metallic Gd deposited on silicon by high pressure sputtering as high permittivity dielectric*". 9th Spanish Conference on Electron Devices (CDE). Valladolid, Spain. February 2013. Oral.

9. P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Gadolinium scandate by high pressure sputtering as a high-k dielectric*". 9th Spanish Conference on Electron Devices (CDE). Valladolid, Spain. February 2013. Poster.

10. E. San Andrés, M. A. Pampillón, C. Cañadilla, P. C. Feijoo, A. del Prado. "*Towards high-k integration with III-V channels: interface optimization of high pressure sputtered Gd_2O_3 on InP*". 9th Spanish Conference on Electron Devices (CDE). Valladolid, Spain. February 2013. Poster.

11. H. García. H. Castán, S. Dueñas, L. Bailón, P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Electrical study of ScO_x-based MIS structures using Al and Ti as gate electrodes*". 9th Spanish Conference on Electron Devices (CDE). Valladolid, Spain. February 2013. Poster.

12. M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Electrical characterization of gadolinium oxide deposited by high pressure sputtering with in situ plasma oxidation*". 18th Conference on Insulating Films on Semiconductors (INFOS). Cracow, Poland. June 2013. Poster.

13. E. San Andrés, M. A. Pampillón, P. C. Feijoo, R. Pérez, C. Cañadilla. "*High permittivity gadolinium oxide deposited on indium phosphide by high-pressure sputtering without interface treatments*". 18th Conference on Insulating Films on Semiconductors (INFOS). Cracow, Poland. June 2013. Poster.

14. Z. Gao, M. F. Romero, M. A. Pampillón, E. San Andrés, S. Martín-Horcajo, T. Brazzini, F. Calle. "*Gd_2O_3 gate dielectric for AlGaN/GaN high electron mobility transistors (HEMTs)*". 22nd European Workshop on Heterostructure Technology (HETECH). Glasgow, Scotland. September 2013. Oral.

15. E. San Andrés, P. C. Feijoo, M. A. Pampillón, M. L. Lucía, A. del Prado. "*High pressure sputtering for high-k dielectric deposition. Is it worth trying?*" 225th Electrochemical Society Meeting (ECS). Orlando, United States. May 2014. Invited talk.
16. S. Wirths, M. A. Pampillón, E. San Andrés, D. Stange, A. T. Tiedemann, G. Mussler, A. Fox, U. Breuer, J. M. Hartmann, S. Mantl, D. Buca. "*Growth and interface engineering of highly strained low bandgap group IV semiconductors*". 7th International Silicon-Germanium Technology and Device Meeting (ISTDM). Singapore, Singapore. June 2014. Oral.
17. M. A. Pampillón, P. C. Feijoo, E. San Andrés. "*Scavenging effect on plasma oxidized Gd_2O_3 grown by high pressure sputtering on Si and InP substrates*". 18th Workshop on Dielectrics in Microelectronics (WoDiM). Kinsale, Ireland. June 2014. Poster.
18. P. C. Feijoo, M. A. Pampillón, E. San Andrés. "*Nano-laminate vs direct deposition on silicon of high permittivity gadolinium scandate by high pressure sputtering*". 18th Workshop on Dielectrics in Microelectronics (WoDiM). Kinsale, Ireland. June 2014. Poster.
19. Z. Gao, M. F. Romero, M. A. Pampillón, E. San Andrés, F. Calle. "*Temperature performance of AlGaN/GaN MOS-HEMTs using Gd_2O_3 as gate dielectric fabricated on Si substrate*". 23rd European Workshop on Heterostructure Technology (HETECH). Giessen, Germany. October 2014. Oral.
20. Z. Gao, M. F. Romero, M. A. Pampillón, E. San Andrés, F. Calle. "*Thermal stability study of AlGaN/GaN MOS-HEMTs using Gd_2O_3 as gate dielectric fabricated on Si*". 10th Spanish Conference on Electron Devices (CDE). Aranjuez, Spain. February 2015. Oral.
21. Z. Gao, M. F. Romero, A. Redondo-Cubero, M. A. Pampillón, E. San Andrés, F. Calle. "*Effects of proton irradiation on AlGaN/GaN based high electron mobility transistors*". 40th Workshop on Compound Semiconductor Devices and Integrated Circuits & 13th Expert Evaluation and Control of Compound Semiconductor Materials and Technologies (WOCSDICE-EXMATEC). Aveiro, Portugal. June 2016. Oral

Patent

1. M. A. Pampillón, C. Cañadilla, P. C. Feijoo, E. San Andrés, Á. del Prado, M. L. Lucía. (Universidad Complutense de Madrid). "*Método de fabricación de estructuras de puerta de transistores MOSFET sobre semiconductores III-V*". Spanish Patent 2435866 A1 (2013).