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Power-Hardware Design and Topologies of Converter-Based Grid Emulators for Wind Turbines

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***Abstract*—Power-electronic-based grid emulators (GEs) emerge as a favorable method for testing grid-code compliances of wind turbines (WTs), thanks to their full controllability and improved efficiency. To accommodate the increasing power and voltage levels of WTs, scalability becomes a critical requirement for the topologies of converter-based GEs. This paper identifies first the power rating of future GEs based on the system architecture and the evolution of WTs, followed by evaluating converter topologies of GEs for high scalability. Design considerations of power semiconductor devices, step-up transformers, dc chopper and dc capacitors are also discussed for existing and prospective GEs.**

***Index Terms*— Grid emulators, grid-code compliance, testing, converter topologies, power hardware**

I. Introduction

WIND turbines (WTs) are undergoing a continuous increase in power rating, from a few megawatts (MW) to 16 MW today [1]. For efficient power transmission, the voltage level of the collector system in wind power plants has also risen to 66 kV and may even reach 132 kV in the future [2], [3]. Driven by the rising power and voltage levels of WTs, a highly scalable grid emulator (GE) is demanded for testing grid-code compliances of WTs [2].

Generally, a power-electronic-based GE employs a back-to-back (BTB) power conversion structure, which consists of an active-front-end (AFE) converter and a controlled voltage generator (CVG) [2], [4]. The AFE converter and CVG are configured with multiple parallel/series-connected power converters for scalability. A common choice is to interleave multi-paralleled neutral point clamped (NPC) converters with a multi-winding transformer [5], [6], [7], where the power rating of GE is increased with the number of NPC converters. Another option is to use the single-phase transformers with a custom-built configuration [8], [9], [10], instead of the multi-winding transformer, leading to a cascaded NPC-based GE. The scalability of the NPC-based GEs is limited by the power efficiency and manufacturing process of transformers [11].

Alternatively, multilevel converters such as the cascaded H-bridge (CHB) converter [12], [13], [14], [15], [16] and the modular multilevel converter (MMC) [17], [18], [19], [20], [21] are also used with GEs, where a standard three-phase step-up transformer is adopted to further scale up the output voltage of CVG [12], [13], [17]. The CHB-based CVG does not have a common dc link, and instead, the H-bridge converters are individually fed by three-phase AFE converters, which are then typically connected to the power grid through multi-winding transformers [15]. However, the number of secondary windings of multi-winding transformers limit the scalability of the H-bridge cells. The BTB-MMC-based GE, on the other hand, can employ dozens of floating submodules (SMs) per arm to increase the output voltage and reduce total harmonic distortion (THD) without adding ac filters [20], [22].

The selection of power semiconductor devices and design of passive power components in these GEs exhibit unique challenges with fulfilling the testing capability requirements. During fault ride-through (FRT) tests, the GE must be able to handle fault currents, i.e., 2 p.u. fault current for type-IV WTs and 7 p.u. fault current for type-III WTs [23], [24], which necessitates oversized current ratings for power semiconductor devices. In particular, interleaved NPC- and MMC-based GEs have circulating current flows [7], [19], due to the interleaved modulation and the lack of separated dc power supply of NPC and SMs, which complicates the oversized design of power semiconductor devices. Additional transformer taps and anti-saturation design of the CVG-side transformer are necessary for a GE to reproduce voltage sags and swells within 1 ms at a range of 0~160% of the rated voltage [25], [26]. This may further exacerbate the complexities of manufacturing multi-winding and custom-built single-phase transformers. The design of neutral-point (NP)/cell/SM capacitance and dc chopper is also important to avoid the over- and under-voltage of dc-link capacitors when emulating multiple consecutive grid faults [27].

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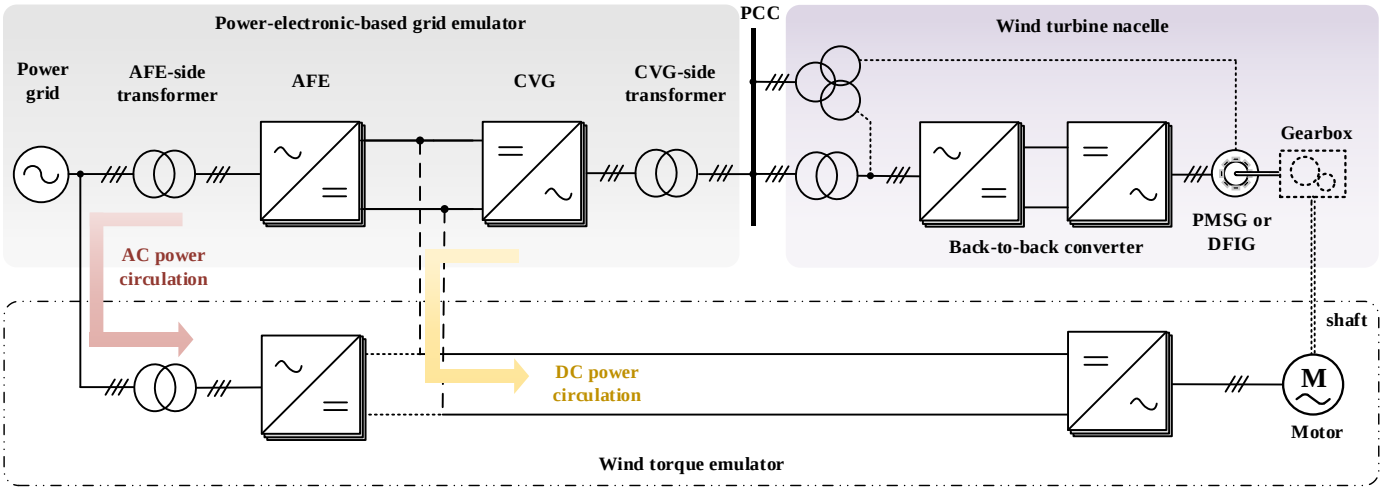


Fig. 1. Overall system diagram of power-electronic-based grid-code compliance testing system for WTs [2], [21].

This paper, thus, gives a review on topologies and hardware design aspects of power components for converter-based GEs. It begins by identifying the power rating requirements for future GEs according to the architecture of grid emulation system and the evolution of WTs. Then, the GEs based on the interleaved NPC, the cascaded NPC, the CHB and the MMC are systematically compared. The design considerations of power components to meet the testing capability requirements of GEs are discussed. Lastly, insights on the hardware design aspects of prospective GEs driven by emerging trends are shared.

II. System Architecture and Power Rating

Fig. 1 depicts the overall architecture of power-electronic-based testing system for WTs [2], [21]. Besides the GE, the testing system comprises a WT nacelle and a wind torque emulator, which together simulate the electrical and mechanical behavior of the WT system. The WT nacelle is equipped with a BTB converter and a generator with/without a gearbox, while the wind torque emulator consists of a motor-drive system and a shaft to reproduce the behavior of a WT rotor. This section elaborates first the short-circuit current capability and power levels of WTs, then outlines the power rating of future GEs and the system architecture.

A. Short-Circuit Current and Power Levels of WTs

Two types of generators are commonly used for WTs, i.e., the permanent magnet synchronous generator (PMSG) and the doubly-fed induction generator (DFIG) [28], [29]. The PMSG-based WTs typically have a maximum short-circuit current capacity of 2 p.u., while the DFIG-based WTs can handle an overcurrent up to 7 p.u. [23], [24], [30].

Fig. 2 depicts the power levels of typically installed and planned WTs [1], [31], [32], [33], [34]. Currently, the maximum power rating of DFIG-based WTs is 7 MW, while the PMSG-based WTs with a power capacity up to 16 MW have been deployed in offshore wind power plants. The development of a 20 MW WT is also expected in the near future [28], [29].

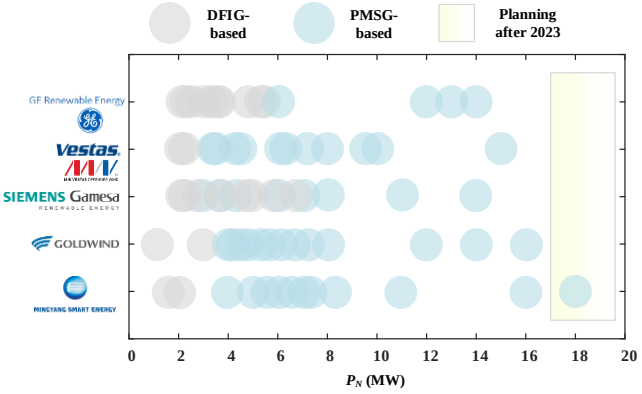


Fig. 2. Power levels of deployed and planning WTs.

B. Power Rating of Future GEs

IEEE 1547-2018 specifies that WTs should be capable of injecting reactive power up to 44% of their nameplate apparent power rating S_{rated} [35], even when the steady-state active power output is at the rated level. For a WT with a rated active power of P_{rated}, the S_{rated} must satisfy

$$S_{rated} \geq \frac{P_{rated}}{\sqrt{1-0.44^2}} \quad (1)$$

Thus, S_{rated} should be not less than 22.3 MVA for a WT with P_{rated}=20 MW. A GE should have a continuous power rating of at least 20 MW/22.3 MVA to accommodate the increasing power level of WTs in normal operation [19], [36]. However, during FRT tests, the CVG must cover a broad range of under- and over-voltage, i.e., 0-160% of rated voltage [26]. The transient fault current at the point of common coupling (PCC) depends on the current reference and control of a WT specified by WT manufacturers, in addition to the intermediate impedance between WT and GE. Consequently, the worst scenario assumes that the WT delivers the maximum current to ride through the 160% of rated voltage [37], [38]. Subsequently, the maximum power responses of PMSG- and DFIG-based WTs can be simplify derived as

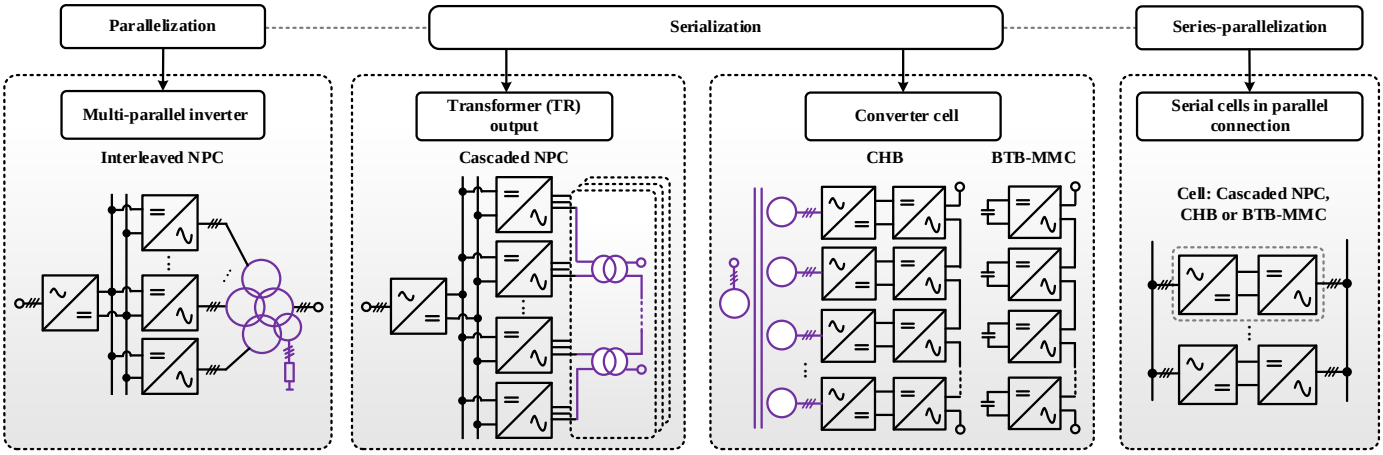


Fig. 3. Topologies of typical medium-voltage megawatt GEs.

$$\begin{cases} S_{\max\_PMSG} = 20 \times 2 \times 1.6 \text{ MVA} = 64 \text{ MVA} \\ S_{\max\_DFIG} = 7 \times 7 \times 1.6 \text{ MVA} = 78.4 \text{ MVA} \end{cases} \quad (2)$$

Hence, taking the power loss into account, the short-term power capacity of a future GE should be at least 80 MVA [39].

C. Wind Torque Emulator and Power Circulation

To reproduce the low-speed dynamics of WTs, the motor-drive system should be able to generate the active power at least 20 MW at an output frequency of 2~10 Hz [6].

For energy-saving purpose, the wind torque emulator can be configured in two ways to cycle active power, i.e., dc power circulation and ac power circulation, as depicted in Fig. 1. The dc power circulation is attained through a shared dc link between the motor-drive system and the CVG of GE [40]. However, for GEs without a common dc link, the ac power circulation may be used instead [12], which requires an additional AFE converter and transformer to power the motor-drive system, potentially increasing the system volume and footprint. It is worth noting that the converters used within the turbine torque emulator follow the same topologies as that of GE for the scalability requirement [2], [6].

III. Topologies of Power-Electronic-Based GEs

Fig. 3 illustrates the categorization of topologies of power-electronic-based GEs into three types: parallel, serial, and series-parallel. The evaluation criteria of these types of GEs are discussed, which are the multilevel output, the placement of ac filter, the complexities of manufacturing transformers, the scalability and the voltage/current stress of power semiconductor devices to compare four types of GEs, see Table I. The actual applications for each GE are also discussed.

A. Multilevel Output and THD of PCC Voltage

Generally, GEs should follow the testing requirements on the harmonic voltage limits at the PCC, i.e., the THD (from 2nd to 50th harmonics) of the line-to-neutral PCC voltage must be below 5% [41]. Currently, a more stringent requirement is posed by IEEE 1547.1-2020, i.e., the THD of PCC voltage (line-to-neutral) should be lower than 3% [42].

1) Interleaved NPC-Based GE: To enhance the power scalability with a reduced THD of the PCC voltage, using the

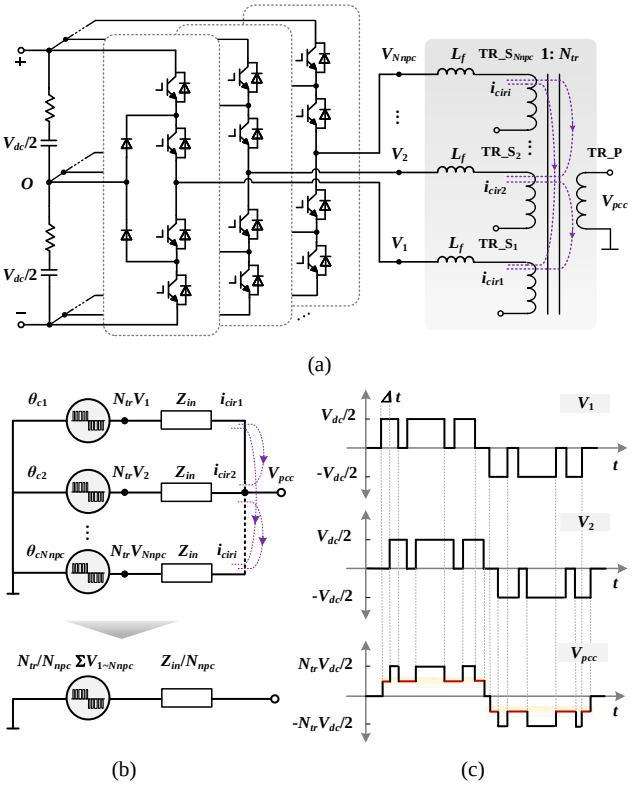


Fig. 4. Operating principle of interleaved NPC inverters. (a) A single-phase interleaved NPC inverter. (b) Single-phase equivalent circuit. (c) An example of single-phase PCC voltage generation of a GE using two NPC inverters.

interleaved NPC inverters based on the phase-shifted-carrier (PSC) pulse width modulation (PWM) is a common solution for the CVG in commercial GEs [5], [6], [7], [43].

Fig. 4(a) depicts a general single-phase CVG circuit of the interleaved NPC-based GE in Fig. 3, where V_{dc}, V_1~V_{Nnpc}, L_f represent the dc-link voltage, ac terminal voltages and L filter of these paralleled inverters, respectively. TR_S$_1$~TR_S$_{Nnpc}$, TR_P and N_{tr} denote the secondary windings, primary winding and step-up ratio of the multi-winding CVG-side transformer, respectively. V_{pcc} is the magnitude of line-to-neutral PCC voltage. Fig. 4(b) illustrates a single-phase equivalent Thevenin circuit of interleaved NPC inverters, where N_{npc} and θ_{c1}~θ_{cNnpc} are the number and phase angles of carrier signals

TABLE I
COMPARISON OF MEDIUM-VOLTAGE MEGAWATT GES

Typical GEs	Interleaved NPC	Cascaded NPC	CHB	BTB-MMC
Number of output line-to-neutral voltage levels	$2N_{npc}$+1	$2N_{npc}$+1 (N_{npc} is even)	$2N_H$+1	$2N_{HB}$+1 for HBSM-based $4N_{FB}$+1 for FBSM-based
CVG-side ac filter	Integrated with CVG-side TR (*RC* filter)	Connected to the PCC (*RC* filter)	Connected to ac terminal of CVG (*LC*/*RLC* filter) or filterless	Connected to ac terminal of CVG (*C*/*RC* filter) or filterless
AFE-side transformer (TR)	Standard or multi-winding	Standard or multi-winding	Single multi-winding or Several multi-winding	Standard
CVG-side TR	Multi-winding	Single-phase and custom-built	Standard	Standard
Scalability	Low	Moderate	Moderate	High
Number of semiconductor devices in the AFE	≥3×6	≥3×6	3×6N_H	6×2N_{HB} for HBSM-based 6×4N_{FB} for FBSM-based
Number of semiconductor devices in the CVG	3×6N_{npc}	3×6N_{npc}	3×4N_H	6×2N_{HB} for HBSM-based 6×4N_{FB} for FBSM-based
Voltage stress of semiconductor devices in the CVG	0.5V_{dc}	0.5V_{dc}	V_{cell}	V_{sm}
Current stress of semiconductor devices in the CVG	$I_{pcc}N_{tr}/N_{npc}$+ (1-1/N_{npc})$N_{tr}V_{dc}/(2Z_{in})$	$I_{pcc}N_{tr}$	$I_{pcc}N_{tr}$	I_{cir}+$I_{pcc}N_{tr}$/2
Advantages	▪ High technology readiness level of interleaved NPCs	▪ Low step-up ratio of custom-built TRs ▪ No circulating current between NPC inverters	▪ No circulating current between H-bridge cells ▪ Filterless is feasible	▪ Using standard transformers ▪ Filterless is feasible
Disadvantages	▪ Circulating current between NPCs related to Z_{in} ▪ Manufacturing complexity of multi-winding TRs	▪ Bulky volume of ac filter as the V_{pcc} increases ▪ Manufacturing complexity of custom-built TRs	▪ Manufacturing complexity of multi-winding TRs	▪ Fluctuations of SM capacitor voltage and circulating current ▪ Bulky SM capacitors and arm inductors

for these inverters. Z_{in} is the equivalent intermediate impedance between the inverter and PCC, which can be expressed as [7], [43]

$$Z_{in} = 2\pi f_1 L_f N_{tr}^2 + Z_{tr} \tag{3}$$

where Z_{tr} is the impedance of multi-winding transformer including the winding resistance and leakage reactance. f_1 is the fundamental frequency.

In Fig. 4(b), i_{cir} is the circulating current caused by the terminal voltage difference of paralleled inverters across the Z_{in} [7], [43]. According to Kirchhoff's Current Law (KCL), without the connected WTs, the sum of output current of each inverter should satisfy

$$\frac{N_{tr}V_1 - V_{pcc}}{Z_{in}} + \frac{N_{tr}V_2 - V_{pcc}}{Z_{in}} + \cdots + \frac{N_{tr}V_{Nnpc} - V_{pcc}}{Z_{in}} = 0 \tag{4}$$

Therefore, the PCC voltage and i_{ciri} (i=1,2,$\cdots N_{npc}$) flowing in each NPC inverter are given by

$$V_{pcc} = \frac{N_{tr}}{N_{npc}} \sum V_{1\sim N_{npc}} \tag{5}$$

$$i_{ciri} = \frac{N_{tr}V_i}{Z_{in}} - \frac{N_{tr}}{N_{npc}Z_{in}} \sum V_{1\sim N_{npc}} \tag{6}$$

TABLE II
OPERATING STATES OF A GE USING TWO INTERLEAVED NPC INVERTERS

Output voltage V_1	Output voltage V_2	Circulating current i_{cir}	PCC voltage V_{pcc}
V_{dc}/2	V_{dc}/2	0	$N_{tr}V_{dc}$/2
-V_{dc}/2	-V_{dc}/2	0	-$N_{tr}V_{dc}$/2
0	0	0	0
V_{dc}/2	0	$N_{tr}V_{dc}/(4Z_{in})$	$N_{tr}V_{dc}$/4
0	V_{dc}/2	$N_{tr}V_{dc}/(4Z_{in})$	$N_{tr}V_{dc}$/4
-V_{dc}/2	0	-$N_{tr}V_{dc}/(4Z_{in})$	-$N_{tr}V_{dc}$/4
0	-V_{dc}/2	-$N_{tr}V_{dc}/(4Z_{in})$	-$N_{tr}V_{dc}$/4

The interleaved NPC inverters can be modelled as a controlled voltage source with the rated voltage V_{pcc} in series with an impedance Z_{in}/N_{npc} [44]. When terminal voltages V_1 to V_{npc} are same, V_{pcc} still exhibits original three-level voltage and i_{cir} is zero. To achieve a multilevel output, it is necessary to regulate different θ_{c1}~θ_{cNnpc} at the same instant, thus making non-zero i_{cir} inevitable.

Fig. 4(c) and Table II show an example of PCC voltage generation and all operating states of a GE using two NPC

inverters [45]. As shown in highlighted area, shifting a time delay (Δt) between V_1 and V_2 can create additional number of output voltage levels. Therefore, the number of line-to-neutral voltage levels N_{ln} at the PCC can be expressed as [44]

$$N_{ln} = 2N_{npc} + 1 \tag{7}$$

According to (6), when only one $V_{dc}/2$ exists among V_1~V_{Nnpc} and the rest are zero, the i_{ciri} attains its maximum value, as follows

$$i_{cir\,max} = \frac{N_{tr}V_{dc}}{2Z_{in}}\left(1 - \frac{1}{N_{npc}}\right) \tag{8}$$

To achieve best harmonic voltage cancellation and minimize the THD at the PCC, the θ_{c1}~θ_{cNnpc} of carrier signals of interleaved NPC inverters are generally shifted by $2\pi/N_{npc}$ radians incrementally [43], [46]. However, the switching frequency, i.e., the carrier frequency, of a NPC inverter is typically lower than 1 kHz and N_{npc} is usually smaller than 4 in megawatt interleaved NPC based GEs [7], [40]. This often causes the THD of the line-to-neutral PCC voltage greater than 10% [43]. Although using more parallel NPC inverters is a simple solution in theory to reduce THD, it requires multiple secondary windings of the CVG-side transformer. Besides, according to (4), the parameter differences in L_f and secondary windings can change the voltage levels of V_{pcc}, which may further affect its THD.

2) Cascaded NPC-Based GE: Fig. 5 illustrates the operation principle of the cascaded NPC-based GE [8], [9], [10], [11]. In the single-phase circuit, V_{T1}~$V_{TNnpc/2}$ and θ_1~θ_{Nnpc} represent the output voltage of each single-phase transformers and the initial phase angles of output voltages for these NPC inverters, respectively. The single-phase transformers are custom-built, with each primary winding of the transformer functioning as a subtractor for output voltages of two NPC inverters, and the series-connected secondary windings summing up all inverter voltages. To create additional number of output voltage levels for V_{T1}~$V_{TNnpc/2}$ and V_{pcc}, it is important to regulate different θ_1~θ_{Nnpc} for each NPC inverter. To achieve this, the carried-based phase-disposition (PD) PWM is widely used in the cascaded NPC-based GEs [8], [11].

Fig. 5(b) and Table III depict an example of single-phase output voltage generation and all operating states of a GE utilizing two cascaded NPC inverters. *m*_NPC1 and *m*_NPC2 denote the modulation references for the two NPC inverters. C1_NPC1 and C2_NPC1 are the carriers for the first NPC inverter, while C1_NPC2 and C2_NPC2 are the carriers for the second NPC inverter. Taking NPC1 as an example, the driving signal S_{a1} in Fig. 5(a) is generated by the comparison between *m*_NPC1 and C1_NPC1, while S_{a2} is produced by comparing *m*_NPC1 with C2_NPC1 [45]. Consequently, a 5-level line-to-neutral voltage at the PCC can be achieved by combining two 3-level output voltages of NPC inverters. In general, the number of line-to-neutral voltage levels N_{ln} at the PCC of the cascaded NPC-based GE is $2N_{npc}$+1 [8], where N_{npc} should be an even value, i.e., 2, 4, etc.

The PD-PWM and custom-built transformers can certainly cancel the switching harmonics and reduce the THD of PCC voltage [11]. In [8], it has been demonstrated that without ac filters at the CVG side, the THD of line-to-line voltage at the

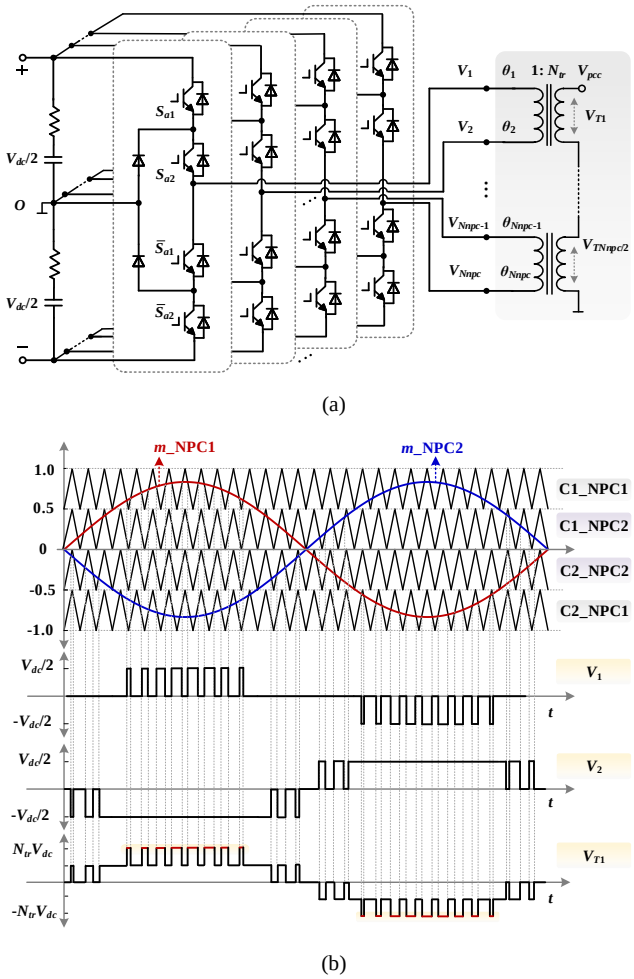


Fig. 5. Operation principle of the cascaded NPC-based GE. (a) Single-phase cascaded NPC inverter. (b) An example of single-phase PCC voltage generation of the GE using two NPC inverters.

TABLE III
OPERATING STATES OF A GE USING TWO CASCADED NPC INVERTERS

Output voltage V_1	Output voltage V_2	Output voltage V_{T1} of 1st transformer
0	0	0
0	$-V_{dc}/2$	$N_{tr}V_{dc}/2$
0	$V_{dc}/2$	$-N_{tr}V_{dc}/2$
$V_{dc}/2$	$-V_{dc}/2$	$N_{tr}V_{dc}$
$-V_{dc}/2$	$V_{dc}/2$	$-N_{tr}V_{dc}$

PCC can be reduced to 3.06% for N_{npc}=4 even if the switching frequency of semiconductors is below 500 Hz. This is because the number of line-to-line voltage levels N_{ll} (i.e., N_{ll}=$2N_{ln}$-1) can be as high as 17 [47]. However, since N_{ln} is only 9, the THD of the line-to-neutral voltage at the PCC may exceed the required limitation of 3%. Increasing the number of NPC inverters can create a higher N_{ln}, but this may pose a challenge to the quality of PCC voltage owing to different stray parameters of multiple single-phase transformers.

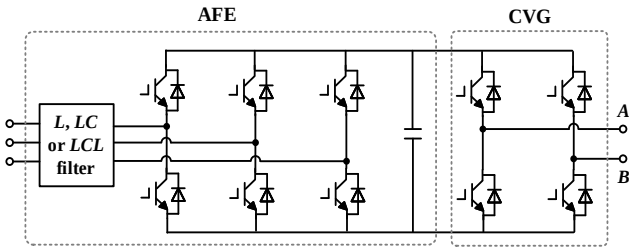


Fig. 6. H-bridge cell and regenerative AFE converter.

3) CHB-Based GE: Fig. 6 depicts the H-bridge cell of CVG and the regenerative AFE converter for the CHB-based GE. The AFE converters are connected to the power grid via a multi-winding AFE-side transformer, as seen in Fig. 3. For the CVG, the PSC-PWM is a practical approach for achieving the multi-level output and reduce the THD of the PCC voltage [13], [14], [17], [18]. In this case, N_{ln} can be given by [45]

$$N_{ln} = 2N_H + 1 \tag{9}$$

where N_H is the number of H-bridge converters per phase, which is one-third of the total number of secondary windings in the AFE-side transformer. A single commercial multi-winding transformer typically has 3 to 15 secondary windings [13], [14], which can offer a maximum N_{ln} up to 11.

To reduce the THD of the PCC voltage, the phase angles of the carriers in H-bridge cells are commonly shifted by π/N_H radians incrementally [48]. Yet, even with a N_{ln} up to 11, [48] has demonstrated that the THD of the line-to-neutral PCC voltage may still not meet the requirement. To achieve lower THD by increasing N_{ln}, the CHB-based GE needs to employ multiple multi-winding transformers for integrating with more H-bridge cells [16], which can result in a large volume and footprint.

4) MMC-Based GE: Fig. 7 illustrates a medium-voltage back-to-back (BTB) MMC-based GE [20]. The half-bridge SM (HBSM) [49] and full-bridge SM (FBSM) [22], [50] are two typical SMs in commercial MMCs. The PSC-PWM is a mature modulation method for HBSM- and FBSM-based MMCs to create the multilevel output, where their N_{ln} can be respectively expressed as [48], [51]

$$N_{ln\_HB} = 2N_{HB} + 1 \tag{10}$$

$$N_{ln\_FB} = 4N_{FB} + 1 \tag{11}$$

where N_{HB} and N_{FB} are the number of SMs per arm for the HBSM- and FBSM-based MMC, respectively.

To reduce harmonic voltages at the PCC, the phase angles of the carriers in each arm need to be shifted by $2\pi/N_{HB}$ [51] and π/N_{FB} [48] for the two types of MMCs, respectively. In particular, when N_{HB} and N_{FB} are even, the displacement angle of carriers between the upper arm and lower arm should be set to π/N_{HB} [52] and $\pi/(2N_{FB})$ [51] for HBSM- and FBSM-based MMC, respectively, to minimize the THD of PCC voltage. Nevertheless, in the absence of ac filters, the THD of line-to-neutral PCC voltage may still exceed 3% in MMC-based GEs when using fewer HBSMs (e.g., ≤6) [43], [48] or FBSMs (e.g., ≤3) [22].

5) Comparison: According to Table I, when $N_{npc}=N_H=N_{HB}=N_{FB}/2$, the interleaved/cascaded NPC-, CHB- and MMC-based

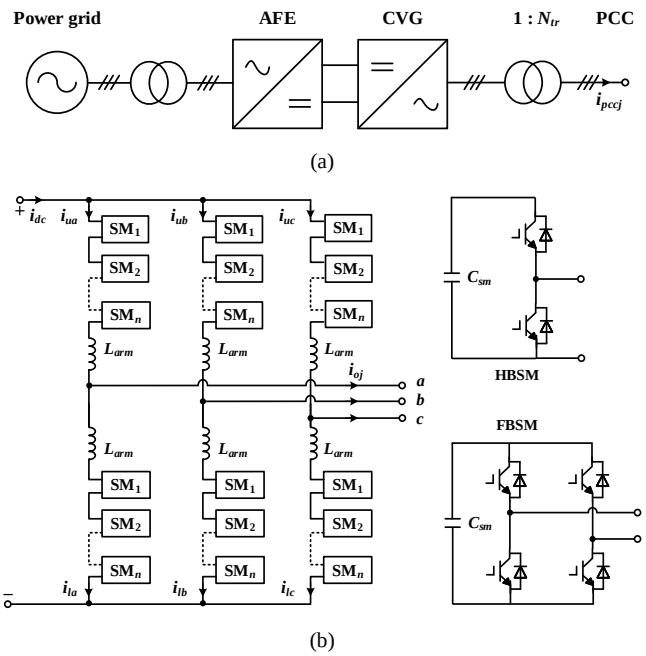


Fig. 7. The MMC-based GE. (a) Overall topology. (b) AFE or CVG topology with typical SMs.

GEs can produce similar multilevel output voltage and THD of PCC voltage. However, increasing N_{npc} to meet the required THD in the NPC-based GEs is limited by the manufacturing process of the CVG-side transformers. The maximum achievable N_H in the CHB-based GE with a single AFE-side transformer is constrained by its secondary windings. In contrast, the CHB-based GE with multiple AFE-side transformers and the MMC-based GE can offer more flexibility to achieve higher number of output voltage levels and to minimize THD.

B. AC Filter and Transformer at CVG Side

1) Interleaved NPC-Based GE: To fulfil the THD requirement, the ac filter is necessary, which may be installed either at the output side of each NPC inverter or at the medium-voltage PCC side. However, both approaches can cause a bulky volume and large footprint. To address this issue, the *RC* filter is typically installed in the tertiary winding with a lower voltage rating of the multi-winding transformer for interleaved NPC-based GEs, as shown in Fig. 3 [6], [7], [53]. Thanks to the leakage inductance of the transformer, an equivalent *RLC* filter is formed at the PCC, where the damping *R* is used to attenuate the *LC* resonance peak [7].

2) Cascaded NPC-Based GE: Even if N_{npc}>4, the ac filter would still be necessary to mitigate the impact of differences of single-phase transformers on the THD of PCC voltage [39]. To avoid a bulky filter bank in cabinets of NPC inverters, the ac filter can be installed at the PCC side [10], [54]. In this case, the leakage inductance of single-phase transformers are equivalent as an *L* filter, while the ac filter generally uses the *RC* filter [54].

3) CHB-Based GE: The standard step-up transformer can be utilized at the CVG side of the CHB-based GE [12], [13]. In cases where a single multi-winding transformer at the AFE side, an *LC* [13] or *RLC* filter [55] is usually used at the

primary (lower-voltage) side of the step-up transformer. Additionally, considering the leakage inductance of the transformer, an equivalent *LCL* filter or *LCL* filter with damping *R* can be seen from the PCC. For the GE using multiple AFE-side transformers, increasing the H-bridge cells may achieve the THD requirement without an ac filter.

4) MMC-Based GE: The arm inductors of MMC are equivalent as the *L* filters at the ac side. Thus, differing from the CHB-based GE, the *C* or *RC* filter should be placed at the primary side of the standard two-winding transformer for the MMC-based GE with fewer SMs [17], [43].

Besides, increasing the number of SMs can remove the additional ac filter, which is able to scale up the inverter output voltage, reducing the ratio and power loss of the CVG-side transformer.

5) Comparison: The ac filter in the cascaded NPC-based GE experiences a higher terminal voltage as the PCC voltage increases, resulting in a larger volume and footprint compared to the other three GEs. Using ac filters in the CHB- and MMC-based GEs can facilitate their scalability, as the filter-less option requires a minimum number of the output voltage levels, and consequently, H-bridge cells and SMs.

Besides, compared to the multi-winding transformer, the custom-built single-phase transformer can achieve the same PCC voltage using a lower step-up ratio N_{tr}. However, the multi-winding and custom-built single-phase transformers bring more manufacturing complexities than the standard transformer. For instance, multiple secondary or primary windings along the core limbs may drive a highly unequal stray inductance for different connected converters [14]. Consequently, the interleaved NPC-based GE is commonly used to test WTs lower than 33 kV [6], while the cascaded NPC- and CHB-based GEs can be employed in 33 kV~66 kV applications [13], [39]. The MMC-based GE shows more advantages at higher voltages, i.e., 66 kV~132 kV [19].

C. Number, Voltage Stress and Current Stress of Power Semiconductor Devices

1) Interleaved NPC-Based GE: It is assumed that the anti-parallel diodes are integrated into the power switches in Fig. 4(a). Considering the neutral-point diodes in each phase, the interleaved NPC-based CVG consists of $3\times6N_{npc}$ power semiconductor devices that must withstand $V_{dc}/2$. According to (8) and Fig. 4(a), the magnitude of current I_{sw} flowing through these power semiconductor devices can be given by

$$I_{sw}=\frac{I_{pcc}N_{tr}}{N_{npc}}+\frac{N_{tr}V_{dc}}{2Z_{in}}\left(1-\frac{1}{N_{npc}}\right) \tag{12}$$

where I_{pcc} is the magnitude of phase current flowing the PCC.

2) Cascaded NPC-Based GE: Figs. 3 and 5 show that the cascaded NPC-based CVG has $3\times6N_{npc}$ power semiconductor devices with the voltage stress of $V_{dc}/2$. The separate design of the custom-built single-phase transformer eliminates the circulating current between NPC inverters [11]. Consequently, I_{sw} is expressed as

$$I_{sw}=I_{pcc}N_{tr} \tag{13}$$

3) CHB-Based GE: Fig. 6 shows that there are $3\times4N_H$ and $3\times6N_H$ semiconductor devices in the CVG and AFE, respectively. Their voltage stress is the cell capacitor voltage V_{cell} [13], [14]. Each AFE converter is equivalent to a controlled dc voltage source, which can eliminate the circulating current flowing between the H-bridge arms [13]. Thus, I_{sw} is also $I_{pcc}N_{tr}$.

4) MMC-Based GE: Fig. 7(b) shows that a CVG/AFE of the HBSM- and FBSM-based MMCs consists of $6\times2N_{HB}$ and $6\times4N_{FB}$ power semiconductor devices, respectively. For both HBSM and FBSM, the semiconductors must be able to withstand the voltage V_{sm} of SM capacitors. Besides, the upper and lower arm current of MMC can be expressed as [20]

$$i_{uj}=i_{cirj}+\frac{i_{pccj}N_{tr}}{2} \tag{14}$$

$$i_{lj}=i_{cirj}-\frac{i_{pccj}N_{tr}}{2} \tag{15}$$

where i_{uj} and i_{lj} are upper and lower arm current per phase (j=*a*, *b*, *c*). i_{pccj} represents the ac current flowing in the PCC. i_{cirj} is the circulating current, including dc and ac components. The dc circulating current i_{cirdc} is used for the active power transmission, while the ac circulating current i_{cirac} (i.e., even-order) is introduced by the voltage fluctuations of floating SM capacitors [56]. Thus, the current stress of the semiconductors in MMC is expressed as

$$I_{sw}=I_{cir}+\frac{I_{pcc}N_{tr}}{2} \tag{16}$$

where I_{cir} is magnitude of the circulating current.

Particularly, i_{cirdc} is one-third of the dc-link current and i_{cirac} can be suppressed by the internal control of MMC during normal steady-state operation [17], [20]. In this case, I_{sw} can be simplified as

$$I_{sw}=\frac{V_{pcc}I_{pcc}}{2V_{dc}}+\frac{I_{pcc}N_{tr}}{2} \tag{17}$$

5) Comparison: The number and voltage stress of power semiconductor devices of the cascaded NPC-based GE are same as those in the interleaved NPC-based GE. However, it is important to design the intermediate impedance Z_{in}, which includes L_f and the leakage impedance of the multi-winding transformer, to mitigate circulating current in the interleaved NPC-based GE [7]. Otherwise, its I_{sw} may be higher than that of the cascaded NPC-based GE, causing more power loss.

Additionally, the voltage stress of power semiconductor devices is similar in the CHB- and MMC-based GE [13], [22], [43]. However, to achieve the same multilevel output, the CHB-based GE will require more power semiconductor devices, as shown in Table I. Generally, V_{dc} is greater than V_{pcc}/N_{tr} in (17), indicating that the steady-state I_{sw} in the MMC-based GE is lower than that in the CHB-based GE [48].

D. Actual Applications

Table IV lists the actual applications of different converter topologies for GEs, along with their system specifications. Figs. 8-14 depict the circuit diagrams of existing converter-based GEs.

Fig. 8 shows two interleaved NPC-based GEs in practice [5], [6], [7], [53]. In addition to increasing the number of

TABLE IV
ACTUAL APPLICATIONS OF MEDIUM-VOLTAGE MEGAWATT GES

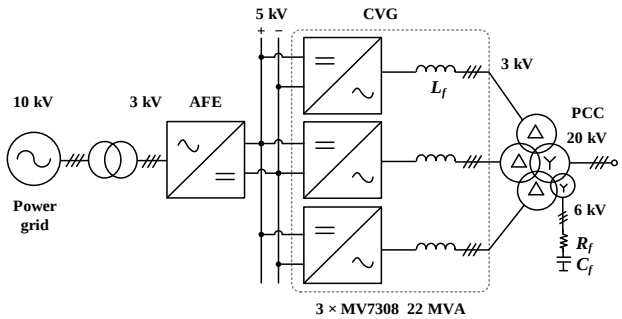
Testing centers	GE type	Apparent power	Short-term power	Converter type	Converters in AFE	Converters in CVG	DC-link voltage	CVG-side transformer
Aachen	Interleaved NPC-based GE	7 MVA	22 MVA	NPC (MV7306)	1	3	5 kV	3 kV/20 kV (7 MVA)
LORC		15 MVA	30 MVA	NPC (MV7315)	2	2	5 kV	3 kV/33 kV (16 MVA)
NREL	Cascaded NPC-based GE	7 MVA	40 MVA	NPC (ACS6000)	1	4	5 kV	3.3 kV/13.2 kV (7 MVA)
Fraunhofer IWES		15 MVA	44 MVA	NPC (ACS6000)	2	4	5 kV	3.3 kV/20 kV (36 kV) (15 MVA)
CEPRI	Single CHB-based GE	6 MVA	---	H bridge	9	9	1 kV	1.7 kV/35 kV (6 MVA)
Clemson	Multi-parallel CHB-based GE	15 MVA	20 MVA	H bridge	8*12	8*12	1.1 kV	4.16 kV/24 kV (2*7.5 MVA)

paralleled NPCs, employing NPCs with larger current ratings can also enhance the short-term power capacity of GEs.

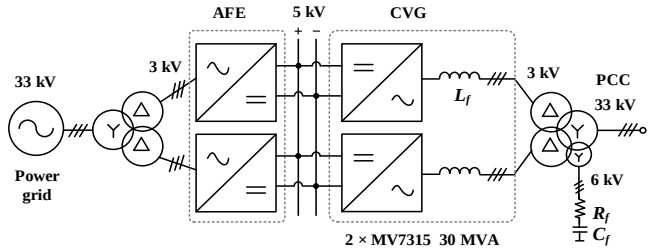
Fig. 9 depicts two commercial cascaded NPC-based GEs [8], [9], [10], [11]. To be able to test WTs with higher active power capacity, increasing the number of NPC inverters in the AFE is a practical solution. To accommodate the increasing power and voltage levels of WTs, Fig. 10 illustrates a GE rating at 20 MVA with a short-term power of 80 MVA, which is under development [39]. It utilizes three single-phase custom-built transformers to sum up the output voltages of 8 inverters, resulting in a PCC voltage up to 66 kV.

Figs. 11-12 show two CHB-based GEs using a single multi-winding transformer at the AFE side [13], [14]. For a higher multilevel output, Fig. 13 depicts another under-development 25 kV-7.5 MVA CHB-based GE [16]. In this configuration, 24 multi-winding transformers, each with 2 secondary windings, are employed to provide more interfaces for H-bridge cells.

Fig. 14 shows a multi-paralleled CHB-based GE for a higher power rating up to 15 MVA [12]. It contains two



(a)



(b)

Fig. 8. Commercial applications of interleaved NPC-based GEs. (a) A GE installed at Aachen (RWTH Aachen University, Germany) [6], [7], [57]. (b) A GE installed at LORC (Lindø Offshore Renewables Center, Denmark) [53].

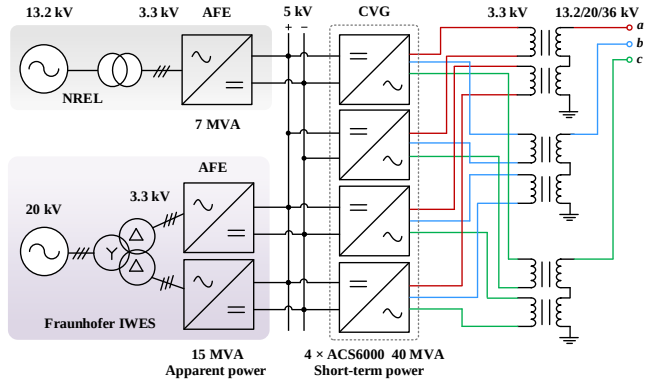


Fig. 9. The cascaded NPC-based GE used at NREL (National Renewable Energy Laboratory, USA) [8], [9], [10] and Fraunhofer IWES (Fraunhofer Institute for Wind Energy Systems, Germany) [6], [11].

groups of power conversion modules, each consisting of four paralleled CHBs and two transformers. Fig. 14(b) depicts the single CHB topology, which employs four multi-winding

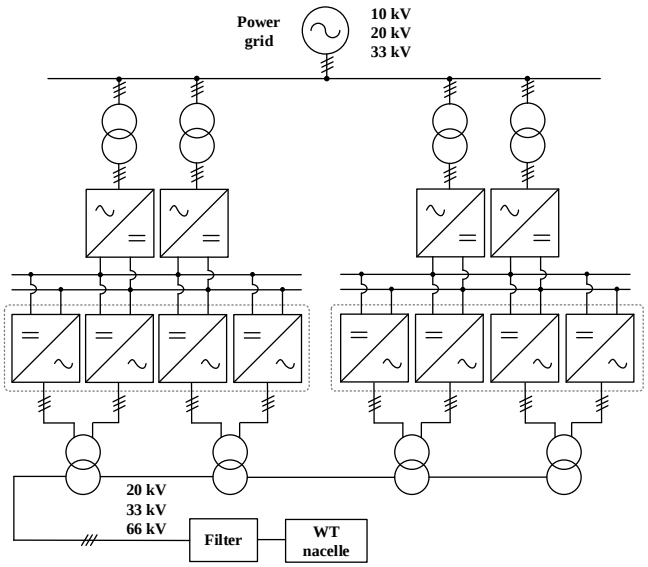


Fig. 10. A 20 MVA GE currently developing by Fraunhofer IWES [39].

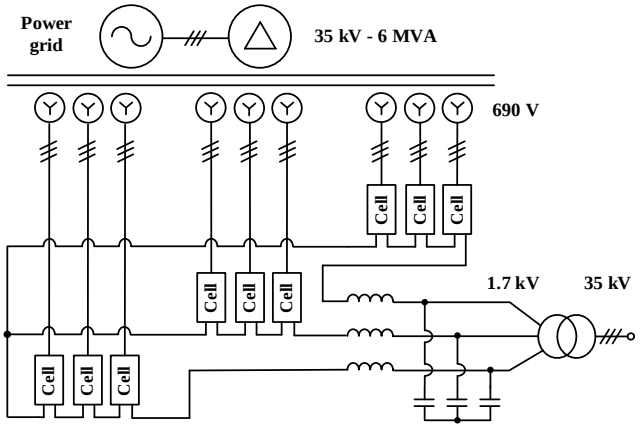


Fig. 11. A 35 kV-6 MVA CHB-based GE installed at the laboratory of CEPRI (China Electric Power Research Institute, China) [13].

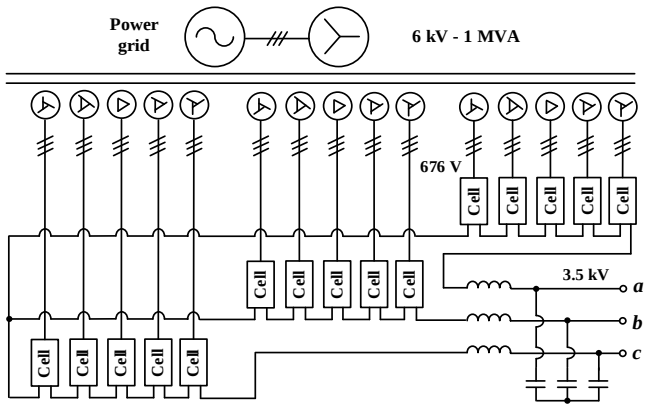


Fig. 12. A 6 kV-1 MVA CHB-based GE currently developing by EPFL (École Polytechnique Fédérale de Lausanne, Switzerland) [14].

transformers and 12 H-bridge cells. Consequently, increasing the number of power conversion modules is flexible to upscale the power rating of GE.

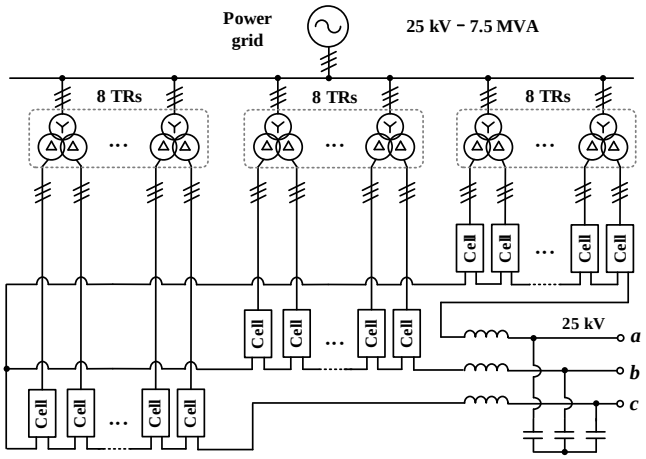
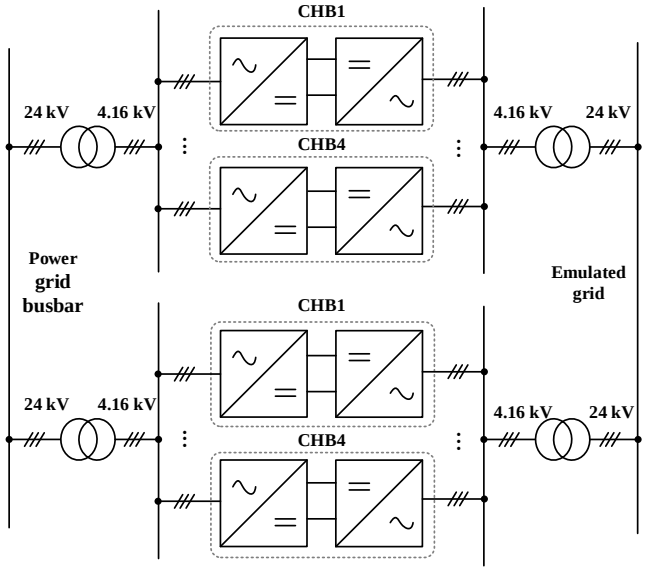
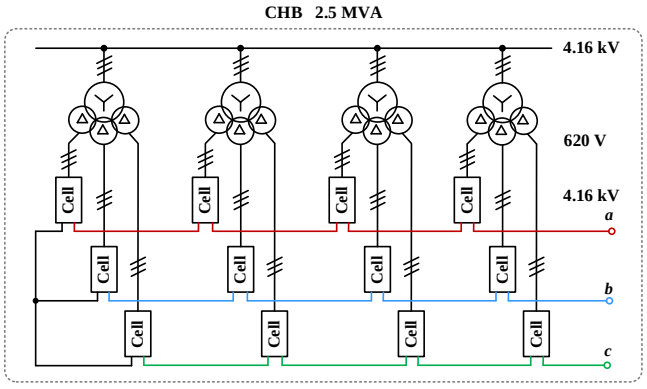


Fig. 13. A 25 kV-7.5 MVA CHB-based GE currently developing by IREQ (Hydro-Québec Research Institute, Canada) [16].



(a)



(b)

Fig. 14. The 15 MVA CHB-based GE installed at Clemson University based on the concept of series-parallel topology [12], [15]. (a) Overall topology. (b) Single CHB topology.

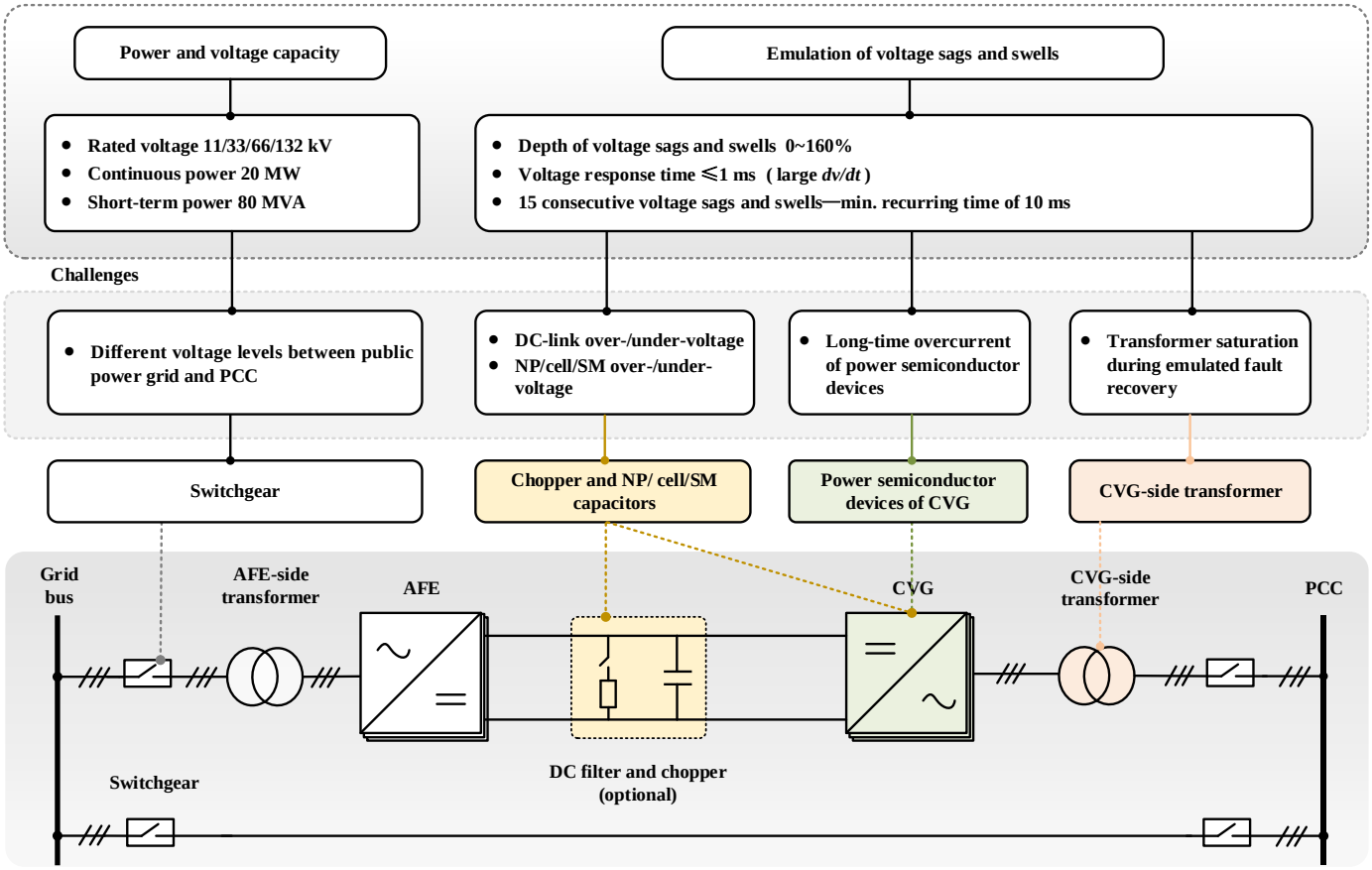


Fig. 15. Challenges of power components in interleaved/cascaded NPC-, CHB-, MMC-based GEs.

IV. Design Considerations of Power Components

Fig. 15 elaborates the challenges posed by latest grid codes and standards [19], [25], [26], [27], [38], [42], [58] for the power components in the interleaved/cascaded NPC-, CHB-, MMC-based GEs. To address these challenges, the design considerations for power components and unique difficulties are discussed.

A. Power Semiconductor Devices of CVG

1) Selecting Current Ratings: The power semiconductor devices of CVG should be able to withstand the continuous overcurrent injected by WTs during each FRT test. Typically, the continuous fault current for the PMSG-based WT is commonly limited within 1.5 p.u. [59]. By contrast, the fault current of the DFIG-based WT depends on the current limitation of BTB converters and the reactance of the DFIG. It can reach up to 7 p.u. and usually recover to 1~3 p.u. within 100 ms [23]. Thus, the maximum root-mean-square (RMS) value I_{fc} of PCC current flowing the GE can be expressed as

$$I_{fc} = \mathrm{Max}\left\{1.5I_{pcc\_PMSG}, 3I_{pcc\_DFIG}\right\} \tag{18}$$

where I_{pcc_PMSG} and I_{pcc_DFIG} are the normal RMS operating currents of PMSG- and DFIG-based WTs, respectively.

For the cascaded NPC- and CHB-based GEs, there is no circulating current and the power semiconductor devices should be rated for at least $I_{fc}N_{tr}$. Additionally, the circulating current flows in the interleaved NPC-based GE, which is dependent on the intermediate impedance Z_{in} and the fluctuations of dc-link voltage during FRT tests. Thus, the minimum current rating I_{cr} of power semiconductor devices for interleaved NPCs should be given by

$$I_{cr} = \frac{I_{fc}N_{tr}}{N_{npc}} + \frac{N_{tr}V_{dc}}{2Z_{in}}\left(1 - \frac{1}{N_{npc}}\right) \tag{19}$$

In respect to the MMC-based GE, the circulating current mainly contains the dc component during the continuous fault process, which represents the active power transmission [20]. Since the WT is required to inject the reactive current during emulated voltage sags and swells, the active current and circulating current will be lower than their normal values. According to (17), the power semiconductor devices should be rated at least

$$I_{cr} = \frac{V_{pcc}\mathrm{Max}\left\{I_{pcc\_PMSG}, I_{pcc\_DFIG}\right\}}{2V_{dc}} + \frac{I_{fc}N_{tr}}{2} \tag{20}$$

2) Types of Power Semiconductor Devices and Overcurrent Capability: The duration of the maximum transient fault current injected by the PMSG- /DFIG-based WTs, i.e., 2 p.u./ 7 p.u., is less than 20 ms in a single fault [23]. However, during the emulation of 15 consecutive faults, the GE is required to reproduce 6 severe faults with voltage magnitude less than 50% [27], [60]. As a result, the GE should be capable

TABLE V
SWITCHING POWER SEMICONDUCTOR DEVICES FOR MEGAWATT GES

Terms	Press-pack IGBT	Press-pack IGCT	Common IGBT
Applications in GEs	Interleaved NPC-based	Cascaded NPC-based	CHB-based
Voltage ratings	4.5 kV	4.5 kV	1.7 kV
Current ratings	0.75 kA~3.3 kA	0.95 kA~5 kA	0.1 kA~3.6 kA
Operating time at max. current	Moderate	Long	Short

of continuously operating at the maximum PCC current I_{fm} within 120 ms. I_{fm} is given by

$$I_{fm} = \mathrm{Max}\left\{2\sqrt{2}I_{pcc\_PMSG}, 7\sqrt{2}I_{pcc\_DFIG}\right\} \tag{21}$$

Besides the neutral-point diodes of NPC-based GEs, Table V illustrates three types of switching power semiconductor devices widely used in MW GEs, such as the press-pack insulated gate bipolar transistor (IGBT) [6], [40], [61], the press-pack integrated gate commutated thyristor (IGCT) [8], [11], [62] and the common IGBT [12], [13].

Owing to the high reliability of press-pack technology, the commercial NPC-based GEs based on press-pack IGBT and IGCT can continuously operate at the I_{fm} for 200 ms [7], [61] and even for 2 s [63] respectively. However, when the current flowing through the devices exceeds their current rating, the maximum duration for common IGBTs is much shorter, e.g., 1 ms [43]. Thus, extra attention should be given to the oversized design for CHB- and MMC-based GEs, indicating that changing power semiconductor devices or increasing current ratings.

In particular, for the MMC-based GE, a fundamental-frequency circulating current is commonly required to be injected to balance the SM capacitor voltage between upper and lower arms during the emulation of transient faults [18], [20]. This further increases the current flowing through the IGBTs and highlights the importance of oversized design.

3) Design Examples: Similar to the design target of the GE at the National Renewable Energy Laboratory (NREL) in the United States, it is assumed that four types of GEs need to test a 6.15 MW DFIG-based WT and a 6.15 MW PMSG-based WT at a same line-to-line PCC voltage V_{pccll}, e.g., 13.2 kV [63]. I_{fc} in (18) and I_{fm} in (21) can be respectively rewritten as

$$I_{fc} = 3I_{pcc\_DFIG} = 3\times\frac{P_{DFIG}}{\sqrt{3}\times V_{pccll}} \approx 810\ \mathrm{A} \tag{22}$$

$$I_{fm} = 7\sqrt{2}I_{pcc\_DFIG} = 7\sqrt{2}\times\frac{P_{DFIG}}{\sqrt{3}\times V_{pccll}} \approx 2660\ \mathrm{A} \tag{23}$$

Regarding the cascaded NPC-based GE with N_{npc}=4, the output line-to-line voltage of each NPC inverter is typically 3.3 kV, which leads to the turns ratio N_{tr}=1 for the custom-built single-phase transformers. Consequently, the current rating I_{cr} and maximum current I_{mc} of power semiconductor devices in the CVG-side NPC inverters must be larger than I_{fc} and I_{fm}, respectively. Besides, the power rating of the AFE-side NPC inverter should exceed 6.15 MW. To ensure high scalability of the GE, the NPC inverters on both AFE and CVG sides are typically identical, and I_{cr} should satisfy

$$I_{cr} > \frac{6.15\times10^{6}}{\sqrt{3}\times3.3\times10^{3}} \approx 1080\mathrm{A} \tag{24}$$

In the commercial ACS6000-series setups, ACS 6107 using IGCT devices with I_{cr}=1300 A and I_{mc}=2700 A can be selected for the cascaded NPC-based GE [62], which is actually implemented in the GE at NREL [8]. However, the current largest 7 MW PMSG-based WTs cannot be tested by this setup, which is currently under upgrading at NREL.

In respect to the interleaved NPC-based GE, the circulating current is generally mitigated below half of normal operating current through designing Z_{in} to prevent high current stress for the power semiconductor devices [7], [53], [57]. According to (19), I_{cr} and I_{mc} should respectively satisfy

$$I_{cr} > \left(I_{fc} + 0.5I_{pcc\_DFIG}\right)\frac{N_{tr}}{N_{npc}} \tag{25}$$

$$I_{mc} > \left(I_{fm} + 0.5I_{pcc\_DFIG}\right)\frac{N_{tr}}{N_{npc}} \tag{26}$$

The commercial MV7000-series setups, featuring press-pack IGBTs, are commonly used for the interleaved NPC-based GEs [40], [57]. When the NPC inverter is rating at 3.3 kV output, the turns ratio of the multi-winding step-up transformer is N_{tr}=4 to realize V_{pccll}=13.8 kV. Considering the limitation of windings of the step-up transformer, if N_{npc}=3, MV7308 with I_{cr}=2100 A and I_{mc}=4200 A [61] can be selected to meet the requirements in (25) and (26).

For the CHB-based GE, the current rating I_{cr} and maximum current I_{mc} of power semiconductor devices must be greater than $I_{fc}N_{tr}$ and $I_{fm}N_{tr}$, respectively. Typically, I_{mc} is twice of I_{cr} in common IGBTs and their maximum operating time at I_{mc} is 1 ms [64]. Due to I_{fm}/I_{fc}>2, the selection of common IGBTs for the CHB-based GE relies on the maximum current I_{mc}. Consequently, an oversized design of a common IGBT is recommended, such as I_{mc}=(1.5~2)$I_{fm}N_{tr}$ and I_{cr}=0.5I_{mc} [65].

Regarding the MMC-based GE, I_{mc} is dependent on both the transient circulating current and the maximum PCC current I_{fm}. In general, the maximum circulating current can be up to 2 times the normal value I_{cir} during transient events [21], [66]. If common IGBTs are used in the MMC-based GE, according to (20), I_{mc} should be expressed as

$$I_{mc} = (1.5\sim2)\left(\frac{V_{pcc}I_{pcc\_DFIG}}{V_{dc}} + \frac{I_{fm}N_{tr}}{2}\right) \tag{27}$$

B. CVG-Side Transformer

1) Additional Taps for Overvoltage Emulation: A practical method for emulating the grid overvoltage is to use additional tap changers in the secondary windings of the CVG-side transformer [11], [12]. For instance, the cascaded NPC-based GE implemented at the Fraunhofer Institute for Wind Energy Systems (IWES) in Germany employs custom-built single-

phase transformers with additional three taps. These taps are rated at 13 kV, 26 kV, and 46.8 kV, allowing the system to achieve a voltage level up to 30% higher than the rated voltage [11], [67]. To prevent transformer saturation during tap changes, the taps should be switched while the transformer is de-energized [9], [12]. Subsequently, the emulation of voltage swells can be achieved by regulating the modulation index of the converter-based GE.

2) Anti-Saturation of Transformer: Fig. 16 illustrates the mechanism of transformer saturation, where v_1, i_1, R_1, L_1, v_2, i_2, R_2 and L_2 are the terminal voltage, winding current, leakage resistance and leakage inductance at the primary- and secondary-side, respectively. R_m, L_m, i_m and λ_m denote the core-loss resistance, magnetizing inductance, magnetizing current and magnetizing flux, respectively. According to Kirchhoff's Voltage Law (KVL), without connecting WTs, the primary side of transformer should satisfy

$$i_1 R_1 + L_1 \frac{di_1}{dt} + \frac{d\lambda_m}{dt} = V_1 \sin(\omega_1 t + \alpha) \tag{28}$$

where V_1, ω_1 and α are the magnitude, angular frequency and initial phase angle of primary-side voltage.

It is assumed that the residual flux is λ_r before the startup of the GE, by solving (28), λ_m after the transformer energization can be derived as [68]

$$\begin{cases} \lambda_m(t) \approx -\lambda_{rated}\cos(\omega_1 t + \alpha) + (\lambda_{rated}\cos\alpha + \lambda_r)e^{-R_1 t/(L_1+L_m)} \\ \lambda_{rated} = \dfrac{L_m V_1}{\sqrt{R_1^2 + \omega_1^2 (L_1+L_m)^2}} \end{cases} \tag{29}$$

When α=0 and $t=\pi/\omega_1$, λ_m has a maximum magnitude $\lambda_p=2\lambda_{rated}+\lambda_r$. Since the saturation flux λ_s of transformer is typically in the range of (1.15~1.4)λ_{rated} [69], $\lambda_m>\lambda_s$ can lead to the inrush current around 2~10 times of the rated current [70], which may trip the GE or even damage the power components. Depending on the ratio of $R_1/(L_1+L_m)$, the natural decaying response of the dc flux and inrush current may take 20 s~90 s [71]. To prevent the transformer saturation during the startup process, selecting a proper α (e.g., $\alpha=\pi/2$) along with a slow ramp of the primary-side voltage is a common approach for GEs [8], [72].

When emulating a voltage sag with a rapid recovery within the required 1 ms [8], [25], the uncertain α and a high rate of change of voltage recovery (i.e., dv/dt) may cause transformer saturation [73], [74]. In this case, considering that leakage flux, the total flux λ_j (j=a,b,c) at the primary side of transformer can be expressed as [73]

$$\lambda_j(t) = \underbrace{\lambda_j(0) + \int_0^t v_j(t)dt}_{\lambda_{j,ac}} + \underbrace{\int_{t_{sag}}^{t_{rec}} \left[v_{j,sag}(t) - v_j(t) \right] dt}_{\lambda_{j,dc}} \tag{30}$$

where $\lambda_j(0)$, $\lambda_{j,ac}$ and $\lambda_{j,dc}$ are the initial value, ac component and dc component of λ_j, respectively. v_j and $v_{j,sag}$ are the primary-side voltage of transformer during normal operation and voltage sag, respectively. t_{sag} and t_{rec} are the time instants of emulated voltage sag and fault recovery.

Consequently, the dc deviation of magnetizing flux $\lambda_{j,dc}$ may lead to transformer saturation, which depends on the types of voltage sags, sag depth, sag instant and fault recovery

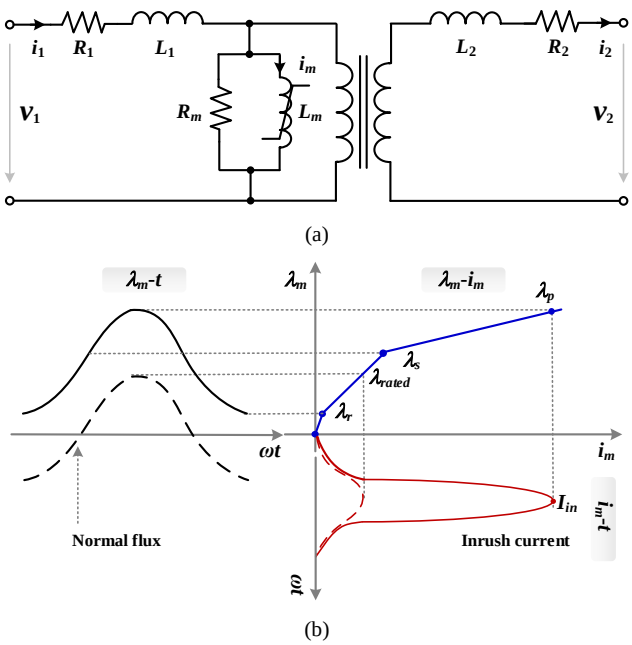


Fig. 16. Mechanism of transformer saturation. (a) Equivalent single-phase transformer model. (b) Magnetic characteristics.

instant. To alleviate the saturation effect from the power hardware perspective, the magnetic cores and coil windings of the GE transformer should be intentionally designed. According to (29), one simple solution is to increase the leakage inductance in the magnetic core, thereby reducing λ_{rated}. This can be accomplished by introducing a larger realistic air gap or a virtual air gap through an auxiliary dc source [75]. However, this approach may lead to increased power loss or a larger volume of the transformer, which may be impractical. Another straightforward solution is to increase λ_s for a higher flux boundary of transformer saturation. The expression for λ_s can be given by [76]

$$\lambda_s = \mu_0 \mu_{r\max} K_T \frac{N_1 I_1}{l_e} A_e \tag{31}$$

where μ_0 is the permeability of air and $\mu_{r\max}$ is the maximum permeability of magnetic materials. K_T is a coefficient related to the temperature of magnetic core. N_1 and I_1 are the number of turns and current of primary winding, respectively. l_e is the height of the coil winding, while A_e is the cross-sectional area of the primary winding.

A_e is directly proportional to the area of magnetic core and is highly dependent on the coil winding distribution [77]. Although selecting a higher N_1 with a larger magnetic core and reducing l_e can increase λ_s, it inevitably increases the volume, footprint and cost of transformer. Alternatively, altering the distribution of coil windings to maximize A_e is suggested in [76] and [77]. For example, in the CHB-based GE system at Clemson University, by selecting the limb configuration and the cross-sectional area of primary windings, a bank of three single-phase step-up transformers with λ_s=1.45λ_{rated} has been employed [12], [65].

C. DC-Link Chopper and NP/Cell/SM Capacitors

During severe voltage sags and swells in the power grid, the WT is required to inject maximum reactive current within 20 ms [78]. Absorbing such current tends to cause the over-/under-voltage of the dc link and NP/cell/SM capacitors of GEs, especially when emulating multiple consecutive grid faults [9], [14], [20]. To address these issues, adding a dc chopper and deliberately designing NP/cell/SM capacitance are needed.

1) Types of DC-Link Choppers: Fig. 17 depicts a commonly used dc chopper in a cascaded NPC-based GE at NREL, which consists of IGCTs, resistors, and capacitors [9]. Fig. 18 shows a modularly designed dc-link chopper that comprises series-connected SMs, which provides a viable option for the MMC-based GE [79]. For the CHB-based GE, there is lack of a common dc link. Installing a chopper in each converter cell can increase its volume and footprint.

2) Designing NP/cell/SM Capacitance: Besides the voltage-ripple and energy storage requirements [80], [81], the transient over-/under-voltage in the GE should be also considered in the design of NP/SM/cell capacitance. Fig. 19 shows a controller-hardware-in-the-loop (CHIL) experimental result of the MMC-based GE with 4 FBSMs per arm during an LVRT test [20]. V_{cu_av} and V_{cl_av} represent the averaged upper- and lower-arm SM capacitor voltage, respectively. i_{o_WT} is the output current of a WT. Due to the fault current injected by WT, the large ripple and transient variation simultaneously occur in V_{cu_av} and V_{cl_av}.

In [20], an average SM capacitor model for the MMC-based GE with FBSMs has been established when emulating the three-phase balanced faults. The relationship between SM capacitance and the maximum/ minimum transient capacitor voltage can be expressed as

$$\begin{cases} \mathrm{Max}\{u_{csm}\} \approx V_c + \dfrac{V_{dc} I_{o\max}}{2N_{FB} V_c \omega_1 C_{sm}} \\ \mathrm{Min}\{u_{csm}\} \approx V_c - \dfrac{V_{dc} I_{o\max}}{2N_{FB} V_c \omega_1 C_{sm}} \end{cases} \tag{32}$$

where V_c and C_{sm} are the rated voltage and capacitance of SM capacitor. $I_{o\max}$ is the maximum current injected by the WT.

The required operating range of SM capacitor voltage is commonly 60%~120% of V_c [20]. Thus, the SM capacitance can be derived as

$$C_{sm} \geq \frac{V_{dc} I_{o\max}}{0.4 N_{FB} V_c^2 \omega_1} \tag{33}$$

Transient variations of the NP/cell capacitor voltages also occur in the NPC-/CHB-based GEs during FRT tests [9], [14]. However, the analytical maximum and minimum capacitor voltages have not yet been reported in NPC-/CHB-based GEs.

D. Switchgear

Fig. 20 illustrates a switchgear configuration of a GE system, which is used to interconnect with the GE, power grid and WT system. The switchgear is used to switch the system between operating scenarios, which are 1) the WT is directly connected to the power grid, and 2) the WT is connected to the power grid via the GE.

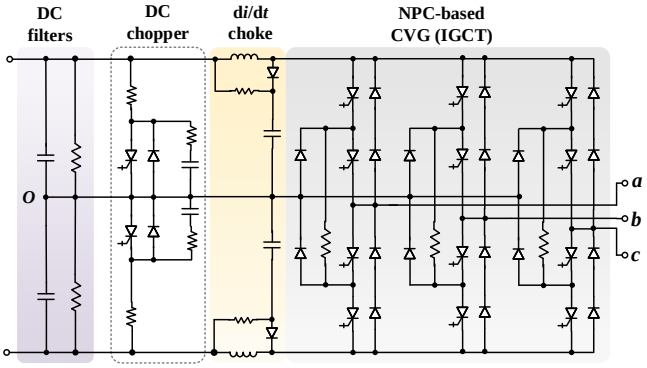


Fig. 17. Topology of IGCT-based NPC ACS6000 converter [9].

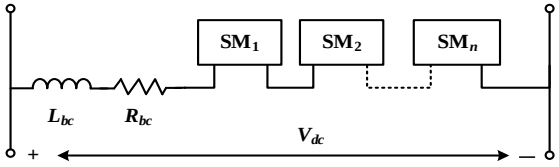


Fig. 18. A modular chopper [79].

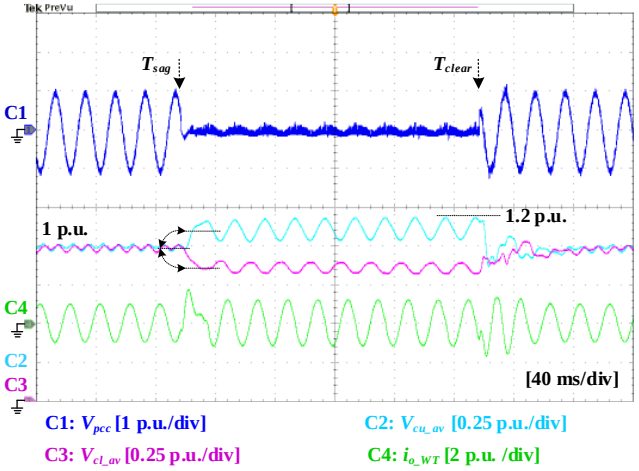


Fig. 19. A CHIL result of the MMC-based GE during an LVRT test [20].

When the output voltage of GE differs from the power grid, the switchgear should be able to separate two different voltage levels [82]. Thus, the highlighted breakers and contactors of Fig. 20 should exhibit double insulation behavior [53], [82]. One common approach to achieve this is by increasing the current rating of the single busbar in GE installations. For instance, at the Lindø Offshore Renewables Center (LORC) in Denmark, a breaker and contactor with a rating of 1250 A/40.5 kV is utilized to separate the public grid from the GE output, whereas other regular breakers and contactors are rated at 630 A/33 kV [53].

V. Emerging Trends

Following the comparisons of converter topologies and the power-hardware design considerations of current GEs, this section explores two emerging trends of hardware design aspects for the future converter-based GEs.

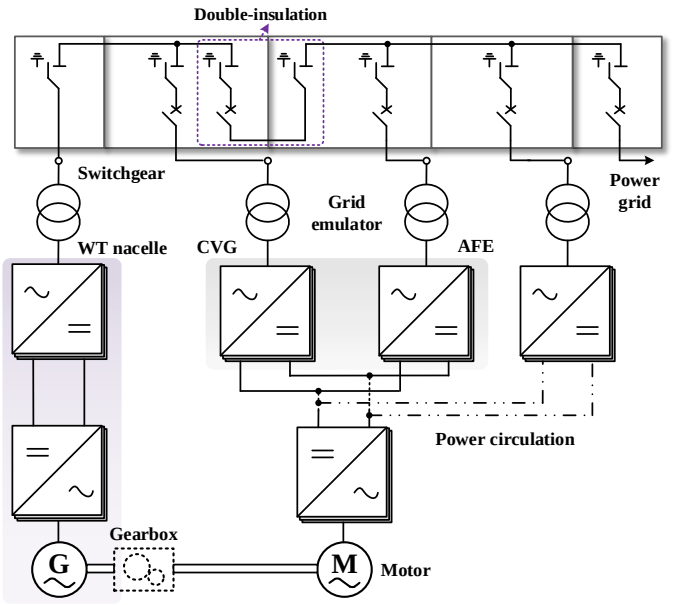


Fig. 20. Grid emulation system with a switchgear for the separation between emulated grid and power grid [53].

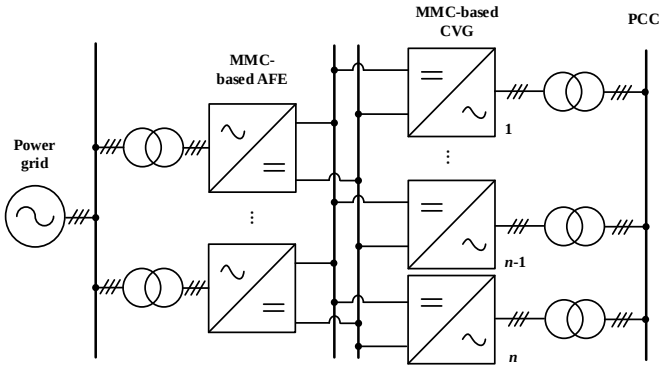


Fig. 21. A GE based on the multi-paralleled MMCs.

A. High-Voltage Grid Emulation

As the power rating of single offshore WT increases, the use of transmission cables with larger wire diameter becomes necessary to accommodate the current PCC voltage of 66 kV. However, this poses challenges for the array design of offshore wind farms [2]. Consequently, the PCC voltage of next-generation WTs tends to be higher, potentially reaching 132 kV [3].

Fig. 21 shows a potential GE based on multi-paralleled MMCs for testing future WTs [83]. Using the standard two-winding transformer with each MMC is important to prevent the circulating current between the paralleled MMCs and to ensure the isolation between GE and WTs. A commercial medium-voltage MMC typically use 5~20 floating SMs per arm in to achieve a 3.3 kV~13.8 kV output voltage [49], [50]. Increasing the number of SMs and using power semiconductor devices with higher current rating in a single MMC can realize its power rating up to 70 MVA [49].

B. Three-Phase Four-Wire System with Single-Phase Step-up Transformers

Recently, the power grid has been experiencing a growing penetration of renewable energy resources, energy storage systems and power-to-x systems, etc. However, when this hybrid energy system is integrated into a single PCC, their dynamic interactions may lead to system instability, despite each individual system meeting the grid-code requirements [63]. It is therefore important for a GE to perform the dynamic interaction test of the hybrid energy system.

The FGW TR3 specifies that the zero-sequence voltage emulation of a GE is unnecessary for the WT testing, owing to the typical use of delta (Δ)-star (Y) transformer with WTs [30], [58]. However, for a hybrid energy system testing, a GE should employ the three-phase four-wire connection at the PCC to provide a path for zero-sequence components [15]. In addition, the CVG-side transformer of the GE must be able to transmit the zero-sequence components while maintaining normal magnetizing current. As a result, it is common practice to employ three single-phase transformers in commercial GEs [9], [12].

VI. Conclusion

This paper provides a comprehensive review on the power hardware design of megawatt power-electronic-based grid emulation system, with a special attention to power converter topologies and design considerations for power components. Three categories of GEs in terms of system configurations are discussed, which point out that the GE technology is evolving towards high scalability and filter-less design for versatile testing of WTs. The interleaved/ cascaded NPC-, CHB-, MMC-based GEs have been compared and the MMC-based GE is identified as a promising solution for future 15+ MW WTs. Design considerations of power components in GEs have also been presented, such as the oversized design of power semiconductor devices, the choice of dc-link choppers, the anti-saturation design of transformers, and the double insulation of switchgear. Finally, design aspects of power hardware are discussed for two prospective GEs, i.e., the multi-parallel MMC-based GE and the three-phase four-wire GE.

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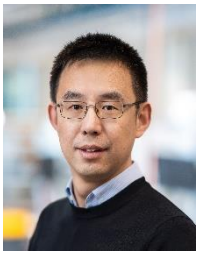

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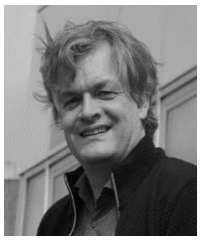

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