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Published in:
IET Power Electronics

DOI (link to publication from Publisher):
10.1049/pel2.12204

Publication date:
2022

Document Version
Publisher's PDF, also known as Version of record

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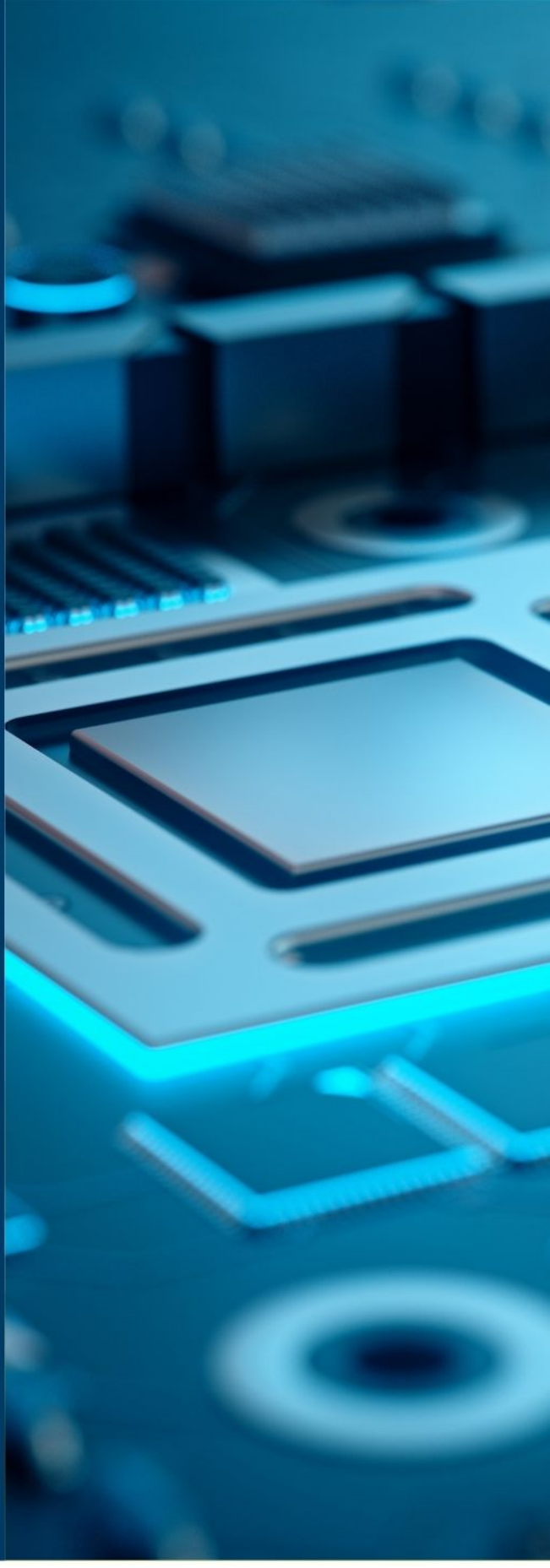

The Institution of Engineering and Technology

Received: 4 January 2021 | Revised: 19 July 2021 | Accepted: 26 August 2021

IET Power Electronics

DOI: 10.1049/pel2.12204

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ORIGINAL RESEARCH PAPER

Development of a current source resonant inverter for high current MHz induction heating

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Funding information
Innovationsfonden

Abstract

High frequency industrial induction heating processes typically employ resonant inverters to reach high efficiency at high power levels. Advancements in wide band gap (WBG) device technology has made it feasible to push the possible frequency of these processes into the MHz regime using solid state technology. Several topologies can be applied, each with advantages and drawbacks. This paper presents a current source resonant inverter (CSRI) employing a custom designed power module utilizing 1700V SiC MOSFETs for MHz operation of a high-Q resonant tank for induction heating, which presents new challenges in the inverter module design. An integrated gate driver structure is demonstrated driving four MOSFETs in parallel in MHz operation. Theoretical analysis predicts substantial parasitic influence on inverter operation, and thus an inverter is constructed to provide experimental verification of MHz operation, while the challenges associated with high frequency CSRI operation are discussed. In the experimental inverter setup, the fabricated power module achieves > 90% efficiency for a calculated reactive power of 170 kVA and 2.3 kW output power during unloaded operation, validating the inverter design for extension to higher power loaded operation.

1 | INTRODUCTION

High power high frequency electrical power is used in several industry applications where power delivery of multiple kW at frequencies of hundreds of kHz to tens of MHz is required. These processes include induction heating, dielectric heating, and plasma processing [1–3]. Inverter systems based on solid state components are commercially available for frequencies up to several hundred kHz, with MOSFET-based inverters dominating the upper frequency range [4]. In recent years, several researchers have investigated the feasibility of pushing the frequency limits of single power inverters of several kWs into the MHz regime, primarily facilitated by the usage of wide band gab (WBG) semiconductor devices [5–8].

In the design of high power generator systems for induction heating applications at MHz frequencies, oscillators based on vacuum tubes are commonly used due to the high frequency and power requirements of the processes. This is, for example, the case for some industrial implementations of zone refining processes for the growth and purification of crystals, where induction heating is applied that may require frequencies of multiple MHz [9, 10]. However, the efficiency of vacuum tube oscillators is low, leading to considerable energy loss in these processes [11, 12]. Solid state technology promises improved efficiency in these applications, but as single turn coils are commonly used, the equivalent resistance of the load may be very low, demanding very high coil current to reach the required power deposition in the load [1]. Additionally, common to induction heating applications, coupling between coil and load can vary greatly depending on workpiece temperature, material, and geometry, requiring the power inverter to be adaptable to changing resonant frequency and loading while maintaining efficiency [13]. Combined with the high frequency requirements, this requires careful design of the inverter system to achieve high efficiency.

Several circuit topologies have been applied to induction heating processes, with the common characterization as either current source resonant inverters (CSRI) or voltage source resonant inverters (VSRI) [14]. The choice of topology for a particular application is largely determined by the application demands, such as the desired operating frequency, power output, load

impedance, and process specific parameters such as working coil short-circuit probability [15]. For low impedance coils designed for loads with low equivalent resistance, the current in the induction coil must be high to deposit appreciable power in the workpiece, which can necessitate the use of a transformer with considerable losses, especially for high frequency operation [16, 17]. Thus, the conventional wisdom is that voltage source systems are preferred for high impedance coils with multiple turns, while current source systems are better suited for low impedance, single turn coils [1, 18]. However, not much attention has been paid to the application of CSRIs based on solid state power components in this frequency regime, likely in part because the requirements for switching speed, power loss handling, and parasitic influence mitigation puts great demands on inverter design. This paper aims to investigate the feasibility of such an implementation.

The coupling to the load is significantly lower for single turn coils than for high impedance coils. Thus to achieve sufficient power delivery a high current flow in the coil is required, which at MHz frequencies means that a relatively high coil terminal voltage must be applied even for low impedance coils. Using lower voltage switches and a transformer to scale up the coil voltage can be attractive, but this option increases switch current stress, increases losses and component count, and introduces parasitics from the non-ideality of the transformer. Utilizing a transformerless CSRI avoids these issues, but requires the use of relatively high voltage switches. Wide band gap devices such as SiC MOSFETs are promising candidates for this type of application, combining high voltage blocking capability with fast switching action [19, 20]. Due to this, SiC has been successfully applied to both domestic and industrial induction heating in recent literature, especially for high frequency applications [21, 22]. Even with this approach, however, it can be necessary to parallel switching devices to improve the inverter current handling capabilities to deliver the required power to the load. The use of parallel devices increases both the gate drive requirements and the effective device parasitics, which enhances the need to pay close attention to inverter interconnections and layout to ensure proper functioning of the system at MHz frequencies. The influence of the parasitic elements in the operation of a high frequency CSRI is most pronounced at very high quality factor (Q-factor) of the work coil, which is thus an important operating point for induction heaters with highly variable loads. The highest attainable Q-factor, that is, unloaded operation, is then a relevant case study to investigate the feasibility of the CSRI using paralleled high voltage SiC MOSFETs in the MHz frequency regime.

To investigate this, this paper aims to demonstrate MHz operation of a bidirectional CSRI power module operating in conjunction with an unloaded parallel resonant tank. The challenges associated with this process, that is, the simultaneous requirements of frequency, resonant current, power, and voltage ranges, demands special attention to critical design parameters such as parallelization strategy, loss handling, gate driving, parasitic influences in the inverter system, and control requirements. These challenges and the proposed design solutions for utilizing paralleled SiC MOSFETs in MHz operation under these requirements will thus be the focus area of this work. Therefore, to address the need for a flexible power module capable of operating with an industrially relevant resonant circuit, a prototype power module is developed. This module showcases possible approaches for overcoming the challenges discussed above by using an integrated gate driver structure in combination with a highly symmetric power module layout with paralleled 1700V SiC MOSFETs and an inverter system designed for high frequency operation. The inverter fundamentals and specifics relevant to this application are presented in Section 2. The developed power module and resonant tank, along with important design considerations, are shown and discussed in Sections 3 and 4, respectively. Experimental tests of the integrated gate drive circuitry are presented in Section 5, along with demonstrations of resonant operation in unloaded conditions.

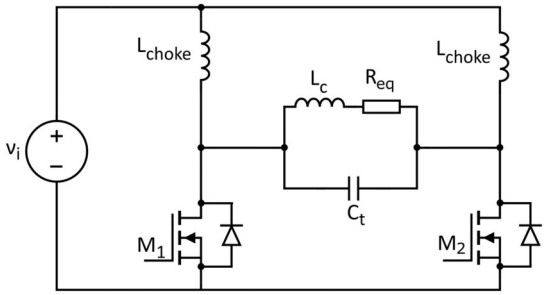

FIGURE 1 Schematic of the bidirectional current source resonant inverter (CSRI)

2 | BIDIRECTIONAL CSRI OPERATION

Although the CSRI topology is well known for induction heating, applying it in the MHz regime using power MOSFETs requires close attention to key design parameters for low impedance coils and high power operation. Therefore, a number of key aspects of the CSRI topology are revisited here and the impact of parasitic elements is analyzed to elucidate important system design parameters. The most common CSRI configuration employs series diodes to create switches that are unidirectional in current, while another option is using the CSRI topology without the series diodes, as is shown in Figure 1. In the CSRI, the input inductors L_{choke} are much larger than the resonant inductor L_c, so in steady state the DC current is constant and the input current to the resonant tank is a square wave. When series diodes are included, the output power level can be controlled through the switching frequency, whereas this is done by controlling the input current level for the diodeless version. The advantage of omitting the diodes, besides the reduced component count and cost, is that if switching operation at the resonant frequency is desired, not using diodes eliminates the losses associated with their on-state voltage drop (mainly relevant at low switch voltage) and reduces the turn-on losses of the switches by not clamping the voltage of the output capacitance prior to the turn-on event, which

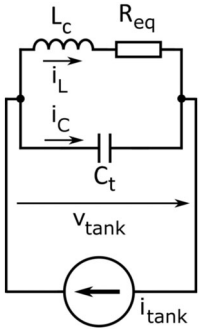

FIGURE 2 Parallel resonant tank of the CSRI

is particularly relevant at high operation frequency and high switch voltage as is the case here [23].

The induction heating coil is modelled as an inductance in series with an equivalent resistance, which includes both the coil resistance and the resistance of the work piece referred to the coil. The quality factor of the coil is defined as the ratio of reactive to real power

$$Q = \frac{|P_{react}|}{P_{real}} = \frac{\omega L_c}{R_{eq}}. \tag{1}$$

Considering ideal operation of the resonant tank with coil inductance L_c and tank capacitance C_t as shown in Figure 2, the input current to the resonant tank by KCL in the Laplace domain is

$$i_{tank}(t) = i_{Ct} + i_{Lc} \;\Rightarrow\; i_{tank}(s) = sCV_{tank} + \frac{V_{tank}}{sL + R_{eq}}. \tag{2}$$

Defining the undamped natural resonance frequency ω_n and the damping ratio ζ

$$\omega_n = \frac{1}{\sqrt{L_c C_t}}, \quad \zeta = \frac{R_{eq}}{2}\sqrt{\frac{C_t}{L_c}}, \tag{3}$$

gives the impedance

$$\begin{aligned} Z(s) &= \frac{V_{tank}(s)}{I_{tank}(s)} = \frac{sL_c + R_{eq}}{s^2 L_c C_t + sC_t R_{eq} + 1} \\ &= (sL_c + R_{eq})\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \end{aligned} \tag{4}$$

which is a well-known second order system. Transferred to the frequency domain, the impedance becomes

$$\begin{aligned} Z(s)|_{s=j\omega} = &\frac{R_{eq}}{(1-\omega^2 L_c C_t)^2 + (\omega C_t R_{eq})^2} \\ &+ j\frac{\omega(L_c - \omega^2 L_c^2 C - C_t R_{eq}^2)}{(\omega C_t R_{eq})^2 + (1-\omega^2 L_c C_t)^2}, \end{aligned} \tag{5}$$

Zero current and zero voltage switching will occur at the resonance frequency ω_r. The condition for this is tied to an impedance phase angle of zero, yielding

$$\angle Z(j\omega_r) = 0 \Longrightarrow \omega_r = \sqrt{\frac{L_c - C_t R_{eq}^2}{L_c^2 C_t}} = \omega_n\sqrt{1-4\zeta^2}. \tag{6}$$

Assuming high Q-factors, the damping term becomes small and $\omega_r \approx \omega_n$. In this case, the magnitude of the impedance at the resonance frequency becomes

$$|Z(\omega_r)|_{\omega_r=\omega_n} = \sqrt{\frac{L_c(C_t R_{eq}^2 + L_c)}{C_t^2 R_{eq}^2}} = R_{eq}Q\sqrt{Q^2+1}. \tag{7}$$

The resonant tank acts as a filter at the resonant frequency, and thus only the first harmonic of the square wave tank current is considered, the RMS value of which is expressed as

$$I_{tank} = \frac{\sqrt{2}}{\pi} I_{in}. \tag{8}$$

By similar analysis to that for the impedance, the transfer function for the current at the resonant frequency (gain) can be approximated assuming high Q-factor [24]

$$\frac{I_{res}(j\omega_r)}{I_{tank}(j\omega_r)} = \frac{1}{1 - \omega_r^2 L_c C_t + j\omega C_t R_{eq}} = -jQ. \tag{9}$$

The power consumed by the equivalent resistance in this case is then expressed from Equations (8) and (9) as

$$P_{out}(\omega_r) = I_{res}^2(\omega_r)R_{eq} = \frac{2I_{in}^2 Q^2 R_{eq}}{\pi^2}. \tag{10}$$

Applying the previous high-Q assumption that $\omega_r = \omega_n$, the impedance at the resonance frequency is purely real, such that $|Z(\omega_r)| = Z(\omega_r) = V_{tank}/I_{tank}$. Using this and the expression for the input power $P_{in} = V_{in}I_{in}$, the efficiency η can by written using Equation (7)

$$\eta = \frac{P_{out}}{P_{in}} = \frac{2I_{in}}{\pi^2 I_{tank}}\frac{V_{tank}}{V_{in}}. \tag{11}$$

Assuming $\eta = 1$ and high Q, the voltage transfer function from input voltage V_{in} to output voltage V_{tank} is then

$$\frac{V_{tank}(j\omega_r)}{V_{in}(j\omega_r)} = \frac{I_{tank}\pi^2}{2I_{in}} = \frac{\pi}{\sqrt{2}}, \tag{12}$$

resulting in a peak voltage for the tank and the switches of πV_{in}.

The analysis thus far has considered the ideal case of an inverter without parasitics. To conserve the basic operating scheme and the general validity of Equations (1)–(12) when considering real components, careful attention must be paid to the physical construction and control of the system.

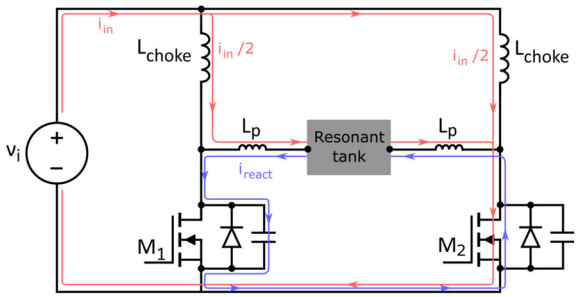

FIGURE 3 Schematic of the CSRI illustrating the current paths during a quarter of a switching cycle

As is apparent from Equation (9), a CSRI with a high Q-factor of the resonant tank circuit allows large resonant current with comparatively low switch current stress. Another advantages of the CSRI is that the parasitic output capacitance of the transistors are absorbed in the resonant tank capacitance since one of the switch capacitances will always be in parallel with the tank. For this reason, load resonant soft-switching can be achieved even considering device parasitics. This means, however, that the switch which is ON will also conduct the reactive current of the output capacitance of the other leg (blue in Figure 3)

$$i_{react} = i_{C_{tank}} \frac{C_{oss,eq}}{C_{tank}}, \quad C_{oss,eq} = \frac{\int_0^{V_{ds}} C_{oss}(V)\mathrm{d}V}{V_{ds}}, \tag{13}$$

where $C_{oss,eq}$ is the charge equivalent output capacitance of the MOSFET [25].

In light load conditions, this current can be of the same or higher magnitude than the DC current when using paralleled power MOSFETs, signifying a large deviation from the ideal circuit for the unloaded condition. Additionally, since there exists a non-zero loop inductance L_p as shown in Figure 3, there will be high frequency ringing with frequency

$$f_{react} = \frac{1}{2\pi\sqrt{2L_p C_{oss,eq}}}. \tag{14}$$

This resonance is only weakly damped due to the low $R_{ds,on}$ of the MOSFETs and low equivalent series resistance (ESR) of the capacitor bank. The parasitic inductance can induce voltage spikes across the switches which can be destructive if not managed in the design. The two general approaches to the control of the CSRI is to either minimize the parasitic inductance and thus neglecting it in the control of the semiconductors, or to introduce an overlap between the gating signals amounting to the time it takes for the current in the parasitic inductance to change direction [26]. For an otherwise ideal circuit considering the parasitic inductance, the optimal overlap where this occurs is [27]

$$\beta = \cos^{-1}\left(1 - \frac{i_{in}\omega L_p}{V_p}\right), \tag{15}$$

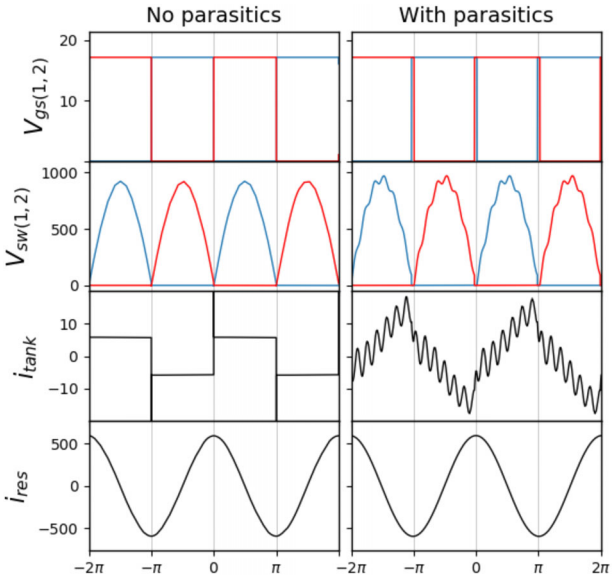

FIGURE 4 Simulations of the CSRI operating with a 2.5 MHz resonant tank with a $Q \approx 80$, $V_{in} = 300$, and ideal switches. (a) No switching device parasitics, with no overlap in the gate signals. (b) With constant $C_{gs} = 0.6$ nF and $L_p = 40$ nH, including overlap in the gate signals from Equation (15). A slight decrease in resonance frequency is observed due to absorption of C_{gs} into C_{tank}, and a parasitic capacitance current i_{react} resonating with L_p. The capacitive current magnitude is fixed, but the amplitude of the parasitic oscillations increases with any deviation from optimal operating conditions

where V_p is the peak value of the voltage across the resonant capacitor. A high Q-factor reduces the required amount of overlap for a given i_{res}, reducing the effect of the parasitic inductance in decreasing the power factor of the circuit, but for high frequency operation, it is generally preferred to minimize the the parasitic inductance [18]. The operation of the high-frequency CSRI is simulated in SPICE and is shown in Figure 4, where the high Q-factor and switching frequency results in a dramatic change in the input tank current waveform when considering realistic parasitic elements for a compact inverter-tank system. The resonant tank current and switch voltages for both cases can be estimated from 9 and 12, respectively. It is seen that by changing the switching frequency slightly and adjusting the duty cycle, the effect of the parasitic elements can be managed. Even so, careful attention must be paid to i_{react}, as on top of producing additional conduction losses, Figure 4 shows that the weakly damped parasitic resonance means that loss of zero voltage switching will introduce high amplitude ringing. The introduction of parasitic elements, inherent to any real system, can make the inverter stability very sensitive to correct frequency tuning, and the successful operation of the inverter thus requires precise timing of the gating signals.

3 | DESIGN OF INVERTER POWER MODULE

In order to test the feasibility of using higher voltage SiC MOSFETs in a CSRI topology for the targeted applications, a power

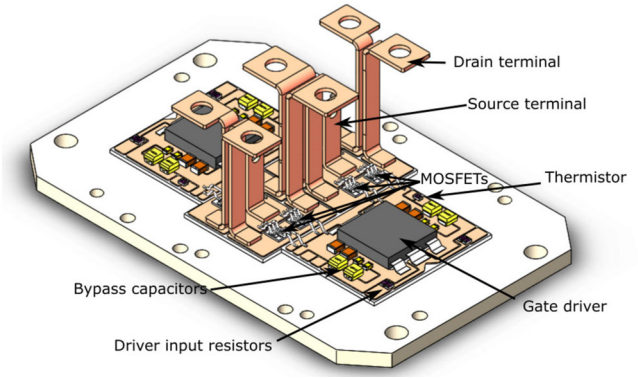

FIGURE 5 Design of the CSRI power module

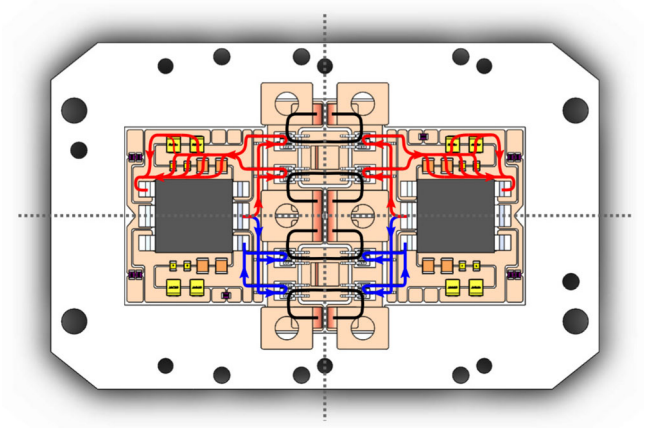

FIGURE 6 Top-down image of the designed power module. Red and blue lines mark the gate current for the MOSFETs when clamped to the positive and negative rails, respectively, while black lines mark the drain-drain current path. The gray dotted lines are symmetry lines

module was designed as shown in Figure 5 based on 1700V CPM2-1700-0080B MOSFETs [28]. To demonstrate a flexible module for a CSRI with the possibility of operating in the MHz regime without a transformer under a wide range of load conditions, the module is designed to have the capability of supplying 30 kW at full load. From the input voltage in Equation (12) and considering a switch voltage derating to 60% of V_{br}, each leg should have a peak current capability of around 100 A. This requires multiple paralleled devices to achieve with a reasonable margin for transistor losses, and thus four MOSFETs were connected in parallel for each switching leg. The parallelization of the MOSFETs in the designed module is thus aimed towards enabling the operation with highly varied loading conditions and power requirements.

Driving the MOSFETs with fast switching performance in the desired frequency range requires special attention to the gate drive circuitry, and it is common to utilize resonant gate drives to source and sink the large currents associated with charging the MOSFET gate [29, 30]. However, in the examined application with variable switching frequency, the resonant behavior can limit the operation frequency range. Additionally, the power loss reduction in the gate drive circuit by using a resonant structure is dwarfed by the copper losses incurred from the high resonant current in the tank. Thus, a conventional hard switched gate drive topology was chosen for flexibility, utilizing an IXRFD630 high current gate driver for each leg. This gate driver is specifically optimized for fast rise and fall times and low thermal impedance through its low inductive package with DBC substrate. The driver can source and sink large peak currents, which is necessary to drive the combined C_{iss} of 9 nF which is expected from the four SiC MOSFETs in each leg. To minimize the inductance in the gate switching loop, as well as to handle the power loss of the driver IC, the driver was mounted directly on a direct bonded copper (DBC) substrate, as was also done in [4, 31]. The CSRI topology is particularly well-suited for this approach since the switches in the CSRI are complimentary and have the same source potential, and thus require identical control and power supply circuits. To reduce the coupling to the power loop, an auxillary source connection was bonded directly to the V_{ss} of the driver.

The power MOSFETs, gate drivers, bypass capacitors, and auxillary components were mounted on a DBC substrate to allow a compact design taking advantage of the high thermal performance of the AlN ceramic [32]. The DBC is soldered to a copper baseplate to provide heat spreading and mechanical rigidity. A plastic housing with embedded pin headers is attached to the module to interface the gate drivers to the supply and measurement PCB.

Low power loop and reactive current loop inductances are advantageous to minimize the effect of power factor reduction and gate signal compensation. In addition, symmetry in the layout for the power loop for each MOSFET is important for balancing the losses and assuring that each switch has the same optimum driving point. These features were accomplished using interleaved symmetric drain terminals as shown in Figure 6. Symmetry of the gate current paths for each MOSFET is also important to ensure inductance balancing in the gate switching loop, and thus to achieve synchronization of the MOSFET gate voltages. These loops were therefore optimized to be very similar such that the paralleled MOSFETs switch as close to simultaneously as possible. Because four MOSFETs are driven in parallel the effective internal gate resistance is low, and because of the non-negligible gate loop inductance, some degree of underdamping in the driving loop is difficult to avoid without external gate resistance. However, to facilitate fast switching speed for this demonstration module, no external gate resistance was added. This is because the CSRI is inherently not as sensitive to shoot-through issues as voltage source topologies are, and thus some oscillation in gate voltage at turn-off can be accepted in exchange for fast switching capability.

While the presented gate driver integration is key for the handling of gate driver losses and inductance, the integration also implies some inherent capacitive coupling between the driver input and the high voltage copper planes [33]. The IXRFD630 supports an input voltage range from -5 V to $V_{cc} + 0.3$ V, so to avoid accidental false triggering of a turn-off signal, the high input signal to the driver is driven to 10 V through a 50 Ω

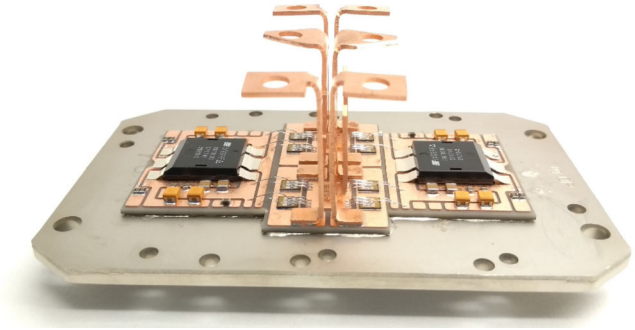

FIGURE 7 Photograph of the fabricated power module before encapsulation

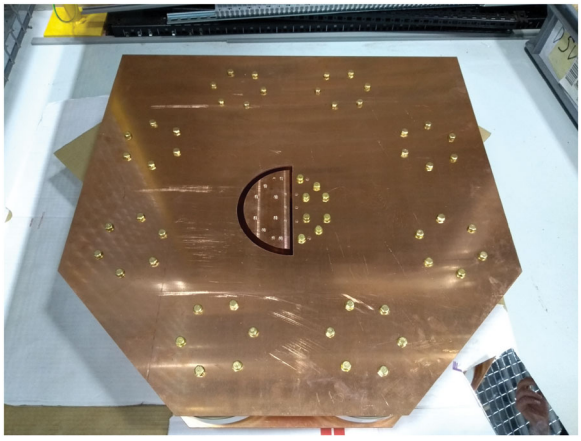

FIGURE 8 Photograph of the resonant capacitor bank with 8 capacitors in parallel for a total capacitance of 40 nF

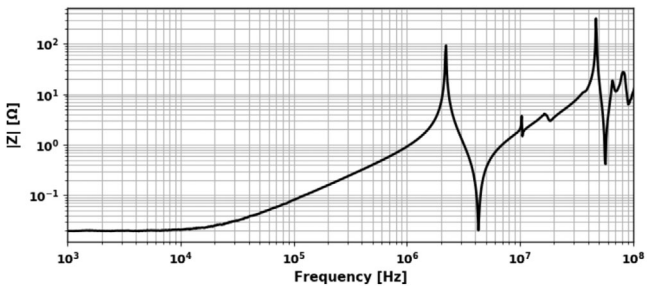

FIGURE 9 Measured impedance at the input to the resonant tank at the centre of the capacitor bank

resistor, significantly increasing the voltage margin to the input threshold V_{th} of around 3 V.

The fabricated power module is shown in Figure 7. After the module was tested for gate driver performance, it was finalized by encapsulating it in silicone gel to provide high voltage insulation [34].

4 | RESONANT TANK SYSTEM

Some of the most important parameters in many induction heating processes is the frequency of the coil current and the power delivered to the load. In addition, the physical structure of the coil itself may be highly important to get the desired heating pattern in the workpiece, which fixes the value of the inductance of the tank, as additional series inductance will lower the voltage of the coil terminals and thus the output power for a given workpiece. For the application considered here of high current single turn coils, which may have an inductance on the order of hundreds of nH, this means that a relatively large tank capacitance may be required to achieve the desired frequency and power delivered to the load.

In the case of low impedance workloads, the current in the resonant tank must be high to dissipate substantial power in the workpiece. Vacuum capacitors are attractive in this application, as they can carry hundreds of amperes and tolerate multiple kilovolts while maintaining very low ESR. However, the capacitance density of vacuum capacitors is limited, requiring special attention to the physical construction of the tank circuit to minimize the parasitic inductance, and if multiple capacitors are connected in parallel, to avoid inductance imbalance by conserving symmetry between the terminals of each capacitor. Thus, to minimize the generation of unwanted oscillations and ensure that the coil current is sinusoidal at the desired frequency, the tank must be constructed such that the circuit functionally matches Figure 2 and Equation (7) remains valid. For this reason, the 8 parallel capacitors in this setup are arranged in a circular pattern, as shown in Figure 8. The power module is connected on one side, while the flat single-turn inductor coil is connected to the other side.

The impedance magnitude plot for the constructed high current resonant tank is shown in Figure 9. Except for the unavoidable series resonance of the capacitors with their lead inductance at just above 4 MHz, a sharp and relatively featureless parallel resonance is observed around 2.2 MHz due to the circular symmetry. The coil current is thus expected to be nearly sinusoidal, irrespective of the shape of the input current waveform. From Figure 9, the Q-factor is estimated to be around 75 for the constructed resonant tank.

5 | EXPERIMENTAL RESULTS

As the final elements in the construction of the CSRI, in addition to the power inverter and the resonant tank, the two DC chokes were constructed using 15 winding EMS-0653327-060 powder cores, resulting in an inductance of around 49 μH and an input-output parasitic capacitance of 25 pF. To connect the power module to the resonant tank, a busbar made of a Mylar sheet with silicone adhesive is sandwiched between two copper plates, with a measured inductance of 12 nH and 320 pF parallel capacitance. The gating signals were supplied by a DE0-Nano-SoC FPGA board running a control algorithm providing adjustable duty cycle and output frequency.

The electrical tests were conducted using a Delta Elektronika SM 600-10 DC power supply. The tank voltage is measured using Teledyne Lecroy PPE4kV passive probes, and the gate voltage is measured with Teledyne Lecroy PP019 low voltage

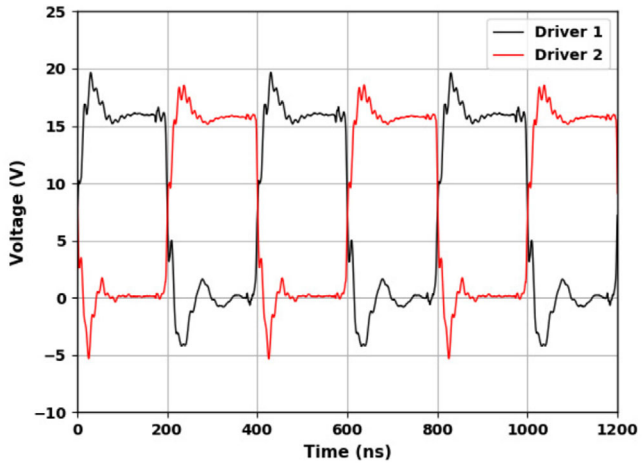

FIGURE 10 Gate driver output voltages measured at 2.5 MHz

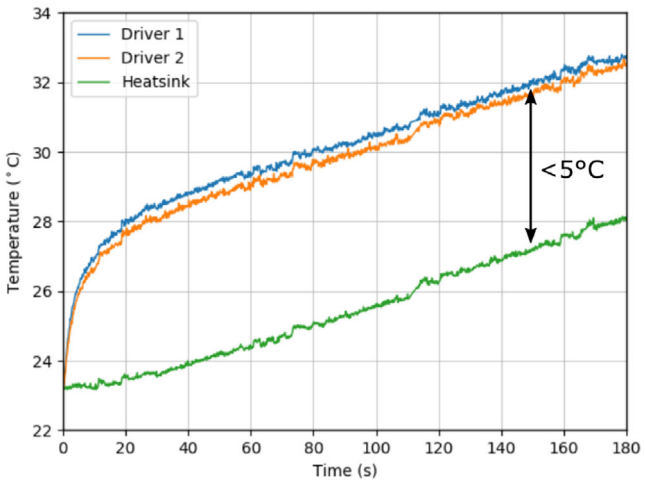

FIGURE 11 Temperature rise for the gate drivers and heat sink for 2.5 MHz operation measured with thermographic camera

probes. The tank input current is measured with a PEM CWT Rogowski current transducer.

The power losses in the active devices are an important metric for inverter performance. However, in this frequency range and considering high frequency ringings in the drain currents, electrical power loss measurements are difficult to assess. The inverter tests were performed on a tests bench with active water cooling for the power module, and thus the dissipated power in the inverter power module was estimated using calorimetric measurements on the water cooling supply for the heat sink.

5.1 | Gate driver circuit assessment

Driving four power MOSFETs in parallel from a single gate driver sets high demands for the driver IC, and it was investigated on the unencapsulated module whether the two complementary drivers are capable of switching the MOSFETs in the MHz regime. For this purpose, before connection to the resonant tank, the power module was mounted on a heatsink suitable for water cooling, and the temperature of the top of the driver ICs and the heat sink temperature was monitored with a FLIR E40 thermographic camera.

The output voltages of the gate drivers were supplied with +16 V for high output and 0 V for low output relative to the common source potential for each switch. 16 V high output is chosen to have large margin to the V_{gs} limit of the MOSFET, and although this is not ideal for optimizing the output characteristics, the datasheet for the MOSFET shows only a moderate difference in $R_{ds,on}$ compared to $V_{gs} = 20$ V. Operation at 2.5 MHz and 50% duty cycle is shown in Figure 10. Slightly underdamped behavior of the gate voltage is observed, with rise and fall times around 20 ns. It is seen that the output voltage of one driver is only slightly affected of the switching of the complimentary driver, which is important for switching stability.

The temperature of the drivers and the heat sink under these operating conditions is shown in Figure 11, where the DC power consumed by each driver is 14 W. The heat sink is not actively cooled during the test, and thus the slow linear temperature rise is due to heating of the heat sink which is not present during normal operation. The thermal performance is therefore demonstrated by the temperature difference between the driver surface and the heatsink, which reaches a steady value after an initial transient in Figure 11. The temperature difference between the drivers are within measurement tolerance, and the steady state temperature difference between the drivers and the heat sink is below 5°C, meaning that the thermal network of the driver is not a bottleneck for higher frequency or driving voltage swings than those used here. This demonstrates the ability of the integrated driver IC to drive the four paralleled 1700 V SiC MOSFETs in the MHz regime.

5.2 | Resonant operation

The unloaded operation tests were conducted under slow variation of the input power to showcase steady state resonant operation, with the CSRI operating at the resonant frequency shown in Figure 12 for $V_{DC} = 40$ V. The clean voltage waveforms indicate that soft-switching is achieved, with the tank input current clearly being primarily reactive. A ripple frequency of around 20 MHz is observed, close to the predicted resonance frequency of 18.5 MHz based on Equation (14), which is calculated by summing the total L_p from contributions of the busbar, power module, and resonant tank to an estimated 34 nH, and estimating a $C_{oss,eq} \approx 385$ pF for each MOSFET based on the data sheet at this operating point.

When the voltage across the resonant tank is increased to levels nearing the highest operating point of the transistors, the input current to the resonant tank in Figure 13 shows that complete soft switching is not achieved. As was argued in Section 2, achieving soft switching requires very finely tuned driving pulses. In the applied control scheme, there is a finite time resolution of the driving signals of 3.3 ns, and thus when the voltage is increased and the output capacitance of the MOSFETs decrease, the gradual change in resonance frequency can make

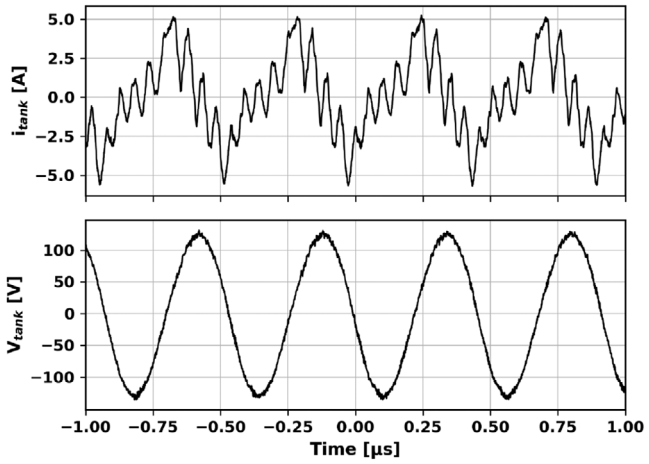

FIGURE 12 Tank voltage and output current of the transistors for a switching frequency of 2.17 MHz and DC voltage $V_{DC} = 40$ V

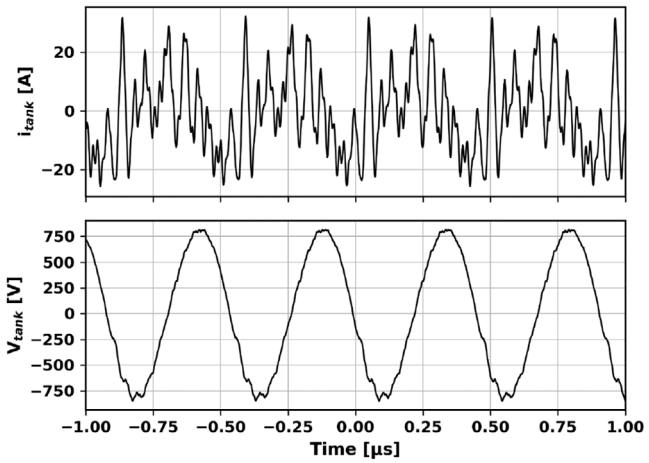

FIGURE 13 Tank voltage and output current of the transistors for a switching frequency of 2.19 MHz and DC voltage $V_{DC} = 280$ V

it difficult to switch precisely at the voltage zero crossings. The loss of soft switching results in large amplitude high frequency ringing that can interfere with the control circuitry and thus limits the operating voltage of the inverter, although the power dissipation in the module is well within the accepted range. Additionally, while the influence of the parasitic elements in general has a negative impact on the quality of the inverter output current, the loss of soft switching reduces this quality further, which can be an important consideration in applications requiring very clean resonant current waveforms. Re-introduction of the series diodes in the CSRI topology could relax the timing requirements in applications where robustness of the control is desired, at the expense of increased losses and component count [24, 27]. Alternatively, using a microcontroller with a high-resolution PWM architecture to create the driving signals, as done in, for example, [35] and [36], would likely also enable operation closer to the breakdown voltage of the switches. The tradeoff in this approach is that if the system is extended to closed loop control,

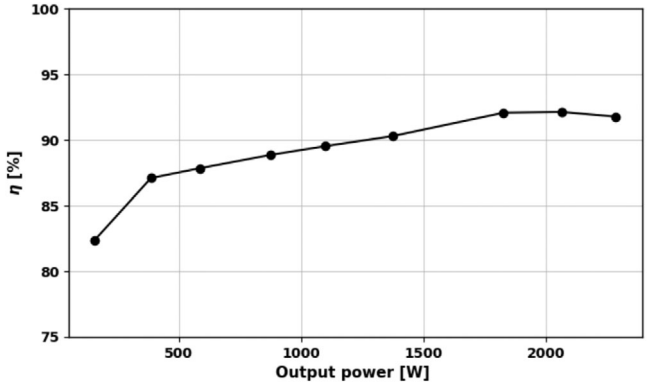

FIGURE 14 Calorimetric measurement of the efficiency of the CSRI power module at varying output power

the FPGA is not available for the implementation of a control algorithm with fast real time response.

For the power module efficiency calculation, it is assumed that the input chokes and cables contribute negligibly to the total losses due to the low input current. This allows the inverter efficiency is estimated as

$$\eta = \frac{P_{in} - P_{module}}{P_{in}} \cdot 100. \tag{16}$$

The efficiency is shown for various output power levels in Figure 14. The lower efficiency at low power levels is due to the power consumption of the gate drive circuits, while the drop at high power levels is explained by the gradual loss of soft switching. Still, even with the increase in the switching losses at higher voltage, efficiency above 90% is achieved. This efficiency is low compared to modern lower frequency induction heating systems [19, 21, 22], but is comparable to other SiC-based MHz inverter systems in the literature [6, 7]. As a large amount of the switch current in the presented measurements is reactive current that is present for any load condition, the efficiency of the inverter is expected to increase with increased loading. At this operating point, using the conservative estimate of the resonant current $i_{res} = C_{tank}\frac{\mathrm{d}V_{Ctank}}{dt}$, a reactive power of 170 kVA is oscillating in the tank circuit. These results showcase that proper design of the inverter system can allow a paralleled SiC MOSFET power module to efficiently drive a high power low impedance coil for MHz induction heating.

6 | CONCLUSION

In this paper, a prototype current source resonant inverter for variable frequency MHz induction heating was presented, and key considerations for the use of power devices with increasing blocking voltage in high frequency operation were discussed. A power module with paralleled 1700V MOSFETs and integrated gate drivers was fabricated, with the gate drivers able to switch the four paralleled MOSFETs at 2.5 MHz with a low temperature increase of 5°C. This demonstrates the viability of handling

both the thermal driver issues at high frequency and the low gate loop inductance requirements of paralleled SiC MOSFETs by using a hard-switching integrated gate driver structure. The power module was tested with an industrially relevant high-Q resonant tank, where switching at the resonant frequency provides clean voltage waveforms even under unloaded conditions, validating the applied approaches to paralleled SiC MOSFET power module design for the high frequency, high-Q inverter system. At higher voltage the inverter performance was limited due to the loss of soft switching, which was ascribed to the finite time resolution of the used driving circuit. Still, higher than 90% efficiency was achieved using the test setup at an output power of 2.3 kW in unloaded conditions, with calculated reactive power of 170 kVA. These results demonstrate the succesful application of a CSRI using paralleled 1700V MOSFETs in MHz operation, and are promising for the further expansion of the power range of MHz induction heating inverters.

ACKNOWLEDGEMENTS

This work was supported by the Innovation Fund Denmark.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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How to cite this article: Aunsborg, T.S., Duun, S.B., Munk-Nielsen, S., Uhrenfeldt, C.: Development of a current source resonant inverter for high current MHz induction heating. IET Power Electron. 15, 1–10 (2022). https://doi.org/10.1049/pel2.12204