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Utilizing Inverse Design to Create Plasmonic Waveguide Devices

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ABSTRACT

In modern communications networks, data is transmitted over long distances using optical fibers. At nodes in the network, the data is converted to an electrical signal to be processed, and then converted back into an optical signal to be sent over fiber optics. This process results in higher power consumption and adds to transmission time. However, by processing the data optically, we can begin to alleviate these issues and surpass systems which rely on electronics. One promising approach for this is plasmonic devices. Plasmonic waveguide devices have smaller footprints than silicon photonics for more compact photonic integrated circuits, although they suffer from typically having higher loss than silicon photonic devices. Inverse design software can be used to optimize the plasmonic device topology to maximize the device throughput, mitigating the inherent loss of plasmonics. Additionally, inverse design tools can help us make plasmonic devices with an even smaller footprint and higher efficiency than conventionally designed plasmonic devices. Recently, commercial inverse design tools have become available for popular photonic simulation software suites. Using these commercial inverse design tools with a compatible plasmonic architecture, we create compact, efficient, and manufacturable devices such as XOR gates, grating couplers, y-splitters, and waveguide crossings. We compare the inverse-designed devices to conventional devices to characterize the performance of the commercial inverse design tool.

Keywords: Nanophotonics, inverse design, FDTD simulation, plasmonics, surface plasmon polaritons, digital logic, optical logic, phase-shift keying

1. INTRODUCTION

Three-dimensional finite-difference time-domain (FDTD) simulations have become a very popular approach for designing nanophotonic devices. These tools are relatively fast, easy-to-use, and allow for fast iteration and robust exploration of the design space at low cost[1-5], making them accessible to photonics researchers and designers with a wide variety of backgrounds.

A popular method used with FDTD simulations to create plasmonic devices is inverse design. Inverse design is an optimization technique, typically using the adjoint method. Inverse design is powerful in many ways, from its relative speed to its abstract nature, removing the need for an exploration of the entire design space[6-11]. By defining a figure of merit (FOM) and allowing the tool to generate an optimized structure, the FOM is either maximized or minimized. Inverse design methods often result in a non-intuitive structure with better performance than their more conventional counterparts. We use Lumerical, a popular, commercially available FDTD software[12], combined with a python based inverse design tool called LumOpt, allowing us to run inverse design optimizations for photonic devices.

Leveraging Lumerical and the inverse design tool we generate compact plasmonic devices made from dielectric-loaded surface plasmon polariton (DLSPP) waveguides. For our XOR gate specifically, we use phase-encoded inputs to generate the logic-gate behavior. Phase-encoding the inputs proved to be a unique challenge as Lumerical is limited in its flexibility for certain tasks. However, we were able to work around the limitations of the software without the need to change the underlying code. After generating the device designs, we compare the performances of conventionally designed plasmonic devices to our own inverse designed devices.

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2. METHODS

2.1 Device Architecture

The plasmonic devices use a layer of silica on top of a silver layer surrounded by air, as depicted in figure 1. Silica waveguides help reduce the heavy loss exhibited by plasmonic devices, and silver helps reduce the cost of manufacturing the device, over other metals such as gold, while preserving the same device behavior. We chose this DLSPP device architecture because it stays within the constraints of Lumerical's inverse design tool and simplifies the complexity of the optimization. Figure 1 also shows the phase-encoded logic where a phase shift of 0 radians of a logic of 0 and a phase shift of π radians is a logic of 1. Finally, all our devices were designed to be operated at a wavelength of 1310nm.

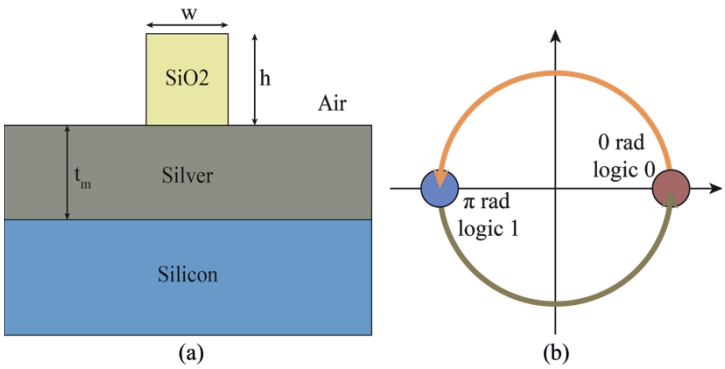

Fig. 1. (a) Cross section of the single-mode waveguide portion of the devices being simulated, where w = 400 nm, h = 440 nm, and tm = 500 nm. (b) Binary phase-shift keying diagram. A relative phase of 0 radians corresponds to a logic 0, and π radians corresponds to a logic 1.

2.2 Optimization Setup

When generating the inverse designs, we found that the optimization set up to achieve the best possible result was dependent on the device we were optimizing. For the XOR gate and the y-splitter, we found that running an initial 2D optimization of the device, then using the 2D device as a starting point for the 3D optimization, resulted in the most efficient 3D device. The grating coupler was optimized by using the conventional device as the starting point for the inverse design optimization. Finally, the waveguide crossing was generated by filling the optimization region halfway between the background and waveguide indices.

2.3 Circumventing Software and Resource Limitations

While Lumerical and LumOpt worked well with some of the devices, other devices, such as the XOR gate and grating coupler, required careful setup in order to be optimized. The XOR gate optimization problems were purely a result of software limitations. In Lumerical you can only use one input source for an optimization, so creating a two-input logic gate would causes some issues. To circumvent this, we created a symmetric or anti-symmetric coupled mode, depending on the desired input to the logic gate, and had the source span across both inputs. This allowed us to use the single source as both inputs to the XOR gate, as if it were two separate sources. In contrast, the grating coupler difficulties were a result of resource limitations. The grating coupler was the largest device we optimized, and due to the overall size of the optimization it was extremely computationally costly and time consuming. To alleviate this, we split the optimization into two steps: first we optimized the teeth regions of the grating, then we optimized the taper region. Doing this optimization in two steps allowed for a much faster optimization overall while still preserving the advantages of inverse design.

3. RESULTS

After running the optimizations, we obtain the topologies and power plots for the inverse designed devices as shown in figure 3, the conventional designed counterparts to the devices are shown in figure 2. We also characterize the results in table 1.

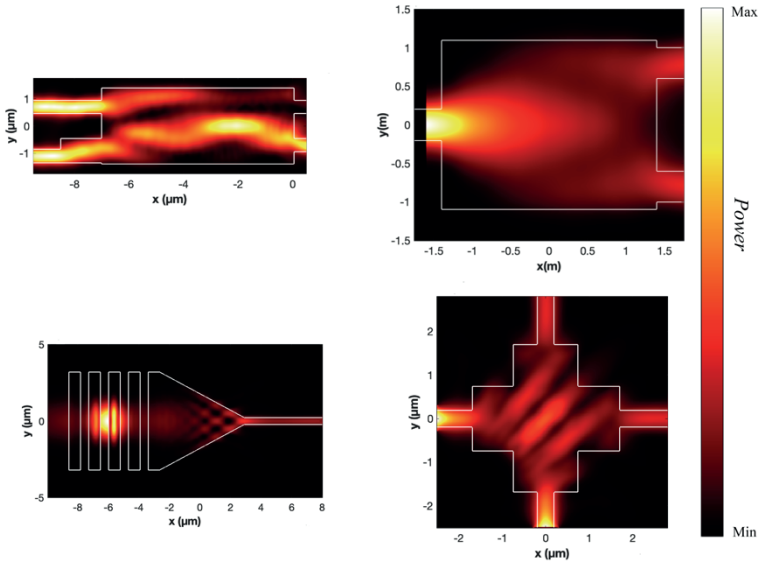

Fig 2. Simulation results for the conventional devices; device images are not to scale. The white outline shows the device topology. The plots show the optical power in each device: (top left) conventional XOR gate with both inputs in-phase, (top right) conventional Y-splitter, (bottom left) conventional grating coupler, (bottom right) conventional waveguide crossing.

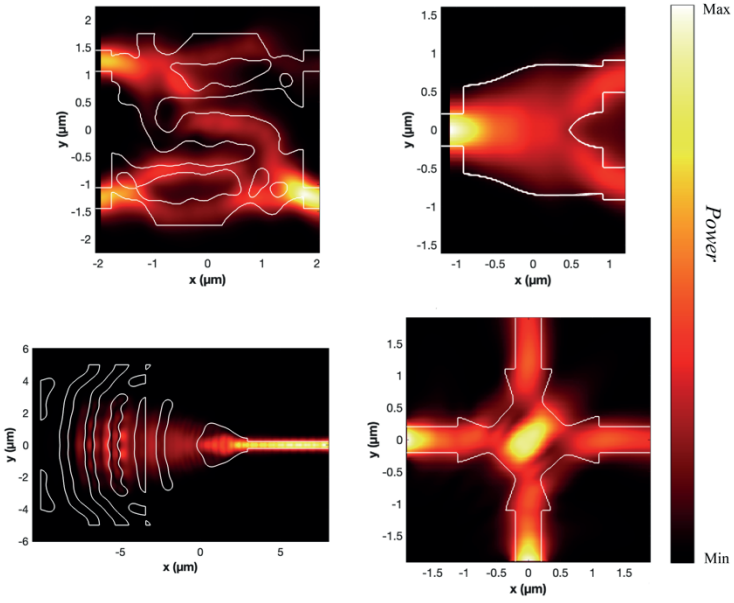

Fig 3. Simulation results for the inverse-design devices; device images are not to scale. The white outline shows the device topology. The plots show the optical power in each device: (top left) inverse-design XOR gate with both inputs in-phase, (top right) inverse-design Y-splitter, (bottom left) inverse-design grating coupler, (bottom right) inverse-design waveguide crossing.

Table 1. Insertion loss, area, and the performance metric for the conventional and inverse designed devices.

Device Design	Insertion Loss	Area	Performance Metric
XOR Gate			***Extinction Ratio***
Conventional	8.31 dB (XNOR) / 7.38 dB (XOR)	23.52 μm^2	8.12 dB (XNOR) / 8.49 dB (XOR)
Inverse	5.24 dB (XNOR) / 5.5 dB (XOR)	12.25 μm^2	6.34 dB (XNOR) / 7.28 dB (XOR)
Y-Splitter			***Splitting Ratio***
Conventional	1.32 dB	6.16 μm^2	50/50
Inverse	0.696 dB	3.96 μm^2	50/50
Grating Coupler			***Coupling Efficiency***
Conventional	17.35 dB	73.67 μm^2	1.84%
Inverse	8.94 dB	129 μm^2	12.78%
Waveguide Crossing			***Crosstalk***
Conventional	3.91 dB	11.56 μm^2	-11.8 dB
Inverse	3.70 dB	4.84 μm^2	-18.4 dB

We can see that, in general, all the of the inverse designed devices are better in some way. Specifically, for the XOR gate and the y-splitter, we were able to vastly reduce their overall footprint and reduce the loss as well. Thus, we can see that for all the devices the inverse designs are superior to the conventional devices across multiple metrics. In the future we will fabricate these devices for testing and validation of their functionality.

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