An Active Dead-Time Control Circuit With Timing Elements for a 45-V Input 1-MHz Half-Bridge Converter

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***Abstract*— In this study, a dead-time control circuit is proposed to generate independent delays for the high and low sides of half-bridge converter switches. In addition to greatly decreasing the losses of power converters, the proposed method mitigates the shoot-through current through the application of superimposed power switches. The circuit presented here comprises a switched capacitor architecture and is implemented in AMS 0.35 μm technology. In the implementation, the proposed dead-time control circuit occupies a silicon area of 70 μm × 180 μm. To realize the technique, a two-sided wide swing current source is employed. Each sides of the current source comes with two capacitors, two Schmitt triggers, and three transmission gates. Results show that the low and high sides of the projected half-bridge converter switches respectively require delays of 35 and 62 ns. The performance of the proposed dead-time circuit is evaluated by assembling it with the half-bridge converter. The proposed dead-time prototype achieves a 40% drop in power losses in the half-bridge circuit.**

***Index Terms*— Power management, half-bridge, switched capacitors, dead-time control circuit, power losses, power converters, shoot-through.**

I. Introduction

DIFFERENT applications require various types of power converters, including DC–DC boost/buck converters [1]–[3], class-D power amplifiers [4], half-bridge converters [5], and switched-capacitor circuits [6]. These converters are mainly applied to system basis chips in automation, including those used in airbag squib drivers, braking valve drivers, and power steering integrated circuits [7]–[10]. Power converters are also widely used in neural stimulation and wireless power transmission in implantable biomedical microsystems [11]–[14].

Dense and miniaturized power converters comprising small passive components are useful in high-frequency application, but the switching losses of power switches limit the operating frequency of these devices [15]–[17]. In addition to switching losses, power converters suffer from conduction and gate charge losses that affect their efficiency [18], [19]. Their safety also tends to be affected by power switches' false or immature ON-state [20]. These drawbacks are mainly attributed to the parasitic inductances and capacitances of power switches [21]. A half-bridge output stage is shown in Fig. 1 along with the equivalent circuit of a power switch with the associated parasitic inductance. The figure also demonstrates the power switch's input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}). These elements cause electromagnetic interferences and parasitic oscillations and are thus undesirable [22].

In implementing gate drivers, several techniques are used to accelerate the charge/discharge of unwanted elements of C_{iss} and C_{oss} and to mitigate the switching and gate charge losses of power switches. A soft-switching technique was proposed in [6], [23], [24] to reduce switching losses. The resonant gate driver approach is also widely used to reduce gate charge losses [25]. In [20], a specific double-pulse test was conducted to study the hard switching of power switches. Moreover, the high-voltage energy storing (HVES) approach was utilized to increase the gate driving speed [26]. In the HVES methodology, the authors aimed to decrease the adverse effects of parasitic gate loop inductance by embedding an on-chip resonant LC tank.

Standard high-voltage automotive data buses often require operating voltage from -27V to +45V to drive hydraulic actuators with power converters [27]. The power converters mainly operate with dead-time control circuits (DTCCs) [28]. These circuits have two main structures. Logic gates are sometimes used to create delays and thereby implement a dead-time between the activation of complementary conductive paths and avoid overlap [20], [29]–[31]. In other cases, time constants are used and implemented with resistors, capacitors, current

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sources, etc. [32]. The latter is preferred for high voltage applications that require long delays [33]. In the use of logic gates, a fixed circuit that is not changed during operation is typically implemented. In the use of time constants, the controlling signals and switching techniques should be regulated to control the current source and capacitors and thereby create the dead-time.

A set of two superimposed complementary power switches makes up a power converter [34]. Half-bridge converters, in particular, utilizes two superimposed complementary power switches as the output stage to drive a given load (Fig. 2(a)). Most of the power budget in a half-bridge circuit is consumed in the output stage, during which shoot-through and losses occur. Shoot-through arises when two power switches are inadvertently closed at the same time, thereby causing unnecessary power losses and potential damages [35]. Such phenomenon can be avoided by creating a dead-time interval between the control signals of power switches [36]. Figure 2(a) shows the circuit of a half-bridge convertor, including a dead-time part, gate driver, high-side power switch (HSPS), and low-side power switch (LSPS). Figure 2(b) shows that in the scenario in which one of the superimposed complementary switches is turned on before or while the other switch is turned off, a shoot-through current can flow from the supply rail to the ground during the overlap time interval. In this case, non-overlapping driving signals should be provided to the power switches via a DTCC [37].

Shoot-through may also result from ringing in the driving circuit; such phenomenon increases the gate-to-source voltage (V_{GS}) of the high-side switches above the threshold voltage (V_{TH}) of the power transistor (Fig. 2(c)) [38]. This issue is commonly observed in gallium nitride (GaN) high electron mobility transistors (HEMTs) because of their low V_{TH} ($\sim$1 V) [39] relative to other types of power switches, such as silicon carbide and conventional silicon (V_{TH} of $\sim$2.5 V) [40]. This property of GaN HEMTs is attributable to the output parasitic capacitance (C_{oss}) of the high-side power switch. GaN HEMTs are commonly applied to power converters because of their various advantages, including their low on-resistance and parasitic capacitance, high operating temperature, and small package size. Furthermore, small junction capacitance, lack of body diode, and no reverse recovery loss are three advantages of GaN transistors over Si or SiC MOS. While, in the Si or SiC MOS, in addition to reverse recovery, there is also forward bias losses (V_F) of the body diode.

As for the ringing effect in the driving circuit, the issue can be addressed by adjusting the damping ratio or by providing enough dead-time interval between the driving signals of complementary switches. The transient response of the main switching circuit can cause the formation of Miller capacitance at the gate of the low-side complementary switch. This condition results in the VGS of the switches to exceed V_{TH} (Fig. 2(d)). In this scenario, the switching frequency of the circuit should be fine-tuned to handle the high dv/dt and di/dt without exceeding V_{TH} [41]. Non-overlapping signal generators and dead-time controllers are therefore important in guaranteeing the safe and efficient operations in half-bridge circuit power converters. These solutions are effective in addressing shoot-through and ringing and can thus decrease losses.

The presented DTCC design enhances the performance of half-bridge power converters. It uses a two-sided wide swing current source, a switched capacitor structure, and a particular signaling technique to generate precise delays between the required non-overlapping gate driving signals, and accurately drive a half-bridge circuit and avoid losses or excessive power consumption due to shoot trough, etc. Compared to other dead-time circuit solutions, our DTCC circuit has the key advantage of generating two asymmetric delays, the operating parameters of which are independent of the half-bridge circuit parameters, for the high side and the low side of the converter. Additionally, the presented solution allows to generate required long delays between the high-side and low-side driving signals, which is highly desirable in high voltage applications. Such design reduces the imperfections in the entire signal propagation process in the half-bridge converter to achieve lower power consumption and better signal quality. In Section II, we describe the main idea and advantages of the proposed dead-time structure. The circuit implementation is also discussed. In Section III, we detail the experimental results. In Section IV, we summarize our conclusions.

II. Proposed Dead-Time Circuit

Cross-connected NAND/NOR gates and a chain of inverters in feedback loops are used in conventional dead-time circuits to generate non-overlapping signals with delays [41]. The propagation delay of these inverters provides the delays in the non-overlapping signals. This configuration of integrated circuits produces typical picosecond delays and is thus not useful in various power applications requiring long delays in the range of nanoseconds (e.g., high-voltage circuits, high currents, and highly reactive loads) [32].

A. Proposed Architecture

The proposed DTCC enables the generation of nanosecond delays and mitigates shoot-throughs at the same time. This property of the proposed DTCC decreases the power losses in power converters. Figure 3(a) shows the presented scheme. Specifically, the scheme comprises two-sided wide swing current sources (TS-WSCS) for linearly charging two capacitors (C_1 and C_2) on each side of the circuit. Each side of the circuit also has three switches for controlling the charging and discharging processes. Moreover, the right and left branches of the circuit are equipped with two Schmitt triggers (STs) with defined comparison hysteresis windows. These STs restrict the values of the generated delays between the two non-overlapping driving signals.

Figure 3 (b) shows the predefined state machine that reflects the originality of the proposed idea. Specifically, the figure illustrates the non-overlapping timing methodology for the low- and high sides of half-bridge converters. The states in this machine are change polarity “CP”, close switch “CS”, charge capacitors “CC”, and Schmitt trigger “ST”. The presented active dead-time circuit is controlled by a finite state machine

(FSM) to generate the required half-bridge control delays. The circuit operation based on the FSM is clarified according to Fig. 3 (b). The circuit operation is illustrated according to Fig. 3 (b). Given an operating high-side power switch (operating HS), the polarity of the signal at its output is supposed to change (CP HS) instantly when the deactivating signal arrives at its gate (deactivating HS). However, the process is time consuming because of the large parasitic capacitance of the HSPS. In meeting the required time, the Φ_2 signal should close the corresponding controlling switch before the LSPS is activated (CS LS). The TS-WSCS then charges the capacitor C_2 linearly (CC LS) to reach the upper bound of the utilized ST (ST LS). At this point, the HSPS is deactivated completely (deactivated HS). This process should generate t_{d2}. In Fig. 3 (b), the process is labeled as the "B" process. The activation of the LSPS (operating LS) is provided similar to "B" process which is named "A" process. This process should also generate the time required to completely deactivate the LSPS before the activation of the HSPS again. Figure 3 (c) presents the timing diagram, which includes four curves tagged by t_{d1}, t_{d2} and the different working states of the proposed DTCC [32].

The proposed DTCC approach offers the following benefits:

1- The amount of current delivered by the TS-WSCS, the values of the capacitors, and the comparison levels of STs determine the generated delay of the circuit. Adjusting these parameters thus helps obtain the long delays needed in high-voltage and power applications, including those requiring large parasitic capacitances (e.g., power switches).

2- To set the delays between non-overlapping signals independently, the proposed circuit generates different time delays t_{d1} and t_{d2}. Such capability facilitates the adjustment of the delays of the low- and high-side parts. In particular, the driving signals of the HSPS go through more stages (i.e., level shifter and gate driver) than those of the LSPS. Thus, ensuring the absence of any overlap between switch operations calls for a longer t_{d2} than t_{d1}.

3- The signals for arranging the capacitors and current source in the presented circuit are based on a predefined FSM. Specifically, this FSM is used to charge/discharge the capacitors and utilize/remove the current source and thereby produce a suitable dead time. This property reflects the originality of the presented circuit.

A gate driver with two independent inputs serves as the interface between the proposed DTCC and output stage of the half-bridge converter. This interface helps fulfill the practical operation of the proposed dead-time circuit for the half-bridge converter. Specifically, the gate driver receives non-overlapping signals from the proposed DTCC and then delivers them to the HSPS and LSPS. It also provides the power switches with an adequate amount of driving current from its supply.

B. Circuit Implementation

Our dead-time circuit prototype chip fulfills the R-L load requirements of a standard high-voltage data bus [27], having V_{IN} =45V and driving a R-L load of R=100 Ω and L=150 μH with a half-bridge converter. The presented dead-time circuit prototype can provide high-side and low-side delays of 35 ns and 62 ns to such a half-bridge converter. The transistor-level implementation of the proposed DTCC is shown in Fig. 4 (a). The TS-WSCS supplies the charging current of capacitors C_1 and C_2. The sources are formed by nine MOSFETs (MP1–MP7 and MN1, MN2). MN1 and MN2 are two diode connected transistors that serve as current sources for respectively generating I_{in} and I_{bias}. MP1, MP2, and MP3 are used to bias the cascaded transistors MP4, MP5, MP6, and MP7. The following design strategies are considered to ensure that the TS-WSCS circuit functions:

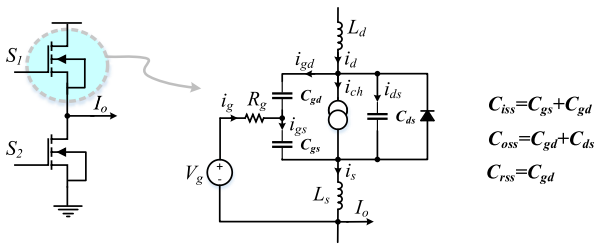

Fig. 1. Half-bridge output stage and equivalent circuit of power switch during operation.

TABLE I
ASPECT RATIOS OF TS-WSCS TRANSISTORS

	MP1, MP2	MP3	MP4 - MP7	MN1, MN2
W (μm)	10	5	10	0.4
L (μm)	0.35	0.35	0.35	5

1) Currents I_{bias} and I_{in} are set to be equal for MP1–MP7 to be in their saturation region.
2) The width of MP3 is set to half of that of MP1, MP2, and MP4–MP7. The setting should bias MP1, MP4, and MP6 properly in the active region.
3) Minimum gate lengths are adopted for MP1, MP4, and MP6 to maximize the frequency response.

The aspect ratios of the transistors used for the TS-WSCS are listed in Table I. A ramp signal is generated using the timing elements MN3–MN8 (i.e., transmission gates), C_1–C_2, and control signals ($\Phi_1 - \Phi_2$). Driven by Φ_1 and Φ_2, MN3–MN8 are utilized to linearly regulate the charging and discharging times of C_1 and C_2. The TS-WSCS circuit can be quickly turned on and off. Therefore, a 0.6 V offset resulting from the residual charges (Fig. 4 (a)) in C_1 and C_2 after one transition is added to the generated ramp signal at nodes 1 and 2 (Fig. 4 (a)). In this case, MN3 and MN6 are added to remove the residual charge and cancel the generated offset. The addition is possible if MN3 and MN6 are activated in phase with MN5 and MN8, respectively. The required delays are generated using two STs. In setting the STs' hysteresis windows, their reference voltages are adjusted to $V_{ref1} = 0.76$ V and $V_{ref2} = 1.74$ V. Following the adjustment, the STs can then generate a non-overlapping signal that provides enough dead-time to avoid shoot-throughs in the converter resulting from the ramp signals generated across the

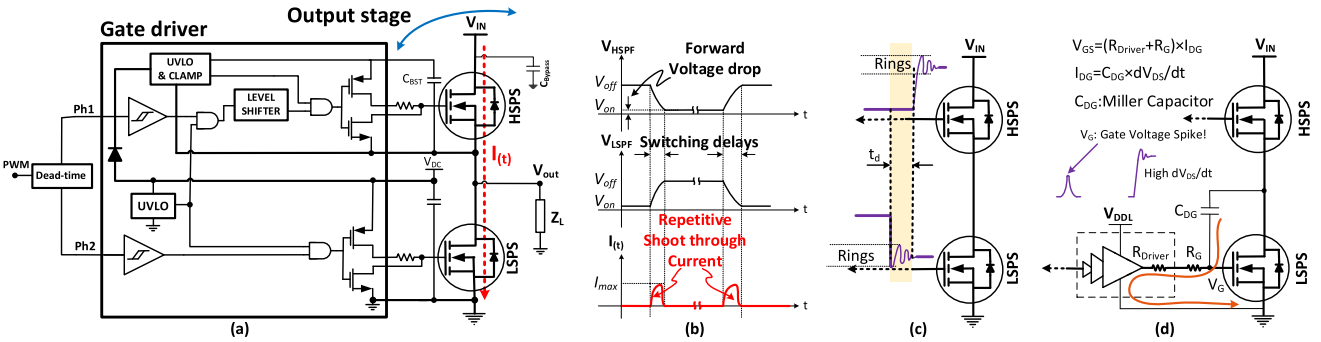

Fig. 2. Power converter and the different sources of shoot-through: (a) half-bridge circuit with simplified dead-time circuit, (b) impact of switching delays, (c) ringing effect due to the output parasitic capacitance (C_{oss}) of HSPS, and (d) Miller capacitor effect.

capacitors C_1 and C_2. Fig. 4 (a) shows that the ST circuits are surrounded by two boxes. Fig. 4 (b) illustrates the effect of the offset added to the ramp signals of node 1 with and without the addition of MN3 and MN6. The slope of the ramp signals decreases because of the added offset without the use of MN3 and MN6. The generated delay is thus 5 ns longer than expected.

The following equations are arranged to show the relation between the generated delays (t_{d1} and t_{d2}) and the circuit parameters. The equation for the capacitor is

$$i_c(t) = C\cdot\frac{dV_c(t)}{dt}, (t_0 \le t \le t_1) => \quad (1a)$$

$$i_c(t)\cdot dt = C\cdot dV_c(t), (V_0 < V_c(t) < V_1) \quad (1b)$$

Constant current is delivered to the capacitors. Hence, the following equation is obtained through the integration from t_0 to t_1 and from V_0 to V_1, with the upper and lower bounds of the integrals being ST reference voltages and their corresponding start and stop times:

$$\int_{t_0}^{t_1} i_c(t)\cdot dt = C\cdot\int_{V_0}^{V_1} dV_c(t) => \quad (2a)$$

$$I\times[t_1 - t_0] = C\times[V_C(t_1) - V_C(t_0)] => \quad (2b)$$

$$I\times[t_1 - t_0] = C\times[V_1 - V_0], \quad (2c)$$

where $V_C(t_0) = V_0 = 0$ as the capacitors are reset after each period and $t_0 = 0$ is the time at which the capacitors start charging at the beginning of each period. Assume that t_1 is the time at which the ramp signal (ramp = k·t, where k = I/C and "t" is the time) reaches the high level of the ST window. In this case, t_{d1} and t_{d2} can be expressed as

$$t_{d1} = (C_1/I_{C_1})\times V_{ref2}, \quad (3a)$$

$$t_{d2} = (C_2/I_{C2})\times V_{ref2}, \quad (3b)$$

where V_{ref2} is the trigger voltage of the STs located on each side of the TS-WSCS. The generated delays in the proposed DTCC rely on the values of the I_{C1} and I_{C2} currents (Fig. 4 (a)) that the TS-WSCS delivers to the capacitors. Given the relation between the output current and the values of I_{in} and I_{bias}, the operation of the proposed design against mismatch and process corners should be validated. Specifically, MN1 and MN2 (Fig. 4 (a)) that are used to adjust the biasing current should be made robust against process variations. The

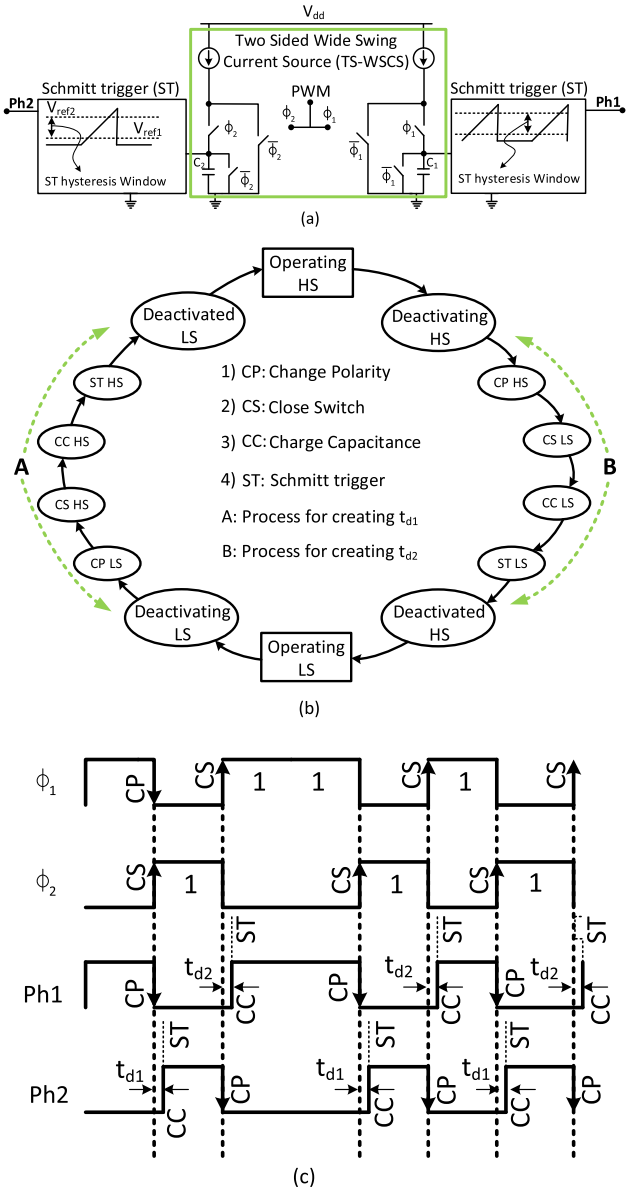

Fig. 3. Proposed dead-time control circuit: (a) simplified schematic, (b) state machine representation, and (c) timing diagram.

operations on both sides of the proposed DTCC during the generation of t_{d1} and t_{d2} are the same. A different t_d is due to the different parameter values on each side of the circuit. Therefore, the circuit is evaluated to be robust against process

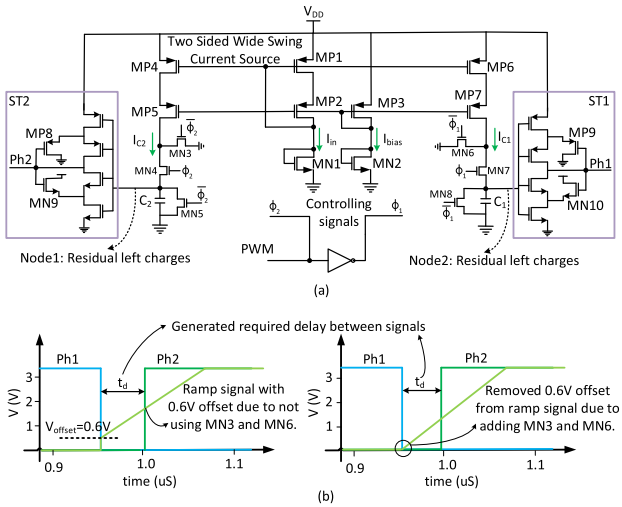

Fig. 4. (a) Transistor-level implementation of proposed DTCC, (b) added offset to the ramp signal with and without MN3 and MN6.

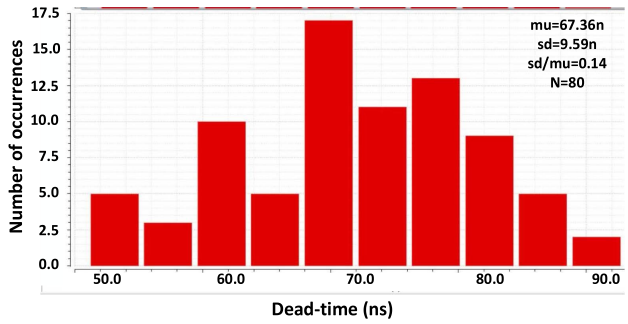

Fig. 5. Evaluation of DTCC operation with a Monte-Carlo simulation.

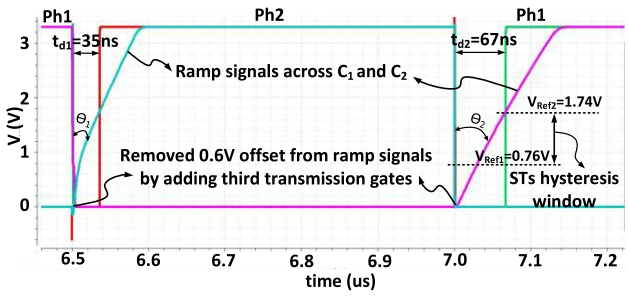

Fig. 6. Simulated dead time between signals.

variations for one of the delays (i.e., t_{d2}). For the designed circuit of the typical case corner, i.e., typical NMOS and PMOS transistors and $V_{DD} = 3.3$V, the simulated dead-time value t_{d2} is 67 ns. A worst-case scenario is simulated to cope with process variations. In the AMS kit, "fast NMOS/fast PMOS" corresponds to "worst power" (WP) while "slow NMOS/slow PMOS" corresponds to "worst speed" (WS). In this study, we evaluate the operation of the proposed circuit in the WP and WS cases. The WP and WS cause process variations and are thus the worst conditions of component operations. The simulated dead-time values t_{d2} for the WP and WS cases are 50.0 and 90.0 ns, respectively. Obviously,

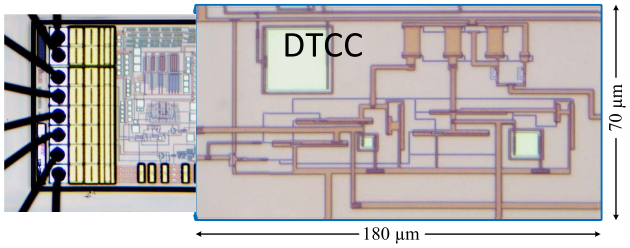

Fig. 7. Chip micrograph of fabricated DTCC in CMOS AMS 0.35 μm.

the WS case yields the longest dead-time while the WP has the shortest dead-time. In this work, the impact of the process variations on the performance of the proposed DTCC is studied using a Monte Carlo simulation. A supply voltage of $V_{DD} = 3.3$ V is set for the simulation. The results for t_{d2} are shown in Fig. 5. Specifically, the simulated t_{d2} shows a log-normal distribution with a variance of 0.14. The *average delay* of t_{d2} is 67.36 ns, and the standard deviation is 9.59 ns. This work aims for a robust design against process variations with the lowest standard deviation. Therefore, the dimensions of MN1 and MN2, which are responsible for biasing the circuit, should be increased. At the same time, the same aspect ratio "W/L" should be maintained. However, both tasks lead to a trade-off between the chip area and the sensitivity of the generated delay to process variations.

The impact of the parasitic inductance on the produced dead-time delays is examined through post-layout simulations. The relevant voltages, including the non-overlapping signals (Ph1, Ph2), and the ramp signal across capacitors (C_1 and C_2) are shown in Fig. 6. The figure also presents the parameters of $t_{d1} = 35$ ns, $t_{d2} = 67$ ns, $V_{ref2} = 1.74$ V, and $V_{ref1} = 0.76$ V. After the addition of the MN3 and MN6 transmission gates at high and low STs, the 0.6 V offset is effectively removed from the ramp signal. As observed in Fig. 6, the generated delays between the non-overlapping signals rely mainly on the slope of the ramp signals. Moreover, the hysteresis windows of the STs differ (as the capacitance of C_2 is relatively large, the slope of the ramp signals is slow). Therefore, the upper bound of the level shifter (V_{ref2}) on the corresponding side of C_2 meets the ramp signals later. The generated t_{d2} is thus longer than t_{d1}. The delays in the design could be set in other ways. For example, the amount of the current delivered to the capacitors can be set. Another option is to set the STs' hysteresis window parameters by the upper and lower bounds on the basis of the sizes of MP8, MP9, MN9, and MN10 in the design (Fig. 4 (a)).

In Fig. 6, Θ_1 and Θ_2 respectively denote the angles between the generated ramp signals and the falling edges of the non-overlapping signals. A ramp signal with a sharp slope yields a small angle. A small angle in this case results in a short dead-time because the ramp signal produced meets V_{ref2} of the corresponding ST early. At this point, the proposed DTCC is implemented to produce fixed t_{d1} and t_{d2} for a specific power converter. In the post-layout simulation, the proposed DTCC without PADs consumes 190 μW of power under no load conditions.

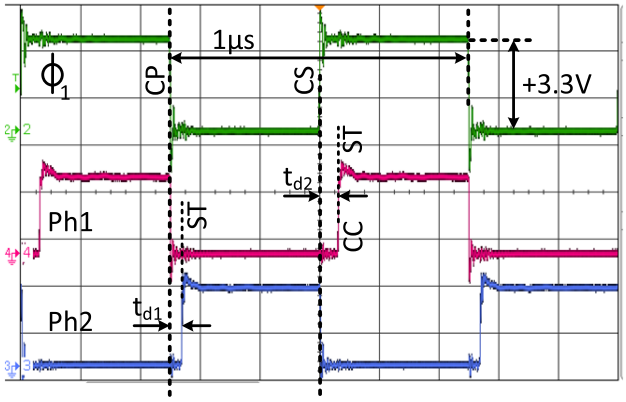

Fig. 8. Measured generated dead-time delays between non-overlapping signals.

III. Measured Performance

We fabricate the proposed DTCC in AMS 0.35 μm CMOS. The micrograph of the integrated chip prototype is shown in Fig. 7. The proposed circuit occupies an area of 180 μm $\times$ 70 μm. The integrated DTCC is designed to generate t_{d1} = 35 ns and t_{d2} = 62 ns for the LSPS and HSPS, respectively, by using C_1 = 30fF and C_2 = 55fF. The lower and upper bounds for both STs on each side are 0.76 and 1.74 V, respectively. The delays meet the requirements of a projected power converter. The dead-time required by a power converter is contingent on the supply voltage (V_{IN}) and the current delivered to the load [3].

A. Results of DTCC Measurement

The measured non-overlapping signals produced by the DTCC prototype for a 1 MHz input square wave signal (Φ_1) and a supply voltage of 3.3 V are shown in Fig. 8. The figure also presents the four states (i.e., CP, ST, CS, and CC), delays (i.e., t_{d1} and t_{d2}), and signals (i.e., Ph1 and Ph2). A good agreement is reached between the experimental results and the projected timing diagram (Fig. 3 (c)). Moreover, the measured results agree well with the post-layout simulation results (Fig. 9 (a)). The measured and simulated delays with a precision of 0.01% and a supply voltage of 3.3 V are equal to t_{d1} = 35 ns for C_1 = 30fF. However, the measured results (62 ns) and simulated results (67 ns) present a difference in t_{d2} values for C_2 = 55fF. The results are presented in Fig. 9 (a). An increase in the supply voltage (V_{DD}) causes a decrease in the generated dead-time between the non-overlapping signals according to a second-order function. In particular, the second-order effect is more distinct in the measurement than in the simulation (Fig. 9 (a)). An increase in V_{DD} boosts the V_{SG} values of MP1, MP4, and MP6 (Fig. 4 (a)). Moreover, the second-order function relates to the V_{SG} values of the MOSFETs biased in the saturation region and their drain current charge the capacitors C_1 and C_2. As presented in Equation (3), the I_{C1} and I_{C2} currents delivered to the capacitors are inversely related to the amount of generated dead-time (i.e., a large charging current results in a steep ramp signal, which in turn produces a short dead-time). Therefore, the generated dead-time is associated with V_{DD} by a second-order descending curve. This work experimentally validates the operation of the proposed DTCC.

The validation is performed at different supply voltages (V_{DD}), over a frequency range of 10Hz-11MHz, and square input signals. Herein, t_{d1} and t_{d2} determine the frequency limitation (11 MHz) at different V_{DD}. The delays produced by the non-overlapping control signals are independent of the input signal frequency. Therefore, the frequency of the input signal can be increased up to $f_p \leq 1/(t_{d1} + t_{d2})$. Such a condition represents the extreme case in the proposed design. The effect of changes in V_{DD} on the maximum operating frequency is illustrated in Fig. 9 (b). The limitation is observed to only affect Ph2 of the non-overlapping signals generated. This result is due to the fact that an increase in frequency with a specific value of V_{DD} causes the values oft_{d1} and t_{d2} to be close. Therefore, Ph2 disappears while Ph1 is available. As mentioned previously, dead-time delay drops when V_{DD} increases. A reduced dead-time delay in turn increases the maximum operating frequency (Fig. 9 (b)).

The amplitudes of the undershoot and the overshoot ringing near the edge of the measured signals are -1.9 and $+1.1$ V, respectively (Fig. 10). In Fig. 10 (a), the red and blue curves mark Ph1 and Ph2, respectively. Ph1 reaches a high state when the ringing of its complimentary signal Ph2 becomes totally damped. The results reveal slight variations in the ringing observed in the non-overlapping parts of control signals which are provided for the gates of the HSPS and LSPS, respectively. The differences may be explained as follows: avoiding any overlap between the on-states of the superimposed complimentary switches of the power converter requires the generation of adequate dead-time (t_d) between the control signals. Figures 10 (a) and (b) respectively present the measured t_{d2} (62 ns) and t_{d1}(35 ns).

In Fig. 11, the measured power consumption of the proposed DTCC is shown as a function of the input frequency for different values of V_{DD}. The power indicated refers to static and dynamic power. Dynamic power is consumed by the charge and discharge of the capacitive load in the outputs of Ph1 and Ph2 of the fabricated chip connected to the half-bridge converter. Additional losses may also be incurred in the active PADs because of the internal CMOS stages used to buffer the I/O signals.

The capacitive load is estimated by measuring the slew rate of the non-overlapping signals generated when the DTCC is connected to the half-bridge converter, that is, $C_L = i_{dynamic}/(\text{slew rate})$. The slew rate is equal to 0.16 V/ns when the signals at the output of the DTCC range from 0.5 V to 3.0 V; the corresponding dynamic current is 2.5 mA. The circuit has two outputs, namely, Ph1 and Ph2. Dynamic current is consumed to drive the capacitive loads at the outputs of Ph1 and Ph2. Therefore, the total capacitive load of the DTCC is $C_{Lph1} + C_{Lph2} = 2.5\text{mA}/(0.16 \times 10^9) = 15.62\text{pF}$. Given the inputs of the gate driver having the same circuit, the capacitive load at each output is $C_{Lph1} = C_{Lph2} = 7.81\text{pF}$.

As shown in Fig. 11, the power consumption varies with frequency. This relationship is attributed to the switching losses of the MOSFETs that increase almost linearly with

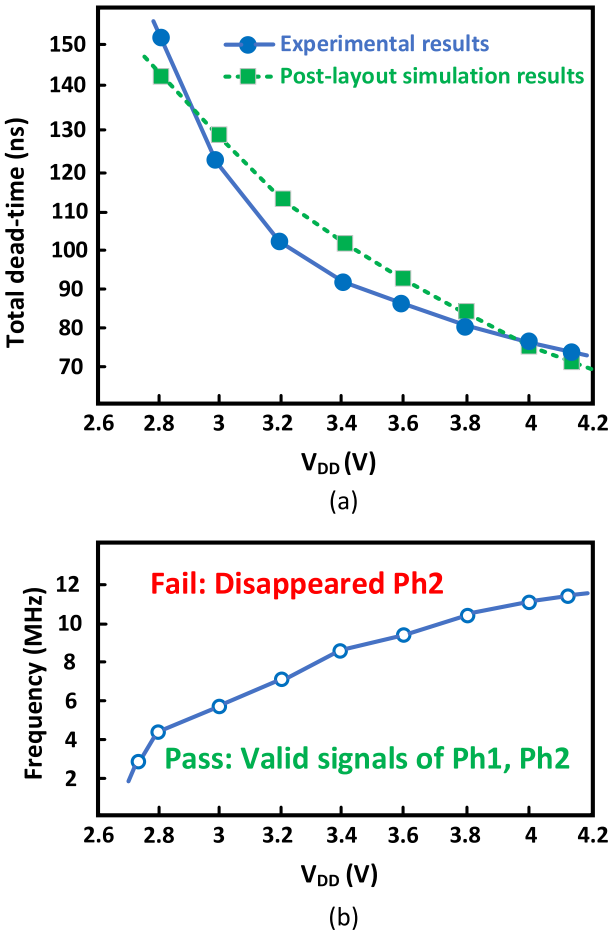

Fig. 9. Measured DTCC performances: (a) Comparison of the experimental and post-layout simulation results of the dead-time delays variation versus the power supply voltage V_{DD}. (b) The effect of V_{DD} on the maximum operating frequency of DTCC.

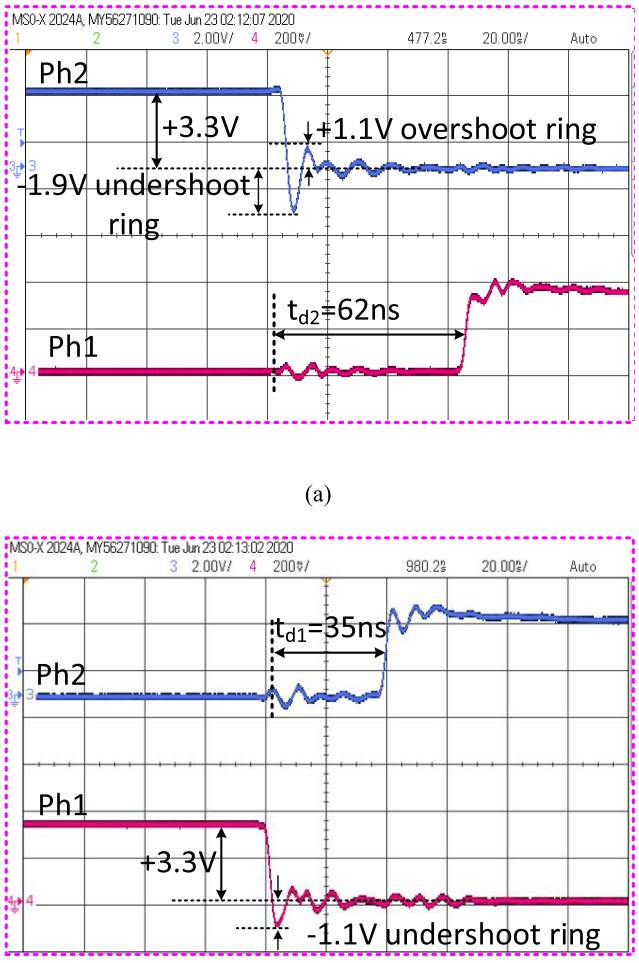

Fig. 10. Measured outputs of Ph1 and Ph2: (a) generated delay t_{d2} for the high side of half-bridge converter, (b) produced delay t_{d1} for the low side of half-bridge converter, and the amplitude of individual ringing at the edges of each phase.

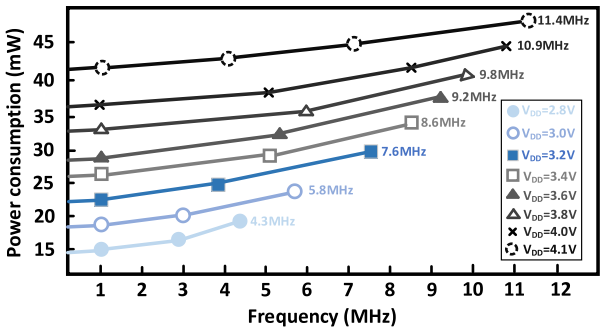

Fig. 11. Measured power consumption variation with respect to the input frequency for different values of V_{DD} for 7.81pF estimated capacitive load in each output of Ph1 and Ph2.

the operating frequency. In the proposed DTCC, the output currents I_{C1} and I_{C2} increase with V_{DD}. The same is true for the power consumption. Figure 11 also presents the variations of power consumption with the operating frequency given eight specific V_{DD} values. The maximum frequency of the circuit changes in line with V_{DD}. As the generated dead-time decreases with V_{DD}, the upper curve ($V_{DD} = 4.1$ V) achieves the highest maximum frequency with 11.4 MHz. As the frequency of the non-overlapping signal further increases and exceeds $1/(t_{d1}+t_{d2})$, Ph2 drops and then disappears completely. For a valid non-overlapping signal, the power consumption varies from 16.8 mW to 41 mW on the basis of V_{DD}, which can vary from 2.8 V to 4.1 V, and the operating frequency, which ranges from 100 kHz to 11.4 MHz.

B. Validation With Half-Bridge Circuit

The DTCC prototype is validated by implementing a half-bridge circuit with commercial components. The block diagram of the implemented half-bridge circuit with the fabricated DTCC is illustrated in Fig. 12. The eGaN HEMTs are driven by the LM5113 gate driver (Fig. 12). The power eGaN FET can work at voltages of up to 100 V and deliver currents as high as 5 A to the load. Two independent high-side and low-side TTL logic inputs comprise the gate driver. These inputs are compatible with the fabricated DTCC chip. The LM5113 contains the required bootstrap (BST) diode. The commercial regulator MCP1703 supplies the gate driver with

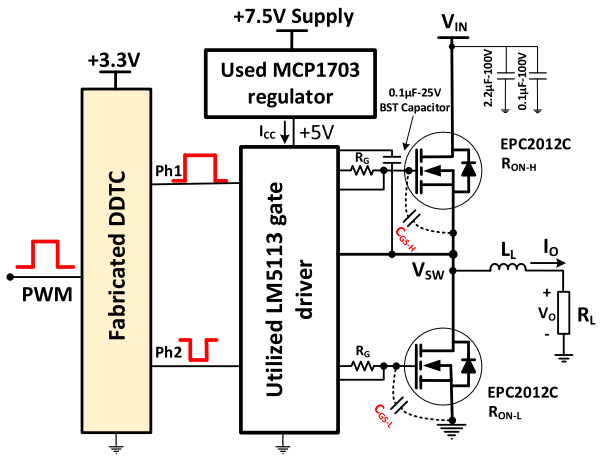

Fig. 12. Block diagram of the test half-bridge circuit with the fabricated DTCC.

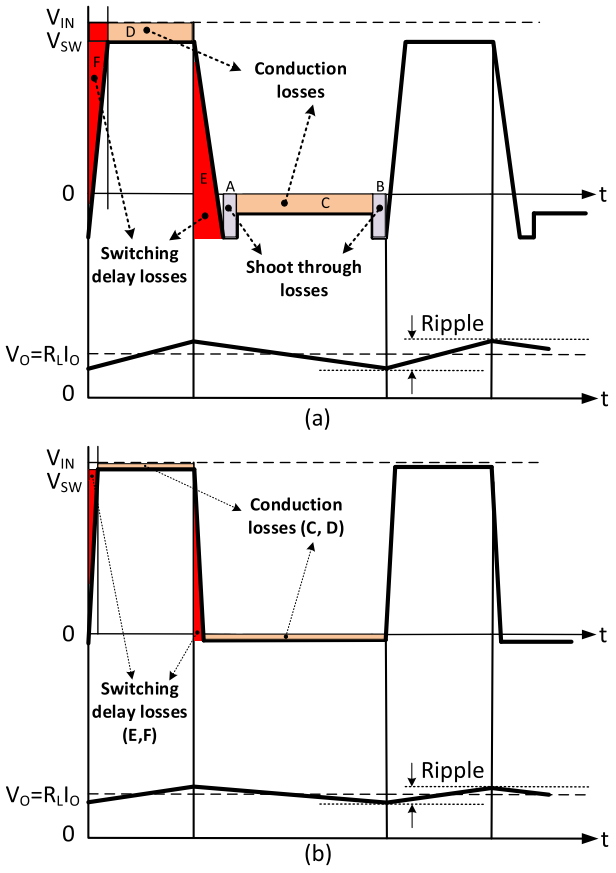

Fig. 13. Relevant waveforms of half-bridge circuit (a) with inconvenient amount of dead-time, showing the dead-time dependent losses of A, B, C, D, E, and F; and (b) with a convenient amount of dead-time, showing a significant dead-time dependent loss reduction.

5 V (Fig. 12). For the output stage of the half-bridge circuit, we utilize two eGaN HEMTs from EPC (EPC2012C), two freewheeling diodes (SDM03U40-7) placed in parallel with each power switch to reduce spikes in the inductive load, and a BST capacitor (C1005 × 5.1E104K050BC). The BST capacitor provides the gate charge for the HSPS, dc bias

TABLE II
PERFORMANCE COMPARISON WITH PRIOR WORKS

	[42]	[48]	[51]	[52]	This work
Results	Meas.	Meas.	Meas.	Meas.	**Meas.**
Tech.(nm)	180	65	350	350	**350**
f_p (MHz)	10	10	10	0.1	**1**
t_d (ns)	0.125	1	Analog	200	**35 and 62**
I_O (mA)	200	120	600	500	**210**
V_{IN} (V)	12	5	3.6	250	**45**
ΔP_{loss}(%)	30.5	--	--	--	**32**
Effic.	81.2%	76.4%	--	77%@20W	**82%**

power for the half-bridge under-voltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The minimum on-time of low-side transistor affects the value of the bootstrap capacitor; a value of over 0.1 μF is deemed satisfactory. Any power supply noise is removed by connecting two bypass capacitors in parallel between the input voltage (V_{IN}) and GND [41], [42].

The basic operations of the half-bridge circuit with inconvenient and convenient dead-time are respectively shown in Figs. 13 (a) and (b). Regardless of the operation, three critical power losses heat up the power switches and substantially affect the safety of the power converter. These power losses depend on the overlap between the activation of the power switches. Hence, they can be minimized using a convenient DTCC. The dead-time dependent power losses (DDPLs) include conduction loss, switching delay loss, and shoot-through loss. These DDPLs are illustrated in Fig. 13 (a) with different colors and names (A, B, C, D, E, and F) [43]–[45]. Given a convenient amount of dead-time, losses A and B in the half-bridge circuit are totally eliminated, and the volumes of C–F are greatly minimized (Fig. 13(b)).

C. Power Loss Analysis

The total power losses in the designed power converter should be calculated on the basis of the measured parameters from the implemented converter [46], [47] to identify the effects of the proposed DTCC on the implemented half-bridge circuit.

The first DDPL is the conduction loss (Fig. 13). The conduction loss of the HSPS (P_{ON-H}) depends on the switch's on-resistance (R_{ON-H}) and the amount of current delivered to the load during the operation. The same description applies to the LSPS, that is, P_{ON-L} depends on R_{ON-L}. The second DDPL is the switching loss. The switching loss is due to the rise and fall times of the switching voltage V_{SW} (Fig. 13). The switching loss of the HSPS (P_{SW-H}) depends on the operating frequency of the power converter. It also relies on V_{IN} and I_O [32]. The third DDPL is the body diode loss (P_D), particularly in the Si or SiC MOSFETs. It is mainly caused by the reverse recovery of the inductor current (L_L current) by the body diode of the LSPS. P_D depends on the operating frequency of the converter and the forward voltage (V_D) of the LSPS' body diode [46]. For a half-bridge circuit, the gate charge loss (P_G) results from the gate charging of the power switches, and the gate driver loss is caused by gate charging

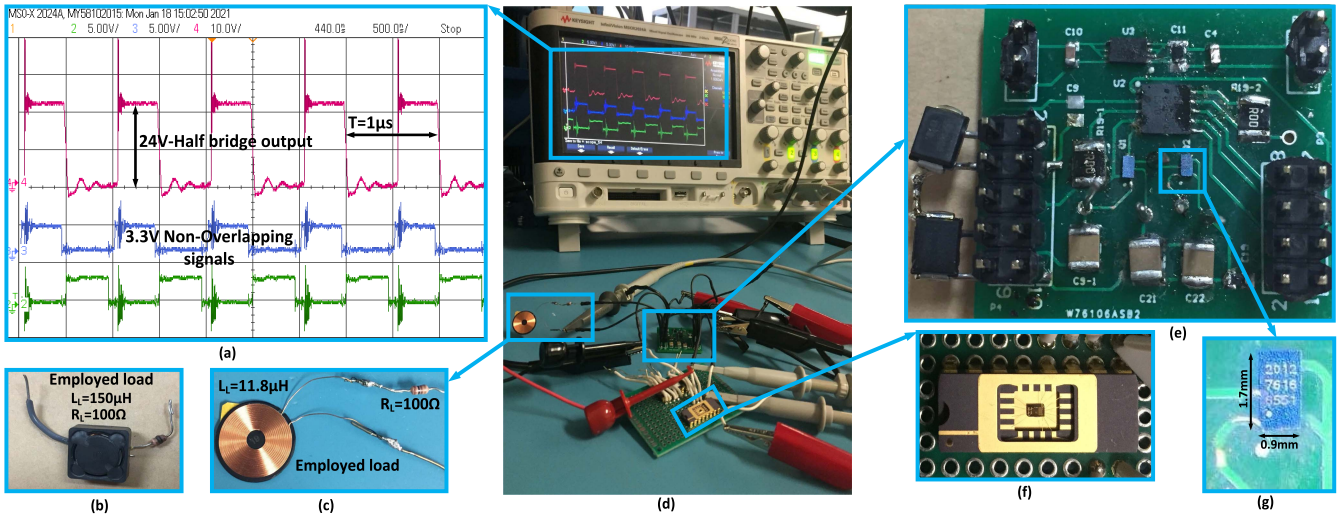

Fig. 14. Experimental setup of the half-bridge circuit. (a) Measured signals. (b) RL load with R = 100-Ω and L = 150-µH load. (c) RL load with R = 100-Ω and L = 11.8-µH load. (d) Test bench. (e) Custom printed circuit board. (f) Packaged fabricated chip. (g) Power GaN transistor.

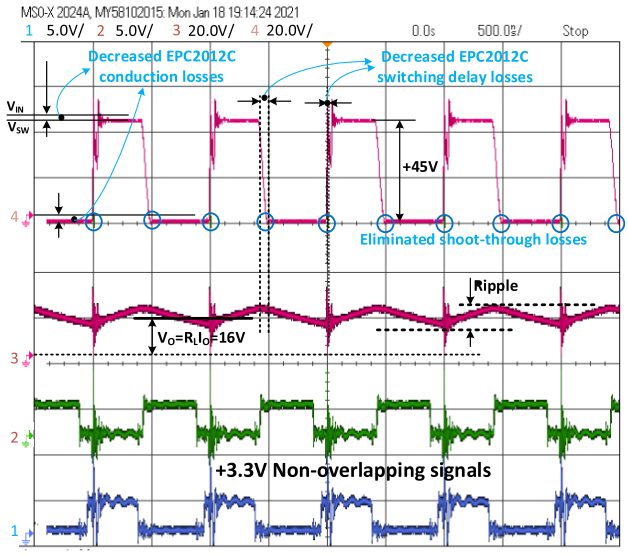

Fig. 15. Measured waveforms of the test half-bridge circuit with the fabricated DTCC circuit.

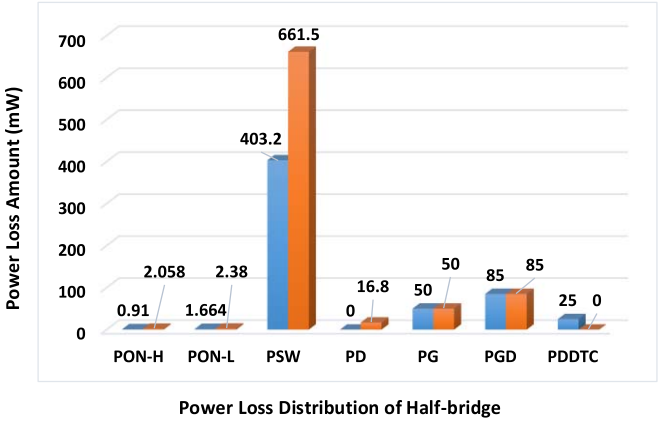

Fig. 16. Histogram of the calculated power losses of the test half-bridge circuit with and without the fabricated DTCC.

(P_{GD}). The loss of the fabricated DTCC (P_{DTCC}) must be added to the attained DDPLs, P_G, and P_{GD} losses to achieve the total power loss of the implemented half-bridge circuit [48]–[53].

The experimental setup for characterizing the implemented half-bridge circuit with the DTCC prototype is presented in Fig. 14. The required dead-time for a power converter depends on the values of the load and V_{IN}. In this work, we measure the performance of the half-bridge circuit with the fabricated DTCC under two conditions. In the first condition, the input voltage (V_{IN}) is 24 V, and the half-bridge circuit is configured to drive a 100 Ω resistor in series with a 11.8 μH inductor. In the second condition, V_{IN} is 45 V, and the load is a 100 Ω resistor in series with a 150 μH inductor. Figure 14 (a) shows a screenshot of the circuit in the first condition (V_{IN} = 24 V, R_L = 100 Ω, L_L = 11.8 μH) taken by an oscilloscope. Meanwhile, Figs. 14 (b) and (c) present the output loads in the experimental setup for the two conditions. Figure 14 (d) illustrates the measurement setup. Figure 14 (e) shows the test's printed circuit board, including the half-bridge circuit. The size of the custom printed circuit board (PCB) used to characterize the half-bridge is 2.54 cm×3 cm and the size of the power switches are 1.7 mm × 0.9 mm. Figures 14 (f) and (g) respectively demonstrate the fabricated wire-bonded chip (DTCC) and one tiny power switch. Figure 15 plots the measured waveforms of the half-bridge circuit with the DTCC under the second condition. As shown in Figs. 14 (a) and 15, the DDPLs decrease significantly. The switching loss of the power switches is associated with the rise and fall times (t_r, t_f) of the V_{SW} (Fig. 13). The same is illustrated in Fig. 15. In the ON-state, the conduction loss of the power switches varies with the differences between the high levels of V_{IN} and V_{SW}. In the OFF-state, the conduction loss depends on the differences between the zero and low levels of V_{SW} (Fig. 13 (a)). As for the shoot-through loss, it is attributed to the A and B parts of the V_{SW} waveform

(Fig. 13 (a)). These parts are eliminated in the presented experimental results in Fig. 15.

D. Calculation of Power Losses

Figure 16 shows the histogram of the losses of the half-bridge circuit with and without the DTCC prototype. The blue and orange colors in the figure respectively represent the calculated losses of the half-bridge circuit with and without the fabricated DTCC. The power losses associated with the DDPLs of the half-bridge circuit with and without the DTCC prototype are 403.774 and 682.738 mW, respectively. This result implies a 40% improvement with the use of the proposed DTCC. The half-bridge circuit with the fabricated DTCC consumes 563.774 mW of total power; without the DTCC prototype, it consumes 834.538 mW. This result implies a 32% improvement in total power consumption when the proposed DTCC is utilized.

The maximum operating temperatures of the sensitive devices with and without the proposed DTCC are calculated. The results highlight the significance of the improvement of the power losses in the operation of the components of the half-bridge circuit. Figure 16 shows that the highest power loss corresponds to the switching loss of the HSPS (P_{SW}). The total power losses of the HSPS (i.e., $P_{ON-H}+ P_{SW}$) with and without the proposed DTCC are 663.558 and 404.11 mW, respectively. According to the equations in [48], [49] and the specifications of EPC2012C, the calculated operating temperatures of the HSPS with (4a) and without (4b) the DTCC are

$$T_{Ja} = 404.11\text{mW} \times 85°\text{C/W} + 85°\text{C} = 119.3°\text{C} \quad (4a)$$

$$T_{Jb} = 663.558\text{mW} \times 85°\text{C/W} + 85°\text{C} = 141.4°\text{C} \quad (4b)$$

The calculated T_{Ja} and T_{Jb} remain below the absolute maximum rating of $T_J = 150$ °C of EPC2012C. Nonetheless, the 22.1 °C improvement in the maximum temperature greatly enhances the safety of the half-bridge circuit.

Table II presents the measured performance of the half-bridge circuit with the proposed DTCC. The switching frequency (f_p), dead-time delay (t_d), output current (I_O), input voltage (V_{IN}), technology (Tech.), total loss improvement (ΔP_{loss}), and efficiency are compared with the reported measurement (Meas.) results of other solutions. The proposed DTCC circuit obviously provides the low and high sides of the half-bridge circuit with independent dead-time delays of 35 and 62 ns, respectively. These dead-times are robust and able to reduce the dependent losses of the half-bridge circuit by 40%. They also enhance the total power consumption by 32%. Meanwhile, the losses greatly decrease the maximum operating temperature of the half-bridge circuit. With the application of the proposed DTCC, the maximum operating temperature is considerably improved, thereby boosting the safety of the half-bridge circuit. A convenient dead-time can decrease the values of t_r, t_f, and the average delivered current. However, the values of V_{IN} and the operating frequency are fixed. That is why the amount of improvement of switching loss is limited.

IV. Conclusion

This study puts forward a circuit for generating dead-time delays to realize the proper non-overlapping operation of power converters. In traditional dead-time circuits, logic gates and inverters are used to create delays. Such scheme is prone to variations and limitations. By contrast, the proposed DTCC uses timing elements that integrate precise capacitors and current sources. The proposed DTCC can produce relatively long and independent time delays for HSPS and LSPS. The generated delays between the non-overlapping control signals meet the general requirements of half-bridge power converters. The proposed DTCC occupies a silicon area of 70 μm × 180 μm. It is validated using a test half-bridge circuit supplied at 45 V and 1 MHz. The half-bridge circuit is implemented with discrete off-the-shelf components. The effects of the proposed DTCC on the losses of the test converter are evaluated herein. The results show that the proposed DTCC improves the dead-time dependent converter losses by 40%. The measured performance of the presented DTCC is also compared with that of previous solutions.

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