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A reconfigurable RF sampling receiver for multistandard applications

Anis Latiri [a,*], Loïc Joet [b], Patricia Desgreys [a], Patrick Loumeau [a]

[a] *LTCI – CNRS UMR 5141, École nationale supérieure des télécommunications de Paris, 46, rue Barrault, 75634 Paris cedex 13, France*
[b] *ST Microelectronics, Crolles R&D, 850, rue Jean-Monnet, BP 16, 38926 Crolles, France*

Abstract

This article presents the architecture of a reconfigurable radio receiver intended for multistandard applications. The receiver is based on RF sampling and discrete time analog signal processing. Anti-alias filtering, downconversion by bandpass sampling, channel selection filtering and sampling rate decimation are performed throughout the receiver chain. By adjusting the input sampling rate, all these operations can be tuned to different RF bands. This achieves full system reconfigurability and allows us to cover most of the existing communication standards. *To cite this article: A. Latiri et al., C. R. Physique 7 (2006).*
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Résumé

Récepteur à échantillonnage RF reconfigurable pour applications multi-standards. Nous présentons dans cet article l'architecture d'un récepteur radio reconfigurable pour applications mutistandards. Le récepteur est basé sur l'échantillonnage en bande RF et sur un traitement de signal analogique à temps discret. Des opérations de filtrage anti-repliement, de translation en fréquences par sous échantillonnage, de filtrage canal et de décimation sont effectuées le long de la chaîne. En ajustant la fréquence d'échantillonnage, il est possible de translater toutes ces opérations d'une bande RF à une autre et d'adresser ainsi la plupart des standards de communication actuels. *Pour citer cet article : A. Latiri et al., C. R. Physique 7 (2006).*
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Mots-clés : Récepteurs radio ; Échantillonnage RF ; Mode courant ; Filtrage anti-repliement ; Temps discret

1. Introduction

The rapid growth of wireless communications and the emergence of new standards increase the demand for low cost multimode radio receivers. For handheld applications, a high level of integration, high flexibility and low power consumption are essential issues. One possible way to achieve multimode operation is *Software-Defined Radio* (SDR) which consists in designing hardware that can be reconfigured by software.

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* Corresponding author.
  E-mail address: anis.latiri@enst.fr (A. Latiri).

In transition from traditional radio receivers schemes to SDR architectures, most signal processing is shifted from the analog to the digital domain. This imposes more severe constraints on the A/D converter (high bandwidth, high dynamic range and sampling rate). The resulting excessive power consumption makes impossible the use of SDR in portable receivers. Discrete time analog signal processing techniques [1–3] (by means of switched capacitor circuits) can be employed here to alleviate the requirements imposed on the A/D converter. Moreover, this sort of processing has the advantage of being flexible and totally reprogrammable.

On the other hand, the evolution of submicron processes makes possible nowadays to sample signals straight at the RF band. By combining RF sampling to discrete time analog signal processing, one can design radio receivers well suited for multistandard applications. In this scheme, the RF signal would be first amplified and anti-alias filtered, then sampled and processed through analog discrete time techniques before being quantized by the A/D converter.

In this article, we propose a radio receiver architecture based on this same principle and intended to cover most of the existing wireless communication standards. The organisation of this paper is as follows. Section 2 reviews the proposed receiver architecture and its different blocks. In Section 3, the bandpass anti-aliasing filter is described. Section 4 presents the discrete time analog signal processing performed after sampling. Conclusions and discussion about receiver's reconfigurability are given in Section 5.

2. Receiver architecture

The proposed RF sampling receiver front-end architecture is shown in Fig. 1. It comprises a set of RF filters and tuned LNAs, anti-aliasing filters, bandpass samplers, discrete time analog signal processing blocks and A/D converters. For a given communication standard, the RF input signal is first filtered and amplified using the appropriate RF filter and LNA, then downconverted to intermediate frequency by subsampling. A continuous time bandpass filter is inserted in prior to provide sufficient protection against aliasing in the subsampling process. Once downconverted, the signal is processed in a discrete time analog way, by means of switched capacitors techniques. Recursive filtering for channel selection, anti-alias filtering and signal decimation are performed in the discrete time analog signal processing block (DTASP). The signal is finally A/D converted and the remaining signal processing tasks are performed digitally. A dedicated digital control unit (DCU) is used to generate all the required clock signals and provide them to the anti-aliasing filter, bandpass sampler and DTASP block.

The use of subsampling as a downconversion method can simplify the design of the receiver. Compared to more conventional RF mixers, only lower frequencies need to be generated and the sampling circuit itself may benefit from relaxed trade-offs. However, subsampling suffers from noise aliasing and interference folding which imposes the use of a specific bandpass filter prior to sampling, as it will be described later.

Note that all of the anti-alias filtering and discrete time signal processing are functions of the sampling frequency f_s and can be tuned to different frequency bands by simply changing the sampling rate. This makes the receiver's architecture fully reconfigurable and well suited for multistandard applications.

In order to achieve full circuit integration, the receiver front-end should be modified. RF filters continue to be a bottleneck for realizing complete receiver integration. The ultimate front-end should be composed then by a unique
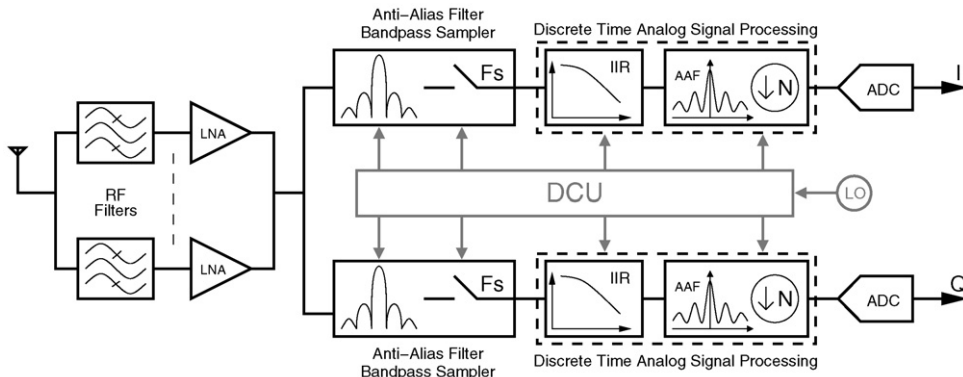

Fig. 1. RF sampling receiver architecture.

wideband LNA and no RF preselect filters at all. Even if realizations of wideband LNAs have already been reported [4], removing the RF filters would complicate the design of the anti-alias bandpass filter, as all the required attenuation will have to be provided by this single block.

3. Bandpass sampling

Bandpass sampling is the technique of undersampling a modulated signal to achieve frequency translation via intentional aliasing [5]. The sampling frequency requirement is no longer based on the frequency of the RF carrier, but rather on the information bandwidth of the signal. The resulting sampling rate can thus be significantly reduced.

3.1. Choice of intermediate frequency

By using bandpass sampling, an RF signal with a bandwidth BW and initially centered at f_c will be downconverted to an intermediate frequency f_{IF}. The f_{IF} is related to f_c and to the sampling frequency f_s as follows

$$f_{IF} = \begin{cases} \text{rem}(f_c, f_s) & \text{if } \lfloor \frac{f_c}{f_s/2} \rfloor \text{ is even} \\ f_s - \text{rem}(f_c, f_s) & \text{if } \lfloor \frac{f_c}{f_s/2} \rfloor \text{ is odd} \end{cases} \tag{1}$$

where $\text{rem}(a, b)$ denotes the remainder of a divided by b, and $\lfloor x \rfloor$ denotes the largest integer less than or equal to x. According to the bandpass sampling theory [6], and in order to avoid any destructive aliasing, the following three conditions must be met

$$f_s > \frac{BW}{2}, \qquad 0 < f_{IF} - \frac{BW}{2}, \qquad \frac{f_s}{2} > f_{IF} + \frac{BW}{2} \tag{2}$$

There are many possible choices for the intermediate frequency f_{IF} (and hence, the sampling frequency f_s). Selecting the more appropriate one for bandpass sampling is governed by the same principles as for conventional RF architectures with mixers. For simplicity reasons, this work will only consider the zero-IF case. All the other cases, where the intermediate frequency is not set to zero (low-IF for instance), are based on the same principle, but will result in more complicated clock schemes.

3.2. Anti-aliasing filter

One of the major drawbacks of subsampling is probably interference folding. When bandpass sampling an initial RF signal centered at f_c, not only the desired signal will be downconverted to f_{IF}, but also all the unwanted components located at frequencies $f_{ALIAS} = f_c \pm k \cdot f_s$ (where $k = 1, 2, 3, \ldots$). In order to avoid this signal destruction, anti-alias filtering must be performed prior to sampling. The bandpass filter to be used here must be centered on the RF channel frequency f_c and must properly attenuate components located at f_{ALIAS} frequencies. The filter must also be reprogrammable, in order to readjust its response when moving from one channel to another. Such a filter can be realized using an integrate-and-dump or windowed integration sampler [7]. A simplified schematic of a charge sampling circuit is given in Fig. 2.
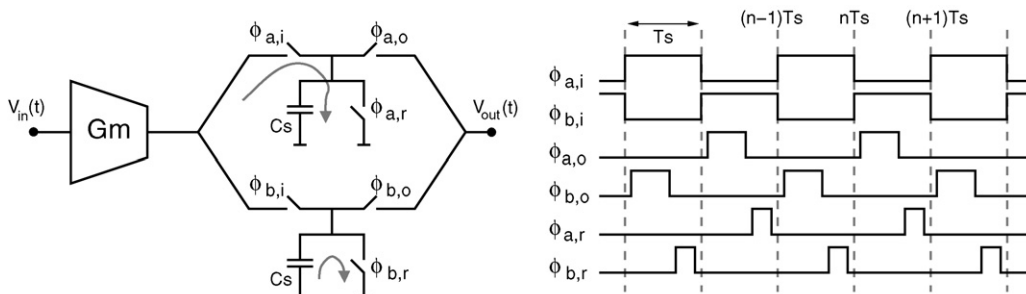

Fig. 2. A simple charge sampling circuit.

The process is composed of charging, holding and resetting phases. The received RF voltage is first converted into current through a G_m transconductance and integrated on a capacitor C_s during one sampling period T_s. Then the capacitor is disconnected and the voltage stored on it comprises a discrete sample. There are actually two sampling capacitors working in a time-interleaved way. While one sampling capacitor is busy integrating the RF current, the second sampling capacitor is not integrating the RF current and therefore its charge can be read out. The roles are then reversed to allow the charge integrated by the first sampling capacitor to be read out.

The voltage resulting from the accumulated charge on a sampling capacitor at time $t = nT_s$ is given by [8]

$$v_{\text{out}}(nT_s) = \frac{G_m}{C_s} \int\limits_{(n-1)T_s}^{nT_s} v_{\text{in}}(u)\,\mathrm{d}u = \frac{G_m}{C_s} \int\limits_{-\infty}^{\infty} v_{\text{in}}(u) \cdot \Pi(nT_s - u)\,\mathrm{d}u \tag{3}$$

where $\Pi(u)$ is the gate function of width T_s. (3) is the expression of the convolution of $v_{\text{in}}(t)$ and $\Pi(t)$ at the sampling time nT_s. In the frequency domain, the output spectrum is the multiplication of the input signal spectrum by the Fourier transform of the gate function $\Pi(t)$, which is equal to

$$F_\Pi(f) = \frac{\sin(\pi f T_s)}{\pi f} \cdot \mathrm{e}^{-j\pi f T_s} \tag{4}$$

Combining this frequency multiplication with the periodic spectrum repetition caused by the sampling process and omitting the holding phase, the final spectrum of the charge sampling is

$$V_{\text{out}}(f) = \frac{G_m}{T_s C_s} \sum_{k=-\infty}^{\infty} V_{\text{in}}(f - kf_s) \cdot F_\Pi(f - kf_s)$$

$$= \frac{G_m}{T_s C_s} \sum_{k=-\infty}^{\infty} V_{\text{in}}(f - kf_s) \cdot \frac{\sin(\pi(f - kf_s)T_s)}{\pi(f - kf_s)} \cdot \mathrm{e}^{-j\pi(f - kf_s)T_s} \tag{5}$$

By considering only the $k = 0$ term of (5), it is possible to extract the transfer function of the filtering operation performed by the charge sampling circuit. The transfer function is given by

$$\left| H(f) \right| = \frac{G_m}{C_s} \cdot \left| \frac{\sin(\pi f T_s)}{\pi f} \right| \tag{6}$$

which is a lowpass sinc function with transmission zeros (notches) at every integer multiple of the sampling frequency kf_s. As the required anti-alias filter should be a bandpass filter centered at the RF channel frequency f_c, a lowpass to bandpass transformation must be operated. The resulting modification on the charge sampling circuit is given in Fig. 3. For simplicity, only one sampling capacitor C_s is shown here, but the circuit still requires two time-interleaved capacitors to continuously integrate the input current.

A differential output transconductor is used at present. The current is now integrated into the sampling capacitor C_s alternately in a positive then a negative direction at the f_c channel frequency rate. Each sampling period T_s is now composed of an integer number of T_c periods ($T_s = N \cdot T_c = N/F_c$), which guarantees that the RF signal will be effectively downconverted to DC, as stipulated by (1). Integrating the input RF current in this way is equivalent, in the time domain, to multiplying the window function $\Pi(t)$ by a square wave carrier at the f_c frequency. In the frequency
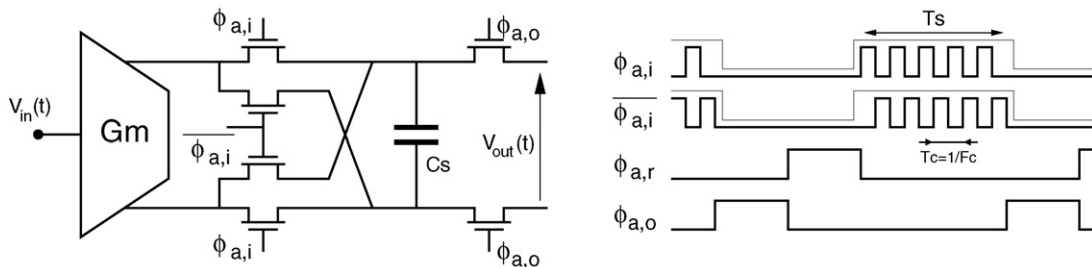

Fig. 3. Schematic of the bandpass charge sampler.

Continuous Time Bandpass Anti–Alias Filter
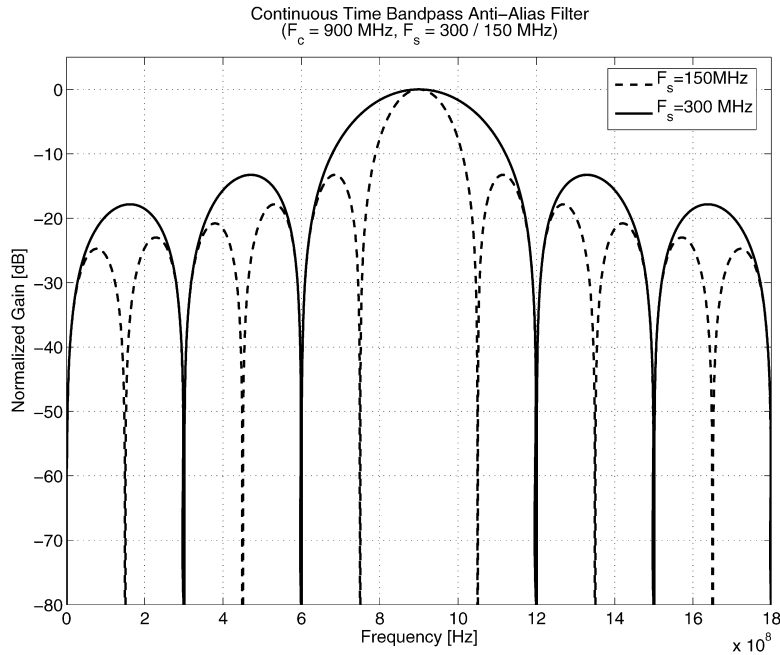(F$_c$ = 900 MHz, F$_s$ = 300 / 150 MHz)

Fig. 4. Frequency response of the filtering performed through the bandpass charge sampler.

domain, the Fourier transform of $\Pi(t)$ is thus convoluted by Dirac impulses at $\pm\lambda f_c$ (where $\lambda = 1, 3, 5, \ldots$), which will have the effect of shifting the filter's response. Without considering the sampling process, the resulting filter transfer function is now given by

$$\left|H_{\text{sinc}}(f)\right| = \frac{G_m}{C_s} \cdot \left|\frac{\sin(\pi(f - f_c)T_s)}{\pi(f - f_c)} + \frac{\sin(\pi(f + f_c)T_s)}{\pi(f + f_c)} + \cdots\right| \tag{7}$$

Considering the first term of (7), the transmission zeros of the bandpass filter are now located at the exact aliasing frequencies $f_{\text{ALIAS}} = f_c \pm k \cdot f_s$. These unwanted components are thus filtered out and will not fold over on top of the desired signal after subsampling. As an example, the filter's response is plotted in Fig. 4 for an RF signal initially centered at $f_c = 900$ MHz and two different sampling frequencies. In both cases, the aliasing components are removed. Only the desired signal will be downconverted to DC by the subsampling process.

Note that it is possible to further reject these aliases by increasing the order of the filter, at the cost of more circuit complexity [9,10]. Higher order filters are actually employed with some stringent wireless standards (like GSM) where attenuations of several tens of dBs are required.

4. Discrete time analog signal processing

The signal at the output of the bandpass sampler is now a discrete time signal centered at DC. High sampling rates and large levels of adjacent channel blockers and interferers would impose severe constraints on the A/D converter, if the signal has to be directly digitized without any further processing. The role of the DTASP is thus to lower the sampling rate and the required dynamic range by decimating and filtering the signal prior to A/D conversion. Switched capacitors techniques will be used here to perform these tasks. All the signal processing operations can be easily transposed from one standard to another by changing the sampling rate, the number and/or the values of the capacitors in use.

4.1. Decimation and FIR filtering

To reduce noise aliasing in RF signal subsampling, a high sampling rate f_s is desirable. On the other hand, a too high sampling rate is not suitable for the A/D converter due to excessive power dissipation. One method to combine
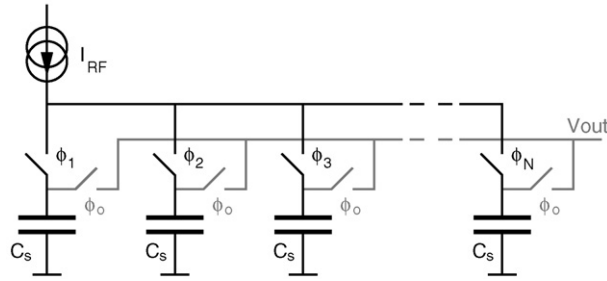
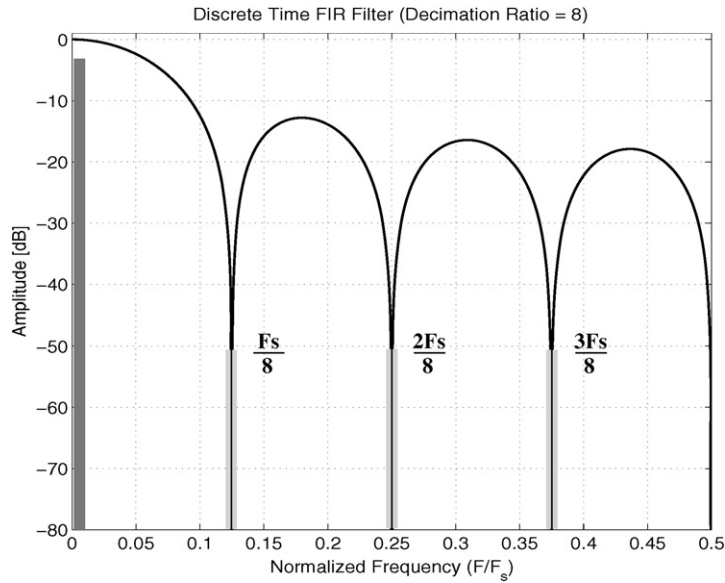Fig. 5. Use of a capacitor bank for signal decimation.

Fig. 6. FIR filtering prior to decimation.

these requirements is to reduce the sampling rate by signal decimation. This decimation will unfortunately cause aliasing of unwanted components located at frequencies $f_{\text{ALIAS}} = \frac{k}{N f_s}$ (where N is the decimation ratio) on top of the desired signal. As for the bandpass sampling process, an anti-aliasing filter must be used prior to decimation. A discrete time FIR filter [11] can be implemented by using capacitor banks for the current integration. A simplified schematic of the circuit is given in Fig. 5.

The capacitor bank is composed of N capacitors in parallel driven by $(\Phi_1, \Phi_2, \ldots, \Phi_N)$ clock signals. During each sampling period T_s, one single capacitor is connected to the input for the current integration and the other capacitors are waiting for their turn. On the next period, the capacitors are rotated and a new one is selected for the current integration. After N cycles, a charge read-out is performed by combining the individual charges together (short circuit the rotating capacitors together) and then reading the combined charge at the final rate of f_s/N. This results in an FIR filtering operation with a moving average of length N and all the coefficients being unity. The FIR filtering can be expressed in equation form as

$$w = \sum_{i=0}^{N-1} u_i, \qquad \frac{W(z)}{U(z)} = \sum_{j=0}^{N-1} z^{-j} \bigg|_{z=e^{j\omega T_s}} \tag{8}$$

where u_i is the ith sample and w_i is the accumulated charge on the sampling capacitor. The FIR filter frequency response is shown in Fig. 6 for a decimation ratio of $N = 8$. Again, the transmission zeros of the sinc function are located at the exact aliasing frequencies and the decimation is hence performed without significant signal degradation.

4.2. IIR filtering

The current-mode sampler can be further modified to perform an infinite impulse response (IIR) filtering operation simply by adding one additional switched capacitor [12]. The IIR filter will perform part of the channel selection by attenuating the adjacent channel interferers. It will also prevent the ADC from saturating by adjusting the power levels to the available input dynamic range. A simplified schematic of the modified capacitor bank is given in Fig. 7.

The newly added capacitor C_H is always connected to the RF input. While the rotating capacitors C_R integrates the current in turn and only during one sampling period T_s, the capacitor C_H continually integrates the current and is used to store its history. Every time a rotating capacitor C_R is disconnected from C_H, charge sharing occurs and each capacitor takes away charge proportional to its size. C_H is never discharged and retains a charge in proportion to the ratio $a = C_H/(C_H + C_R)$ as C_R is separated from it. This creates an IIR filter equation where the pole is ideally determined by the ratio of C_H and C_R. This can be expressed as

$$s_j = a \cdot s_{j-1} + w_j, \qquad \frac{S(z)}{W(z)} = \frac{1}{1 - a \cdot z^{-1}}\bigg|_{z=e^{j\omega T_s}} \tag{9}$$

where w_j is the input charge integrated over the most recent N cycles and s_j is the total charge stored in the system at sampling time j. The IIR filter frequency response is drawn in Fig. 8 for two different capacitor ratios.
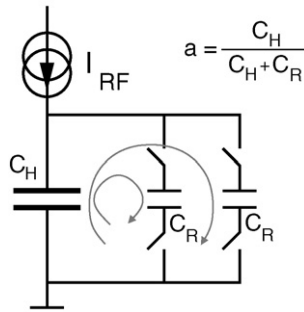

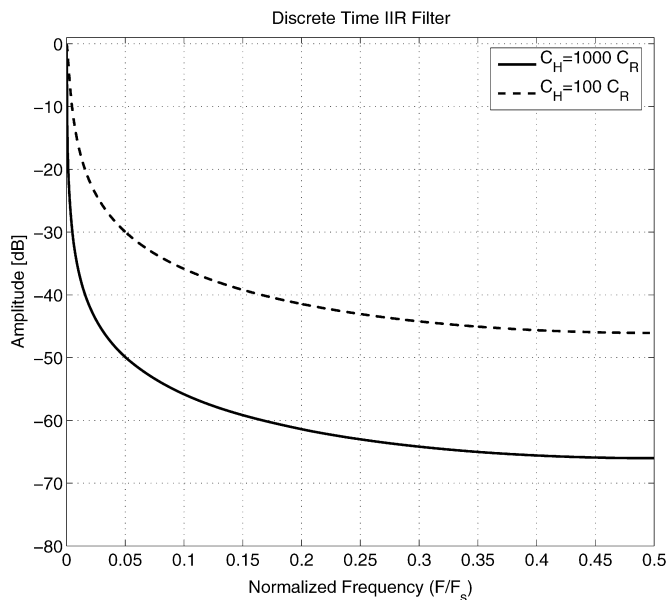Fig. 7. IIR operation through history capacitor.
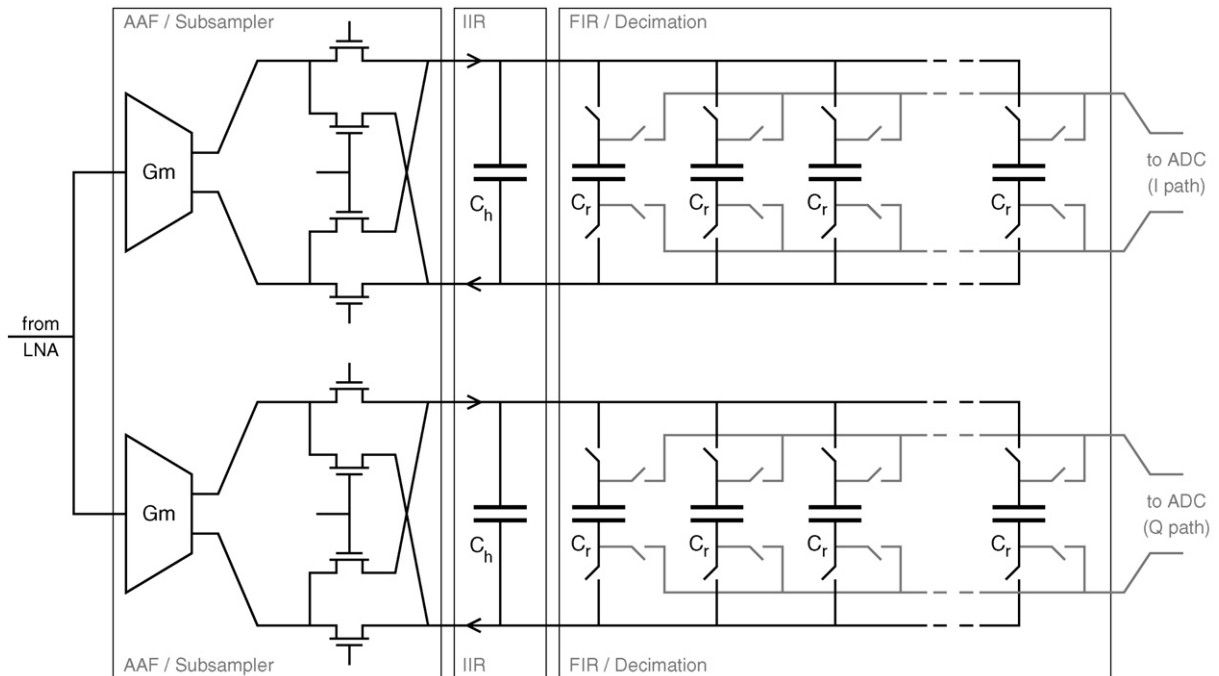

Fig. 8. IIR filter transfer function.

Fig. 9. Bandpass charge sampler and discrete time analog signal processing block in series.

The filter selectivity is only limited by the largest value allowed for the history capacitor. Note that high selectivity filtering may lead to in-band signal attenuation, especially in the case of wideband standards. This problem can be addressed by signal processing later in the digital domain, provided that the attenuation remains low. Practically, the size of each rotating capacitor will be a few hundred femtofarads, while the history capacitor will be several tens of picofarads.

A complete schematic of the bandpass charge sampler together with the DTASP block is given in Fig. 9. The in-phase (I) and quadrature (Q) paths are identical, though controlled by clock signals with a $\pi/2$ phase difference. The anti-alias filtering response is centered at the desired channel frequency f_c by adjusting the clock signals controlling the different switches of the bandpass charge sampler. The clock waveforms depends only on the sampling frequency f_s and the RF channel frequency f_c. After anti-alias filtering, the signal is downconverted to baseband through bandpass sampling. The decimation factor N, which is also the number of rotating capacitors per bank, is set by the ratio of the initial sampling frequency f_s to the ADC's maximum sampling frequency. Finally, the adjacent channel levels together with the ADC's dynamic range input set the required IIR filter selectivity and hence imposes a certain C_H to C_R capacitor ratio.

5. Conclusion

A fully reconfigurable RF receiver front-end architecture for multistandard applications is proposed in this article. The receiver uses direct RF bandpass sampling and discrete time analog signal processing. By adjusting circuit parameters such as the input sampling rate, the number and the values of the switched capacitors in use, it is possible to adapt the performed signal processing to any desired wireless communication standard.

Acknowledgements

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