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Advancements in passive planar lightwave circuits and hybrid integration devices

Progrès dans les circuits optiques passifs à technologie plane et composants intégrés hybrides

James R. Bonar *, Russell Childs, Richard I. Laming

Alcatel Optronics UK Ltd, Starlaw Park, Starlaw Road, Livingston EH54 8SF, UK

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Abstract

Planar silica device technology provides the ability to filter, route, switch, and attenuate optical signals for Wavelength Division Multiplexing (WDM) based photonic networks. As network capacity expands there is a requirement to increase the complexity, scale and density of the functions whilst reducing cost. It is also important that both the optical performance and long term stability of the devices are not compromised. The following paper reviews recent progress on these types of devices for large-scale manufacture, concentrating on key performance parameters for filter type structures and hybrid integrated devices such as insertion loss and polarisation dependent loss (PDL). ***To cite this article: J.R. Bonar et al., C. R. Physique 4 (2003).***

Résumé

La technologie d'intégration planaire de composants à base silice permet le filtrage, le routage et la commutation. Elle rend également possible l'atténuation de signaux optiques pour les applications de réseaux photoniques multiplexés en longueur d'onde (WDM). Au fur et à mesure de l'expansion de la capacité de réseau, il faut augmenter la complexité, l'échelle et la densité de ces fonctions tout en réduisant le coût associé. Il est également important de ne pas compromettre les performances optiques et la stabilité à long terme de ces composants. Nous passons en revue les progrès récemment effectués dans ce domaine sur le plan de la fabrication à grande échelle, nous concentrant particulièrement sur les paramètres-clé que représentent les pertes d'insertion et les pertes dûes à la polarisation (PDL) pour les composants de filtrage et d'intégration hybride. ***Pour citer cet article : J.R. Bonar et al., C. R. Physique 4 (2003).***

Keywords: Integrated optics; Array waveguide gratings; Wavelength division multiplexing; Variable optical attenuator; Integrated tap detector; Semiconductor optical amplifier; Hybrid integration; Fabrication

Mots-clés : Optique intégré ; Réseaux en faisceaux de guides d'onde ; Multiplexage en longueur d'onde ; Atténuateur optique variable ; Échantilonneur de signal intégré ; Amplificateur à semi-conducteur ; Intégration hybride ; Fabrication

* Corresponding author.
E-mail address: jim.bonar@alcatel.co.uk (J.R. Bonar).

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1. Introduction

Planar silica technology lends itself to fibre-based systems [1,2] as the high silica technology offers the potential of integrating a number of passive functions on a Si motherboard [3–5]. The technology provides intrinsically low loss material, which is suitable for fibre coupling and is rugged, mass producible and low cost in comparison to labour intensive bulk-optic configurations [6]. The following sections provide the reader with a more in-depth study of the processes adopted.

High performance Array Waveguide Grating devices (AWGs) for multi/demultiplexer functions are described. Particular focus is drawn to the low insertion loss, low polarisation dependent loss and low crosstalk for the AWG family of products. The performance and repeatability of the devices is indicative of the high quality of the material leading to low phase and amplitude errors for low crosstalk AWGs.

Hybrid integration advances within Alcatel Optronics (AOUK) have established leading edge capability with the adaptation of micro-opto-electro-mechanical systems (MOEMs) for planar silica technology. This offers, as an example, variable optical attenuators (VOAs) that are low loss, compact and have low power consumption. Techniques have also been adapted to provide integrated tap coupler and photodetector capability. Within this article an 8-channel combiner device will be discussed which accommodates 41 discrete optical functions onto the one substrate. The advantages this offers with relation to size, fibre management and cost are detailed. Active and passive integration has also been realised. An InP semiconductor optical amplifier (SOA) has been flip chipped onto a silica on silicon platform and coupled to an AWG. This single hybrid chip amplifier is needed to compensate for the losses in the demux function and to improve receiver sensitivity

2. Advanced fabrication techniques

The planar lightwave circuit (PLC) process at AOUK is based on flame hydrolysis deposition (FHD) and reactive ion etching (RIE). The high silica on silicon process is fabricated on 8″ silicon wafers. This technology breakthrough offers the advantages of complex optical functions to be fabricated on the one substrate, providing a path for active and passive integration. From a manufacturing point of view it also yields more devices per wafer leading to lower product costs and is compatible with state of the art, high volume, semiconductor equipment.

FHD is an industry standard technique for forming high silica waveguide structures. However, to provide devices with leading edge performance such as AWGs, it is necessary that both the base waveguide dimension and index be accurately controlled. Fig. 1, is a thickness map for the standard FHD core layer on an 8″ wafer. It is observed that the thickness control is excellent with a 3σ value of 1.5% and a thickness range of <0.2 μm across the 7 μm layer. Fig. 2 is a high-resolution

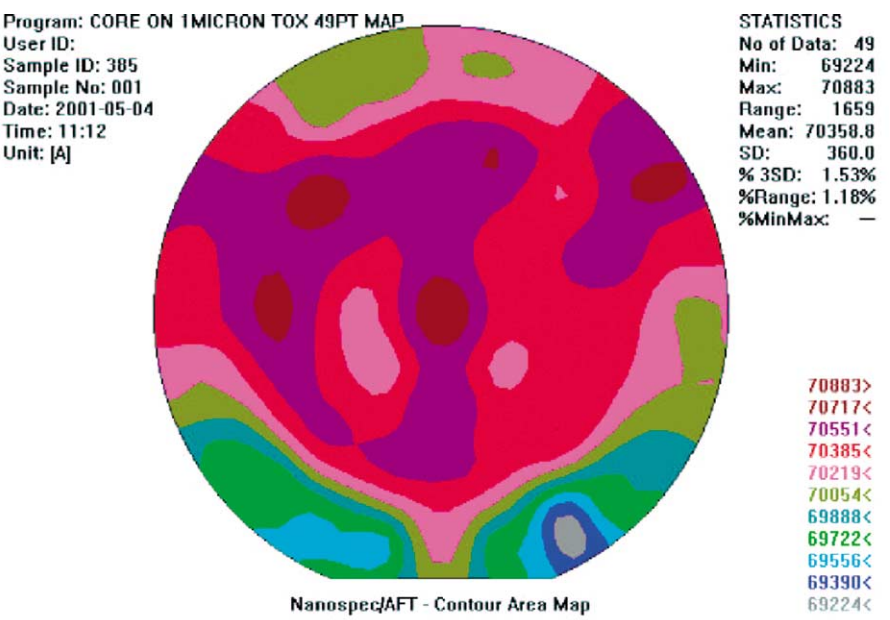

Fig. 1. Thickness map of a standard FHD core layer across an 8″ wafer.

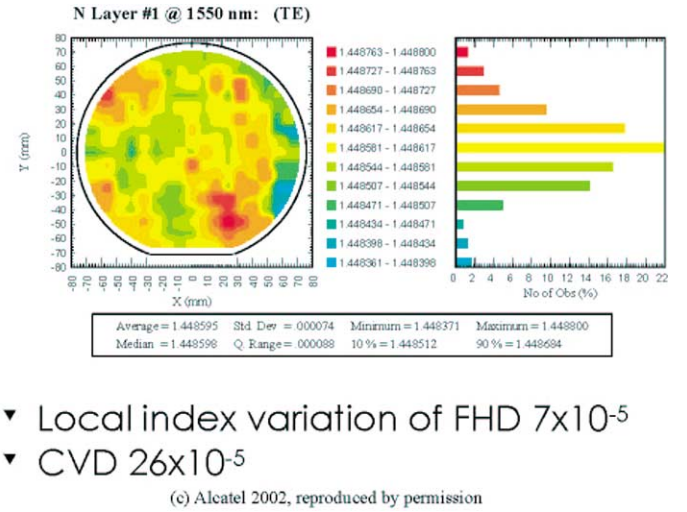

Fig. 2. High-resolution wafer map of the refractive index. The local refractive index measured at 1 mm intervals is provided for improved FHD core (7×10^{-5}).

wafer map of the refractive index. The resolution of the system is 1×10^{-5}. Once again the refractive index control is very good. Local index measurements were taken on a 1 mm period on different material with nominally the same refractive index ($\delta n = 0.7\%$), as measured using the standard prism coupler technique. The local index variation for AOUK (plasma enhanced vapour deposition (PECVD)) techniques was measured to be 26×10^{-5}. However, by optimising the FHD process parameters and system set up it was possible to improve the local index value for FHD to 7×10^{-5}. The impact this has on AWG device performance is discussed later. The improvement in core layer performance also enabled low loss channel waveguides to be fabricated. Using spiral waveguide masks of 1.5, 2 and 3.5 metre waveguide lengths the propagation loss was measured to be typically $\sim$0.02 dB/cm for 0.7% index contrast waveguides. The polarization-dependent loss (PDL) was also measured to be typically less than 0.1 dB for all lengths of spiral waveguides. These values are indicative of high performance plasma etching.

To pattern the PLC devices typical photolithographic masking techniques use either standard contact or projection type mask aligners. At AOUK a wide-angle stepper system is employed which is compatible with $8''$ wafer requirements. The non-contact stepper offers many advantages and the mask magnification properties offer sub-micron resolution and reduced defectivity due to non-contact operation [7,8]. Also, mask consumption and associated cost is much reduced. Typical PLC devices may also require stitching together of multiple object fields (reticles) to provide the overall device structure. Techniques have been developed and devices with multiple fields fabricated. The impact on optical performance of the improved photolithography is demonstrated in the next section.

Plasma etching techniques must also be suitable for waveguide core etching [9,10]. Both the masking and core are plasma etched to reduce the effect of sidewall roughness. Techniques based on lift-off or metal etch were observed to impact both the roughness and the corrugation periodicity. Thus, to establish channel waveguide losses of $<$0.02 dB/cm the etch quality was dramatically improved, as shown in Fig. 3(a). This was also developed to enable suitable etch rates such that deep silica etch profiles could be established. Fig. 3(b) is a scanning electron microscope (SEM) image of a slot through the SiO_2 clad, core and buffer material. This indicates the excellent optical quality of the $\sim$40 μm facet which is essential for providing slot structures for shutter type attenuators [11] in PLC circuits. The sidewall angle is $>89°$ and the roughness is low ($<$50 nm) to provide low insertion and return loss.

To integrate both MOEMs and active devices (detectors and lasers) advanced photolithography and metal deposition techniques have been developed to enable both electrical and optical functions on a single chip. Localised hermetic capping capability has also been developed to protect the devices from moisture ingression and airborne contaminations.

AuSn bumps and Au tracks as well as micro mechanical alignment structures are fabricated at the bottom of wells that are 40 μm deep. The MOEM devices are precision flip chipped to an alignment accuracy of ± 1 μm in the lateral and vertical directions. To integrate photo diode arrays, flip chip and 're-direction of light' techniques have been developed. The re-direction of light involves advanced stepper lithography to provide 45°-angled slots in the tap waveguide sections [12]. The slots are subsequently metal coated. Smoothening techniques provide mirror like facets to provide out of plane re-direction of light on to front illuminated InGaAs Pin diodes. Techniques have also been developed for integration of edge type photo detectors [4]. However, integration of front side detectors is the preferred solution for array type devices. Fig. 4 provides a schematic of the process.

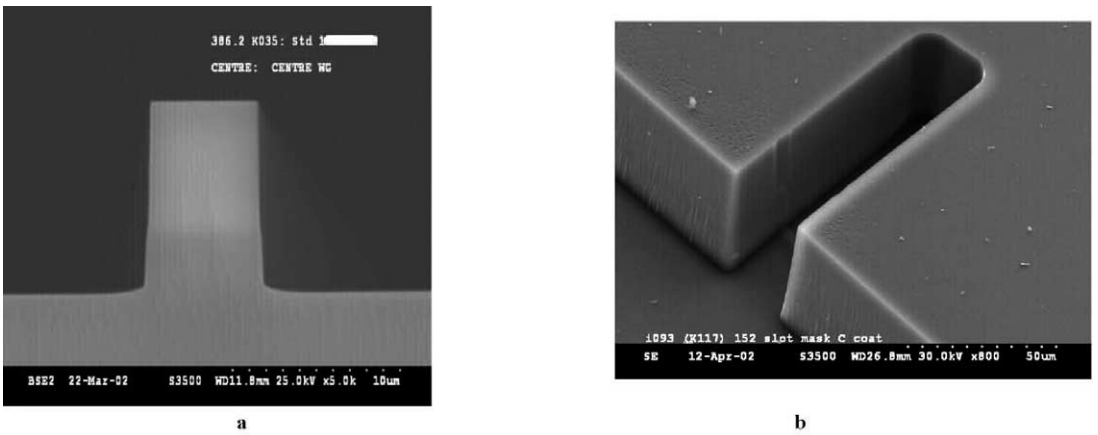

Fig. 3. (a) Scanning Electron Microscope (SEM) of etched waveguide core; (b) SEM of 40 μm deep slot in SiO_2.

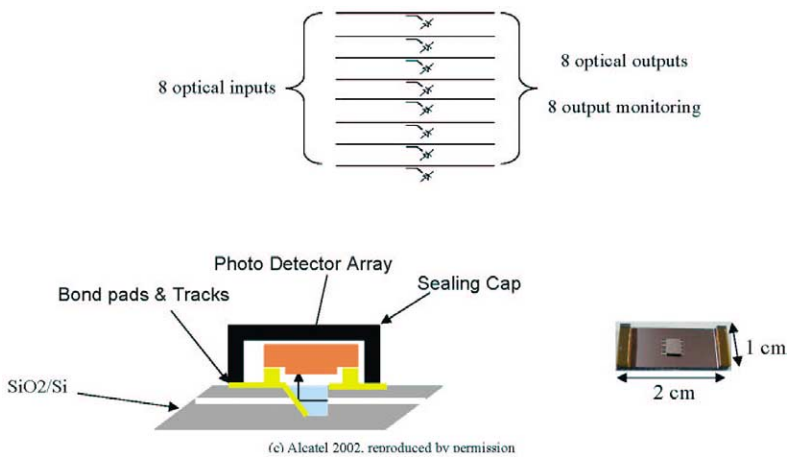

Fig. 4. Schematic of integrated 8-array tap detector structure. Side elevation of 're-direction of light' and photo diode is also included, with the final 8-array device size indicated.

3. Array Waveguide Gratings (AWG's)

A fundamental component for the multiplexing and demultiplexing of wavelengths in optical dense wavelength-division multiplexing (DWDM) networks is the AWG. The planar-based solution is well established [13–15] and is increasingly becoming the favoured solution for medium and high channel count ($\geqslant 8$) applications. The preferred manufacturing technique is based on silica-on-silicon as it provides a means to low loss material, which is ideally suited to single-mode fibre requirements. The devices have many appealing optical qualities such as low loss, low PDL, low crosstalk, scalable design and low dispersion. The stability and compactness of the device is also advantageous. As systems migrate to higher line rates (10 Gb/s and 40 Gb/s) it is important that there are system components with lower dispersion, especially as multiple filters are concatenated through the system.

The AWG is similar in principle to a prism or diffraction grating, i.e., it spatially separates different wavelengths of light. Fig. 5 illustrates the device layout, where the slabs act as a lens and the array waveguides as a prism. The lengths of the adjacent array waveguides have a near constant path length difference ΔL which is an integer multiple of the centre wavelength of the AWG. The effect is to cause dispersion and thus to direct different wavelengths to different output waveguides, i.e., the location of the focused signal wavelength, λ, is due to the phase delay in each array waveguide, given by $\Delta L/\lambda$. The centre wavelength, λ_c, is satisfied by the condition $N_{\text{eff}} \cdot \Delta L/m$, where N_{eff} is the effective index of the waveguide mode and m is the grating diffraction order.

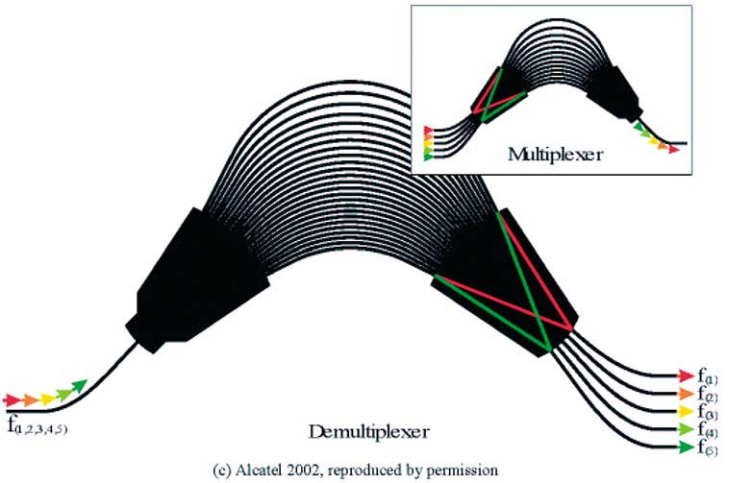

Fig. 5. Typical demultiplexer/multiplexer AWG layout.

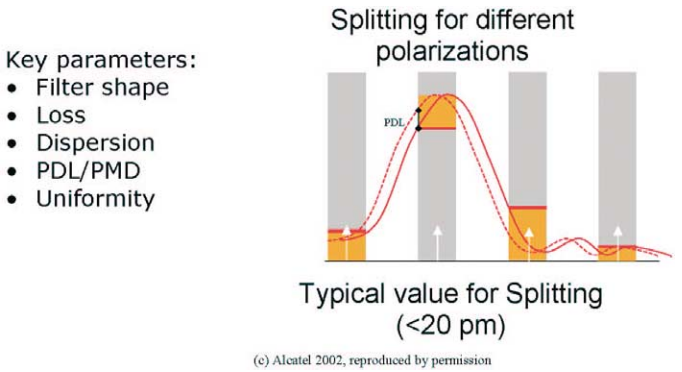

Fig. 6. Schematic representation of the 'clear window' parameter definition. This provides the system designer with the worst-case values. Key parameters: filter shape, loss, dispersion, PDL/PMD, uniformity.

Fig. 5 illustrates the AWG operating principle. The input light is launched into the input waveguide and then diverges laterally as it crosses the input slab where the beam is collected by the arrayed waveguides. The light coupled into the array usually has a Gaussian type of distribution. At the second slab the light constructively interfere at a focal point, thus reproducing the input field distribution. The position of the focal point varies linearly along the output aperture (image plane). This focal line follows a radius of curvature and the receiver waveguides are appropriately positioned on this line (R_x). The impact of this is that design modules allow the channel spacing and number of channels to be varied with no substantial impact on performance.

With regards optical performance it is important to establish parameter definitions, which provide the network designers with the performance of the device over the entire wavelength bands, used in the system [16]. It is essential that the worst-case values, over lifetime, be provided to determine the system link budget. To enable this a 'clear window' is defined around each ITU wavelength. For a 100 GHz demultiplexer, a window of 25 GHz is commonly quoted. Fig. 6 provides as an example the impact the definition has on the PDL quoted performance. It should be apparent that the PDL of a device is in fact the maximum that the transmission can vary over all polarisations at a fixed wavelength over the entire clear window and is not the peak-to-peak variation or the PDL at the standard ITU (International Telecom Union) wavelength. Table 1 is a summary of the standard performance of a 40 channel 100 GHz AWG. The leading edge performance highlights the developments in both process and design.

Fig. 7 illustrates the spectra of a standard 40 channel 100 GHz AWG. Particular points of interest are the low insertion loss, noise floor and the steep filter shape. The low loss is indicative of the low loss of the base material and the advanced design. Spot size converter [17,18] structures have been developed for the standard 0.7% waveguide structures where waveguide down tapering has been implemented to reduce the fibre chip coupling loss. Careful consideration has been given to the design to implement adiabatic tapers that do not have detrimental effects on both the process capability and the PDL performance

Table 1
Standard performance of 40 channel 100 GHz AWG

Device	Flat top	Gaussian
Number of channels	100 GHz	
Clear window (GHz)	25	30
Insertion loss in clear window (dB)	4.5–5	3–4
Insertion loss @ ITU grid (dB)	3.5–4	1.5–2.5
Insertion loss uniformity (dB)	0.5	1–1.5
Pass band uniformity (dB)	0.5	1
Polarisation dependent loss in clear window (dB)	0.3	0.5
Polarisation dependent loss, peak-to-peak (dB)	0.1	0.1
Adjacent cross talk (dB)	28	28
Nonadjacent cross talk (dB)	35	35
Maximum integrated cross talk (dB)	25	25
Differential group delay (ps)	0.3	
Chromatic dispersion (ps/nm)	±10	

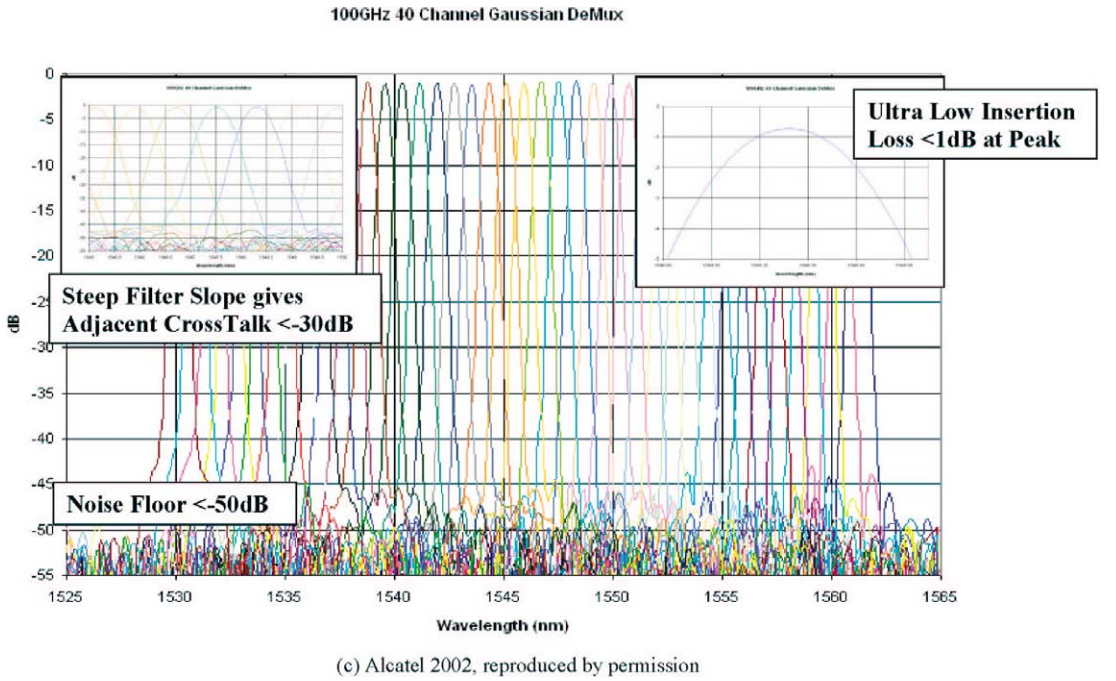

Fig. 7. Spectra of a standard 40 channel Gaussian 100 GHz AWG. Inset captions indicate the low loss and steep filter roll-off.

(<0.05 dB). Typical connection loss is approximately 0.2 dB per point. This is in comparison to the standard coupling loss of >0.5 dB point for standard 0.7%, 6×6 μm^2 waveguides. The design of the AWG has been based on reducing the waveguide spacing at the array waveguide transition region. The number of array waveguides is also large to reduce truncation effects, which leads to both extra loss and crosstalk. The advanced lithography and the FHD properties enable waveguides with edge to edge separation of 1 μm to be fabricated which can then be clad with >30 μm layers without the requirement of multiple deposition steps and re-flows. Crosstalk effects due to possible array coupling are negligible by minimising the effects of higher order excitation. Fig. 8 is the centre channel of an AWG plotted for different design iterations that indicates the impact of the design improvements, material homogeneity and the lithography advancements. This indicates a noise floor of 60 dB, with no additional trimming techniques required such as UV induced index changes [19] or laser trimming of α-Si layers [20], which are both costly, time-consuming and not suitable for large volume manufacturing. Maximum integrated crosstalk, for 40 channel 100 GHz AWG devices, are routinely measured to be >25 dB.

Characterisation methods for investigating phase and amplitude errors have also been developed. Techniques based on Optical Low Coherence methods (OLC) have been established [21]. Fig. 9 is the phase and amplitude distribution of the light

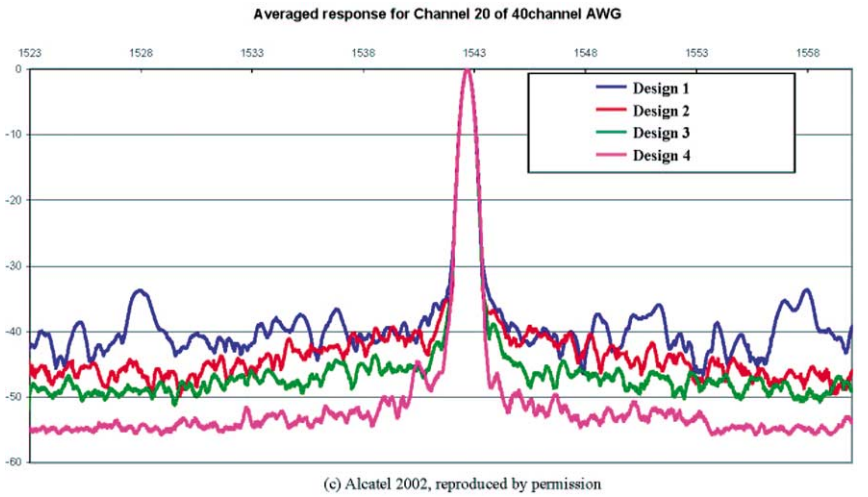

Fig. 8. Centre channel of a 100 GHz AWG plotted for improved process and design iterations.

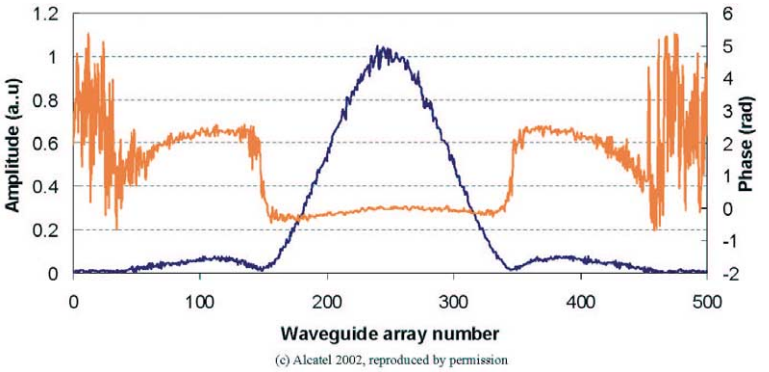

Fig. 9. Phase and amplitude distribution measured within the AWG array waveguides.

propagating through each arrayed-waveguide. Any deviations in phase will result in a degradation of the AWG transmission performance. The phase error is induced by deviations in waveguide parameters (index and dimensions), which intuitively becomes worse as the distance across the array waveguides increases. This generally results in good adjacent crosstalk and poor noise floor characteristics. A technique based on Inverse Fourier Transformation (IFT) has been successfully demonstrated which allows the characterisation of AWGs with small ΔL increments [22]. This is due to the fact that broadband sources with a coherence length shorter than ΔL are required. This technique was used successfully to characterise an AWG with a ΔL of 23 μm.

Fig. 10, illustrates the spectra of overlapped 25, 50 and 100 GHz devices. To provide this, the frequency response of the 25 GHz spectra is quadrupled and the frequency response of the 50 GHz is doubled and overlaid on to a standard 100 GHz device. Inset, is the spectra of the overlapped 50 and 100 GHz devices. This indicates the scalability and highlights the excellent performance of the insertion loss and noise floor (crosstalk) for the designs even at low power levels. As mentioned, this reflects the homogeneity of the base material and the photolithographic and plasma etching capability.

The design and process have also been developed to produce devices that have low intrinsic birefringence. It is generally accepted that birefringence takes place due to the difference in thermal expansion properties between layers in the device structure, which causes stress mismatch when the device is cooled after sintering or annealing. This impacts on the performance of the AWG where the focal position of the 2 orthogonal polarisation states are different, causing a polarisation dependent wavelength variation (splitting). To manufacture devices with low splitting, various techniques have been reported. Most have concentrated on altering the thermal coefficient of expansion (TCE) of the cladding to that of the Si substrate [23,24]. This has been demonstrated to be successful; however, careful consideration must be taken as this can lead to dopant rich claddings which are sensitive to moisture leading to device unreliability [25]. A technique based on stress relieving grooves along the side of the array waveguides has also been demonstrated [26], but this is unattractive due to the additional process step

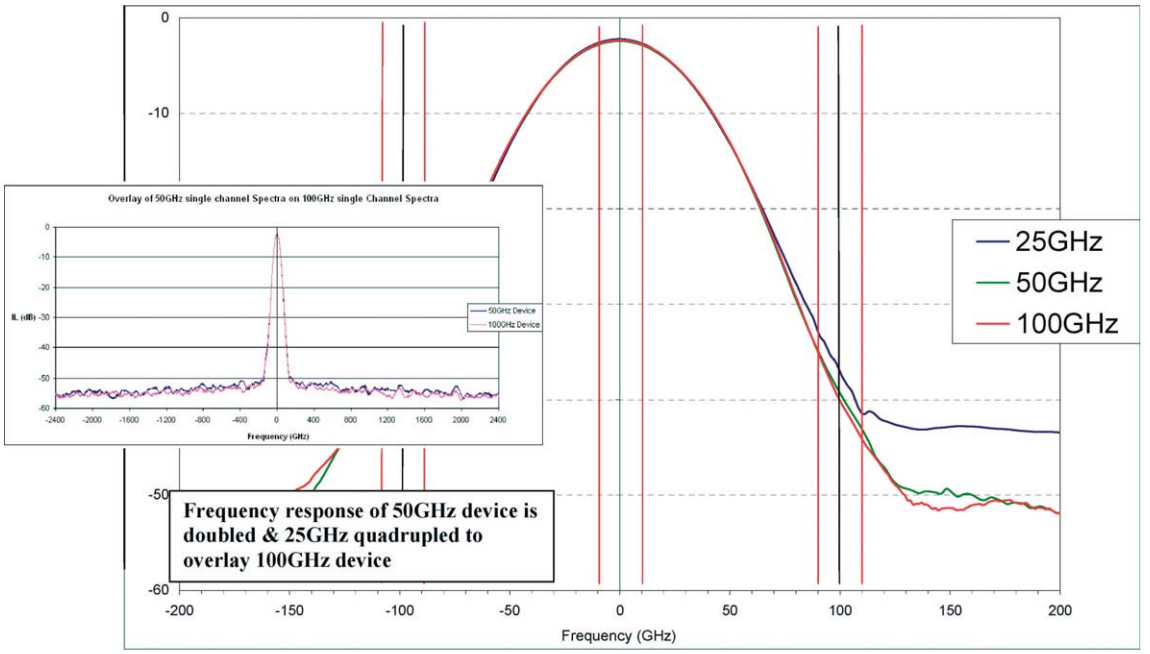

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Fig. 10. Spectra of overlapped 25, 50 and 100 GHz AWGs (frequency responses have been modified to allow overlap, e.g., 25 GHz has been quadrupled).

and the groove to waveguide alignment tolerance, as well as the extra device area required. Other polarisation compensation techniques demonstrated, have also been based on insertion of thin half-waveplates [27] and array waveguide width control [28]. The waveplate technique is unattractive as it involves extra processing, an additional part in the build of material, physical interruption in the array path (leading to increased possibility of phase errors) and additional groove loss when high index AWG's are used for high density or compact AWG architectures. Quartz substrates have also been demonstrated. This reduces the birefringence miss-match [29]; however, this is impractical for large device structures due to the cost and availability of quartz substrates and also the possibility of wafer warpage during consolidation. Also, these types of wafers do not lend themselves to advanced semiconductor manufacturing and hybridisation schemes.

The relationship between core and clad stress versus splitting has been modelled. This indicates that to achieve zero birefringence a clad layer, which is almost tensile, is required. This has been observed to be very susceptible to moisture ingress due to the high level of doping and also to cause core waveguide diffusion during the clad stage. However, a core over-etch technique, to form a mesa has been developed [30] which provides a means of fabricating devices with low birefringence without the need for either heavily doped cladding layers or additional grooves. Fig. 3(a) indicates a typical mesa type structure for an AWG input waveguide. When the core is subsequently clad it extends to below the level of the core. This has been observed to affect the core birefringence. Finite Element Modelling was used to determine the induced stress on the waveguide core. It was established that there was a linear distribution between the birefringence and the over-etch depth. Note, for practical reasons it is preferable to have a cladding with a larger TCE to reduce the over-etch depth requirement. As a result, a design of experiments (DOE) was conducted to look at the influence of various parameters on the splitting value. This has enabled optimisation of the splitting for the overall AWG structure and thus provided a stable technology model which extends across the AWG product portfolio, i.e., core stress, clad stress, average array waveguide spacing etc. Using this technique, robust and reliable 1209/1221 Telcordia compliant AWGs are fabricated with high yields.

The performance of a wavelength division multiplexing (WDM) system is affected by the properties of filters, especially as they are cascaded throughout the network [31]. Phase distortion within the channel passband produces unwanted dispersion that leads to pulse distortion ultimately resulting in transmission errors [32]. Thus, it is desirable to manufacture AWGs with small phase errors as demonstrated in Fig. 9.

The three interrelated parameters of interest are the differential group delay (DGD), Group velocity dispersion (GVD) and polarization-dependent wavelength (PDW) splitting. There relationship can be defined as follows;

$$\mathrm{DGD(ps)} = \mathrm{GVD(ps/nm)} \times \mathrm{PDW(nm)}.$$

Fig. 11 illustrates the relationship between the measured DGD and PDW for a Gaussian AWG. Fig. 12, indicates that for devices with low PDW, that the DGD and GVD is <0.5 ps and <5 ps/nm, respectively. Thus, Gaussian type AWG structures are available with low dispersion qualities, which lend themselves to higher bit rate systems.

Ideally the spectral response of the filter should be square. Flat and broadened filter shapes are desirable for system architectures due to laser diode drift, high bit rates, cumulative passband narrowing etc. For an AWG it is possible to flatten the response of the filter by producing a rectangular field profile at the exit of the second slab coupler (focal plane) [33–36]. Fig. 13 provides a spectra of a typical Flat Top 40 channel 100 GHz AWG.

Careful consideration must be given to the technique to flatten the passband, as this can cause detrimental behaviour for DGD and GVD [37]. The GVD is proportional to the phase difference $\Delta\phi$ between the fundamental and the second order mode

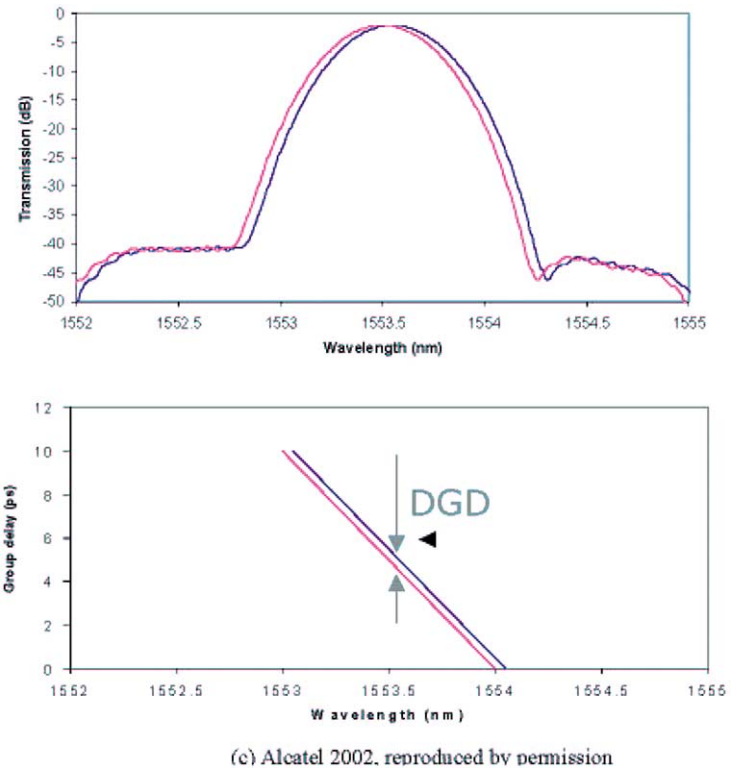


Fig. 11. Measured relationship between DGD and PDW for a Gaussian AWG.

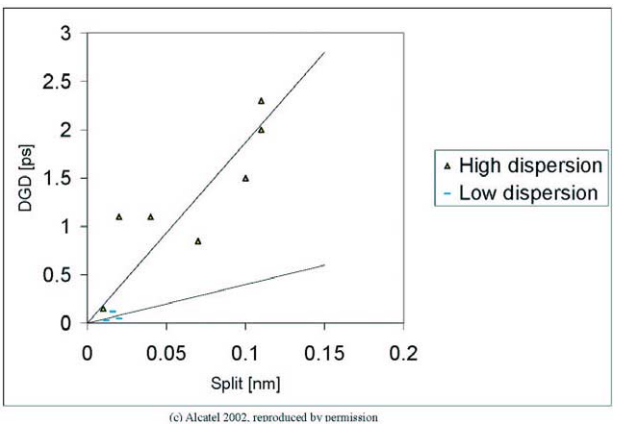


Fig. 12. Impact of PDW on measured DGD for AWG's with different process conditions.

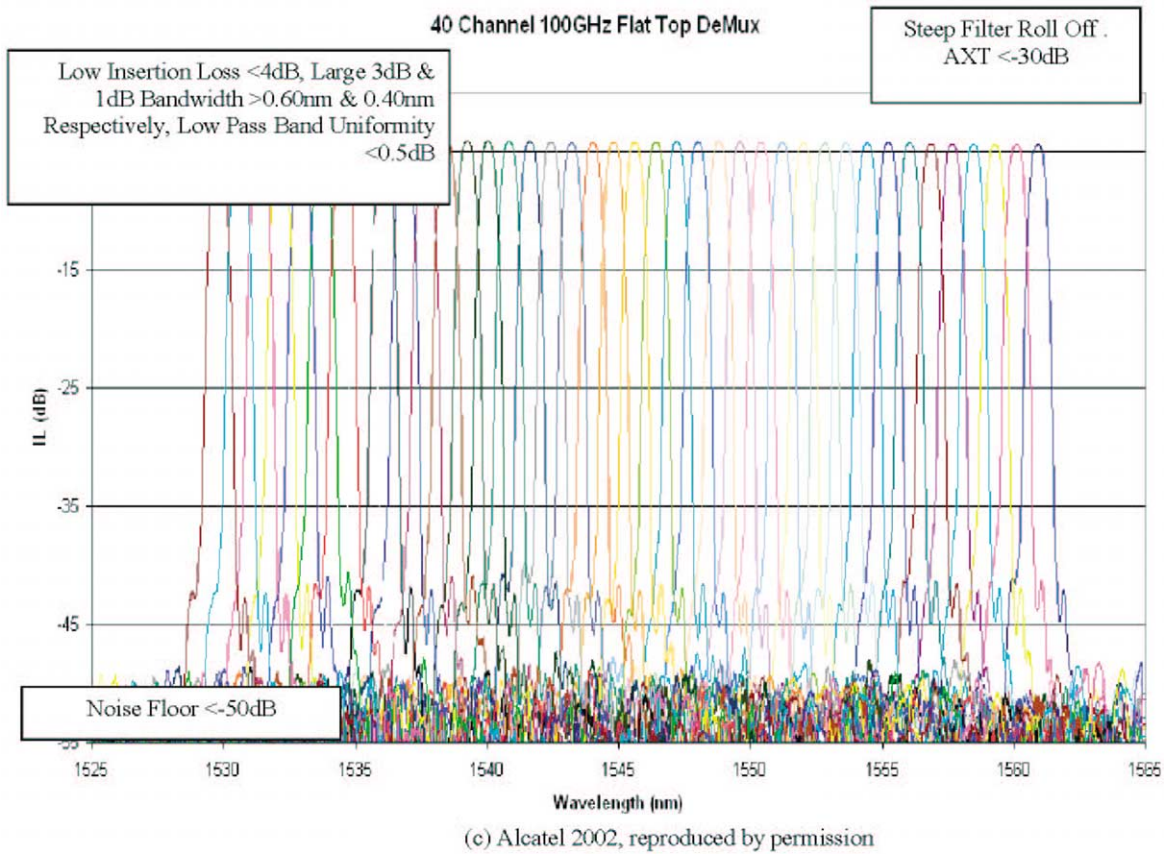


Fig. 13. Spectra of a standard 40 channel Flat Top 100 GHz AWG.

in pass band flattening structure, thus this can be designed to minimise $\Delta\phi$. Defocusing of an AWG can also be used at either the input or output waveguides. A positive defocusing indicates that the waveguide ends at a distance longer than the slab of the AWG. If the phase front is parabolic then this technique can be used to compensate the GVD. Also, the GVD can be improved by altering the phases in the array to obtain a flat phase front in front of the receivers.

Demultiplexer devices have been described. With respect to multiplexer devices AOUK have developed devices with particular emphasis based on low insertion loss. The performance of 40 channel 100 GHz multiplexer devices in a production environment has resulted in worst-case insertion loss values of 2 dB (including PDL) across the channel window of ± 12.5 GHz (note <1 dB to the peak of the filter). This is achievable due to the low intrinsic loss of the material and the designed low coupling loss to standard singlemode fibres. The noise floor of the devices manufactured are typically 50 dB and the integrated crosstalk measured to be >15 dB (limited by the adjacent crosstalk, as there is a requirement to have a large filter bandwidth).

For the AWG product family described the standard package configuration exhibits a typical wavelength drift of $< \pm 1.5$ pm (± 0.1875 GHz) over an ambient temperature range of -5 to 70 °C.

4. Hybrid integration

AOUK have successfully manufactured devices to provide attenuation, switching and gain equalisation using the established thermo-optic effect. Substantial knowledge has been gained to provide devices with low polarisation dependent loss, which is often a cause of concern for Mach–Zehnder type devices. Fig. 14 is a schematic of a re-configurable dynamic gain equalizer (DGE) based on PLC technology. This is a Finite Impulse Response (FIR) filter where each stage consists of a variable coupler and variable delay line [38]. To manufacture this 5-stage device a relatively high index core (1.5% Δn) was used to allow a minimum bend radius of 2 mm. Fig. 15 indicates the performance of the DGE, where the output attenuation curve closely follows that of the Er^{3+} amplified spontaneous emission (ASE) target compensation vector. Of particular note are the excellent optical properties, such as accuracy (<0.5 dB) and PDL (<0.4 dB). Other external polarisation compensation techniques have

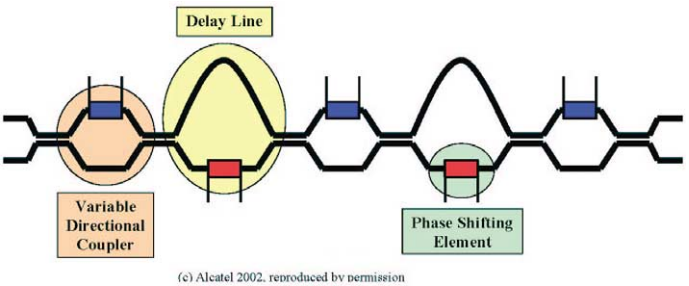
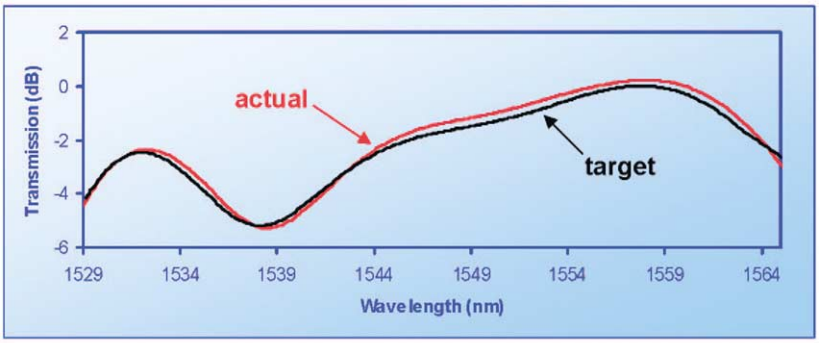


Fig. 14. Illustration of Finite Impulse Response (FIR) filter.



Specification level	Accuracy	Insertion loss	PDL	abs(CD)	Pol GD	RL
Current performance (EDFA target vector)	0.5dB	6.5dB	0.4dB	0.2 ps/nm	0.13 ps	- 51.6 dB

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Fig. 15. Measured performance of Dynamic Gain Equalizer.

been used to try and reduce the induced PLC birefringence [39]. One such polarisation diversity scheme involves a circulator, polarisation beam splitter and polarisation maintaining fibre, which adds insertion loss and is bulky and not cost-effective. By optimising the design and waveguide fabrication AOUK have formed complex thermo-optic devices with relatively low dynamic PDL.

Thermo-optic devices offer excellent performance for discrete devices such as Variable Optical Attenuators (VOAs) and DGE', however, to enable more advanced integration techniques, AOUK have established the integration of PLC's with micro-optoelectromechanical (MOEMs) devices. This provides substantial benefits in relation to integration due to thermal management, power consumption, size and cost. It also provides the necessary basic building blocks to establish more complex design solutions.

The basis of the MOEMs actuator device is to translate electrical signals into mechanical motion. Fig. 16 is an image of an actuator array device for variable optical attenuation. In this configuration the shutter is moved in and out of the free space beam between the input and output channel waveguides. The shutter is connected to a flexible suspension beam that is electrostatically actuated by comb drives. The displacement/voltage characteristic is proportional to the square of the applied voltage. Fig. 17(a) is the attenuation versus voltage curve for a normally closed VOA (i.e., in the blocking stage). This illustrates that the isolation for the micro-opto-electromechanical (MVOA) array is better than 65 dB with a typical value of >70 dB and that there is good grouping of the 8 attenuation curves. Fig. 17(b) provides the measured PDL at the 0, 10 and 20 dB attenuation set points, relative to the base loss for a standard MVOA. The maximum PDL across the C and L transmission band was measured to be no larger than 0.4 dB at 20 dB attenuation.

To fabricate the actuator, silicon-on-insulator (SOI) technology (single-crystal silicon layer) is used [40]. This offers advantages with relation to large-scale manufacture, as it is relatively simple and requires a comparatively small number of process steps. An important requirement is to be able to plasma etch the Si to form deep structures that are accurately controlled and have smooth sidewalls. Localised metal deposition on the shutter is also required to provide high-quality mirrors.

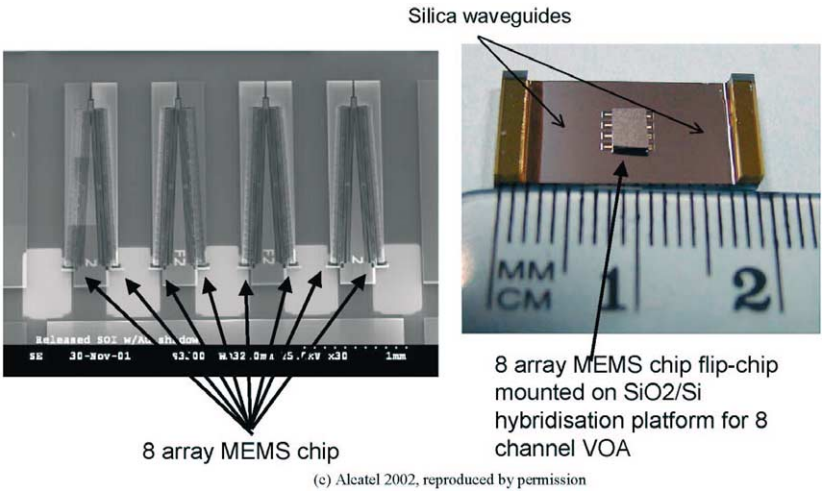

Fig. 16. SEM of actuator array chip and 8 array MEM's chip flip-chip mounted on PLC.

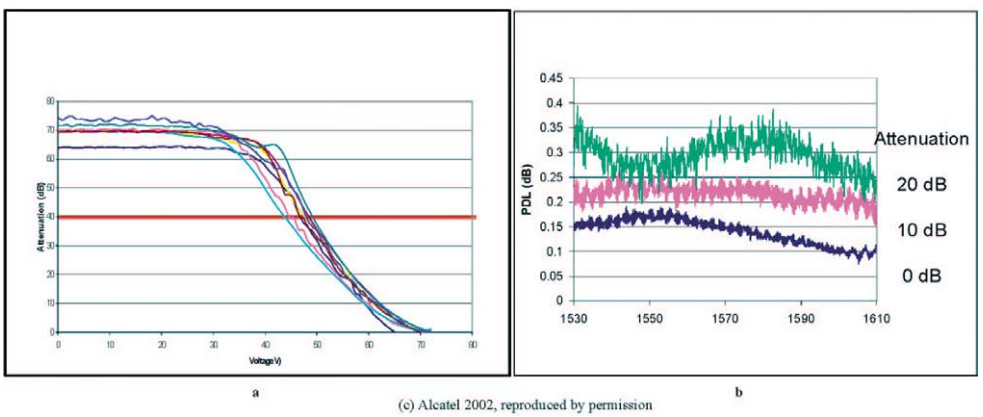

Fig. 17. (a) Attenuation versus voltage curve for normally closed shutter; (b) measured PDL for VOA setting of 0, 10 and 20 dB.

The PLC is fabricated and the actuator is flip chip bonded onto the PLC. To enable this process, high quality deep etching of the PLC and metalisation techniques are used. This enables slots of <20 μm width to be fabricated with sidewall angle of $\sim 90°$. The etch depth of the slot and well is ~ 40 μm. The quality of the facet results in low excess loss across the slot.

High quality single-crystal Si and simple mechanical designs provide extremely reliable components. There is only one potential failure mode for silicon components that can be activated by a combination of moisture and stress. Careful mechanical design and suitable localised packaging can alleviate both of these concerns. Electrical design is also required to prevent electrostatic comb drive levitation [41].

Tap detectors in conjunction with VOAs also offer the ability to interrogate the attenuated signal to provide the network engineer with channel control functionality. Within the optical network this is often carried out by a fibre tap filter, attached to an InGaAS PIN photodiode. AOUK have developed both integrated tap and detector capability. The taps have been specifically designed to provide accurate tap ratio and low PDL in both the express and tap path across the full C and L band. Re-direction of light techniques have also been designed and fabricated to provide on chip detector capability. In a similar manner to MOEMs, flip chip bonding and localised packaging techniques have been developed. Fig. 4 is a schematic representation of the tap array. As has been discussed previously, devices such as tap couplers are PDL sensitive, especially in the tap path where there is only 4% of the light coupled across. PDL management is possible by design and fabrication optimisation. Fig. 18(a) is a typical PDL response for the express paths of an 8-channel coupler array and Fig. 18(b) is the response for the tap path. The average PDL value for the express and tap paths are <0.1 and <0.2 dB, respectively.

Combining all these techniques an 8-channel multiplexer has been fabricated. This incorporates 16 power taps, 16 integrated photo detectors, 8 MOEMs based VOAs and a multiplexer along with integrated drive electronics. This device provides

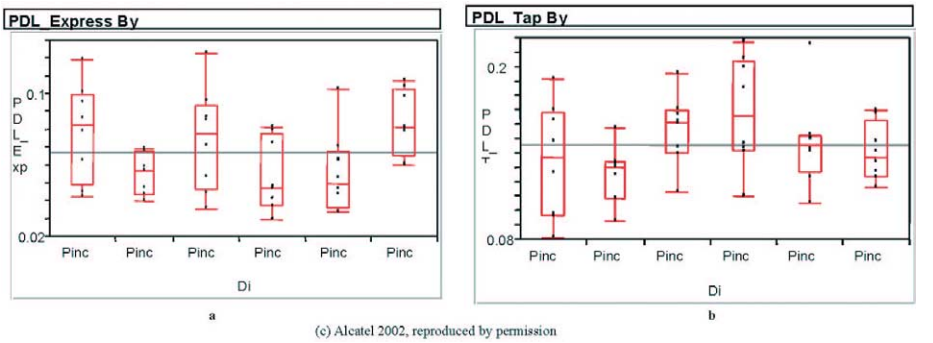

Fig. 18. (a) Measured PDL response for the express path of the tap coupler array; (b) measured PDL response for the tap path of the tap coupler array.

independent control of 8 channels for terminal or add-drop equipment. Device performance has been shown to achieve low loss and low dynamic PDL. In the blocking state the device exhibits more than 40 dB of isolation.

The device incorporates 41 optical functions on a single die and involves 8-fibre input and a single fibre output. The associated electronics are enclosed within the package, to provide 0 to 5 V DC drive control for the attenuation range and also the electrical outputs for the tap detectors. In relation to discrete components this offers substantial savings in component cost, size and inventory levels.

Active and passive integration of an InP Semiconductor Optical Amplifier (SOA) and an 8 channel 50 GHz AWG has also been demonstrated. This type of compact amplified demultiplexer device provides compensation for the small filter loss and the necessary gain to improve receiver sensitivity at the terminal. A 10 Gb/s Non Return to Zero (NRZ) signal has been measured for various input powers and different Optical Signal to Noise Ratio (OSNR). The device exhibited a low distortion penalty with >15 dB dynamic range measured.

5. Conclusion

Developments in PLC technology have led to industry accepted AWG filter solutions. These devices offer many competitive advantages, relating to optical performance and manufacturability. The added advantage of PLC technology is the capability not only to provide discrete components but also to provide the customer with increased functionality through hybrid integration of both passive and active devices. At AOUK, developments have taken place to provide a suite of discrete components, which can be used to form the basic building blocks for these advanced structures. Components have been developed which bring advantages with regards their commonality on the same platform and which also exhibit the required optical performance. MOEMs technology has been developed which is compatible with PLC solutions, providing compact, low power integrated VOA arrays. AWGs have been integrated with SOA devices for amplified demux solutions. Further integration techniques have led to integrated tap and photodetectors on the PLC. Thus, 41 optical functions for multiplexing, attenuating and interrogating the optical signal have been demonstrated. This ability to mix and match, in a production environment a variety of technologies and functions with the excellent properties of the silica PLC platform provides a future proof approach to meet the component requirements for the ever demanding optical telecom system.

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