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A Framework for the Evaluation of Distributed Control Systems in Industrial Control Applications

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ABSTRACT

The research develops a test-bench and framework to evaluate distributed control systems (DCSs) against industrial control system requirements. A real-time hardware-in-the-loop (HIL) test-bench and framework has been used for the evaluation of a DeltaV M3 DCS from Emerson Process Management. The test-bench measures: process control behaviour including overshoot and settling time; and I/O throughput, latency, and jitter for analog, digital, Modbus serial and OPC over Ethernet. The DCS successfully controls a real-time Matlab simulation model of a Nuclear Power Plant (NPP) steam generator, with a maximum water-level overshoot of 4.20%. The evaluated DCS has I/O throughput between 1.06 and 5.05 Hz, and latencies between 72 and 310 ms. The OPC over Ethernet is the most deterministic I/O channel, but has the lowest throughput. The test-bench and framework enables the evaluation of new technology for use in NPP and many other industrial control applications.

Keywords: Evaluation distributed control system nuclear power plant hardware software test-bench, framework, hardware-in-the-loop simulation.

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NOMENCLATURE

AC	Alternating Current
AECL	Atomic Energy of Canada Limited
AI	Analog Input
AI/O	Analog Input and Output
AO	Analog Output
BPS	Bits per Second
CANDU	Canadian Deuterium Uranium
CNS	Canadian Nuclear Society
CNSC	Canadian Nuclear Safety Commission
CTS	Clear-to-Send Signal in an RS232 Communication
DC	Direct Current (Continuous Current)
DCS	Distributed Control System
DI	Digital Input
DI/O	Digital Input and Output
DO	Digital Output

EIA	Electronic Industry Alliance
FF	Foundation Fieldbus
FF-HSE	Foundation Fieldbus High Speed Ethernet
FFT	Fast Fourier Transform
FPSS	Full Power Steady State
HIL	Hardware-in-the-Loop
I/O	Input and Output
IAEA	International Atomic Energy Agency
IEC	International Electrotechnical Commission
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
IETF	Internet Engineering Task Force
LOCA	Loss of Coolant Accident
MPC	Model Predictive Control
Mbit	Megabit (One Million Bits)
NPP	Nuclear Power Plant

NRC	U.S. Nuclear Regulatory Commission
NSCA	Nuclear Safety and Control Act (1997, c. 9)
NSERC	Natural Science and Engineering Research Council of Canada
OLE	Object Link Embedding
OPC	OLE for Process Control
OPG	Ontario Power Generation
ORNL	Oak Ridge National Laboratories
OSI	Open Systems Interconnection
PID	Proportional Integral and Derivative
RS232	Recommended Standard 232 for Serial Communication
RFC	Request for Comments (organized by the IETF)
RTS	Request-to-Send Signal in RS232
RX	Received Signal in a Communication System
SCADA	Supervisory Control and Data Acquisition
SG	Steam Generator
SGLC	Steam Generator Level Control

SGPC	Steam Generator Pressure Control
SIL	Safety Integrity Level
TX	Transmitted Signal in a Communication System
UNENE	University Network of Excellence in Nuclear Engineering
UTSG	Upright Tube Steam Generator
V&V	Validation and Verification
VAC	Volts AC
VDC	Volts DC

1 INTRODUCTION

1.1 Background

Nuclear power plants (NPPs) have many processes that need to be controlled, ranging from redundant flow valves to high-speed steam generator flow. These control needs can be met by instrumentation, measurement, and control system products from companies such as ANP, ABB, Allen-Bradley, Foxboro, Hitachi, Honeywell, Invensys, ICS Triplex, Rockwell Automation, Schneider, Triconex, Westinghouse and Yokogawa. These companies provide products based on state-of-the-art technologies including sensors, actuators, communication networks, instrumentation, and distributed control systems (DCSs) to meet the specifications of control loops in the plant.

A distributed control system is defined by multiple geographically distributed controllers connected for the purpose of performing coordinated control on one or more systems. Distributed control systems can distribute control functions among multiple physical controllers. Processes with fast dynamics may require dedicated controllers to minimize communication delays. Other controllers may be responsible for hundreds of slowly varying variables in a cluster of related control loops. Control algorithms are designed in one of the five standard IEC 61131-3 programming languages: ladder logic, function block diagram, structured text, instruction list, and sequential function chart. These systems communicate with the rest of the plant equipment and processes using standard and or open communication networks and protocols including Foundation Fieldbus, Profibus, and OPC over Ethernet.

Distributed control systems are the state-of-the-art in industrial control. Many industries have used DCSs to increase reliability and decrease design and development costs. The NPP industry differs from other industries in two important aspects: regulation and safety. The Canadian nuclear power industry is heavily regulated by the Canadian

Nuclear Safety Commission (CNSC). The licensing of a NPP by the CNSC, under the Nuclear Safety and Control Act (NSCA) of Canada, requires detailed control systems design documentation and commissioning procedures[1].To employ DCSs in NPP, DCSs must be evaluated against NPP specific requirements and CNSC regulations.

1.2 Motivations

Although DCSs have been used in other industries, they have not been very widely used in nuclear power plants. Nuclear power plants have many special requirements for their control systems, including a heavily regulated certification process. Unfortunately, there are no well accepted testing frameworks for evaluating DCSs for nuclear power applications. The motivation and focus of this thesis is to develop a framework for evaluating the applications of DCSs in NPPs.

Distributed control systems are well suited to the applications in NPPs: firstly they solve the problem of existing control system obsolescence [2][3], and secondly, DCSs provide the additional functionality required to achieve NPP operational improvements [4]. As of December 2007, Areva, a major NPP vendor, had 7 projects underway in the United States employing Teleperm XS and XP DCS technology [5].

The applications of DCSs in NPP designs must undergo rigorous testing, evaluation and certification. The ability of a DCS to receive plant inputs, to perform control calculations, and to generate outputs are the key to its successful deployment. The DCS I/O throughput, throughput jitter, latency, and latency jitter are four important performance measures. The percent overshoot and steady-state accuracy of a DCS controlled loop provides a measure of the overall capability of the system. The behaviour of these parameters must be characterized in order to compare DCS against existing control systems. While the DCS vendor may provide some key DCS properties not all parameters are available e.g. I/O channel latency.

In many ways a NPP is similar to other industrial plants such as petrochemical or fossil fuel power plants. A plant has hundreds of complex processes that need to be monitored and controlled, each with unique dynamics. For example, an upright tube steam generator (UTSG) and a natural gas fired boiler both exhibit dynamics on the scale of minutes. The core flux control of a nuclear reactor and the thickness control of a paper mill both exhibit dynamics on the scale of milliseconds [6].

In industries other than NPPs, DCSs have been successfully used to implement instrumentation and control (I&C) strategies. However, in NPP the heavy regulation of the electricity production process, not the product, has made the nuclear industry slow to adopt new technologies including DCS. The thesis aims to develop a test-bench and framework for the evaluation of DCSs. The evaluation of DCSs is an important step towards the adoption of DCSs in NPPs.

1.3 Problem statements

To determine the suitability of DCSs for NPP applications, and in order to meet licensing requirements, DCSs must undergo validation and verification (V&V) throughout the entire life-cycle of the plant. Verification ensures each phase of the design meets the imposed requirements. Validation ensures the design meets functional, performance and interface requirements. Final commissioning tests ensure that the DCS was correctly installed and performs according to the vendor requirements. No well accepted methods exist to conduct V&V for DCS use in NPPs.

The thesis deals with the issues in designing a test-bench and framework with which DCSs can be evaluated as a component of NPP design. Control system requirements are provided by the NPP vendors. The regulatory bodies provide methods for determining the suitability of DCSs for NPPs [7]. The methods of analysis are thorough, though time consuming and require the judgment of human experts. Firstly, converting these processes into systematic V&V tests would enable more complete evaluation of DCSs for

their use in a NPP. Lastly, the evaluation of DCSs must be conducted in an independent manner, and at arm's length from DCS vendors.

The functional and performance requirements of NPP processes are described in terms of system behaviour such as I/O throughput and latency. To accurately conduct V&V tests the test-bench and framework must allow for real-time evaluation of DCS behaviour. The abilities of the framework should reflect the testing recommendations of local NPP regulators and those of the international NPP community. The applicable testing recommendations are described in detail in Chapter 2. The scope of the criteria for the application of commercial grade control equipment in a NPP is selected from the published recommendations of AECL, the NRC, and IAEA's technical working group on NPP control and implementation, in particular [4], [7] and [8]. The criteria are selected based on their suitability to be measured, for example "acceptable performance record" is a criterion which can't easily be measured.

1.4 Objectives of the thesis

The objective of this research is to design and construct a test-bench and to develop a framework with which DCSs can be evaluated against NPP requirements. The test-bench and framework should include the capability to assess the following DCS properties:

- I/O throughput, latency,
- I/O jitter, and
- Overshoot and settling time of PID control loops.

The developed framework must allow the integration of simulated processes with the hardware DCS under test. The test results should be automatically processed into a list of DCS properties for comparison against evaluation requirements.

1.5 Scopes of research

The scope of this research is to evaluate DCS I/O and process control. The selected I/O is digital, analog, serial, and OPC over Ethernet. High-speed serial and Ethernet I/O are two of the many possible I/O available from DCS vendors. PID control is chosen because it is a commonly used control strategy in industrial applications. The test-bench and framework may be used to evaluate any DCS that has at least one I/O interface. A serial interface is required to conduct process control tests. The reliability of the DCS hardware is beyond the scope of the current research. Calibration of the test-bench, including measurement overhead, the reliability of timing sources, and the quality of the software used to construct the test-bench is not considered. The throughput, latency, and jitter of the I/O interfaces is considered. The percent overshoot and settling time of the tuned PID loops is also considered.

1.6 Contributions

The thesis contributes a hardware test-bench and software framework for evaluating DCSs against NPP requirements. The hardware test-bench supports the following I/O interfaces:

- analog 4-20 mA,
- digital 25V DC,
- Modbus over serial RS232,
- and Ethernet over twisted pair copper.

The software framework supports the following features:

- real-time sampling of DCS I/O interfaces,
- real-time tests using National Instruments (NI) LabWindows/CVI,

- interfacing of a real-time Matlab model to the DCS,
- and automated analysis of test results.

Validation and verification tests have been written in ANSI C using NI LabWindows/CVI, and Matlab M-Files. The DCS component of the tests may be written in any of the languages supported by the vendor. The framework and test-bench may be used to interface to any DCS that supports the hardware test-bench I/O interfaces. The automated analysis of the test results was carried out by a suite of Matlab functions.

1.7 Organization of the thesis

Chapter 2 presents the concept of distributed control systems and their potential applications in NPPs. The literature review looks at the requirements that must be met to deploy DCSs in NPPs; from the position of a regulator and that of a NPP I&C system designer. The literature on DCS evaluations for NPP applications has been reviewed.

Chapter 3 describes the test-bench and framework. The test-bench and framework are designed to evaluate I/O and control performance. Four I/O channels are tested specifically: analog, digital, serial, and Ethernet I/O. An upright tube steam generator (UTSG) level control (SGLC) in a CANDU 6 plant is selected as the NPP process to be tested.

Chapter 4 examines each experiment in detail, including an outline of the test, and the results. The Emerson Process Management DeltaV M3 DCS I/O and control are tested. Four I/O channels and one PID control system are examined.

Chapter 5 presents the analysis and evaluation of the tests and their results. The experiments in Chapter 4 are summarized and the performance between I/O channels is compared. Finally, future work and potential extensions of the research are discussed,

including future DCSs and I/O channels to test, and additional performance criteria to measure.

2 LITERATURE SURVEY

This chapter provides general information on DCSs, their applications, in particular to NPPs, and the evaluation of DCSs for use in NPPs. First, the state-of-the-art in DCS is examined including a summary of supported I/O interfaces for 12 DCSs. The differences between DCS and conventional control systems are examined. Next, literature covering DCS applications in NPP are examined, including what should be evaluated, and how it should be evaluated. Presented last is a summary and outline of the methods chosen for the thesis.

2.1 Definition and history of distributed control systems

Distributed control describes a control strategy where multiple connected controllers perform coordinated control of one or more sub-systems. In DCSs the controllers are not centrally located, but are distributed throughput the system. Each sub-system is controlled by one or more controllers. Traffic signal control is an early example of distributed control [9]. All attributes of the definition are present: multiple connected controllers, coordination, and control of one or more sub-systems. The concept of distributed control is not new. Veterans of the process control industry employed distributed control well before the commoditizing of the microcontroller [10]. The evolution of microcontrollers and high-speed data networks sparked industrial experiments such as Honeywell's "Experimental Distributed Processor" [11]. At the same time, the nuclear industry outlined its requirements for distributed computer control of future NPPs [8]. Over the years many industries have adopted DCSs, including automotive [12], pulp and paper [13], oil and gas [14], power generation [15] and pharmaceutical [16]. The nuclear industry lags behind in the adoption of DCS technology. New DCS technology can provide many benefits to the NPP industry including improved plant operation, and decreased maintenance costs [2, 3].

2.2 Distributed control systems: A state-of-the-art review

DCSs encompass all the traditional aspects of supervisory control and data acquisition systems (SCADA) including I/O, hardware, controllers, human machine interfaces (HMI), networks, communication, and software. Distributed control systems differ from traditional control systems in five important aspects. Distributed control systems provide the following features over traditional control:

- networked with plant systems,
- networked with other DCSs,
- networked with actuators and sensors,
- advanced hardware redundancy, and
- advanced control design software.

The first three differences between DCSs and traditional control systems are shown schematically in Figure 2.1 and defined in sections 2.2.1 and 2.2.2. The last two points are defined in section 2.2.3 and 2.2.4 respectively.

2.2.1 Networked with plant systems and other DCS

Networked DCSs provide process variables to the plant alarm management expert system [17] or NPP balance of plant software [18]. The deregulation of the Canadian power market has forced competition among energy suppliers. Nuclear power plants will use plant efficiency and plant balancing to increase their competitiveness. In traditional control systems multiple disconnected controllers are used to operate one plant. Balance of plant using traditional control systems is achieved through the use of additional sensors and off-line plant efficiency analysis. Additional sensors are used to measure key process variables. The collected data is analyzed to determine the efficiency of the plant and each control loop.

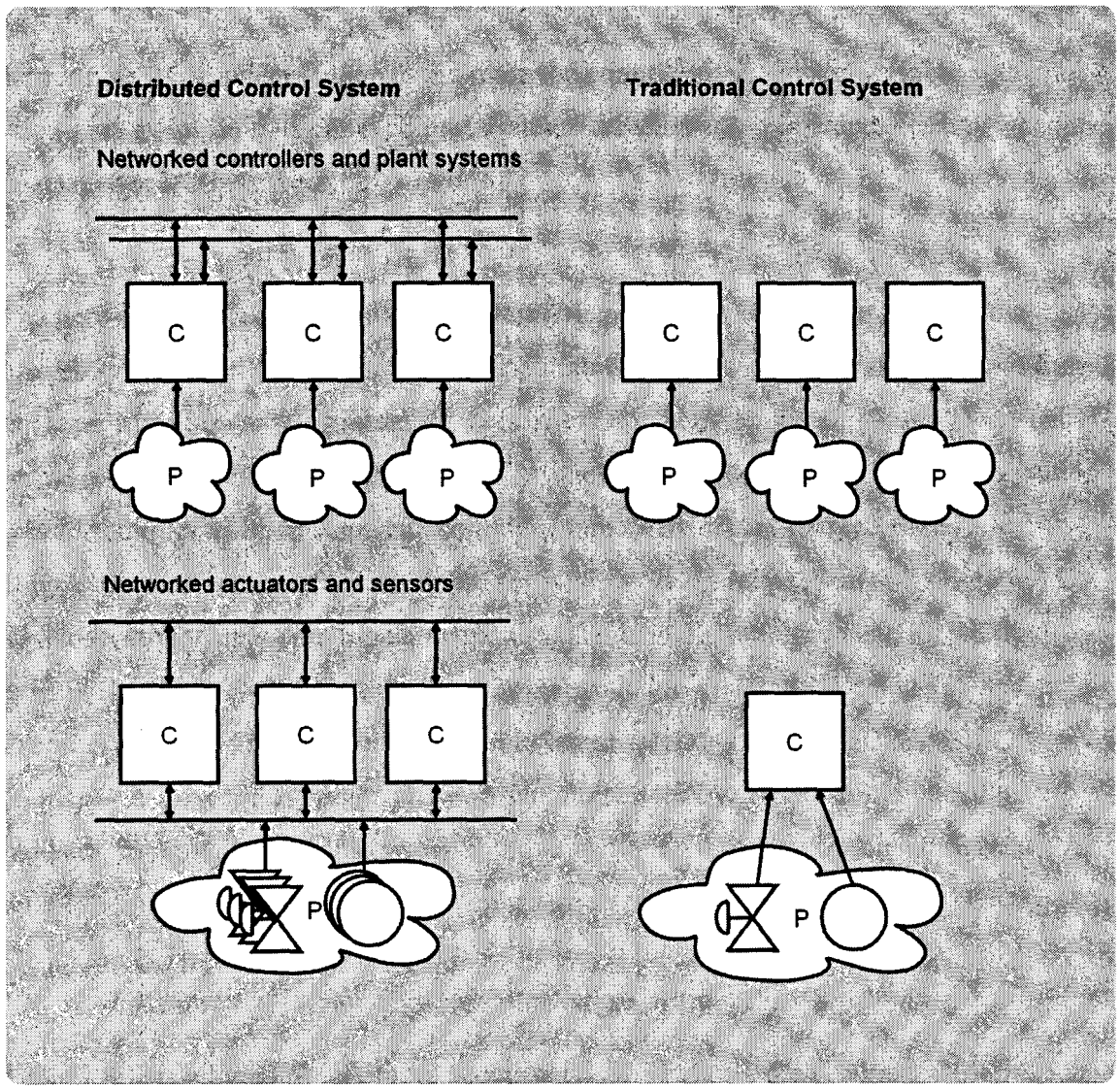

Figure 2.1: Networked DCS

2.2.2 Networked sensors and actuators

Networked actuators may be controlled by one or more DCSs. If a controller failure is detected, a backup controller may take over the control action. In a Foundation Fieldbus (FF) network, each DCS is a link active scheduler (LAS). A primary LAS is responsible for arbitrating communication on the FF segment. During the failure of the primary LAS, other backup LAS may take over the task of bus arbitration [19]. Should all DCS LASs

fail, the control may be delegated to a LAS in either the valve or sensor. The valve and sensor operate in a closed-loop to maintain the control of the process variable at the last known set-point. In traditional control systems the control of the process ceases when the controller or I/O interfaces fail.

The networked DCSs, sensors and actuators use open network protocols that allow integration between all levels of plant functioning. The full integration of the plant from the sensor level up to the operator HMI is offered by both the "Experion PKS" system from Honeywell [20] and the "PlantWeb" system from DeltaV [21]. This full integration is made simpler by open standards communication networks. Open standards communication networks are important for NPPs to avoid reliance on any single vendor. Vendors provide networks based on open standards including Ethernet (IEEE 802.3), Serial (EIA RS-232-C, EIA 485, EIA 422), Foundation Fieldbus (IEC 61158), and Profibus (IEC 61158). Distributed control system solutions employ TCP/IP (RFC 793/RFC 791) over Ethernet, a proven technology used by the telecommunications industry, to provide reliable network communication. All major vendors provide TCP/IP over Ethernet as the backbone of their plant-wide network (c.f. [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31]).

Table 2.1 lists all the I/O interfaces supported by the major DCS vendors, while

Table 2.2 gives a comparison of supported I/O interfaces for each major DCS vendor. The tables are derived from vendor datasheets (c.f. [21]-[31]). For each entry in Table 2.1, example applications in NPP are proposed.

Table 2.1: I/O interfaces

Technology	Description	Application in NPP
Analog control over	• Standard industrial analog control	• Differential pressure transducers for UTSG

Technology	Description	Application in NPP
4-20 mA lines	• Line break detected with 0 mA • Signals vary between 4-20 mA	• Out-of-core and in-core flux detectors • Thermocouples for coolant temperature • Flow valve control
Digital I/O at 25 VDC	• Digital I/O is employed to indicate one of two binary states, either on or off.	• Relay controlled logic
HART over 4-20 mA control	• Digital protocol using 4-20 mA lines	• Valve configuration and diagnostics
Profibus for process automation (PA)	• Supports intrinsically safe installations • Designed by Siemens	• Flow meters • Remote I/O
Profibus for distributed periphery (DP)	• Device level fieldbus • Designed by Siemens	• Motor control • Remote I/O
Foundation Fieldbus (FF) H1	• Fieldbus Foundation created in 1994 • Intelligent devices. Local control • Remote diagnostics	• Valve control • Flow measurements • Thermocouples
Modbus RTU/ASCII	• Industry standard for over 30 years • Serial communication • Employed widely	• Remote I/O
Profinet CB, RT, IRT	• Designed by Siemens • Protocol running on Ethernet	• Reactor control • Moderator control

Technology	Description	Application in NPP
	• Hard and soft real-time.	
OPC Client/Server	• Designed by Microsoft • Based on OLE and DCOM.	• Enterprise data gathering from DCS
Ethernet/IP	• Ethernet based • Implements Common Industrial Protocol (CIP)	• Remote I/O • Motor control • Operator HMI • Heating, ventilation and cooling (HVAC)
Ethernet over copper	• Cost effective networking technology • Widely deployed networking infrastructure	• Plant-wide automation and integration • Enterprise resource and planning networks
Ethernet over fibre	• Ethernet adapted to a fibre optic physical layer	• Systems where EMI and noise are too high to run standard copper cables
Ethernet over wireless communications IEEE 802.11a/b/g	• Ethernet adapted to a radio physical layer	• Non-critical, non-safety, enterprise data
AS-i	• Actuator Sensor Interface • Low cost, multiple device, two wire network	• Sensor networks • Push-buttons • Switches
CANBus, CANOpen	• Controller area network (CAN)	• Controllers to controllers • Remote I/O
DataHighway (DH), DH+, DH485	• Local area network • Plant floor applications	• Operator HMI

Technology	Description	Application in NPP
DeviceNet	• Based on CAN	• Pneumatic valves • Controllers to controller • Remote I/O
ControlNet	• Real-time control network. • Unit configuration and programming	• Controller networks
LON or i.LON	• Building control	• Fans • HVAC • Motor control • Lighting

Table 2.2 provides a summary of the DCSs and their supported I/O interfaces. Each row in

Table 2.2 is a state-of-the-art DCS from a different vendor, while each column is one of the available I/O hardware interfaces.

Digital and analog I/O can be categorized as first generation field-buses, providing one-directional communication using current or voltage levels. Digital and analog I/O is heavily used in the industry.

HART I/O is a small step forward from current sensed analog values. It provides binary data, encoded as FSK, on top of 4-20mA signals. The controller can choose to interpret

this extra data. The additional HART data may include status information, sensor integrity, and error ranges.

A number of mature standards are based on RS232, RS422 or RS485 (IEC-485). These systems employ protocols on top of the standards defined transmissions. Protocols include Modbus RTU or ASCII, DH-485, and Profibus DP. Modbus is a traditional master-slave protocol, while DH-485 and Profibus DP are more complex involving master voting, token passing, and multiple masters with multiple slaves.

Profibus PA is a variant of Profibus DP and provides connectivity to intrinsically safe areas. Siemens was the initial developer of Profibus, which is now an IEC standard. Profibus DP is targeted at factory automation, while PA is for process automation.

Datahighway (DH) and Datahighway+ (DH+) are two proprietary protocols developed by Allen-Bradley. Both DH and DH+ should be grouped with DH-485. These protocols are used by Allen-Bradley systems and 3rd party manufacturers to interface with Allen-Bradley PanelView HMIs.

Foundation Fieldbus (FF) is one of the newer fieldbuses. FF devices provide diagnostics, status updates, and the ability to control actuators on the same segment. While FF is not a high data-rate bus there is a high-speed version i.e. Foundation Fieldbus High-Speed Ethernet (FF HSE).

Ethernet provides the basic format for transporting network data. Important physical mediums include copper, fibre and wireless. Copper is a low cost wiring solution with high data rates. Fibre provides higher data rates than copper with EMI immunity, though at higher cost. Wireless Ethernet provides flexibility not previously possible. Wireless Ethernet devices can be placed on mobile processes, provide positional feedback using GPS, or bridge the gap between areas where wiring is not physically possible.

There are a number of protocols that can be used over Ethernet. These protocols include TCP/IP and UDP/IP, providing reliable connection oriented transmission and unreliable streaming transmission. Protocols built on top of TCP/IP and UDP/IP include OPC clients and servers, Simple Network Management Protocol (SNMP), Hyper Text Transport Protocol (HTTP), Ethernet Industrial Protocol (EthernetIP), and parts of ProfiNet CBA and RT. Ethernet is heavily used in office networks and major telecommunications infrastructure. Ethernet however is a non-deterministic protocol using a random back-off algorithm (CSMA/CD) to arbitrate bus utilization. Siemens' ProfiNet IRT mitigates some of Ethernet's non-determinism by introducing token passing between all connected systems.

Echelon Networks' LON is a standardized ANSI/EIA 709.1 communication system. It has data rates in the range of 78 kbps to 1.25 Mbps. The higher data-rates are limited to shorter fixed lengths of cabling. LON provides a complete framework for device configuration and communication. A LON network can be setup as a free-bus system where devices can be connected at any point. LON networks are primarily used for building temperature sensors, lighting, and HVAC.

Controller Area Network (CAN) bus was initially developed in 1983 by BOSCH as an internal vehicle network. The protocol and medium quickly became an accepted standard in the automotive industry. CANOpen is the standard defining the complete framework from software tools to object attributes for standard devices. CAN bus data rates range from 10kbps to 1 Mbps. CANBus is standardized as ISO 11898.

DeviceNet is a CAN based protocol. It uses CAN messages at the physical and data link layers. It provides master-slave configurations and peer-to-peer communication. Data rates on DeviceNet can range from 125-500 kbps. DeviceNet uses the Common Industrial Protocol (CIP) at the application level. CIP is being integrated into ControlNet and EtherNetIP at the application level, such that common software tools can be used for all three networks.

ControlNet is a deterministic network system with data rates up to 5Mbps. ControlNet International's founding members includes Honeywell and Rockwell Automation. The network is a higher data-rate alternative to DeviceNet, but is not based on CAN. ControlNet can provide dedicated communication resources to a controller. ControlNet implements CIP at the application level.

Actuator Sensor Interface (AS-i) was designed as a sensor bus. The bus interface consists of two wires, one carrying data signals and power while the other is ground. The bus is low data-rate and intended as a low cost sensor network.

Table 2.2: Supported I/O interfaces

Distributed Control System	Analog I/O	Digital I/O	HART I/O	Profibus PA	Profibus DP	Foundation Fieldbus	Modbus RTU/ASCII	Profinet CB,RT,IRT	OPC Client/Server	Ethernt/IP	Ethernet (Copper)	Ethernet (Fibre)	Ethernet (Wireless)	**AS-i**	CANBus / CANOpen	DH/DH+/DH-485	DeviceNet	ControlNet	LON
AB ControlLogix	✓	✓	✓			✓	✓		✓	✓	✓					✓	✓	✓	
ABB 800xA	✓	✓	✓		✓	✓	✓				✓								
ANP Teleperm XP	✓	✓	✓		✓		✓		✓		✓								
DeltaV M3	✓	✓	✓		✓	✓	✓		✓		✓	✓		✓			✓		
Foxboro IA A^2 T940	✓	✓			✓		✓		✓		✓						✓		
Honeywell C300	✓	✓	✓			✓			✓		✓	✓	✓						
ICS Triplex	✓	✓					✓		✓		✓	✓							
Schneider Quantum	✓	✓		✓	✓		✓				✓	✓		✓					✓
Siemens S7-300	✓	✓	✓	✓	✓		✓	✓	✓		✓	✓		✓					
Triconex Tricon	✓	✓					✓		✓		✓					✓			
Westinghouse Ovation	✓	✓	✓			✓			✓		✓								

Distributed Control System	Analog I/O	Digital I/O	HART I/O	Profibus PA	Profibus DP	Foundation Fieldbus	Modbus RTU/ASCII	Profinet CB,RT,IRT	OPC Client/Server	Ethernt/IP	Ethernet (Copper)	Ethernet (Fibre)	Ethernet (Wireless)	AS-i	CANBus / CANOpen	DH/DH+/DH-485	DeviceNet	ControlNet	LON
Yokogawa CS3000	✓	✓	✓	✓	✓	✓	✓		✓		✓						✓		

Table 2.2 contains a "✓" when the I/O interface is directly available on the DCS of safety PLC. We include both DCS and safety PLC as a comparison between two different technologies that have some feature overlap. The DCSs with highest number of available I/O interfaces are Emerson Process Management DeltaV M3 and Rockwell Automation Allen-Bradley ControlLogix. The DCSs with lowest number of available I/O interfaces are the Triconex Tricon and the ICS Triplex. The Tricon and Triplex DCSs are intended for use as safety shutdown systems, while the DeltaV M3 and the ControlLogix systems are designed for process control. The process to certify a DCS for use as a safety shutdown system may affect the number of available I/O interfaces.

2.2.3 Advanced hardware redundancy

Hardware redundancy is the duplication of critical system components with the intent of increasing system realiability by using backups or fail-safe secondary or tertiary components. Distributed control systems are categorized into safety and non-safety related systems. Safety related DCSs have a lot in common with traditional programmable logic controllers including operating on discrete logic functions, but like DCS they are able to communicate over a network. Non-safety related DCS do not perform any regulatory defined safety instrumented functions. Both safety and non-safety

DCS provide advanced hardware redundancy. Safety DCSs may employ hardware redundancy as a requirement of their safety certification, while non-safety DCSs employ hardware redundancy as a method to achieve higher availability.

Redundant controllers have become common practice among DCS vendors. Tricon, a safety DCS from Triconex uses a triplicate set of inputs, which are then voted upon, and passed to a triplicate controller system [23]. The Tricon is used for safety shutdown systems where a high degree of availability is required. The DeltaV SLS 1508 logic solver, a safety DCS from Emerson Process Management, may be configured in redundant controller pairs, with independent power supplies, and redundant communication links [32].

Redundant I/O interfaces are available from all of the major vendors. The C300 controllers from Honeywell can be configured with additional network and I/O modules to provide no single point of failure [33]. The DeltaV provides redundant serial, FF, and Hart I/O configurations; each interface uses a redundant pair of I/O modules [34]. The software developed by Emerson Process Management automatically detects the redundant Delta V I/O configuration, and presents designers with only one I/O interface, but provides additional alarming modes to enable the designer to inform operators of hardware failure.

2.2.4 Advanced control design software tools

The programming languages used to develop control strategies have become standardized and adopted by most DCS vendors. The IEC 61131-3 standard defines five standard languages for use with programmable logic controllers. The five standard languages are: (1) ladder logic, (2) function block diagram, (3) structured text, (4) instruction list, and (5) sequential flow diagram. The logic required to run the plant is written in a standardizing language. The design is therefore independent of the physical hardware

controller. While the languages are not as flexible as writing microprocessor instructions directly, they protect the designer from changes in the hardware. The goal of standardized language is to allow the NPP designers to develop process control functions that can run on any hardware which implements the software standard. Portable control algorithms allow NPPs to migrate control to newer or alternative hardware.

2.3 Application of DCSs in NPPs

The application of DCSs in NPPs has been examined by the academic community, NPP vendors, and NPP regulatory agencies. Each of the three groups provides important and complementary views of the requirements for applying DCSs in NPPs.

Williams and Jouse [35] outline a set of attributes that intelligent control must possess to qualify for being used in the NPP industry. The three main requirements are:

- integration,
- robustness, and
- fault-tolerance.

These attributes are considered high-value attributes for the NPP industry. Integration involves providing a common communication system and human-machine interface for all aspects of the plant. Robustness is the ability to withstand plant disturbances. Fault-tolerance is the ability to perform required tasks despite system faults or design errors.

Yan *et al.* [8], from the perspective of AECL, an NPP vendor, take a more practical perspective, and recommend three general guidelines for the adoption of DCSs:

- integration of all electronic systems in the plant;
- adaptable to changes in technology; and

- compatible with, but not restricted by, the design principles adopted by the utilities and the licensing board.

The U.S. NRC broadens the scope to include all commercial grade equipment, and in [7] the NRC outlines four important requirements in using commercial equipment in NPPs. The U.S. NRC lists:

- special test and inspection,
- commercial-grade survey of supplier,
- source component verification, and
- acceptable item performance record.

The three viewpoints summarize which DCS requirements should be evaluated. The next section details how the DCS requirements should be evaluated and which requirements are considered measurable by the test-bench.

2.4 Evaluation of DCSs for use in NPPs

A framework and test-bench for the evaluation of DCSs for use in NPPs should encompass some or all of the criteria listed in section 2.3. However, not all the criteria can be measured objectively. For example an acceptable performance record is not measured, but instead is recorded and provided by the vendor. Source component verification is carried out by the regulatory body. A test-bench and framework is able to examine the following:

- robustness,
- fault-tolerance,
- integration, and
- special testing,

The robustness of the controller is dependent on the control structure used by the DCS, and it is difficult to determine without thorough mathematical analysis [36][37]. To evaluate the fault-tolerance of the controller or I/O interfaces the test-bench would need to induce faults with the potential to damage the DCS. The fault-tolerance analysis is normally carried out by the vendor with the help of a certification agency such as TUV [38]. The integration of the DCS with the rest of the plant is accomplished through the use of open and standard network protocols as described in section 2.2.2. This thesis focuses on providing a test-bench and framework for testing of the DCS and I/O interfaces.

The International Atomic Energy Agency (IAEA) recommends that any evaluation of DCSs for use in NPPs should consider the problem of obsolescence in NPP I&C systems [2]. Instrumentation and control in ageing NPPs must be replaced. Unfortunately, replacements may not exist. Upgrading to DCSs is made easier if existing NPP sensors and actuators can be used by the newly introduced DCSs. Evaluating the use of legacy I/O, and control loops such as

- analog 4-20 mA,
- digital 25 VDC, and
- PID control loops,

is the key to upgrading existing NPP. In [39], reports from Germany, Finland, Korea, Sweden, and the United States show that validation and verification through the testing of DCSs against functional requirements, including control and I/O behaviour is an important step towards the application of DCS in safety and non-safety NPP processes. In [3] it is strongly suggested that I/O interface

- throughput, and
- latency,

should be evaluated, with particular attention to latencies induced by network protocols.

This framework developed in this thesis is focused on the evaluation of throughput, latency, and jitter for analog, digital, serial, and Ethernet I/O interfaces. The framework

also examines the DCS ability to use PID to control a NPP process, namely steam generator level.

2.4.1 Methods of evaluation

There are several methods to evaluate DCSs in the literature. One group of literature advocates complete simulation, where the DCS is modeled, associated networks are modeled, and performance is estimated through simulation. Another group advocates complete physical construction of the system under test. Each approach has a different set of problems. Model design and simulation is time consuming and error prone, while physical construction of the test system is prohibitively expensive. A review of recent literature presents a middle ground, where researchers have successfully employed hardware-in-the-loop (HIL) to interface and test controller hardware with process models.

Distributed control systems for NPPs have to undergo rigorous testing, evaluation and certification before they can be used in particular applications. To facilitate such a process, simulation models of the entire plant processes and their controllers are being developed [40]. Industrial DCS hardware is designed for generic control tasks and may not be tested or verified against any specific process model. The evaluation of industrial DCSs becomes an important step in adopting DCSs in NPPs.

The evaluation of DCSs has been carried out for specific applications. Manduchi presents the evaluation of DCSs for control of fusion processes [41]. DCSs are evaluated by complete simulation in [42] and [43], but no clear method for modeling the DCSs is presented. Kopetz [44] provides guidelines for partitioning centralized systems into distributed components. Kopetz examines the benefits of distributed systems, including how elementary interfaces between components allow for simpler testing and modeling.

Partitioning systems into simulation and hardware is called HIL. Hardware in the loop designs are adopted in scenarios where a model of the controller is not fully developed, or

when doing so would cause an explosion in the number of simulated variables. Hardware-in-the-loop is an effective way to verify the correct operation of hardware and software before they are integrated into the physical plant. There are many examples of HIL, including the design of traffic signal controllers [45], engine control designs [46], and control software verification on real hardware [47].

The approach taken by the industry follows HIL testing. An HIL framework offers attractive benefits, principally that the most costly component, the plant, is simulated, while the control system under test is the exact hardware to be installed in the plant. In HIL, the hardware functionality can be fully tested against criteria prescribed by a regulator, such as the U.S. NRC criteria of "special test and inspection" [7]. In Canada, new commercial equipment should be tested to meet the criteria of "integration of all electronic systems in the plant" of AECL [8].

2.5 Summary

A review of the existing literature covering the application of DCSs in NPPs suggests that a test-bench and framework should measure I/O throughput and latency. To facilitate upgrading existing NPPs the testing should include legacy I/O interfaces and traditional PID control.

When designing a test-bench the benefits of using HIL are apparent:

- a model of the DCS is not required; and
- low-cost compared to the complete construction of a working model.

A model of the NPP process under test is still required, but this changes less frequently than DCS technology.

In Chapter 3 a framework to test DCSs and evaluate the integration of DCSs in NPPs will be developed.

3 FRAMEWORK FOR EVALUATING DCS

3.1 Introduction

The test-bench interfaces with the DCS using one of the supported I/O interfaces. The framework uses I/O interfaces to communicate with the DCS and measure the property under test. The test-bench framework allows process models to interface with the hardware DCS under test. The test-bench, I/O tests, process control and simulation all operate in real-time. The framework imposes a hard real-time constraint on all operations, for example one second in the simulated process must not take more than one second to compute. Figure 3.1 shows an overview of the complete test-bench and framework, DCS, and engineering workstation.

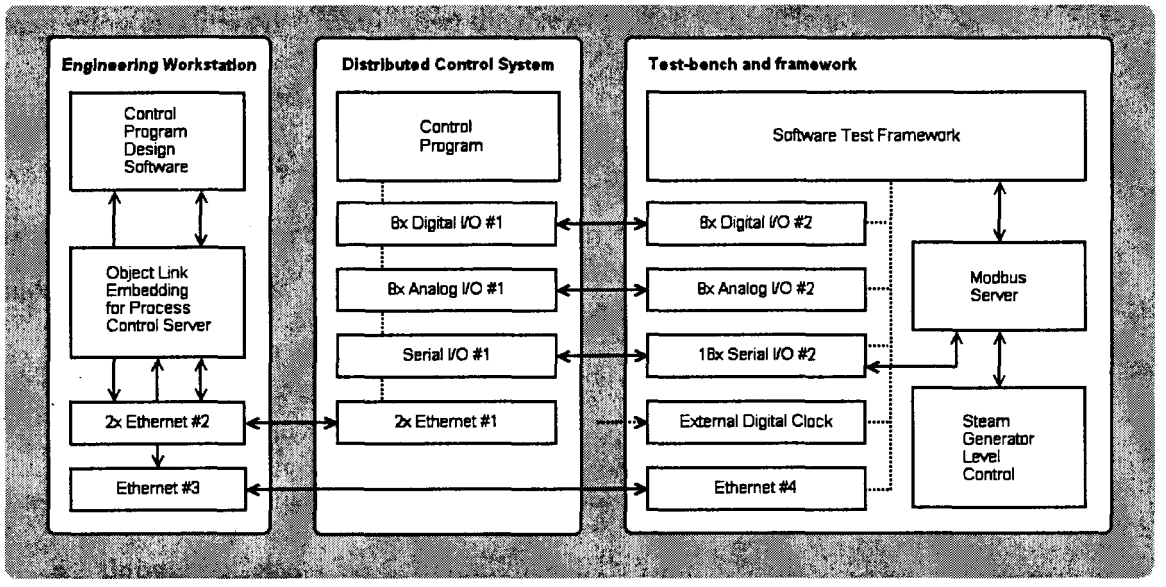

Figure 3.1 Test-bench and framework

3.2 Objectives and scope of the experimental framework

The goal of the research is to develop a system test-bench and framework with which to evaluate DCSs against NPP system requirements. The scope of the framework is DCS I/O and control. The test-bench framework goals include: evaluating DCS I/O hardware, and control algorithms. The DCS hardware and control behaviour is measured using HIL techniques. The DCS and the framework coordinate to conduct a test. For example, the framework generates data, the DCS echoes the data, and the measured time difference between the output and input data is the I/O latency.

3.3 Test-bench requirements

Testing the DCSs hardware against functional requirements, including control and I/O behaviour has been shown to aid in the adoption of DCS in safety and non-safety NPP processes [48]. Section 2.4 recommends the evaluation of legacy I/O in order to facilitate upgrading existing NPP. Evaluating the use of legacy I/O, such as

- analog 4-20 mA, and
- digital 25 VDC,

is the key to upgrading existing NPP. Next the test-bench incorporates the following modern I/O interfaces:

- Modbus serial, and
- OPC over Ethernet.

Lastly in [3] it is strongly suggested that I/O interface

- throughput, and
- latency,

should be evaluated, with particular attention to latencies created by network protocols.

3.4 Framework requirements

In the event of a large process disturbance the response time of the control systems is critical. The time between an initiating event and response is called latency. Latency is a property of a DCS configuration. Throughput is the quantity of data delivered per unit time and is a property of the encoding of the data and the DCS configuration. Throughput limits the number of remote I/O which can be controlled over a data bus. The throughput and latency of a DCS are specific to a configuration. These two parameters are not always constant; their variations with time are referred to as jitter. These properties are important aspects of a DCS, and the test-bench is constructed to measure throughput, latency, and the associated jitter for 4 DCS I/O hardware interfaces: analog, digital, serial, and Ethernet. Digital PID is evaluated as the DCS control algorithm for NPP process control.

The framework requirements are:

- Hardware interfaces
    - DCS System
    - DCS I/O Interfaces
    - HIL Interfaces
- Simulation environment
- Data acquisition
- Data analysis.

Each of the four requirements is examined in detail to determine the set of components required for the test-bench and framework.

3.4.1 Hardware interfaces

The complete physical setup of the components from Figure 3.1 is shown in Figure 3.2, Figure 3.3, and Figure 3.4 including the engineering workstation, DCS, and test-bench respectively.

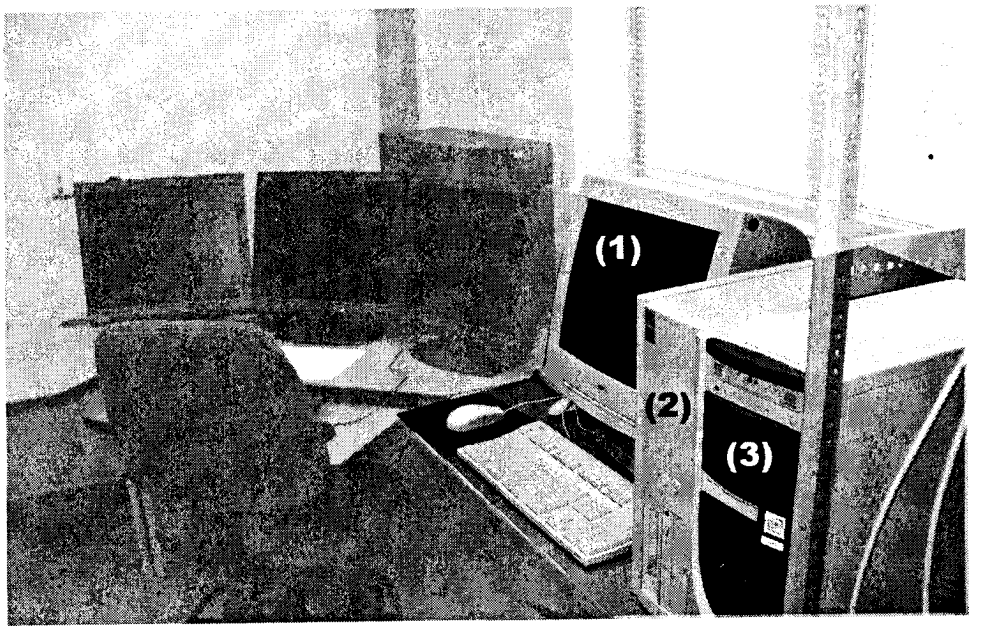

Figure 3.2: Engineering workstation

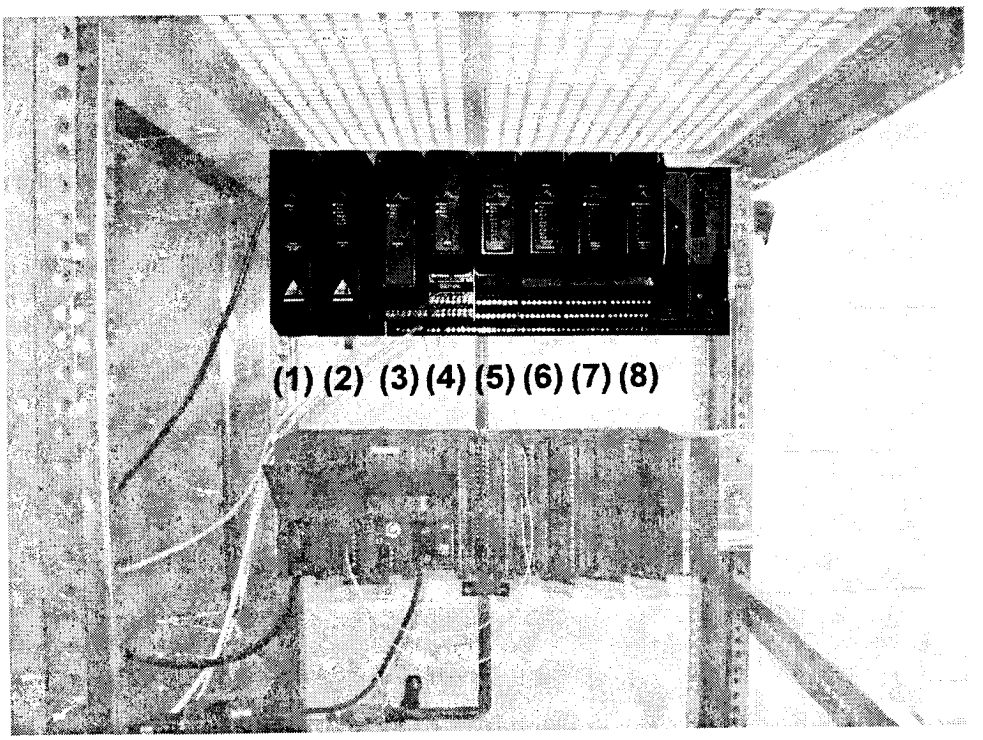

Figure 3.3: DeltaV M3 Distributed control system

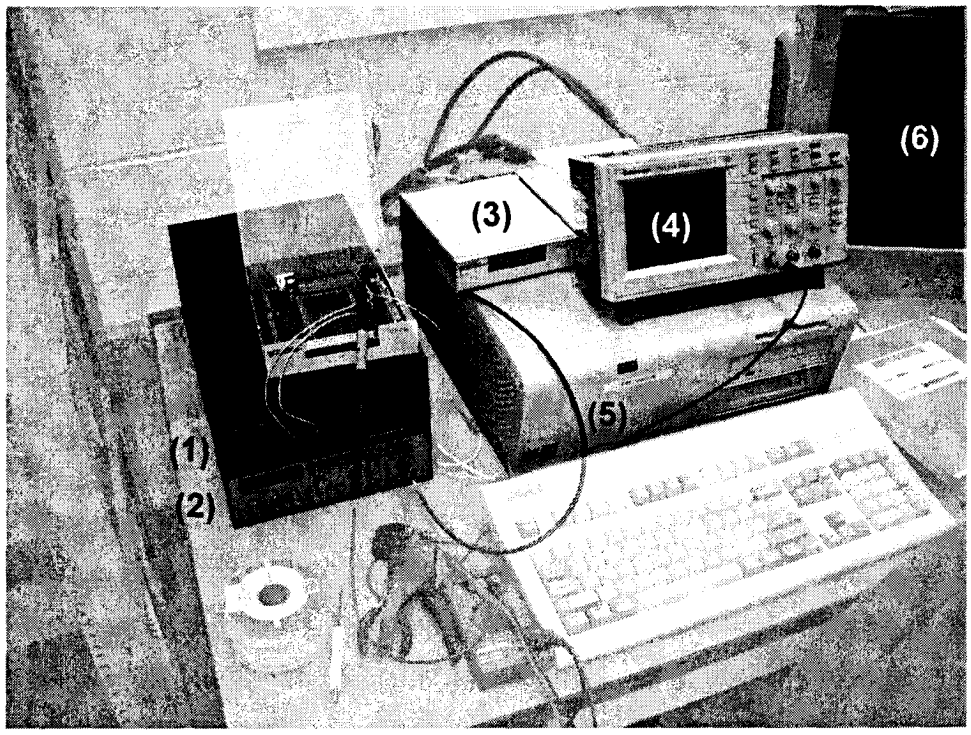

Figure 3.4 Test-bench

3.4.1.1 DCS hardware

The DCS communicates with the plant through I/O interfaces. The I/O interfaces may also be connected to other I/O interfaces. The I/O is considered to terminate at either a sensor or actuator. The DCS and DCS I/O hardware is placed into a industry standard 19 inch wide rack and configured before testing.

The test-bench must be able to perform the following actions: write a test, upload a test to the DCS, and run a test. To program the DCS, the test-bench design must include an engineering workstation. The workstation has the vendor software and hardware required to upload tests to the DCS. The ability to start and stop tests on the DCS is covered by functionality provided by the engineering workstation. Figure 3.2 depicts the engineering workstation setup. The engineering workstation is marked as item (3). The developer sits

facing the monitor marked (1). The computer marked as (2) is a firewall system protecting the engineering workstation from the external network.

3.4.1.2 DCS I/O Interfaces

The DCS I/O hardware is configured using the engineering workstation and vendor software. The DCS hardware I/O module must be installed in the DCS. Figure 3.3 shows the hardware after initial installation. Item (1) is the DCS power supply, provided by the building 120 VAC. Item (2) is the DCS controller. The items marked (3) through (8) are I/O interfaces connected to the internal DCS serial data bus. Item (4) is a Modbus RS232 Serial interface. Items (5) and (6) are analog I/O, and items (7) and (8) are digital I/O. The DCS has two empty chassis slots for future expansion. Items (5) through (8) require 24 VDC bussed field power which is provided by the local power supply marked item (1) shown as the black rectangle on top of item (2) in Figure 3.4.

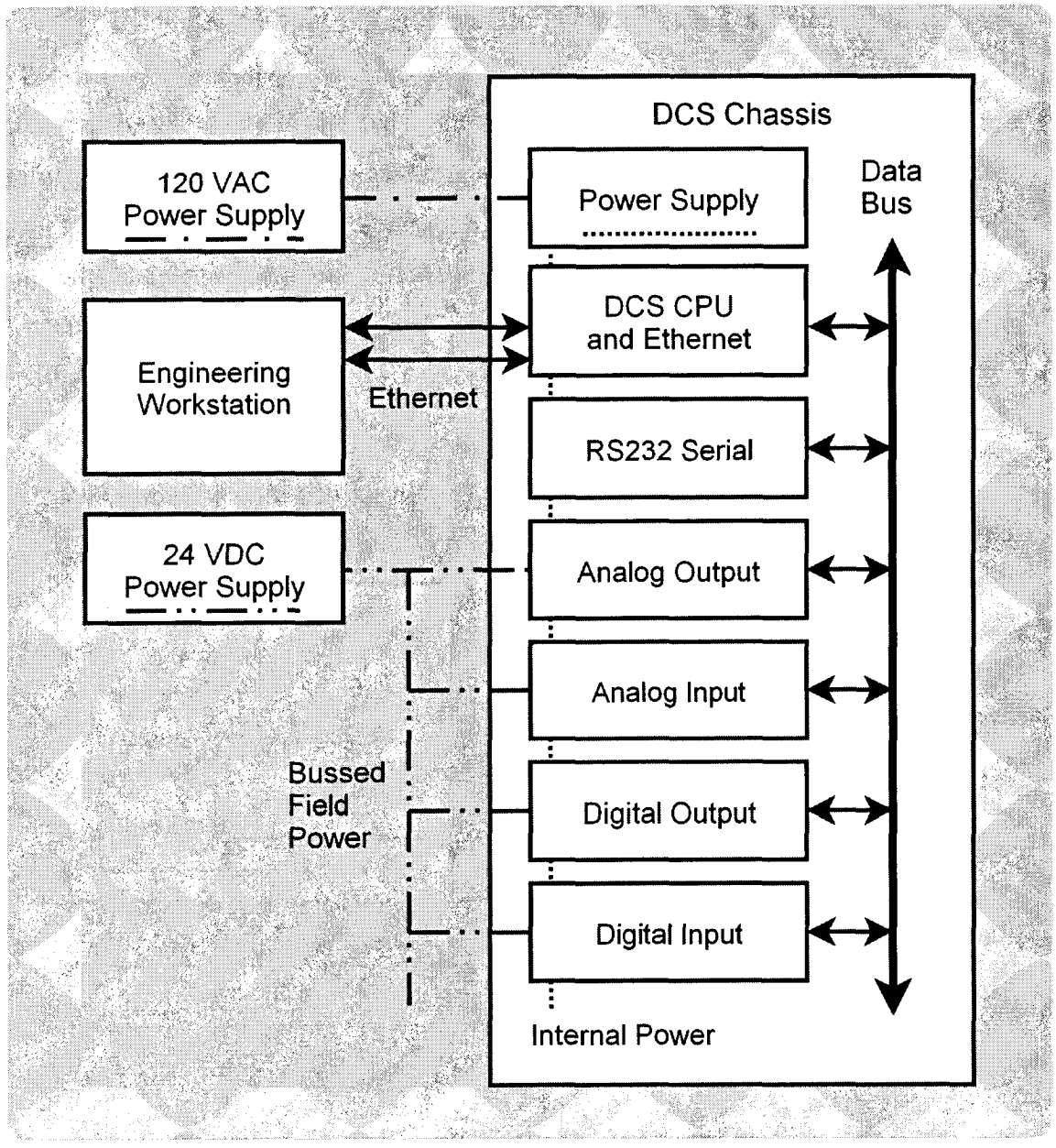

Figure 3.5: Hardware system connections

Figure 3.5 shows all the hardware connections, including power and data networks required to setup the DCS and I/O for use with the test-bench. Figure 3.5 represents logical connections required to setup the DCS components in Figure 3.3.

3.4.1.3 HIL interfaces

For each I/O under test the test-bench and the DCS must have matched hardware. Each I/O hardware has a unique interface to the simulated process. National Instruments (NI) hardware and software is selected as the data acquisition system. The NI hardware and software met all of the requirements for measuring analog, digital, serial and Ethernet data, including hardware sampling and high-accuracy timing. The technical specifications and measurement tolerances of all the test-bench NI interface hardware is listed in the Appendix. For digital I/O a National Instruments 6515 digital input card is used for the test-bench interface.

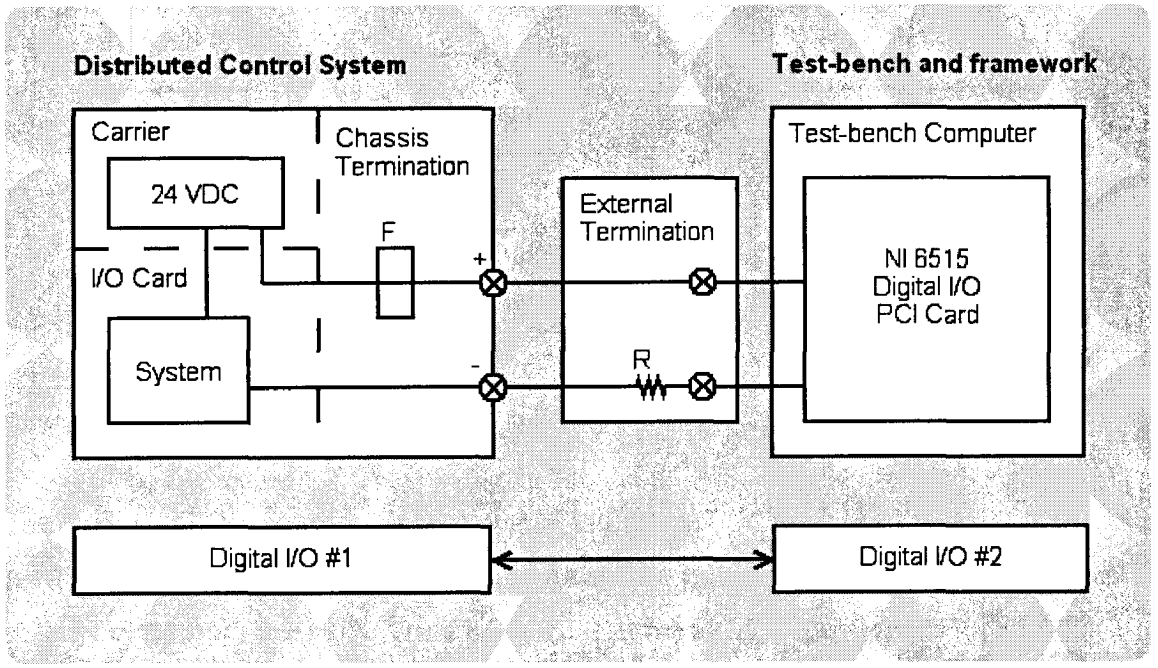

Figure 3.6: Digital I/O HIL interface

The digital I/O HIL interface is represented in Figure 3.6, the 1 kΩ (10% tolerance) current limiting resistor is marked as R, and the DCS chassis termination fuse is marked as F. Since not all DCS chassis termination blocks have a fuse F connected, a resistor, R, is connected to limit current. The external termination box in Figure 3.6 can be seen in the test-bench as item (3) in Figure 3.4. The digital output from the test-bench is configured as a current sink, and the DCS digital input is configured as a current source.

The NI 6515 can configure digital inputs and outputs as either a current sink or source, making it possible to connect to both types of digital I/O configurations.

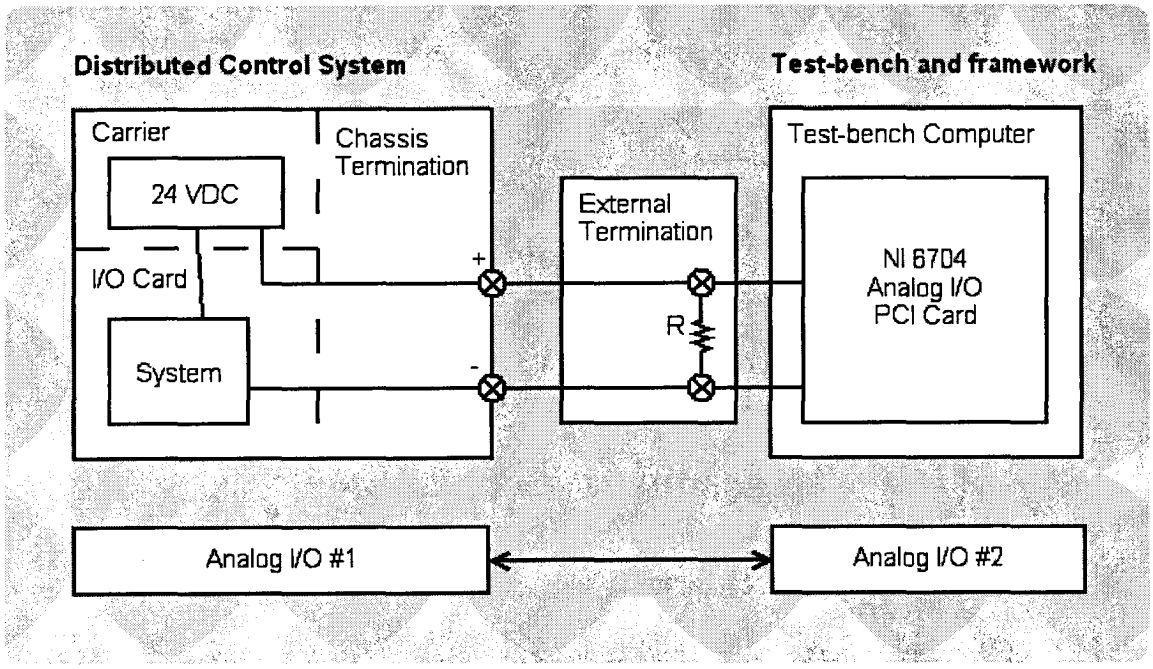

Figure 3.7: Analog I/O HIL interface

The analog I/O HIL interface is represented in Figure 3.7. The analog I/O from the DCS produces a current proportional to the output analog value. The full-scale analog current output ranges from 4-20 mA. The analog value at the DCS is converted from a 12-bit value to a current output. The current applied to resistor R in Figure 3.7 produces a voltage that is then measured by the NI 6704. The resistor R is chosen such that the voltage range matches the measurable voltage range of the NI 6704, which is 0 to 10 V. The resistor R is chosen as 470 Ω (10% tolerance) to produce a full-scale voltage range of 1.88 to 9.40 V.

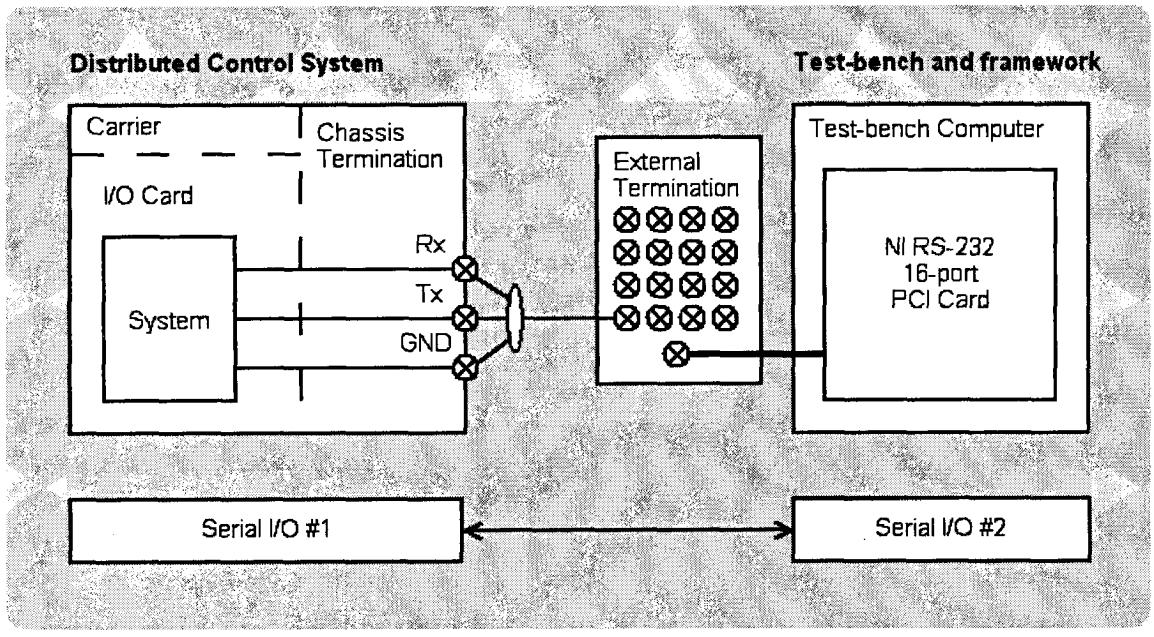

Figure 3.8: Serial I/O HIL interface

The serial I/O HIL interface for one connected serial port is shown in Figure 3.8. The NI RS-232 interface can communicate with sixteen serial ports. The test-bench connector is attached to an external termination board which splits into connectors for all sixteen ports. A serial port on the DCS is connected to a serial I/O port on the external termination by connecting the receive (RX) to the DCS to transmit (TX), and TX at the DCS to RX. The external termination ground (GND) is connected to the DCS GND. Lastly, both sides have the request-to-send (RTS) looped back as clear-to-send (CTS), allowing a three-wire serial interface to function even if one interface doesn't support hardware flow control. Should one side raise the RTS line high, the CTS line will also be raised, allowing the device to transmit whenever it is ready.

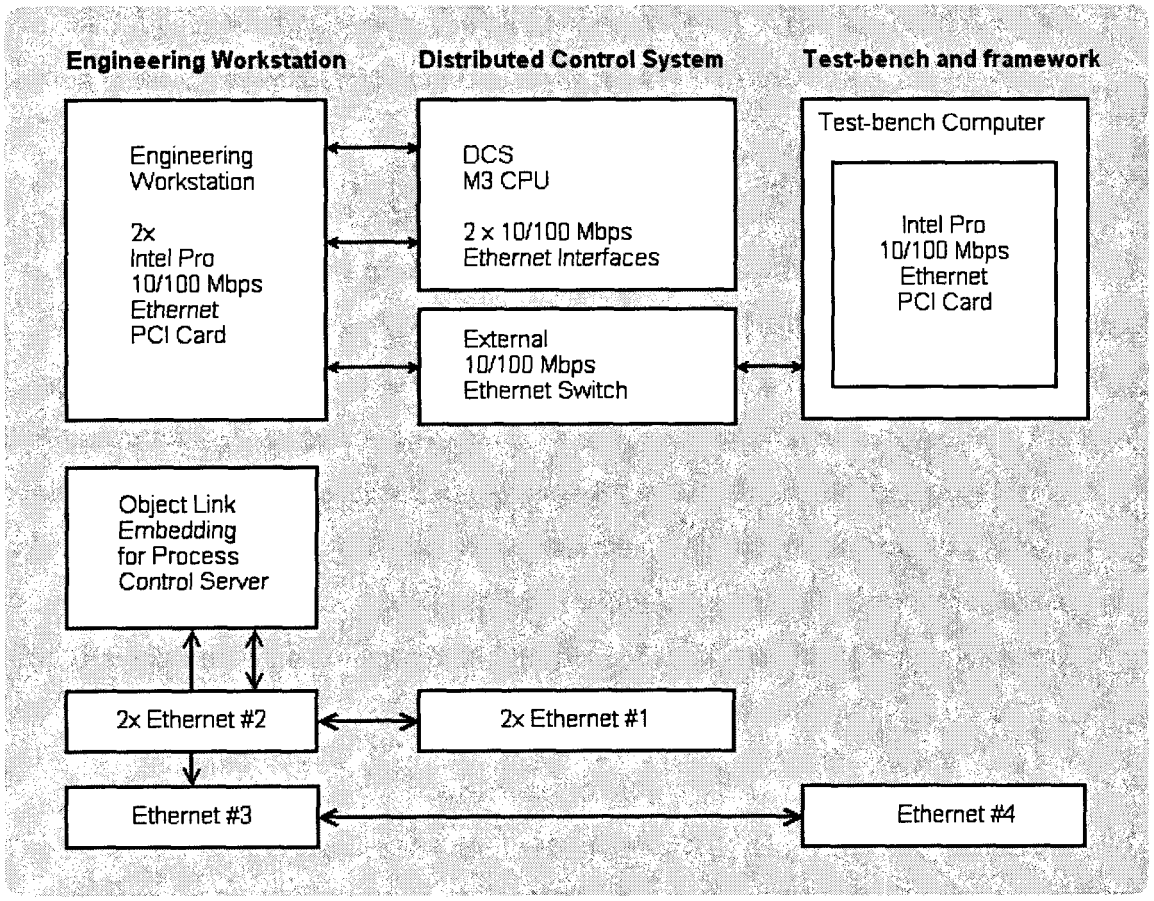

Figure 3.9: Ethernet I/O HIL interface

Figure 3.9 represents the Ethernet I/O HIL interface shown in Figure 3.1. The DCS connects to the engineering workstation, which acts as an intermediary between other systems and the DCS. The test-bench connects to the engineering workstation through a high-speed Ethernet switch. The engineering workstation is running an Emerson Process Management OPC server to provide the DCS status and process values as OPC data. The test-bench uses the OPC DA 2.0 client provided by the OPC Foundation. Process data from the DCS is sent to the test-bench via the intermediate OPC server.

3.4.2 Simulation environment

The test-bench uses a second computer, labeled "test-bench and framework" in Figure 3.1 and marked items (5) and (6) in Figure 3.4, to run tests in real-time. The process is simulated by the test-bench computer. The computer is equipped with a Microsoft

Windows 2000 operating system and NI LabWindows/CVI. The test-bench tests are written in the C programming language using the CVI libraries.

The simulation models are written in Matlab M-file scripts. The framework provides functions for the simulation models to send and receive data from the DCS via the LabWindows/CVI interface. The framework uses a local TCP/IP session to communicate between the scripts and the LabWindows/CVI software. The framework imposes real-time constraints on the simulation. The scripts must update the framework after 100 ms of simulation time has elapsed. If the framework detects that simulation time is not proceeding in real-time it will abort the simulation. The framework uses the 1 ms accurate Microsoft Windows high-precision multimedia timers to determine the elapsed time. The high-precision timers count time using the independently running hardware real-time clock.

The DCS behaviour is captured by the LabWindows/CVI data acquisition software. The software is used to capture data from the I/O channels involved in the test. The captured data is timed using an external trigger provide by a WaveTek signal generator shown as "External Digital Clock" in Figure 3.1 and item (2) in Figure 3.4. Matlab is used to analyze the data off-line. The Matlab analysis is automated and produces plots and values for the dynamic properties.

Manual verification of signal rates and output waveforms is accomplished using a Tectronic Oscilloscope shown as item (4) in Figure 3.4.

3.4.3 Data acquisition

The test-bench is designed to measure throughput, latency, and jitter for each of the four selected DCS I/O interfaces. For each of the four I/O interfaces we measure the property of one I/O active and all I/O active to determine the behaviour of the I/O card when fully

active. The test-bench is also designed to evaluate the DCS control of a simulated process.

3.4.3.1 Throughput

Throughput is the rate of transmission of a communication channel. The throughput is dependent on the encoding of the data. The throughput of DCS I/O is an important factor in deciding which process variables to assign to a given I/O channel. Multiple variables from a slowly changing process can be assigned to a single DCS, but variables for a fast dynamic process may utilize all of the DCSs' resources. The throughput tests conducted with the test-bench consist of two steps:

1. a program is written for the DCS which generates a maximum output throughput for a specific I/O channel; and
2. a program is written for the DCS which generates a known throughput.

Both the maximum and known throughput programs are executed and the output is recorded. The known throughput is used when calculating the throughput jitter. The Matlab analysis scripts use the expected throughput to calculate jitter e.g. using a known value to calculate an unknown parameter.

3.4.3.2 Latency

Latency is the time between the start of the input event, and the measurement of the output event. On the test-bench the input event is the start of a local transmission over the selected DCS I/O channel. The output event is the measurement of the output transmission over the selected DCS I/O channel. If an input and output can share the same communication channel, they will be transmitted on the same channel; otherwise two channels are used in the test. The test-bench is programmed to generate a known input sequence, and the DCS is programmed to echo the same sequence on the output. The time difference between the start of the sequence at the test-bench, and the reception

of the output sequence is measured as latency. The DCS does not perform any processing of the input signals; therefore this configuration will result in the lowest possible latency. Additional processing at the DCS will increase the latency. Latency is an important parameter in the processing of emergency events, and represents the time for the DCS control program to react to an initiating event.

3.4.3.3 Digital PID

A SGLC has been selected as the test process. The feedwater valves are the actuators. The steam generator level is the controlled variable. At the start of the simulation the steam flow, and reactor power are balanced based on the energy balance of the system. The simulation tests are based on the tests conducted in [49] at Oak Ridge National Labs. The dynamics of the simulated steam generator is a one-dimensional model based on the conservation of energy. The real-time solution of the steam generator equations is proposed by [50], and it is used to implement a real-time model in Matlab. The Matlab model uses a steam generator whose physical dimensions are the same as those used in a CANDU 6 plant. The simulation steam flow, water flow, and reactor settings are matched against the OPG NPP Simulator running at full power steady-state. The real-time Matlab model communicates over a TCP/IP session to a Modbus gateway written in LabWindows CVI. The gateway forwards the simulation values to the DCS over a serial Modbus interfaces. The simulation model is run at full power steady state and the DCS PID level control loop is tuned using a Ziegler-Nichols open-loop reaction rate method. The tuning is carried out automatically by the DCS engineering workstation. In the first three tests the water level set-point is adjusted and responses are measured. In the final three tests the steam load and reactor output are perturbed and responses are measured.

3.4.4 Data analysis

3.4.4.1 Throughput

The throughput is measured in Hz. The throughput tests measure the mean, standard deviation, minimum and maximum frequency of the resulting output waveforms. The result of a throughput test is two periodic output waveforms generated by the DCS using the I/O channel under test.

In the first output, the frequency with maximum magnitude, as taken from the FFT, is selected as the maximum frequency for the I/O channel.

In the second output the difference between the known throughput period and the actual period is throughput jitter.

If multiple I/O channels are involved in the test then the mean of all the results is calculated as the final result. The entire test process, including the selection of a true output frequency is automated using Matlab.

3.4.4.2 Latency

The result of the latency test is two output waveforms, one generated by the test-bench; the other is the echo from the DCS over the I/O channel under test. The zero crossings of each waveform are recorded, and the difference between the zero crossings is the latency of the DCS over the I/O channel. The mean, standard deviation, minimum, and maximum of the latency are recorded. If multiple I/O channels are involved in the test then the mean of all the results is calculated as the final result.

3.4.4.3 Digital PID

The simulation software records the system state at a sampling rate of 1 Hz. The recorded system state is used to calculate the time to steady state within a 1% threshold. The output variable is monitored until the averaged value is within 1% of the set-point. The

analyses of the simulation results are done with the knowledge of the test set-point, and both overshoot or undershoot values are calculated from the expected set-point.

3.5 Conclusions

The constructed test-bench and framework includes:

- HIL interface for analog, digital, serial and Ethernet I/O to the DCS under test;
- Matlab process simulation and interface to the DCS under test;
- I/O throughput, latency and jitter tests;
- DCS PID SGLC tests; and
- automated analysis of measured results using Matlab.

This test-bench and the proposed framework will be used to evaluate a DCS against NPP requirements. Chapter 4 presents the results of using the test-bench and framework to evaluate the DCS I/O interfaces and the PID control of SGLC.

4 EXPERIMENTS AND ANALYSIS

4.1 Introduction

The Emerson Process Management DeltaV controller is tested using the designed test-bench and framework. The tests cover 4 DCS I/O interfaces and DCS digital PID control. The results of each test are presented and analyzed. Each test is run a minimum of 3 times to ensure the results are repeatable, but only the final run is analyzed.

4.2 Test-bench tests

This research contains 19 tests covering 4 classes of I/O and 1 class of control. Test one through 13 measure I/O throughput, latency and jitter.

Digital I/O:

Test 1: The throughput and jitter for one digital output.

Test 2: The throughput and jitter for eight digital outputs.

Test 3: The latency and jitter for one digital I/O.

Test 4: The latency and jitter for eight digital I/O.

Analog I/O:

Test 5: The throughput and jitter for one analog output.

Test 6: The throughput and jitter for eight analog outputs.

Test 7: The latency and jitter for one analog I/O.

Test 8: The latency and jitter for eight analog I/O.

Modbus Serial:

Test 9: The throughput and jitter for one serial Modbus output.

Test 10: The throughput and jitter for eight and 100 serial Modbus outputs.

Test 11: The latency and jitter for one serial Modbus output.

Test 12: The latency and jitter for eight serial Modbus output.

OPC Ethernet:

Test 13: The throughput and jitter for one OPC output.

Digital PID:

Test 14 through 19 measure digital PID controller behaviour. All experiments begin with the reactor at full power steady state (FPSS). The digital PID tests are based on the test carried out by Oak Ridge National Laboratories in their NPP boiler level control research [49].

Test 14: The control loop response subject to 10% water level set-point change.

Test 15: The control loop response subject to 20% water level set-point change.

Test 16: The control loop response subject to 30% water level set-point change.

Test 17: The control loop response subject to a 10% steam flow and reactor power increase.

Test 18: The control loop response subject to a 20% steam flow changed and a 15% reactor power increase.

Test 19: The control loop response subject to a 30% steam flow changed and a 15% reactor output power increase.

4.3 Evaluating DCS properties

The following tests evaluate the properties of the DCS I/O channel including throughput, throughput jitter, latency, and latency jitter.

4.3.1 Digital I/O

4.3.1.1 Test 1: Throughput and jitter for one digital output

The purpose of the first test is to measure the effective throughput of the DCS digital output. There is no input to the DCS; therefore, all resources are used to generate the output square wave at a maximum frequency.

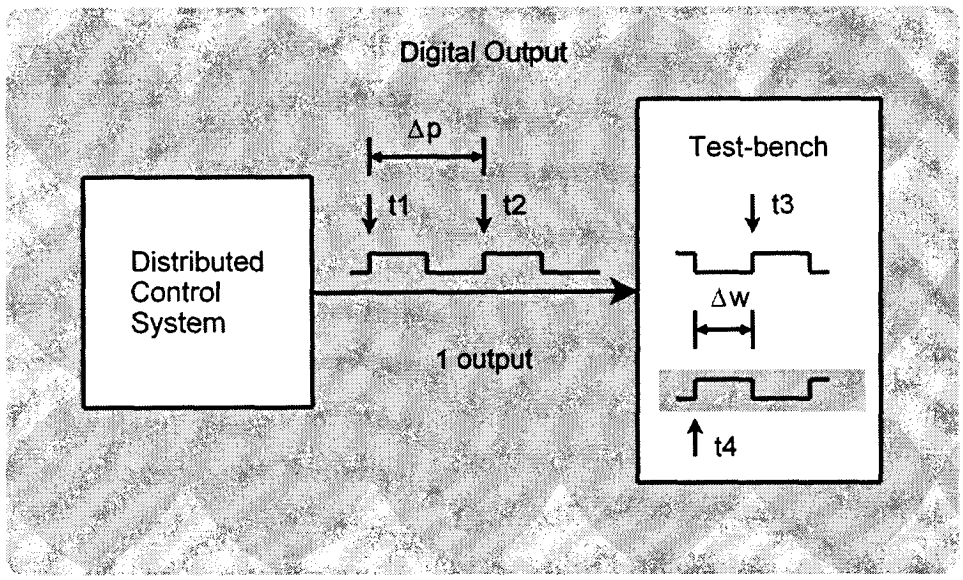

Figure 4.1: Schematic of digital output throughput and jitter

The minimum period of the digital output is determined. The minimum period is represented by Δp in Figure 4.1.

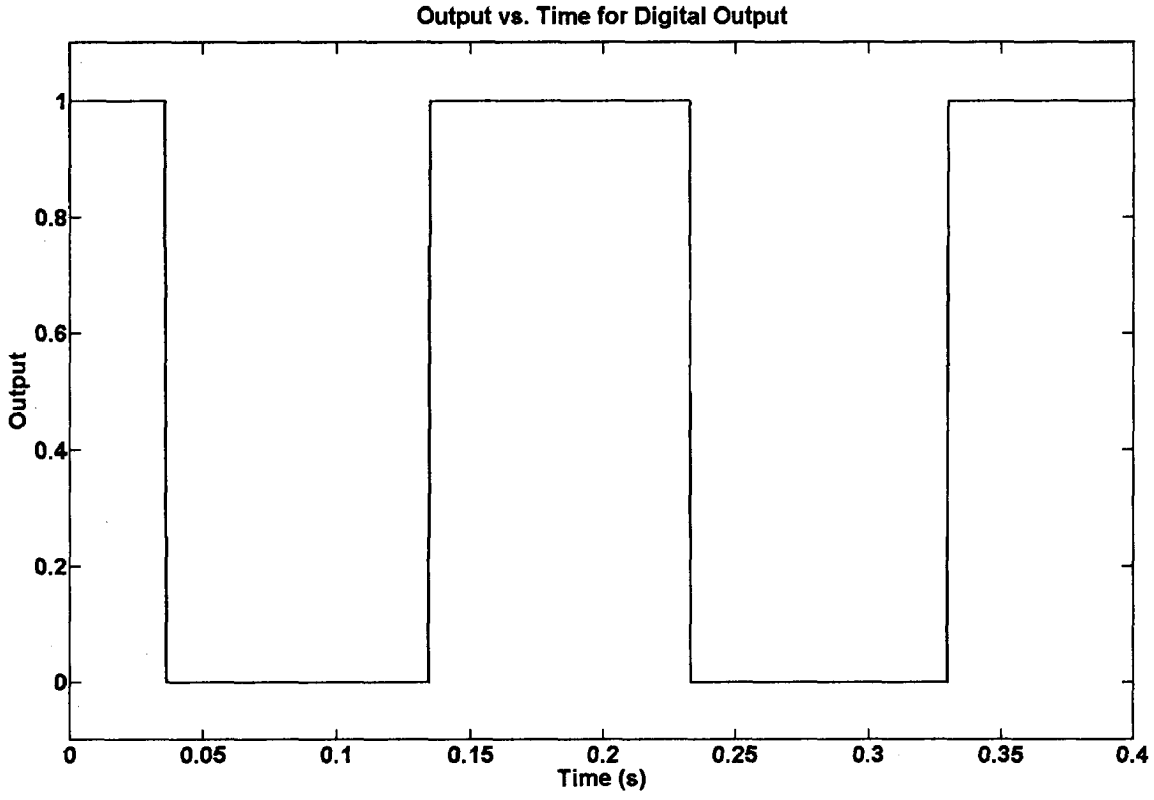

Figure 4.2: Single digital output waveform

A selection of digital output pulses generated by the DCS is shown in Figure 4.2. The DCS generates a output square wave using a digital sequence of logic one and logic zero values. The DCS I/O interface generates a voltage output corresponding to the digital sequence, and the test-bench converts the voltage back into a digital state.

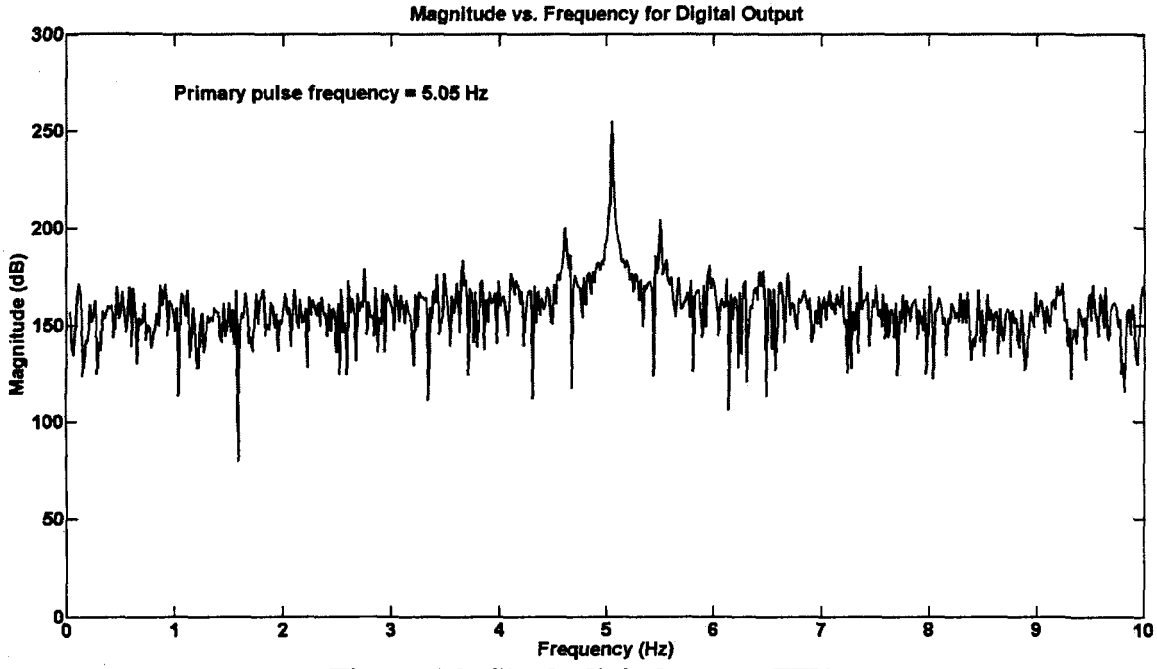

Figure 4.3: Single digital output FFT

The Fast Fourier Transformation (FFT) of the sampled waveform is shown in

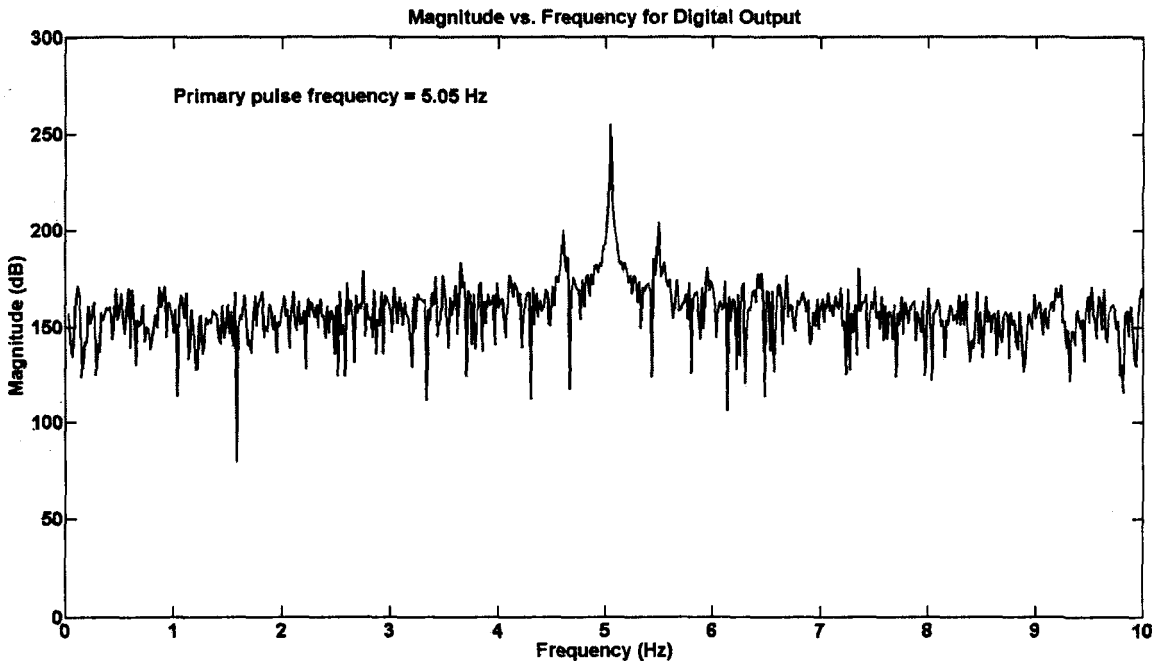

Figure 4.3. The pulse frequency is 5.05 Hz. The FFT frequency spacing is 0.01 Hz. The output is sampled at 2 kHz and 200,000 samples or 100 s is used in the FFT to achieve a resolution of 0.01 Hz in the frequency domain. The frequency with the highest magnitude is considered the output frequency for the DCS I/O channel.

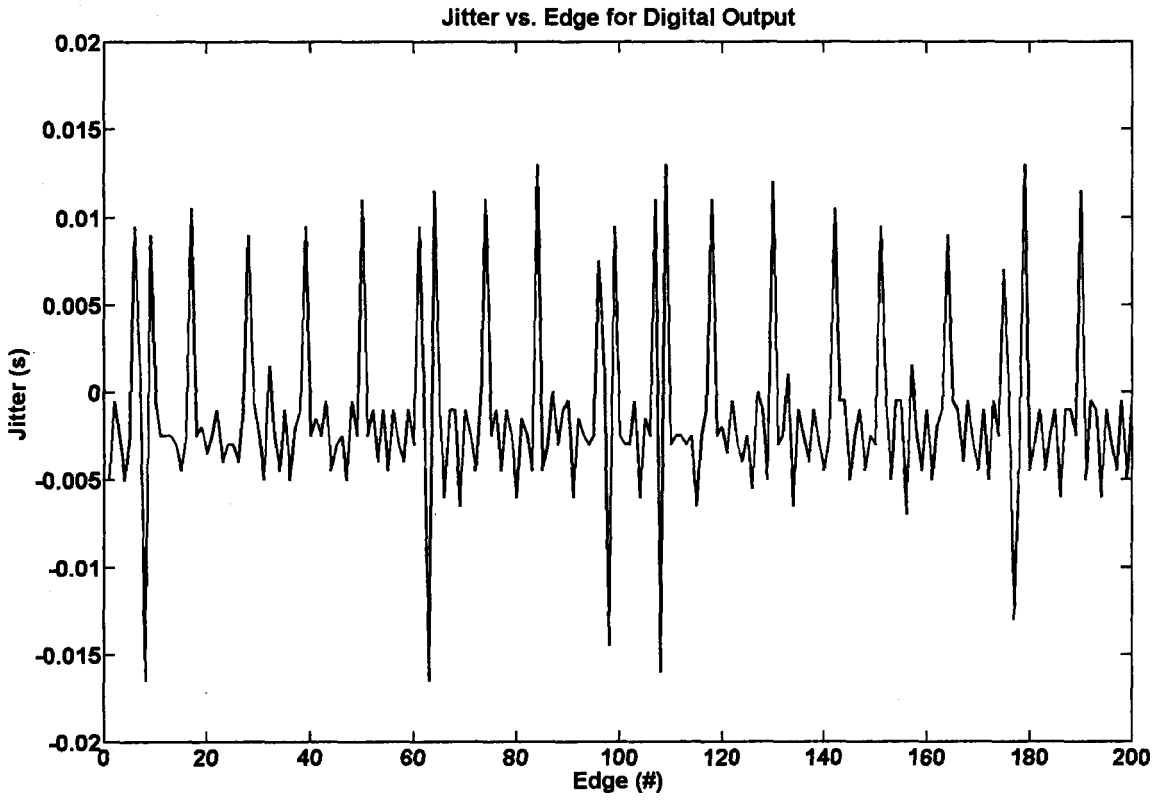

Figure 4.4: Single digital throughput jitter

The ideal waveform is a 5 Hz square wave. The DCS is programmed to produce a 5 Hz square wave. The period of the ideal waveform is double Δw shown in Figure 4.1. For each period starting at time t3 in the DCS waveform, and time t4 in the ideal waveform, the difference between the generated and ideal periods is shown in Figure 4.4. The figure shows the deviation of the DCS generated waveform period and the expected waveform period. The deviation from the expected waveform is defined as jitter. The x-axis represents the edge and starting period in the waveform, and the y-axis is the deviation in seconds from the expected time. If the I/O were perfectly deterministic then Figure 4.1 would be a flat line at zero representing no deviation in the output waveform.

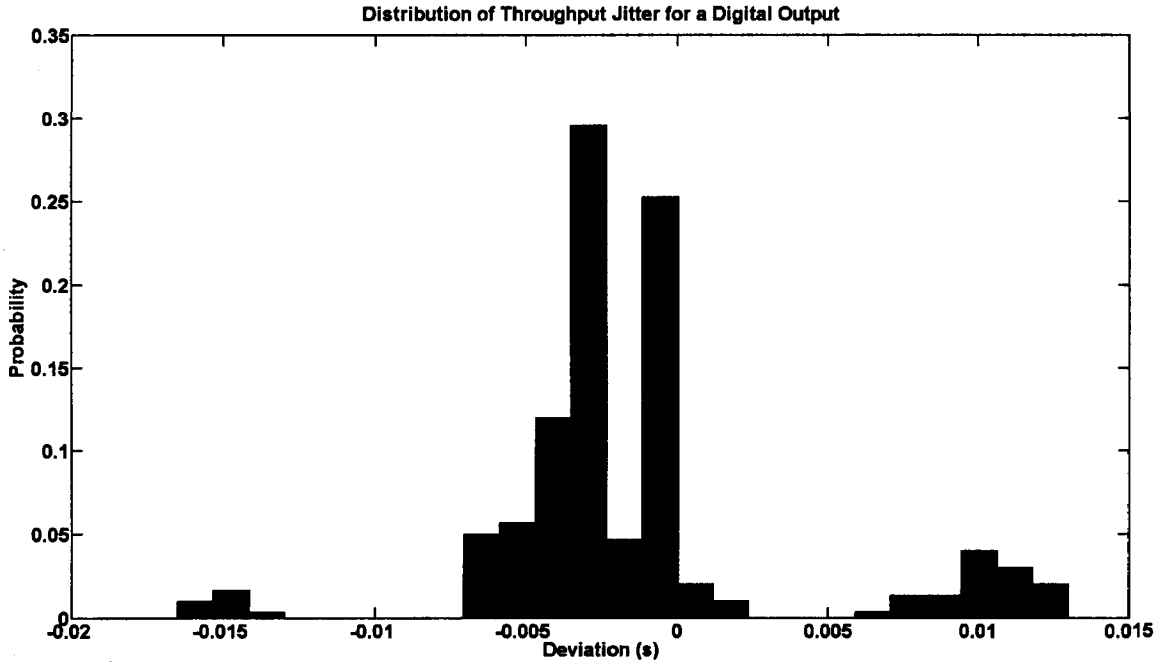

Figure 4.5: Single digital throughput jitter histogram

A distribution of the jitter is shown in Figure 4.5. The mean of the deviations is -1.2 ms, with the maximum and the minimum deviations at +15 ms and -14 ms respectively. Since the mean of the deviations are negative, it means that, on average the pulses arrive early. It is not known why the DCS outputs pulses arrive early. The DCS may prefer early pulse delivery over late pulse delivery, which is preferable under certain control scenarios like shut-off valve activation.

This test shows that the DCS can output digital data at a maximum rate of 5.05 Hz. The bits per second rate is equal to double the toggle rate, thus the maximum raw rate is 10 bps. The results of all the tests are summarized and tabulated in Chapter 5.

4.3.1.2 Test 2: Throughput and jitter for multiple digital outputs

The purpose of this test is to measure the effective throughput of multiple digital outputs. The only function of the DCS is to generate an output square wave at a maximum

frequency on 8 digital output channels. The minimum period is shown schematically in Figure 4.6 as Δp or the time difference between t1 and t2.

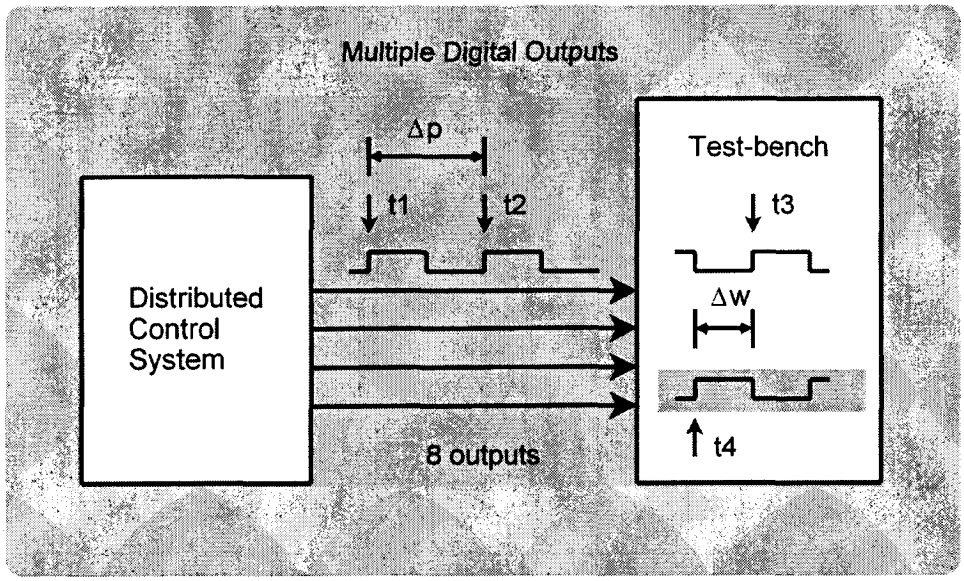

Figure 4.6: Schematic of multiple digital output throughput and jitter

The 8 digital output pulses generated by the DCS are shown in Figure 4.7. To help differentiate the outputs each output is given an artificial y-axis offset. This sequence is measured by the test-bench framework.

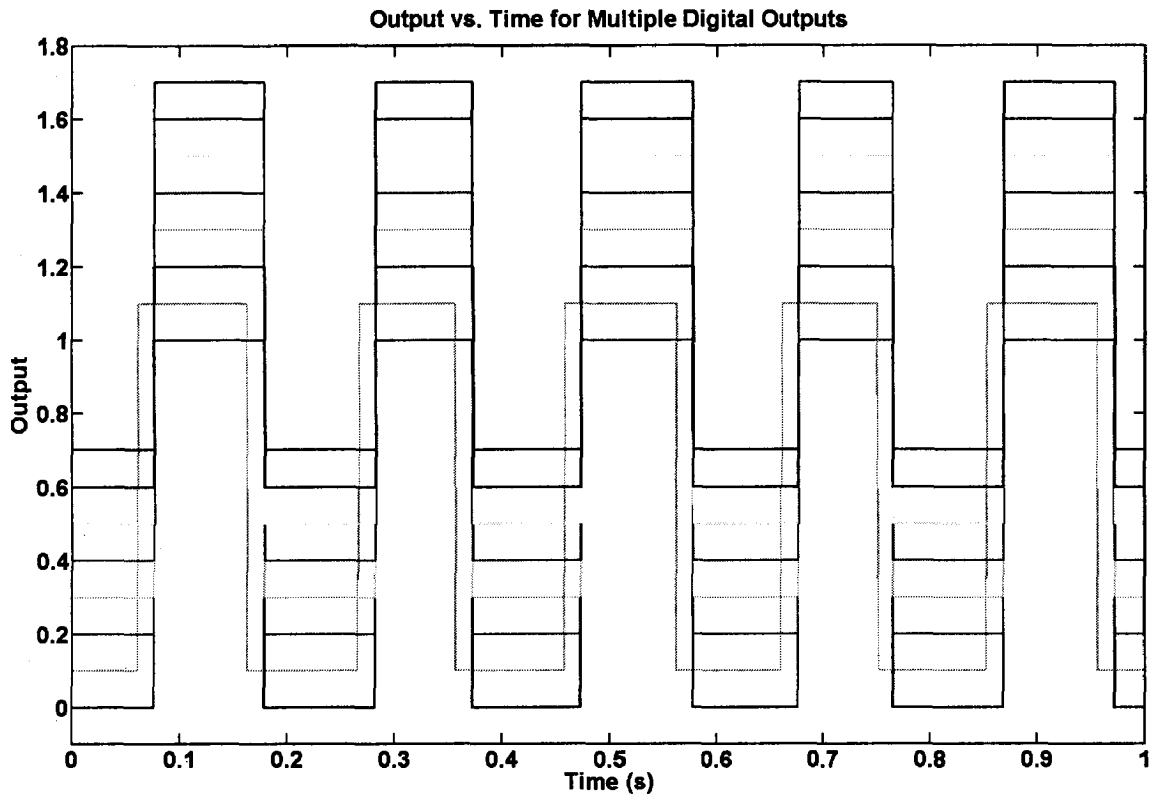

Figure 4.7: Multiple digital output waveforms

A test program, written for the DCS, is used to drive all outputs through both digital states as fast as possible. The second digital output triggers 11 ms earlier than all other digital outputs. The reason for the early triggering is not known and is present at each test repetition.

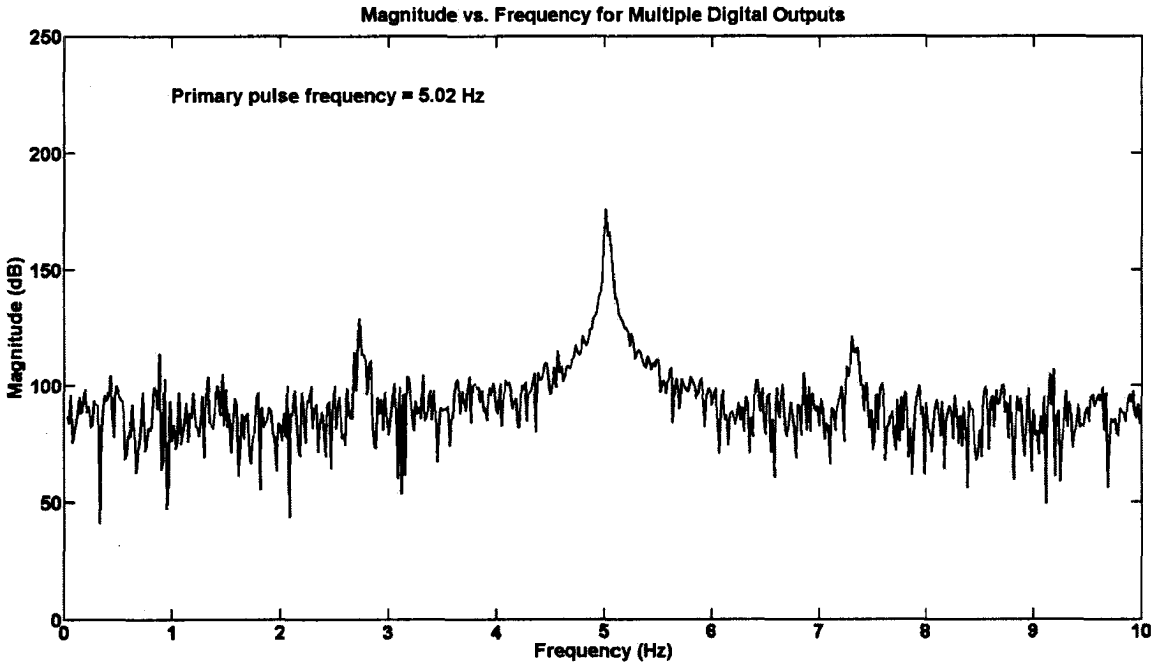

Figure 4.8: Multiple digital outputs FFT

The FFT of one digital output is shown in Figure 4.8. The pulse frequency is measured as 5.02 Hz. The mean frequency of all 8 digital outputs is 5.02 Hz. The FFT frequency spacing is 0.01 Hz. The output is sampled at 2 kHz and 200,000 samples or 100 s is used in the FFT to achieve a resolution of 0.01 Hz in the frequency domain. Increasing the number of digital outputs to 8 has lowered the throughput from 5.05 Hz to 5.02 Hz.

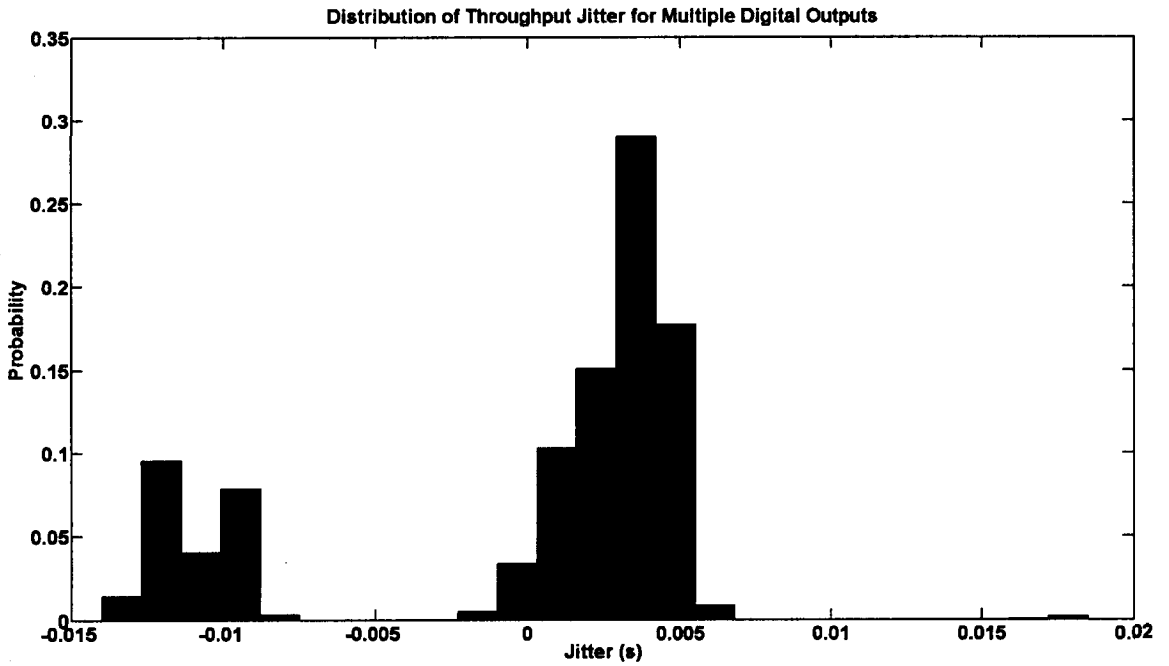

Figure 4.9: Multiple digital throughput jitter histogram

The distribution of digital output jitter is shown in Figure 4.9. The DCS is programmed to generate a 5 Hz square wave on all outputs. If the response of the DCS is deterministic, the deviation from the expected frequency will be zero.

Digital output pulses which arrive later than expected appear in the positive range of the histogram. Pulses which arrive early are in the negative range. Pulses arriving between [-0.005,0.005) s, as shown in Figure 4.9, constitute 75% of early pulses. The final 25% of the pulses also arrive early within a 20 ms window. None of the pulses arrive earlier or later than 100 ms. The earliest pulse arrives 0.018 s early, while the latest pulse arrives 0.013 s late. The pulse jitter has a mean value of 0.000 s, a median value of 0.002 s, and a standard deviation of 0.006 s.

4.3.1.3 Test 3: Latency and jitter for one digital I/O

This test measures the latency of a digital loop. A digital output is generated from the test-bench, and used as an input by the DCS. The DCS program reproduces the input event on a digital output which is then measured by the test-bench. In this configuration, the time between generated output and received input is the latency of the DCS. The latency of the DCS is represented schematically in Figure 4.10 as the time difference between event t1 and t2.

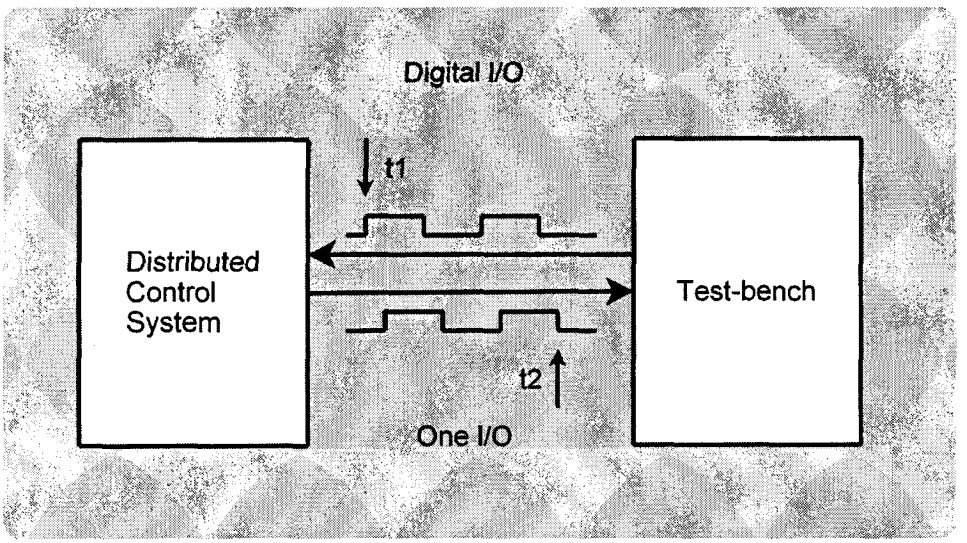

Figure 4.10: Schematic of single digital I/O latency

Latency is critical in some NPP safety systems. The time taken to respond to an input emergency event, like turbine failure, will affect the pressure in the steam generators. The shorter the response time, i.e. low latency, the faster the actuation of the atmosphere steam discharge valves, and the lower the probability of boiler damage. Latency is the time taken by the DCS to process an input event and generate an output event. The latency is deterministic if the standard deviation of the latency tends towards zero.

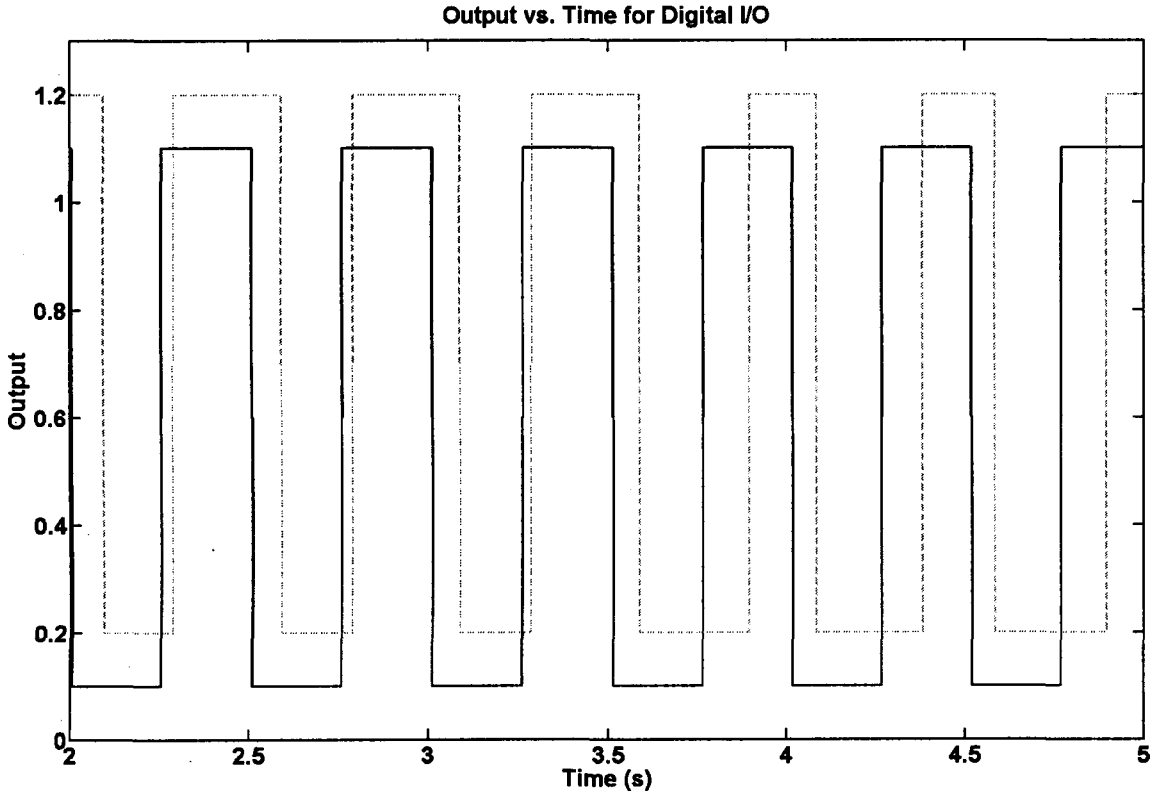

Figure 4.11: Single digital input vs. output

The test-bench output waveform as a solid line and the reproduced output as a dashed line are shown in Figure 4.11. To help differentiate the output it is given an artificial y-axis offset.

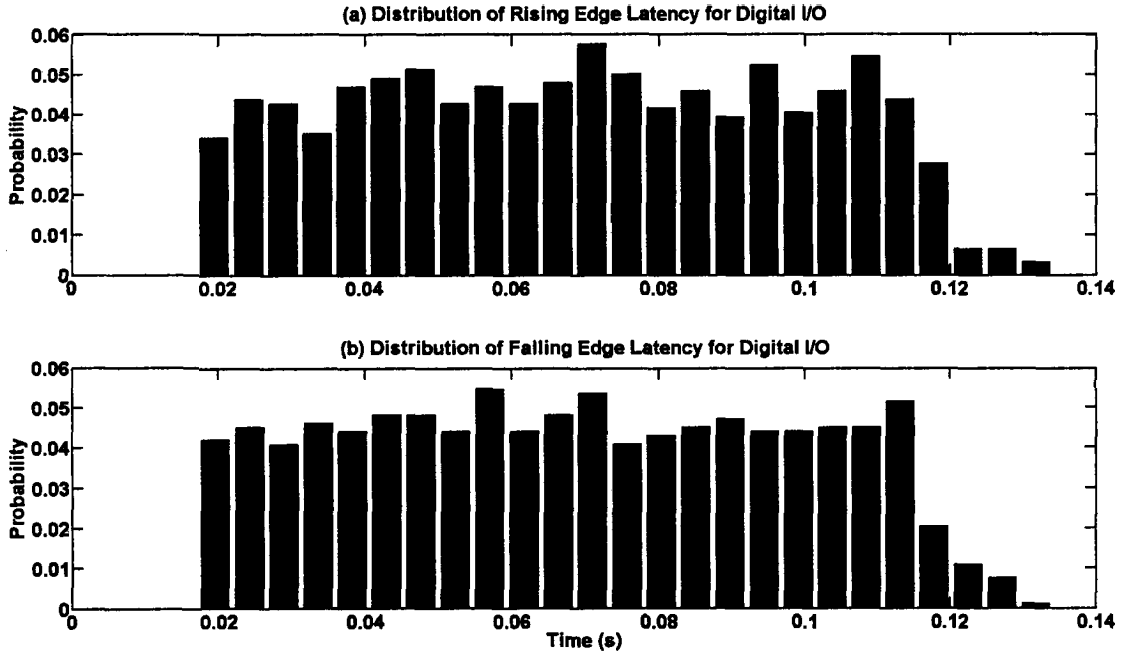

Figure 4.12: Single digital I/O rising and falling edge latency histogram

A digital waveform has both rising and falling edges. A distribution of the (a) rising edge latency and (b) falling edge latency is shown in Figure 4.12. The latency of each event is measured separately in order to determine if there is a difference between rising and falling edges. The average and the standard deviation of the rising and the falling edge latency are equal to within a 1% threshold. The mean rising edge latency is 0.072 s, with a standard deviation of 0.029 s. The mean falling latency is 0.072 s with a standard deviation of falling edge latency of 0.029 s. The minimum latency is 0.019 s, and the maximum latency is 0.136 s

The rising and falling edge latency are the same, and are referred to collectively as latency in the digital channel. In this test, the DCS is programmed to do the least amount of work possible before returning the digital value. This means that the values presented are the best case latency for the digital channel. Any additional computations can cause an increase from the measured latency.

4.3.1.4 Test 4: Latency and jitter for multiple digital I/O

This test measures the latency of multiple digital loops. A set of digital outputs is generated from the test-bench, and is used as multiple digital inputs to the DCS. The DCS module must reproduce each input event on a digital output which is then measured on the test-bench. The time between the generated output and the received the input is the latency of the DCS in this configuration. This test is represented schematically in Figure 4.13.

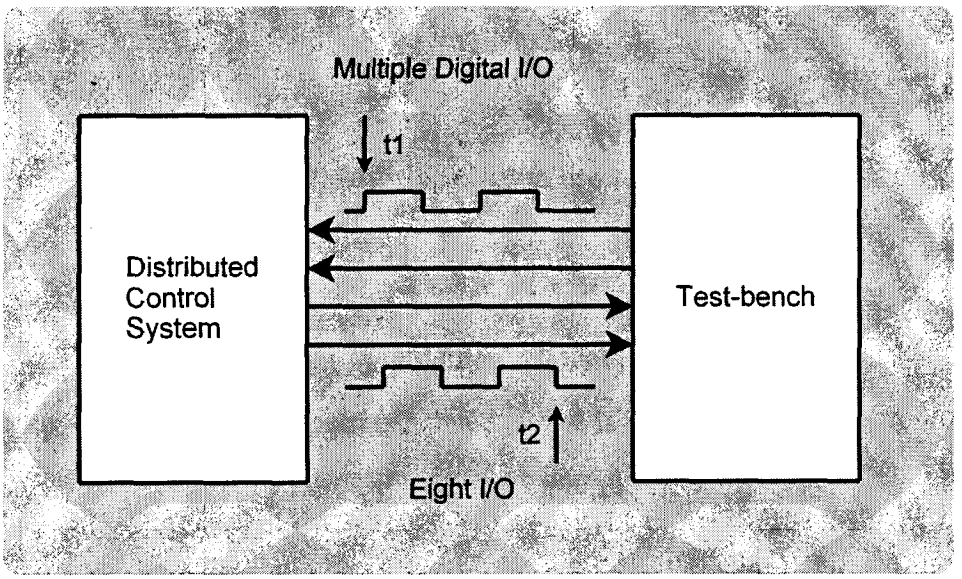

Figure 4.13: Schematic of multiple digital I/O latency and jitter

The test can be used to determine if the behaviour of multiple loops is different from that of the single loop. If a DCS can respond to multiple digital input events with the same latency as a single input event, the DCS can be used to control multiple loops with similar latency.

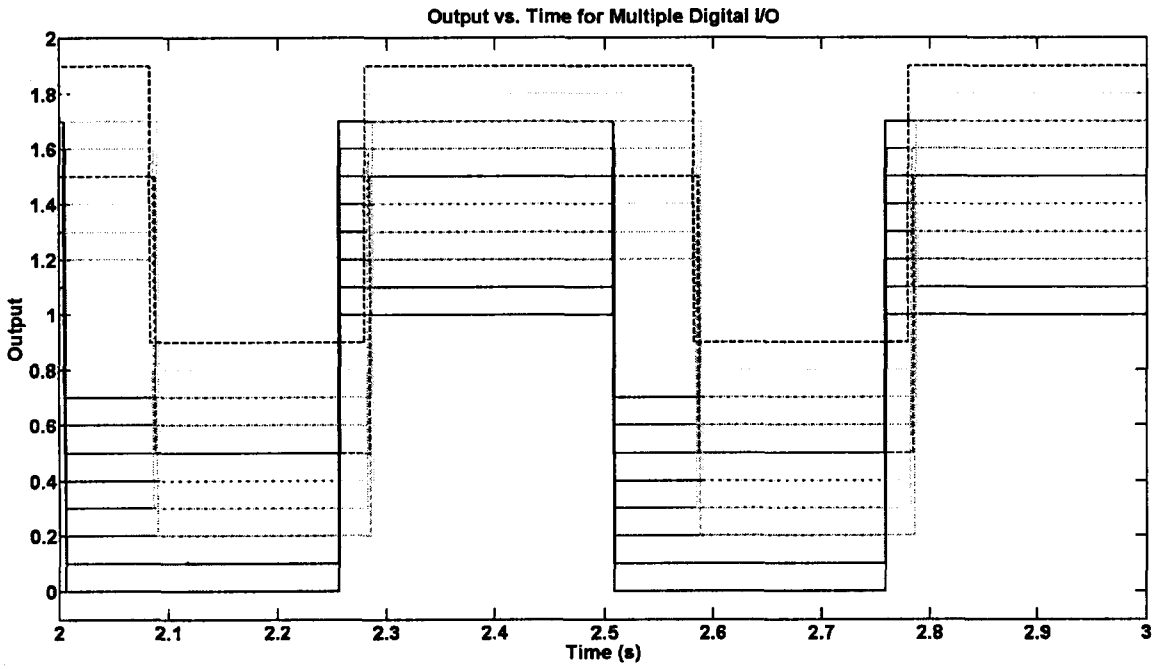

Figure 4.14: Multiple digital inputs vs. output.

The test-bench digital output and DCS digital output are shown in Figure 4.14, the test-bench digital output values appear as solid line style and the DCS digital output as dashed lines. To help clarify the figure each input and output is given an artificial y-axis offset. The early triggered digital output seen in test one does not occur with this DCS program even when repeated.

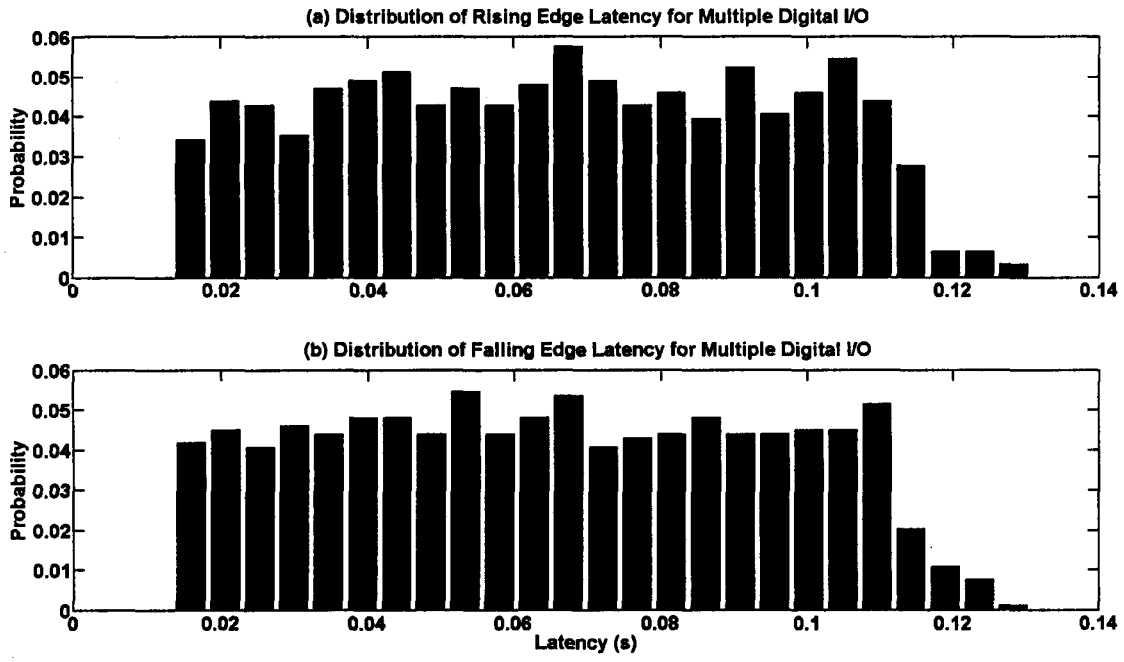

Figure 4.15: Multiple digital I/O rising and falling edge latency distribution

This test measures the time between the input event and the output event. The (a) rising-edge latency and (b) falling edge latency distribution are shown in Figure 4.5. The mean latency over all 8 I/O is 0.072 s with a standard deviation of 0.029 s. For all 8 I/O the minimum latency is 0.019 s with a maximum latency of 0.136 s, as shown in Figure 4.15. The one I/O and the eight I/O test have identical minimum and maximum latency of 0.019 s and 0.136 s. This test demonstrates that the addition of 7 I/O channels, all physically present on the same DCS digital output card, did not significantly alter the behaviour of the DCS digital I/O latency.

4.3.2 Analog I/O

4.3.2.1 Test 5: Throughput and jitter for one analog output

In this test the DCS outputs two analog values at a maximum rate. The two values output are the minimum and maximum values for the output range.

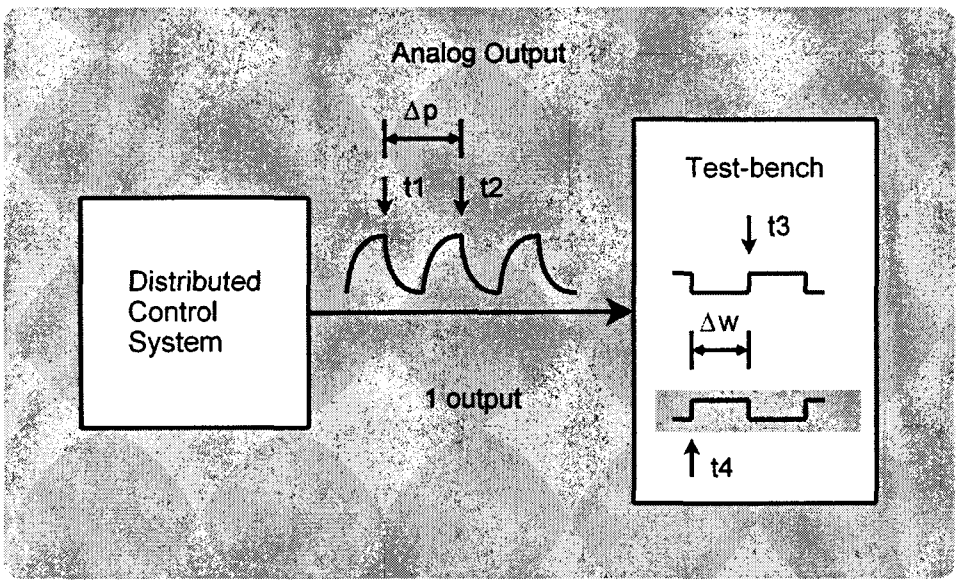

Figure 4.16: Schematic of analog output throughput and jitter

The system overview of the analog output process is shown schematically in Figure 4.16. The width of one period is shown as Δp in Figure 4.16

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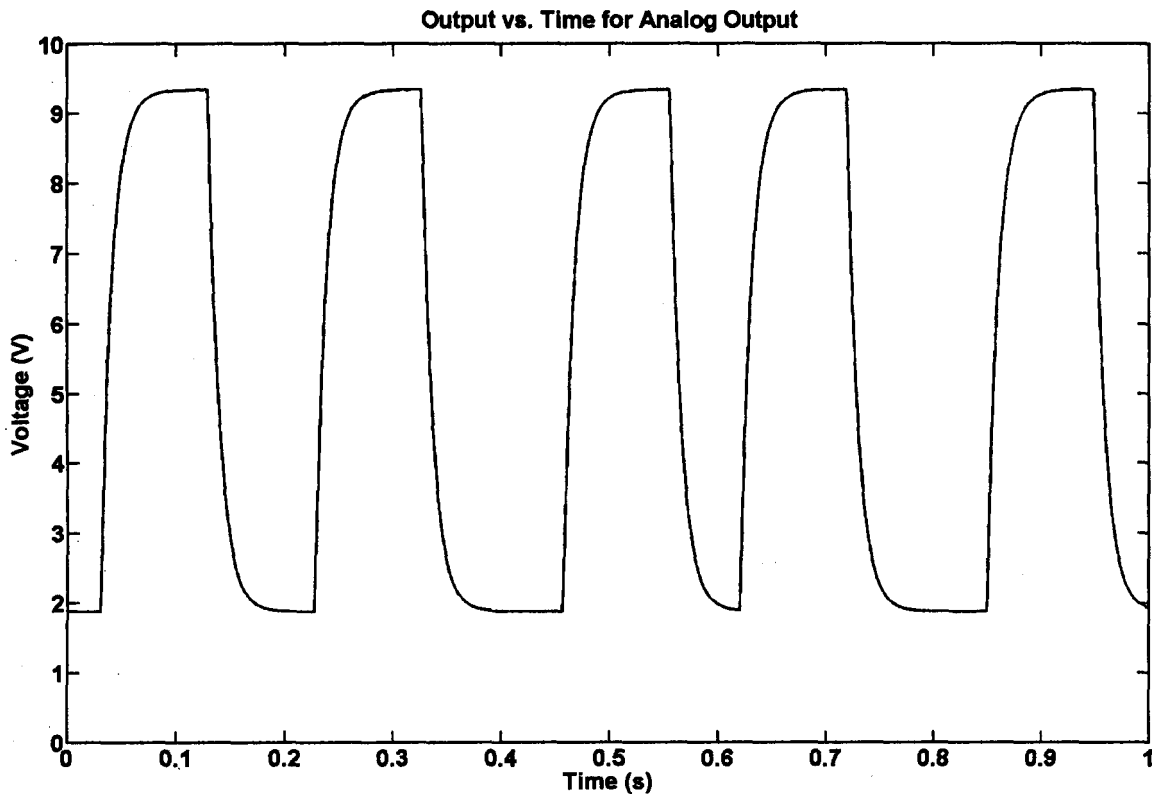


Figure 4.17: Single analog output waveform

The output waveform of the analog output is shown in Figure 4.17. The analog output waveform cycles between 4 mA and 20 mA. The test-bench, using a 470 Ω resistor, converts the current into a measured voltage from 1.88 V to 9.40 V.

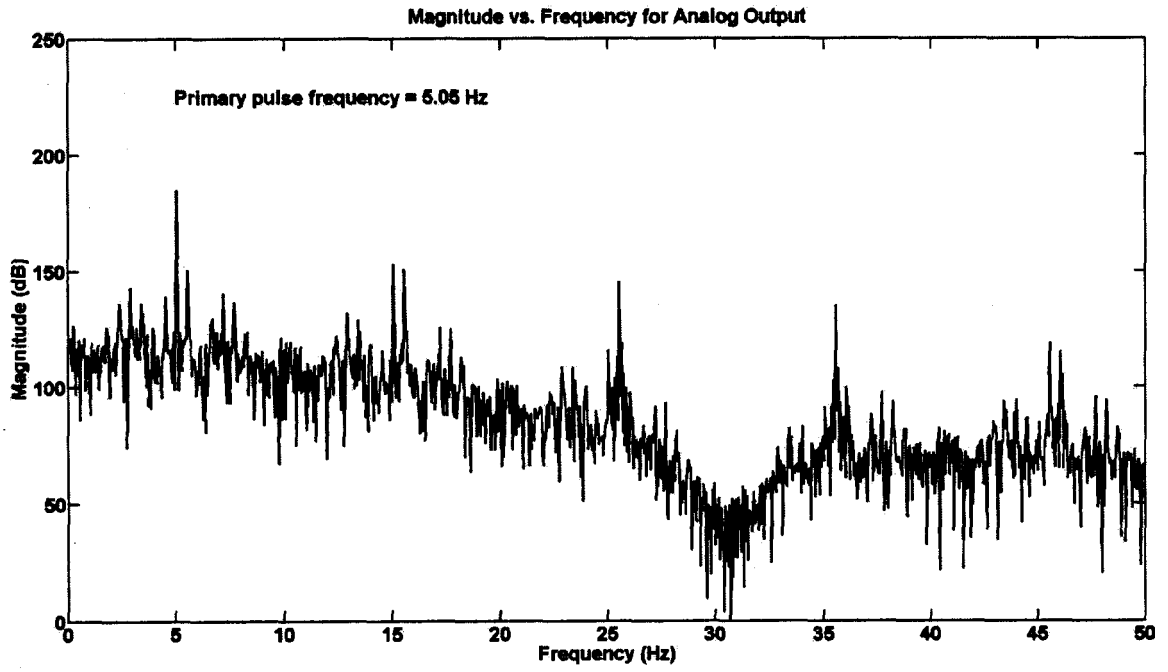


Figure 4.18: Single analog output FFT

The frequency of the output is measured by taking the FFT of the waveform and selecting the value with the highest magnitude. The output waveform has a frequency of 5.05 Hz as shown in Figure 4.18.

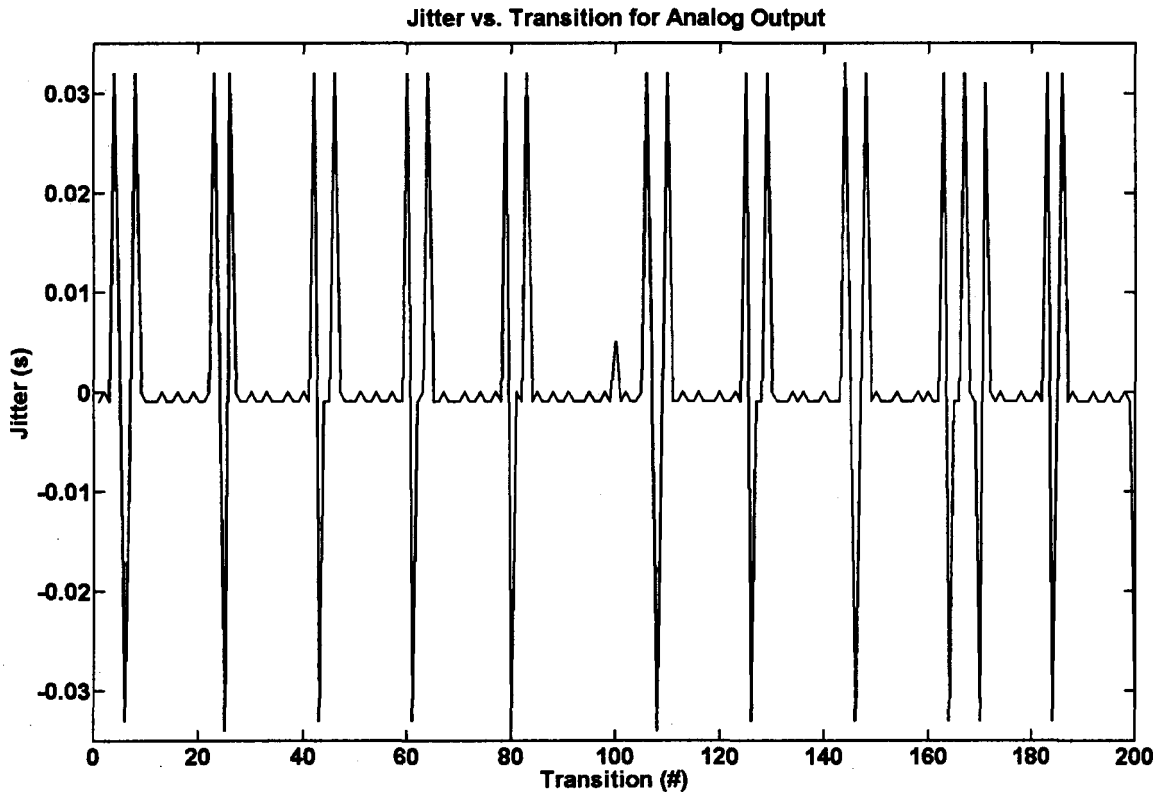


Figure 4.19: Single analog throughput jitter

The DCS is programmed to produce an expected frequency of 5.0 Hz. The output analog waveform is converted to a set of edge transitions from high to low and low to high. The high to low and low to high transitions occur at the 3 dB point of the output waveform. The time of an expected transition is t4 in Figure 4.16, while t3 is the actual transition. For each transition the difference in transition time is shown as jitter in Figure 4.19. The expected analog output jitter ranges from -0.034 s to +0.033 s.

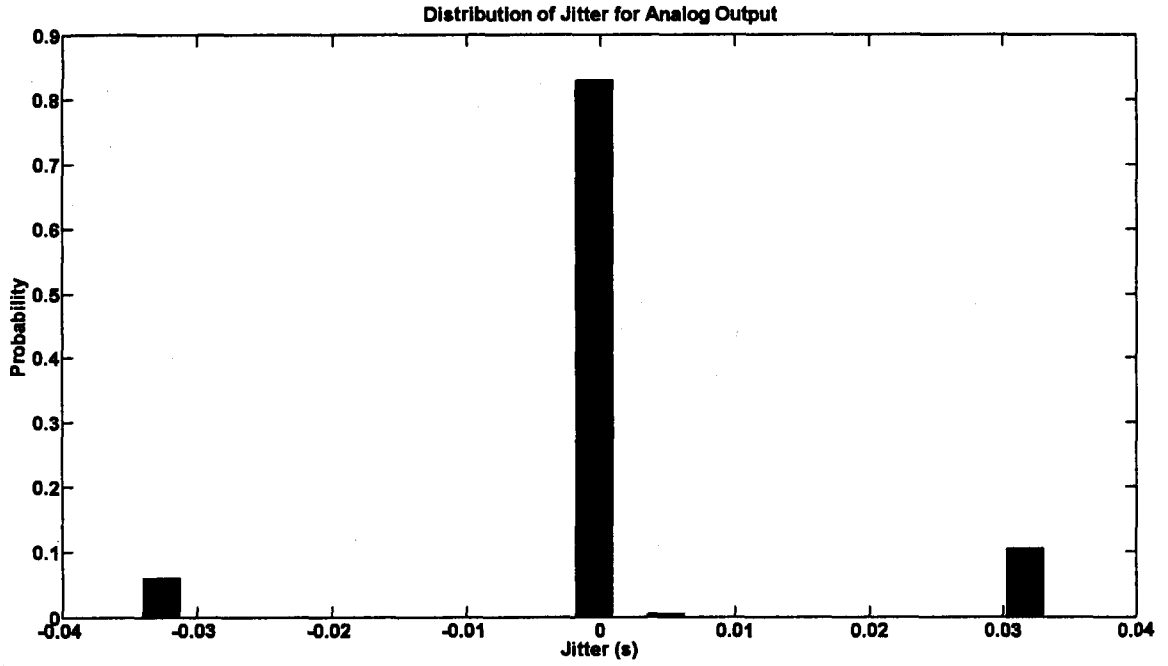


Figure 4.20: Single analog throughput jitter histogram

The distribution of the jitter is shown in Figure 4.20. The mean of the jitter is 0.000 s with a standard deviation of 0.013 s. All pulses arrive within [-0.040,0.040) s and 83% arrive within [-0.005,0.005). The DCS is not processing other events and the values in Figure 4.20 are the best case throughput values for output values that cover the full analog range.

4.3.2.2 Test 6: Throughput and jitter for multiple analog outputs

In this test the DCS outputs multiple analog waveforms. Similar to test 5, the DCS outputs the maximum and minimum analog output values. This test is shown schematically in Figure 4.21.

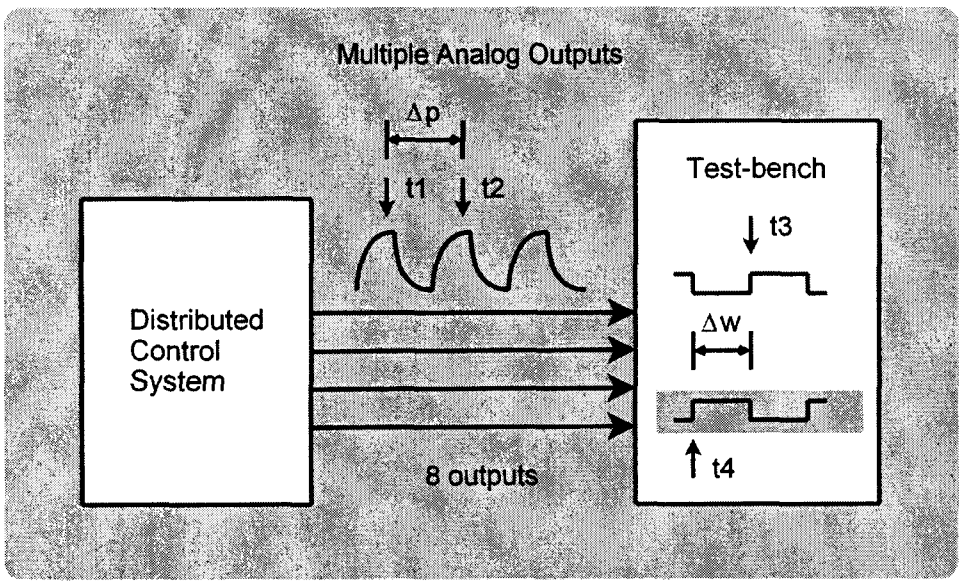


Figure 4.21: Schematic of multiple analog output throughput and jitter

Examples of analog values in a NPP include valve position, flow control, rod position, and pressure measurement. In a nuclear power plant the analog outputs can be used to set the value of plant parameters which have more than just a Boolean state. Excursions in analog values should not be too large during the stable operation of the plant, but the maximum rate of change represents the upper limit on the slew rate of the output. The output period is represented in Figure 4.21 as Δp or the time difference between time t2 and t1.

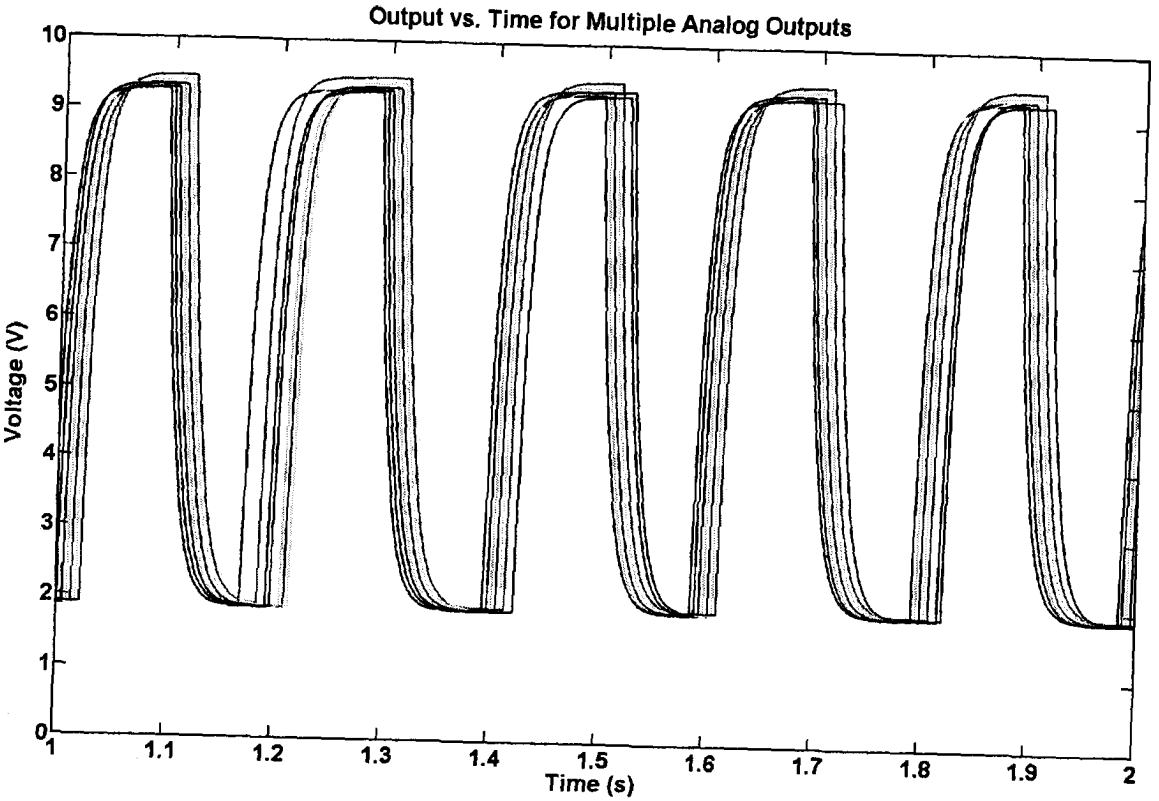


Figure 4.22: Multiple analog output waveforms

The output waveform for 8 analog outputs is shown in Figure 4.22. The analog output values vary between 0 and 100% of the DCS analog output full range. The transition start times for each of the analog outputs are different. The analog output sequencing jitter is not measured by the framework. The framework measures the jitter of individual analog outputs, but not the relationship between two analog outputs.

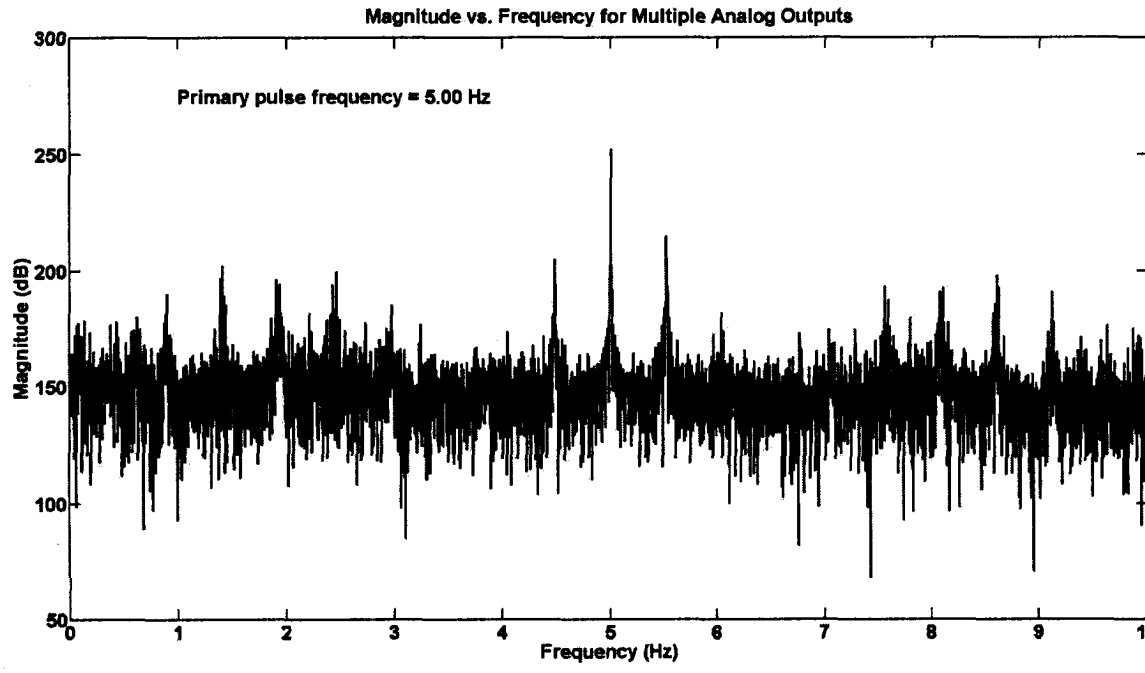


Figure 4.23: Multiple analog output FFT

The maximum frequency of the analog output shown in Figure 4.23 is 5.00 Hz. This value is calculated from the FFT of the output pulses. The frequency with the highest magnitude is also shown in Figure 4.23.

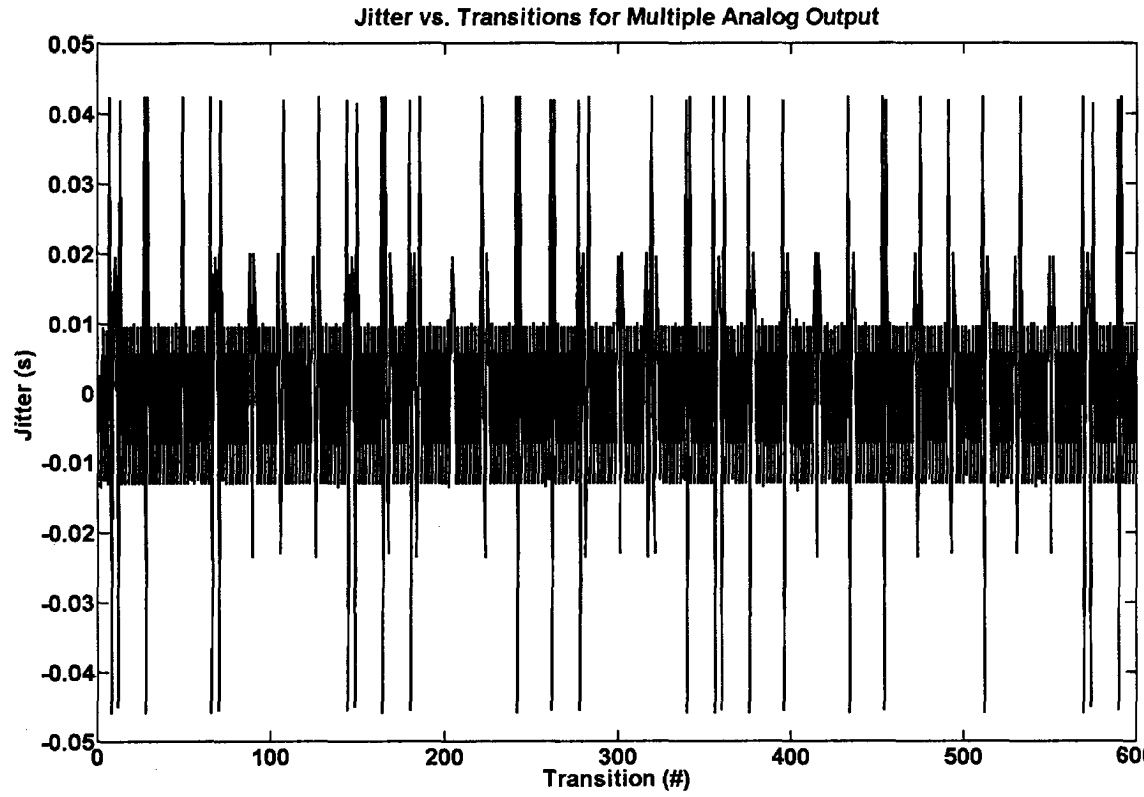


Figure 4.24: Multiple analog output jitter

The determinism, or jitter, of this output analog pulse is shown in Figure 4.24. An analog pulse that has a fixed frequency would produce a straight line in a jitter versus transition plot. Variations in the analog output period produce jitter in the output analog pulse. The maximum jitter is 0.023 s, with a mean of 0.000 s and a standard deviation of 0.009 s. The latency shown in Figure 4.24 is quantized into 4 levels, and the cause of this is not known. The quantization of the latency may be due to the manner in which the outputs are energized e.g. one ore more outputs are energized at equally spaced intervals to prevent overloading the bussed power supply.

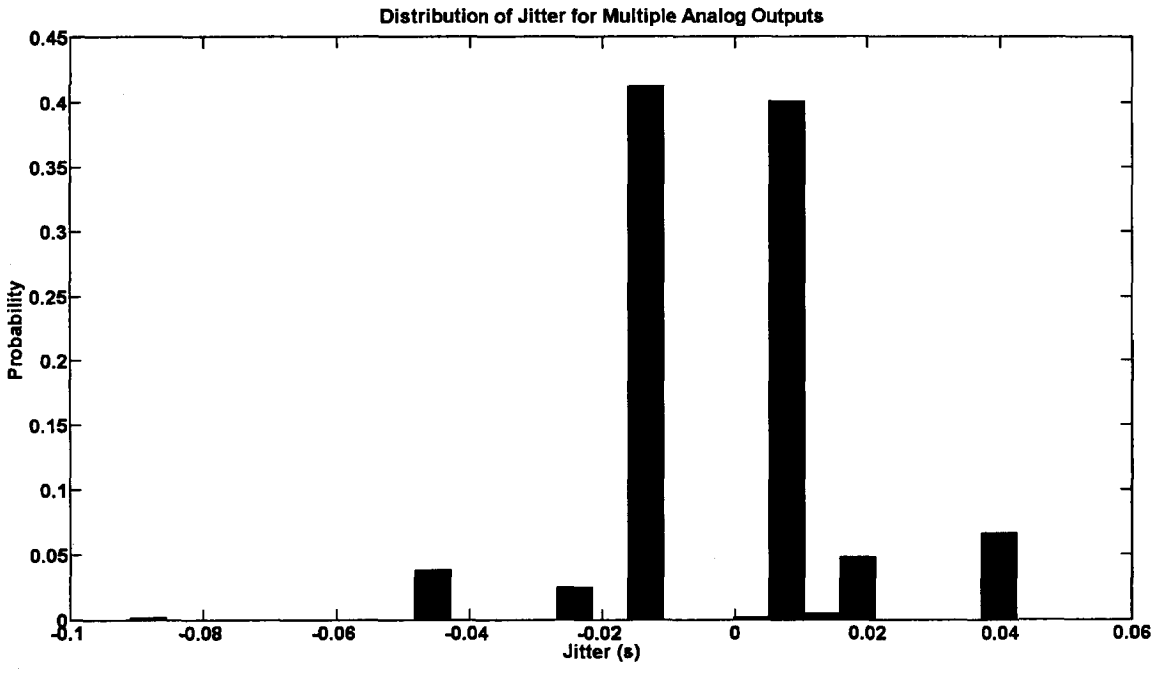


Figure 4.25: Multiple analog throughput jitter histogram

The distribution of jitter for all analog outputs is shown in Figure 4.25. A total of 51% of the pulses fall on the positive axis; this indicates that the pulse deviation has a slight tendency to be late instead of early. If the analog pulses produced a precise single frequency, and never deviated, the figure would have a single line in the middle at zero.

4.3.2.3 Test 7: Latency and jitter for one analog I/O

This test measures the latency of an analog loop. An analog output is generated from the test-bench; this is observed as an analog input by the DCS. The analog loop is represented schematically in Figure 4.26. The DCS module must echo the input event on an analog output line which is then measured by the test-bench. The time between generating the output and receiving the input is the latency of the DCS in this configuration. The latency is the time difference between the initiating event at t3 on Figure 4.26, and the arrival of the response t4 at the test-bench.

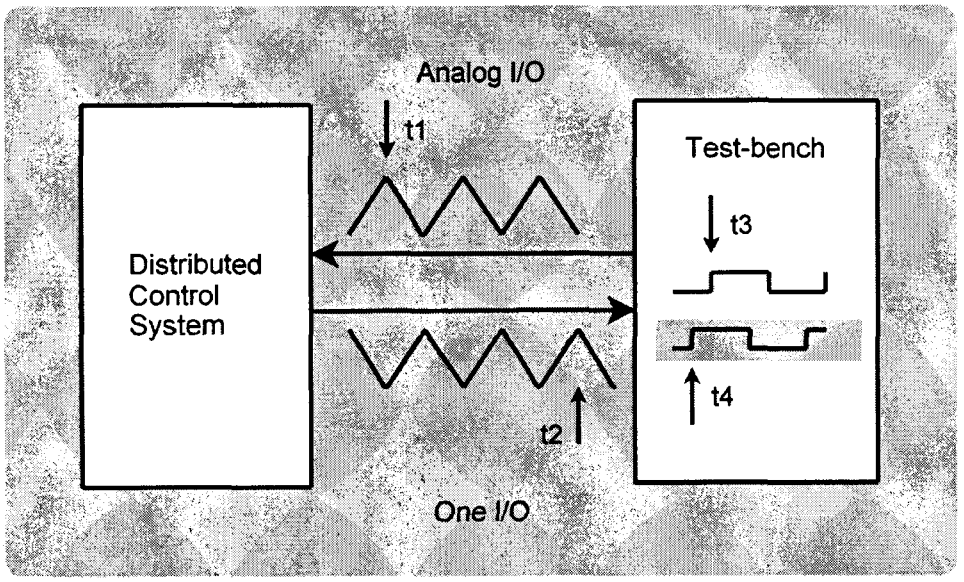


Figure 4.26: Schematic of analog I/O latency and jitter

In tests 5 and 6 the DCS exhibited shortened analog output periods. The shortened output periods were followed by lengthened output periods, such that the average remained near zero. The DCS appeared to be attempting to maintain an average number of pulses in a fixed time period. In this test a triangle waveform is generated as output. A triangle waveform limits the rate of output voltage change, and experimentally exhibits lower jitter while still allowing the test-bench to measure latency. The purpose of this test is to measure latency but not throughput.

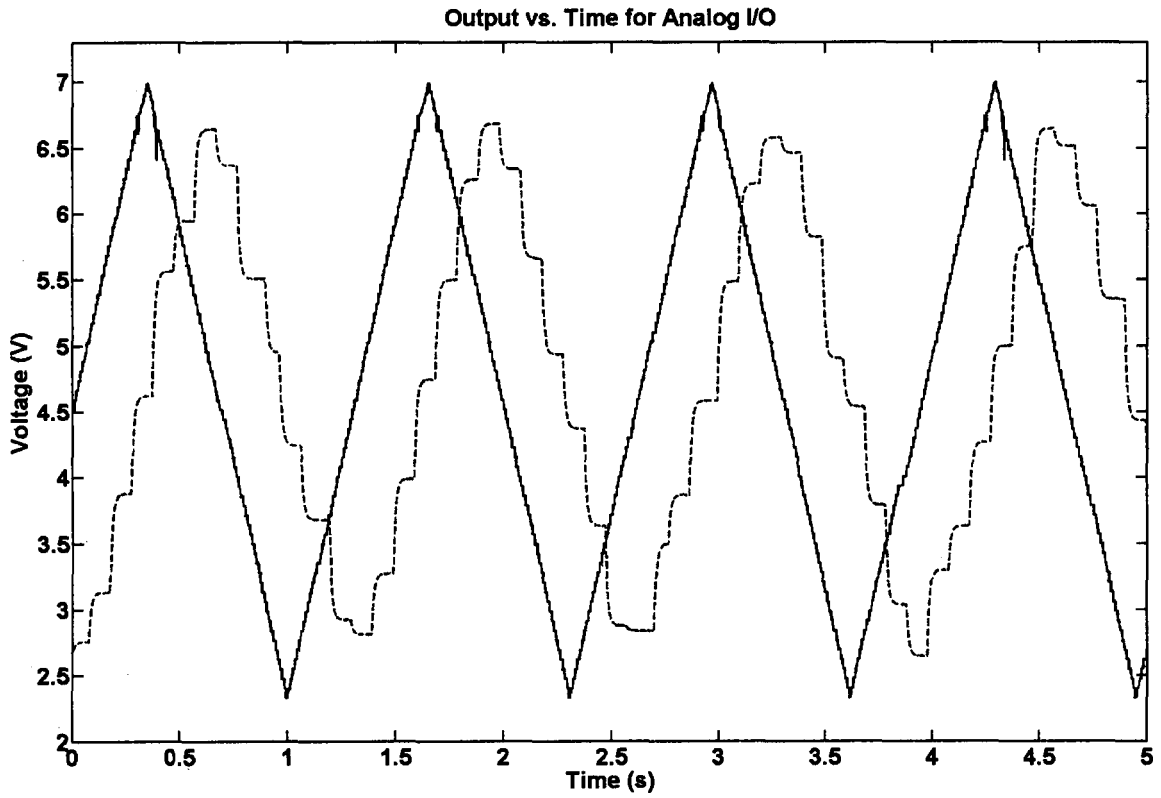


Figure 4.27: Single analog I/O input vs. output

The mid-point of the output range is subtracted from the input and output to produce zero crossings. The zero crossings of the data are identified. The time difference between the zero crossing of the input sequence and the output sequence is the latency measured in seconds.

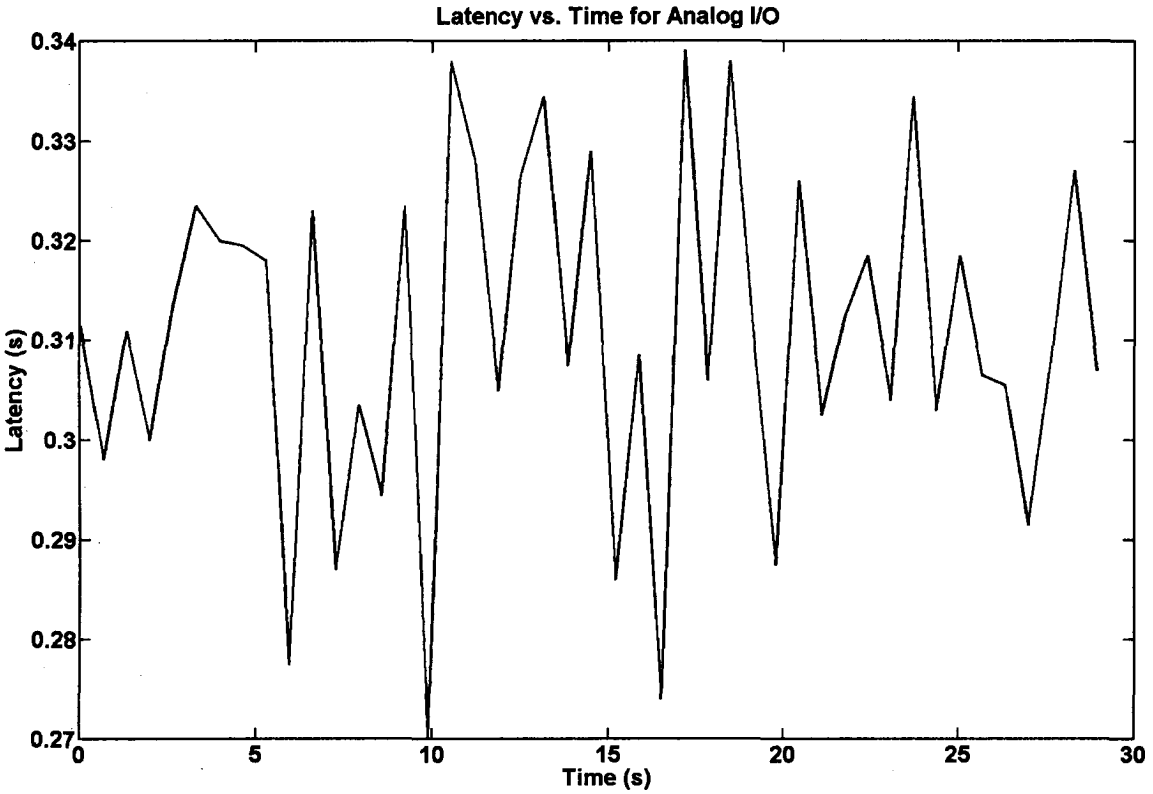


Figure 4.28: Single analog I/O latency

The mean latency of the analog I/O is 0.310 s, with a standard deviation of 0.017 s. The minimum latency is 0.270 s, and the maximum latency is 0.339 s. The analog I/O has the highest latency of all the tested I/O interfaces. For a comparison of latencies see Table 5.3: DCS I/O Latency.

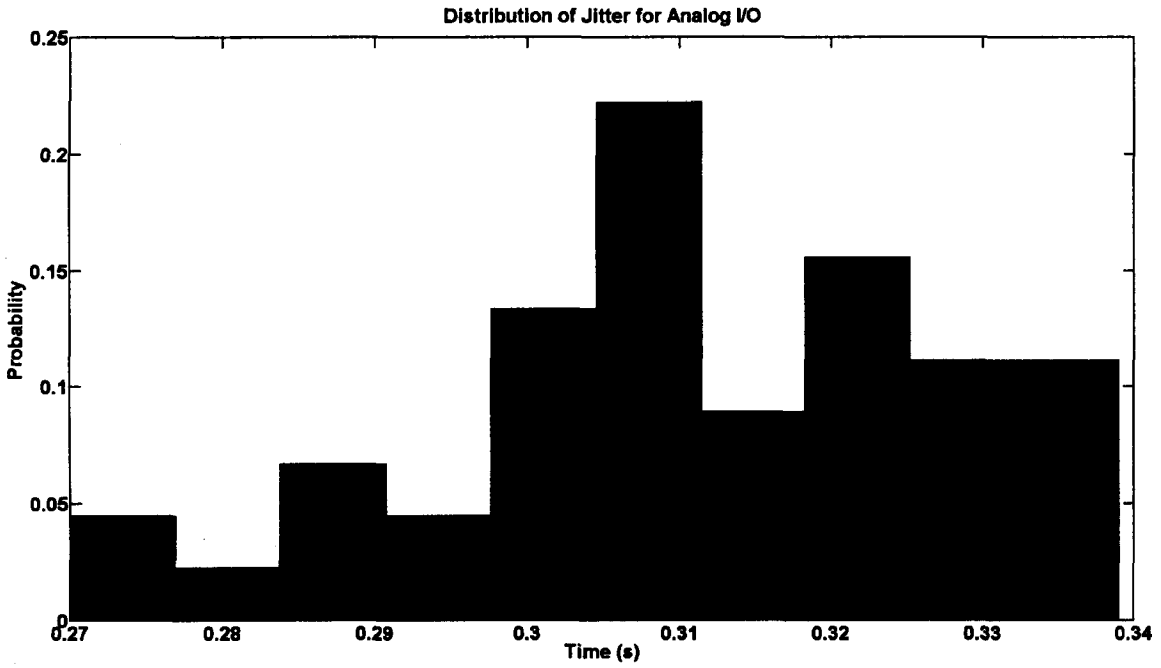


Figure 4.29: Single analog I/O latency histogram

The latency associated with the analog I/O pulse sequence is higher than the digital I/O latency. The mean latency is 0.310 s, visible as the central peak in Figure 4.29. The mean of the latency is 0.017 s, with a maximum latency of 0.339 s, and a minimum latency of 0.270 s. The analog output latency is significantly higher than that of the digital output.

4.3.2.4 Test 8: Latency and jitter for multiple analog I/O

This test determines the latency and jitter of multiple analog I/O channels. Multiple input events trigger multiple output events. The latency of the events is measured. This configuration is represented schematically in Figure 4.30. Latency is represented as the time difference between time t1 and t2 in Figure 4.30. Latency jitter is represented as the time difference between the expected and the actual times, or t3 and t4 respectively.

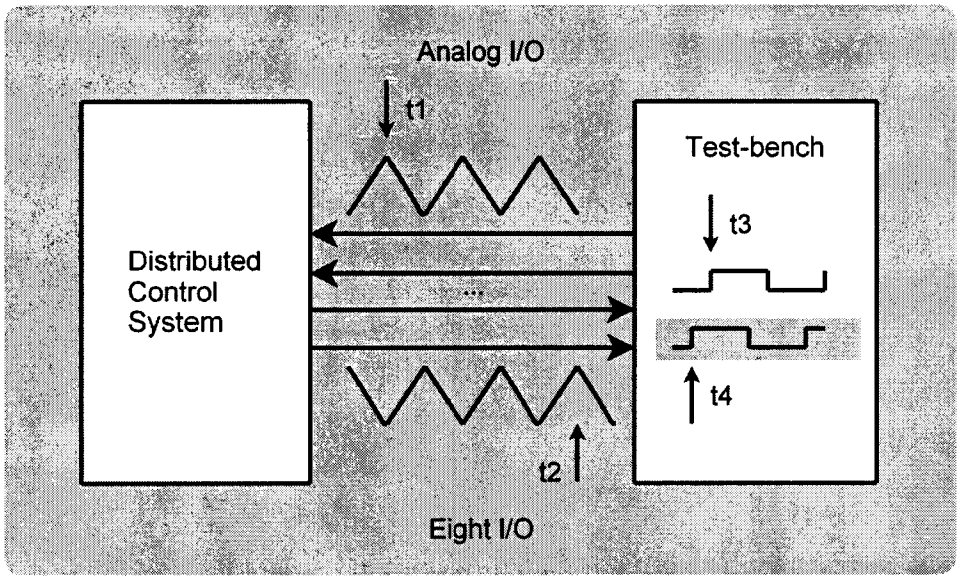


Figure 4.30: Schematic of multiple analog I/O latency and jitter

The test-bench analog output waveform is shown in Figure 4.31, starting from the far left at time 0.5 s and voltage 4 V. The DCS analog output waveforms start on the far left at time 0.5 s and voltage 3 V.

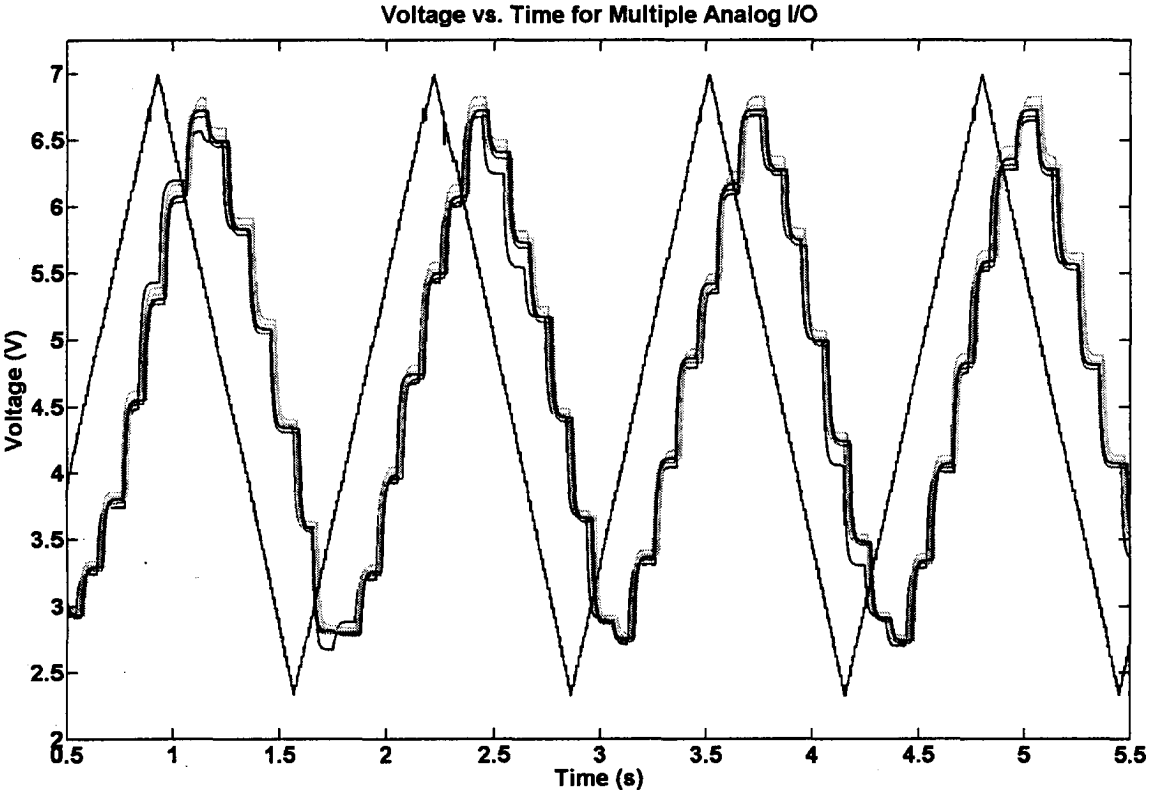


Figure 4.31: Multiple analog I/O waveforms

The mid-point of the output range is subtracted from the input and output to produce zero crossings. The zero crossings of the data are identified. The latency of the system is the time difference between the zero crossing of the input sequence and the output sequence. The latency is shown in Figure 4.32.

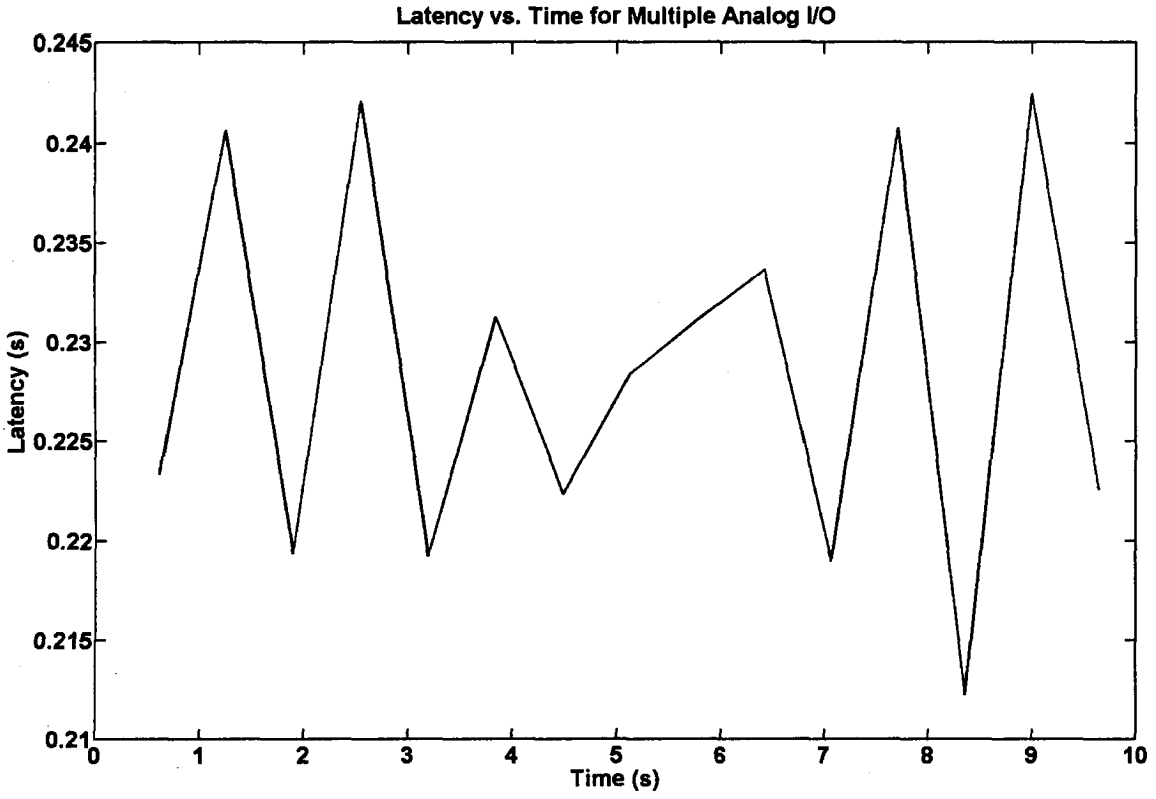


Figure 4.32: Multiple analog I/O latency

The latency and the jitter for multiple analog I/O are reduced by 27% from that of a single analog I/O. The latency jitter for a single analog I/O is shown in Figure 4.32. All of the analog I/O will be averaged to produce the final histogram.

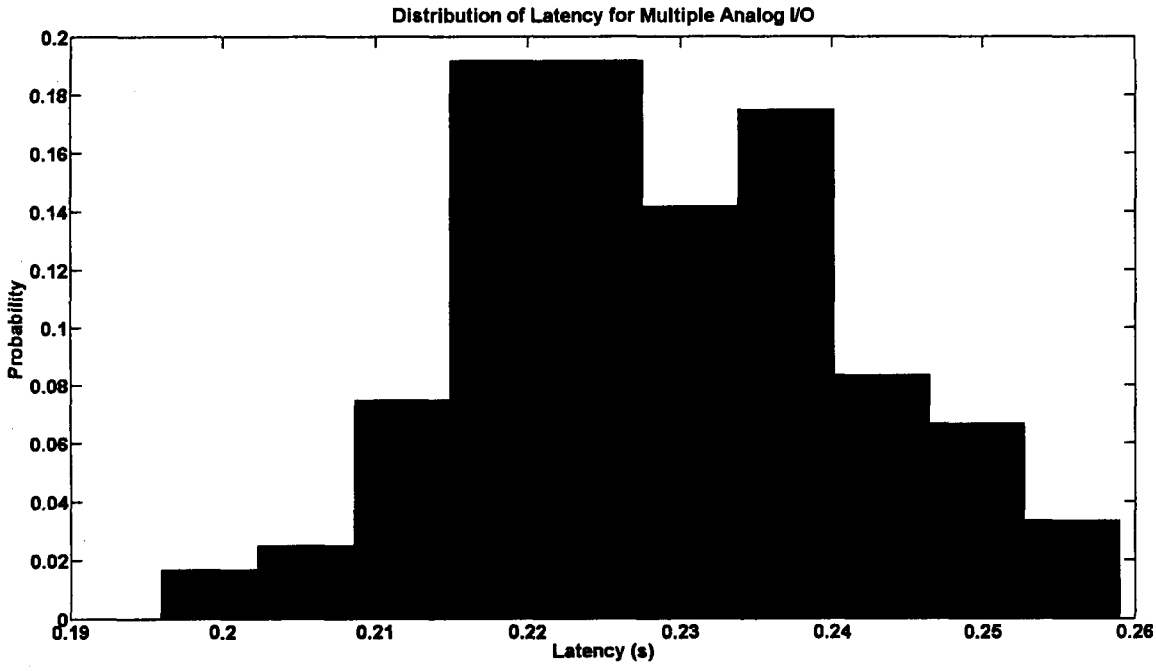


Figure 4.33: Multiple analog I/O jitter histogram

The latency has a mean of 0.229 s, and a standard deviation of 0.009 s. The minimum latency is 0.215 s, and the maximum latency is 0.242 s. The mean and standard deviation of the 8 analog I/O is less than that of a single channel. The reduction in latency may be due to the averaging of eight times more samples in the multiple analog I/O latency test

4.3.3 Modbus serial

4.3.3.1 Test 9: Throughput and jitter for a single Modbus output

This test measures the throughput and jitter of serial I/O using the Modbus protocol. The Modbus protocol is used to send single output values. Figure 4.34 represents the behaviour of the serial protocol. A write is sent by the Modbus master, and the Slave writes the value to a location in memory, called a register, and responds with an acknowledgement. The throughput is the rate at which writes can be delivered. Throughput is calculated as $1/\Delta t$, where Δt is represented as the difference between time

t1 and t2 in Figure 4.34. The Modbus write timing is measured using an instrumented Modbus client that was written specifically for the test-bench.

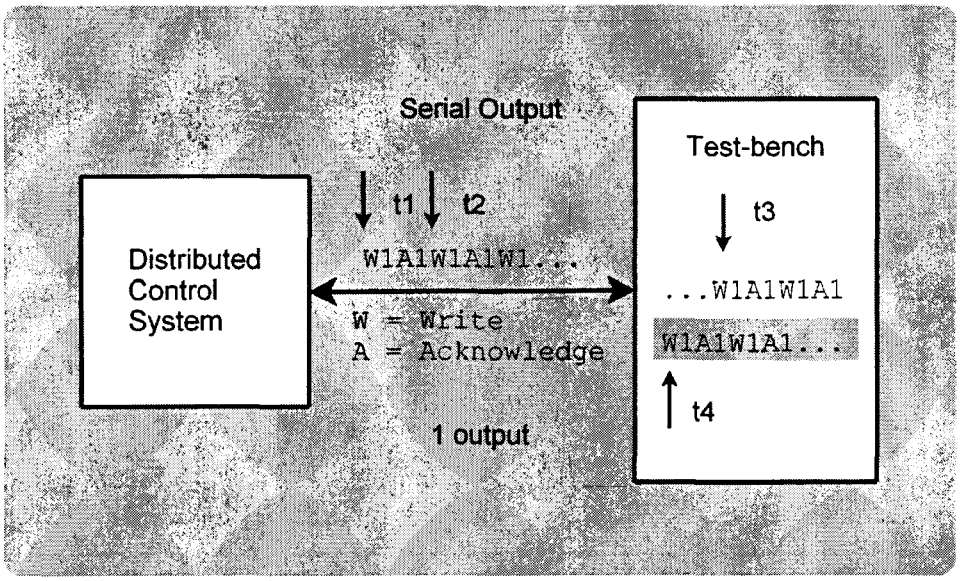


Figure 4.34: Schematic of serial output throughput and jitter

The difference between the expected and actual write times is the I/O jitter. It is represented as the time interval between t3 and t4 in Figure 4.34.

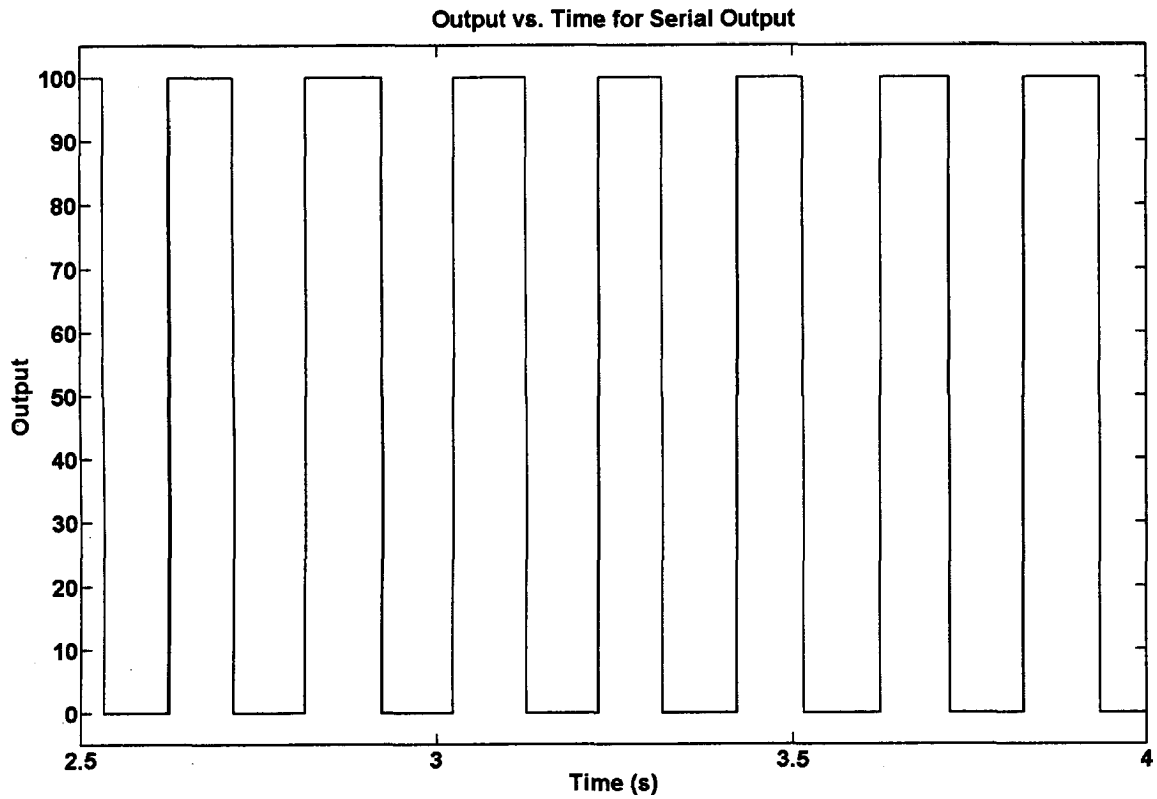


Figure 4.35: Single serial output waveform

The waveform of one serial output is shown in Figure 4.35. The output is the value written to the Modbus slave register.

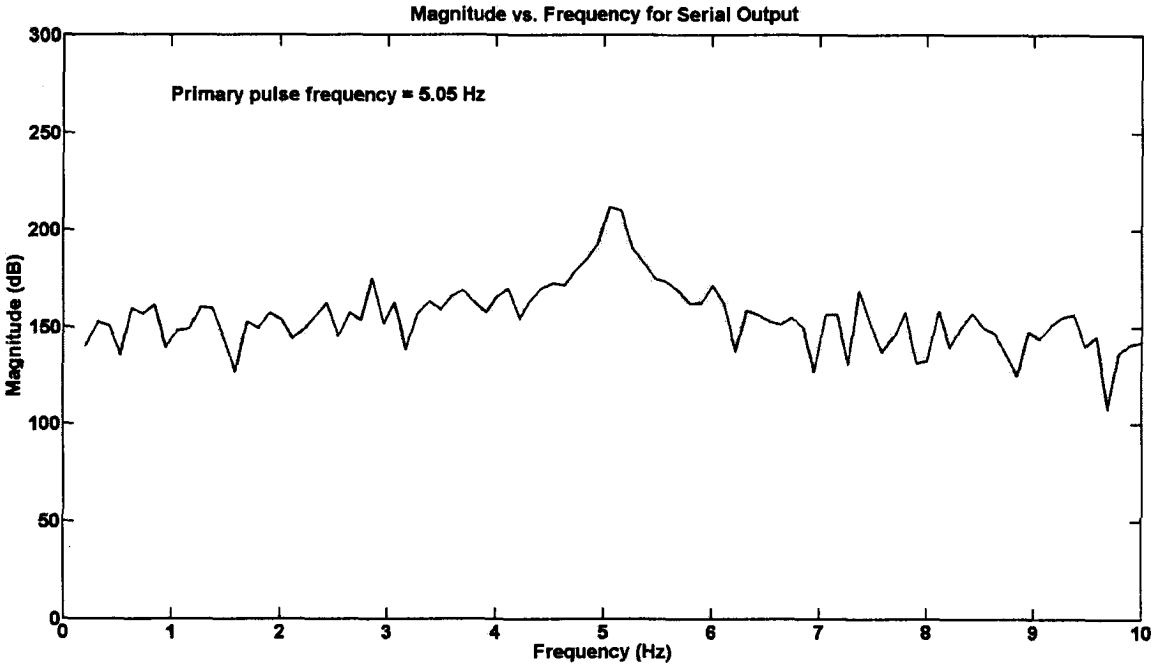


Figure 4.36: Single serial output FFT

The FFT of the serial output is shown in Figure 4.36, with a maximum throughput of 5.05 Hz. The throughput of 5.05 Hz is the same as the digital and analog channels.

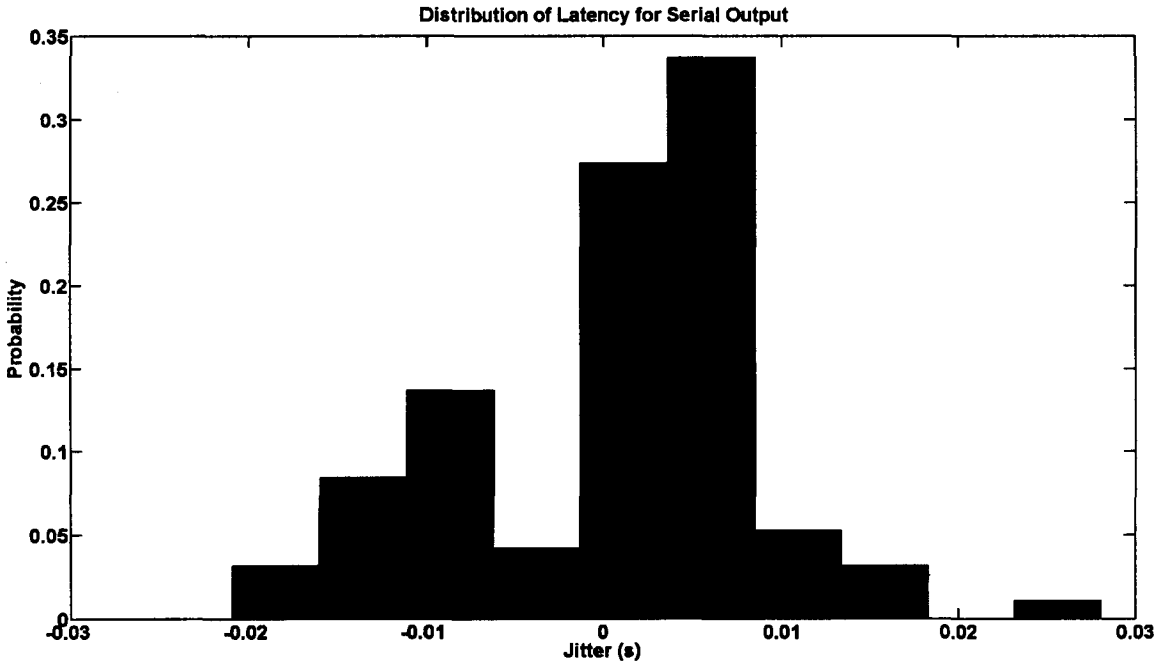


Figure 4.37: Single serial output throughput jitter histogram

The distribution of the jitter is shown in Figure 4.37. The jitter has a mean of 0.000 s, with a standard deviation of 0.008 s and a maximum of 0.028 s. The serial throughput jitter and maximum jitter are in part dependent on the Modbus slave implementation that is running on the test-bench. The test-bench Modbus slave must acknowledge write requests from the DCS and this in turn will affect the timing of subsequent writes. All tests were conducted with exactly the same Modbus slave implementation on the test-bench.

4.3.3.2 Test 10: Throughput and jitter for multiple Modbus outputs

The purpose of this test is to measure the throughput of multiple Modbus outputs. The communication between the DCS and the test-bench is divided into two asynchronous communication channels, one channel between the DCS and the serial output card, and another between the serial output card and the test-bench. The serial output card on the DCS updates all Modbus slaves asynchronously. The DCS updates the serial output card asynchronously. The serial output card update rate is presented in the following figures.

The serial output card update rate is more than twice the DCS update rate. The serial output card is super-sampling the values from the DCS and sending them to the Modbus clients. The Nyquist sampling criteria is held between the DCS, the serial output card, and the test-bench.

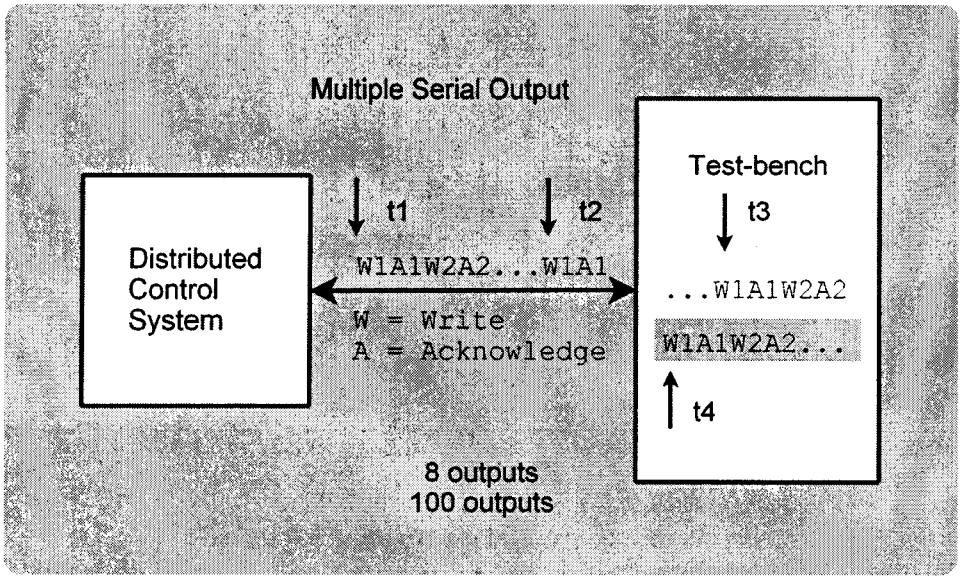


Figure 4.38: Schematic of multiple serial output throughput and jitter

The sequence of writes and acknowledgments for all the outputs is represented in Figure 4.38. The throughput is proportional to the time between t1 and t2 in Figure 4.38. The jitter is represented by the difference between the actual and expected time represented by t3 and t4 respectively.

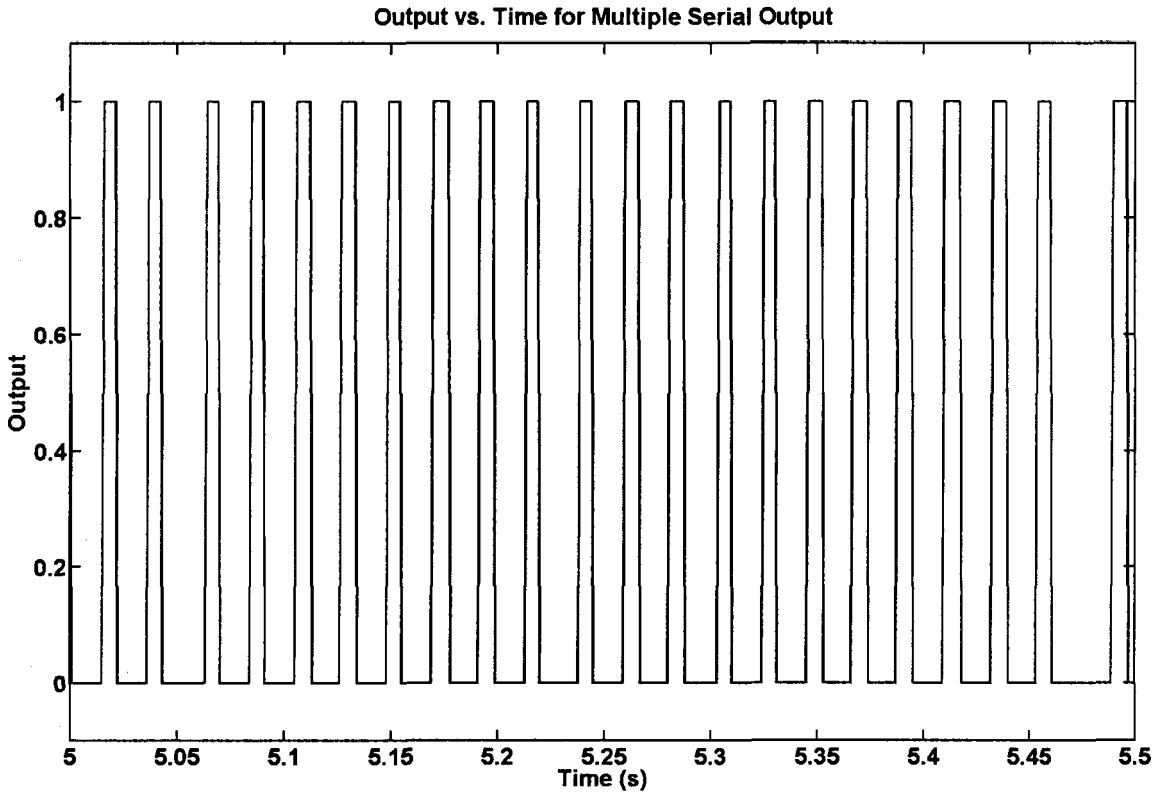


Figure 4.39: Eight serial output waveforms

The update rate for 8 serial output is shown in Figure 4.39. Each square pulse is a set of 8 output Modbus protocol writes and their associated acknowledgments. The throughput of the 8 serial outputs is 4.95 Hz.

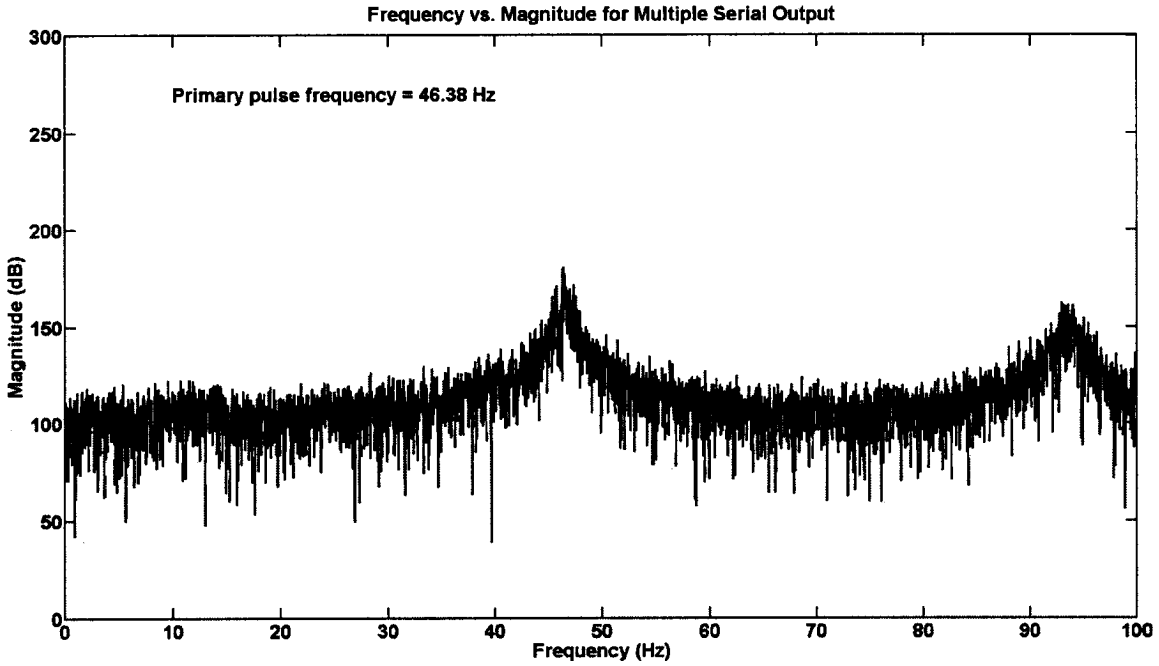


Figure 4.40: Eight serial output FFT

The FFT of the serial output write rate is shown in Figure 4.40. The write throughput between the serial output card and the test-bench is 46.38 Hz. One cycle requires two writes, and therefore the throughput of one value is 23.19 Hz. The DCS update rate is only 4.95 Hz, and therefore the extra updates are redundant.

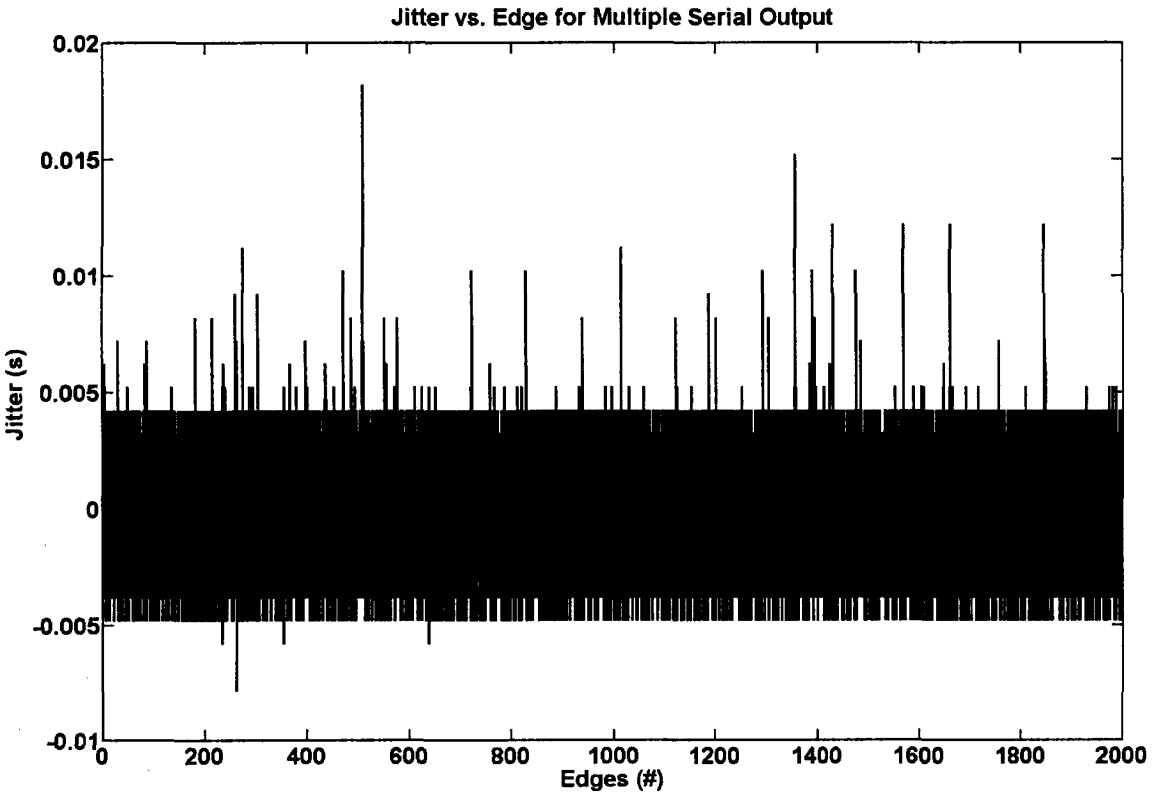


Figure 4.41: Eight serial output throughput jitter

The jitter for each of the 8 outputs is concatenated and the mean is computed. The standard deviation of the jitter is 0.004 s. The jitter for the 8 serial output is shown in Figure 4.41.

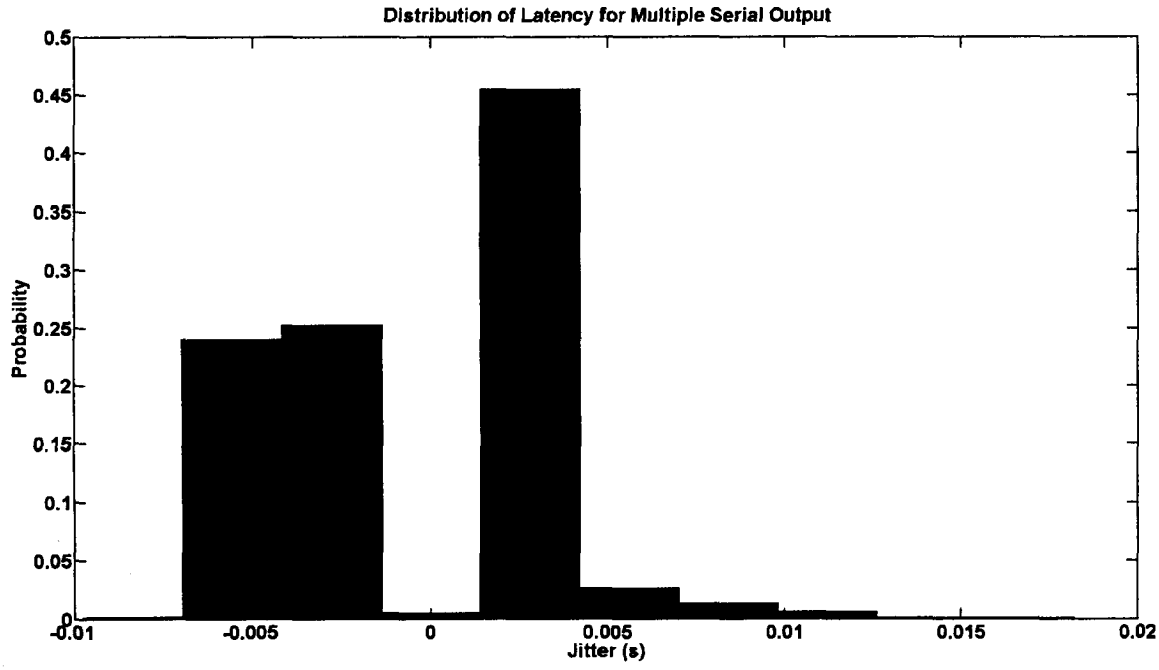


Figure 4.42: Eight serial output throughput jitter histogram

The deviation of the jitter for 8 serial outputs is shown in Figure 4.42. The mean jitter is 0.000 s, with a standard deviation of 0.004 s and a maximum jitter of 0.018 s. The serial outputs are either 0.004 s early or late, but are not normally distributed between the range (-0.004,0.004).

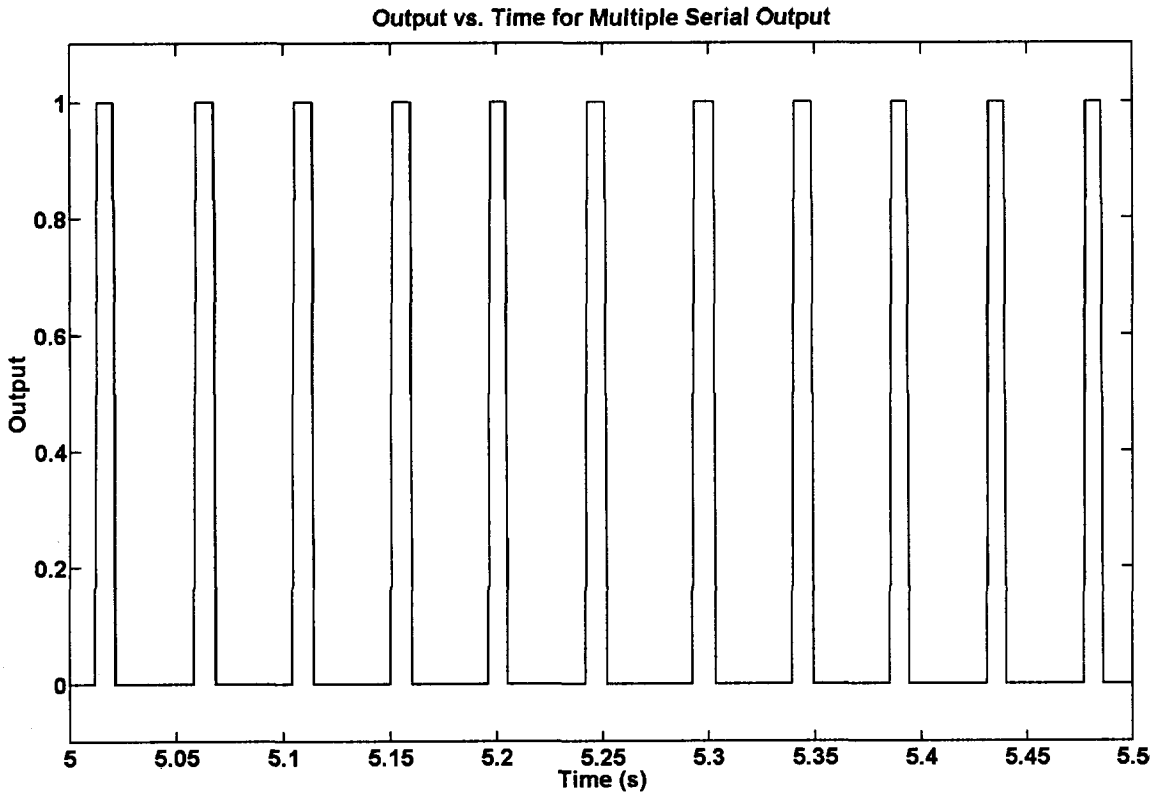


Figure 4.43: One hundred serial output waveform

The DCS maximum of 100 serial outputs is tested. Each pulse in Figure 4.43 is the duration of 100 serial Modbus protocol output writes and their associated acknowledgments. The DCS processing, and protocol handling constitutes the time between pulses. The write throughput between the serial I/O and test-bench for 100 outputs is 2.14 times slower than 8 serial outputs, but the value throughput remains 4.95 Hz.

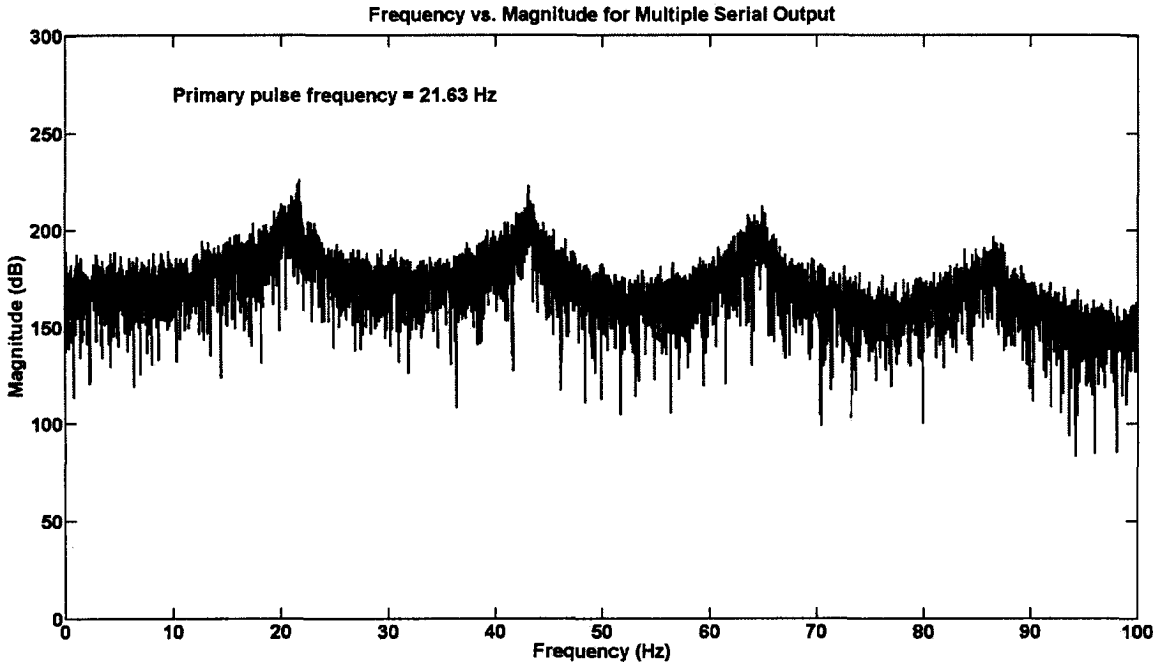


Figure 4.44: One hundred serial output FFT

The FFT of 100 serial write outputs is shown in Figure 4.44. The write throughput of 100 serial outputs is 21.63 Hz. One cycle requires two writes therefore the maximum throughput of one value output is 10.8 Hz. Reading 100 outputs approaches the limit of the serial card, if the sampling rate drops below 10.1 Hz, twice the DCS update rate of 5.05 Hz, then the Nyquist criteria will not be met and the DCS values will not be sampled correctly by the serial I/O card.

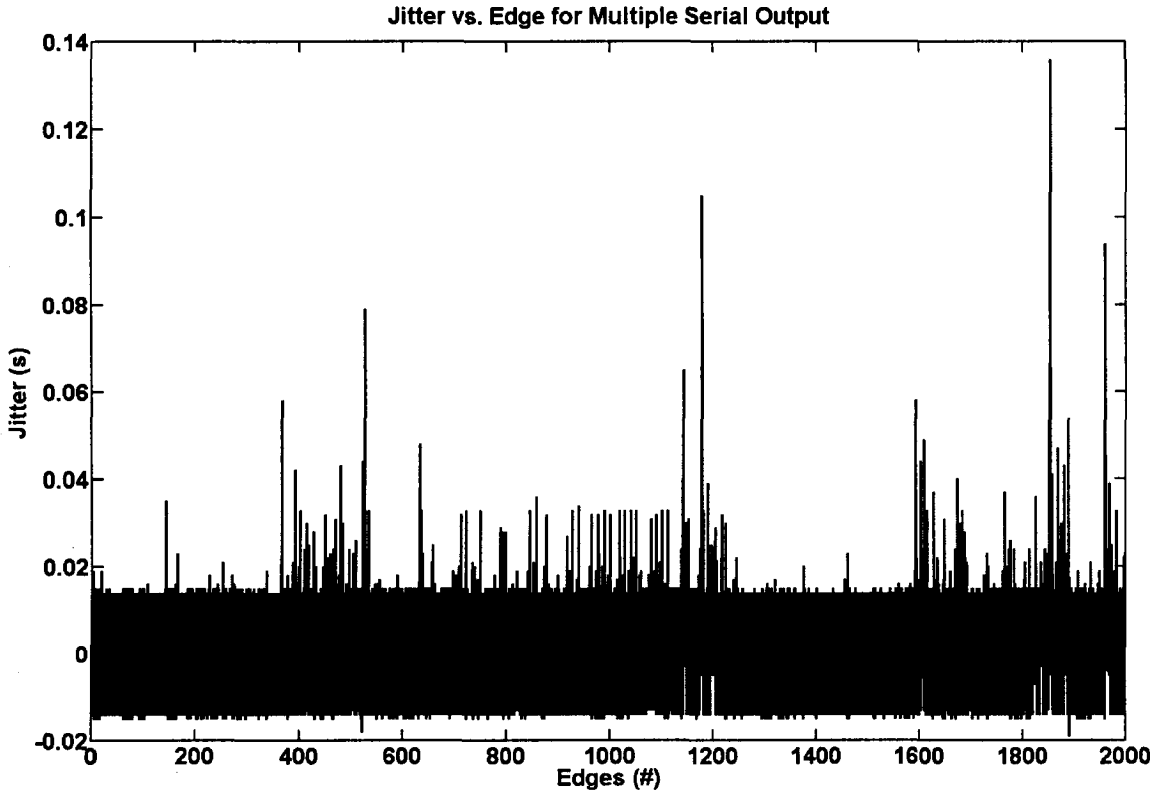


Figure 4.45: One hundred serial output throughput jitter

The throughput jitter for 100 serial outputs is shown in Figure 4.45. The standard deviation in this case is 4.0 times larger than the jitter for 8 serial outputs shown in Figure 4.41. The write throughput decreases by a factor of 2.14 when the number of outputs increases by 12.5 times. As an upper bound, while avoiding under-sampling, and linearly extrapolating using the previous factors, the serial output card may update no more than 105 outputs.

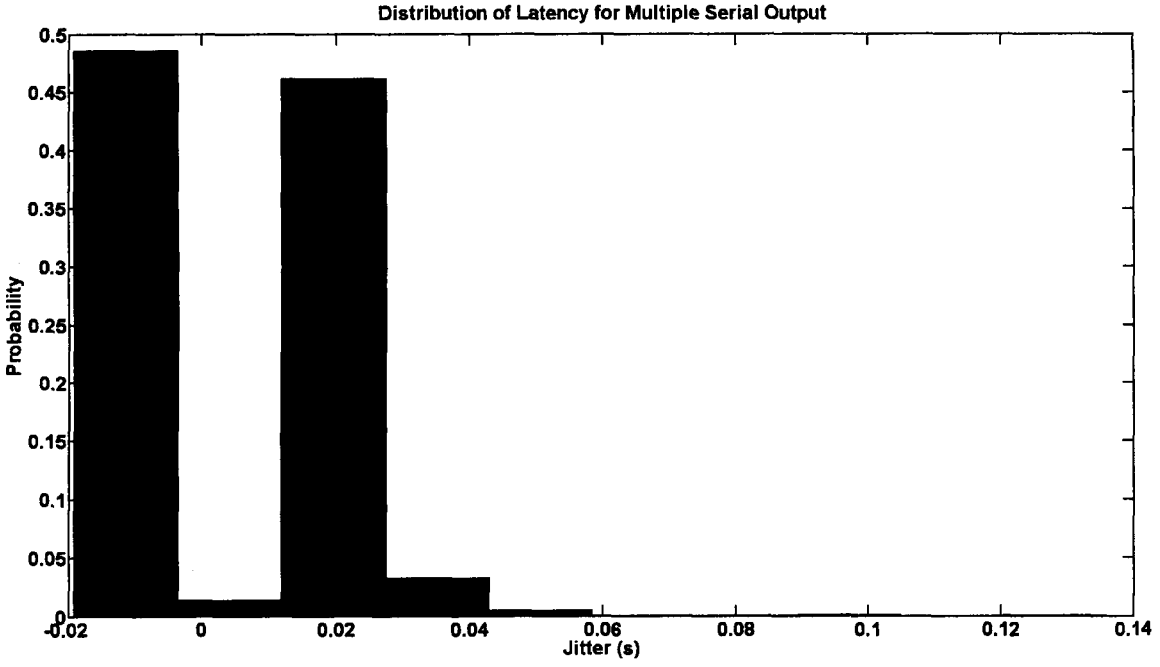


Figure 4.46: One hundred serial output throughput jitter histogram

The distribution of the jitter for 100 serial outputs is shown in Figure 4.46. The mean jitter is 0.001 s, with a standard deviation of 0.016 s and a maximum jitter of 0.136 s.

The value throughput for 8 Modbus outputs is the same as that for 100 Modbus outputs. This test demonstrates that the serial output card updates Modbus slaves asynchronously from the DCS updates, and at different rates dependent on the number of outputs. The serial I/O write throughput is greater than twice the DCS value throughput to maintain the Nyquist sampling criteria.

4.3.3.3 Test 11: Latency and jitter for a single Modbus I/O

The purpose of this test is to measure the latency of a single Modbus I/O. The DCS is the Modbus master, and the test-bench is the Modbus slave. The test-bench writes a value into the slave register and measures the time taken by the DCS to copy the value to a different register.

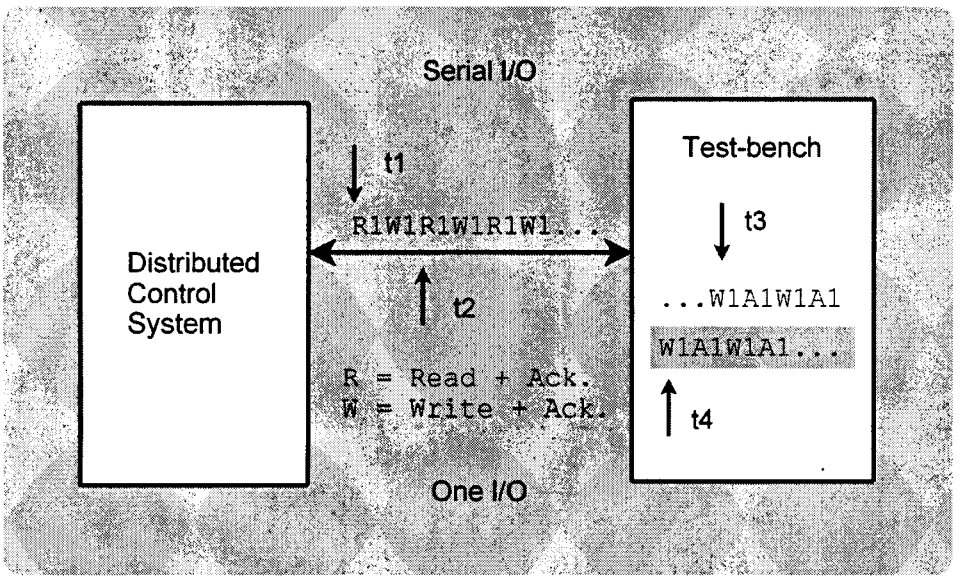


Figure 4.47: Schematic of single serial I/O latency and jitter

The latency is represented as time between the read of one register and the write to the second register, shown as the time between t1 and t2 in Figure 4.47. The latency jitter is the difference between the expected write and the actual write, show as the time between t3 and t4 in Figure 4.47.

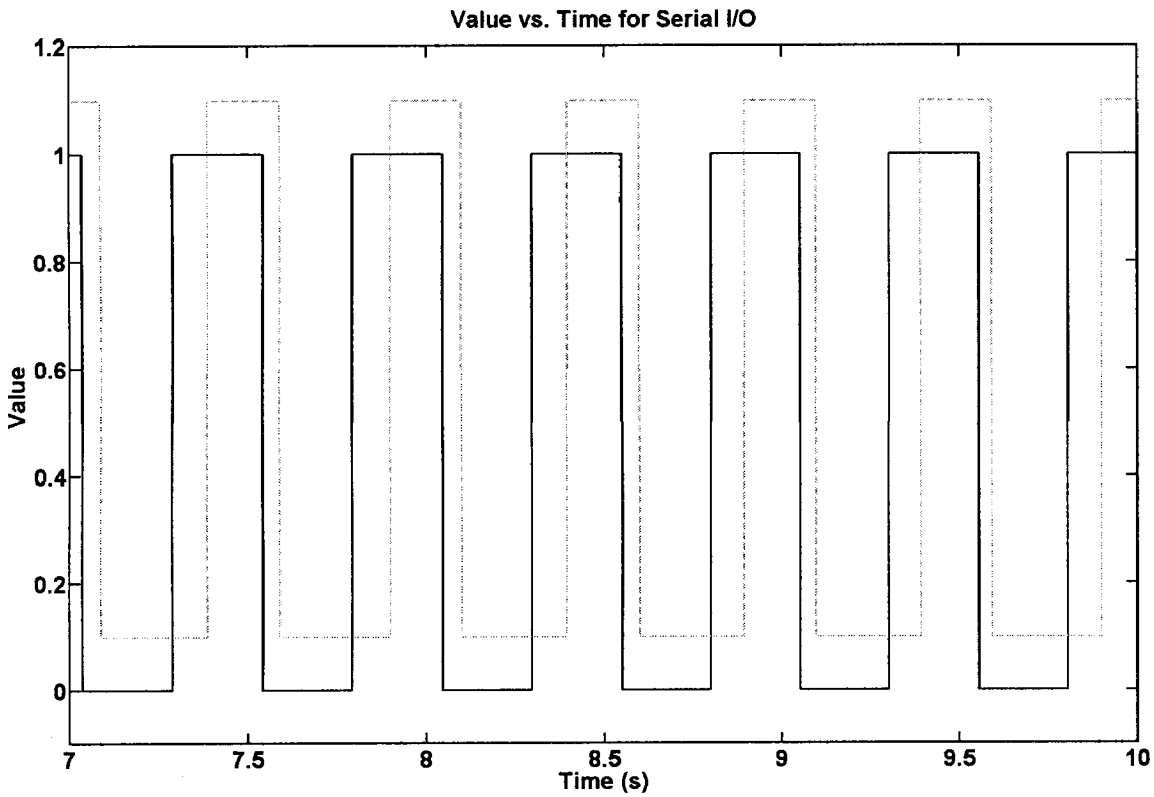


Figure 4.48: Single serial input vs. output

The input, in a solid line, and the resulting output from the DCS, in a dashed line, are shown in Figure 4.48. In the figure the sold and dashed lines represents the value of two unique Modbus registers used in the test. The output is offset such that the differences are easily distinguishable.

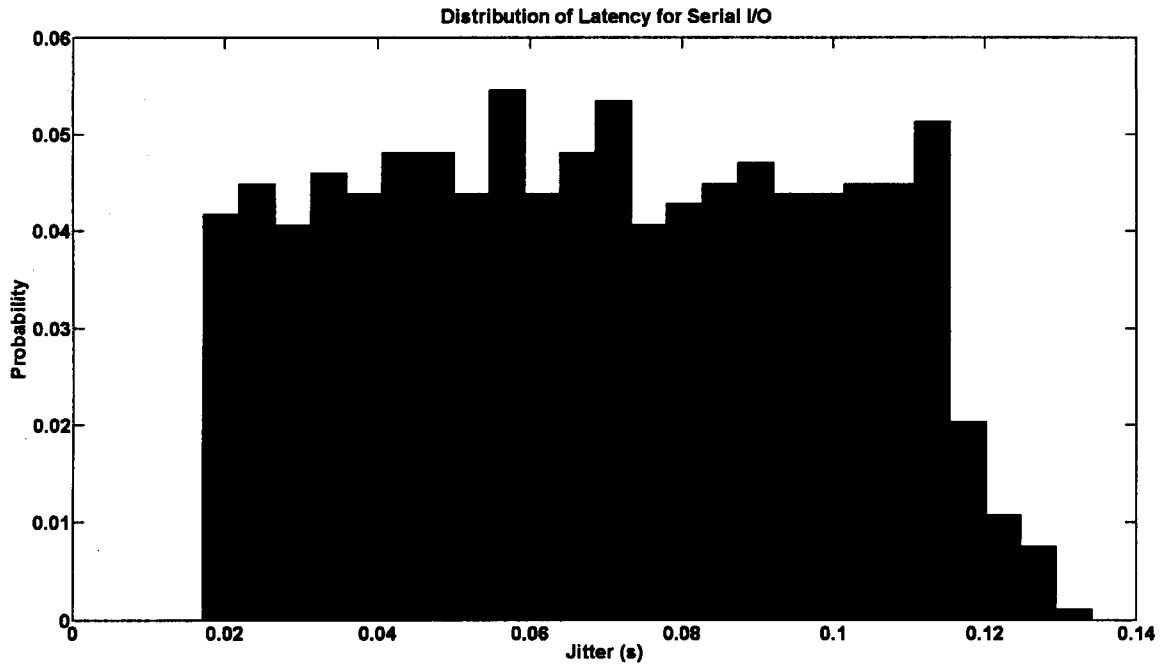


Figure 4.49: Single serial I/O latency histogram

The distribution of the latency jitter is shown in Figure 4.49. The mean latency is 0.072 s with a standard deviation of 0.029 s. The latency is the same as that of a single digital channel within a 1% threshold.

4.3.3.4 Test 12: Latency and jitter for multiple Modbus I/O

The purpose of this test is to measure the latency of a multiple Modbus I/O. The DCS is the Modbus master, and the test-bench is the Modbus slave. The test-bench writes multiple values into multiple sequential slave registers and measures the time taken by the DCS to copy all values to a different set of sequential slave registers.

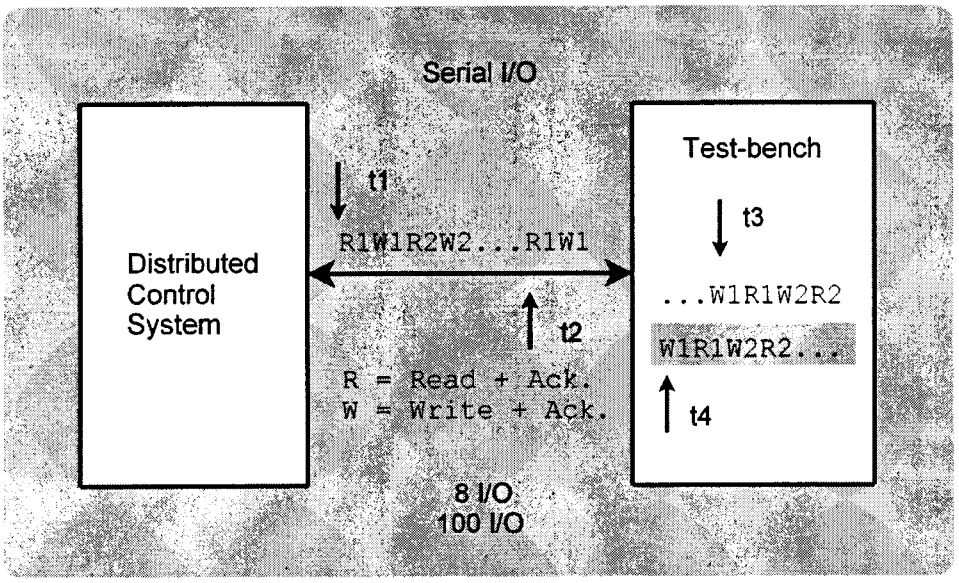


Figure 4.50: Schematic of multiple serial I/O latency and jitter

The test-bench configuration for measuring the latency of 8 I/O is represented in Figure 4.50. The latency of a single I/O is the time between the read of one register and the write to the second register, shown as the time between t1 and t2 in Figure 4.50, while the jitter is the difference between the expected write and the actual write, show as t3 and t4 respectively.

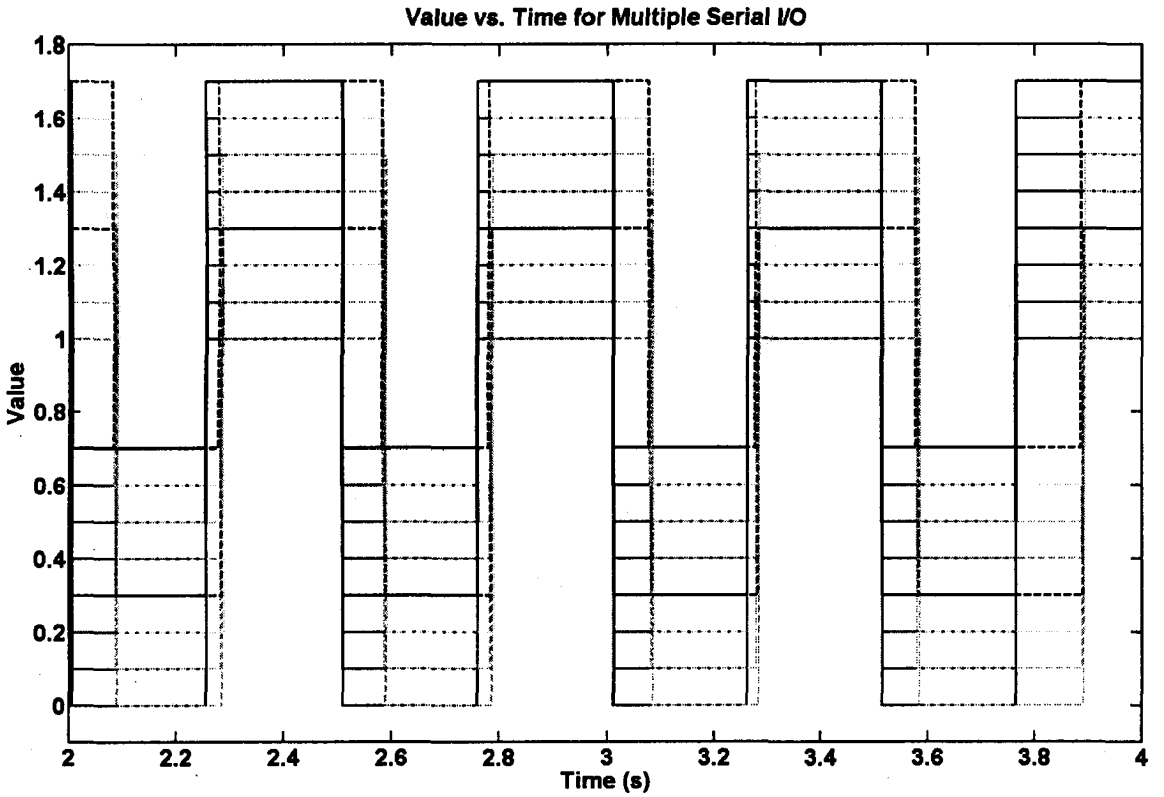


Figure 4.51: Eight serial I/O waveforms

Eight serial I/O, with solid lines as inputs and dashed lines as outputs are shown in Figure 4.51. All 8 output Modbus registers are changed at the same time, and the changes in the 8 input registers are monitored.

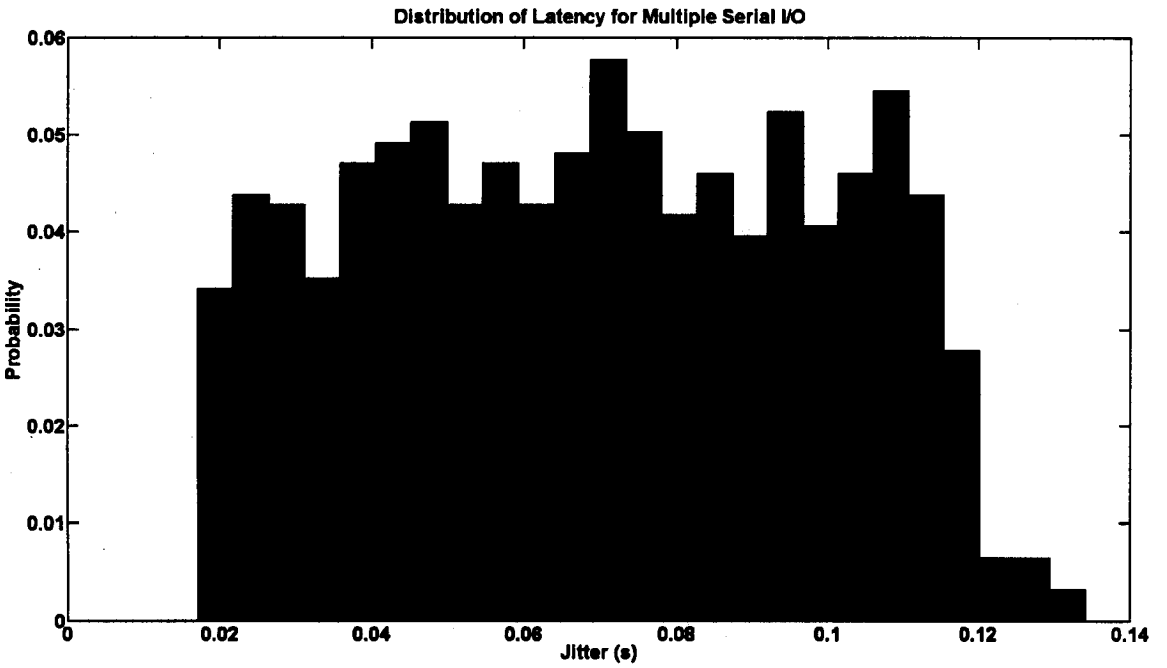


Figure 4.52: Eight serial I/O latency histogram

A distribution of the latency jitter is shown in Figure 4.52. The mean latency is 0.079 s, and the standard deviation is 0.029 s. The latency for 8 serial I/O is the same as that for 1 serial I/O within a 1% threshold.

4.3.4 OPC Ethernet

4.3.4.1 Test 13: Throughput and jitter for one OPC output

This test measures the throughput and jitter of one OPC output over 100Mbit Ethernet. The DCS is configured to change an internal register value as quickly as possible between an "on" and "off" state. The engineering workstation is configured as an OPC server and retrieves the DCS internal register value. The test-bench is configured as an OPC client and reads the DCS internal register value from the OPC server copy.

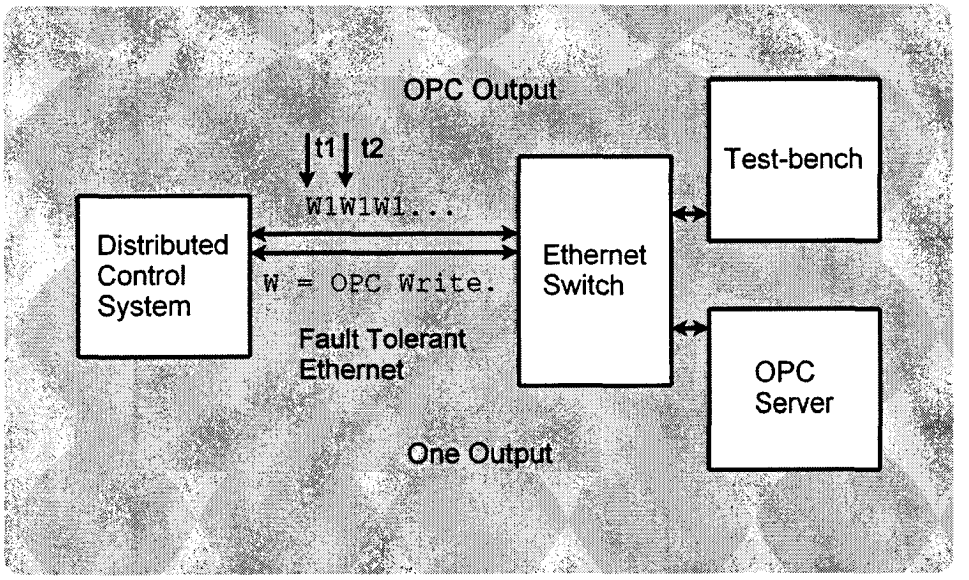


Figure 4.53: Schematic of Ethernet OPC output

The test-bench configuration is shown in Figure 4.53. The throughput for the OPC output is the time difference between t1 and t2 in Figure 4.53.

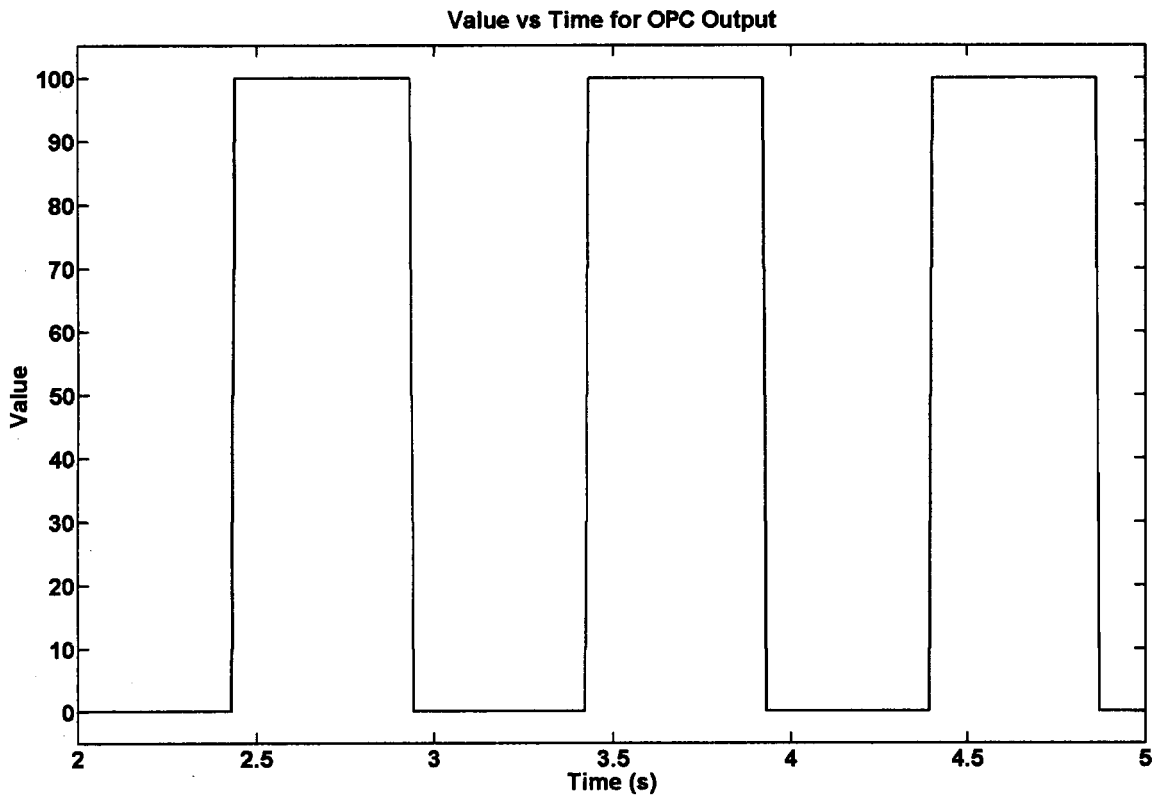


Figure 4.54: Single OPC output waveform

The output waveform is output at a maximum rate from the DCS. A sample OPC output waveform is shown in Figure 4.54. The test-bench captures the OPC output waveform from the OPC server.

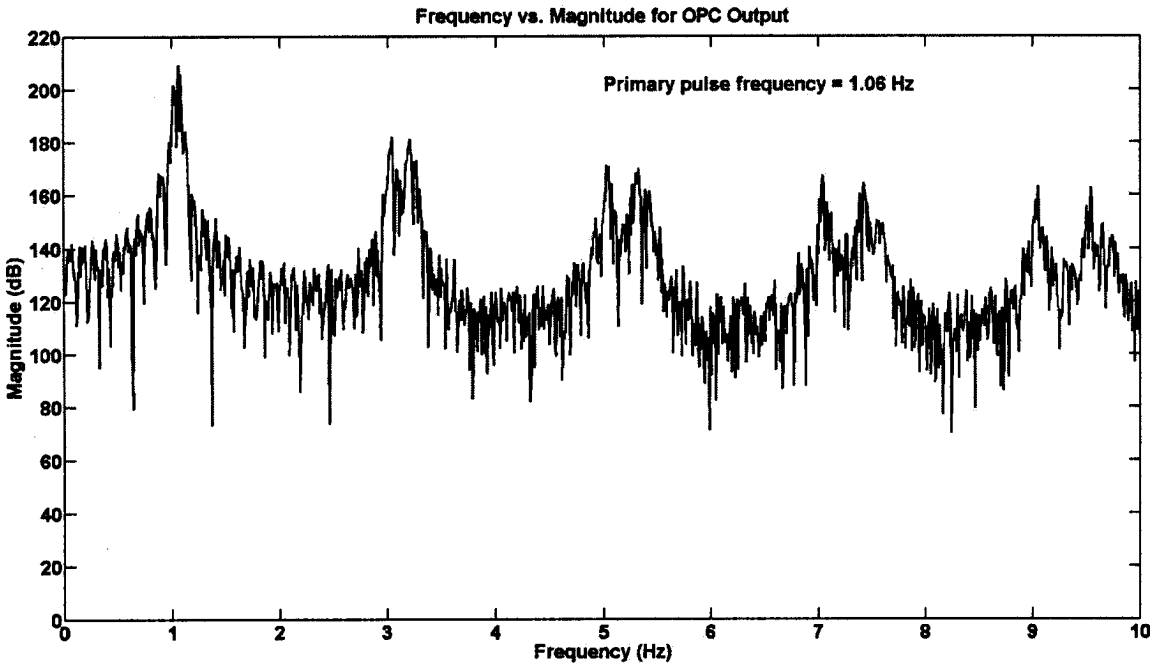


Figure 4.55: Single OPC output FFT

The throughput of the OPC output is 1.06 Hz as shown in the output waveform FFT in Figure 4.55. The OPC output is 4.8 times slower than 1 digital output.

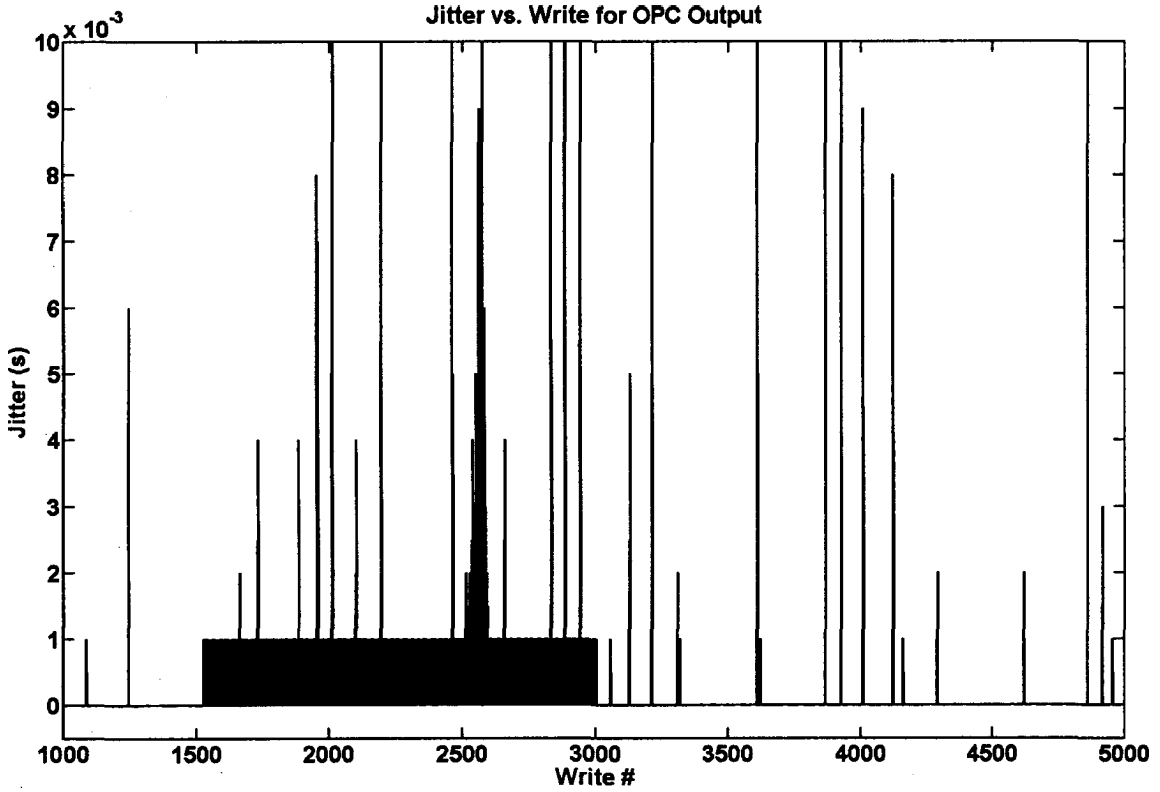


Figure 4.56: Single OPC throughput jitter

The mean OPC throughput jitter is 0.000 s, with a standard deviation of 0.004 s. The worst case jitter is 0.337 s.

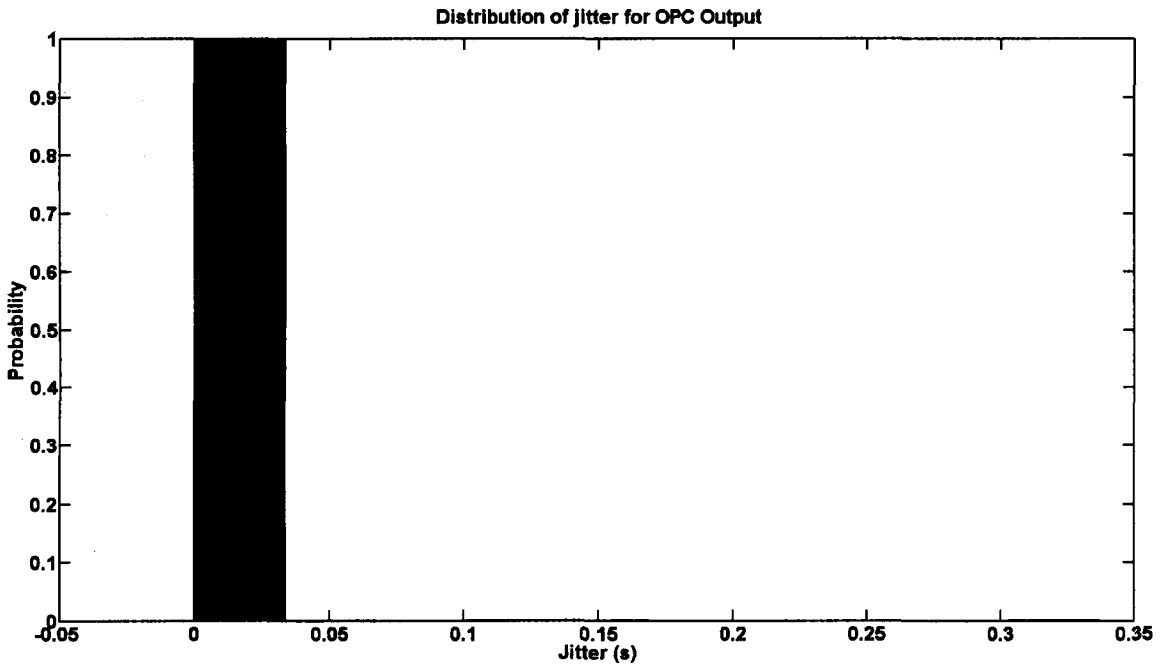


Figure 4.57: Single OPC throughput jitter histogram

The distribution of the OPC output throughput jitter is shown in Figure 4.57. There is a non-zero probability that the OPC output jitter can be as high as 0.337 s.

The OPC output over switched 100 Mbit Ethernet provides an output with 0.000 s mean jitter. The OPC output is the slowest, but has the smallest jitter, and is therefore the most deterministic.

4.3.5 Digital PID

The following tests involve a nuclear power plant SG simulation. The physical parameters of the boiler are taken from the CANDU 6 designs, and the operating levels are taken from the full power steady state parameters used in the OPG NPP simulator. This configuration is shown schematically in Figure 4.58, which represents the control executing on the DCS hardware, connected via serial I/O to the test-bench, connected via TCP/IP to the Matlab simulation, all in real-time.

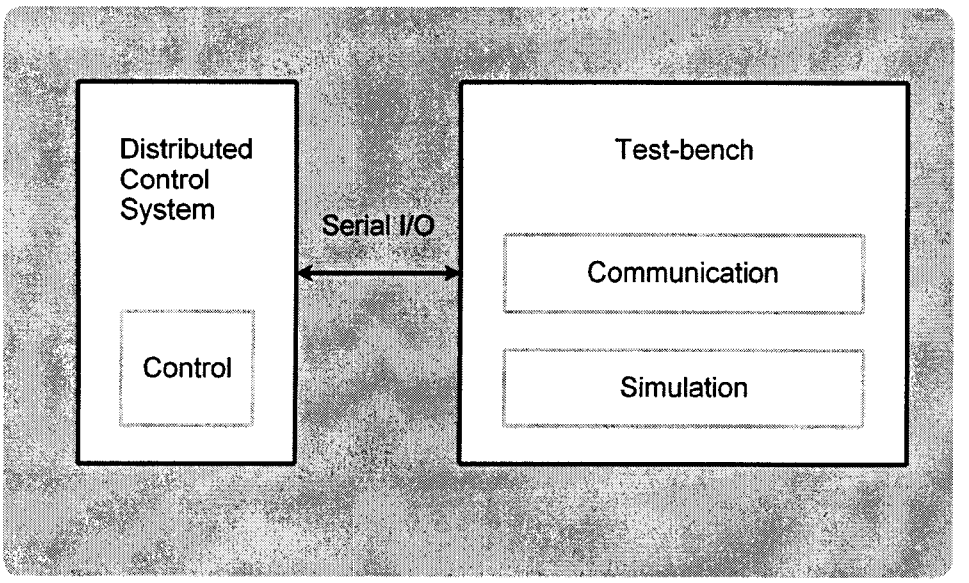
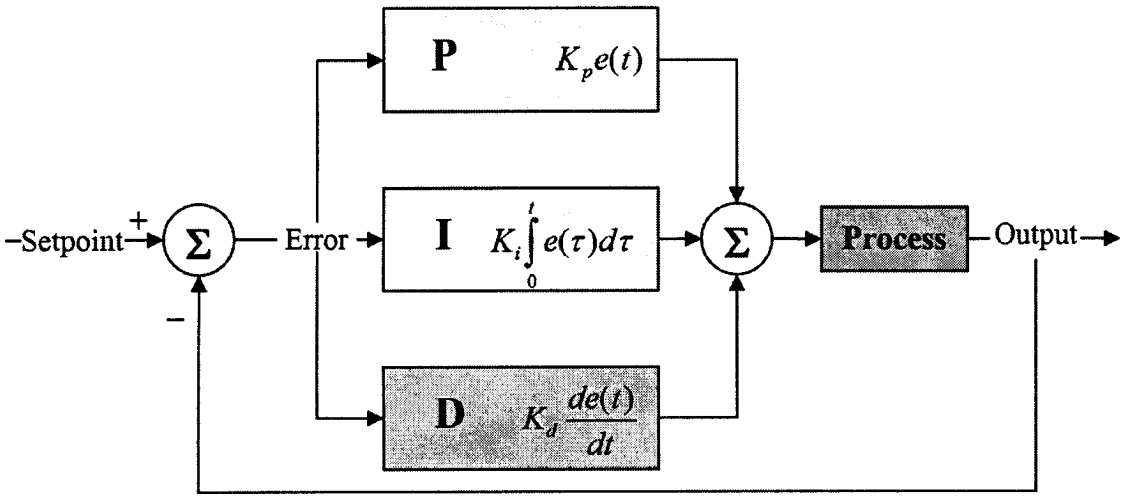


Figure 4.58: Schematic of real-time control and simulation

The parameters include reactor output in joules, SG water level in meters, steam flow rate in kg/s, and feed-water flow rate in kg/s at full power. These parameters were used to stabilize the non-linear SG equations between 70% and 100% power. Reactor power and steam load are SG model inputs. The feed-water valve position is the control output. The generator water level and pressure are model outputs.

The SG is simulated in real-time with Matlab. A communication link between Matlab and the controller is established using a Modbus serial link. The controller runs a PID control loop for the level control of the SG. The PID loop was tuned using the DeltaV Tune software with an automated Ziegler-Nichols closed-loop method. The controller parameters are gain, reset and rate. There is no unit for the gain. The reset is the parameter corresponding to the integral term. The reset is the time taken for an integral control component to move output by the same percent as the gain, given a step input. The reset has a unit of seconds. The rate is the parameter corresponding to the derivative term. The rate is the time difference between an output change without a derivative and an output change with a derivative term. The rate is measured in units of seconds. The PID equation is as follows:



These tests are derived from tests in [49], but the control variables have been changed slightly. The first three tests, 14, 15 and 16 are controller responses to adjusting the level set-point with a step change. The next three tests, 17, 18, and 19 simulate increases in SG load. In these two scenarios, both the changes in level set-point and the load are required in the overall operation of any reactor.

4.3.5.1 Test 14: Water level set-point change by 10%

The purpose of this test is to examine the behaviour of the DCS under the following conditions: known stability gain and phase margins, PID tuning using gain and phase margins, and moving the set-point using a step change

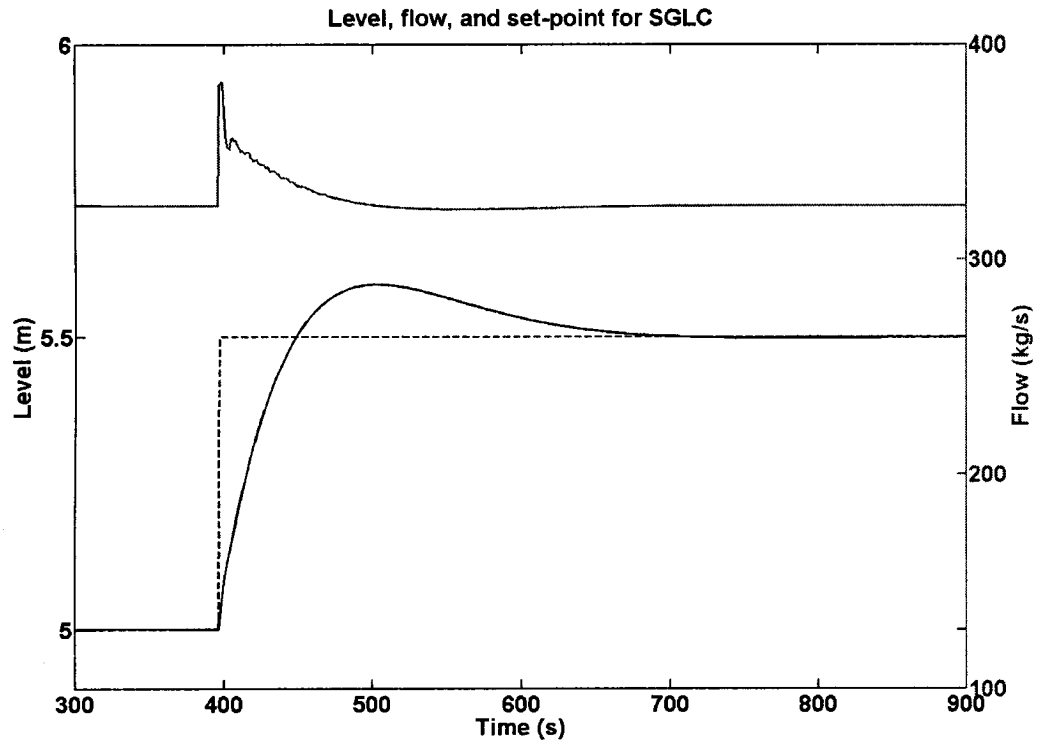


Figure 4.59: Water level set-point change by 10%

The test begins with the reactor output power at 100%. The water level set-point is 5 m above the risers. Before the test begins the controller is allowed time to bring the level to the set-point. The set-point is then increased by 10% to a level of 5.5 m. The ideal set-point, SG level, and feedwater flow values are shown in Figure 4.59.

The gain is at 1.12, with a reset at 83.64 s, and rate at 13.34 s. The time to stabilize was 323 s (tolerance 1%), with an overshoot of 1.6% (5.59 m). The maximum allowable overshoot is 45% (8 m) before reaching the clearance to the steam outlet.

It takes on average 323 seconds to stabilize a 10% level set-point change. The controller cannot use gain to create a large overshoot since this could cause water to enter the steam lines above the UTSG. The overshoot is 0.09 m and below the 8 m clearance to the steam outlet.

4.3.5.2 Test 15: Water level set-point change by 20%

The purpose of this test is to examine the behaviour of the DCS under the following conditions: known stability gain and phase margins, PID tuning using gain and phase margins, and moving the set-point using a step change.

The test begins with the reactor output power at 100%. The water level set-point is 5 m above the risers. Before the test begins the controller is allowed time to bring the level to the set-point. The set-point is then increased by 20% to a level of 6.0 m. The ideal set-point and the true level are shown in Figure 4.60.

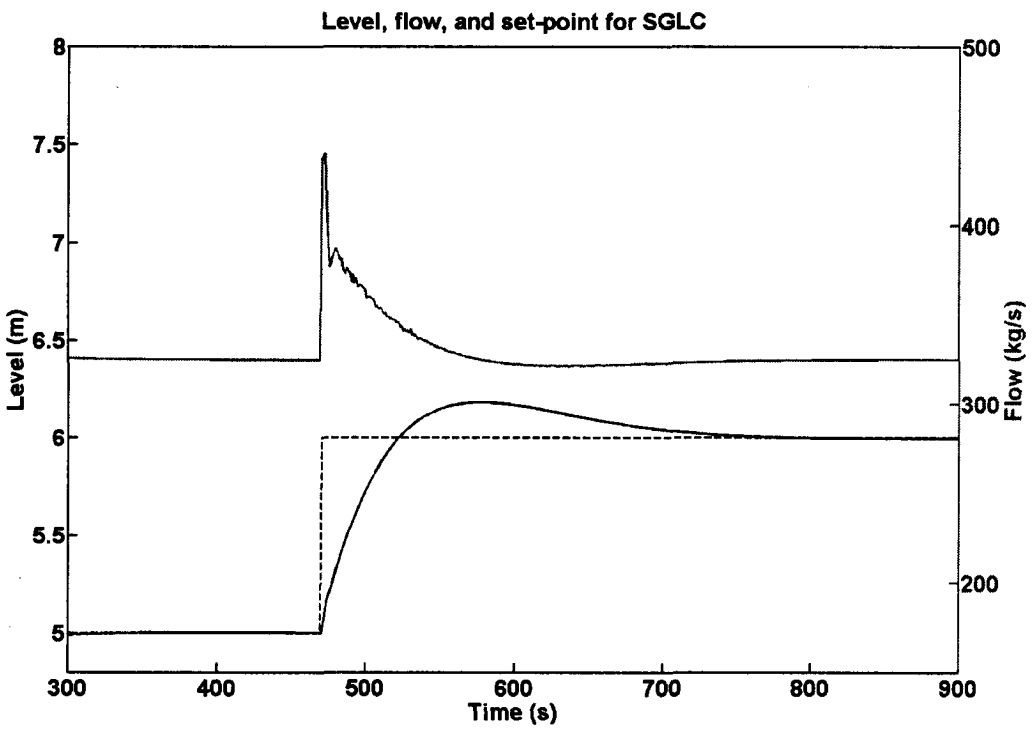


Figure 4.60: Water level set-point change by 20%

The time to stabilize is 324 s (tolerance 1%) with an overshoot of 3% (6.18 m). The maximum allowable overshoot is 33% (8 m). The DCS control loop successfully prevents the water level from reaching the steam outlet.

4.3.5.3 Test 16: Water level set-point change by 30%

The purpose of this test is to examine the behaviour of the DCS under the following conditions: known stability gain and phase margins, PID tuning using gain and phase margins, and moving the step set-point using a step change.

The test begins with the reactor output power at 100%. The water level set-point is 5 m above the risers. Before the start of the test the controller is allowed time to raise the level to the set-point. The set-point is then increased by 30% to a level of 6.5 m. The ideal set-point and the true level are shown in Figure 4.61.

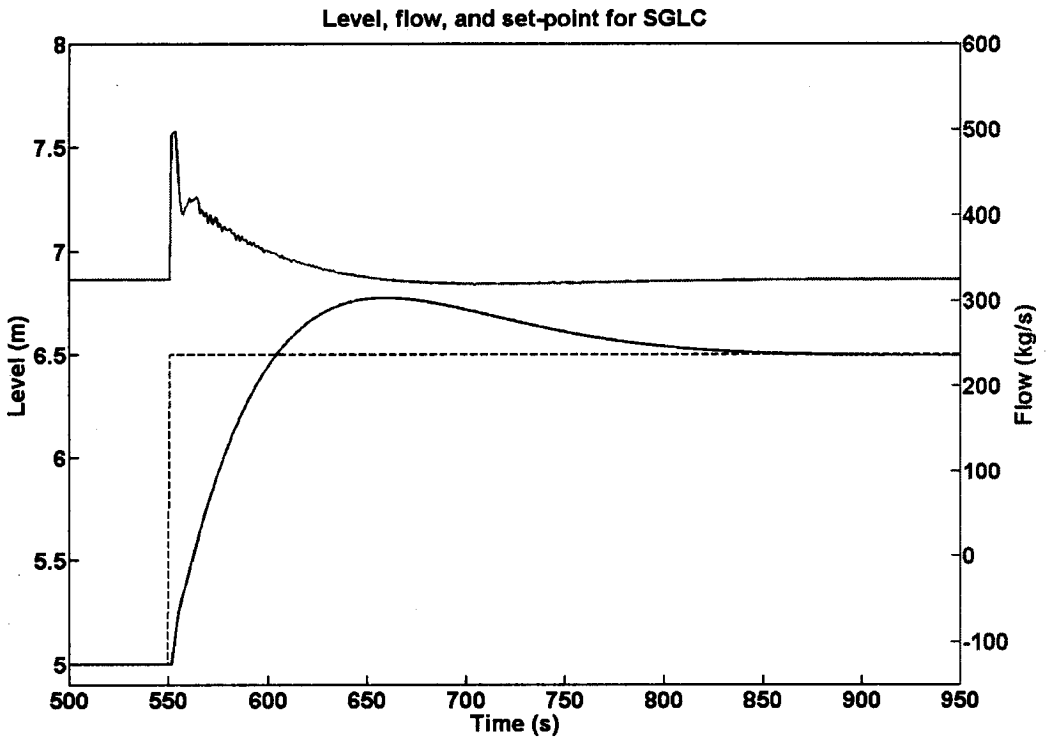


Figure 4.61: Water level set-point change by 30%

The time to settle is 326 s (tolerance 1%), with an overshoot of 4.2% (6.77 m). The maximum allowable overshoot is 23% (8 m). The DCS control loop successfully prevents the water level from reaching the steam outlet.

4.3.5.4 Test 17: Flow rate change by 10%, reactor step 10%

The purpose of this test is to examine the response of the tuned controller to load changes. It is the responsibility of the steam generator pressure control (SGPC) to coordinate reactor power to maintain steam generator pressure. The independent SGLC in this case will attempt to maintain generator level.

The reactor safety limits approach unacceptable values for tests 17-19. A normal reactor power increase of 10-15% percent would mean that the reactor is operating at 75-80% of full power. At any level above 60% full power the adjuster rods can compensate for Xenon buildup during load changes [51]. At high power the steam generator pressure control program will change the reactor set-point such that it will behave like a reactor-follows-turbine system. In a reactor-follows-turbine scenario the reactor output power is adjusted to accommodate for turbine steam load. In steady state the SGPC program is limited to 5% reactor power increase from the current set-point. The SGPC in this scenario will allow up to 15% increases in reactor output power. The tuned controller gain is 2.14, with a reset of 29.17 s, and a rate of 4.67 s.

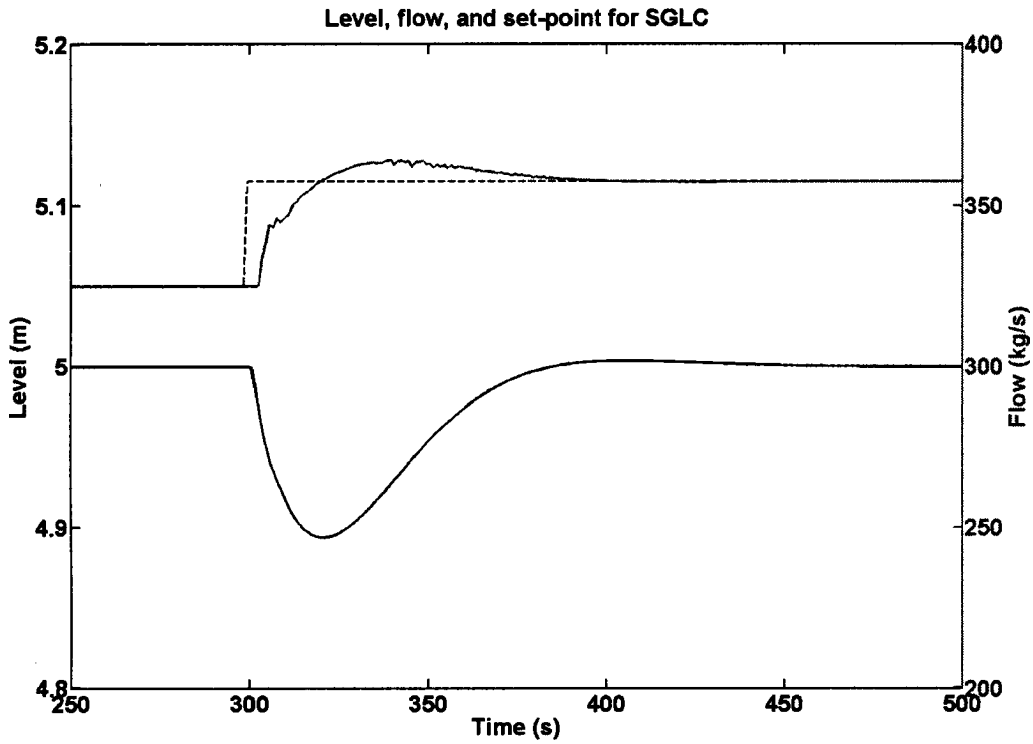


Figure 4.62: Flow rate change by 10%, reactor step 10%

The time to stabilize is 172 s, with an overshoot of 0.06% (5.003m) and an undershoot of 2.2% (4.89 m). The maximum overshoot is 60% (8 m) and the maximum undershoot is 100% (0 m). The DCS control loop successfully prevents the water level from exposing the boiler tubing.

This test indicates that a low-level is as much as a problem a high level. At maximum undershoot the heat exchange tubing is exposed, leading to overheating and possible damage of the steam generator. In tests 14, 15, and 16 the controller must avoid overshoot. In tests 17, 18, and 19 the controller must respond quickly to avoid SG level undershoot.

4.3.5.5 Test 18: Flow rate change by 20%, reactor step 15%

The purpose of this test is to examine the response of the tuned controller to load changes. The steam flow rate is increased by 20% and the reactor output power is increased by 15% using a step change.

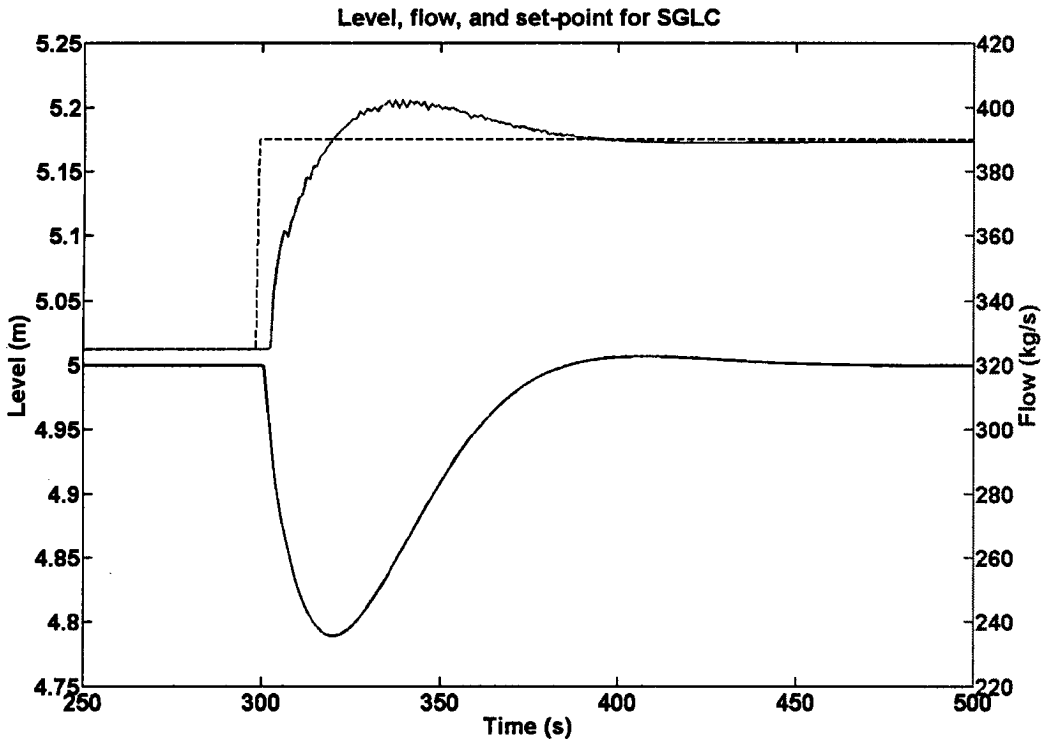


Figure 4.63: Flow rate change by 20%, reactor step 15%

The time to stabilize the level is 173 s, with an overshoot of 0.12% (5.006 m), and an undershoot of 4.4% (4.78 m). The maximum overshoot is 60% (8 m) and the maximum undershoot is 100% (0 m). The DCS control loop successfully prevents the water level from exposing the boiler tubing.

4.3.5.6 Test 19: Flow rate change by 30%, reactor step 15%

The purpose of this test is to examine the response of the tuned controller to load changes. The steam flow rate is increased by 30% and the reactor output power is increased by 15% using a step change.

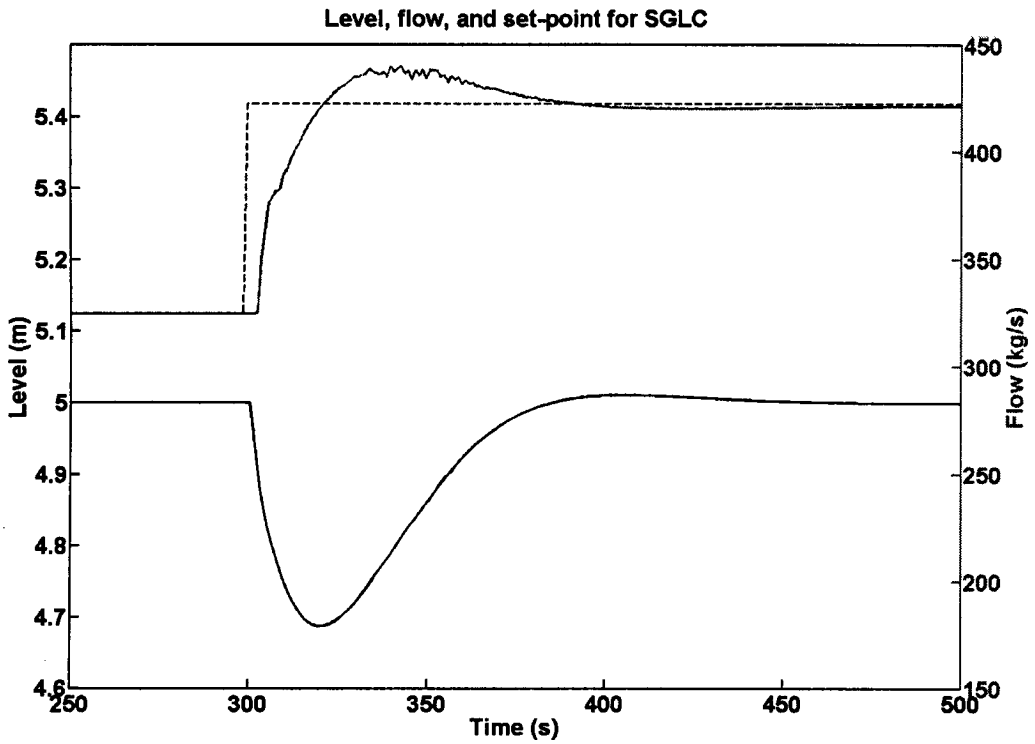


Figure 4.64: Flow rate change by 30%, reactor step 15%

The time to stabilize is 162 s, with an overshoot of 0.2% (5.01 m), and an undershoot of 6.4% (4.68 m). The maximum overshoot is 60% (8 m) and the maximum undershoot is 100% (0 m). The DCS control loop successfully prevents the water level from exposing the boiler tubing.

The DCS PID control loop successfully controls the steam generator level in all 6 of the SGLC tests.

5 CONCLUSIONS AND FUTURE WORK

This thesis has developed a test-bench and a framework for evaluating DCSs for use in industrial control, with specific applications to NPPs. A DeltaV M3 DCS from Emerson Process Management, a leading DCS manufacturer, has been evaluated. The tests have produced performance results which may be used to recommend a DCS for the control of a particular process.

5.1 Results

This research provides a test-bench and framework on which DCSs can be evaluated against the industrial control requirements. The test-bench framework successfully measured the following DCS properties:

- I/O throughput and latency for analog, digital, serial and OPC over Ethernet;
- PID control percent overshoot and settling time.

5.2 Summary

The framework measures the throughput for four different I/O channels. The measurements include standard deviation, maximum value, and minimum value. Table 5.1 presents the complete summary of throughput for each of the I/O interfaces.

Table 5.1: DCS I/O Throughput

#, Experiment	*Parameter*	*Value*	*Standard Deviation*	*Max*	*Min*
1, Digital x1	Throughput	5.05 Hz	0.03 Hz	5.43 Hz	4.69 Hz
2, Digital x8	Throughput	5.01 Hz	0.15 Hz	5.40 Hz	4.59 Hz

#, Experiment	*Parameter*	*Value*	*Standard Deviation*	*Max*	*Min*
5, Analog x1	Throughput	5.05 Hz	0.34 Hz	6.10 Hz	4.32 Hz
6, Analog x8	Throughput	5.00 Hz	0.42 Hz	6.49 Hz	4.12 Hz
9, Modbus x1	Throughput	5.05 Hz	0.21 Hz	5.64 Hz	4.42 Hz
10, Modbus x8	Throughput	4.95 Hz	0.22 Hz	5.60 Hz	4.43 Hz
10, Modbus x100	Throughput	4.95 Hz	0.22 Hz	5.60 Hz	4.43 Hz
13, Ethernet x1	Throughput	1.06 Hz	0.01 Hz	1.07 Hz	1.05 Hz

The I/O throughput is normalized to simplify comparisons against future DCS tests. The values are normalized using each channel's bit width. Throughput is normalized using the following bit-widths:

1. Analog outputs are 12-bit values.
2. Digital outputs are 1-bit values.
3. Modbus values are IEEE754 32-bit single precision values.
4. Ethernet values are IEEE754 64-bit double precision values.

Table 5.2 is a list of the I/O channels with normalized output in bits per second (bps). Normalized output rates allow these channels to be compared against other DCS under test. If a future DCS tested with the test-bench uses 16-bit analog values, the difference will appear as higher throughput in bps. The values in Table 5.2 are calculated by multiplying the bit width of the I/O channel by the throughput frequency.

Table 5.2: Normalized DCS throughput

#, Experiment	*Throughput (bps)*	*Standard Deviation (bps)*
1, Digital x1	5.05	0.03
2, Digital x8	5.01	0.15

#, Experiment	*Throughput (bps)*	*Standard Deviation (bps)*
5, Analog x1	121.2	8.04
6, Analog x8	120.0	10.08
9, Modbus x1	161.6	6.72
10, Modbus x8	158.4	7.04
10, Modbus x100	158.4	7.04
13, Ethernet x1	67.84	0.64

The framework measures the latency for four different I/O channels. Table 5.3 presents the complete summary of latency for each of the I/O interfaces.

Table 5.3: DCS I/O Latency

#, Experiment	*Parameter*	*Value*	*Standard Deviation*	*Max*	*Min*
3, Digital x1	Latency	0.072 s	0.029 s	0.136 s	0.019 s
4, Digital x8	Latency	0.072 s	0.029 s	0.136 s	0.019 s
7, Analog x1	Latency	0.310 s	0.017 s	0.339 s	0.270 s
8, Analog x8	Latency	0.229 s	0.009 s	0.242 s	0.215 s
11, Modbus x1	Latency	0.072 s	0.029 s	0.130 s	0.020 s
12, Modbus x8	Latency	0.079 s	0.029 s	0.130 s	0.020 s

The I/O interfaces can be sorted using the performance indexes measured by the test-bench. The I/O interfaces in order of decreasing throughput:

Modbus, analog, Ethernet, and digital.

The I/O interfaces in order of increasing throughput jitter:

Ethernet, digital, Modbus, and analog.

The I/O interfaces in order of increasing latency:

digital, Modbus, and analog.

The I/O interfaces in order of increasing latency jitter:

Modbus, analog, and digital.

Lastly the framework measures the behaviour of the DCS PID control of a simulated steam generator level. The framework measures steady state time, overshoot and undershoot. The steady state time, overshoot and undershoot for tests 14-17 are shown in Table 5.4: Process control performance.

Table 5.4: Process control performance

#, Experiment	*1% Steady State (s)*	*Overshoot (%)*	*Undershoot (%)*
14, Level 10% change	323	1.60	0.00
15, Level 20% change	324	3.00	0.00
16, Level 30% change	326	4.20	0.00
17, Flow 10% change, power 10% change	172	0.06	2.20
18, Flow 20% change, power 15% change	173	0.12	4.40
19, Flow 30% change, power 15% change	162	0.20	6.40

The DCS successfully controlled the steam generator level under two distinct scenarios: water level set-point change and load change. The time taken for the controller to respond to changes in load is much smaller than the time taken to respond to changes in level set-point. A level set-point change requires a loss or gain of a volume of water that is much larger than the simple rebalancing of feedwater flow to match the load change. Therefore, a level set-point change takes more time to reach steady-state than a load change.

The test-bench and framework successfully measures DCS I/O throughput and latency, and PID process control behavior.

5.3 Conclusions

A test-bench and a framework are designed and constructed to evaluate DCSs against NPP requirements. The test-bench is used to evaluate the Emerson Process Management DeltaV M3 DCS. The test-bench is used to measure DCS I/O and PID control performance. The test-bench measures the throughput, latency, and jitter of four DCS I/O interfaces. The DCS PID performance is measured under NPP SGLC. Nineteen tests are carried out to demonstrate the functions of the test-bench and framework.

The test-bench is used to measure the throughput, latency, and jitter of up to 8 digital I/O channels. The digital I/O throughput for 8 channels is 1% lower than that for one channel, but the latency remains constant. The decrease in throughput may be due to the increased processing required for 8 channels. The digital I/O latency is the lowest for all measured I/O channels. The test-bench is used to measure the throughput, latency, and jitter of up to 8 analog I/O channels. The analog I/O throughput for 8 channels is 1% lower than that for one channel, but the latency decreases. The decrease in performance from one to 8 analog channels is similar to that seen from one to 8 digital channels. This reinforces the conclusion that increasing the number of channels decreases the throughput.

The test-bench is used to measure the throughput, latency, and jitter of up to 100 Modbus serial I/O values. The Modbus serial I/O throughput for 100 values is 2% lower than that for one channel, but the latency remains constant. The Modbus serial I/O throughput is the highest for all measured I/O channels.

The test-bench is used to measure the throughput and jitter of one OPC Ethernet I/O channel. The throughput of the OPC Ethernet I/O is five times lower than all the other I/O channels. Detailed examination of the Emerson Process Management OPC server documentation revealed that this OPC server has a minimum update period of 1000 ms, resulting in a maximum throughput of 1 Hz.

The throughput values in Table 5.1 for all I/O channels have a mean value no greater than 5.05 Hz. Detailed examination of the product documentation revealed that the Emerson Process DeltaV M3 has a minimum CPU update period of 100 ms, resulting in a maximum theoretical throughput of 5.00 Hz across all I/O interfaces updated by the CPU. The product literature does not identify if the CPU update period is a soft or hard limit. The test-bench tests reveal that the throughput may be lower or higher than 5.00 Hz; therefore the CPU update period of 100 ms is likely a soft limit. The DeltaV M3 cannot sample process dynamics faster than 2.5 Hz.

The DCS is used to control the NPP steam generator water level in two control scenarios: level set-point change and load change. The test-bench framework interfaces the Matlab steam generator simulation to the DCS control, and measures the behaviour of the process variables. The DCS control tests demonstrates the use of the framework's TCP/IP simulation interface. The network enabled interface allows simulation to take place on remote computers. Remote simulation gives the test-bench the flexibility required to incorporate other simulation software into the framework.

5.4 Future work

The current work contained an evaluation of 4 I/O interfaces. Additional I/O interfaces should be considered for evaluation. Profibus, Profinet, Foundation Fieldbus H1 and Foundation Fieldbus HSE are candidates for future testing. All four fieldbuses are part of the IEC 61158 international fieldbus standard. Foundation Fieldbus H1 interface modules are available from National Instruments and can directly integrated into the test-bench

with the existing National Instruments software. Profibus, Profinet or Foundation Fieldbus HSE modules are not available for National Instruments. These three buses could be connected to the test-bench using a protocol gateway from the fieldbus to Ethernet.

Only PID control is evaluated in this work. Additional control algorithms should be evaluated. Model predictive control (MPC) and fuzzy control are candidates for future testing.

One DCS is evaluated in this work. Additional DCS should be evaluated and compared against NPP process requirements. The Yokogawa CS3000 and ABB 800xA are full featured DCSs that may be capable of meeting NPP design requirements.

Additional performance criteria should be considered. A "utilization" index could describe a ratio of controller processor utilization to I/O throughput during testing. The more a controller is utilized during a test the less idle time it has to perform emergency tasks or handle multiple loops.

The evaluation of new technology for use in nuclear power plants will always be an ongoing project.

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7 APPENDIX

7.1 NI 651x Specification

NI 651*x* Specifications

This document lists the specifications for NI 651*x* devices. These specifications are typical at 25 °C, unless otherwise noted.

Power Requirements

Power consumption on
+5 VDC (±5%)..... 150 mA, *maximum*

Power consumption on
+3.3 VDC (±5%)..... 300 mA, typical;
500 mA, maximum

(NI 6512/6513/6514/6515 only)
Power available at I/O connector.... +3.75 to +5.25 VDC

Note The power at the I/O connector is derived from the output Vcc (user-provided). If Vcc is greater than 10 VDC, then the output voltage is 5 VDC (±5%).

Digital I/O

Channel distribution and I/O connector. All channels are optically isolated.

Device	Inputs	Outputs	Connector Type
NI 6510*	32 source/sink	0	37-pin male D-SUB
NI 6511†	64 source/sink	0	100-pin keyed female SCSI
NI 6512†	0	64 source	100-pin keyed female SCSI
NI 6513†	0	64 sink	100-pin keyed female SCSI
NI 6514†	32 source/sink	32 source	100-pin keyed female SCSI
NI 6515†	32 source/sink	32 sink	100-pin keyed female SCSI
NI 6516*	0	32 source	37-pin male D-SUB
NI 6517*	0	32 sink	37-pin male D-SUB
NI 6518*	16 source/sink	16 source	37-pin male D-SUB
NI 6519*	16 source/sink	16 sink	37-pin male D-SUB

* All channels belong to one isolated bank and use the same common.

† 8 lines per bank. All lines in the same bank use the same common.

Data transfers..... Interrupts, programmed I/O

Isolated Inputs

Maximum input voltage ..... 30 VDC

Level	Min	Max
Input logic low voltage (V_{IL})	0 VDC	±4 VDC
Input logic high voltage (V_{IH})	±11 VDC	±30 VDC

Input current
11 V inputs..... 4.5 mA/line, maximum
30 V inputs..... 12.5 mA/line, maximum

Propagation delay..... 30 µs, typical

Isolated Outputs

Power-on state..... 0 (open), default; *user-programmable* to 0 or 1

Maximum switching voltage..... 30 VDC

NATIONAL INSTRUMENTS

The following table lists the derated current values for the PXI-6512, PXI-6513, PXI-6514, and PXI-6515 devices at a 100% duty cycle.

Ambient Temperature	PXI-6512/6514, All Lines	PXI-6512/6514, One Line per Port	PXI-6513/6515, All Lines	PXI-6513/6515, One Line per Port
Up to 25 °C	75 mA	350 mA	125 mA	500 mA
Up to 35 °C	75 mA	350 mA	125 mA	500 mA
Up to 45 °C*	75 mA	350 mA	120 mA	500 mA
Up to 55 °C†	75 mA	350 mA	100 mA	500 mA

* **(PXI-6512/6513 only)** For PXI-1000B and PXI-101*x* chassis, the ambient temperature for the current rating is 40 °C.

† **(PXI-6512/6513 only)** For PXI-1000B and PXI-101*x* chassis, the ambient temperature for the current rating is 50 °C.

The following table lists the derated current values for the PCI-6512, PCI-6513, PCI-6514, PCI-6515, PCI-6516, PCI-6517, PCI-6518, and PCI-6519 devices at a 100% duty cycle.

Ambient Temperature	PCI-6512/6514/ 6516/6518, All Lines	PCI-6512/6514/ 6516/6518, One Line per Port	PCI-6513/6515/ 6517/6519, All Lines	PCI-6513/6515/ 6517/6519, One Line per Port
Up to 25 °C	75 mA	350 mA	125 mA	475 mA
Up to 35 °C	65 mA	350 mA	125 mA	425 mA
Up to 45 °C	55 mA	350 mA	115 mA	375 mA
Up to 55 °C	50 mA	300 mA	100 mA	325 mA

Propagation delay ..... 80 µs, typical, 100 µs, maximum

Programmable power-up states response time ..... 400 ms

Physical Characteristics

PCI dimensions

NI 6510/6511 ..... 15.1 cm × 12.1 cm (5.94 in. × 4.75 in.)

NI 6512/6513/6514/6515/6516/6517/6518/6519 ..... 14.1 cm × 11.4 cm (5.54 in. × 4.47 in.)

PXI dimensions

NI 6511/6512/6513 ..... 21 cm × 13 cm (8.38 in. × 5.12 in.)

NI 6514/6515 ..... 16 cm × 10 cm (6.3 in. × 3.9 in.)

PCI weight

NI 6510/6511 ..... 87.9 g (3.1 oz)

NI 6512/6513/6514/6515 6516/6517/6518/6519 ..... 70.9 g (2.5 oz)

PXI weight

NI 6511/6512/6513 ..... 136 g (4.8 oz)

NI 6514/6515 ..... 172.9 g (6.1 oz)

Environmental

NI 651*x* devices are intended for indoor use only.

Operating Environment

Ambient temperature range ..... 0 to 55 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2)

Relative humidity range ..... 10% to 90%, noncondensing (tested in accordance with IEC-60068-2-56)

Altitude ..... 2,000 m (at 25 °C ambient temperature)

Storage Environment

Ambient temperature range ..... –20 to 70 °C (tested in accordance with IEC-60068-2-1 and IEC-60068-2-2)

Relative humidity range..... 5% to 95%, noncondensing (tested in accordance with IEC-60068-2-56)

Shock and Vibration (PXI-6511/6512/6513/6514/6515 Only)

Operational shock ..... 30 g peak, half-sine, 11 ms pulse (tested in accordance with IEC-60068-2-27; test profile developed in accordance with MIL-PRF-28800F)

Random vibration

Operating..... 5 to 500 Hz, 0.3 grms

Nonoperating..... 5 to 500 Hz, 2.4 grms

Random vibration is tested in accordance with IEC-60068-2-64. The nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

This device is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This device is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit `ni.com/environment/weee.htm`.

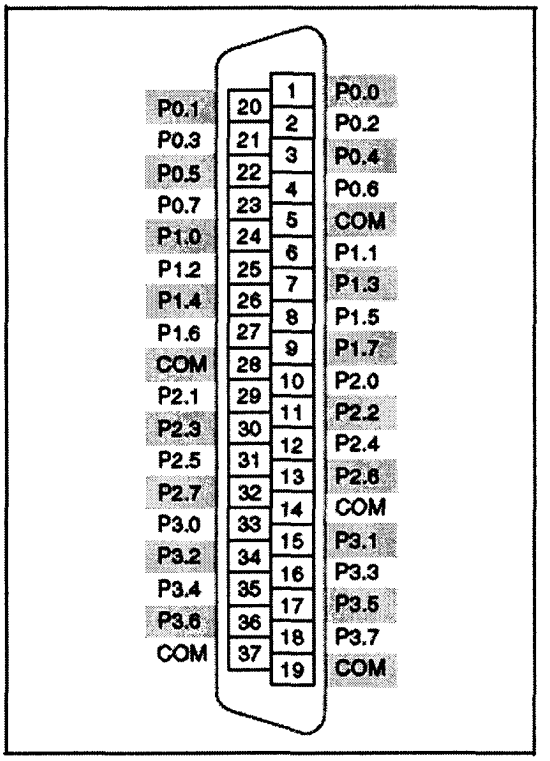

Figure 1. NI 6510 Pin Assignments

A

Specifications

This appendix lists specifications for the NI 6703/6704. These specifications are valid for an ambient temperature of 0 to 55 °C, unless otherwise noted.

Analog Output

Number of voltage channels 16

Number of current channels on the NI 6704..... 16

Resolution 16-bit

Recommended warm-up time ..... 15 minutes

Transfer Characteristics

INL..... ±1 LSB max

DNL ..... ±1 LSB max

Monotonicity..... 16 bits, guaranteed

Voltage Output

Range ..... ±10.1 V

Output coupling..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±10 mA max

Load capacitance..... 10,000 pF max

Protection ..... Short-circuit to ground

Absolute accuracy ..... ±1 mV max

Noise ..... 100 µV rms, DC to 1 MHz

Power-on state ..... Independent, user-defined values

Current Output (NI 6704 Only)

Range ..... 0.1 to 20.2 mA

Type ..... Source, does not require external excitation source

Output impedance ..... 1 GΩ min

Output compliance ..... 0 to 10 V, not clamped

Absolute accuracy ..... ±2 µA max

Noise ..... 1 μA_{rms}, DC to 1 MHz

Protection ..... Short-circuit and open circuit

Power-up state ..... Independent, user-defined values

Dynamic Characteristics

Settling time (including channel latency)

Accuracy	Time
±0.1%	1.8 ms typ, 5.6 ms max
±0.01%	3.6 ms typ, 11.2 ms max
±0.001%	14.4 ms typ, 48.8 ms max

Stability

Offset temperature coefficient

Voltage ..... 5 µV/ °C

Current (NI 6704 only) ..... 10 nA/ °C

Gain temperature coefficient

Voltage ..... 1 ppm/ °C

Current (NI 6704 only) ..... 2 ppm/ °C

Physical

Dimensions (not including connectors)

NI PCI-6703/6704 ..... 9.9 × 17.5 cm (3.9 × 6.9 in.)

NI PXI-6703/6704 ..... 10 × 16 cm (3.9 × 6.3 in.)

I/O connector ..... 68-pin male

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth ..... 11 V, Installation Category I

Environmental

Operating temperature ..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Humidity ..... 5 to 90% RH, noncondensing

Maximum altitude ..... 2,000 m

Pollution Degree (indoor use only) 2

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Immunity	EN 61326:1997 + A2:2001, Table 1
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety)	73/23/EEC
Electromagnetic Compatibility Directive (EMC)	89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

7.3 NI PCI RS232/16 Specifications

Model	Power Requirements (from PCI, PXI, PCMCIA, or ISA Channel) +5 VDC Typical Current (mA)	+5 VDC Maximum Current (mA)	+12 VDC Typical Current (mA)	+12 VDC Maximum Current (mA)	Signal Compatibility I/O Connectors	Optical Isolation	All Signals	Only RXD, TXD, GND, RTS, and CTS	Data Line ESD Protection (HBM) (kV)	Max Transfer Rate (kb/s)	FIFO Size (B)	DB-9 Adapter(s) Included	Part Number
High-Performance Plug-In													
PCI													
PCI-8430/2 (RS232)	325	500	–	–	DB-9 male	–	✓	–	15	1000	128	–	779878-01
PCI-8420/4 (RS232)	400	600	–	–	18-position jack	–	✓	–	15	1000	128	–	779879-01
PCI-8420/8 (RS232)	600	900	–	–	SCSI 68-pin interface	–	✓	–	15	1000	128	–	779147-01
PCI-8431/2 (RS485)	500	750	–	–	DB-9 male	–	–	✓	15	2000	128	–	779880-01
PCI-8421/4 (RS485)	725	1100	–	–	18-position jack	–	–	✓	15	2000	128	–	779881-01
PCI-8421/8 (RS485)	1300	1900	–	–	SCSI 68-pin interface	–	–	✓	15	2000	128	–	779148-01
PXI													
PXI-8430/2 (RS232)	325	500	–	–	DB-9 male	–	✓	–	15	1000	128	–	779882-01
PXI-8420/4 (RS232)	400	600	–	–	18-position jack	–	✓	–	15	1000	128	–	779883-01
PXI-8431/2 (RS485)	500	750	–	–	DB-9 male	–	–	✓	15	2000	128	–	779884-01
PXI-8421/4 (RS485)	725	1100	–	–	18-position jack	–	–	✓	15	2000	128	–	779885-01
PCI													
PCI-232/2	50	100	20	200	DB-9 male	–	✓	–	15	115.2	64	–	777642-02
PCI-232/4	70	150	40	400	18-position jack	–	✓	–	15	115.2	64	–	777642-04
PCI-232/8	100	150	80	800	SCSI 68-pin interface	–	✓	–	15	115.2	64	✓	777642-08
PCI-232/16	500	1000	–	–	SCSI 100-pin female	–	Ports 1 to 8	Ports 9 to 16	15	115.2	64	✓	777642-16
PCI-232i/2	400	650	–	–	DB-9 male	✓	–	✓	15	115.2	64	–	777654-02
PCI-232i/4	500	750	–	–	18-position jack	✓	–	✓	15	115.2	64	✓	777654-04
PCI-485/2	250	750	–	–	DB-9 male	–	–	✓	2	460.8	64	–	777641-02
PCI-485/4	700	1100	–	–	18-position jack	–	–	✓	2	460.8	64	–	777641-04
PCI-485/8	1100	2000	–	–	SCSI 68-pin interface	–	–	✓	2	460.8	64	✓	777641-08
PCI-485i/2	600	1300	–	–	DB-9 male	✓	–	✓	15	460.8	64	–	777653-02
PCI-485i/4	1000	1500	–	–	18-position jack	✓	–	✓	15	460.8	64	✓	777653-04
PXI													
PXI-8420/2	100	150	20	200	DB-9 male	–	✓	–	15	115.2	64	–	777720-02
PXI-8420/4	125	200	40	400	18-position jack	–	✓	–	15	115.2	64	–	777720-04
PXI-8420/8	150	250	80	800	SCSI 68-pin male	–	✓	–	15	115.2	64	✓	777713-08
PXI-8420/16	500	1000	–	–	SCSI 100-pin female	–	Ports 1 to 8	Ports 9 to 16	15	115.2	64	✓	777722-16
PXI-8421/2	350	700	–	–	DB-9 male	–	–	✓	2	460.8	64	–	777725-02
PXI-8421/4	700	1300	–	–	18-position jack	–	–	✓	2	460.8	64	–	777725-04
PXI-8421/8	1100	2000	–	–	SCSI 68-pin female	–	–	✓	2	460.8	64	✓	777725-08
PXI-8422/2	400	650	–	–	DB-9 male	✓	–	✓	15	115.2	64	–	777726-02
PXI-8422/4	500	750	–	–	18-position jack	✓	–	✓	15	115.2	64	–	777726-04
PXI-8423/2	600	1300	–	–	DB-9 male	✓	–	✓	15	460.8	64	–	777727-02
PXI-8422/4	1000	1500	–	–	18-position jack	✓	–	✓	15	460.8	64	–	777727-04
PCMCIA													
PCMCIA-232	40	150	–	–	DB-9 male	–	✓	–	2	921.6	16	✓	777278-01
PCMCIA-232/2	60	250	–	–	DB-9 male	–	✓	–	2	921.6	16	✓	777278-02
PCMCIA-232/4	80	200	–	–	DB-9 male	–	✓	–	15	115.2	64	✓	777278-04
PCMCIA-485	110	225	–	–	DB-9 male	–	–	✓	2	921.6	16	✓	777278-01
PCMCIA-485/2	150	400	–	–	DB-9 male	–	–	✓	2	921.6	16	✓	777278-02
ISA													
AT-232/2	250	340	–	–	DB-9 male	–	✓	–	2	115.2	16	–	777312-02
AT-232/4	340	450	–	–	18-position jack	–	✓	–	2	115.2	16	–	777312-04
AT-232V2	150	200	–	–	DB-9 male	✓	–	✓	15	115.2	16	–	777309-02
AT-232V4	200	320	–	–	18-position jack	✓	–	✓	15	115.2	16	✓	777309-04
AT-485/2	300	510	–	–	DB-9 male	–	–	✓	2	115.2	16	–	777311-02
AT-485/4	500	700	–	–	18-position jack	–	–	✓	2	115.2	16	–	777311-04
AT-485V2	220	260	–	–	DB-9 male	✓	–	✓	15	115.2	16	–	777901-02
AT-485V4	300	360	–	–	18-position jack	✓	–	✓	15	115.2	16	✓	777901-04

Model	Power Requirements (from PCI, PXI, PCMCIA, or ISA Channel) +5 VDC Typical Current (mA)	+5 VDC Maximum Current (mA)	+8 to +30 VDC Typical Current (mA)	+8 to +30 VDC Maximum Current (mA)	Signal Compatibility I/O Connectors	Optical Isolation	All Signals	Only RXD, TXD, GND, RTS, and CTS	Data Line ESD Protection (HBM) (kV)	Max Transfer Rate (kb/s)	FIFO Size (B)	DB-9 Adapter(s) Included	Part Number
External													
USB													
USB-232	100	500	–	–	DB-9 male	–	–	–	15	230.4	128	–	779472-01
USB-232/2	200	500	–	–	DB-9 male	–	–	–	15	230.4	128	–	779473-02
USB-232/4	200	500	–	–	DB-9 male	–	–	–	15	230.4	128	–	779473-04
USB-485	175	500	–	–	DB-9 male	–	–	–	15	460.8	128	–	779475-01
USB-485/2	300	500	–	–	DB-9 male	–	–	–	15	460.8	128	–	779476-02
USB-485/4	–	–	225	500	DB-9 male	–	–	–	15	460.8	128	–	779476-04
Ethernet													
ENET-232/2	–	–	600	1000	DB-9 male	–	–	–	15	230.4	128	–	779804-02
ENET-232/4	–	–	600	1000	DB-9 male	–	–	–	15	230.4	128	–	779804-04
ENET-485/2	–	–	600	1000	DB-9 male	–	–	–	15	460.8	128	–	779805-02
ENET-485/4	–	–	600	1000	DB-9 male	–	–	–	15	460.8	128	–	779805-04