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Flip Flops Design in Quantum Dot Cellular Automata Technology: Towards Digitization

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Abstract—Quantum-Dot Cellular Automata (QCA) is a transistor-less technology. In QCA, Columbic repulsion between electrons in the quantum dots makes data transfer possible. This paper presents the design of flip flops using a proposed Rotated-Normal Cells with Displacement (RND) inverter and a cell interaction method. The SR latch, SR Flip Flop (FF), D FF, and T FF are developed using QCA. The proposed D FF gives total and average energy dissipation of 1.31e-002eV and 1.19e-003eV respectively. It also gives a delay of 1 clock phase. The Proposed T FF provides total and average energy dissipation of 2.40e-002eV and 2.18e-003eV respectively, depicting efficient D FF and T FF in energy dissipation. The proposed SR Flip flop design gives an efficient area. The FFs with the proposed RND inverter and cell interaction method can be the best choice for future Nano communication to construct Nano circuits with less energy dissipation and high speed.

Keywords-Quantum-Dot Cellular Automata (QCA), Nanotechnology, Flip Flops (FF), Complementary Metal Oxide Semiconductor (CMOS), Rotated- Normal Cells with Displacement (RND) inverter.

I. INTRODUCTION

Manufacturing integrated circuits have evolved a lot with CMOS technology. But in CMOS technology, physical limits like leakage current, short channel effect, the material used and power dissipation are faced due to further scaling down of the transistors. QCA is the best technology among all the alternatives to overcome these CMOS technology problems [1]. QCA technology operates at a high frequency in the range of THz. It is a transistor-less technology. It has less device density, less power consumption, less delay and operates based on columbic repulsion between electrons. In QCA, routing information and computation is at the Nanoscale-[2]. The efficient flip-flops designed have applications in designing memory architectures for optimized results [3-4].

The QCA layout and its simulation result are possible through the QCA Designer tool. QCADesinger 2.0.3 uses three engines; a digital simulation engine, a nonlinear approximation engine and two-state simulation engines. Two-state simulation engine provides more accurate simulations compared to the other. The two-stage system uses the Hamiltonian shown in (1). The stationary states of the cells in the environment described by this Hamiltonian use the Schrodinger equation to get solved.

$$H_i = \sum_j \begin{bmatrix} -\frac{1}{2} P_j E_{i,j}^k & -\gamma_i \\ -\gamma_i & -\frac{1}{2} P_j E_{i,j}^k \end{bmatrix} \tag{1}$$

Here, $E_{i,j}^k$ is the kink energy between cell i and cell j. P_j is the polarization of the cell. γ_i is the tunneling energy of electrons within the cell. The overall sum is for all cells with the effective radius of the cells. Use the Jacobi algorithm to find the Hamiltonian's Eigenvalues and Eigenvector in QCADesigner.

This paper is structured as follows. Section two gives related work in the QCA flip-flop. Section three shows the proposed RND inverter gate in QCA with layout and simulation. The proposed design and simulations of the flip flop are in Section four. Finally, section five concludes the work.

II. RELATED WORK

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processor, please use the font closest in appearance to Times. Avoid using bit-mapped fonts if possible. True-Type 1 or Open Type fonts are preferred. Please embed symbol fonts, as well, for math, etc The Authors in [5] have proposed the optimum design of sequential circuits like flip-flops and shift registers by using majority gates. They have used the cell minimization technique. The MGs have a parallel connection. Without using extra cells achieves less area.

Ratna Chakrabarty et al. [6] have demonstrated the QCA layout design of D FF, T FF and JK flip-flops using a derived expression from the SR flip-flop. The kink energy and energy dissipation calculations are required to determine the robustness of the designed flip-flops [6].

SR flip flop, JK flip flop, and T flip flops are given by Bahar et al. [7]. These designs have used multiplexer, three-input Majority gate, and XOR gate. The proposed T flip-flop archives a 35% improvement in terms of cell count. SR and JK flip-flop requires 43% and 50% less area compared to the previous best single-layer designs [7].

An efficient D FF has been designed and used further to implement 5 bit counter, Single Edge Generator (SEG), a divide by two counter, oscillators, an edge-triggered K Pulse Generator (KPG) and a Negative Pulse Generator (NPG) [8].

JK FF and T FF design with the use of basic SR FF is by Karthik R et al. [9].

Authors in [10] designed D FF and memory cells using the rotating structure of a conventional three-input majority gate. The results show that D FF designs are superior in comparison to the present designs. A proposed memory cell is 33%, 79%, and 20% more effective in terms of cell counts, area, and latency. Level-triggered, Positive, Negative and dual edge triggered D FFs are considered for discussion by them. In the level triggered D flip flop, cell count and area occupations are 52% and 60% less than the most compact existing design. Positive and negative edge-triggered D flip flops are 55% more efficient in total area and 36% faster than earlier structures. The dual edge triggered D flip flop surpasses the previous best design in total area and is fast by at least 25%.

Mojtaba Gholamnia Roshan et al. [11] have used one layer for designing D Latch, D FF with the rising edge, falling edge, and dual edge triggered D FF. The D latch proposed uses only 19 cells with a delay of 0.75 clock cycles. The proposed structures are superior to previous works. They have added Set and Reset pins in the design. Here 2:1 multiplexer with simple change is used to achieve the D latch.

This paper highlights the design of the D flip-flops with both reset and set pins. The proposed D flip-flop has three cases: sensitive to rising edge, sensitive to falling edge and sensitive to dual-edge triggering. In addition, the proposed D flip-flops have few cells, consume a smaller area, and generate less delay than previous circuits. Synchronous and non-synchronous modes for reset and set pins have been considered for discussion. The best D latch from the past paper [13] is used to implement D FF by adding a comparative circuit [12].

The level-sensitive D FF, edge-to-level triggered converter, and a robust and efficient QCA design of synchronous counter is proposed in this paper. These designs have less complexity and less power dissipation. The Authors have presented two QCA layouts for level-sensitive D FF. One of them uses a 4×4 USE grid with a square dimension of 5×5 QCA cells. It has 74 cells, an area of 0.1 µm2, and a latency of 1.5 QCA clocking cycle. The second design is more robust and uses 27 cells in an area of 0.02 µm2 and a latency of 0.5 QCA clocking cycle. The counter design of 1-bit, 3-bit, and n-bit are given. A comparison between earlier implementations of D FF and counters by Abutaleb M M [13].

The Authors in [14] have presented D latch and D FF with positive and negative edge triggers using a multiplexer and with the addition of a level-to-edge converter circuit. The Majority gate is added at the output to add a set and reset feature to it. D latch is improved by 50% in terms of area and 32% by cell count, whereas D FF cell by 26% and total area by 57%. According to the authors, the improvement in these parameters is a multiplexer circuit used.

Paramartha Dutta et al. [15] have discussed SR FF, JK FF, D FF, and T FF. SR FF uses only 18 cells. The output is available at phase 2 of the first clock. JK FF is designed with 54 cells and constructed by connecting two AND gates at S and R inputs. The feedback from Q' is with J input, and the feedback from Q is with K input. Its result is available at the '0' phase of the 2nd clock. D FF by a connection of NOT gate between S and R inputs of SR FF. It makes use of 21 cells. The output is available at Phase 2 of the first clock cycle. The joining of J and K inputs together with 58 cells forms a T FF. The final result is available at the '0' phase of the 2nd clock [15].

A scan flip flop using a 2:1 multiplexer and a D FF has been proposed. In processors for built-in self-test, scan FF is applicable. They scan the internal chip and detect faults before fabrication to reduce cost and time. The output of the 2:1 multiplexer is given as input to D FF to design a scan FF. The authors compared the total area for scan FF using QCA

and CMOS technology. According to Shanthala G M et al. [16], the researcher can design more complicated circuits using this technique.

III. PROPOSED RND INVERTER AND FLIP FLOPS

The proposed RND NOT gate aims to provide four cells with high polarization, less space, less delay, and less energy dissipation. It provides routing information and computation faster in secure Nano communication. It employs normal cells and rotated cells with a displacement of 10nm. Figure 1 depicts the QCA layout and simulation result.

The cell interaction or cell placement methodology provides the best results in terms of less number of cells and less area by the placement of cells in an effective way. Flip flops have been designed using these methods to get an efficient design in terms of the number of cells, cell area, delay, and polarization.

Figure 1: QCA Layout and simulation result of Proposed RND Gate

The simulation result shows that it gives polarization of 9.77 which is better compared to a 9.51 in standard two-cell QCA inverter. The fork-shaped inverter uses 9 cells with an area of 7198 nm^2 whereas the proposed RND gate uses 4525.55 nm^2 area. The improved parameters are indicated in Table 1.

Table 1. Comparison of proposed RND gate with Standard NOT gate

Digital Logic Gate	Number of cells			Total Area (nm^2)		
	Standard	Proposed	Improvement	Standard	Proposed	Improvement
Proposed RND inverter Gate	9	4	44%	7198	4525.55	62.8%

The proposed RND gate is robust and gives the best results as compared to all the existing gates designed and named 'Tougaw et al Inverter Model', 'Farazkish et al Inverter Model', 'Farazkish et al Inverter Model', 'Navi et al Inverter two-layer design Model', 'Navi et al Inverter Three layer design Model', 'AOI (And-Or-Inverter) Inverter Model', etc. The RND inverter is better in terms of cell count, polarization achieved and total area as shown in Table 2.

Table 2. Comparison of proposed RND gate with Existing inverters

Inverter Model	Cell Count	Total Area in nm2	Polarization achieved
Tougaw et al Inverter Model[2]	8	5684	0.775
Farazkish et al Inverter Model[18]	6	3724	0.486
FNZ Inverter Model [18]	8	6084.00	0.931
Navi et al Inverter two-layer design Model[19]	6	1764	0588
Navi et al Inverter Three layer design Model[19]	8	1764	0.842
AOI (And-Or-Inverter) Inverter Model [20]	7	12744	+0.525 and -0.629
Standard NOT gate with fork shape	9	7198	0.951
Proposed RND Inverter model	4	4525.55	0.977

A. SR Latch

SR latch design uses 26 cells, an area of 0.03 µm2, the polarization of +9.87 and -9.87 for Q output, +9.68 and -9.68 for Q bar output. It gives a delay of a complete 1-clock cycle. The QCA design layout and the simulation result are depicted in figure 2.
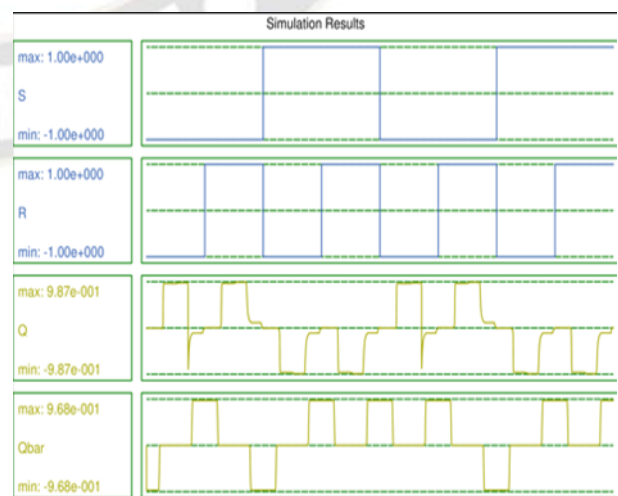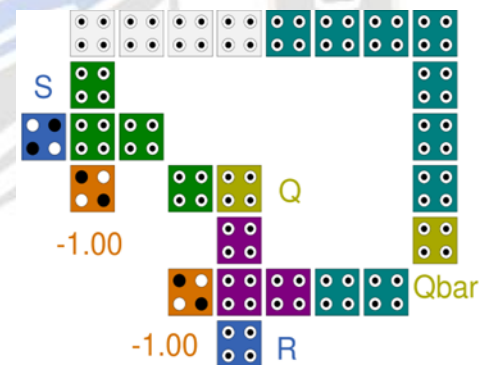

Figure 2: QCA Layout and simulation result of SR latch

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The latch gives the best polarization of +/- 9.87 as compared to the existing latch. The output has less distortion or errors compared to the existing SR latch.

B.   SR Flip Flop

The SR flip-flop design is by conversion of the D flip-flop in [12] to the SR flip-flop. This SR flip-flop design gives an output polarization of +9.89 and -9.85. It makes use of 47 cells and a total area of 0.05 µm2. The D flip flop has been applicable to convert it into SR flip flop by conversion rules. D flip flop is converted into SR flip flop by connecting ORing of S input with ANDing of Q and R'. In mathematical form, it is D = S+Q.R'. The conversion table is shown below in table 3. The K map simplification and schematic diagram are shown in figure 3a and figure 3b. The QCA layout and simulation result of SR FF is in figure 4.

Table 3 Conversion of D FF to SR FF

S	R	Q_N	Q_{N+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X
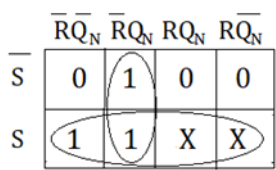
(a)
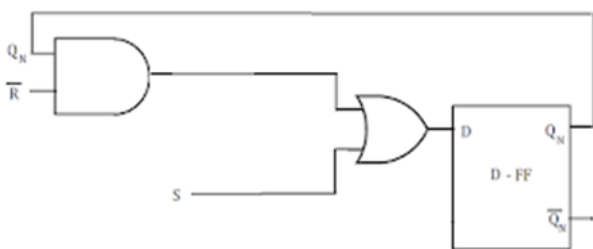
(b)

Figure 3: (a) K-Map simplification   (b) D FF to SR FF Schematic Diagram

The proposed SR FF gives an improvement in polarization and the total area of the QCA layout compared to the existing SR FF. Even though the circuit uses 47 cells compared to 40 cells in [7] it provides better area due to the cell placement methodology used here.

Figure 4: QCA Layout and simulation result of SR FF

2:1 Mux with proposed RND Inverter gate

Figure 5 shows the 2:1 multiplexer implemented using the RND gate. This is modified to get the QCA layout of the D flip flop.
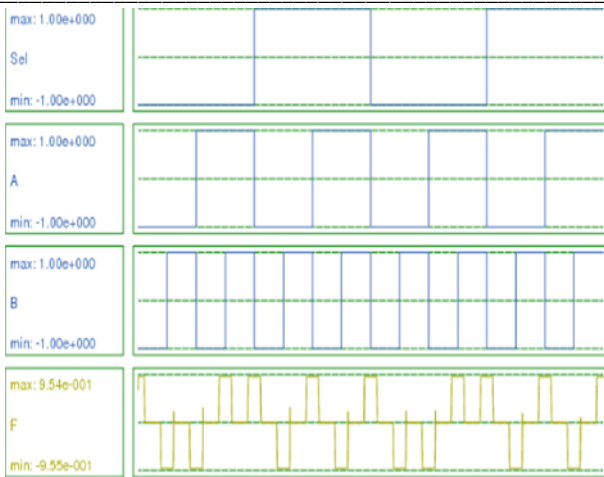
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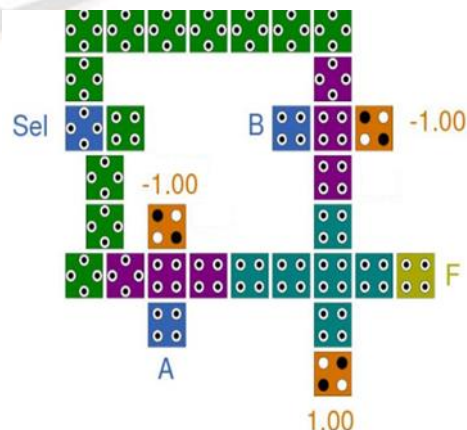
Figure 5: QCA Layout and simulation result of 2:1 Mux

C. D flip flop

The proposed D flip flop uses a 2:1 Multiplexer implemented with a proposed RND NOT gate. The output is feedback to one of the inputs of the multiplexer with delay. The QCA layout and simulation result of D FF are in Figure 6.
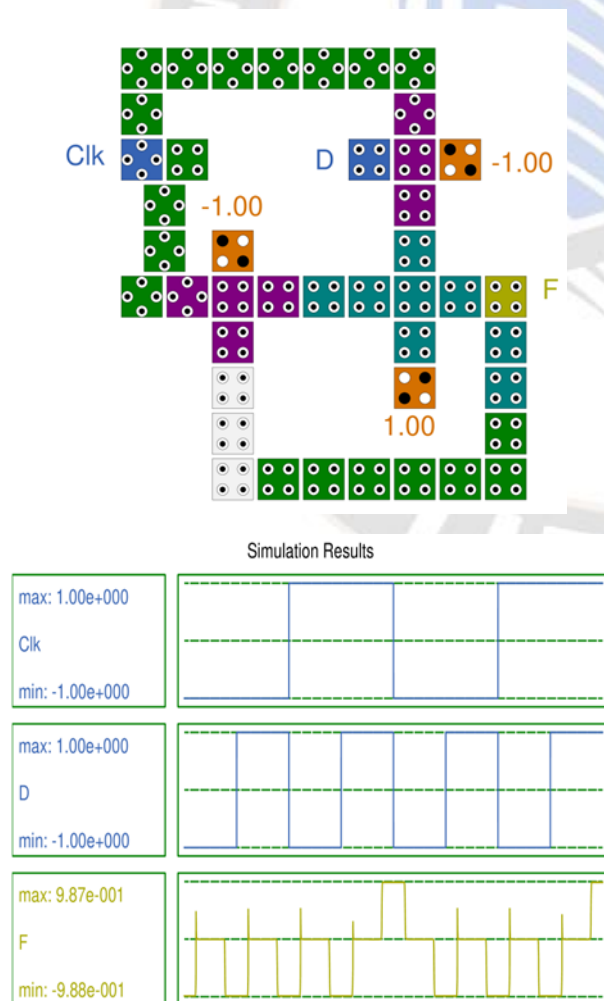
The proposed D FF dissipates less energy and has less delay. It is efficient in terms of high speed and energy dissipation even though it requires more cells and space as compared to the existing design [13].

In [13], the total energy dissipation is 1.47e-002eV and the average energy dissipation is 1.34e-003eV. The proposed design has a total energy dissipation is 1.31e-002eV and an average energy dissipation is 1.19e-003eV. It shows efficient D FF in energy dissipation. Due to the RND inverter gate and cell placement methodology, this flip flop provides a delay of 1 clock phase instead of 2 clock phases [13].

D. T Flip flop

T flip flop design uses the JK flip flop in [13] by combining J and K inputs with a single input connection named T. The output is delayed by one clock cycle and has the polarization of + 9.49, -9.49 with a total area of 0.05μm2. It makes use of 45 cells. The QCA layout and simulation result of T FF is in figure 7. T FF is efficient in terms of area and energy dissipation [7].
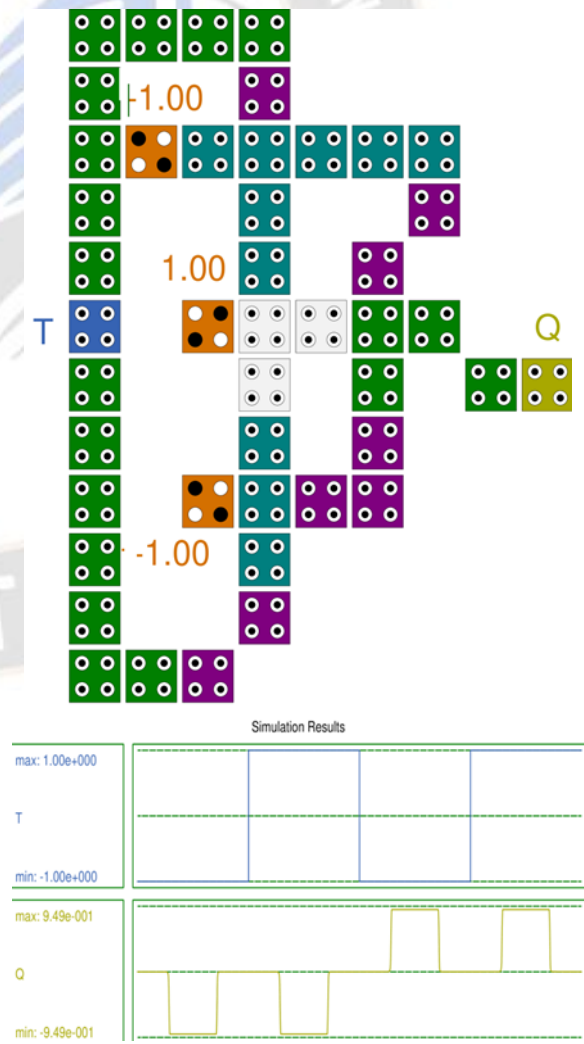

Figure 6: QCA Layout and simulation result of D FF

Figure 7: QCA Layout and simulation result of T FF

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IV. RESULTS AND DISCUSSION

QCA sequential circuits need to be given more concentration because of the complexity and difficulty in their architecture and to achieve synchronization. Flip flops are the basic building block in sequential circuits. QCA flip-flops can be designed either by line-based or loop-based design methods.

In the first method, data storage can be with three clock zones. In loop based method, the data storage is by a loop of four clock zones. The loop-based design is preferred over the line-based design as it has lower complexity [13]. The comparison of existing flip-flop designs in QCA and the proposed flip-flops is in tables 4, 5, 6 and 7.

Table 4 Comparison of SR Latch

Circuit Implemented	Number of cells	Total Area (µm²)	Polarization	Delay	Cells used	Total Energy Dissipation
SR Latch [15]	18	0.02	+9.53, -9.53 +5.07, -5.07	1 clock cycle	Normal	5.39e-003 eV, Average : 4.90e-004 eV
Proposed Latch	26	0.03	+9.87, -9.87 +9.68, -9.68	1 clock cycle	Normal	1.37e-002 eV Average : 1.25e-003 eV

Table 4 shows that the polarization is improved by a difference of 34% and the output is robust and error-free compared to the existing design in [15]. The output polarization in the existing design for Qbar is just +5.07 and -5.07 compared to +9.68 and -9.68 in the proposed SR latch.

Table 5 Comparison of SR Flip Flops

Circuit Implemented	Number of cells	Total Area (µm2)	Polarization	Delay	Cells used	Total Energy Dissipation
SR FF [7]	40	0.06	+9.52, -9.55	1 clock cycle	Normal	1.76e-002 eV, Average: 1.60e-003 eV
Proposed SR FF	47	0.05	+9.89, -9.85	1 clock cycle	Normal	2.05e-002 eV Average:1.87e-003 eV

Table 5 shows that the proposed SR flip-flop is efficient in terms of total area and polarization. Even though the number of cells required is higher than [7], due to proper cell placement the area required is improved by 10%.

The proposed D FF dissipates less energy and has less delay. It is efficient in terms of high speed and energy dissipation. The proposed design has a total energy dissipation of 1.31e-

002eV and an average energy dissipation of 1.19e-003eV. It shows efficient D FF in energy dissipation. Due to the RND inverter gate and cell placement methodology, this flip flop provides a delay of 1 clock phase instead of 2 clock phases [13].

Table 6 Comparison of D Latch and/or D Flip Flops

Circuit Implemented	Number of cells	Total Area (µm²)	Polarization	Delay	Cells used	Total Energy Dissipation
D Latch [14]	13	0.01	+9.87, -9.87	3clock phases	Normal	6.31e-003 eV, Average : 5.74e-004 eV
D Latch [15]	21	0.02	+8.89, -8.88	Phase 2 of the first clock cycle	Normal	5.44e-003 eV Average : 4.94e-004 eV
D FF [13] Level Sensitive	28	0.02	+9.88, -9.88 output not perfect	2 Clock Phases	Normal	1.47e-002 eV Average : 1.34e-003 eV
Proposed D FF	43	0.05	+9.87, -9.88	0.25	Rotated and Normal	1.31e-002 eV Average : 1.19e-003 eV

Table 7 Comparison of T Flip Flops

Circuit Implemented	Number of cells	Total Area (µm²)	Polarization	Delay	Cells used	Total Energy Dissipation
T FF[15]	58	0.06	+9.19, -9.19	output Not correct, delay of 0.75	Normal	2.62e-002 eV, Average : 2.38e-003 eV
T FF [7]	43	0.06	+9.52, -9.55	1 clock cycle	Normal	2.47e-002 eV, Average : 2.25e-003eV
Proposed T FF	45	0.05	+9.49, -9.49	1 clock cycle	Normal	2.40e-002 eV Average :2.18e-003 eV

T FF is efficient in terms of the total area and energy dissipation in [7] as shown in the tabular data.

The software tools used to design the QCA layout are QCADesigner 2.0.3 and QCADesigner – E. QCA Designer 2.0.3 is used to design the QCA layout and to observe the simulation result. QCADesigner – E gives the energy dissipation of the QCA layout design. The standard parameters used in the QCADesigner 2.0.3 tool are listed in table 8 and additional parameters used in QCADesigner – E are listed in table 9.

Table 8 Parameters used in the QCADesigner 2.0.3 tool

Parameter	Description	Standard Value
QD size	Size of a quantum dot	5nm
Cell Area	Dimensions of each cell	18nmx18nm
Cell Distance	Distance between two cells	20nm
Layer Distance	Distance between QCA Layers in case of multilayer crossing	11.5nm
r	Relaxation Time	1E-15s
γ H	Maximum Saturation energy of clock signal	9.8E-22J
γ L	Minimum Saturation energy of clock signal	3.8E-23J
ϵ^r	Relative permittivity of material for QCA	12.9*
Temp	Operating Temperature	1 K
reffect	Distance between cells considered	80nm[†]

* Relative permittivity of GaAs and AlGaAs

[†]Interaction effects between two cells decay inversely with the fifth power of its distance.

Table 9 lists the additional parameters used in the QCADesigner-E tool. This tool gives the total and average energy dissipation of the QCA layout design.

Table 9 Parameters Used in QCADESIGNER-E Tool

Parameter	Description	Standard Value
$T_γ$	Period of the clock signal	10E-12s
γslope	Rise and fall time of the clock signal slopes	1E-12s
γshape	Shape of clock signal slopes[RAMP/GAUSSIAN]	GAUSSIAN
Tin	Period of the input signals	10E-12s
Tsim	Total simulation time	80E-12s
Tstep	Time interval of each iteration step	1E-17s

V. CONCLUSION

In this work, latch and efficient flip flops are proposed with the best results and compared with the existing latch and flip flops. Different methodologies are available to implement these flip-flops. They are like using MV3, and MV5, using a multiplexer, using the XOR gate, and simplification of the characteristic equations. Every method has its advantages or disadvantages to achieving the optimized parameters. The SR latch design gives the best polarization of +-9.87 compared to the existing design methods. The output has less distortion or errors compared to the existing SR latch. The polarization achieved is improved even though the number of cells and area required is slightly more. T FF shows improvement in the area and the polarization. D FF and T FF are energy efficient. The proposed T flip flop has total energy dissipation of 2.40e-002eV and average energy dissipation of 2.18e-003eV. D FF is designed by using the proposed RND NOT gate with 2:1 multiplexer. SR flip flop is by using a technique of flip flop conversion, the D FF to SR FF conversion technique. These results show efficient flip-flop designs.

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