EXPLORING POLYMER DIELECTRICS FOR DONOR-ACCEPTOR AND SMALL MOLECULE BASED TRANSISTORS AND VOLTAGE INVERTERS

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By

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The undersigned, appointed by the Dean of the Graduate School, have examined the dissertation entitled:

Exploring Polymer Dielectrics for Donor-Acceptor and Small Molecule Based Transistors and Voltage Inverters

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This body of work is dedicated to my family. Without their continuous support and encouragement, its realization would not have been possible.

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NOMENCLATURE

BGBC – Bottom gate / bottom contact

BGTC – Bottom gate / top contact

C_i – Capacitance (per unit area) of insulator
C-F – Capacitance versus frequency

C-V – Capacitance versus voltage

CFO – Cobalt ferrite

cPVP – Crosslinked PVP *(see PVP)*

DCB – 1,2 dichlorobenzene

DMF – N,N-dimethylformamide

DMSO – Dimethyl sulfoxide

DPP-DTT – Diketopyrrolopyrrole dithienylthieno[3,2-b]thiophene

HOMO – Highest occupied molecular orbital

FET – Field effect transistor

FTIR – Fourier transform infrared

I-V – Current versus voltage

I_{DS} – Drain/source current

I_{off} – "Off" state current

I_{on} – "On" state current

IID - Isoindigo

LUMO – Lowest unoccupied molecular orbital

MIM – Metal-insulator-metal

MIS – Metal-insulator-semiconductor

MOS – Metal-oxide-semiconductor

OTS - Octadecyltrichlororsilane

PEIE - Polyethylenimine ethoxylated

PFBT – Pentafluroubenzenethiol

PGMEA - Propylene glycol monomethyl ether acetate

PMMA – Polymethyl methacrylate

PMMF – Poly(melamine-co-formaldehyde)

PVDF - Polyvinylidene fluoride

PVA - Poly(vinyl alcohol)

PVP - Poly (4-vinyl phenol)

Qx – Quinoxaline

SEM – Scanning electron microscopy

Si++ - Heavily doped silicon

SiO_2 – Silicon dioxide

SS – Subthreshold swing

T_C – Curie temperature

TEM – Transmission electron microscopy

TGA - Thermal gravimetric analysis

TGBC – Top gate / bottom contact

TGTC – Top gate / top contact

TrFE - Trifluoroethylene

Tv - Thienylenevinylene

V_{DD} – Supply voltage

V_{DS} – Drain/source voltage

V_{GS} – Gate/source voltage

V_{in} – Input voltage

V_{out} – Output voltage

V_T – Threshold voltage

Wt% - weight percent

W/L – Ratio of channel width to channel length

XRD – X-ray diffraction

ZnO – Zinc oxide

κ – dielectric constant

μ - mobility

ABSTRACT

Organic semiconductor devices have gained much attention over the past several decades. Solution processability of polymer materials lends itself towards the realization of flexible, wearable electronic devices, owing to the low energy needs and the applicability of large-scale roll-to-roll casting methods. Unlike traditional field effect transistor technologies which rely on doped semiconductors and operate in the inversion regime, organic transistor devices utilize intrinsic semiconductors and operate in the accumulation regime. For this reason, the unique physical properties of both the dielectric layer and the semiconductor layer are crucial to driving charge transport.

Hole-transporting field effect transistors were fabricated using the ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) as the dielectric along with a donor-acceptor polymer based on diketopyrrolopyrrole as the semiconductor layer. These devices yield carrier mobilities upwards of 0.4 cm^2/Vs and high on/off ratios when the ferroelectric layer is electrically poled. Furthermore, through the application of self-assembled monolayers, the device characteristics are observed to be modified by orders of magnitude for devices of the same architecture utilizing a non-ferroelectric dielectric.

Fluorination of donor–acceptor copolymers has been one strategy employed towards enhancing polymer coplanarity, increasing crystallinity, and improving charge transport mechanisms in organic devices. Towards the realization of dedicated n-type polymer semiconductors, the synthesis of thiazole flanked fluorinated isoindigo copolymers is reported and their field effect transistor properties are demonstrated. The selenophene-substituted isoindigo shows improved performance over the thiophene units. Top-gate

devices with varying dielectric layers showed n-type transport with electron carrier mobilities of the order of 10^{-2} cm^2/Vs and on/off ratio of 10^5.

Several proof-of-concept complementary voltage inverter circuits have been constructed utilizing the various dielectrics and donor-acceptor semiconductors explored prior in this work. In addition to these, ozone-treated zinc oxide and the donor-acceptor polymer quinoxaline are explored for application in constructing inverter circuits. The contribution of each device's characteristic to the overall inverter behavior is demonstrated. Furthermore, a basic inverter model is used to simulate the inverter characteristics of one such circuit using parameters from the individual device characteristics.

A viable route for enhancing the dielectric constant of polymer dielectrics is via the incorporation of semiconducting and insulating nanoparticles. Returning the focus back to the influence of the dielectric layer, improved performance of organic capacitor and transistor devices after incorporating magnetic nanoparticles into non-ferroelectric dielectrics is observed. In particular, the threshold voltage, subthreshold swing, and observable hysteresis are reduced in pentacene devices using cross-linked poly(4-vinyl phenol) polymer dielectric with incorporated cobalt ferrite nanoparticles. The application of an external magnetic field is also observed to further tune device behavior.

Chapter 1: Introduction

Development of modern technology revolves around our ability to pack electronic devices into smaller, more efficient circuits to deliver the logic-based behavior that is at the foundation of computing. Constructing such devices relies on the use of semiconductors. One of the most fundamental semiconductor devices is the transistor, which acts as a voltage-controlled "switch" for guiding current through complex circuits. The idea surrounding a field effect transistor (FET) was first patented in 1925 by Julius Edgar Lilienfeld and began to explode in research and popularity in the 1970s [1]. Its development from that point forward began to usher in the digital age, with these devices acting as a cornerstone of semiconductor and microchip technology. As the research and development of this technology has continued to grow, the devices themselves have continued to shrink. In 1975, Gordon Moore put forward an essay in which he suggested that the number of transistors that could fit into a single chip would double every two years, a concept that would later become well known throughout the computer industry as "Moore's Law." As processors and memory devices have continued to shrink and become more complex, sustaining this same rate of increase has become more difficult owing to issues stemming from heat, switching speed, and production cost [2]. Researchers today are looking for ways to move beyond Moore's Law as well as to develop new types of transistors that can fulfill the special technological needs of modern equipment, such as flexibility and mobility.

The three-terminal architecture of the FET allows for innovation through the choice of semiconductor type, contact material, insulators used, material dimensions and phase, and

differing charge-transport mechanisms. Among the most popular is the metal-oxide-semiconductor field effect transistor (MOSFET) which utilizes inorganic, elemental semiconductors. Chapter 2 will begin by exploring the fundamental physics surrounding semiconductors and MOSFET technology. From there it will expand into the use of organic semiconductor materials and how they differ in charge transport, fabrication, and operation when utilized in a FET architecture. Chapter 3 will provide insights into the methods employed for designing, fabricating, and characterizing FET devices as well as delving into the construction and characterization of complementary inverter architectures.

As will be demonstrated in Chapter 2, the physical properties associated with the dielectric layer plays a strong role in the performance of organic FET devices. Chapter 4 provides an overview of the various dielectric materials used and the influences of their physical properties on device behavior. A large part of this chapter will discuss employing a ferroelectric polymer for the dielectric layer, and the influence that external electric fields can have on tuning the charge transport in such devices.

In Chapter 5, the focus will shift from the dielectric layer towards the use of donor-acceptor semiconducting polymers and the improvement of the charge-transport capabilities of the material based on device architecture. From there, Chapter 6 will explore the creation of simple logic circuits through the combination of FET devices from the previous chapters in complement to one another. This chapter will explore the use of organic FETs paired with each other, paired with inorganic FETs, as well as paired with themselves in the case of ambipolar materials. Chapter 7 will then turn the focus back towards the dielectric, exploring how the incorporation of magnetic nanoparticles could act to influence the capacitance of the layer and how the application of external magnetic fields

could act to introduce magnetocapacitive behavior. Finally, Chapter 8 will seek to summarize and tie together the results of the previous chapters as well as outline possible directions for these studies to improve.

Chapter 2: Fundamentals of Semiconductors and Devices

This chapter aims to introduce the fundamental physical mechanisms which lead to charge transport in semiconductors as well as the construction of devices made using them - including capacitors and transistors– to contextualize the results which are reported in the later chapters of this work. For the sake of brevity, as there are entire books dedicated to these subjects, the information presented herein is not completely exhaustive.

2.1 Introduction to Semiconductors

In the study of solid state physics, many materials are considered to have polycrystalline structures on a microscopic level, even if such periodicity is not apparent from a macroscopic viewpoint. For such materials, crystal structures are defined to mathematically reflect the translational uniformity of atoms, ions, or molecules which comprise it [3]. An electron under the influence of a periodic potential - which can be produced by the atomic nuclei when arranged in a lattice structure - are defined as Bloch electrons. The wavefunction of these electrons within this periodic potential gives rise to differing energy levels the electrons can occupy [3,4]. The formation of these levels can also be understood more qualitatively as the spreading of the orbital levels of individual atoms when many are combined into a solid structure [5]. These energy levels constitute what is known as the *band structure* of the solid, with each band becoming continuous in a solid structure made up of many atoms. The most notable bands to consider are the valence band (which is the highest energy band filled with electrons) and the conduction band (which is the lowest energy band that lacks electrons). A semiconductor's Fermi level represents an energy level that sits halfway between the valence and conduction bands at

0 K [5]. The energy difference between these two bands is known as the *bandgap* of the material. The ease with which an electron can move from one band to the other (and therefor the size of the bandgap) dictates the conductivity of that material. When an electron is energetically promoted to the conduction band, it leaves behind an unoccupied state in the valence band, which is commonly referred to as a “hole.” This empty state results in the flow of charges within the valence band, ultimately acting to produce a current as if the hole were a positive charge, which is customarily how it is treated in the field of semiconductor research.

The simplest definition of a semiconductor is a material that has an energy bandgap that is larger than 0 eV (which defines metals and semimetals) and smaller than 4 eV, where greater values would merit labeling the material an insulator [3,4]. Semiconductors are solids where one can reasonably expect thermal excitation of electrons across the bandgap when the temperature is greater than 0 K but lower than the material’s melting point [3]. As this promotion of electrons across bands is thermally activated, semiconductors demonstrate an increase in conductivity with temperature, unlike metals whose conductivity drops with increasing temperature due to larger instances of scattering. There exists a multitude of materials which can be defined as semiconductors, including elemental crystals, compounds, oxides, organic molecules, and more! Each type of material comes with differing physical and chemical characteristics, charge transport properties, and methods which can be employed to grow or cast it. Among the elemental semiconductors, the process of doping will often be used to modify the material’s conductivity. Doping acts to purposefully introduce impurities into the crystal which add “extrinsic” carriers to make the material more *p-type* (hole transporting) or *n-type* (electron transporting) [5]. The

introduction of these “donor” or “acceptor” impurities (usually stemming from Group V or Group III elements, respectively) creates additional energy levels near either the conduction or valence band [5]. Such doping is not necessary for organic semiconductors, which are known as “intrinsic” semiconductors; however, as will be explored later, some polymer groups can be paired with “donor” or “acceptor” copolymers which act in a manner reminiscent to doping towards tuning charge transport.

2.2 The MOSFET

The metal-oxide-semiconductor field effect transistor (MOSFET) represents the cornerstone of transistor technology and integrated circuits for modern electronics. MOSFETs make use of inorganic semiconducting materials, the most popular of which are elemental silicon or germanium, and an oxide layer which separates the semiconductor from a metallic layer known as the “gate.” To understand the operation of a MOSFET, one must first consider how the motion of charges within the semiconducting layer varies under the influence of an external electric field.

To begin, Figure 2.1 below outlines the band diagram of a simple metal-oxide-semiconductor (MOS) capacitor device. Here, the metallic surface allows one to apply a bias which can be varied over time. The oxide layer acts to shield the semiconductor layer from the metallic contact such that there is no current flowing between them, and the only influence on the semiconductor originates from the electric field produced by the bias applied to the metal. To understand how the electric field modifies the charges at the semiconductor/oxide interface, Figure 2.1 outlines the alteration to the energy levels of the MOS device as differing biases are applied to the metal. The figure, as well as the

explanation which follows in this section, are adapted based on information provided in the sixth chapter of *Solid State Electronic Devices* by Streetman and Banerjee [5].

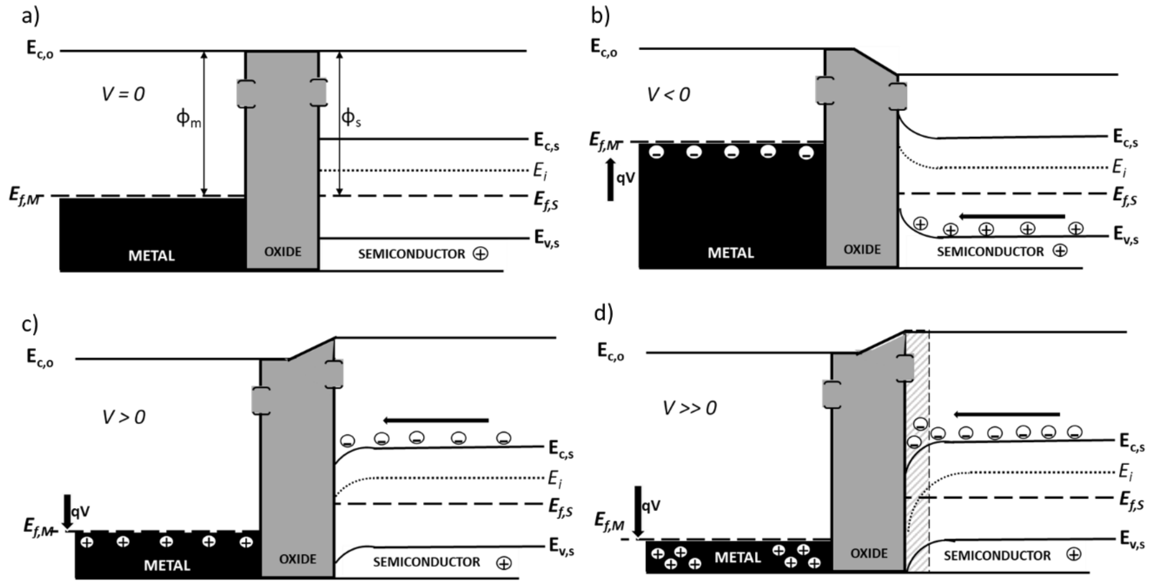

Figure 2.1. MOS band structure outlining the a) flat band state b) accumulation state c) weak inversion state and d) strong inversion state. The dashed rectangle in d) represents the inversion layer. The semiconductor is treated as doped to be p-type.

Here it is assumed that this is an ideal case, where the Fermi level of the metal ($E_{f,M}$) is perfectly aligned with the Fermi level of the semiconductor ($E_{f,S}$) when the bias applied to the metal surface is zero, as shown in Figure 2.1 a). φ_M and φ_S are the modified work functions for the metal-oxide and semiconductor-oxide interfaces, respectively, representing the amount of energy required to move an electron to the conduction band of the oxide. E_i represents the intrinsic energy level of the bulk semiconductor. The brackets along the borders of the oxide layer are meant to demonstrate that the oxide's conduction band is much greater than that of the semiconductor ($E_{C,O}$>>$E_{C,S}$). Assuming that the semiconductor is p-type, when a negative bias is applied to metal surface $E_{f,M}$ raises relative to the semiconductor, as shown in Figure 2.1 b). Because φ_M and φ_S are not changed by the applied voltage, the upward shift of $E_{f,M}$ causes the conduction band of the oxide to bend.

This in turn causes a bending of the energy bands in the semiconductor which acts to promote the accumulation of holes - which are the majority carrier for a p-type semiconductor - at the semiconductor/oxide interface as the valence band shifts towards the Fermi level. Similarly, the application of a positive bias to the metal causes a downward shift in $E_{f,M}$ and a subsequent downward bending of the semiconductor bands. The field acts to deplete the semiconductor of holes and bend the conduction band towards the Fermi level, resulting in drawing in electrons, as shown in Figure 2.1 c). As the positive bias continues to increase, the large collection of minority carriers forms what is known as an *inversion layer*. This layer, although part of the p-type semiconductor, is effectively n-type.

In a MOSFET, the inversion layer acts as the channel through which injected charges - which are first introduced from heavily-doped regions of the contacts applied onto the semiconductor - are transported across the channel length [6]. As such, MOSFETs are said to operate in the *inversion regime*. Continuing the example from the MOS architecture, for a p-type semiconductor the contacts for the semiconductors (known as the “source” and “drain’) would be heavily doped n-type areas, such that current will not normally flow in the p-type semiconductor between them. Once the inversion layer creates an n-type channel, charge injection into the semiconductor can occur and current from source to drain be facilitated. In the operation of a MOSFET, the minimum gate bias necessary to form the conducting channel is known as the threshold voltage (V_T). Before this voltage is achieved, the device acts like a resistor with the channel current increasing linearly with voltage. This part of FET operation is similarly denoted as the *linear regime*. After the threshold voltage is achieved, the current through the conducting channel becomes constant and does not increase further. This part of FET operation is denoted as the *saturation regime*. Both of

the regimes of device operation and how they relate to device performance will be explored in more depth in Chapter 3.

To understand why saturation occurs in the first place, it is important to keep track of the biases applied to the source and drain. Generally, the source contact will be held at ground while some voltage is applied to the drain contact (V_D). This bias between source and drain acts to drive the charge carriers and form the current in the channel. With this in mind, one can see in Figure 2.2 that when a bias is applied to the gate, the potential between the gate and the drain and that between the gate and the source will be different. When $|V_D|=|V_G-V_T|$, the area near the drain contact is depleted of free charge and the charge carriers move according to a space charge limited current. Here, the channel is considered to be “pinched off.” Continuing to increase the drain bias further only acts to widen the “pinched off” region between the channel and the drain, and as such the current will no longer increase with increasing V_D and will have saturated.

Although the gate bias experienced at the drain and source contacts will have some difference to each other, for the remainder of this work, the bias applied at the gate will be generally referred to as V_{GS} and V_{GD} will not be considered. Similarly, the bias between the drain and source contacts will be generally referred to as V_{DS}.

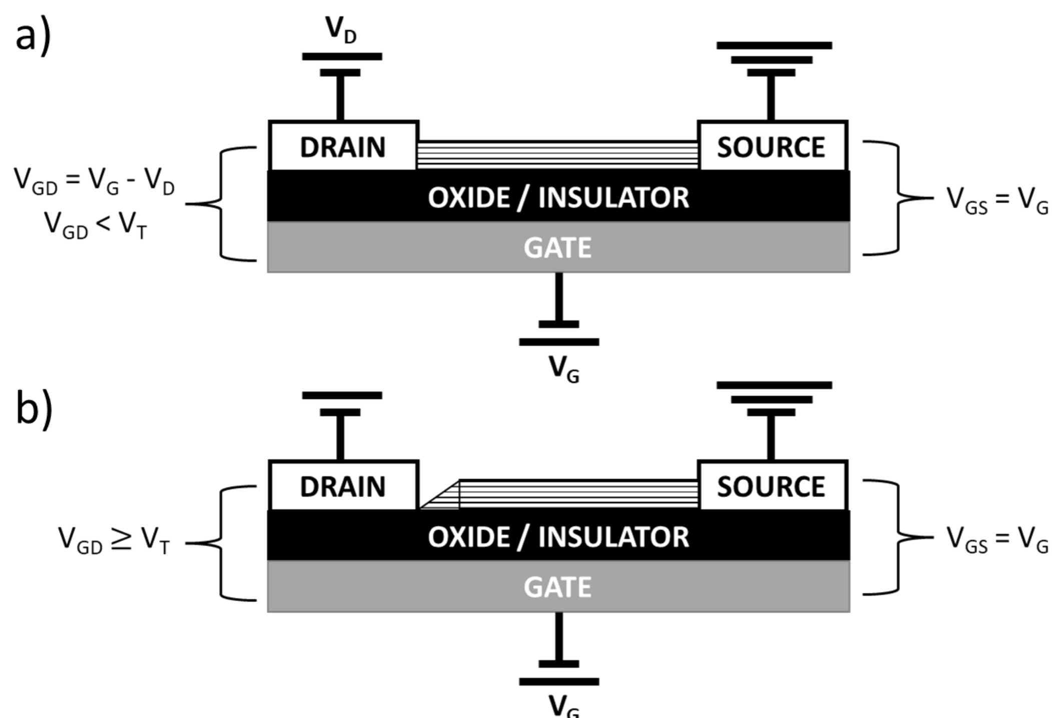

Figure 2.2. A simplified MOSFET architecture, with the dashed rectangle representing the transport channel in the semiconducting layer. In b) the channel is "pinched off."

For single-crystal silicon as the semiconductor layer, MOSFETs are reported to have charge carrier mobilities on the order of 10^2-10^3 cm^2/Vs [7,8]. The high processing temperatures and vacuum required for fabrication renders the realization of MOSFETs energy intensive. Additionally, the brittle nature of materials such as silicon or germanium make large scale fabrication and the realization of flexible technology much more difficult. To overcome some of these drawbacks, one can turn to organic semiconductor devices.

2.3 Charge Transport in Organic Semiconductors

In recent years, researchers have turned to investigating the properties of organic semiconductor materials instead of traditional elemental semiconductors. These materials, owing to their weaker van der Waals interactions, allow for easier solution processing

techniques such as spincoating, dropcasting, and inkjet printing [7-9]; however, it also results in the electron transport across the material being tightly bound to localized states [10]. For organic materials, charge transport does not occur through the band-to-band transport that is common in inorganic systems. One must consider the highest occupied molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO) of the material in a way which is synonymous to the valence and conduction bands in inorganic semiconductors.

Organic semiconductors generally come in two varieties, conjugated small molecules and conjugated polymers. The π-orbitals stemming from the hybridized bonds between carbon atoms in organic systems results in the delocalization of a valence electron from the carbon atoms, which permits charge transport across the molecule. Individual molecules or small sets of molecules act as localized states, with the efficiency of charge transport being determined by how easily the charges move from one state to another. The charges in organic semiconductors are polaronic (short-range Holstein), and their transport as a function of temperature has been described by several models – variable range hopping, delocalized charge transport, multiple trapping and release, and other hybrid models [11-16]. The variable range hopping model presents quantum mechanical tunneling as the primary mechanism for charge transport, in which the charges "hop" from one localized state to another with the probability of this event occurring varying with distance and energy distribution [7]. The multiple trapping and release model, on the other hand, considers the charges to be trapped in the localized states owing to defects, and that charge transport occurs when these charges are promoted to an "extended-state band" [7]. The initial injection of charges from the contact into the bulk can be described by a combination

of thermionic and field emission as well as possible contributions from hopping between localized states [8].

Extensive research has been done into not only different organic semiconductors but also the impact of fabrication methods which are used for processing those materials. Highly uniform organic semiconductor films can be obtained through a variety of methods such as thermal evaporation, electric-blade deposition, single crystal growth methods, spray coating and more [17]. Each of these introduce unique parameters that can be tuned to acquire a desired film thickness or polycrystallinity, and some (such as inkjet printing) allow for large scalability. Crystallinity in the semiconductor film is crucial for high charge mobility because it leads to higher overlap of the molecular orbitals, which facilitates better charge transport between the localized states [7-9].

The choice of metals used for source and drain contacts which are applied to an organic semiconductor are also of great importance. Unlike the contacts in a MOSFET - which utilized heavily doped regions of the semiconductor to promote the minority carrier transport while screening the majority carrier transport – metallic contacts are employed in organic systems to directly inject the charge carriers into the semiconductor [7]. An ohmic contact with negligible voltage drop is desired [8]. The ease with which the charges can be injected into the semiconductor depends on the alignment of the metal's work function with the HOMO and LUMO levels of the semiconductor. Alignment with the HOMO level results in p-type transport, alignment with the LUMO level results in n-type transport, and a work function that sits close to the Fermi level of the semiconductor can give ambipolar behavior. The interface between the semiconductor and metal will result in band-bending as a common Fermi energy is established. Other effects such as Fermi level pinning and

the push-back effect result in shifting of the HOMO and LUMO levels and energy barriers, making exact prediction of alignment difficult [8]. Figure 2.3 shows a simplified diagram of the band-bending when the contact material and semiconductor are brought together. Here φ_m represents the work function of the metal, Δp represents the difference in energy between the HOMO level and the Fermi level, and Δn represents the difference in energy between the LUMO level and the Fermi level. In Figure 2.3 a) Δp is less than Δn, which indicates that holes will be more easily injected than electrons. In Figure 2.3 b) Δn is less than Δp, which indicates that electrons will be more easily injected than holes.

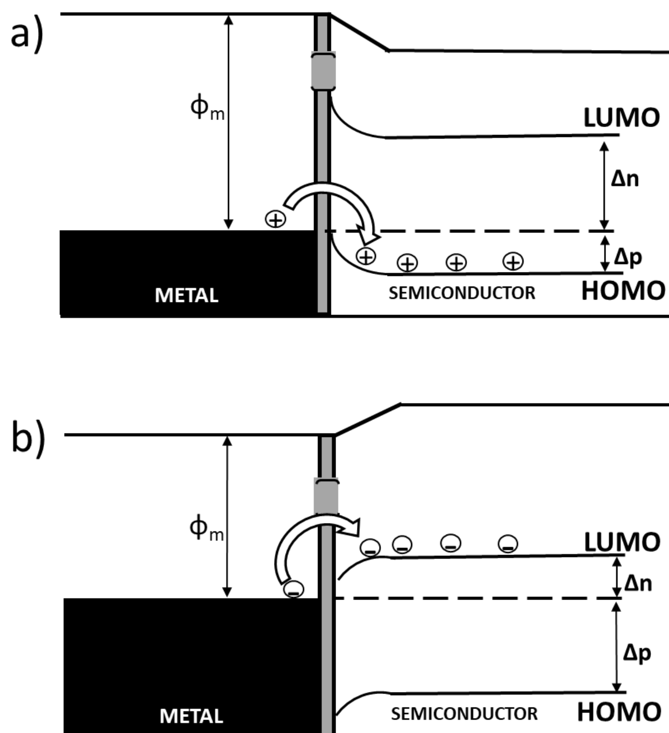

Figure 2.3. Simple diagram outlining the injection of a) holes and b) electrons into an organic semiconductor from a metallic contact. The dashed line represents the common Fermi level established when the metal and semiconductor are brought into contact with one another. Adapted based on [8].

The lower temperature processing conditions of these organic materials also allow for polymer dielectrics to be used to separate the charge-transport channel from the metallic

gate in capacitor and FET architectures. The use of such polymers introduces more tunable parameters which can be studied based on their chemical composition, surface energy, and more to observe changes to device performance, which will be discussed in later sections.

2.4 Polymer and Small Molecule Semiconductors

This section will focus on some of the physical characteristics of the conjugated polymers and small molecules considered throughout this work. Beyond this overview, their application in devices will be explored further in later chapters.

Small Molecules - Pentacene and TIPS-Pentacene

Small molecule semiconductors are generally insoluble in organic solvents and rely on the usage of thermal sublimation or vapor deposition to form polycrystalline films [7]. Among small molecule semiconductors, one of the most commonly studied is pentacene, an aromatic hydrocarbon made up of five benzene rings. This material features an edge-to-face and face-to-face molecular packing [18]. Dr. John Anthony further developed this material through the functionalization of pentacene with triisopropylsilylethynyl (TIPS) to render a material which was soluble in common organic solvents, air stable, and features improved overlap of π-orbitals to facilitate stronger charge transport [7,18]. This solubility opens up the possibility of exploring solution-processing methods, such as spincoating and dropcasting.

Pentacene, obtained through TCI Chemicals, was deposited via thermal evaporation utilizing a quartz crucible. The film evaporated at a rate of 0.3 angstroms/second and would evaporate to a maximum thickness between 50 – 60 nm. TIPS-Pentacene was obtained from Dr. John Anthony's research group as well as from Sigma Aldrich, whose

characteristics are outlined in Figure 2.4 below. To form a solution, it was dissolved in anhydrous toluene, which was obtained through Sigma Aldrich, at a concentration of 2 mg/mL. A TIPS-Pentacene film was usually formed via an elevated dropcasting method, which is discussed in more detail in Chapter 3. The application of both of these materials in FET devices will be discussed in more depth in Chapters 4 and 7.

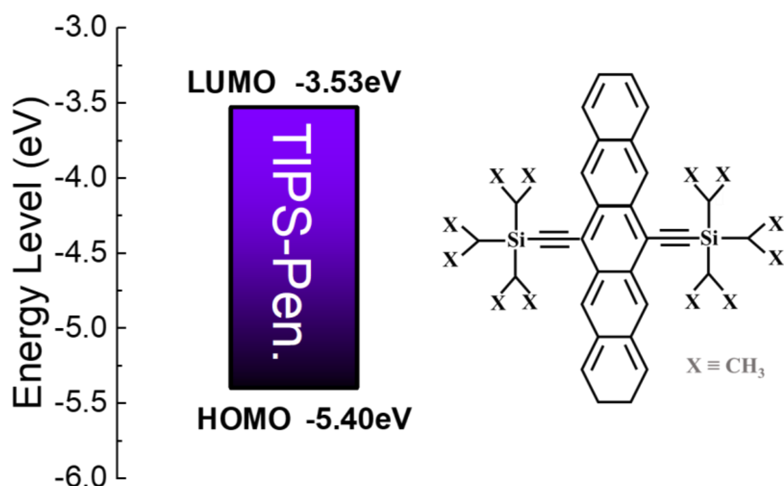

Figure 2.4. Energy level diagram of TIPS-Pentacene outlining its HOMO and LUMO levels. Inset shows chemical structure of TIPS-Pentacene and was adapted based on [7,18].

Conjugated Donor-Acceptor Polymers - DPP-DTT and Isoindigo

Conjugated alternating donor - acceptor (D-A) polymers are a class of organic materials whose properties can be tuned in a manner synonymous to the doping of inorganic semiconductors. The strong charge delocalization in donor-acceptor (D-A) copolymers continue to attract attention in electronic devices due to their versatility and tunability. The choice of donor or acceptor moieties when incorporated can be balanced to achieve the desired behavior, affecting charge injection at the electrode/semiconductor interface,

molecular ordering, and overlap of the π-orbitals [19]. D-A polymers are inherently ambipolar with the majority charge carrier type determined by the relative strength of the moieties – more donor groups enhancing hole transport (p-type), and more acceptor groups enhancing electron transport (n-type).

In the area of p-type solution processable FETs, diketopyrrolopyrrole (DPP) based copolymers have proven to be air-stable, robust, and demonstrate high carrier mobilities [20-22]. The tuning of the donor-acceptor (D-A) moieties in DPP copolymers not only lowers the band-gap energies but renders chemical stability. The enhanced intermolecular interactions between the D-A units result in molecular packing with increased electronic bandwidths, which is favorable for charge transport [23]. A DPP copolymer, with the donor moiety of dithienylthieno[3,2-b]thiophene (DTT) and an acceptor moiety of n-alkyl (referred to hereafter fully as DPP-DTT) has reported HOMO and LUMO levels of -5.2 eV and -3.5 eV, respectively [19]. These characteristics are outlined in Figure 2.5 below. For good hole injection, gold (Au) is utilized as the metallic contact for this semiconductor. P-type carrier mobilities > 5 cm^2/Vs have previously been shown in FET architectures with modified SiO_2 dielectrics, as well as upon modifying the copolymer in a polystyrene matrix using self-assembly phenomena [23]. DPP copolymers with SiO_2 and divinyltetramethylsiloxane bisbenzocyclobutene (BCB) dielectrics in bottom gate FET configurations or low κ dielectrics such as CYTOP in top gate FET architectures, show relatively high operating voltages [23]. To overcome these high operating voltages, the utilization of high-κ dielectric layer is explored. Use of DPP-DTT with this dielectric will be discussed further in Chapters 4 and 6.

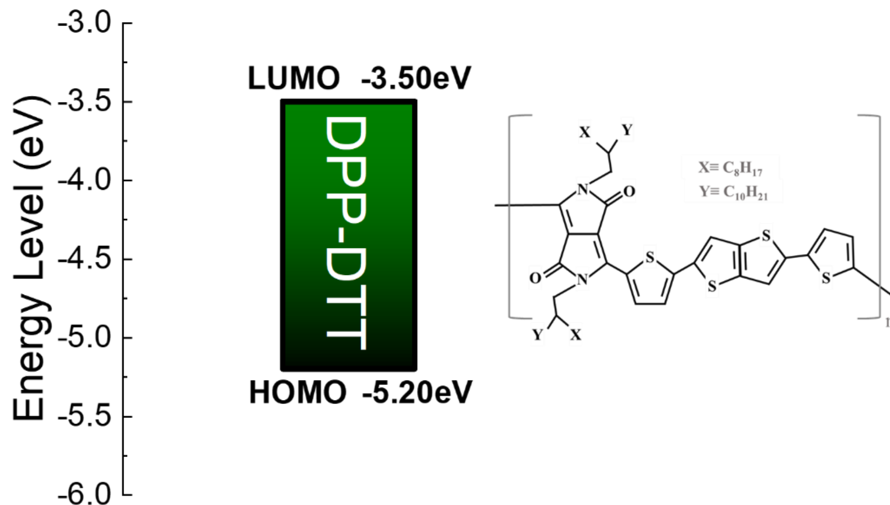

Figure 2.5. Energy level diagram of DPP-DTT outlining its HOMO and LUMO levels. Inset shows chemical structure of DPP-DTT and was adapted based on [19].

The DPP-DTT copolymer was procured through 1-Material Inc. Chloroform (HPLC grade) and 1,2-Dichlorobenzene (anhydrous 98%) were obtained from Sigma Aldrich. DPP-DTT precursor solution was made by dissolving the polymer in either equal parts chloroform and 1,2 dichlorobenzene or pure 1,2 dichlorobenzene to obtain a 5.0 mg/mL concentration. A magnetic stirrer was added, and the solution was allowed to stir at room temperature overnight (>12 hours).

Isoindigo (IID), another D-A copolymer, has received less attention compared to others, presumably due to its low charge carrier mobility. Some of the early work using isoindigo, dates back to more than 10 years ago, where the optical and electrochemical properties of IID based polymers were found to be favorable for optoelectronic devices [24]. Since then, electron deficient IID units have been incorporated in solar cells [25,26], and their ambipolar nature has been exploited in p- and n-type FETs [27-30]. Furthermore,

thiazole-based materials are emerging as a viable route towards n-type or ambipolar properties in conjugated polymers [31-33]. This polymer will be further discussed in regard to its properties and fabrication methods in Chapter 5.

2.5 Organic FET Devices

Unlike MOSFETs which operate by inducing the inversion regime in the semiconductor, organic semiconductors operate by utilizing the electric field produced by the gate to accumulate majority charge carriers at the semiconductor-dielectric interface. The accumulated charges produce the channel through which transport between the source and drain contacts can occur. Charge accumulation at the interface is directly proportional to the capacitance of the dielectric layer and the bias applied to the gate. The capacitance of the dielectric layer can be expressed by the following equation:

$$\frac{C}{A} = \frac{\kappa}{d}\varepsilon_0 \quad (2.1)$$

where κ is the dielectric constant, ε_o is the permittivity of free space, and d is the thickness of the dielectric layer, and A is the cross-sectional area of the device. It is apparent from equation 2.1 that the capacitance of the dielectric layer (and by extension the amount of accumulated charge) can be enhanced by reducing the film thickness and by using a material with a high dielectric constant for the layer. Solution processable polymers lend themselves towards the former form of enhancement, allowing for thin films (< 1μm) through fabrication techniques that require very low energy for processing. Looking back at the variable range hopping model discussed earlier, the accumulation of charges is considered to fill lower energy states and reduce the activation energy associated with the hopping effect [7]. Because the semiconductor-dielectric interface governs charge

transport mechanisms in FET architectures, achieving intrinsic carrier mobility specific to a semiconductor is challenging. The dielectric layer not only influences the morphology of the semiconducting layer, but it may also affect the density of states (DOS) due to local polarization effects [34-36].

Once the charges have been accumulated at the interface, the bias applied between the metallic drain and source contacts (V_{DS}) similarly drives the charges across the channel. It is important to note here that in organic semiconductors the threshold voltage (V_T) represents the small bias necessary to first allow charge carriers to fill trap states (due to crystal nonuniformity or other defects) before the rest of the free charges can move through the channel. Using this definition of threshold voltage, the organic FET operates in a way synonymous to the traditional MOSFET. The charge carrier mobility, an important performance metric, in organic FETs has increased by orders of magnitudes in the last two decades from 10^{-5} to 10^{-6} cm^2/Vs in the early 1990s to over 10 cm^2/Vs more recently [37].

Another crucial metric of device performance is the contact resistance due to the interface between the source (and drain) contact and the organic semiconductor, as previously discussed in regard to Figure 2.3. Parasitic contact effects in such systems can arise from several different origins, such as contact architecture, charge-carrier density, interface dipoles, film morphology, and more [38]. When the metal-semiconductor interface forms, a common Fermi level is established and Schottky barriers dominantly determine the ease with which charges can be injected to either the HOMO or LUMO level of the semiconductor [38]. Pinning of the Fermi level can occur if there are interfacial defect states present, resulting in no variation to the Schottky barrier heights when the work function of the metal is altered [38]. For short channel FETs, the contact resistance affects

the linear region more than the saturation region, with a high contact resistance demonstrating non-ohmic behavior for the contacts that can be observed in the devices' output characteristics [8,38]. Device simulation at the molecular level suggests that mobilities obtained from the saturation and linear region are similar as long as the energetic disorder of the semiconductor is less than 50 meV [39]. The contact resistance of a device can be determined using the Transmission Line Method under the assumption of ohmic contacts. Prior to the "pinch off" point, the device is operating in the linear regime and acts as a variable resistor. Here, the total resistance between the contacts can be expressed as:

$$R_T = R_{Ch} + R_S + R_D \qquad (2.2)$$

where R_T denotes the total resistance, R_{Ch} denotes the resistance of the semiconducting channel, and R_S and R_D represent the resistances of the source and drain contacts, respectively. The total resistance (R_T) is related to the change in the channel current with a changing drain-source bias ($\partial V_{DS}/\partial I_{DS}$). This value can be determined from the inverse of the slope from a fit of the linear regime of the I-V characteristics for the FET device, which is shown in Figure 2.6 a). The device's output characteristics can be used for this purpose. The channel resistance can be approximated as follows,

$$R_{Ch} \approx \frac{L}{\mu_{eff} C_i W (V_{GS} - V_T)} \qquad (2.3)$$

where μ_{eff} is the effective mobility in the absence of the influence of contact resistance. By combining equation 2.2 with equation 2.3, the total resistance can be linearly related to the channel length. If the total resistance is plotted against the varying channel length, the intercept of this linear relationship reflects that resistance if the channel length were zero, resulting in the combined contact resistance of both source and drain. This is shown in

Figure 2.6 b). The slope of this relationship can also be used for calculating the effective mobility if V_T is known. The characterization and behavior of organic FET devices will be explored in more depth in the following chapter.

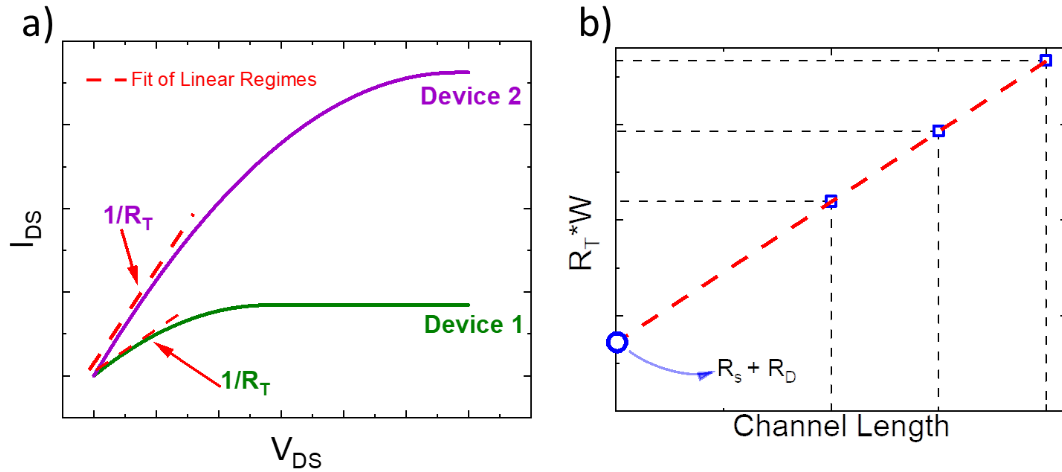

Figure 2.6. a) Example of the inverse of the total resistance of a device extracted from the linear region of the channel I-V characteristics for an FET device. b) Example plot of the width-normalized resistance versus the varying channel length of each device, where the resistance of the contacts is extract from the intercept with the y-axis.

Chapter 3: Fabrication and Characterization of Devices

As previously mentioned, the use of organic semiconductors in electronic devices opens the possibility of employing solution processing methods in fabrication. This chapter seeks to outline some of these methods that have been employed as part of this research as well as to demonstrate the techniques used to characterize the resulting devices. In future chapters, when the methods used to fabricate each of the devices studied are discussed, they will frequently refer back to this chapter for a more detailed description.

3.1 FET Architectures

The field effect transistor is an electronic device comprised of three terminals. As previously discussed, two of these terminals are in contact with the semiconductor layer and are denoted as the "source" and "drain." The other metallic terminal is separated from the semiconductor by the oxide or dielectric layer and is denoted as the "gate." When constructing a FET device, one can adopt up to four different architectures which can be divided into two families of structures: coplanar and staggered. A coplanar structure will either be a Bottom Gate / Bottom Contact (BGBC) or a Top Gate / Top Contact (TGTC) architecture. A staggered structure will either be a Bottom Gate / Top Contact (BGTC) architecture or a Top Gate / Bottom Contact (TGBC) architecture. Figure 3.1 demonstrates each of these architectures. The staggered structure approach in organic devices has a lower contact resistance than the coplanar structure owing to a larger effective area for charge injection [7,38]. The charge injection in staggered structures, however, are also plagued by resistive effects stemming from the thickness of the semiconductor layer [26]. In this way,

reducing the thickness of the semiconductor will be important to improving charge transport in the device when utilizing such a structure.

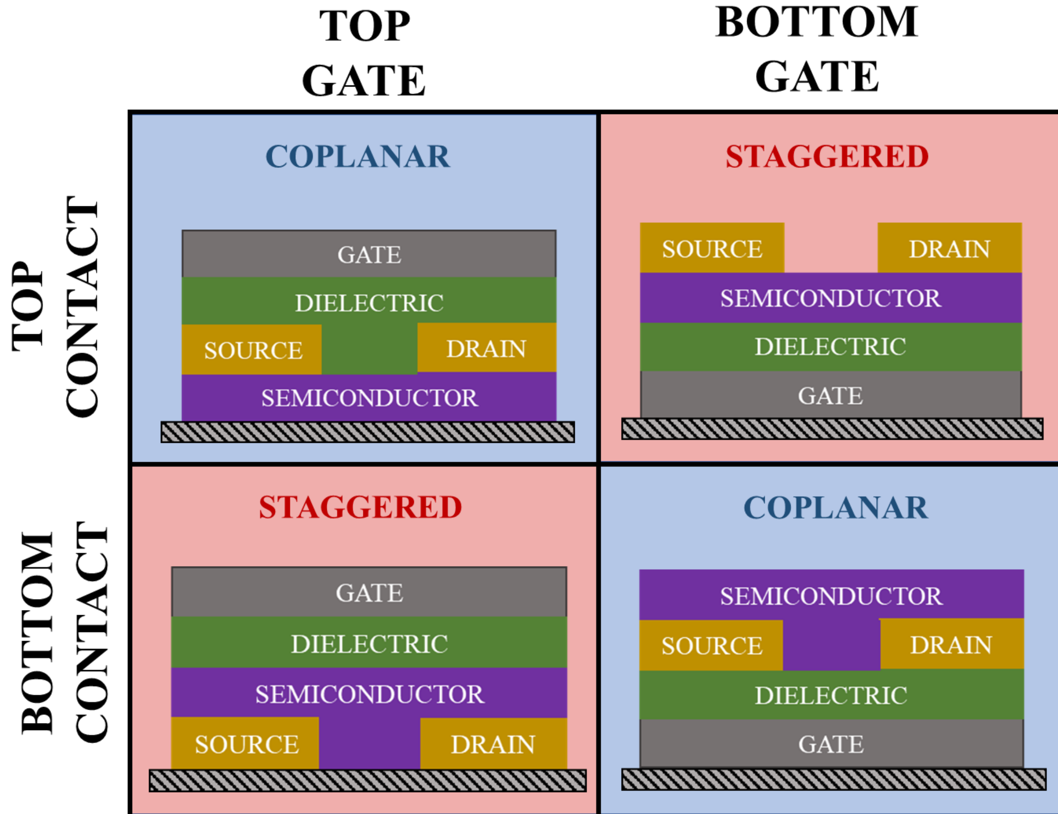

Figure 3.1. Types of architectures for FET devices. For a coplanar structure the source and drain contacts rest on the same plane as the semiconductor/dielectric interface while in a staggered structure the contacts are separated from the interface by the thickness of the semiconductor layer.

The question of which architecture to employ when fabricating a device can be influenced by several different factors. Firstly, what dielectric is being employed? If an oxide is being used as the dielectric, then either a BGTC or BGBC architecture would likely be utilized. If using spincoated CYTOP, then either a TGBC or TGTC architecture would be utilized, as it would otherwise prove difficult to deposit the semiconducting layer on top of this dielectric owing to its heavy fluorination. Secondly, does the semiconductor layer require encapsulation? Some semiconductors are air-stable, while others can see vast

changes in their behavior owing to the presence of oxygen. This is one of the key differences between small molecules pentacene and TIPS-pentacene, where only the latter is air-stable. By employing a TGBC or TGTC structure, the dielectric layer (when deposited over the semiconductor in a vacuum or nitrogen environment) can act to shield the charge transport layer from ambient atmosphere when the device is in operation. Thirdly, are any surface treatments being applied to your contacts to alter its interface with the semiconductor? If so, the contacts' surfaces need to be modified before the semiconductor is applied, and the charge injection interface formed. In this way, one would need to use either a BGBC or a TGBC architecture to ensure the source and drain are exposed before the semiconductor layer is formed. All of the devices described within this work utilize a staggered structure.

3.2 Substrate Preparation and Cleaning

The substrate used for the device acts as the foundational layer upon which everything else is built. In this work, the substates commonly used across all devices are either glass or heavily doped silicon with a 200nm oxide layer (referred hereafter as just "silicon" or "Si++/SiO_2"). The glass is 1mm-thick microscope slides obtained from Fisher Scientific and the silicon wafers were obtained through Silicon Quest International Inc as well as Wafer Pro. For a given set of devices, a 25.4mm x 25.4mm (1in x 1in) square was cut using a diamond-tipped pen. The size was chosen such that the substrate will fit neatly inside of the holders use for thermal evaporation, which was always utilized to apply one or more of the metallic layers for the devices.

Once cut, the substrates were rinsed with acetone and placed in an acetone bath, where they were ultrasonicated for 10 minutes. This step was then repeated with isopropanol. The substrates were then rinsed with DI water and dried with compressed air or a nitrogen gas flow. Finally, the substrates were baked in an oven at 100°C to remove any remaining moisture. The substrates were then placed into containers to protect them from any dust particles or other contaminants present within the lab space. This organic cleaning process represents the minimum amount of cleaning performed for each device. The importance of this process cannot be overstated, as the presence of dust or other contaminants in any of the layers act as defects and can facilitate charge trapping or leakage of current through the dielectric layer, even to the point of short-circuiting the device. As such, pristine surfaces are the necessary starting point for device fabrication, and care needs to be taken throughout the process to ensure no contamination alters any step of building the device.

Further treatment of the substrates will sometimes also include the use of a plasma treatment. A Harrick Plasma PDC-32G plasma cleaner was used to expose the surfaces to plasma formed from oxygen gas (obtained through AirGas). This oxygen plasma acts to etch away any unwanted organic matter remaining after the cleaning process while minimally affecting the roughness of the surface or damaging it. As will be discussed in more detail later on, this process can also be used to fill oxygen vacancies in films (a process referred to hereafter as a UV-Ozone treatment) [40]. The substrate (or film) was exposed to the oxygen plasma at a gas pressure between 300-500 mTorr for 10 minutes (or 60 seconds in the case of filling vacancies).

Further beyond this, a strong piranha solution can be employed to chemically remove any remaining organic contaminants; however, this process also results in the surface being

incredibly hydrophilic. For the devices made as part of this work, this solution was only employed as a prerequisite to applying a self-assembled monolayer, which will be discussed later.

3.3 Techniques for Making Thin Films

This section outlines several of the methods used for creating the thin films and layers utilized in this work, including those used for metals, semiconductors, and insulators.

Thermal Evaporation

After the substrate has been cleaned, the next step is to add one of the metallic layers, either the source/drain contacts for a TGBC architecture or the gate for a BGTC architecture. In the case of Si++/SiO_2, this step does not need to be completed if using the oxide as the dielectric, as the heavily doped portion of the silicon is conductive and will act as the conductive gate.

For a metallic gate, aluminum is used in this work as it adheres well to the surface of glass when evaporated. For the source and drain contacts, more care must be taken in choosing the metal employed. As previously outlined in Chapter 2, the presence of an energetic mismatch between work function of the metal contact and the Fermi level of the semiconductor can result in less efficient charge injection. Generally, gold (Au) and silver (Ag) will be used for p-type semiconductors (or ambipolar systems) whereas aluminum (Al) or even calcium (Ca) will be used for n-type semiconductors. For the devices constructed as part of this work, the metals commonly used are gold and aluminum. 99.99% pure wires of each material were acquired through Kurt J. Lesker Inc.

Evaporation is a version of physical vapor deposition (PVD) which can be used to form thin films. Although there are several ways to achieve vaporization of the target material, each method takes place under vacuum to ensure that the vapor can directly travel upwards onto the substrate. An Mbraun Thermal Evaporation system was employed with both a roughing pump (Edwards) and turbomolecular pump (Pfeifer Vacuum) to allow for the ambient atmosphere to reach pressures on the order of 10^{-5} mbar within the chamber. Through the thermal evaporation approach, metallic boats as well as crucibles are used to house the bulk material which is then heated via a strong electric current to vaporize it. Tungsten (W) boats were used for the evaporation of both aluminum and gold (although it should be noted that there were separate boats for each material). For the small molecule material semiconductor pentacene, as well as other organic materials, a quartz crucible was employed. Each material's deposition is controlled by an SQC-222 controller associate with the thermal evaporator system, allowing the specification of power applied to the boat, desired thickness, the upper limited allowed for the thickness, and the desire deposition rate (among other parameters). During the deposition, the thickness of the layer was monitored using 6MHz gold-coated quartz crystals obtained from Inficon. The thickness usually set for each of our evaporated layers is 50nm (with an upper limit of 51nm). Unless otherwise stated, it is assumed each evaporated layer reported as part of this work has this same thickness. During the thermal evaporation process, a metallic mask was usually applied to the substrate and held in place with screws to pattern the contacts to the desired shape, size, and orientation.

Spincoating

After the initial metal layer is evaporated, the next step is to apply the polymer films, starting with either the semiconductor (in the case of a top-gate structure) or the dielectric (in the case of a bottom-gate architecture). Solvents such as chloroform, dichlorobenzene (DCB), dimethyl sulfoxide (DMSO), dimethyl formamide (DMF) and toluene are some examples of solvents used for forming solutions with polymers. It should be noted that when using both a solution-processable semiconductor and dielectric, one must be careful not to choose materials for each layer which share common solvents, as the deposition of the second layer could act to remove the first. For the polymer materials used in this work, the specific solvents used for each is discussed in their relevant sections. The concentration of the solution (reported hereafter as either a mass weight percent or as milligram of solute per milliliter of solvent) will affect the thickness of the film. Generally, increasing the concentration of the solution (and in turn its viscosity) will lead to thicker films.

For the spincoating process, a small volume of solution was dropped onto the surface of the substrate which is being made to spin at a constant rotational speed, reported in this work as rotations per minute (RPM). The volume dropped was in excess of what will actually contribute to the final film, so as to ensure that uniform coverage of the entire surface. As the substrate continued to spin, solution spread across the surface, and the excess volume was ejected from the sides. As the substrate's final rotational speed was achieved, the film continued to thin owing to a combination of effects of the excess solution being ejected and solvent evaporation.

The dropping of solution onto the substrate will usually be performed in one of two ways: *dynamically* or *statically*. During dynamic dropcasting, the solution was expelled onto the substrate after it had already begun to spin and is reaching its maximum rotational speed. For static dropcasting, solution was applied to the surface prior to initiating the spincoating process. Between both methods, the static dropcasting will usually result in thicker films. Static dropcasting will sometimes be preferrable to dynamic as it can help to ensure uniform coverage of the substrate.

Following the casting of the film, further annealing is performed to remove any remaining solvent and guide film formation. The temperature used can be tuned to achieve the desired properties of the film. Studies have previously demonstrated how the variation of annealing temperature of similarly cast films will affect the characteristics of the film. For example, Ashraf et al observed a drop in the threshold voltage of FET devices made using a modified isoindigo polymer as the annealing temperature was varied between 80°C and 300°C [41]. In this way, spincoating and subsequent annealing of the film offers many parameters which can be tuned to achieve the desired film thickness and uniformity through modifying the solution concentration, spin speeds and times, and annealing temperatures. Some film properties can be further modified through processes such as cross-linking or electrical poling, which will be discussed later.

For this work, a specialty coating system version 3.4e Model 6708D integrated to the Mbraun glove box system was used for spincoating, in which a vacuum is used to hold substrates in place. Within the glove box, an oven was used for the purposes of annealing. For either of these steps, the system made use of a charcoal-based solvent trap to catch solvent vapor before it would spread to the other parts of the glove box system. Unless

otherwise stated, any film reported in this work which used spincoating can be assumed to have been coated and annealed in a nitrogen atmosphere. The spin speeds and annealing temperatures will be discussed on a case-by-case basis. In many devices, these films would be patterned through use of Teflon tape, which would be administered to the substrate prior to spincoating and removed prior to annealing. This patterning would act to restrict the flow to a thin channel for the purposes of ensuring the films did not cover or come into contact with other parts of the architecture.

Dropcasting

Thermal evaporation and spincoating represent the cornerstones of thin film processing techniques employed for the fabrication of devices in this work. Both methods render uniform films. Sometimes, though, specific patterning is desired towards enhancing crystallinity in semiconductors. One method that can be altered to invoke such crystallinity is dropcasting.

Dropcasting works by simply putting some small volume of solution onto the substrate and allowing it to dry. These films will generally be thicker and less uniform than those achieved through spincoating but can be modified in simple ways to promote a particular type of solvent evaporation to guide film formation and crystallinity. One such method was demonstrated by Lee et al., in which a solution of triisopropylsilylethynyl pentacene (TIPS pentacene) was dropcast onto a tilted substrate and allowed the film to form in a solvent atmosphere [42]. Here, the upper contact line of the solution acts as a pinning site, allowing for the growth of ribbon-like crystals along the direction of the substrates tilt [42]. This crystallinity in organic systems allows for greater overlap of the π-π^* orbitals which

facilitate charge transport across the molecules, and devices made using this method of dropcasting have demonstrated FET devices with mobilities on the order of 0.1 – 1 cm^2/Vs [42,43].

In this work, the tilted dropcasting method has been used for TIPS-Pentacene devices made in a BGTC architecture. The TIPS-Pentacene was obtained from Dr. John Anthony and the toluene used as the solvent was obtained from Sigma Aldrich. The solution was made at a concentration of 3mg/mL and was allowed to heat for 1 hour at 60°C and then stirred until needed. Solution dropcasting was performed within a large crucible resting on a hot plate at 60°C, with the entire setup taking place within a fume hood. The hot plate was adjusted to ensure it was level. Figure 3.2 outlines the setup below. Five pieces of tape were placed on one side of the crucible, and a metallic box (one inch on each side) was placed within the crucible such that one side rested on the tape and one side rested on the other end of the crucible. The slight elevation of the tape creates the tilt to guide the flow of solution and formation of crystals. The substrate (already containing the gate and dielectric layers) was placed on top of the metal box in such an orientation that the solution would descend in a direction parallel to the source-drain channel (perpendicular to the patterned gate). Prior to dropcasting the solution, 80μL of toluene was dropped within the crucible (at its base) to enhance the solvent atmosphere, which aids in the film formation. 80μL of the TIPS-Pentacene solution was dropped in a straight line across the elevated end of the substrate. A cover was immediately placed to capture the toluene vapor to form the solvent atmosphere within the crucible. The film was allowed to form in this way for 30 minutes. The substrate was then removed, and the sides of the substrate were rinsed with toluene to remove unwanted coverage of the semiconductor, restricting it to the area above

the gate where the contacts would be placed to form the devices. For TIPS-Pentacene, Au contacts were thermally evaporated for the source and drain.

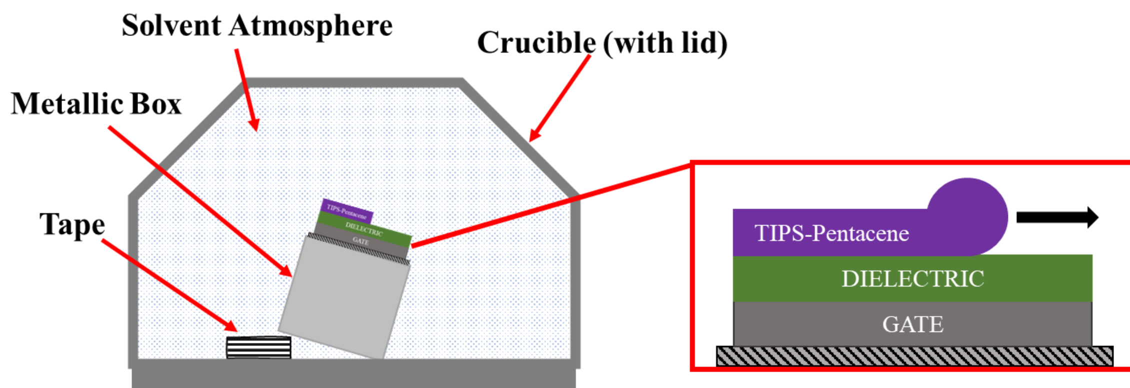

Figure 3.2. Setup for dropcasting a film at an angle while maintaining a solvent atmosphere.

3.4 Surface Modification Methods

Contact Modification

As discussed previously in Chapter 2, the difference in energy between the work function of the metal contacts and the semiconductor layer plays a crucial role in determining the ease with which charges are injected for transport. There are several methods that can be employed to modify the metallic contacts to better facilitate charge injection; however, such methods require the use of a bottom contact architecture (TGBC or BGBC).

The introduction of interlayers through physiosorbed or chemisorbed self-assembled monolayers (SAM) has been shown to alter the work function of metals they are applied to, and in some cases, improve the charge injection between the metal and semiconductor layers [38,44,45]. The application of pentafluroubenzenethiol (PFBT) or polyethylenimine ethoxylated (PEIE) has been shown to improve hole and electron transport, respectively

[38,45]. The method by which each of these layers were applied to devices of this work will be outlined below.

PFBT can be used to increase the work function of gold and drive it closer to the HOMO level of some of the semiconducting materials discussed in this work. This layer acts to improve hole injection and thus p-type behavior of the final FET device. A 10mM concentration solution of PFBT was made by mixing 40μL of stock PFBT with 30mL of isopropanol. After a short mixing period, the organically cleaned substrates with evaporated gold contacts sat in the mixture for 30 minutes to allow the monolayer to form. The substrates were then rinsed with isopropanol, allowed to briefly rest in an isopropanol bath, and then finally dried with either compressed air or nitrogen gas.

On the other hand, PEIE can be used to decrease the work function of gold and drive it closer to the LUMO level of some of the semiconducting materials discussed in this work. This layer acts to improve electron injection and thus n-type behavior of the final FET device. A 0.4 wt% solution of PEIE was made by mixing a 92:1 ratio (by weight) of 2-methoxyethanol to the PEIE solution (which was already diluted to 37% in water in the stock solution). 200 μL of the solution was dynamically spincoated onto each substrate at 5000 RPM for 60 seconds. The layer was then annealed on a hotplate at 100°C for 10 minutes in ambient atmosphere (specifically within a fume hood).

It has also been demonstrated that the formation of a thin AuO_x layer on gold contacts can act to improve hole injection and reduce contact resistance [46]. In this way, one could feasibly use the plasma cleaning / UV-Ozone method previously discussed to improve the performance of p-type FET devices.

Oxide Modification

When utilizing silicon wafers as the gate/oxide layer for device fabrication, a self-assembled monolayer of octadecyltrichlororsilane (OTS) applied to the oxide can act to make the surface more hydrophobic and improve the formation of spincoated films. The OTS material has a hydrophilic "tail" which readily anchors to a hydrophilic surface, which then orients the hydrophobic "head" upwards to form the surface of the monolayer on top of the oxide.

To form this SAM of OTS, the substrates were organically cleaned. Following this, the substrates were bathed in a Pirhana solution (using a 10:3 ratio by volume of sulfuric acid to hydrogen peroxide) for 10 minutes, which acts to remove any remaining organic contaminants and makes the surface more hydrophilic to guide the alignment of the OTS. Each substrate was then rinsed with DI water and allowed to sit in a DI water bath before being dried with compressed air. To ensure that the water had been fully removed, the substrates were allowed to sit for 24 hours before proceeding. The substrates were later placed into a solution of OTS (about 25 mg/mL in HPLC-grade toluene) for 25 seconds before being rinsed with HPLC-grade toluene, briefly sonicated in a toluene bath, rinsed with isopropanol and DI water, and finally dried with compressed air.

3.5 Operation and Characterization of FET Devices

As previously discussed in Chapter 2, depending on the bias applied between the source and drain contacts of an FET device, it can operate in two regimes - the linear regime and the saturation regime - which are separated based on the "pinch off" point for the device. A MOSFET works through creating an inversion layer to transport charges and an organic

FET works through accumulating charges to form the transport channel. Although there are differences in the charge-transport mechanisms as well as some parameters (such as how the threshold voltage is defined), the operation of both types of FET devices can be described in a similar manner, as will be outlined below.

In the linear regime, which occurs when $|V_{DS}| \leq |V_{GS} - V_T|$, the current between the drain and source contacts (I_{DS}) of an FET can be expressed with the following equation,

$$I_{DS} = \frac{W}{L}\mu C_i\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \qquad (3.1)$$

where W and L are the channel width and length of the device, μ is the mobility, and C_i is the capacitance per unit area of the oxide (or insulator) layer. In a similar manner, the current in the saturation regime, which occurs when $|V_{DS}| \geq |V_{GS} - V_T|$, can be expressed as follows,

$$I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_T)^2 \qquad (3.2)$$

Varying V_{GS} and observing the modulation of the I_{DS}-V_{DS} sweep of the device comprises what is known as the *output characteristics*, which is shown in Figure 3.3 a). Similarly, observing changes in I_{DS} with varying V_{GS} while holding V_{DS} constant produces what is known as the *transfer characteristics* of the device, which is shown in Figure 3.3 b). From the transfer characteristics, the mobility of the charge carriers can be determined from measurements taken in either the linear or saturation regime,

$$\mu_{lin} = \frac{L}{WC_iV_{DS}}\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \qquad (3.3)$$

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad (3.4)$$

In both above equations, the differentials in parentheses can be calculated from the slope of a linear fit taken from the transfer characteristics when measured in the associated regime. The on/off ratio can also be determined from this data by dividing the maximum current (I_{on}) by the current measured prior to the threshold voltage (V_T), denoting the "off" state (I_{off}). Using the previously mentioned linear fit, by finding the intercept with the I_{DS} axis, the threshold voltage for the device can also be calculated. Finally, the device's subthreshold swing (SS) can be calculated from a linear fit of the transfer data when the current is plotted in a logarithmic scale:

$$SS = \frac{\partial V_{GS}}{\partial(log_{10} I_{DS})} \qquad (3.5)$$

These parameters provide insight into the charge transport within the semiconductor layer and how the variation of the one or more device parameters might affect it. High mobilities, reflecting large amounts of charge being moved through the device channel, are desirable. A large on/off ratio coupled with a small subthreshold swing will denote a device that has distinctly different "on" and "off" states which can be switched between rapidly. Minimizing the threshold voltage-and by extension the operating biases of the device-will reduce power consumption.

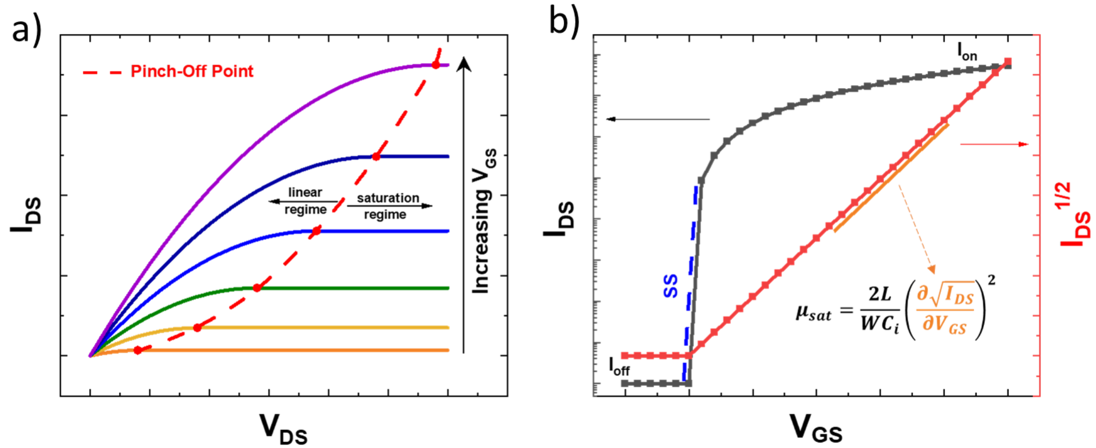

Figure 3.3. a) Example of an FET's output characteristics, where the pinch off point increases within increasing gate bias. b) Example of an FET's transfer characteristics demonstrating how both the semi-log and square root of the I-V data is used to extract the device characteristics.

Both the output and transfer characteristics were measured by making use of Keithley 2400 and Keithley 236 source meters, where the 2400 would act to apply the gate bias and measure any parasitic current while the 236 would apply the source-drain bias and measure the relevant channel current. Figure 3.4 a) shows how the connections across each source meter were made. The biases were applied to the device by carefully touching the evaporated contacts with probes. As shown in Figure 3.4 b), the setup featured an adjustable stage as well as a microscope which could be used to carefully adjust probe position. The substrate was held to the stage using an applied vacuum. The stage itself is conductive, so when using Si++/SiO_2 for the gate/oxide layer, one could apply the bias to the stage directly rather than via a probe. The microscope also had a Leica EC3 digital color camera attachment, allowing for capturing optical images of the devices and films on a scale of hundreds of micrometers. Programs written in LabView were used to sweep and step the biases in the desired fashion for the measurements. It is worth noting here that the measurement of the parasitic current using the 2400 source meter cannot be measured

accurately below the nanoamp range. As an alternative to the 2400 & 236, a Keithley 2612 B would sometimes be utilized to measure the device characteristics, in which case the current could be measured down to 1 picoamp.

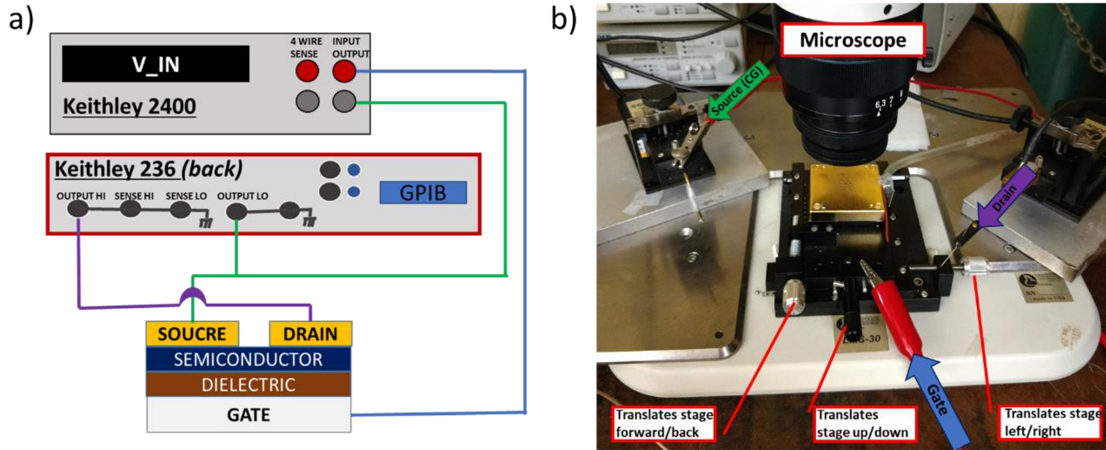

Figure 3.4. a) Diagram outlining how the sourcemeters were connected to measure FET devices. b) Image of measurement stage used, including the probes used to apply biases, stage translating elements, and optical microscope.

3.6 Operation and Characterization of Capacitor Devices

Capacitance measurements of either metal-insulator-metal (MIM) or metal-insulator-semiconductor (MIS) devices were performed using a Hewlett Packard 4284A LCR Meter. For some of the FET devices fabricated, the evaporation mask used would provide circular masks for forming MIS devices as well, but in many cases separate MIM and MIS substrates would be fabricated alongside their FET counterparts to ensure that a large variety of capacitive devices could be measured and compared. Figure 3.5 a) shows the setup of the LCR meter with an MIS device for measurement and Figure 3.5 b) demonstrates a measurement of such a device. A Labview program was used for both the capacitance versus voltage (C-V) and capacitance versus frequency (C-F) measurements of the device.

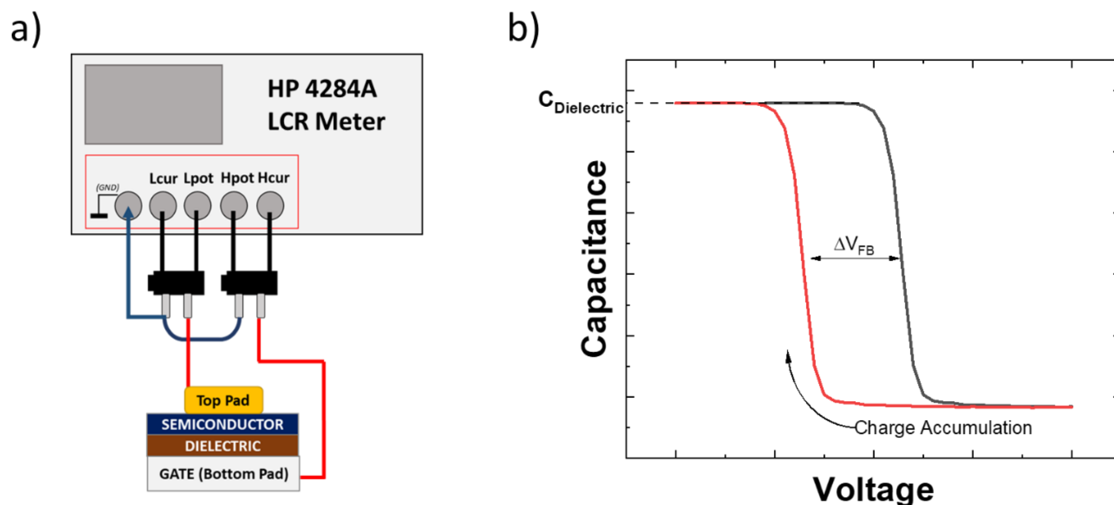

Figure 3.5. a) Diagram outlining the connections between the LCR meter and an MIS device. b) Example C-V characteristics for an MIS device.

During a C-V measurement of an MIM device, the measured capacitance should not vary greatly as the only layer being measured is the dielectric. For an MIS device, by sweeping the bias voltage, the capacitance changes from accumulation, depletion, and inversion of charges at the semiconductor-dielectric interface. Due to the long relaxation of the minority carriers, the inversion layer is not typically observed in organic MIS diodes. The accumulation capacitance is effectively the capacitance of the dielectric layer. This can be understood as considering the MIS to be comprised of two capacitors in series, one from the dielectric layer and the other from the semiconductor layer. In series, capacitances add inversely, resulting in lower total values the more devices you add. Once the semiconductor layer saturates, it no longer acts as a capacitor and the total capacitance of the MIS is only influenced by the dielectric layer. As such, if one wants to determine the capacitance of the dielectric layer from an MIS – either for determining thickness or the capacitance per unit area of the layer – then the value of capacitance must be taken from the saturation regime of the C-V curve.

C-V curves from MIS diodes also highlight properties at the semiconductor-dielectric interface. For a full set of characteristics, it is important to sweep the voltage both from a positive bias to a negative bias and the reverse, which comprises what is known as a hysteresis curve. During such a measurement, one may observe a shift between the onset of accumulation, also known as a flat band shift (ΔV_{FB}). This shift will sometimes indicate the presence of interfacial trap states between the two layers, which will be discussed more later on.

3.7 Operation and Characterization of Inverter Circuits

P-type and n-type FETs can be combined into a simple complementary logic architecture known as an inverter circuit. There are several reports of organic voltage inverters utilizing all organic p-type and n-type FETs [47-52]. The basic configuration is shown schematically in Figure 3.6 a). Here, the drain contact of the p-type FET (also known as the "pull-up" transistor in this circuit) is connected to the drain of the n-type FET (the "pull-down" transistor). The gates of both devices are connected to serve as the input node of the circuit and the connection between the devices' drain contacts act as the output node of the circuit. The source of the pull-up transistor is connected to the power supply (V_{DD}) and the source of the pull-down transistor is connected to ground. As the input bias at the connected gates (V_{in}) is swept from 0 to V_{DD}, the inverter switches between stable states in which only one device is operating, allowing for the steady states to act as logic "1" and "0". The sharpness of this transition determines how well the circuit can act as a logic device. To facilitate high noise-margins, the transition should occur at $V_{DD}/2$, which can be achieved when both transistors have similar currents. The point at which this transition occurs is known as the "trip point" and is defined as when the input voltage (V_{in}) is equal

to the output voltage (V_{out}) of the circuit. The power consumption of an inverter circuit comes only while the switching between states occurs.

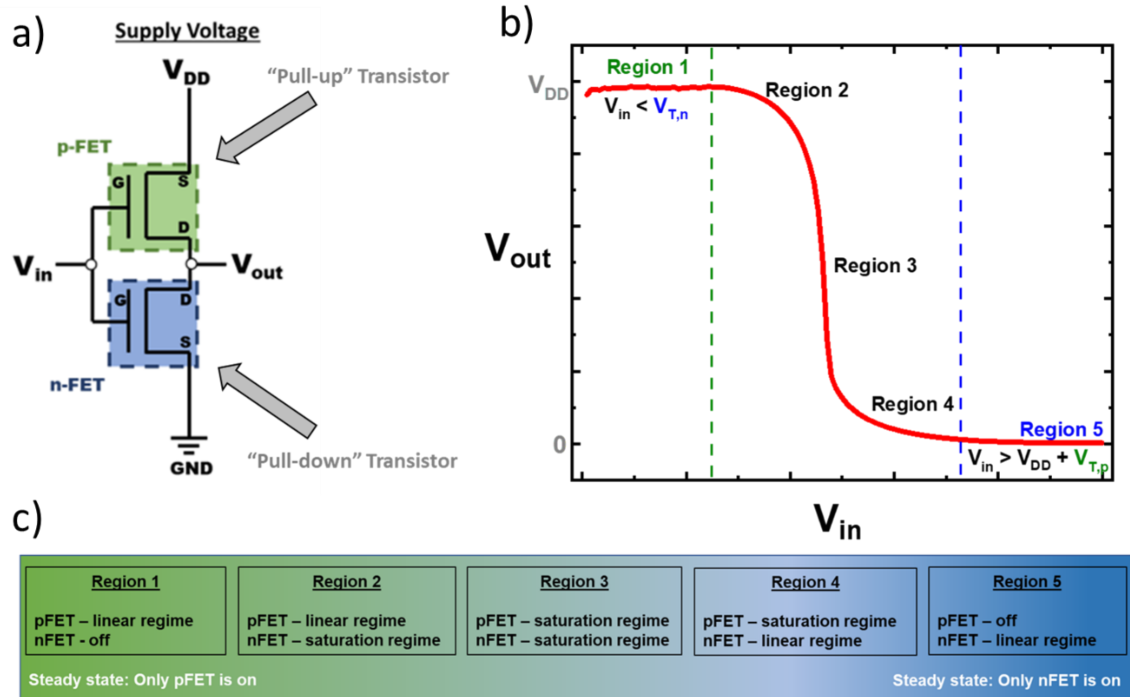

Figure 3.6. a) Diagram of how two complementary FETs is connected to form an inverter circuit. b) Example of the characteristics of how the output voltage measured for an inverter varies with input voltage. c) An outline of the state of each individual FET throughout the operation of the inverter.

To perform the measurement of the inverter devices, similar to the individual FET devices the Keithley 2400 and Keithley 236 source meters were used. An additional Keithley 2400 source meter was also employed for the purpose of establishing the source bias (V_{DD}). To distinguish between them, this sourcemeter will be referred to as Keithley 2400-EXT. Figure 3.7 a) shows the connections using the source meters to perform the inverter measurements. In this example, the inverter is formed by connecting two separate FET devices. Here, the Keithley 2400 applies a common V_{in} to the gate of each FET, the Keithley 2400-EXT applies V_{DD} to the source contact of the p-type (pull-up) FET, and the Keithley 236 measures V_{out} through a common connection between each of the device

drain contacts. Each of the sourcemeters share a common ground, which is connected to the source of the n-type (pull down) FET. As the supply voltage (V_{DD}) is increased step-by-step, the trip point and maximum V_{out} for each V_{in} sweep also increase. The (voltage) signal gain for the circuit is related to the rate of change of the output as the input voltage is swept ($\partial V_{out}/\partial V_{in}$). Because the most drastic change occurs at the trip point, the gain is expected to peak at this point.

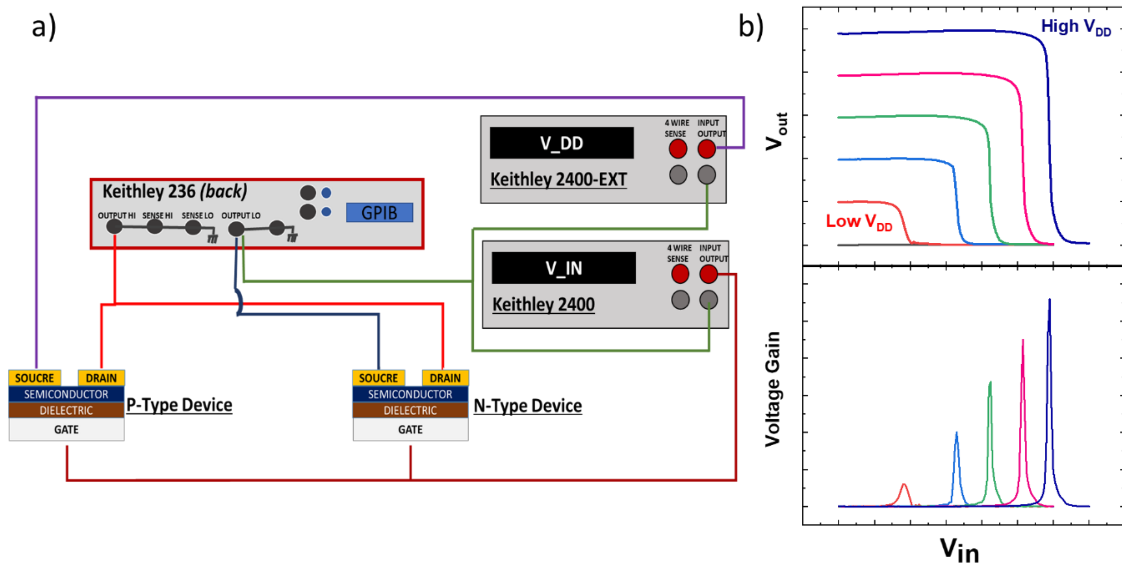

Figure 3.7. a) Connection between FETs to form complementary inverter. b) Example of a suite of inverter measurements for various V_{DD} and their associated signal gain.

3.8 Modeling Inverter Characteristics

Many of the organic FET simulations thus far have been conducted in SPICE (Simulation Program with Integrated Circuit Emphasis) using the MOSFET model, and other commercial circuit simulation software. As an alternative to SPICE, the open-source Python programming allows easy access to coding FET and other circuit characteristics. The output curves are evaluated in this work using two methods. Method 1 uses the basic

transistor equations with small modification for the sake of fitting where the drain-source current in the linear regime is given by [53,54]:

$$I_{DS} = -\frac{W}{L}\mu C_i\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \qquad (3.5)$$

In the saturation region, the drain-source current can be expressed by:

$$I_{DS} = -\frac{W}{2L}\mu C_i(V_{GS} - V_T)^2\left(1 - \lambda\big(V_{DS} - (V_{GS} - V_T)\big)\right) \quad (3.6)$$

where the parameter λ denotes the variation of the conductance with V_{DS} in the saturation region. Several of the transistor properties such as carrier mobility (μ), subthreshold swing (SS), and threshold voltage (V_T) may be obtained from the saturation region of the transfer characteristics as discussed in the previous section.

Method 2 is denoted as the unified model and parameter extraction method by Estrada et al. [55] where the drain current in the linear and saturation region is modelled together and given by:

$$I_{DS} = \frac{W}{L}C_i\frac{\mu(V_{GS} - V_T)}{\left(1 + R\frac{W}{L}C_i\mu(V_{GS} - V_T)\right)} \times \frac{V_{DS}(1 + \lambda V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{1/m}} + I_0 \quad (3.7)$$

In equation (3.7), the saturation voltage (V_{DSsat}) is defined by using another modulation parameter, α, V_{DSsat}=α(V_{GS}-V_T); R is the source and drain resistance, I_0 is the leakage current, and m is another fitting parameter which considers sharpness of the knee region. Here the gate-field dependence of μ is ignored.

An analytical model has been used by Bode et al. [47] for the five different regimes of operation of the FETs to predict the inverter output characteristics. Figure 3.5 b).

schematically shows the different regions of the direct current (DC) output characteristics of an inverter circuit with a p-type FET (green) and an n-type FET (blue) (Figure 3.5 a)). For low values of V_{in}, specifically while it is lower than the threshold of the n-type FET (V_{Tn}), V_{out} is at maximum and is equal to V_{DD}. In this region, the p-type FET is operational, and the n-type FET is off. Similarly, when the input voltage is high, the n-type FET is operational, and the p-type FET is off. Ideally, since only one of the FETs is on in the steady state, there is no static current or power dissipation.

Regions 2 – 4 may be outlined using an analytical model which relies on the current through the p-type FET and n-type FET being equal and opposite (I_{DSn}=-I_{DSp}). Using this condition to solve for relevant biases results in a cubic polynomial in regions 2 and 4. For details, see [47]. In region 3 both FETs are in saturation. The methods used for regions 2 and 4 are outlined below.

In region 2, when $V_{in} > V_{Tn}$ and while the n-type FET is in saturation and p-type FET is in the linear region, and in region 4, while the p-type FET is in saturation and the n-type FET is in the linear region, the output voltage has the form:

$$V_{out} = \delta_{2,i} V_{DD} + \sqrt{\frac{-p_i}{3}} \cos(\Theta_i) - \frac{a_i}{3} \qquad (3.8)$$

where

$$\Theta_i = \frac{\arctan\left(\frac{2}{-q_i}\sqrt{-\frac{q_i^2}{4} - \frac{p_i^3}{27}}\right) + n_i \pi}{3} \qquad (3.9)$$

$$p_i = b_i - \frac{a_i^3}{3} \qquad (3.10)$$

$$q_i = c_i + \frac{2a_i^3 - 9a_i b_i}{27} \tag{3.11}$$

Equations 3.8 - 3.11 are a result of solving the cubic polynomial from the equal and opposite condition of the drain-source current using the Cardano method [47]. In the above equations, *i* represents regions 2 or 4 and n_i is a phase factor which is related to the form of the cubic polynomial. The parameters, a_i, b_i, and c_i vary for the two regions and can be expressed in terms of V_{in}, V_{DD}, and other FET parameters. Channel width (*W)*, channel length (*L)*, carrier mobility, threshold voltage, the parameter, λ - which is found from Eqn. 3.5 or 3.6 – are all required to obtain the *a*, *b*, and *c* parameters [47] .

In Chapter 6, it will be explored how this model can be applied to experimental characteristics and how its modification can provide insight into device behavior.

Chapter 4: Ferroelectrics and Other Polymer Dielectrics in FETs

Polymeric high κ ferroelectric dielectrics are advantageous in lowering the operating voltage as well as enhancing the performance of organic FETs [56-59]. This chapter will outline devices employing the ferroelectric polymer polyvinylidene fluoride (PVDF) with trifluoroethylene (PVDF-TrFE) as the dielectric layer in capacitor and transistor devices. It will also explore the impact that other, non-ferroelectric dielectrics can have on the dielectric/semiconductor interface, and the other advantages that they present.

4.1 Physical Characteristics of Ferroelectrics

Ferroelectricity in insulators denotes a material which has differing polar characteristics depending on whether it lies above or below its Curie temperature (T_c). Below this temperature, the material is said to be pyroelectric, in which the primitive cell of the material's crystal lattice structure has a nonvanishing dipole moment [3]. This spontaneous polarization of the material allows for the dipole moments to be oriented and influenced by external electric fields. When the material is well below T_c, the distortion from the dipoles is stronger, and the polarization is difficult to reverse via external electric fields [3]. When the material is close to T_c; however, it is relatively easy to reorient the dipoles of the ferroelectric insulator, reflected in the material having a very high dielectric constant near this temperature [3]. When the material is above the Curie temperature, the crystal becomes non-pyroelectric and behaves as a paraelectric.

Ferroelectric materials have no center of symmetry, and the appearance of spontaneous polarization causes a strain, resulting in piezoelectric behavior. Ferroelectric behavior is

common in perovskite materials, such as $BaTiO_3$. The crystallinity of these perovskites has proven to be a key factor in influencing its ferroelectric characteristics. This too holds true for polymer ferroelectrics, which will be discussed later, where the net dipole moment arises from the backbone chain conformation of the molecule.

Ferroelectrics are desirable in FET devices, as their temperature-dependent dielectric constant and their polarization allow for parameters which can fine tune the charge transport behavior of these devices. Furthermore, solution-processable ferroelectric polymers are highly desirable for use with organic semiconductors, as their films can be fabricated with very low thicknesses. This reduction in thickness works in tandem with its high dielectric constant to facilitate charge accumulation. When forming a full picture of the charge transport in organic semiconductors while utilizing a polar dielectric, one must consider the influence of the long-range interactions between the charge carriers and optical phonons of the dielectric layer, known as Fröhlich polarons [17]. The dynamic coupling of the charge carriers to the electronic polarization at the semiconductor-dielectric interface results from an image force at the interface and from the Coulomb interaction of the charge carriers with the surface phonons of the dielectric. An immediate consequence of such an interaction is a decrease the carrier mobility, which can be understood on the basis of a renormalization of the transfer integral and an increase in the effective mass of the carriers [60]. The charge-dipole coupling broadens the density of states at the semiconductor-dielectric interface, increasing the localization of carriers. This inherently means that low-κ dielectrics in organic FETs achieve better performance compared to high-κ dielectrics.

When an external electric field is applied to a ferroelectric during the material's crystallization, the process is defined as *poling*. This process is performed near T_c – in other words, at the ferroelectric-paraelectric transition point – where the dipoles will be the most susceptible to reorientation. By varying the direction of the electric field relative to the surface of the material, one can similarly influence the direction of its polarization. As will be demonstrated later in this chapter, this poling process can act to alter the charge transport characteristics of organic FET devices.

4.2 Properties of PVDF and PVDF-TrFE

The discovery of the piezoelectric effect in polyvinylidene fluoride (PVDF) dates back several decades, and since then its structural and ferroelectric properties have been heavily investigated; however, research related to its application in organic electronic devices came much later [61-64]. PVDF and its copolymers such as PVDF trifluoroethylene (PVDF-TrFE) have played a crucial role in memory applications, wearable electronics, and sensors [65-78]. Figure 4.1 provides a snapshot of the numerous technological applications of PVDF and its copolymers, and Figure 4.2 d-f) outlines the structure of PVDF and its copolymer PVDF-TrFE. Applications in actuators and memory devices predominantly arise from its ferroelectric and piezoelectric properties. PVDF-based ferroelectrics have been hailed as an important group of materials for advancing the internet of things; in particular, they provide a viable path towards sustainable smart sensors [73]. Several applications exploit the piezoelectric nature of PVDF; for instance, energy harvesting materials or sensors which are incorporated in the human body. The memory applications, demonstrated via capacitors or transistors, exploit the ferroelectric properties of PVDF and its copolymers. In addition, due to its robust chemical resistance and high thermal stability,

PVDF is heavily used as membranes for gas separation and pollutant removal, although these applications are not explored in depth in this work. The metal-polymer interface in diode architectures and the thickness of the layer can impact switching times during endurance tests [78]. . PVDF-based films are not without disadvantages. The inherent dipolar disorder results in surface roughness which manifests itself as gate leakage currents, when used as a dielectric layer in FETs.

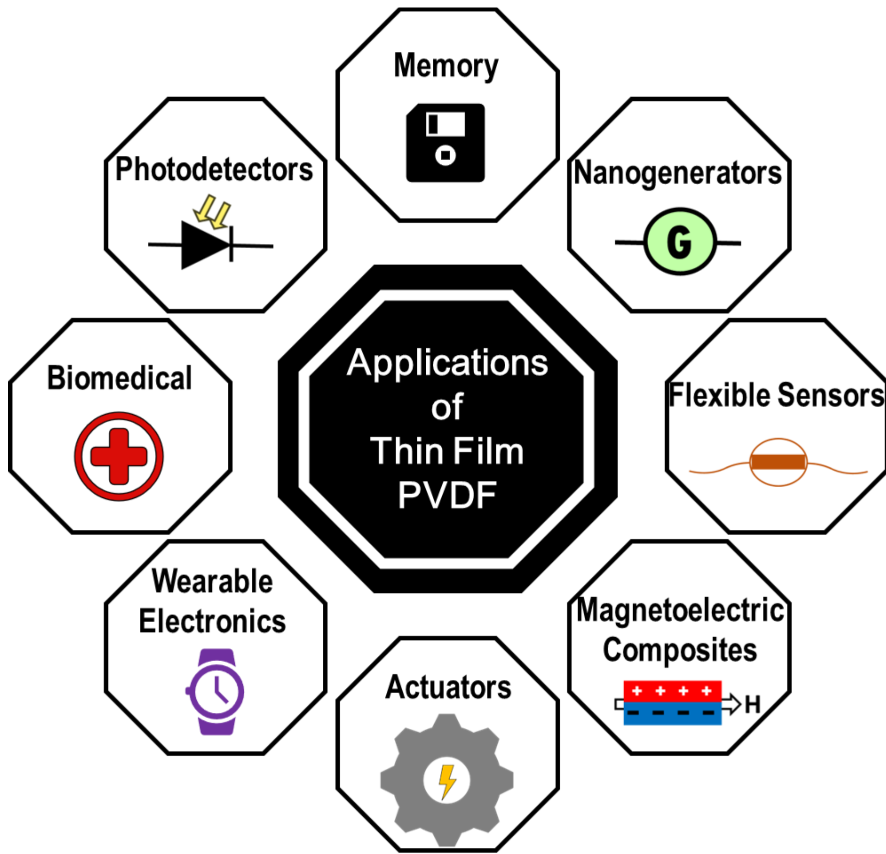

Figure 4.1. Applications of PVDF-based copolymers in thin film electronics.

PVDF is semicrystalline in nature and organizes into crystalline lamellae with folded chains interwoven within amorphous layers [63]. PVDF and its copolymers belong to a class of polymers with crystalline dipolar domains surrounded by a non-crystalline matrix, as schematically shown in Figure 4.2 a). X-ray diffraction (XRD) performed by various

research groups has confirmed that the ferroelectric phase originates from a field-induced orientation of the dipoles on the chains and not due to the orientation of the dipoles associated with the amorphous phase [62,79-84]. Application of the previously mentioned poling process acts to orient these dipoles, shown schematically in Figure 4.2 b-c), where they may be aligned either parallel or perpendicular to the film plane based on the chosen direction for the external electric field. It has previously been demonstrated using scanning electron microscopy (SEM) that the process of reorienting the dipoles via poling alters the surface morphology of films made using PVDF-TrFE, with the film showing clear domains > 1μm in size when poled [85].

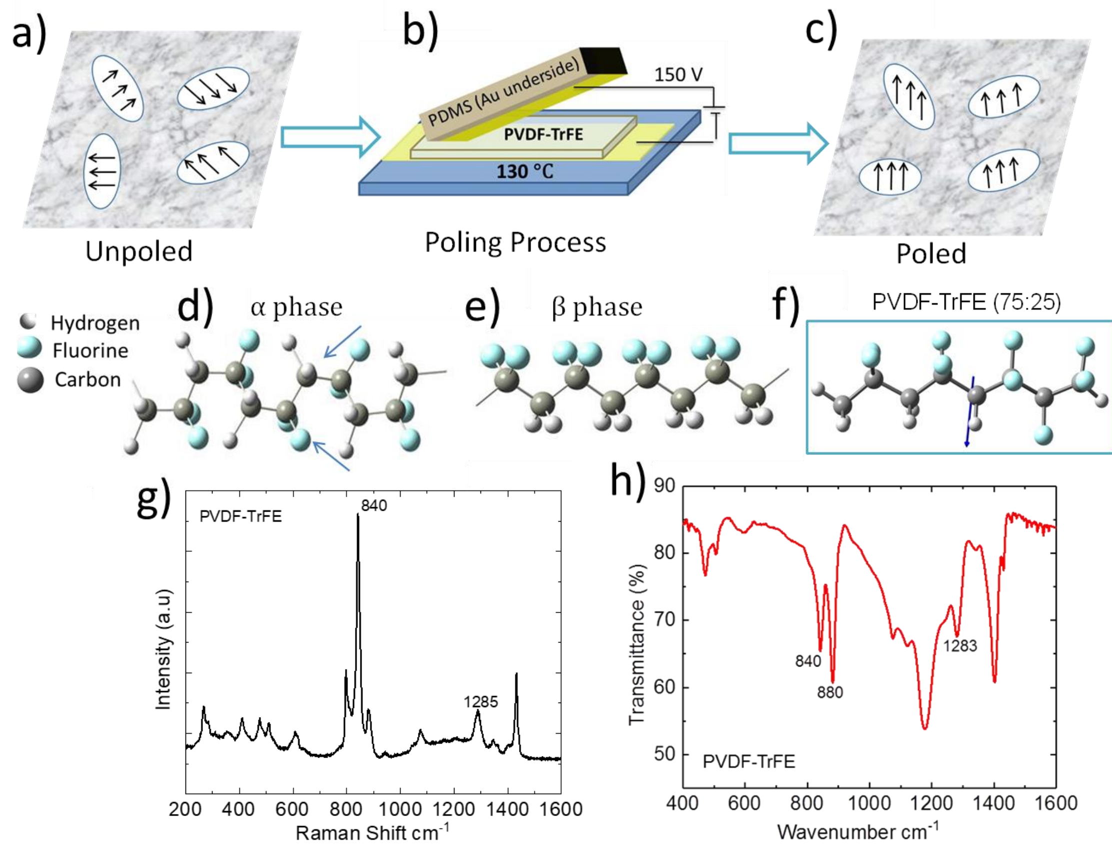

Figure 4.2. Chemical structure and spectroscopic fingerprint of PVDF. a) Schematic representation of unpoled PVDF-TrFE. It has crystalline domains with directed dipole moments in an amorphous matrix. b) Application of a vertical electric field, while heating the film just above the ferroelectric-paraelectric

transition temperature, results in an alignment of the net dipole moment in c). Schematic representation of d) α PVDF, e) β PVDF, and f) β PVDF-TrFE (75:25). g) Raman spectrum of PVDF-TrFE (75:25). h) FTIR spectrum of PVDF-TrFE (75:25). Adapted from my published work [86].

The net dipole moment in the PVDF molecule arises from its backbone chain conformation. At least four different phases have been identified. The two predominant phases are the paraelectric (α) phase and the ferroelectric (β) phase [64]. The α phase has a backbone conformation of alternating *trans-gauche* configuration ($TG^{+}TG^{-}$) and the β phase is the *all-trans* configuration (TTTT). These two phases are shown in Figure 4.2 d-e) with the arrows denoting the direction of the dipole moment. As seen for the α phase, the individual dipole moments cancel out due to the backbone conformation. The ferroelectricity of the β phase arises from the differences in electronegativity of hydrogen and fluorine atoms, giving rise to a dipole moment for each molecule in a direction perpendicular to the backbone. The γ phase has a chain conformation in between the α and β phases. The δ phase is a polar analog of the α phase, and its ferroelectric properties were experimentally determined a few years ago [87]. The additional fluorine atom in the TrFE monomer, shown in Figure 4.2 f), prevents the polymer from being in the *trans-gauche* α phase as long as the molecule is above 11% TrFE The copolymer used in this work is a 75:25 ratio PVDF-TrFE, which is most frequently used [88]. The competition between the short-range van der Waals interaction of the molecular dipoles and the long-range dipole-dipole interactions between the chains dictate the ferroelectric phenomenon in PVDF-TrFE. Unlike PVDF, the advantage of the copolymer PVDF-TrFE is that it is ferroelectric directly after casting the film. The β phase in PVDF-TrFE may be further enhanced by thermal annealing above the ferroelectric-paraelectric phase transition temperature. The 840 cm^{-1} vibrational peak in the Raman and FTIR spectra (Figure 4.2 g-h)) is assigned to the CF_2 group and appears only when the backbone is in the *all-trans* conformation. The

1285 cm^{-1} Raman peak is from the coupling of the CF_2 stretching and skeletal C-C stretching modes, and the 1400 cm^{-1} band in the FTIR spectrum is assigned to the CF_2 bending modes. In this way, the Raman and FTIR spectra from PVDF-TrFE confirm the backbone chain conformation, and thus the β phase. There are several other binary copolymers of PVDF, such as PVDF-HFP with hexafluoropropylene (HFP), PVDF-CTFE with chlorotrifluoroethylene (CTFE) and even ternary copolymers with PVDF-TrFE; however, none of these copolymers are further explored in this work.

When working with solution-processable polymers of any kind, the solvent plays a crucial role in the characteristics of the film which is formed. Knotts *et al*. performed a study on PVDF-TrFE capacitors where the ferroelectric dielectric was dissolved in solvents of various dipole moments (D) before casting the films [58]. The solvents employed included dimethyl sulfoxide (DMSO) (4.1 D), dimethyl formamide (DMF) (3.8 D), and 2-butanone (MEK) (2.7 D). The remnant polarization was found to be the largest for DMSO (5.6 $\mu C/m^2$) and the coercive field varies between 52 MV/m to 74 MV/m, the lower value being for MEK [58]. The capacitor where DMSO was used as the solvent showed a hysteresis in the displacement at the lowest field, indicating that there was some ordering of the dipoles even before the field is applied [58].The improved properties with high dipole moment solvents are believed to be due to an extended chain conformation in solution which is maintained after processing the films. The usage of high-D solvents in dissolving non-ferroelectric dielectrics has also been shown to be beneficial for improving device performance of organic diodes and FETs [89,90]. In many scenarios, the high dipole moment solvents further help in the processing of thin dielectric layer, which enhances the

stability of MIS diodes and FETs. In this work, based on the above cited study, DMF was chosen as the solvent for preparing the PVDF-TrFE solutions.

4.3 Electrical Poling of PVDF-TrFE

A study conducted by Laudari et al. shows that by reorienting the dipoles of PVDF-TrFE by 90º, a process referred to hereafter as “vertical poling” or “v-poling”, an enhancement of the charge carrier mobility and on/off ratio of the p-type organic molecule TIPS-pentacene is produced [43]. A lateral reorientation of the dipoles is also reported. Lateral poling near the semiconductor-dielectric interface has the disadvantage of invoking a substantial drain-source current even in the absence of a gate voltage due to the presence of a spontaneous parallel polarization field [43]. By carefully tuning the strength of the field in relation to the thickness of the dielectric layer, Laudari et al. report a combination of vertical poling the bulk of the PVDF-TrFE film while lateral-poling a thin region near the gate. This process is referred to hereafter as “texture-poling”, and was shown to further enhance the FET properties as well as help reduce the parasitic current [43]. The poling method employed for the devices in this work is based off of that study. Figure 4.3 below outlines the setup of each type of poling.

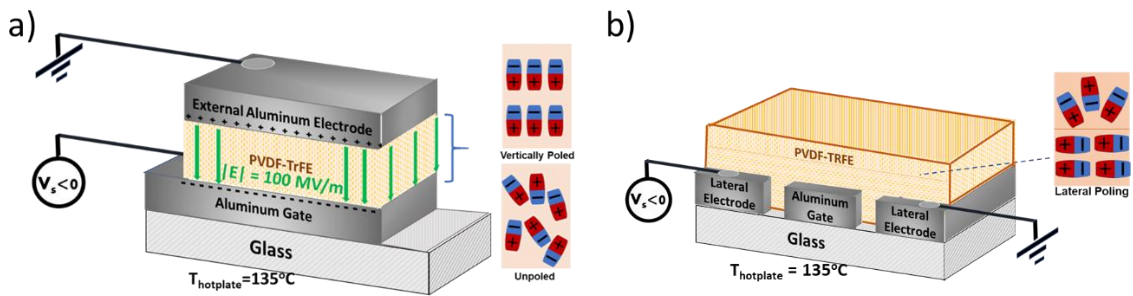

Figure 4.3. a) Setup for vertically poling PVDF-TrFE b) setup of laterally poling PVDF-TrFE. For textured poling, the process shown in b) would be performed immediately after that shown in a).

Fabrication and Poling of PVDF-TrFE Films

The PVDF-TrFE (75:25) copolymer was procured from Measurement Specialties Inc. and the solvent DMF was acquired from Sigma Aldrich. PVDF-TrFE was combined with DMF at a concentration of 50 mg/mL. This was allowed to stir at room temperature overnight (>12 hours). Under nitrogen atmosphere, the solution was spincoated onto a substrate with the already-evaporated Al gate. The solution was cast statically (to ensure uniformity) and then accelerated to reach a final spin speed of 1600 rpm for 60s. The substrate was then briefly annealed in a nitrogen atmosphere at 70°C for 10 minutes. This is done to ensure the majority of the solvent has been evaporated. The substrate was then placed on a hot plate in ambient atmosphere for poling.

For vertical poling, an electric field of 100 MV/m magnitude was applied between the gate and external contact with the orientation chosen such that the biases applied during FET operation would not act to reorient the dipoles. This poling was performed for 1 hour in total. During the first 30 minutes, the field was applied as the hotplate is allowed to heat up to (and then sit steadily at) 135°C. This temperature was chosen as it is near PVDF's Curie temperature and would allow for greater reorientation of the dipoles, as discussed earlier in this chapter. For the last 30 minutes, the substrate was allowed to cool back to room temperature, with the bias continuing to be applied to hold the reoriented dipoles in place during the cooling process.

For texture-poling of a sample, following the initial vertical poling a lateral field was applied between two extra contacts that were coplanar to the gate (see Figure 4.3 b)). Such contacts were evaporated onto the substrate at the same time as the gate electrode. The

magnitude of this lateral electric field was small (0.01 MV/m) to ensure that it only acts to reorient the dipoles in the region of the PVDF-TrFE film close to the gate. Because of this, the dipole orientation at the dielectric/semiconductor interface is expected to be the same as for vertical poling, and the direction of lateral poling should not influence the polarization at the interface. The lateral poling was performed for 30 minutes in total - 15 minutes to heat up and 15 minutes to cool down, with the field applied the entire time.

4.4 Fabrication and Characterization of DPP-DTT/PVDF-TrFE FETs

The poled PVDF-TrFE films were explored in this work as a means to enhance the charge transport in FET devices utilizing the donor-acceptor copolymer DPP-DTT as a p-type semiconductor. 75 μL of the DPP-DTT solution - made using equal parts chloroform and 1,2 dichlorobenzene (DCB) as the solvent - was dynamically spincoated on top of the existing PVDF-TrFE layer at 900 rpm for 60 seconds under nitrogen atmosphere. The DPP-DTT film was restricted to a small channel during spincoating by applying Teflon tape. After removing the Teflon tape, the film was annealed at 100°C for an hour and a half under nitrogen atmosphere. DPP-DTT can be annealed at higher temperatures; however, the temperature was chosen such that it would sit well below the ferroelectric/paraelectric transistor temperature so that heating the substrate would not risk reorienting the dipoles in the PVDF-TrFE film. 50 nm gold electrodes were thermally evaporated onto the substrates using a patterning mask to act as the source and drain contacts. A given substrate would have four devices, each with a channel width of 1000 μm and varying channel lengths (50 μm, 75 μm, 100 μm, and 125 μm).

Figure 4.4 a-b) shows the transfer characteristics from two DPP-DTT/PVDF-TrFE FETs. In one case, the PVDF-TrFE film was vertically-poled and in the other case the dielectric layer was texture-poled. The carrier mobility, which was extracted in the saturation region, was observed to be an order of magnitude higher for the texture-poled device compared to the vertical-poled device. Similar behavior was observed previously as part of research into PVDF-TrFE FETs utilizing TIPS-pentacene as the semiconductor [59], where the texture-poled FETs showed $\mu > 1$ cm^2/Vs without changing the processing condition for TIPS-pentacene; the vertically-poled TIPS-pentacene FETs show almost an order of magnitude smaller carrier mobilities. Since the bottom region of the PVDF-TrFE layer (the region near the gate electrode) has a lateral orientation of the dipole moment in textured-poled devices, the parasitic leakage current and its dependence on the voltage is further reduced. It should be noted that in both vertical-poled and textured-poled dielectrics the dipoles are oriented in a similar fashion at the semiconductor-dielectric interface.

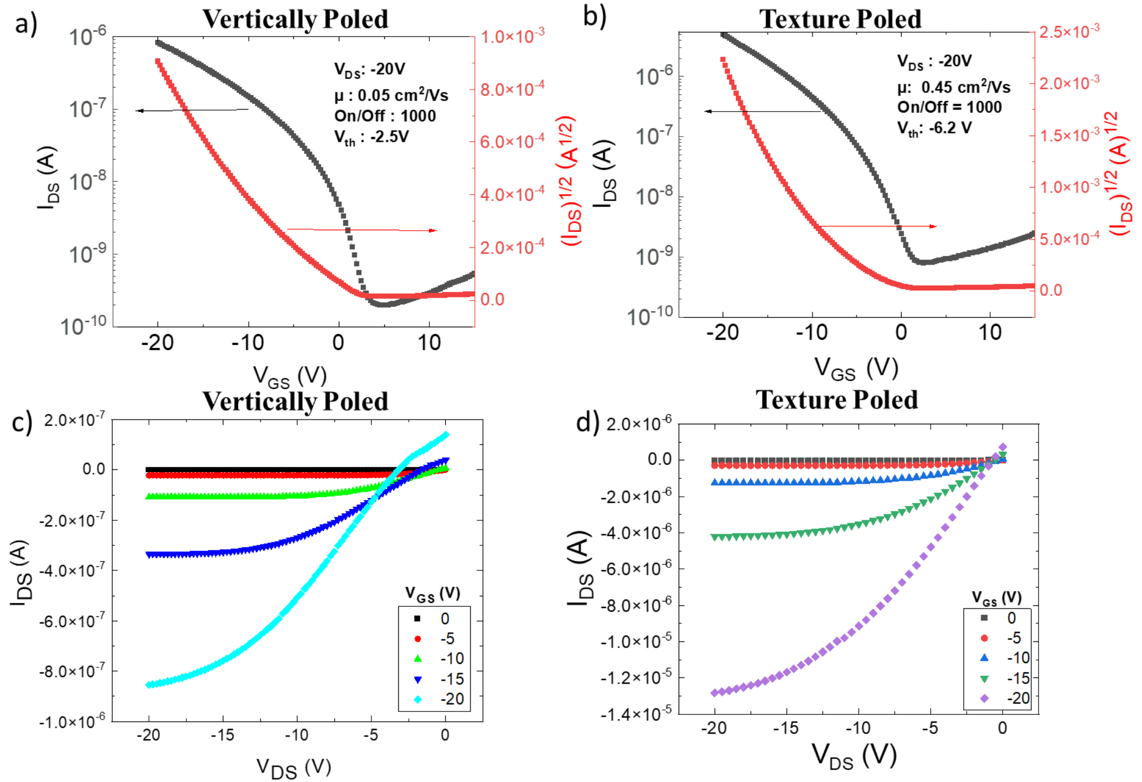

Figure 4.4. Transfer characteristics from a DPP-DTT FET device fabricated on a) vertically poled PVDF-TrFE and b) texture-poled PVDF-TrFE. Output characteristics from a DPP-DTT FET fabricated on c) vertically poled PVDF-TrFE and d) texture poled PVDF-TrFE.

The threshold voltages for the vertical-poled and texture-poled DPP-DTT FETs were -2.5 V and -6.2 V, respectively. Although the carrier mobility is higher for the texture-poled FET, the off-current was seen to be higher compared to the vertical-poled device. This could be an issue with texture-poled devices, especially if the lateral poling from the bottom is too high. If the lateral field during poling penetrates too deep into the PVDF-TrFE layer from the bottom, there is the possibility that the PVDF-TrFE domains are aligned in the lateral direction close to the semiconductor interface, resulting in a spontaneous parallel field and thus an enhancement of the off-current. The output characteristics of the vertical-poled device (Figure 4.4 c)) demonstrated non-zero current when V_{DS} = 0 V, with this current on the same order of magnitude as the saturation current. This can be a sign of parasitic (leakage) current in the device, and it was noticeably not present in the texture-

poled device (Figure 4.4 d)). This indicates that the texture-poling acted to reduce the influences of the parasitic current between the gate and source/drain contacts.

As it was demonstrated in these devices and those previously reported for TIPS-Pentacene [43], the poling condition of the ferroelectric dielectric plays a significant role in improving transport properties in organic FETs. Further, the higher κ value of ferroelectric dielectrics compared to other non-ferroelectric polymer dielectrics or oxide dielectrics such as SiO_2 allowed these DPP-DTT FETs to operate at low voltages.

It is important to note here that although DPP-DTT is reported to be ambipolar when utilizing Au as the source/drain material, only p-type behavior was observed in these devices, with the n-type behavior effectively removed. This could likely be due to trapping of electrons at the DPP-DTT / PVDF-TrFE interface. To make the move from simple FET architectures to more complex logic, it is important to develop devices that have electron transport comparable to the hole transport of the organic p-type devices. The next section will focus on one such material explored for this purpose.

4.5 Using CYTOP for Organic FET Devices

This section and those which follow seek to outline some of the other popular polymer dielectrics that are focused on in this work, specifically CYTOP, polymethyl methacrylate (PMMA), and poly (4-vinyl phenol) (PVP). Compared to oxides and other inorganic dielectrics, organic polymer dielectrics offer freedom of architecture, being useful in both top-gate and bottom-gate structures, while also being applicable to flexible substrates [35,91,92]. Here, the focus will lie on their general physical characteristics, film fabrication methods, and some examples of ways they have been used in FET devices, with each material receiving more attention in later chapters as well.

CYTOP™ is a transparent organic fluoropolymer with a low dielectric constant ($\kappa \approx 2.0$) [92]. Owing to its low dielectric constant, CYTOP-based devices will still require large biases to properly accumulate charges in organic systems. This polymer will usually be used for top-gate architectures in FET devices, as its highly hydrophobic nature can make it difficult to solution cast semiconducting films on top of. In this way, CYTOP will also be used as a means to encapsulate organic semiconductors from ambient atmosphere, removing some environmental impacts on device performance. Using CYTOP as a dielectric for bottom-gate architectures is not unheard of. Kalb et al demonstrated devices with such architectures using single-crystal rubrene and pentacene grown via physical vapor transport [92]. Interestingly, for these devices they observe essentially no interfacial defects for holes, which they attribute to its hydrophobic nature [92]. For the devices considered in this work, which are usually formed using a solution casting method, CYTOP is used exclusively in TGBC architectures.

The precursors for making CYTOP solution, CTL-809M and CT-solv-180, were obtained from AGC Chemicals Americas. The solution was made by mixing 200 μL of CTL-809M with 150 μL of CT-solv-180. To form the dielectric layer, the CYTOP solution was spincoated at 2000 RPM for 60s, casting 40μL of solution statically and subsequently dynamically casting 100μL of solution as the substrate accelerated to its final rotational speed. The film was then annealed at 140°C for 1.5 hours resulting in a film that was around 280 nm thick.

Figure 4.5 below demonstrates characteristics of a TGBC device made using DPP-DTT as the semiconductor and CYTOP as the dielectric layer. It is worth noting that for this device, a monolayer of PFBT (as discussed in Chapter 3) was applied to the gold contacts

to improve hole transport. The resulting device shows good on/off characteristics and a mobility which is on the same order of magnitude as the vertically-poled DPP-DTT/PVDF-TrFE device previously discussed; however, its threshold voltage is almost five times as high, likely due to CYTOP's lower dielectric constant.

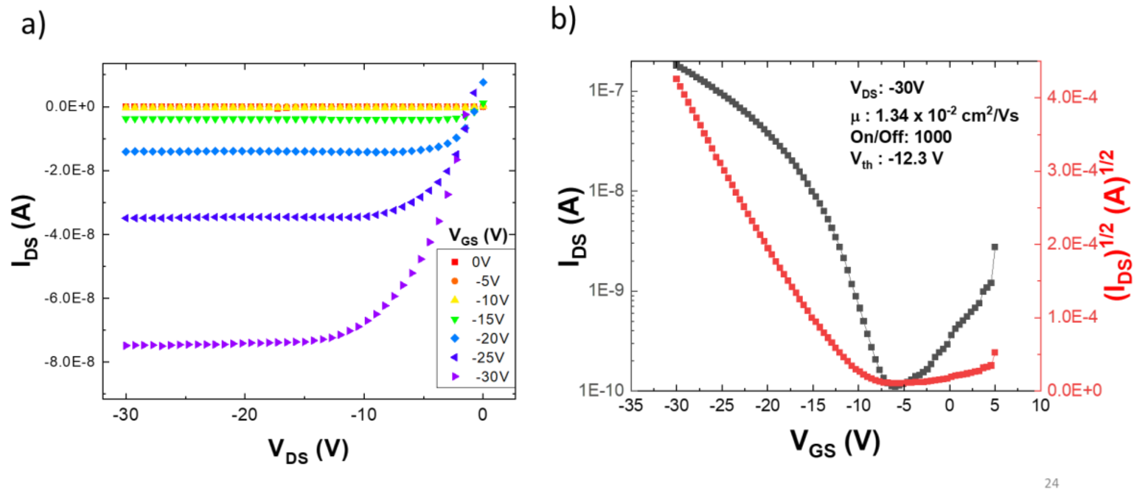

Figure 4.5. a) Output and b) transfer characteristics for FET made using DPP-DTT and CYTOP.

The use of CYTOP in TGBC architectures for FET devices will be discussed further in Chapter 5 where other donor-acceptor polymers are explored. The impact of PFBT and PEIE on the performance of DPP-DTT FETs will be explored further in the following section.

4.6 Using PMMA for Organic FET Devices - Influence of Contact Modification

Polymethyl methacrylate (PMMA) features a slightly higher dielectric constant ($\kappa \approx$ 3.5) compared to CYTOP and is also a favorable organic polymer used often in TGBC architectures for FET devices [35,91]. The PMMA and dimethyl sulfoxide (DMSO) used for making the solution were obtained from Sigma Aldrich. The solution was made at a

concentration of 60 mg/mL, which was then heated at 80°C and magnetically stirred for 45 minutes. It was further allowed to stir overnight off heat. The thin film was formed via spincoating at 5000 RPM for 60s, with 100μL being cast dynamically as the substrate began to accelerate. The PMMA film was then annealed at 100°C for 20 minutes, resulting in a film about 140 nm thick.

Like CYTOP, FET devices were fabricated using PMMA as the dielectric layer in a TGBC architecture. Figure 4.6 shows the output and transfer characteristics of such a device. What is interesting here is that unlike the DPP-DTT/PVDF-TrFE devices which were exclusively p-type, in the DPP-DTT/PMMA devices ambipolar behavior was observed, likely due to less electron trap states at the semiconductor-dielectric interface.

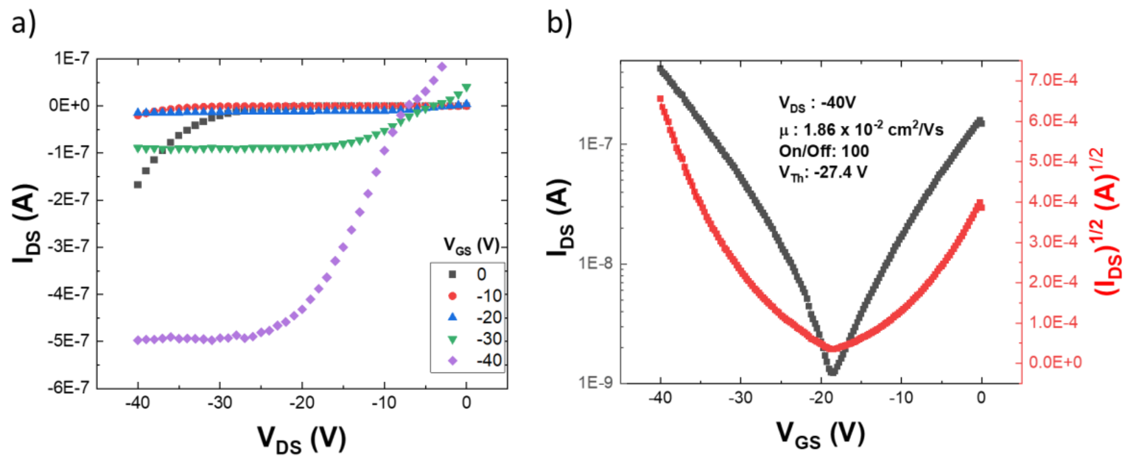

Figure 4.6. a) Output and b) transfer characteristics for a DPP-DTT FET made using PMMA.

Because the DPP-DTT/PMMA devices demonstrate ambipolarity, they presented an ample opportunity to compare the influence of self-assembled monolayers (previously discussed in Chapter 3) on tuning the work function of gold towards enhancing either hole or electron charge injection. Towards this end, three separate DPP-DTT/PMMA devices were fabricated: one which was plasma treated, one with a PFBT monolayer, and one with

a PEIE monolayer. Figure 4.7 shows a comparison of the output characteristics of each of these devices swept with both negative biases (p-type) and positive biases (n-type). For the device with plasma-treated Au contacts (black curves in Figure 4.7), the device shows ambipolar behavior with slightly higher saturation currents for hole transport compared to electron transport. For the device with PEIE-treated Au contacts (red curves in Figure 4.7), the device showed a clear preference for electron transport, suggesting a shift in the work function of gold closer to the LUMO level of DPP-DTT. Similarly, the device with PFBT-treated Au contacts (blue curves in Figure 4.7) showed a clear preference for hole transport, suggesting a shift in the work function of gold closer to the HOMO level of DPP-DTT.

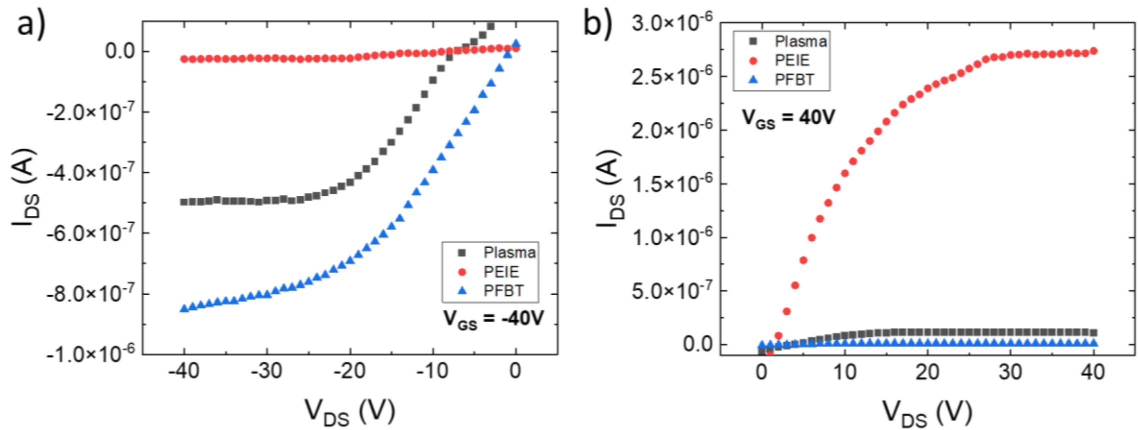

Figure 4.7. Comparison of output characteristics for various DPP-DTT/PMMA devices with differing treatment of the Au source/drain contacts. a) Comparison of hole transport and b) comparison of electron transport.

From the transfer characterization of these devices, the influence of the contact treatment on device performance was further demonstrated. Table 4-1 outlines the mobility, on/off ratio, and threshold voltage for both p-type and n-type operation. After a PEIE treatment was performed, the hole mobility dropped by one order of magnitude whereas the electron mobility was seen to increase by one order of magnitude compared to

contacts only cleaned with oxygen plasma. Conversely, when a PFBT treatment was performed, the hole mobility was seen to increase slightly whereas the electron mobility decreased slightly compared to plasma-treated contacts. The on/off ratio and threshold voltages were also observed to shift accordingly.

Table 4-1.FET characteristics for DPP-DTT/PMMA devices.

	μ_{hole}(cm^2/Vs)	On/Off	V_{Th} (V)	$\mu_{electron}$(cm^2/Vs)	On/Off	V_{Th} (V)
Plasma	1.86×10^{-2}	100	-27.4	4.78×10^{-3}	10	28.5
PEIE	1.48×10^{-3}	1	-31.3	3.96×10^{-2}	100	18.5
PFBT	4.18×10^{-2}	100000	-24.1	1.25×10^{-3}	1	24.5

The application of SAMs provides a useful tool by which to enhance or prevent charge transport. In the case of ambipolar materials, it allows the tuning of hole and electron transports such that one could effectively select which will dominate device behavior. In the next chapter, the application of PMMA as a polymer dielectric will be further explored.

4.7 PVP as a Dielectric for Small Molecule-Based FETs

Poly (4-vinyl phenol) (PVP) is another organic polymer commonly used as the dielectric layer for organic FET systems. The dielectric constant of PVP varies somewhat in the literature; however, a value of $\kappa = 3.9$ is used in this work [91,93]. One drawback to PVP is that it features a high number of hydroxyl (-OH) groups, which can lead to charge trapping and result in a noticeable hysteresis in device characteristics [94,95]. A common way to combat this issue is to perform crosslinking of PVP using poly(melamine-co-formaldedyde) (PMMF, aka PMF or MMF). The crosslinking of the polymer with PMMF reduces the influence of the hydroxyl groups on charge transport in the semiconducting channel and improves device performance [94]. For the devices considered in this work, crosslinked PVP is used in the formation of BGTC architectures.

The poly(4-vinylphenol) (PVP) (M_w= 25,000) and crosslinking agent poly(melamine-co-formaldedyde) (PMMF) (84 wt% in 1-butanol) were purchased along with solvents propylene glycol monomethyl ether acetate (PGMEA) and N,N-dimethylformamide (DMF) from Sigma Aldrich. A stock solution of 5wt% PVP + 2.5wt% PMMF was heated at 80° C for 1 hour and stirred overnight. PGMEA was generally used as the solvent; however, in some cases, such as those that will be expanded on in Chapter 7, DMF was used in its stead so as to facilitate better incorporation of other materials dissolved in a common solvent. If a thinner film of crosslinked PVP (cPVP) was desired, the stock solution was diluted to a lower concentration. To form the film, the solution was spincoated onto the substrate at 5000 RPM for 60 seconds and then annealed at 120°C for 1 hour to facilitate crosslinking.

TIPS-Pentacene FETs were made in a BGTC architecture using cPVP as the dielectric layer. The cPVP solution was made at an 80mg/mL concentration, resulting in a film which was around 90nm thick with a capacitance per unit area of 40 nF/cm^2. The TIPS-Pentacene solution (2 mg/mL in toluene) was dropcast at an angle (as discussed in Chapter 3) to allow for thin, ribbon-like crystals to form connecting the source and drain contacts. The electrical characteristics of such a device are demonstrated below in Figure 4.8. These devices demonstrated strong field effect mobilities, on the order of 0.1 cm^2/Vs, at low voltages (< 10V) with distinct “on” and “off” regions.

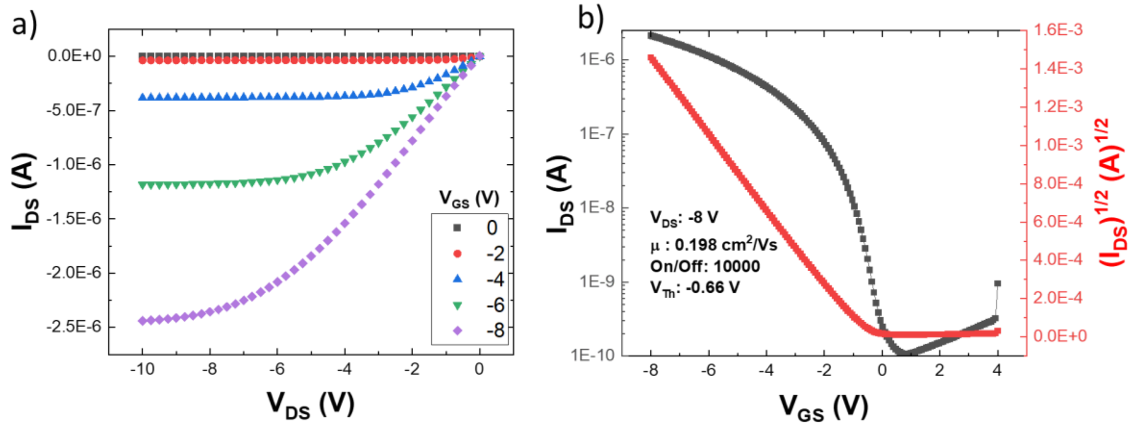

Figure 4.8. a) Output and b) transfer characteristics of a BGTC FET made using TIPS-Pentacene and cPVP.

Another interesting way that cPVP can be used is as a bilayer with another dielectric, specifically PVDF-TrFE. By depositing a thin layer of cPVP on top of PVDF-TrFE, a bilayer can be formed which benefits from the dipole-aligning poling from the ferroelectric PVDF-TrFe while the cPVP acts to modify the surface for the dropcasting of TIPS-Pentacene (which is sensitive to rough surface morphology). To form this bilayer, the cPVP solution was diluted to a concentration of 20 mg/mL, which resulted in a film that was around 20nm thick. This film was formed on top of a vertical-poled PVDF-TrFE film which was around 150nm thick. Together, the bilayer had a capacitance per unit area of 28.4 nF/cm^2. Despite PVDF-TrFE having a much higher dielectric constant than cPVP, the bilayer film has a much lower capacitance overall. This is due firstly to the fact that, as previously discussed for the MIS structures, a bilayer film will act two capacitors in series. Secondly, the bilayer film is also thicker (at around 170nm total) than the pure cPVP film (which was around 90nm thick). Figure 4.9 shows a comparison of transfer characteristics of a device utilizing this bilayer compared to the device shown in Figure 4.8. Because the capacitance per unit area of the bilayer film was smaller than that of the pure cPVP film, one would expect for the device to perform worse; however, the bilayer film demonstrated

a slightly higher on/off ratio as well as a higher mobility compared to the pure cPVP film. This suggests that the dipole alignment of the PVDF-TrFE layer facilitated charge accumulation at the interface.

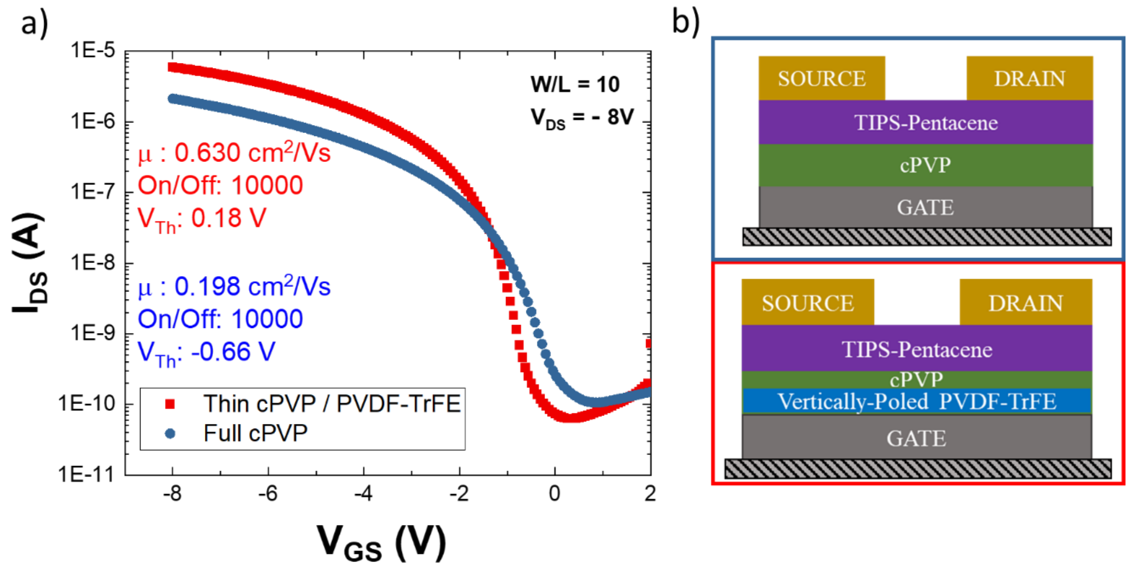

Figure 4.9. a) Transfer for a TIPS-Pentacene device made using cPVP compared to one made using a bilayer of cPVP / PVDF-TrFE. b) Diagram outlining the structure of each device.

Each of the polymer dielectrics discussed thus far (both ferroelectric and non-ferroelectric) have demonstrated excellent potential for building p-type FET devices.. Despite DPP-DTT's ambipolarity, without any extra modification of the contacts it still favors p-type behavior over n-type, especially when using PVDF-TrFE as the dielectric. The next chapter will focus on another donor-acceptor material, isoindigo, towards the realization of n-type FET devices.

Chapter 5: Copolymers for N-type Semiconductors

Through collaboration with a group in the Department of Chemistry of the University of Texas A&M at Qatar, thiazole-flanked fluorinated isoindigo (IID) samples were fabricated and incorporated into FET architectures whose performance will be explored within this chapter.

5.1 Modification of Isoindigo (IID)

An approach for tuning the HOMO-LUMO gap of isoindigo with facilitating solid state interactions is to replace the sulfur (S) atom in the five-membered ring with heavier atoms such as selenium (Se) or tellurium (Te) [96,97]. The size of the heteroatom dictates both the solubility and the size of the optical bandgap. Replacing S with Se in IIDs has been seen to favorably enhance charge transport properties in FETs [98]. Fluorination of D-A moieties has been another strategy for improving the ambipolar nature of charge transport by lowering the LUMO level. Not only does fluorination enhance crystallinity, it promotes molecular orbital hybridization between the monomer units, resulting in planarization of the backbone [99]. Fluorinated benzothiadiazole based conjugated systems were shown to enhance the degree of coplanarity, leading to improved charge transport properties [32,100]. Fluorinated IID polymers in FETs have shown electron mobilities upwards of 0.5 cm^2/Vs while maintaining a high hole mobility under ambient conditions [27]. Fluorination may also be exploited to enhance the dipole moment of the system for nonlinear optical properties, which can be utilized for visualizing transport in FETs [101].

Dr. Salahuddin Attar, working with Dr. Mohammed Al-Hashimi at the University of Texas A&M at Qatar, synthesized thiazole flanked fluorinated isoindigo copolymers with

thiophene (referred hereafter as IID-T) and selenophene (referred hereafter as IID-Se) units. This chapter explores utilizing these materials in different FET geometries. The discussion of the materials' structure and properties will not be fully exhaustive here, and for more information surrounding the fabrication process, the reader is referred to Ref [102].

5.2 Physical Properties of the Thiazole-Flanked IID

Following synthesis, each of the polymers possessed adequate solubility in chlorinated solvents such as chloroform and chlorobenzene. Gel permeation chromatography was utilized to determine the number-average molecular weight (M_n) of each material, which were found to be 90 and 29 kDa for IID-T and IID-Se, respectively. The HOMO / LUMO levels for IID-T and IID-Se were found to be -5.70eV / -3.84eV and -5.56eV / -3.74 eV, respectively, which are outlined in Figure 5.1 below. Based on these values, gold was chosen as the metal to be used for the source/drain contacts in FET architectures.

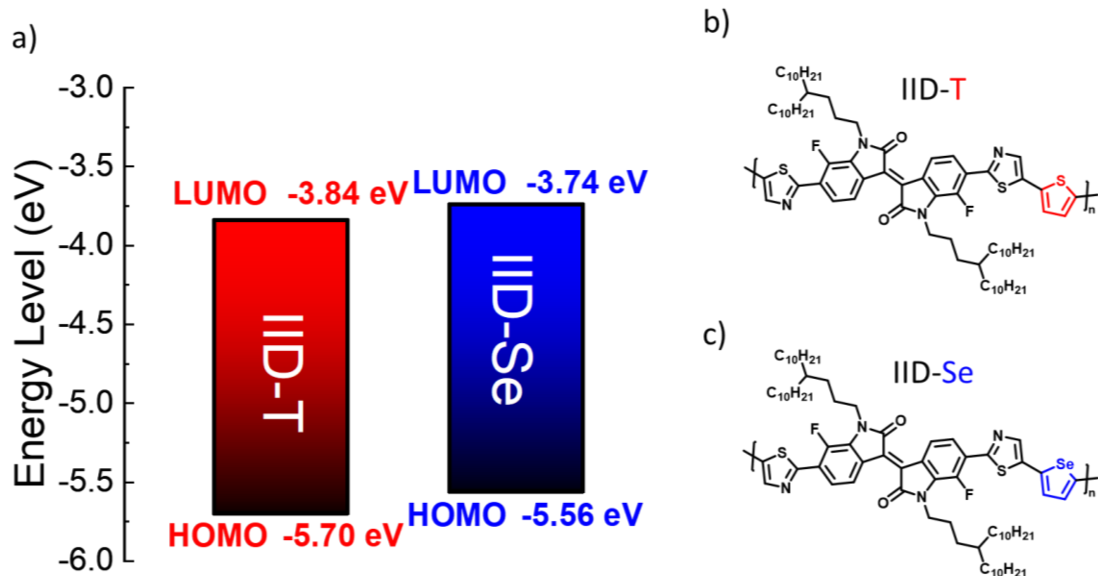

Figure 5.1. a) Energy level diagram of IID-T and IID-Se. b-c) Chemical structures of IID-T and IID-Se, respectively. The chemical structures were adapted from my published work [102].

5.3 Fabrication of IID Devices

The FETs were fabricated using both types of staggered structures discussed in Chapter 3. The first set of devices utilized the BGTC architecture, utilizing silicon substrates. Several other recent works which explored IID polymers in FET devices have made use of TGBC architectures [27,30,103,104] owing to the ability of the dielectric layer to encapsulate the material from atmospheric influences.

To realize the BGTC devices, the substrates were cleaned with an organic method and treated to administer an OTS self-assembled monolayer to alter its surface energy and improve film formation. From there the IID-T or IID-Se solution was spincoated to form the semiconducting film, followed by the application of the gold source and drain contacts via thermal evaporation.

The TGBC architectures were made using glass as the substrate. Gold source and drain contacts were evaporated onto the glass substrates following the organic cleaning process. After the solution was spincoated to form the semiconducting film, either CYTOP or PMMA were spincoated as the dielectric films. Finally, an aluminum gate was formed using thermal evaporation. To reduce parasitic currents through the dielectric, a mask was used to pattern the aluminum into a 500μm-wide channel.

For the initial set of FETs (those made on silicon), copolymers IID-T and IID-Se were dissolved in equal parts of chloroform and 1,2 dichlorobenzene (DCB) at a 5 mg/mL concentration. The solution was heated for several hours on a hotplate and allowed to stir overnight without heat. The solutions were then filtered through a 0.45μm PTFE filter. The IID-Se copolymer was observed to dissolve better than IID-T and retain most of its volume following filtration. In the TGBC device, to improve the dissolution of the polymers in the solvent and film formation, 1,2 dichlorobenzene was used by itself as the solvent to allow for heating the solution at higher temperatures for the other CYTOP and PMMA devices. The other aspects of the solution (concentration and filtering) were kept the same.

The semiconductor films were formed by spincoating at 1500 RPM for 40s, with 75μL of the solution being dynamically cast onto the substrate as it accelerated to its final speed. For the TGBC architecture, the films were restricted to a thin channel by using Teflon tape. The films were then annealed at 180°C for 10 mins. For the BGTC architecture devices, gold contacts were then thermally evaporated onto the film using a patterning mask to produce many devices with varying W/L ratios. Spincoating and annealing of the semiconductor films were carried out in a glove box under a nitrogen atmosphere.

The application of the dielectric polymers is as described in Chapter 4. When using either CYTOP or PMMA films as the dielectric layer, both were also patterned into a thin channel using Teflon tape while spin coating. Spin coating and annealing of the dielectric films were carried out in a glove box under a nitrogen atmosphere.

5.4 Performance of IID-T & IID-Se Devices

All electrical measurements were performed under ambient conditions. For the BGTC architecture devices in which the semiconductor is exposed to atmosphere, a flow of nitrogen gas was applied over the device during measurement to reduce the influence of oxygen on deteriorating the channel. For the TGBC architecture devices, the CYTOP or PMMA acted to encapsulate the semiconductor, removing any influence from the atmosphere on the channel.

In the BGTC architecture (using SiO_2 as the dielectric), both IID-T and IID-Se exhibited ambipolar behavior. Comparing their performance (Figure 5.2), IID-T demonstrated p-type and n-type behavior with average mobilities of 1.6 x 10^{-6} cm^2/Vs and 1.2 x 10^{-6} cm^2/Vs, respectively. In contrast, IID-Se showed a clear preference towards n-type behavior with an average mobility of 1.2 x 10^{-4} cm^2/Vs, which is almost two orders of magnitude higher than its average p-type mobility of 7.6 x 10^{-6} cm^2/Vs. As seen below, the top-gate architecture devices show futher improved FET performance.

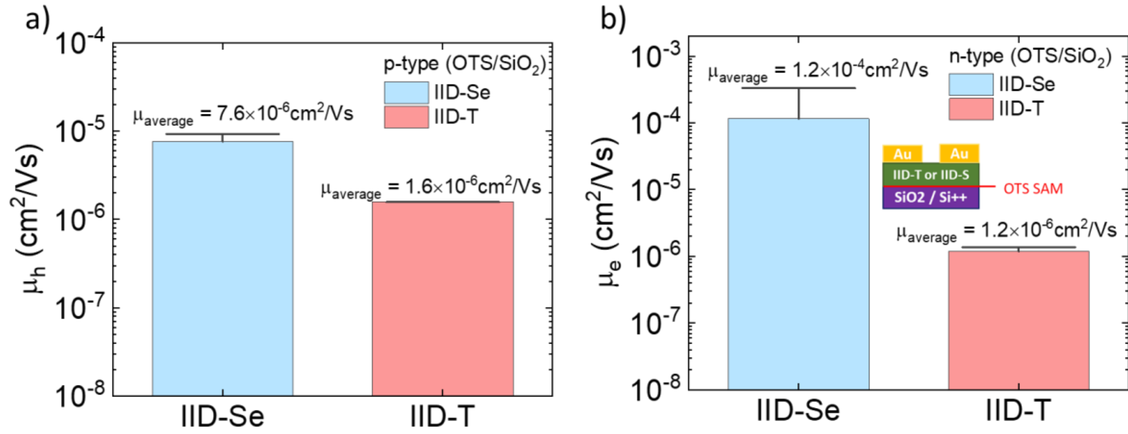

Figure 5.2. a) The average hole carrier mobilities extracted from the saturation region of IID-T and IID-Se based FETs. b) Average electron carrier mobilities extracted from the saturation region of IID-T and IID-Se based FETs. Inset of b) outlines the staggered device structure. The average carrier mobilities are obtained from 5-10 devices. Adapted from my published work [102].

CYTOP was initially used as the dielectric in fabricating the TGBC devices; the general architecture is shown in Figure 5.3 a). IID-Se demonstrated exclusively n-type behavior in the TGBC architectures. Figure 5.4 a) and b) demonstrate the transfer characteristics for IID-T and IID-Se FETs, respectively. IID-T in this architecture signaled a weak ambipolar nature; however, as shown in Figure 5.5, the leakage current was high with CYTOP as the dielectric. The average mobility and on/off ratio for the IID-Se devices were an order of magnitude higher than that of the IID-T devices, while both sets of devices had comparable threshold voltage values. A histogram of mobilities from IID-Se FETs is shown in Figure 5.3 b) with an average electron mobility of 1.1×10^{-2} cm^2/Vs. For IID-T, the average electron mobility across devices made using CYTOP was 7.3 x 10^{-3} cm^2/Vs.

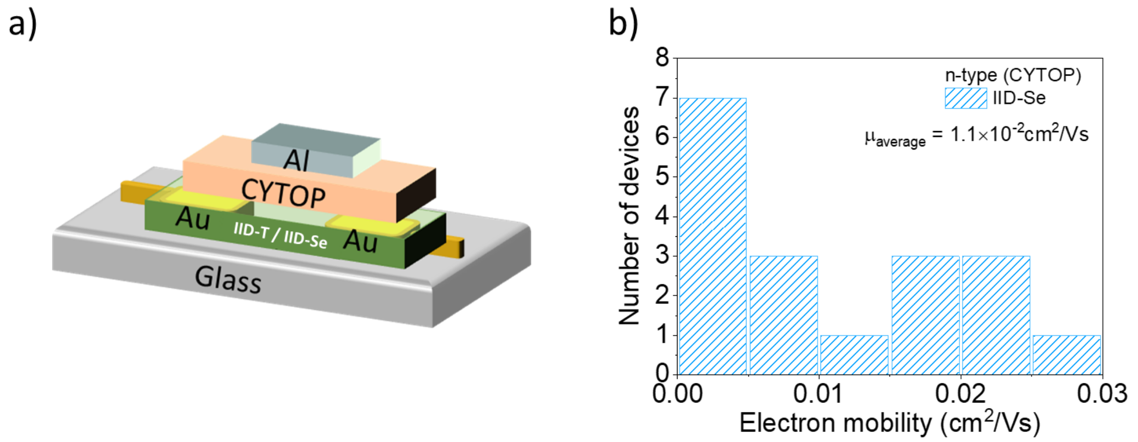

Figure 5.3. a) Schematic of the device architecture. b) Histogram of electron mobilities from top-gate IID-Se FETs. Adapted from my published work [102].

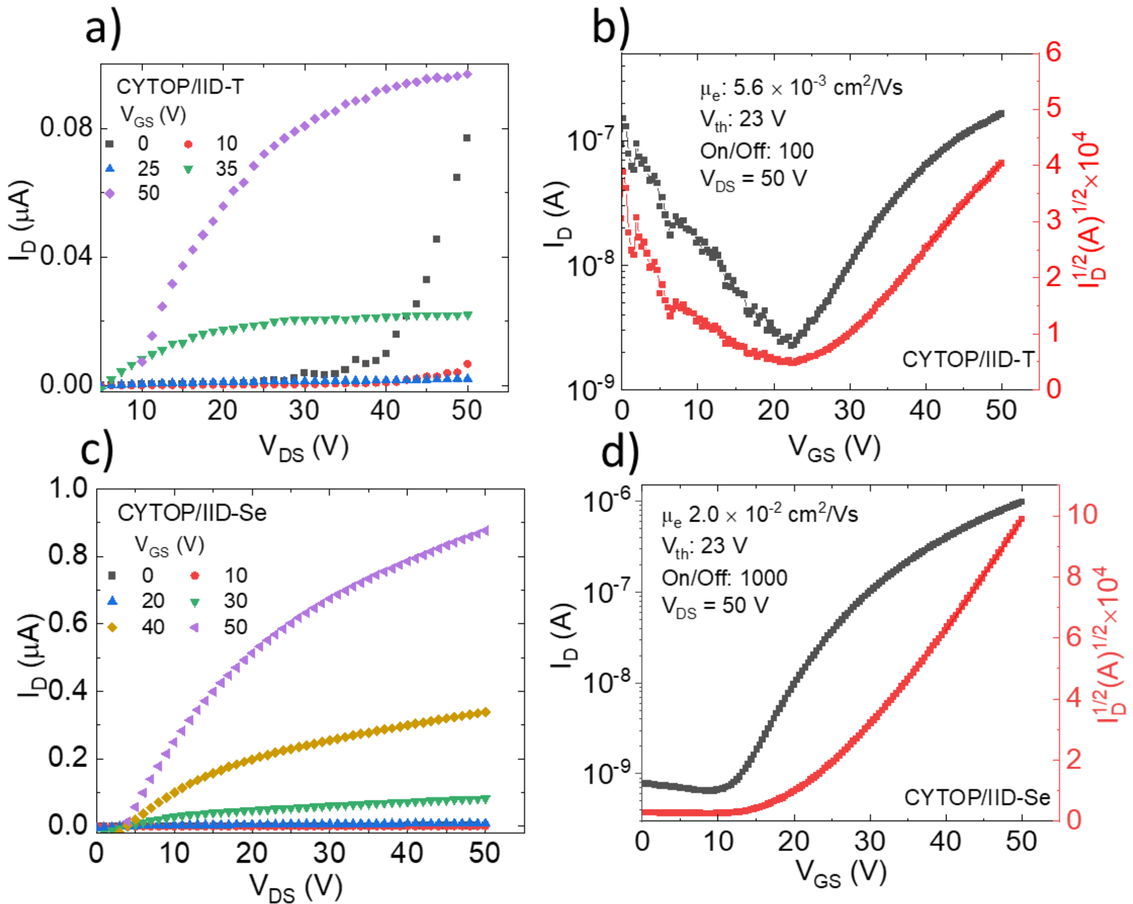

Figure 5.4. a-b) Output and transfer characteristics of FET made using IID-T with CYTOP. c-d) Output and transfer characteristics of FET made using IID-T with CYTOP. Adapted from my published work [102].

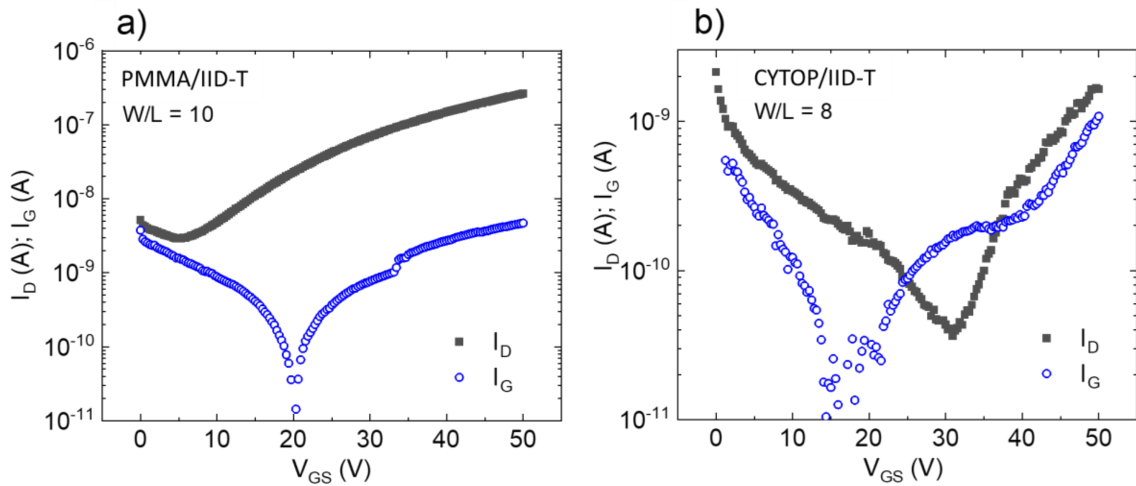

Figure 5.5. Typical transfer characteristics from TGBC IID-T FETs with gate leakage current in a) PMMA and b) CYTOP devices. Adapted from my published work [102].

To reduce the gate leakage current, top gate IID-T and IID-Se FETs with PMMA were also fabricated. Results from IID-T are presented in Figure 5.6. Results from IID-Se are presented in Figure 5.7, where the FETs showed a higher on/off ratio (10^5) compared to the CYTOP devices. By comparing the output curves in Figure 5.4 c) and Figure 5.7 a), it is evident that there is higher leakage in the CYTOP/IID-Se FET. There was a slight improvement in the carrier mobility upon using PMMA, but the order of magnitude was the same as the CYTOP devices**.** Figure 5.7 c) shows a histogram of the electron mobilities from 15 devices. Figure 5.7 d) plots the contact resistance from one such PMMA/IID-Se FET.

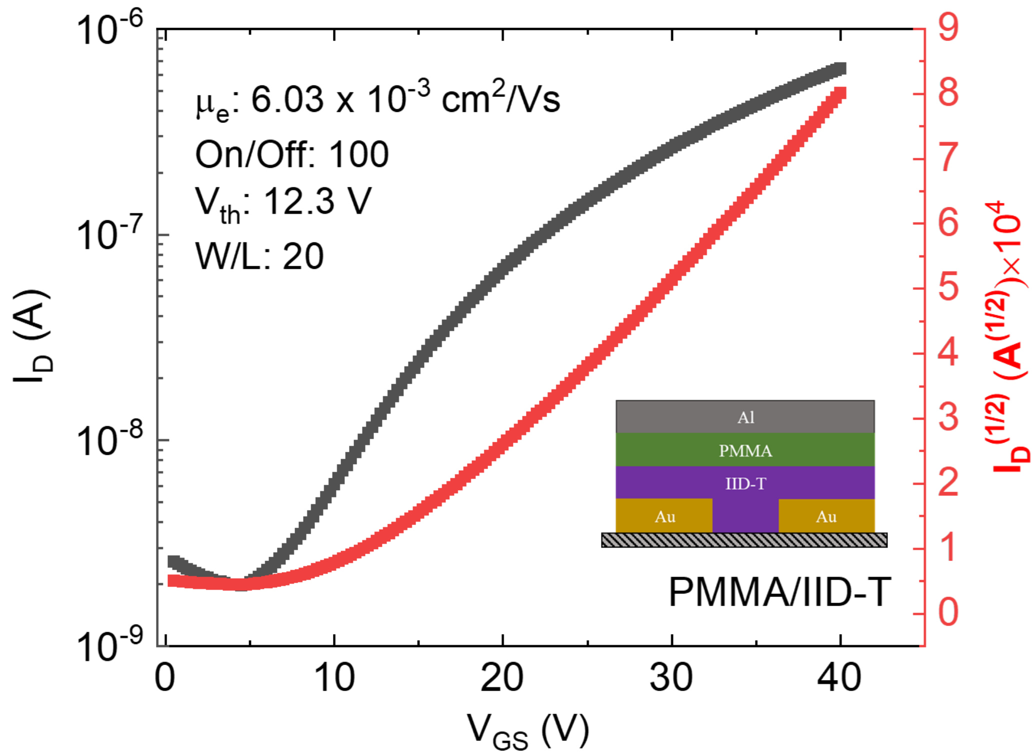

Figure 5.6. Transfer characteristics from a TGBC IID-T / PMMA FET. Inset shows device architecture, which was similarly employed for the IID-Se / PMMA devices. Adapted from my published work [102].

A clear improvement is seen in the transition from BGTC to TGBC devices. The n-type characteristics in both IID-T and IID-Se are strongly enhanced in TGBC FETs, similar to what has been observed in other D-A systems such as benzodipyrrolidone-based copolymers [105]. Moreover, IID-Se shows an order of magnitude higher FET carrier mobility compared with IID-T.

To gain further insight into the carrier motion - specifically to observe whether n-type is the predominant behavior - and to obtain a better estimate of the carrier mobility, free from contact resistance, a nonlinear optical method has been utilized which will be discussed more in the following section.

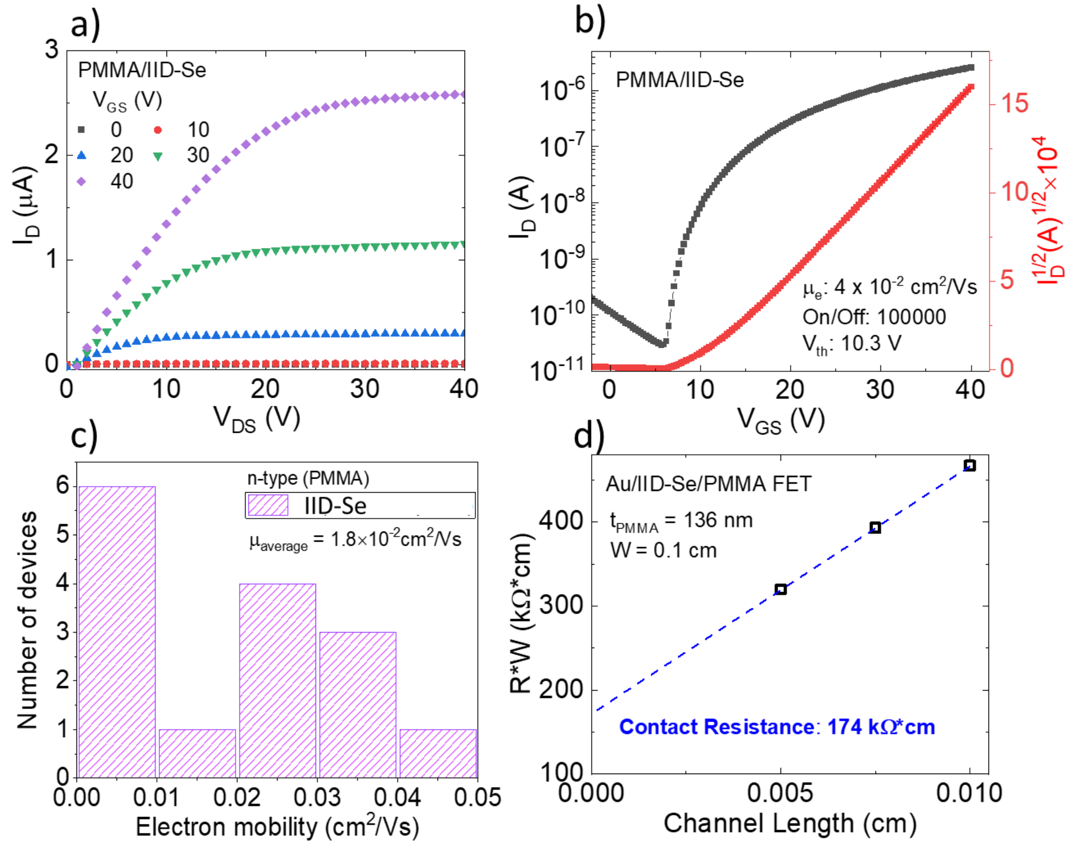

Figure 5.7. a-b) Output and transfer characteristics of TGBC IID-Se / PMMA FET (with W = 1000 µm, L = 100 µm). c) Histogram of electron mobilities from TGBC IID-Se / PMMA FETs. d) Contact resistance estimation. The product of the channel width and total resistance versus channel length for TGBC IID-Se / PMMA FET. Adapted from my published work [102].

5.5 Ascertaining Contact Resistance of IID-Se Devices

To explore the contact resistance of the PMMA/IID-Se devices, the previously mentioned transmission line method (TLM) was utilized. Although there could be differences between the contact resistance obtained from the normal linear region and the saturation region [106], the slope from Figure 5.7 d) was used to estimate μ_{eff} for a rough comparison with the electrical measurements and the EFISHG mobility discussed later in this section. For V_{GS} = 50V, where V_T varies between 7V– 9V, μ_{eff} = 0.06 cm^2/Vs. The average value of the contact resistance from the IID-Se devices is 170 kΩ*cm. It should,

however, be noted that since V_T varies from device to device, the TLM method is not completely reliable to obtain contact-free carrier mobility; a better electrical method is the gated four-probe method [107].

Another method by which one can ascertain a contact-free mobility is through use of nonlinear optics. In the late 1990s it was shown that the second-order nonlinear optical response in the presence of an electric field allowed mapping the charge distribution at the interface in Si-based metal-oxide-semiconductor devices [108,109]. Since then, transient electric field-induced second harmonic generation (TR-EFISHG) methods have provided a path for probing dynamic carrier motion in organic FETs [110-112]. To realize EFISHG behavior, materials are not required to be non-centrosymmetric. Typical electric fields (~ 10^4 V/cm) applied as the parallel source-drain fields in FETs are adequate to break the symmetry, and if excited with light of frequency, ω, it results in the second harmonically generated light at 2ω. In TR-EFISHG, the carrier motion is indirectly probed by visualizing the movement of the dielectric polarization induced by the electric field of the moving carriers.

Payal Bhattacharya performed all the TR-EFISHG measurements for the PMMA/IID-Se devices and obtained a mobility of $\mu = 0.25 \pm 0.025$ cm^2/Vs. This mobility is almost an order of magnitude higher than what is obtained from the electrical measurements. For more detailed information on the TR-EFISHG setup and how the results were obtained, the reader is referred to Ref [102].

From these results, IID-Se and IID-T are shown to provide excellent n-type behavior for the organic IID polymer. With the existing plethora of excellent p-type organic polymers, including TIPS-Pentacene and DPP-DTT, the use of these IID copolymers opens

a path towards complimentary logic behavior, which will be explored in the following chapter.

Chapter 6: Complementary Inverter Architectures

As outlined in Chapter 2, p-type and n-type FET devices can be interconnected to construct complementary inverter circuits, which are one of the simplest forms of a logic circuit. This chapter will explore various inverter circuits which were constructed based on both the p-type DPP-DTT and the n-type IID-Se (IID) copolymers as well as other materials which have not yet been discussed in this work.

6.1 DPP-DTT Inverter

A complementary inverter system was designed using DPP-DTT FETs for both the pull-up and pull-down portions of the circuit. Individual FET devices utilizing DPP-DTT with PMMA as the dielectric were fabricated as previously discussed in Chapter 4. To form the inverter circuit, one contact pad for each device were soldered together, forming the common "drain" through which the output voltage (V_{out}) would be biased. The behavior of this circuit can be seen in Figure 6.1 below. The FET device acting as the "pull up" transistor (p-type) had a mobility of 0.14 cm^2/Vs and a threshold voltage of -17.8V. By comparison, the FET device acting as the "pull down" transistor (n-type) had a mobility of 0.02 cm^2/Vs and a threshold voltage of 27.5 V.

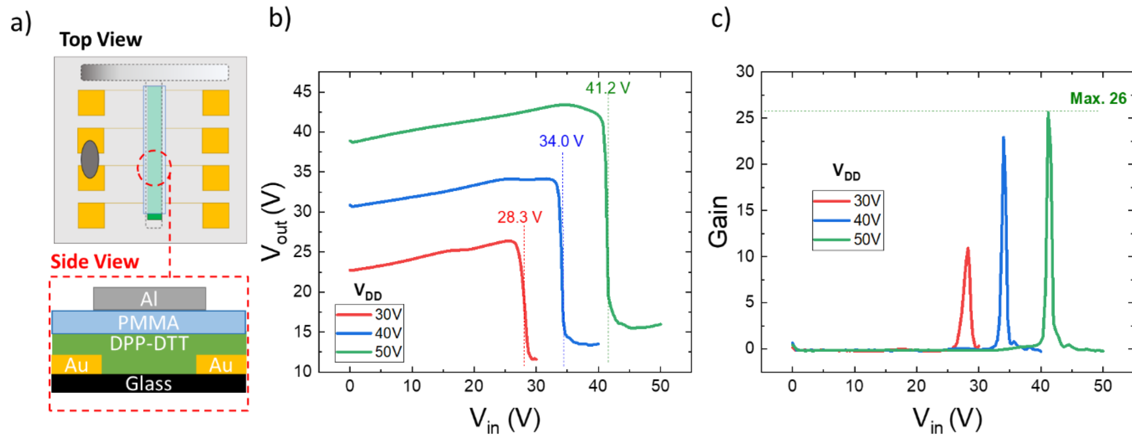

Figure 6.1. a) Architecture of DPP-DTT/PMMA FETs. The grey oval connecting two of the left Au pads in the Top View is the solder used to form the inverter. b) voltage transfer characteristics of DPP-DTT Inverter c) voltage gain characteristics of the DPP-DTT Inverter. The dotted lines in a) mark the trip point for each value of V_{DD}, and the dotted line in b) marks the maximum gain achieved.

It is immediately apparent from the voltage transfer characteristics (Figure 6.1 b)) that the inverter circuit was not behaving in an ideal manner. Firstly, at low input voltages (V_{in}), the pull-up transistor should pull V_{out} to the supply voltage (V_{DD}). As shown here, V_{out} slowly increased with V_{in} but was never fully equivalent to V_{DD} before reaching the trip point. Secondly, at high V_{in}, the pull-down transistor should pull V_{out} to zero. None of the characteristics were pulled below 10 V. Thirdly, the trip-point should occur around $V_{in} = V_{DD}/2$; however, all of the trip points were shifted to voltages approximatley 13-16 V higher than expected. Each of these nonidealities can serve as a guide to further understanding inverter behavior.

The issues of the circuit failing to be fully pulled-up or pulled-down is a result of the inverter being constructed with ambipolar transistors. It has been shown previously that complementary inverters made using ambipolar transistors are affected by “minority carriers” allowing for the flow of current in each device throughout the entire operation of the circuit [113-115]. Conceptually, one can imagine that if the n-type transistor can also

facilitate hole transport, then at low values of V_{in} the pull-down transistor is not in the steady "off" state as expected. A similar argument could be made for the pull-up transistor at high values of V_{in}. Another issue that can arise for the pull-down transistor is that if it has low electron conductivity, it does not produce enough current to pull V_{out} down to ground [114]. These DPP-DTT/PMMA devices demonstrated hole mobilities that were an order of magnitude higher than their n-type mobilities. Additionally, the threshold voltage for the pull-down transistor was about 10 V higher in magnitude than the pull-up transistor. This mismatch of currents can act to shift the trip point of the circuit away from $V_{DD}/2$, and thus result in nonideal noise margins.

To remedy this, FET devices must be constructed which share similar performance and which favor one type of transport rather than being ambipolar. Based on the previous discussion of SAMs with DPP-DTT, one can envision applying PFBT to some devices and PEIE to others to modify the charge transport of the pull-up and pull-down transistors, but this can prove to be difficult in practice when working with a single substrate. Even with precaution the SAM layers may extend beyond the desired boundaries without clever patterning techniques. For this reason, it is easier to select materials that are already p- or n-type rather than trying to modify.

6.2 DPP-DTT and IID-Se Inverter

Another inverter was constructed by making use of a DPP-DTT/PMMA FET as the pull-up transistor and an IID-Se/PMMA FET, as the pull-down transistor. In Chapter 5, the IID-Se material was shown to demonstrate excellent n-type behavior when used with PMMA as the dielectric. For these devices, a special mask was employed for both the gate

and source/drain contacts to form complementary inverter architectures on a single substrate. Figure 6.2 below shows the structure of these devices. For these devices, the gold and aluminum contacts were evaporated as normal, but using the new masks. For the spincoating of DPP-DTT, IID-Se, and PMMA, Teflon tape was used to deposit each channel individually without overlap. Both DPP-DTT and IID-Se were spincoated dynamically at 1500 RPM for 60 seconds and subsequently annealed at 180°C for 10 minutes.

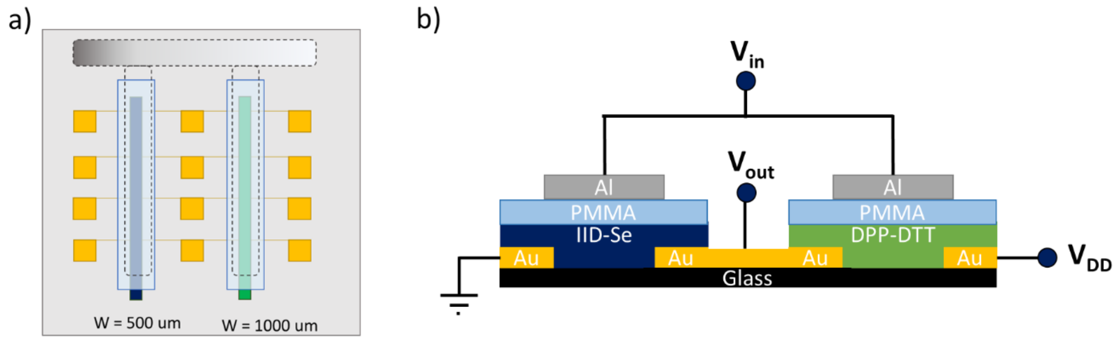

Figure 6.2. a) Top and b) side diagram of complementary inverter architecture.

For individual FET characteristics, the IID-Se device showed a mobility on the order of 10^{-3} cm^2/Vs and the DPP-DTT device showed a mobility on the order of 10^{-2} cm^2/Vs. Although there is an order of magnitude difference between the devices' mobilities, the magnitude of their threshold voltages were very close to one another, with values of -19.9 V and 18.1 V for DPP-DTT/PMMA and IID-Se/PMMA, respectively. It should also be noted here that the channel width for the DPP-DTT device (W_p) was double that of the IID-Se device (W_n). The relative width of the p- and n-type devices is inversely proportional to the currents through the devices:

$$\frac{Wp}{Wn} = \frac{In}{Ip} \qquad (6.1)$$

For submicron complementary inverter devices, it is typical for the current through the n-type device (I_n) to be double that of the p-type device (I_p) [116]. Altering the size of each device can act to shift the trip point in inverter voltage characteristics.

Figure 6.3 below shows the voltage characteristics and gain of the inverter. In comparison to the circuit made from only DPP-DTT devices, the DPP-DTT / IID-Se inverter demonstrated values of V_{out} at low V_{in} that are much closer to the expected V_{DD}. The trip point of this circuit was also closer to $V_{DD}/2$, although it is still somewhat shifted to higher positive values, likely owing to the difference in mobility of the pull-up and pull-down transistors. Although the inverter was initially pulled-down close to $V_{out} = 0$ V, as V_{in} continued to increase V_{out} began to be pulled up again. This could be due to the influence of the DPP-DTT device, which was still ambipolar and likely not completely "off" in this state. For this reason, it is important to try and construct an inverter without using an ambipolar material for either device.

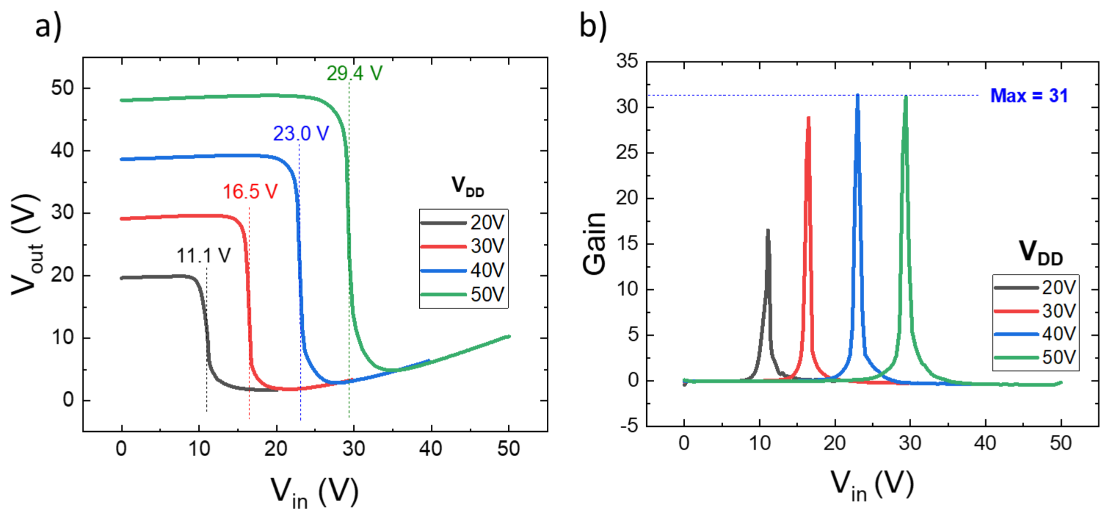

Figure 6.3. a) Voltage characteristics and b) voltage gain of DPP-DTT/IID-Se inverter circuit. The dotted lines in a) mark the trip point for each value of V_{DD}, and the dotted line in b) marks the maximum gain achieved.

6.3 Quinoxaline and IID-Se Inverter

Quinoxaline (Qx) - a polymer made up of a benzene ring and a pyrazine ring - is another polymer material which has been explored in the area of applying donor or acceptor substitutions towards the realization of reliable semiconductors for organic photovoltaic devices [117-121]. As part of these donor-acceptor systems, Qx acts as an electron deficient acceptor group. As part of ongoing work in further collaboration with Dr. Mohammed Al-Hashimi's research group at the University of Texas A&M at Qatar, they have sent a sample of Qx functionalized with thienylenevinylene (Tv) as an electron-rich donor group. The entire polymer will be referred to hereafter as Tv-Qx. As this part of the work is currently ongoing, the contents of this section will not explore the synthesis of this copolymer nor compare its individual performance to similar copolymer systems. This section will instead briefly explore the usage of Tv-Qx in FET devices as well as its application in complementary inverter circuits with the previously detailed IID-Se.

A solution of Tv-Qx was formed in 1,2 dichlorobenzene at a concentration of 5 mg/mL. The solution preparation, its spincoating, and the subsequent annealing of the film were all the same as the previously considered IID-T and IID-Se in Chapter 5. These films were similarly incorporated into TGBC architectures which utilize PMMA as the dielectric layer. Figure 6.4 below outlines some of the electrical characteristics of such an FET device. The Tv-Qx material demonstrates p-type semiconducting behavior when gold is utilized for the source and drain contacts.

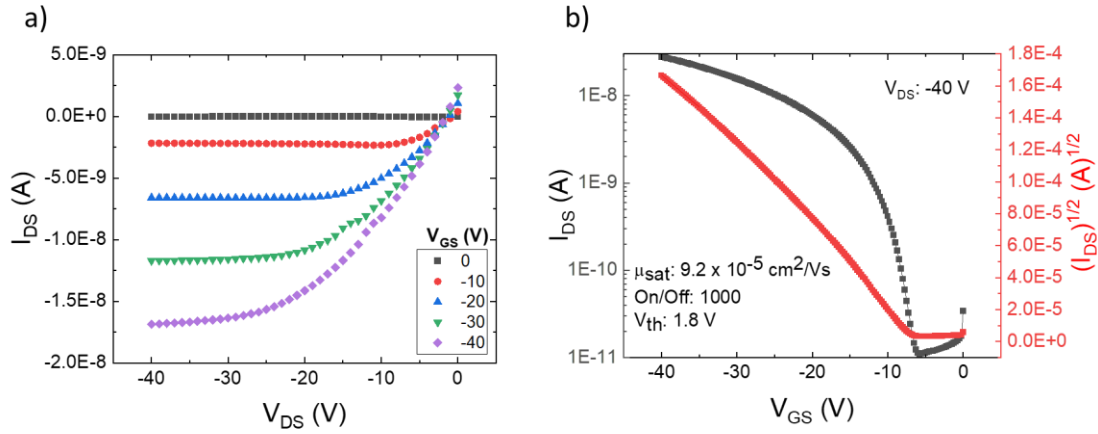

Figure 6.4. a) Output and b) transfer characteristics of a Tv-Qx FET utilizing PMMA as the dielectric layer. This particular device utilized OTS-SiO$_2$ as the substrate instead of glass to try and improve film formation.

The p-type devices using Tv-Qx demonstrated an average hole mobility of 5.57 x 10^{-4} cm^2/Vs and an average threshold voltage of -9.5 V when measured in saturation with a drain source bias of -40V. By comparison, n-type devices fabricated using IID-Se demonstrated an average electron mobility of 1.2 x 10^{-3} cm^2/Vs and an average threshold voltage of 14.8 V.

Although the IID-Se devices had a slightly higher mobility and threshold voltage than the Tv-Qx devices, both sets demonstrated comparable performance within one order of magnitude of each other for every characteristic. For this reason, devices from each substrate were connected to each other using solder to create simple inverter circuit architectures. Here the Tv-Qx device was acting as the pull-up FET and the IID-Se device was acting as the pull-down FET. Figure 6.5 below outlines the voltage transfer characteristics and gain of one such inverter circuit. It is worth noting that each device for this inverter had the same channel width.

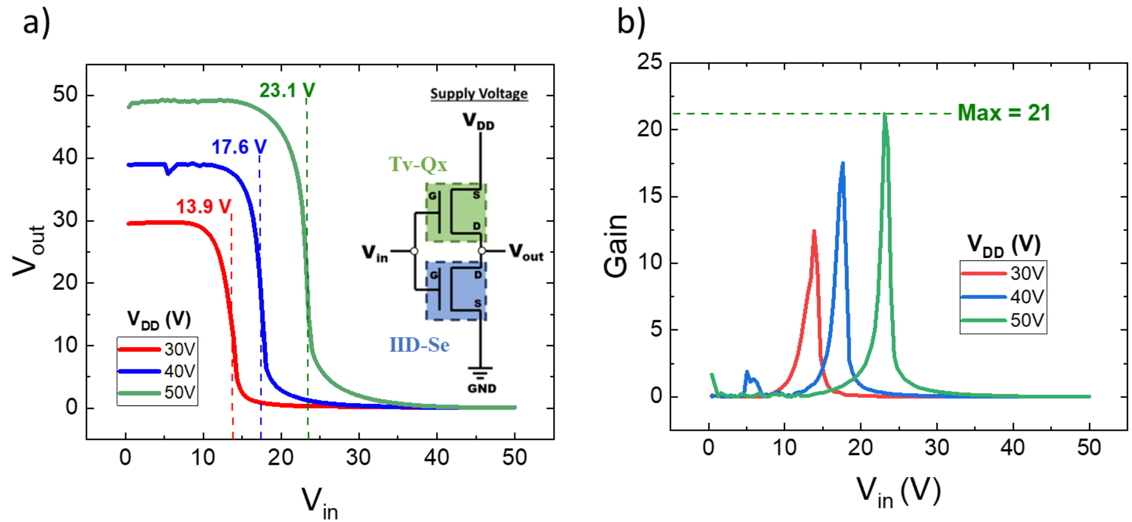

Figure 6.5. a) Voltage transfer characteristics of Tv-Qx / IID-Se inverter circuit. Inset represents circuit layout. b) Signal gain of the Tv-Qx / IID-Se inverter.

The voltage transfer characteristics of this inverter circuit were much closer to an ideal case than the DPP-DTT-based inverters that have been discussed up until now. With Tv-Qx acting as a dedicated hole transport material and IID-Se acting as a dedicated electron transport material, the steady state characteristics of V_{out} did not vary greatly with V_{in}. That is to say, at low values of V_{in}, V_{out} remained pulled up to V_{DD} and there appeared to be no influence of minority carriers from the IID-Se device. Similarly, at high values of V_{in}, V_{out} remained pulled down to ground. Furthermore, the trip point occured at voltages that are very close to $V_{DD}/2$, suggesting that the influences on device current from channel width, mobility, and threshold voltage were fairly balanced.

6.4 Sol-Gel Processed Zinc Oxide for N-type FETs

Another candidate for a material which would give reliable n-type FET behavior is the oxide semiconductor zinc oxide (ZnO). ZnO is non-toxic metal-oxide semiconductor and has several methods which can be used to deposit thin films of it, including atomic layer

deposition [122], pulsed laser deposition [123,124], spray pyrolysis [125], hydrothermal deposition [126], and vapor deposition methods [127]. Another low-cost method towards realizing thin film ZnO is a sol-gel processes [128,129]. Solution processed ZnO films have shown high n-type carrier mobilities in FET architectures; annealing temperatures of 500 °C have resulted in μ values being as high as 6 cm^2/Vs [130]. These ZnO films utilized hydration chemistry for designing benign but highly reactive aqueous precursors. The sol-gel films used in this work and other reports use a simpler route of spincoating an organometallic diethylzinc precursor solution and annealing the films in air at relatively low temperatures [131]. Further, by controlling the humidity condition, while annealing ZnO films, one can adjust the intrinsic doping levels, carrier concentration, and thus improve FET performance [132]. There are further reports of using indium ZnO for enhanced FET performance with on/off ratio over 10^7 [133].

Naturally occurring oxygen vacancies (V_O) in ZnO films may lead to trap sites that are detrimental to device performance. Several groups have demonstrated that a UV-ozone treatment after film growth is an effective means of filling the vacancies [40,134,135]. This is seen to dramatically improve the performance of hybrid photodiodes [136] and thin film transistors [137]. Electron energy loss spectroscopy has suggested thay oxygen vacancy sites are passivated within the bulk of the film to at least 90nm upon UV-ozone treatment [136]. This is beneficial for bottom-gate ZnO FETs since film thicknesses are typically less than 90nm, ensuring that trap sites due to oxygen vacancies at the ZnO-dielectric interface can be minimized.

Fabrication of ZnO FETs

Zinc Acetate Dihydrate ($C_4H_6O_4Zn\ 2H_2O$, ACS Reagent ≥98%), ethanolamine (C_2H_7NO, ACS Reagent ≥99.0%), and 2-methyoxyethanol ($C_3H_8O_2$, anhydrous 99.8%) were obtained from Sigma Aldrich. The Zinc Oxide (ZnO) precursor solution was made by combining 270 μL of ethanolamine with 10 mL of 2-methoxyethanol and then adding 1g of zinc acetate dihydrate. A magnetic stirrer was added to the solution vile, and the solution was allowed to stir for >12 hours at room temperature. The solution was then filtered with a 0.22 μm PTFE filter prior to spincoating.

Silicon substrates were utilized for the ZnO devices, with the heavily doped side acting as the gate contact and the 200nm SiO_2 layer acting as the dielectric. These substrates were cut and cleaned using an organic method. 500μL of ZnO solution was cast and spincoated onto the cleaned substrates under ambient conditions at 2000 rpm for 60 seconds. The films were annealed in an oven set to 100°C for 10 minutes and then placed into the chamber of a Harrick Plasma PDC-32G plasma cleaner. To fill the oxygen vacancies, a UV-ozone treatment (as outlined in Chapter 3) was performed on the ZnO film at an O_2 pressure of 300 mTorr for 60 seconds. Following this treatment, the film was further annealed for 50 minutes on a hotplate set to 275°C followed by annealing in an oven at 220°C for 24 hours. 60nm aluminum layers were thermally evaporated onto the ZnO film to form the source and drain contacts of the FET devices.

Performance ZnO FETs and the Impact of UV-Ozone

During a UV-Ozone treatment UV light dissociates ozone, O_3, to form atomic oxygen which can then react with the ZnO film and fill V_O. This process is outlined schematically

in Figure 6.6 a). Extended exposure may result in interstitial oxygen, which is why the exposure time was limited to 60 seconds rather than the 10-minute period usually employed for plasma cleaning surfaces. The output characteristics of two ZnO FETs, where the ZnO film was left either untreated or having undergone a UV-ozone treatment are shown in Figure 6.6 b) and c). In the untreated film, when the device enters the saturation region, there is a rapid loss in current. This is attributed to trapping of charge carriers by V_O within the conducting channel. With UV-ozone treated films, a clear saturation region is observed in the output characteristics. It has been further observed that a large positive threshold voltage as well as a hysteresis in the transfer characteristics are linked to a high density of interfacial trap states due to V_O. Compared to the untreated ZnO FETs, the UV-ozone treated FETs show hardly any hysteresis in the transfer characteristics [137]. For non-treated ZnO FETs, the median mobility across several devices is 2.5×10^{-5} cm^2/Vs. Some of the high performing UV-ozone treated FETs yield mobilities in the 10^{-2} cm^2/Vs range, which were used in an inverter circuit architecture discussed in the following section.

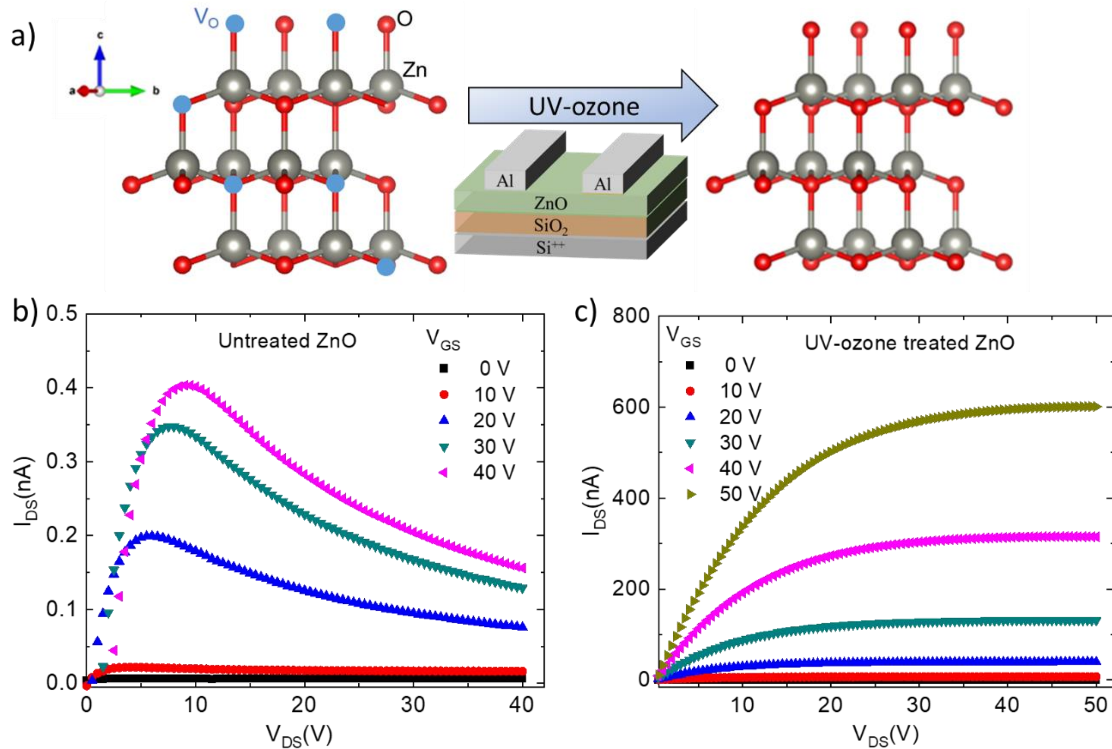

Figure 6.6. a) Diagram outlining how a UV-Ozone treatment acts to fill oxygen vacancies in ZnO films. b) Output characteristics of an untreated ZnO film c) Output characteristics of a UV-Ozone treated ZnO film. Adapted from my published work [138].

6.5 DPP-DTT and ZnO Inverter

A complementary inverter circuit was constructed using the previously discussed ZnO and DPP-DTT FETs. The DPP-DTT FETs were constructed in a BGTC architecture utilizing PVDF-TrFE for the dielectric layer. The performance of such devices is discussed in Chapter 4 in more depth and are expected to be entirely p-type as opposed to ambipolar due to the dielectric-semiconductor interface of DPP-DTT and PVDF-TrFE. For the purposes of building the inverter circuit, a vertical-poled DPP-DTT/PVDF-TrFE sample was utilized because its mobility was comparable to that of the ZnO FET, as will be shown later. Wires were soldered onto the contacts of the p-type FET, while for the n-type FET, due to the geometry of the contacts, it was easier to attach the probes directly. The drain

contact of n-type FET (ZnO) was connected to ground and its source contact connected to the drain of the p-type FET. Connections between the two FETs as well as between the FETs and the instrumentation were external, and the instruments used for the DC inverter characteristics were the same as outlined in Chapter 3.

Figures 6.7 a) and b) show the transfer characteristics of the individual DPP-DTT and ZnO FETs which were used to construct the inverter circuit. One aspect to realize here is that V_T of the n-FET is higher than that of the p-FET, because a low κ (SiO_2) dielectric was used, which will have an important impact on the results when compared to the model.

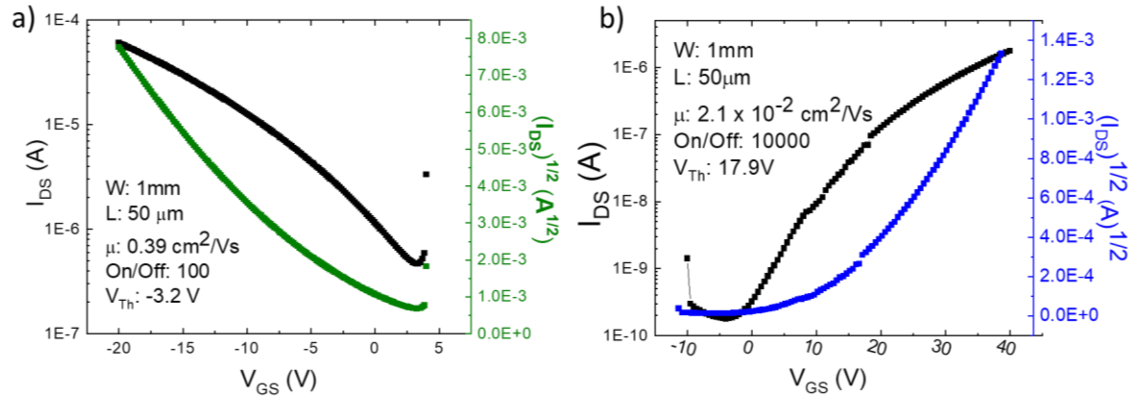

Figure 6.7. a) Transfer characteristics for DPP-DTT FET using vertically-poled PVDF-TrFE as the dielectric. b) Transfer characteristics of UV-Ozone ZnO utilizing SiO_2 as the dielectric. Adapted from my published work [138].

Inverter Characteristics and Application of Model

For modelling the inverter circuit, parameters from individual FETs are required. Figure 6.8 shows examples of how the models were applied to the data to extract the parameters. The experimental output characteristics, plotted by the dotted lines, are the same in both and are from a DPP-DTT FET. Returning to the equations considered earlier in Chapter 3, equations (3.5) and (3.6) - which are denoted here as “Method 1” - were used to model the output characteristics in Figure 6.8 a), shown by the bold lines. Similarly, the

application of equation (3.7) is denoted as "Method 2" and was used to model the same set of output characteristics, shown in Figure 6.8 b) by the bold lines. Apart from some deviations with the experimental data, Method 2 performed better. Both methods, however, yielded similar values of $\lambda = 0.005\ V^{-1}$, which is required as an input parameter for the inverter circuit.

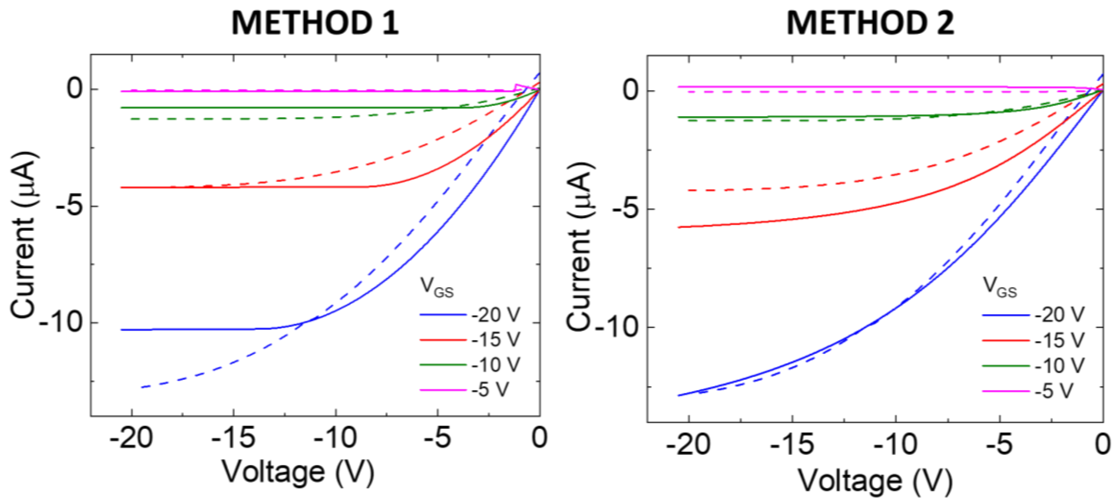

Figure 6.8. Application of models of FET characteristics (solid lines) to experimental data (dashed lines) for the output characteristics of a textured-poled DPP-DTT/PVDF-TrFE FET. Adapted from my published work [138].

Table 6-1 shows the parameters used in the inverter model. The inverter output characteristics are shown in Figure 6.9 a) at V_{DD} of 20V and 25V. A maximum voltage gain ($-dV_{out}/dV_{in}$) of 28 was observed when V_{DD} was held at 25V. The theoretical simulations are plotted along with the experimental data in Figure 6.9 b). One can reconcile the differences observed between the model and the experimental results based on the information presented in Chapter 3 and the behavior of inverter circuits in the previous sections of this chapter. The higher V_T of the n-FET compared with the p-FET extends the initial steady state to high input voltages, in general. Even then, this region extended to higher voltages in the experimental data compared to the simulated data. Most likely the

reason is twofold. First, the magnitude of the drain-source current in the n-FET was smaller than the p-FET, requiring a higher input voltage for turning on the n-FET. Second, the model used here is an ideal inverter without considering any leakage current or parasitic capacitance [48]. Leakage currents should be modelled as a parallel resistor to the inverter, which have not been considered in the simulations.

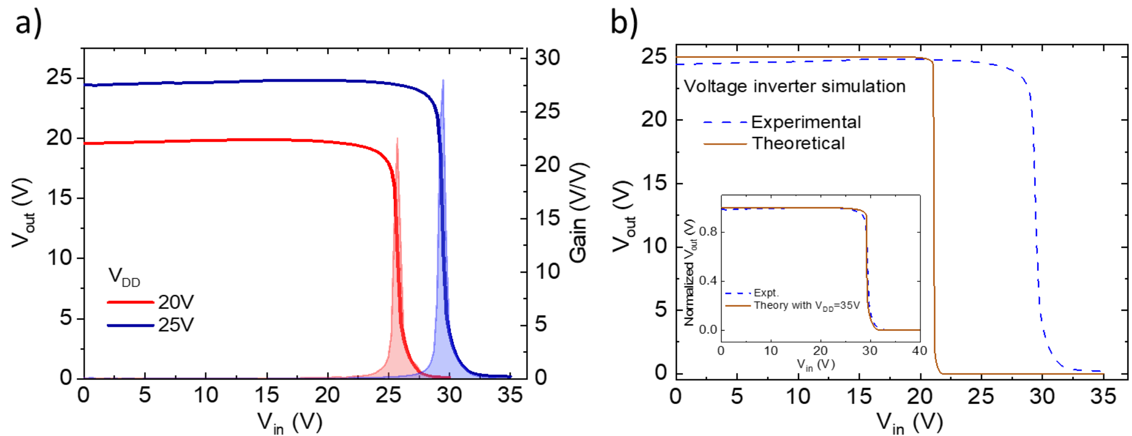

Figure 6.9. a) Voltage transfer characteristics for DPP-DTT/ZnO inverter circuit with signal gain placed on the inset of each curve. b) Comparison between the experimental data (dashed line) and the theoretical data from the inverter model. Adapted from my published work [138].

Further, it is interesting to note that when the inverter simulations were performed using V_{DD}=35V, and when the experimental and theoretical output characteristics are normalized, both experimental and theoretical curves mimic each other as shown in the inset of Figure 6.9 b),. This suggests that the additional voltage provides a higher input current to turn the n-FET on, taking into effect the leakage current through the FETs.

Table 6-1. The values of the individual parameters of p-type and n-type FETs used for the inverter model. Adapted from my published work [138].

Parameter	p-type (DPP-DTT)	n-type (ZnO)
L	1000 μm	1000 μm
W	50 μm	50 μm
V_{Th}	-3.2 V	17.9 V
μ	0.38 cm^2/Vs	0.02 cm^2/Vs
λ	0.005 V^{-1}	0.0005 V^{-1}

The results of this chapter have demonstrated that several proof-of-concept inverter circuits can be constructed utilizing a wide variety of materials and architectures. From these results, it is clear that any steps which can be taken to reduce parasitic effects and fine tune device performance will lead to better voltage inverters which have strong steady-state logic, fast switching, and uniform noise margins. The use of contact modification, alteration of device geometry, and the previously discussed poling of ferroelectric materials all provide ways that such tuning could be achieved. The next chapter will seek to explore another way that, through modification of the dielectric layer, one might be able to further tune device behavior.

Chapter 7: Addition of Magnetic Nanoparticles to the Polymer Dielectric

In the early discussion of organic FETs in Chapter 2, the importance of the dielectric constant - and by extension the dielectric layer's capacitance - towards the accumulation of charges was outlined. In Chapter 4, it was demonstrated how modifications of a ferroelectric polymer via an external field can further modify a device's behavior. Adding insulating nanoparticles - in particular, magnetic nanoparticles - in a controlled fashion to a polymer dielectric layer has the benefit of enhancing the capacitance without affecting the localization of carriers at the interface in the same way that polarizable dielectrics do. An added advantage of such a strategy is that it provides a potential mechanism for tuning charge transport in organic FETs via external magnetic fields. This chapter will seek to explore modification of a common polymer dielectric through the addition of cobalt ferrite magnetic nanoparticles and the effects this addition has on the layer's effective dielectric constant, capacitance, uniformity, and the effects it can produce when applied to MIM, MIS, and FET architectures.

7.1 Impact of Insulating Nanoparticles

Metal-doped nanoparticles of spinel MFe_2O_4 - where M is a +2 cation of Mn, Fe, Co or Ni - have received a lot of attention as contrast agents for magnetic resonance imaging [139]. In particular, cobalt ferrite ($CoFe_2O_4$ or CFO), owing to its moderate values of saturation magnetization, high magneto-crystalline anisotropy, high Curie temperature, and easy tunability of particle size [140,141] has been used in biomedical applications [142-145]. CFO, which belongs to the iron oxide (Fe_3O_4) group with ferrimagnetic spin

structure, is a partially inverse spinel structure. A perfect spinel structure has 24 cations (of A^{2+} and B^{3+} type) occupying 8 of the 64 available tetrahedral (T_d) sites and 16 of the 32 available octahedral (O_h) sites in addition to the 32 oxygen anions. For a perfect inverse spinel structure, half of the B^{3+} occupy the T_d sites, and 8 A^{2+} ions and 8 B^{3+} ions occupy the O_h sites. The structure of Fe_3O_4 with the O_h and T_d sites is represented in Figure 7.1 a). Fe^{2+} and Fe^{3+} ions occupying the O_h sites align parallel to an external magnetic field and Fe^{3+} ions in the T_d sites lattice sites align antiparallel to the field [146], as depicted by the blue and black arrows. The Co ions in CFO mainly occupy the O_h site, replacing the Fe^{2+} ions. In the perfect case, $(Fe^{3+})_{Td}$ $(Co^{2}+, Fe^{3+})_{Oh}$, the spins of Fe^{3+} in the O_h and the T_d sites would cancel, leaving only the Co^{2+} to contribute. From the effective Bohr magneton: $g[J(J+1)]^{1/2}$, where J is the total angular momentum and g is the Landé g-factor, the effective magnetic moment (μ_B) per ion for Co^{2+} ($3d^7$) is 3.87. A higher or a lower value of the saturation magnetization compared to 3.87 suggests the occupation of some T_d sites by Co ions such that a complete cancellation of spins by the Fe^{3+} ions is not achieved.

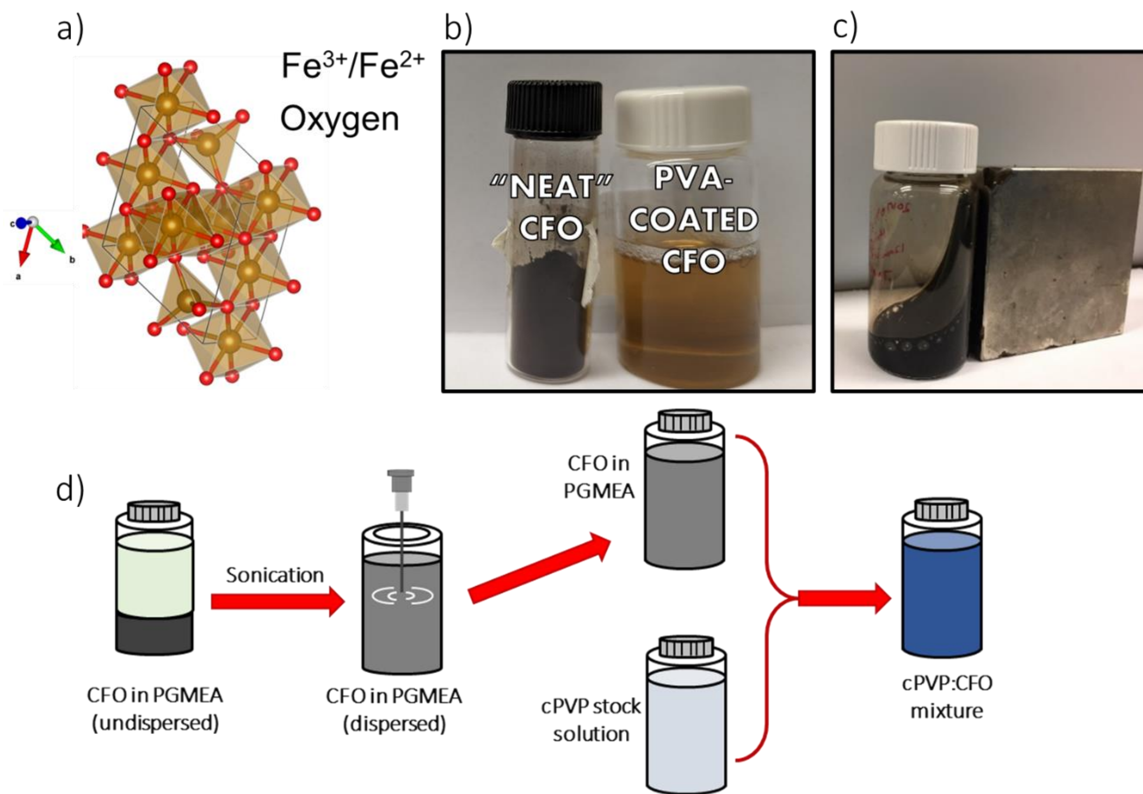

Figure 7.1. a) Crystal structure of Fe_3O_4, where the Fe^{3+} ions occupy both the T_d and O_h sites, and the Fe^{2+} ions occupy the O_h sites. The black and the blue arrows depict the direction of the magnetic moment of Fe ion on the T_d and O_h sites, respectively. In CFO, the Co^{2+} ions replace the Fe^{2+} ions in the O_h site. b) Comparison of "neat CFO" in its bulk state to the PVA-coated CFO, already dispersed in DMF. c) Response of CFO dispersion to an external magnet. d) process used to disperse the bulk CFO in PGMEA and mix to form cPVP:CFO solution. Adapted from my published work [147].

CFO is attractive for use as a gate dielectric in organic FETs owing to its insulating properties, making magnetic field controlled transistors and devices an attractive possibility [148]. Zang *et al*. demonstrated gate engineering in flexible organic FETs by using Fe_3O_4 nanoparticles incorporated silver nanowires as the gate electrode [149]. These flexible FETs show a dramatic change (increase in current) in the transistor transfer characteristics when a small field of 150 mT is applied upon deformation, mainly due to the magnetic force acting on the gate electrode.

CFO nanoparticles tethered to self-assembled peptide nanostructures have provided a platform for tuning the magnetic properties as well as a viable route towards using it as a

dielectric in organic FETs. In particular, the operating voltage of pentacene FETs with CFO embedded peptide nanostructures as a gate dielectric layer have been shown to be substantially lower compared to using only peptide nanostructures a dielectric layer of similar thickness [150]. The roughness and the nonuniformity of peptide nanostructured films often result in gate leakage current in FETs. It should be pointed out that the peptide nanostructures are also ferroelectric, inducing polarization effects at the semiconductor-insulator interface.

Herein, the performance of organic FETs using CFO-embedded cross-linked poly (4-vinyl phenol) (cPVP) is explored. Both commercially-obtained CFO nanoparticles (~20nm) as well as CFO nanoparticles synthesized by a thermal decomposition method and coated with poly(vinyl alcohol) (PVA) (~5nm) have been used.

7.2 Fabrication of PVP/CFO Devices

The PVP solution was made along with the crosslinking agent PMMF as outlined in Chapter 4. This solution was made using PGMEA as the solvent when incorporating the commercially-available CFO and was made using DMF as the solvent when incorporating the PVA-coated CFO nanocrystals. The commercially-available CFO (hereafter referred to as “neat CFO”) was purchased from Inframat Advanced Materials with an average particle size of 20 nm. The PVA-coated CFO nanocrystals were obtained through collaboration with Dr. Jaewon Lee in the Department of Chemical Engineering at the University of Missouri, where he employed a thermal decomposition method, which is outlined in Ref. [151]. Dr. Lee also studied the morphology and properties of these nanocrystals using transmission electron microscopy (TEM), thermal gravimetric analysis (TGA), and x-ray diffraction (XRD). Some of these results will be alluded to throughout

this chapter; however, for a full outline of the synthesis process and the nanocrystals' properties, please refer to Ref. [147]. As a final step, the PVA-coated nanocrystals were dispersed in DMF.

For the solutions made using the neat CFO, 6 mg of the nanoparticles were dispersed into 500 μL PGMEA and horn tip sonicated at 10 kHz for 45 seconds to evenly disperse. The stock cPVP solution (~80 mg/mL concentration) was divided into two parts, 500 μL each. One part was mixed with 500 μL PGMEA to form the pure cPVP solution (~40 mg/mL concentration) and the other part was combined with the CFO dispersion (~40 mg/mL cPVP, ~6 mg/mL CFO). This method for incorporating "neat CFO" is outlined in Figure 7.1 d). For the PVA-coated CFO, the nanocrystal dispersion was mixed with the PVP stock solution (this time utilizing DMF instead of PGMEA) in a 1:1 ratio by volume, resulting in a final mixture which had a concentration of 60 mg/mL in cPVP and 3 mg/mL CFO.

Film Formation

Glass substrates were cleaned using an organic cleaning method. Aluminum gate contacts were thermally evaporated onto the cleaned glass. Each solution - containing pure cPVP, cPVP with added neat CFO (hereafter referred to as cPVP:CFO), or cPVP with added PVA/CFO nanocrystals (hereafter referred to as cPVP:CFO/PVA) - was spincoated onto the glass substrates at 5000 RPM for 60 seconds and the resulting films were then immediately annealed at 120°C for 1 hour to facilitate crosslinking. Both the spincoating and annealing were performed under a nitrogen atmosphere. To produce a metal-insulator-

metal (MIM) structure, Au contacts were then thermally evaporated onto the films using a mask which produced circular pads which varied in diameter from 250μm to 1000μm.

To realize metal-insulator-semiconductor (MIS) and FET devices, the small molecule pentacene (obtained through Tokyo Chemical Industry) was utilized as the semiconducting layer. The process for forming the dielectric layer was the same, but prior to depositing the Au top contacts, 50 nm of pentacene was thermally evaporated. In the case of FET devices, a mask was used to restrict the semiconductor channel to a thin line in the center of the substrate. For the FET devices, the evaporated Au contacts used a different mask than that of the MIM or MIS structure, such that separate source and drain contacts were created with varying W/L ratios for the devices. Each FET device had a channel width of 1000 μm and the channel length varying from 50 μm to 125 μm.

7.3 Characteristics of MIM and MIS Diodes

MIM capacitors fabricated from as-is cPVP and 20:1 wt% cPVP:CFO films of the same thickness (50 nm) show a difference in their capacitance values, as demonstrated in Figure 7.2 b). The CFO nanoparticles in these films were the ones commercially obtained without any coating. It was clearly observed that the addition of CFO nanoparticles enhances the effective κ of the dielectric layer as a whole.

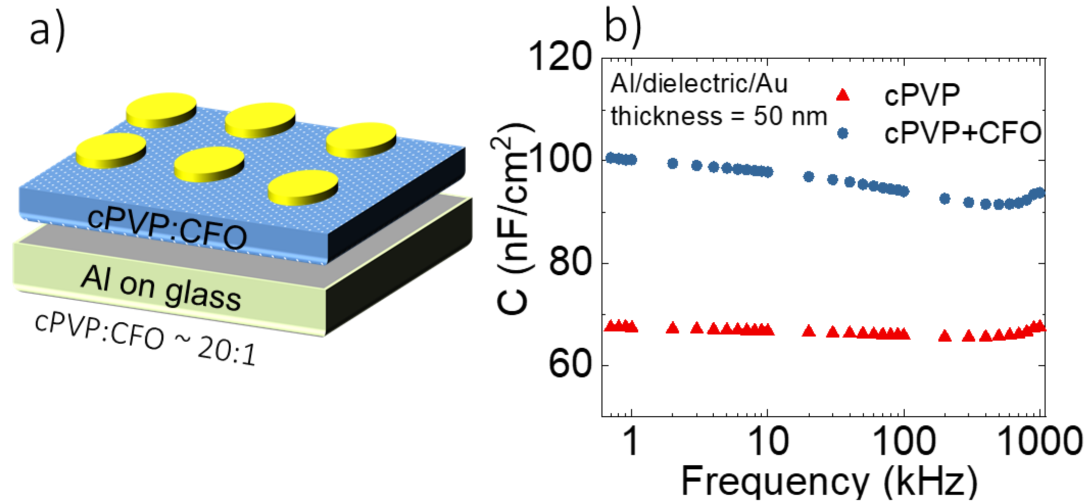

Figure 7.2. a) MIM structure b) C-F characteristics of cPVP and cPVP:CFO films of equal thickness. Adapted from my published work [147].

To ascertain whether the synthesized PVA coated CFO nanocrystals provide a similar platform for enhancing the capacitance of a polymer dielectric compared to neat CFO, MIS diodes were fabricated with pentacene as the semiconducting layer. Increasing the concentration of CFO/PVA in cPVP resulted in some non-uniformity of films, as shown in the optical images of spincoated films in Figure 7.3. For the MIS and FET architectures, the 16:1 (cPVP:CFO/PVA) concentration was chosen as an optimized film architecture. This concentration demonstrated uniform coverage over an area where several devices could be compared along with the goal of achieving a higher capacitance compared to as-is cPVP devices.

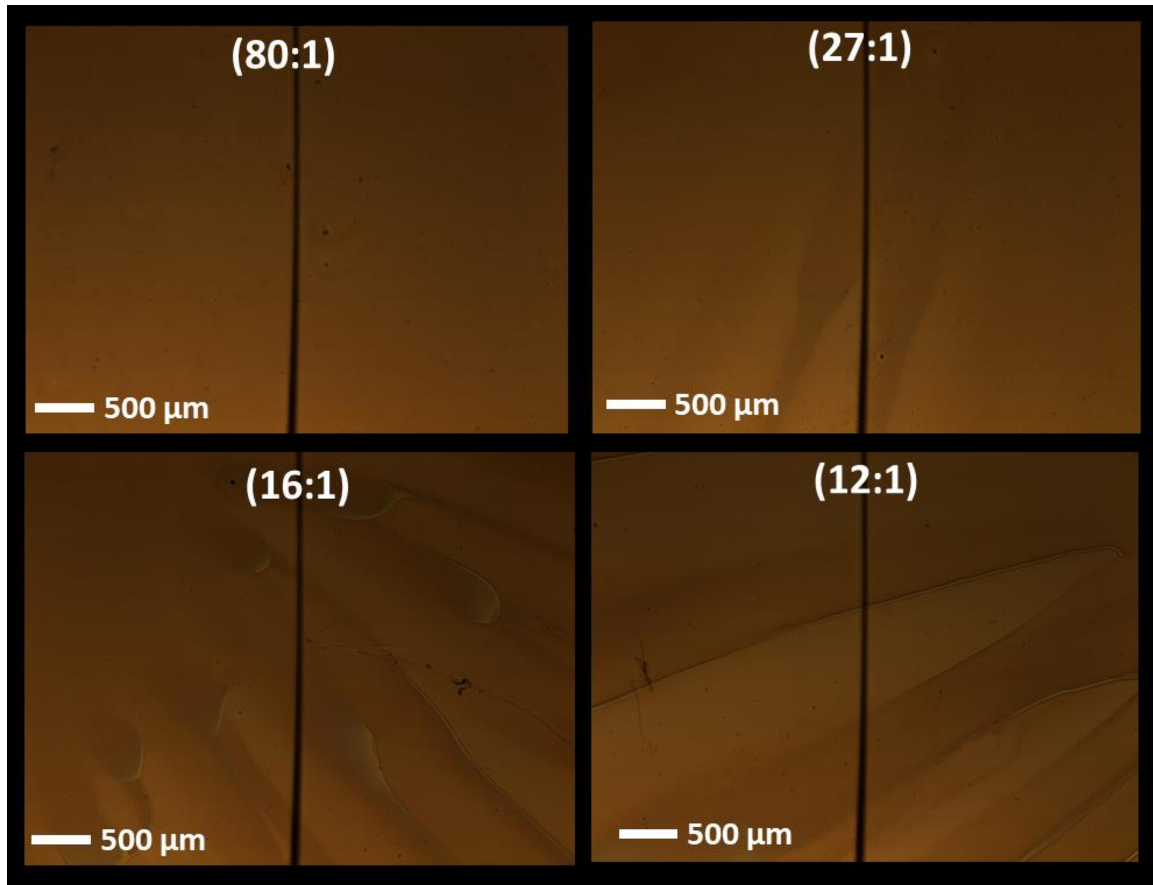

Figure 7.3. Optical microscope images of cPVP:CFO/PVA films. All films were fabricated with the same spincoating parameters with only their concentration varying. This value is listed in parentheses of each image as the ratio of cPVP to CFO/PVA. Adapted from my published work [147].

For identical film thicknesses, the capacitance of the MIS diode with cPVP:CFO/PVA was higher than only cPVP (shown in Figure 7.4 b)), which is again an indication that the addition of CFO/PVA in cPVP enhances κ. It was further seen that the hysteresis, which may arise due to the polarizing dipole charges of the hydroxyl (-OH) group, was reduced when CFO/PVA was added to the dielectric. The hysteresis that results from the polar -OH group of polymers is well documented in the literature; the polar group acts as a trapping site [95]. Further, the crosslinking agent that couples the -OH groups with either hydrogen or methyl groups has been shown to reduce this hysteresis [152]. The further reduction in the influence of the hydroxyl groups in cPVP in this work can be understood based on a

physical crosslinking occurring between the -OH group and the oxide group of CFO nanoparticles. A similar reduction has been previously demonstrated by Beaulieu *et al*, who observed a noticeable decrease in hysteresis of their device characteristics as they increased the amount of ZrO_2 nanoparticles in their polymer layer [153].

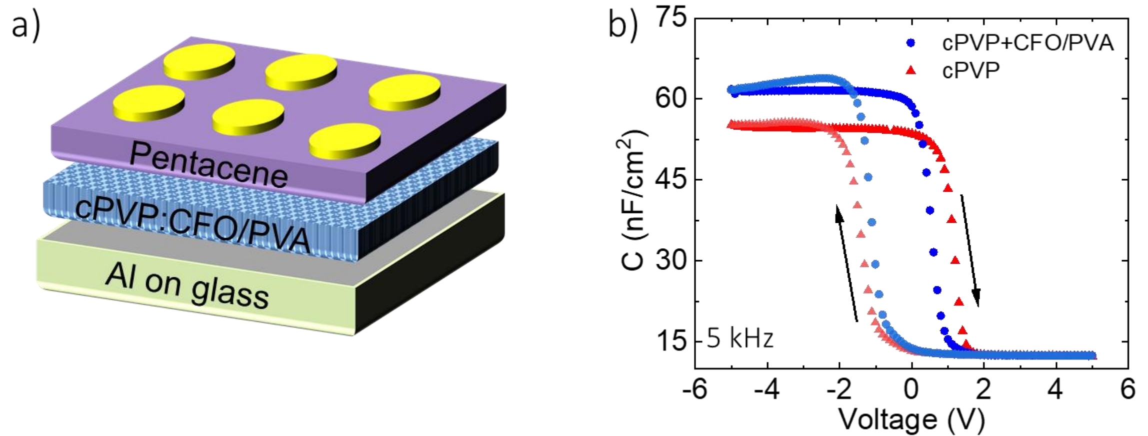

Figure 7.4. a) Structure of MIS device using cPVP:CFO/PVA with pentacene. b) Hysteresis curves for cPVP and cPVP:CFO/PVA MIS devices across a 5V window. Adapted from my published work [147].

7.4 Characteristics of FET Devices

In addition to MIM and MIS devices, the influences of these films were studied in BGTC FET architectures while utilizing 50nm of pentacene as the semiconducting layer. Pentacene was chosen over TIPS-pentacene for these devices owing to the uniformity afforded by thermal evaporation. As previously mentioned, the film formation via dropcasting of TIPS-Pentacene is sensitive to surface morphology, which varied somewhat with these samples. The output and transfer curves from a pentacene FET with cPVP:CFO as the dielectric layer are shown in Figure 7.5 a-b). The transistors operated well below 2V with a threshold voltage (V_T) of approximately -1V. Due to the nonuniformity of neat CFO nanoparticles in cPVP, using cPVP+CFO/PVA in FETs gave a higher level of control. The

transfer characteristics from a cPVP:CFO/PVA FET with a specific W/L ratio are shown in Figure 7.5 c-d). The transfer characteristics of two similar pentacene FETs are compared: one with as-is cPVP and the other with cPVP:CFO/PVA. The dielectric thicknesses were approximately the same (55nm).

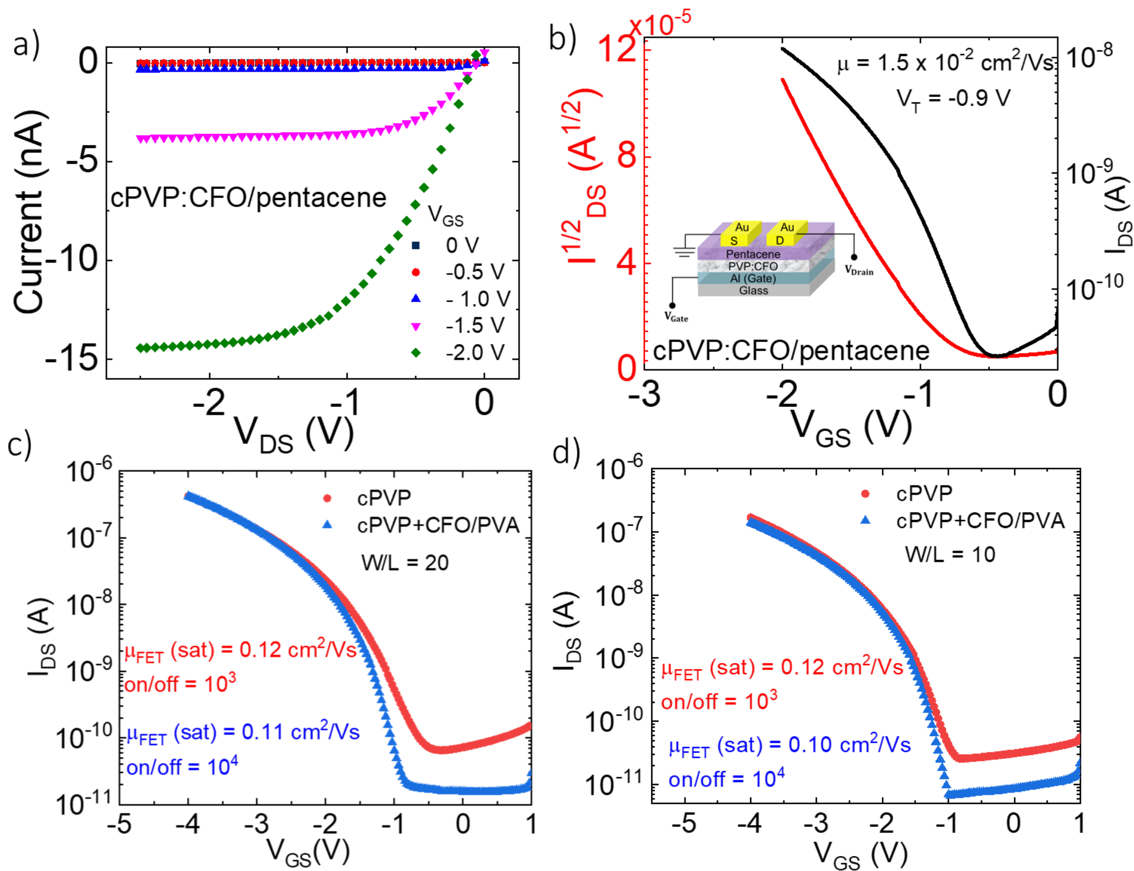

Figure 7.5.a) Output and b) transfer characteristics of cPVP:CFO/pentacene FET. The inset in (b) shows a schematic of the FET geometry. c-d) Transfer characteristics from a pentacene FET with cPVP (red curve) and cPVP+CFO/PVA (blue curve) dielectrics. Adapted from my published work [147].

The average carrier mobilities and V_T from all three dielectrics (with comparable thickness) are represented in Figure 7.6. As seen, V_T was the smallest for cPVP:CFO FET; however, due to a clustering effect with neat CFO, the on/off ratio and carrier mobility were lower compared with cPVP:CFO/PVA FETs. Although the carrier mobilities and V_T were similar for cPVP and cPVP:CFO/PVA devices, the on/off ratio was enhanced by an

order of magnitude with the addition of CFO/PVA; the addition of nanocrystals reduced the off current. The polarizing -OH group in PVP, which results in a hysteresis of the C-V curve could have induced a spontaneous polarization along the lateral direction of the FET, resulting in an increase in the off current. This behavior has been observed with polarizable ferroelectric dielectrics discussed in Chapter 4 where lateral poling, which sets up a parallel spontaneous electric field, similarly increases the off current [56]. The addition of CFO could have reduced the spontaneous polarization, consistent with the previously discussed reduction in the hysteresis of the C-V curve for the MIS devices, thereby decreasing the off current. In Table 7-1, the performance of these devices is compared with those of other works utilizing nanoparticle-polymer composites towards enhancing the dielectric properties in FET devices.

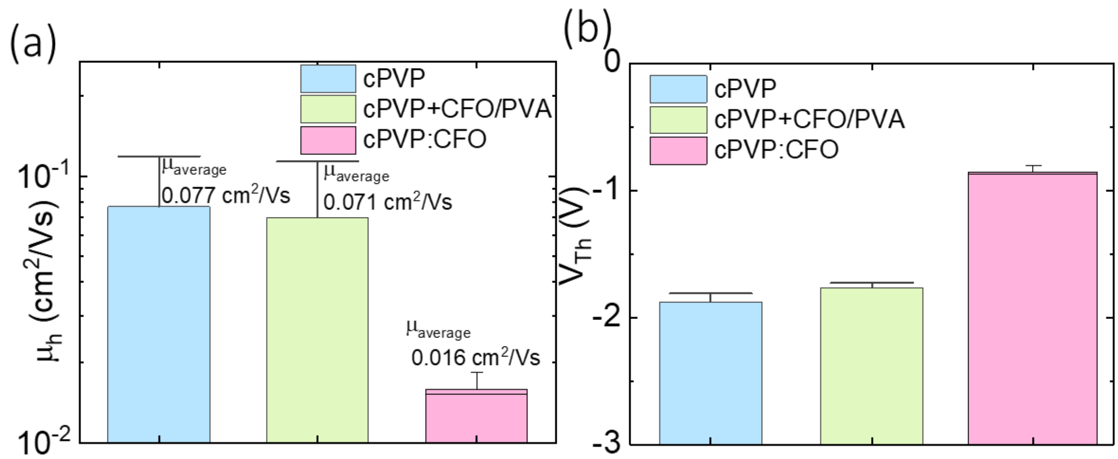

Figure 7.6. a) Average carrier mobilities and b) average threshold voltages from pentacene FETs using cPVP (blue), cPVP:CFO/PVA (green) and cPVP:CFO (pink) dielectrics. Adapted from my published work [147].

Table 7-1.FET performance with various polymer nanocomposites. Adapted from my published work [147].

Dielectric Polymer	Nanoparticle	Semiconductor	μ_{sat} (cm^2/Vs)	On/Off	V_{th} (V)	Reference
cPVP	CFO	Pentacene*	0.018	10^2	-0.87	This work
cPVP	CFO/PVA	Pentacene*	0.110	10^4	-1.75	This work
cPVP	AT/ODPA	Pentacene*	0.400	10^4	-5.00	[154]
cPVP	AT/ODPA	F_{16}CuPC**	0.005	10^3	+2.00	[154]
cPVP	BZ	Pentacene*	0.200	10^4	-6.00	[155]
cPVP	TiO_2	Pentacene*	0.105	10^3	-0.80	[156]
PI	HfO_2	Pentacene*	0.110	10^4	-6.19	[157]
PVA	Al_2O_3	CuPC*	0.057	-	-	[158]
CYLEP	ZrO_2	P3HT*	0.080	10^3	-1.00	[153]

* p-type semiconductor; ** n-type semiconductor; cyanoethyl pullulan (CYELP); polyimide (PI); AT (aluminum titanate); ODPA(n-octadecylphosphonic acid); BZ(barium zirconate).

7.5 Effects of an External Magnetic Field on Device Behavior

Coin-shaped neodymium magnets - purchased from K&J Magnetics, Inc – were used to apply a small magnetic field (0.1T) to the previously mentioned cPVP:CFO MIM device. From here the capacitance was observed to further increase, as shown in Figure 7.7 a). The increase in capacitance at a field strength of 0.1T is approximately 4%. There are several possible origins to magnetocapacitance. The phenomenon of magnetocapacitance in tunneling junctions such as Pd/AlOx/Al arises due to the spin-dependent potential on electron screening lengths [159]. A magneto-dielectric/capacitance response in nanocomposites has been attributed to the interfacial polarization of the two phases [160,161]. This usually occurs in multiferroic composites where ferroelectricity and ferromagnetism co-exist. Such films can exhibit giant magnetocapacitance values due to the large compressive stress in the CFO phase. Organic semiconductors doped with spin radicals upon photoexcitation show enhanced magnetocapacitance due to an internal spin-exchange interaction [162]. One may be able to invoke the multiferroic ideas to explain the behavior, although PVP is not ferroelectric. However, as previously seen, the capacitance-

voltage curves showed a hysteresis, similar to what is seen in polymer ferroelectric dielectrics, signaling polarization effects. It is likely that the presence of the magnetic field resulted in a field dependent structural organization, enhancing the space charge polarization and, thus, the capacitance. A similar effect was also observed with capacitors fabricated with CFO tethered to self-assembled peptide nanotubes, where the peptide nanotubes act as the dielectric layer [150].

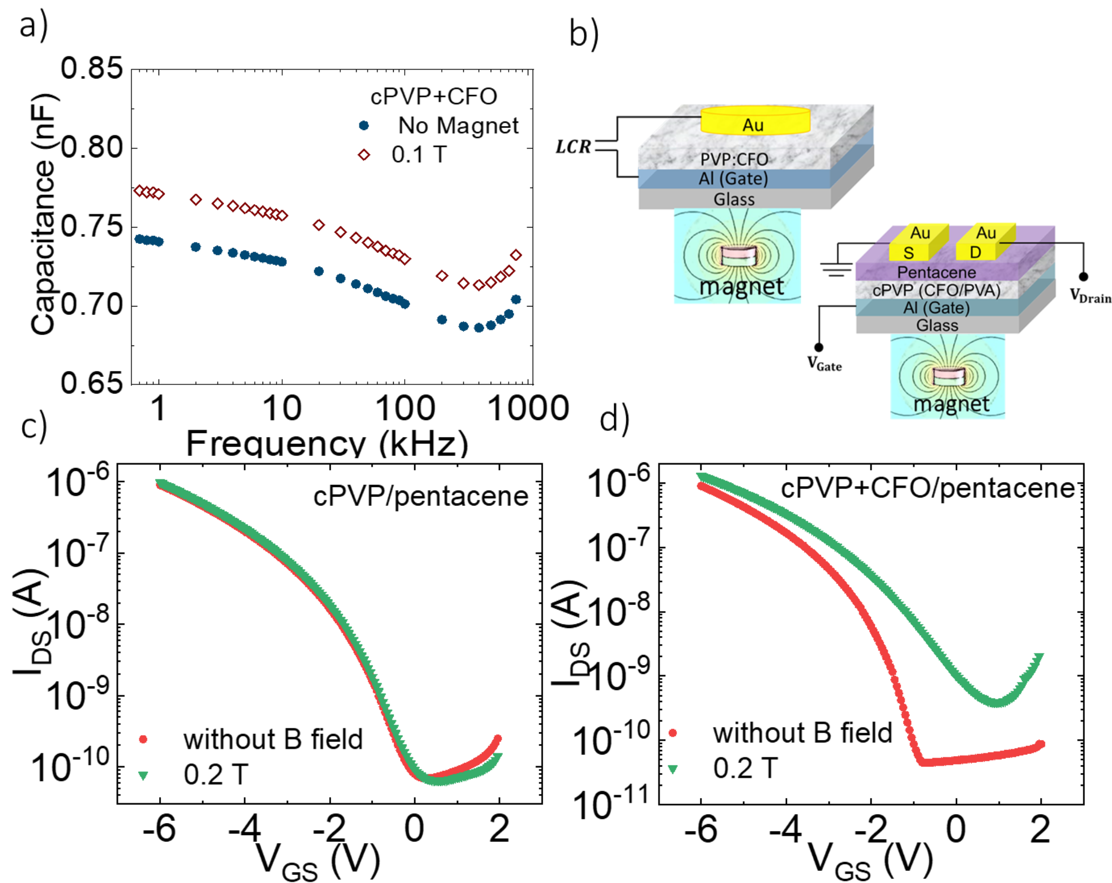

Figure 7.7. a)C-F characteristics of cPVP+CFO MIM capacitor with (0.1 T) and without magnetic field. b) outline of the MIM and FET architectures studied with the application of a magnetic field. c) Transfer characteristics of as-is cPVP (pentacene FET with and without an external magnetic field. d) Transfer characteristics of cPVP+CFO/PVA/pentacene FET with and without an external magnetic field. Adapted from my published work [147].

The transfer characteristics of pentacene FETs using both cPVP and cPVP:CFO/PVA were also studied in the presence of a small magnetic field, as shown in Figure 7.7 c-d). In

the absence of CFO within the dielectric, no changes were observed in the transfer characteristics upon applying a small field. In a polymer layer containing CFO, however, I_{DS} increased with a slight increase in the off current in the presence of a 0.2T magnitude field. Upon removing the field, the transfer characteristics did not completely recover, at least within half an hour, suggesting that some trapping sites may have been filled/unfilled. Although the effect of the magnetic field here seems to degrade the FET performance, with a different FET geometry and the orientation of the field, one may be able to enhance the on/off ratio.

In bendable FETs with magnetic electrodes, it has been shown that the change in the transfer characteristics (enhancement in I_{DS}) upon the application of a field (B_0) arises due to a magnetic force (F_B), where $F_B \propto B_0 \frac{dB}{dz}$; z being perpendicular to the FET in the direction of the applied field [149]. Since the distribution of the CFO nanoparticles in the dielectric here was not uniform, there may have been a gradient, due to which the magnetic force may influence the trap states, altering the transfer characteristics. Hence, it is conceivable that in the presence of a bending force (where the substrate itself can be bent), the change in I_{DS} under the presence of an external field was accentuated.

Chapter 8: Summary and Outlook

This work has explored the mechanics which drive charge transport in organic transistor systems. In Chapter 4, it was demonstrated how the reorientation of the dipole moments inherent to ferroelectric materials using an external field could act to enhance charge accumulation and transport. The higher κ value of ferroelectric dielectrics compared to other non-ferroelectric polymer dielectrics allow DPP-DTT FETs to operate at low voltages. The influence of the semiconductor/dielectric interface and device architecture was also demonstrated, as DPP-DTT FETs were observed to recover their expected ambipolar behavior when used in a TGBC architecture using PMMA as opposed to a BGTC architecture using PVDF-TrFE. Furthermore, the impact of modifying the metal contacts' work function was observed through utilizing PEIE and PFBT to enhance electron and hole injection, respectively. Finally, the potential use for dielectric bilayers, which bring certain physical characteristics of each individual layer, was also demonstrated.

In Chapter 5, the n-type characteristics of fluorinated isoindigo with substituted thiophene and selenophene groups were shown to be strongly enhanced in TGBC FETs, although the selenophene-substituted polymer showed stronger characteristics. This is similar to what has been observed in other D–A systems such as benzodipyrrolidone-based copolymers [163]. The higher effective mobility from both TLM and TR-EFISHG when compared to that determined experimentally for FET devices suggests that by reducing the contact resistance, for example by treating the Au electrodes by a SAM layer previously discussed for DPP-DTT, it is possible to achieve improved charge injection and electron carrier mobilities upwards of 0.2 cm^2/Vs in selenophene substituted IID copolymer.

In Chapter 6, many donor-acceptor polymers, including DPP-DTT, IID-Se, and Tv-Qx, were used in concert with one another as well as with the sol-gel processable semiconductor ZnO to form proof-of-concept voltage inverter circuits. Building from fully ambipolar architectures to dedicated p- and n-type complementary architectures helped to demonstrate the role each transistor plays in the circuit's operation, and why shifting the work function of the metallic contacts (such as through SAM) would be an important step towards realizing new types of fully organic complementary systems. Additionally, a mathematical model was used to simulate the DC inverter characteristics using an open source program. Such models, which may be further improved by incorporating parasitic capacitance and leakage currents, can act as a guide in the development of complementary inverter circuits.

Finally, in Chapter 7, the incorporation of magnetic nanoparticles into cPVP demonstrated an increase in the effective dielectric constant of the dielectric layer as well as a reduction to the influence of -OH groups belonging to PVP on charge-trapping. Furthermore, magnetocapacitive behavior was shown to modify the dielectric characteristics and the charge-transport characteristics in MIM and pentacene-based FET devices, respectively.

Future Works

There are several possible routes for continuation of this research. Firstly, in regard to inverter circuits, it is critical to explore the creation of single-substrate architectures as opposed to interconnecting devices by hand, so as to avoid introducing extra resistive influences into the circuit that could be present in solder or wires used in the connections.

One such architecture was demonstrated in this work for the DPP-DTT/IID-Se inverter. Such an architecture presents challenges surrounding carefully patterning each layer to ensure that no overlap occurs between each channel. Consideration must also be taken for the processing steps of each channel to ensure that the annealing temperature of each semiconductor will not act to damage the other. Furthermore, the development of strategies to allow for the application of SAM layers to each set of contacts separately could lead to the realization of reliable inverter behavior while still relying on ambipolar materials. This, as well, will require careful quarantining of each set of contacts during each treatment process to ensure no unwanted overlap occurs.

Once inverters can be fabricated on a single substrate, where multiple devices operate reliably, the next step would be to interconnect several of such devices into the next step in circuit complexity, a ring oscillator. This would require a development of a new patterning mask for the metallic gates and contacts, as the common drain contact (V_{out}) would need to connect into the common gate (V_{in}) of the next inverter, with a commonly applied V_{DD} across all inverters. The formation of such a ring oscillator would allow for a deeper understanding of the transistors which comprise it, as their performance will limit the cutoff frequency of the circuit as a whole [7]. If a large number of stages for this circuit is desired, either large substrates will need to be used or smaller device sizes patterned to facilitate its creation on a single substrate. In the former case, for the sake of uniform patterning of all of the polymer layers, one would likely need to move away from spincoating and instead rely on inkjet printing or thermal evaporation for the formation of layers.

When considering the incorporation of magnetic nanoparticles into polymer dielectrics, there are several directions to take the research moving forward. Firstly, each of the types of nanoparticles explored in this work – "neat" and PVA-coated CFO – presented issues of uniform dispersion. The "neat" CFO tended to form micrometer-size clusters. While horn-tip sonication was explored as a method to disperse these particles and reduce aggregation, the particles remained clustered even after sonicating for more than an hour at a time. Extended sonication times (8 or more hours) or the exploration of other solvents which may act to better keep the particles separated may be necessary. For the PVA-coated CFO, the addition of the nanoparticles to cPVP resulted in nonuniformity of spincoated films (as previously demonstrated in Figure 7.3). At one time, slot-die coating was explored as an alternative to spincoating for these films; however, the operating parameters of the machine resulted in very thick, nonuniform films. Inkjet printing may be another route through which these films could be deposited, but one must be careful to avoid aggregation of the nanoparticles within the solution, as it could clog the nozzle of the printing head.

As the CFO-incorporated films become more reliably uniform, it would be interesting to delve deeper into the field-dependent magnetocapacitive effects. The effects demonstrated thus far made use of simple neodymium magnets, which limited how strong of a field could be applied while also accounting for the amount of space each magnet took up. Using a solenoid system to control the magnetic field strength with voltage would allow for the observation of capacitive changes with field strength. As another direction, the possibility of using CFO with ferroelectric materials is also of interest. A magnetoelectric effect (ME) has been previously demonstrated for systems which make use of a composite of both piezoelectric materials and magnetostrictive materials for applications in memory

devices, energy harvesters, and magnetic field sensors [164]. Based on the work presented in Chapters 4 and 7, one could envision the incorporation of CFO into PVDF-TrFE films directly or the formation of bilayers utilizing both PVDF-TrFE and CFO-incorporated cPVP separately. It has also previously been shown how the presence of oxygen vacancies within cobalt ferrite nanoparticles affects the material's intrinsic strain and, by extension, its magnetization [165]. In this way, one could envision applying a UV-Ozone treatment in the same manner previously discussed for ZnO and exploring how the magnetization of the particles change with exposure prior to incorporating into the films.

Finally, for the donor-acceptor polymers, more emphasis should be put into fine-tuning the application of PEIE and PFBT SAMs as well as exploring the use of alternative contact materials for modifying the metal/semiconductor interface and charge injection. For the SAMs, dedicated studies into the variance of layer thickness and roughness via atomic force microscopy is necessary to ensure that a reliable interfacial layer is being formed. Additionally, for the semiconductor films, exploring the application of other solution casting methods – such as tilted dropcasting, slot die coating, or other electrical blade deposition methods – could potentially invoke a level of crystallinity as observed for TIPS-pentacene.

REFERENCES

[1] A. Sharma, C. Madhu, and J. Singh, International Journal of Computer Applications **89**, 36 (2014).

[2] M. M. Waldrop, Nature News **530**, 144 (2016).

[3] N. M. Ashcroft, N. David, *Solid State Physics* (Cengage Learning, 2017).

[4] M. Cardona and Y. Y. Peter, *Fundamentals of semiconductors* (Springer, 2005), Vol. 619.

[5] B. G. Streetman and S. Banerjee, *Solid state electronic devices* (Prentice hall New Jersey, 2000), Vol. 4.

[6] C. Liu, Y. Xu, and Y.-Y. Noh, Materials Today **18**, 79 (2015).

[7] H. Klauk, Chemical Society Reviews **39**, 2643 (2010).

[8] Z. A. Lamport, H. F. Haneef, S. Anand, M. Waldrip, and O. D. Jurchescu, Journal of Applied Physics **124**, 071101 (2018).

[9] J. A. Lim, H. S. Lee, W. H. Lee, and K. Cho, Advanced Functional Materials **19**, 1515 (2009).

[10] M. Fox, (American Association of Physics Teachers, 2002).

[11] I. Austin and N. F. Mott, Advances in physics **18**, 41 (1969).

[12] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva Filho, J.-L. Brédas, L. L. Miller, K. R. Mann, and C. D. Frisbie, The Journal of Physical Chemistry B **108**, 19281 (2004).

[13] R. J. Chesterfield, J. C. McKeen, C. R. Newman, C. D. Frisbie, P. C. Ewbank, K. R. Mann, and L. L. Miller, Journal of applied physics **95**, 6396 (2004).

[14] S. E. Koh, B. Delley, J. E. Medvedeva, A. Facchetti, A. J. Freeman, T. J. Marks, and M. A. Ratner, The Journal of Physical Chemistry B **110**, 24361 (2006).

[15] M. Vissenberg and M. Matters, Physical Review B **57**, 12964 (1998).

[16] K. Waragai, H. Akimichi, S. Hotta, H. Kano, and H. Sakaki, Physical Review B **52**, 1786 (1995).

[17] A. Laudari and S. Guha, Journal of Applied Physics **117**, 105501 (2015).

[18] C. D. Sheraw, T. N. Jackson, D. L. Eaton, and J. E. Anthony, Advanced Materials **15**, 2009 (2003).

[19] J. Li *et al.*, Sci. Rep. **2**, 754 (2012).

[20] P. Sonar, S. P. Singh, Y. Li, M. S. Soh, and A. Dodabalapur, Adv. Mater. **22**, 5409 (2010).

[21] C. Kanimozhi, N. Yaacobi-Gross, K. W. Chou, A. Amassian, T. D. Anthopoulos, and S. Patil, J. Am. Chem. Soc. **134**, 16532 (2012).

[22] S. P. Senanayak, A. Z. Ashar, C. Kanimozhi, S. Patil, and K. S. Narayan, Phys. Rev. B **91**, 115302, 115302 (2015).

[23] A. Pickett *et al.*, ACS Appl. Mater. Interfaces **10**, 19844 (2018).

[24] R. Stalder, J. Mei, and J. R. Reynolds, Macromolecules **43**, 8348 (2010).

[25] Z. Ma, E. Wang, M. E. Jarvid, P. Henriksson, O. Inganäs, F. Zhang, and M. R. Andersson, J. Mater. Chem. **22**, 2306 (2012).

[26] E. Wang, Z. Ma, Z. Zhang, K. Vandewal, P. Henriksson, O. Inganäs, F. Zhang, and M. R. Andersson, J. Am. Chem. Soc. **133**, 14244 (2011).

[27] T. Lei, J.-H. Dou, Z.-J. Ma, C.-H. Yao, C.-J. Liu, J.-Y. Wang, and J. Pei, Journal of the American Chemical Society **134**, 20025 (2012).

[28] E.-S. Shin, Y. H. Ha, E. Gann, Y.-J. Lee, S.-K. Kwon, C. R. McNeill, Y.-Y. Noh, and Y.-H. Kim, ACS Appl. Mater. Interfaces **10**, 13774 (2018).

[29] S. E. Yoon, S. J. Shin, S. Y. Lee, G. G. Jeon, H. Kang, H. Seo, J. Zheng, and J. H. Kim, ACS Appl. Polym. Mater. **2**, 2729 (2020).

[30] J. Yang *et al.*, Adv. Mater. **29**, 1702115 (2017).

[31] Y. Shi *et al.*, Chem. Mater. **30**, 7988 (2018).

[32] M. Barłóg *et al.*, Chem. Mater. **31**, 9488 (2019).

[33] S. Dey *et al.*, ACS Appl. Mater. Interfaces **13**, 41094 (2021).

[34] H. Chen, W. Zhang, M. Li, G. He, and X. Guo, Chem. Rev. **120**, 2879 (2020).

[35] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, and S. Mohialdin Khaffaf, Advanced Functional Materials **13**, 199 (2003).

[36] T. Richards, M. Bird, and H. Sirringhaus, J. Chem. Phys. **128**, 234905 (2008).

[37] S. Fratini, M. Nikolka, A. Salleo, G. Schweicher, and H. Sirringhaus, Nature materials **19**, 491 (2020).

[38] J. W. Borchert, R. T. Weitz, S. Ludwigs, and H. Klauk, Advanced Materials **34**, 2104075 (2022).

[39] H. Li, N. Tessler, and J. L. Brédas, Advanced Functional Materials **28**, 1803096 (2018).

[40] Q. Bao, X. Liu, Y. Xia, F. Gao, L.-D. Kauffmann, O. Margeat, J. Ackermann, and M. Fahlman, Journal of Materials Chemistry A **2**, 17676 (2014).

[41] R. S. Ashraf, A. J. Kronemeijer, D. I. James, H. Sirringhaus, and I. McCulloch, Chemical communications **48**, 3939 (2012).

[42] W. H. Lee, D. H. Kim, Y. Jang, J. H. Cho, M. Hwang, Y. D. Park, Y. H. Kim, J. I. Han, and K. Cho, Applied physics letters **90**, 132106 (2007).

[43] A. Laudari, A. Pickett, F. Shahedipour-Sandvik, K. Hogan, J. E. Anthony, X. He, and S. Guha, Advanced Materials Interfaces **6**, 1801787 (2019).

[44] O. Fenwick, C. Van Dyck, K. Murugavel, D. Cornil, F. Reinders, S. Haar, M. Mayor, J. Cornil, and P. Samorì, Journal of Materials Chemistry C **3**, 3007 (2015).

[45] Y. Zhou *et al.*, Science **336**, 327 (2012).

[46] B. Stadlober, U. Haas, H. Gold, A. Haase, G. Jakopic, G. Leising, N. Koch, S. Rentenberger, and E. Zojer, Advanced functional materials **17**, 2687 (2007).

[47] D. Bode, C. Rolin, S. Schols, M. Debucquoy, S. Steudel, G. H. Gelinck, J. Genoe, and P. Heremans, IEEE transactions on electron devices **57**, 201 (2009).

[48] S. Jung, J. Kwon, S. Tokito, G. Horowitz, Y. Bonnassieux, and S. Jung, Journal of Physics D: Applied Physics **52**, 444005 (2019).

[49] A. Opitz, M. Bronner, and W. Brütting, Journal of Applied Physics **101**, 063709 (2007).

[50] A. Petritz *et al.*, Advanced Functional Materials **28**, 1804462 (2018).

[51] M. Uno *et al.*, Advanced Electronic Materials **1**, 1500178 (2015).

[52] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler, and A. Facchetti, Nature **457**, 679 (2009).

[53] S. De Vusser, J. Genoe, and P. Heremans, IEEE Transactions on Electron Devices **53**, 601 (2006).

[54] S. M. Sze, Y. Li, and K. K. Ng, *Physics of semiconductor devices* (John wiley & sons, 2021).

[55] M. Estrada, A. Cerdeira, J. Puigdollers, L. Resendiz, J. Pallares, L. Marsal, C. Voz, and B. Iñiguez, Solid-state electronics **49**, 1009 (2005).

[56] A. Laudari, A. R. Mazza, A. Daykin, S. Khanra, K. Ghosh, F. Cummings, T. Muller, P. F. Miceli, and S. Guha, Phys. Rev. Appl. **10**, 014011 (2018).

[57] A. Laudari and S. Guha, J. Appl. Phys. **125**, 035501 (2019).

[58] G. Knotts, A. Bhaumik, K. Ghosh, and S. Guha, Appl. Phys. Lett. **104**, 233301 (2014).

[59] A. Laudari, A. Pickett, F. Shahedipour-Sandvik, K. Hogan, J. E. Anthony, X. He, and S. Guha, Adv. Mater. Interf. **6**, 1801787 (2019).

[60] S. Konezny, M. Bussac, and L. Zuppiroli, Physical Review B **81**, 045313 (2010).

[61] H. Kawai, Japanese journal of applied physics **8**, 975 (1969).

[62] R. Kepler and R. A. Anderson, Journal of Applied Physics **49**, 1232 (1978).

[63] A. J. Lovinger, Science **220**, 1115 (1983).

[64] A. J. Lovinger, D. Davis, R. Cais, and J. Kometani, Macromolecules **19**, 1491 (1986).

[65] Y. Bar-Cohen and Q. Zhang, MRS bulletin **33**, 173 (2008).

[66] A. V. Shirinov and W. K. Schomburg, Sensors and Actuators A: Physical **142**, 48 (2008).

[67] P. Saketi, S. K. Latifi, J. Hirvonen, S. Rajala, A. Vehkaoja, T. Salpavaara, J. Lekkala, and P. Kallio, Sensors and Actuators A: Physical **222**, 194 (2015).

[68] A. Song, Y. Han, H. Hu, and J. Li, IEEE Transactions on Instrumentation and Measurement **63**, 1739 (2013).

[69] W. Liu, A. Menciassi, S. Scapellato, P. Dario, and Y. Chen, Robotics and Autonomous Systems **54**, 513 (2006).

[70] M. Zirkl *et al.*, Advanced Materials **23**, 2069 (2011).

[71] Y. Tanaka, D. P. Nguyen, T. Fukuda, and A. Sano, in *2015 IEEE World Haptics Conference (WHC)* (IEEE, 2015), pp. 146.

[72] L. Seminara *et al.*, IEEE Sensors Journal **13**, 4022 (2013).

[73] B. Stadlober, M. Zirkl, and M. Irimia-Vladu, Chemical Society Reviews **48**, 1787 (2019).

[74] T. J. Reece, S. Ducharme, A. Sorokin, and M. Poulsen, Applied Physics Letters **82**, 142 (2003).

[75] S. Ducharme, V. M. Fridkin, A. V. Bune, S. Palto, L. Blinov, N. Petukhova, and S. Yudin, Physical Review Letters **84**, 175 (2000).

[76] Q. Zhang, V. Bharti, and X. Zhao, Science **280**, 2101 (1998).

[77] J. J. Brondijk, K. Asadi, P. W. Blom, and D. M. De Leeuw, Journal of Polymer Science Part B: Polymer Physics **50**, 47 (2012).

[78] R. C. Naber, K. Asadi, P. W. Blom, D. M. De Leeuw, and B. De Boer, Advanced materials **22**, 933 (2010).

[79] P. L. Martins, A. C.; Lanceros-Mendez, S., Prog. Polym. Sci, 683 (2014).

[80] M.-C. L. Garcia-Gutierrez, A.; Martin-Fabiani, I.; Hernandez, J. J.; Soccio, M.; Rueda, D. R.; Ezquerra, T. A.; Reynolds, M., Nanoscale **5**, 6006 (2013).

[81] D. Guo and N. Setter, Macromolecules **46**, 1883 (2013).

[82] H. Dvey-Aharon, T. Sluckin, P. Taylor, and A. Hopfinger, Physical Review B **21**, 3700 (1980).

[83] R. G. Kepler and R. Anderson, Advances in physics **41**, 1 (1992).

[84] G. A. Samara, in *Solid State Physics* (Elsevier, 2001), pp. 239.

[85] A. Laudari, A. Mazza, A. Daykin, S. Khanra, K. Ghosh, F. Cummings, T. Muller, P. Miceli, and S. Guha, Physical Review Applied **10**, 014011 (2018).

[86] A. Laudari, J. Barron, A. Pickett, and S. Guha, ACS applied materials & interfaces **12**, 26757 (2020).

[87] M. Li, H. J. Wondergem, M.-J. Spijkman, K. Asadi, I. Katsouras, P. W. Blom, and D. M. De Leeuw, Nature materials **12**, 433 (2013).

[88] F. Oliveira, Y. Leterrier, J.-A. Månson, O. Sereda, A. Neels, A. Dommann, and D. Damjanovic, J. Polym. Sci. B Polym. Phys. **52**, 496 (2014).

[89] N. B. Ukah, J. Granstrom, R. R. Sanganna Gari, G. M. King, and S. Guha, Appl. Phys. Lett. **99**, 243302 (2011).

[90] N. B. Ukah, S. P. Senanayak, D. Adil, G. Knotts, J. Granstrom, K. S. Narayan, and S. Guha, J. Polym. Sci. B Polym. Phys. **51**, 1533 (2013).

[91] J. Veres, S. Ogier, G. Lloyd, and D. De Leeuw, Chemistry of materials **16**, 4543 (2004).

[92] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, and B. Batlogg, Applied Physics Letters **90**, 092104 (2007).

[93] C. Koutsiaki, T. Kaimakamis, A. Zachariadis, and S. Logothetidis, Materials Today: Proceedings **19**, 58 (2019).

[94] S. C. Lim, S. H. Kim, J. B. Koo, J. H. Lee, C. H. Ku, Y. S. Yang, and T. Zyung, Applied physics letters **90**, 173512 (2007).

[95] S. Lee, B. Koo, J. Shin, E. Lee, H. Park, and H. Kim, Appl. Phys. Lett. **88**, 162109 (2006).

[96] M. Al-Hashimi, Y. Han, J. Smith, H. S. Bazzi, S. Y. A. Alqaradawi, S. E. Watkins, T. D. Anthopoulos, and M. Heeney, Chem. Sci. **7**, 1093 (2016).

[97] D. Patra *et al.*, Macromolecules **51**, 6076 (2018).

[98] K. H. Park, K. H. Cheon, Y.-J. Lee, D. S. Chung, S.-K. Kwon, and Y.-H. Kim, Chem. Comm. **51**, 8120 (2015).

[99] S. Holliday, J. E. Donaghey, and I. McCulloch, Chem. Mater. **26**, 647 (2014).

[100] M. Barłóg, I. Kulai, X. Ji, N. Bhuvanesh, S. Dey, E. P. Sliwinski, H. S. Bazzi, L. Fang, and M. Al-Hashimi, Org. Chem. Front. **6**, 780 (2019).

[101] S. Khanra, S. V. Vassiliades, W. A. Alves, K. Yang, R. Glaser, K. Ghosh, P. Bhattacharya, P. Yu, and S. Guha, AIP Adv. **9**, 115202 (2019).

[102] J. Barron, S. Attar, P. Bhattacharya, P. Yu, M. Al-Hashimi, and S. Guha, Journal of Materials Chemistry C **10**, 14653 (2022).

[103] Y. Gao, Y. Deng, H. Tian, J. Zhang, D. Yan, Y. Geng, and F. Wang, Adv. Mater. **29**, 1606217 (2017).

[104] Y. Jiang, J. Chen, Y. Sun, Q. Li, Z. Cai, J. Li, Y. Guo, W. Hu, and Y. Liu, Adv. Mater. **31**, 1805761 (2019).

[105] J. W. Rumer, S. Rossbauer, M. Planells, S. E. Watkins, T. D. Anthopoulos, and I. McCulloch, J. Mater. Chem. C **2**, 8822 (2014).

[106] M. Imakawa, K. Sawabe, Y. Yomogida, Y. Iwasa, and T. Takenobu, Appl. Phys. Lett. **99**, 233301 (2011).

[107] C. Rolin, E. Kang, J.-H. Lee, G. Borghs, P. Heremans, and J. Genoe, Nat. Comm. **8**, 14975 (2017).

[108] O. A. Aktsipetrov, A. A. Fedyanin, E. D. Mishina, A. N. Rubtsov, C. W. van Hasselt, M. A. C. Devillers, and T. Rasing, Phys. Rev. B **54**, 1825 (1996).

[109] O. A. Aktsipetrov *et al.*, Phys. Rev. B **60**, 8924 (1999).

[110] T. Manaka, E. Lim, R. Tamura, and M. Iwamoto, Nat. Photon. **1**, 581 (2007).

[111] M. Iwamoto, T. Manaka, and D. Taguchi, Jpn. J. Appl. Phys. **53**, 100101 (2014).

[112] M. Iwamoto, T. Manaka, and D. Taguchi, J. Phys. D: Appl. Phys **48**, 373001 (2015).

[113] T. D. Anthopoulos, D. M. de Leeuw, E. Cantatore, S. Setayesh, E. J. Meijer, C. Tanase, J. C. Hummelen, and P. W. Blom, Applied Physics Letters **85**, 4205 (2004).

[114] K.-J. Baeg, J. Kim, D. Khim, M. Caironi, D.-Y. Kim, I.-K. You, J. R. Quinn, A. Facchetti, and Y.-Y. Noh, ACS Applied Materials & Interfaces **3**, 3205 (2011).

[115] C. Lin, B. Peng, J. Wu, Z. Huang, M. Chen, D. Hu, S. Ke, B. C. K. Tee, and H. Li, Advanced Electronic Materials **8**, 2200557 (2022).

[116] Y. Taur and T. H. Ning, *Fundamentals of modern VLSI devices* (Cambridge university press, 2021).

[117] M. E. Köse, The Journal of Physical Chemistry A **116**, 12503 (2012).

[118] T. Mikie, Y. Iwasaki, and I. Osaka, Materials Chemistry and Physics **287**, 126225 (2022).

[119] C. Sun, C. Zhu, L. Meng, and Y. Li, Advanced Materials **34**, 2104161 (2022).

[120] J. Yang *et al.*, ACS applied materials & interfaces **10**, 23235 (2018).

[121] D. Gedefaw, M. Prosa, M. Bolognesi, M. Seri, and M. R. Andersson, Advanced Energy Materials **7**, 1700575 (2017).

[122] M. S. Oh, D. K. Hwang, K. Lee, W. J. Choi, J. H. Kim, S. Im, and S. Lee, J. Appl. Phys. **102**, 076104 (2007).

[123] R. K. Gupta, K. Ghosh, and P. K. Kahol, Physica E Low Dimens. Syst. Nanostruct. **41**, 617 (2009).

[124] W. E. Bowen, W. Wang, and J. D. Phillips, IEEE Electron Device Lett. **30**, 1314 (2009).

[125] J. Smith, A. Bashir, G. Adamopoulos, J. E. Anthony, D. D. C. Bradley, M. Heeney, I. McCulloch, and T. D. Anthopoulos, Adv. Mater. **22**, 3598 (2010).

[126] R. Wahab, S. G. Ansari, Y. S. Kim, H. K. Seo, G. S. Kim, G. Khang, and H.-S. Shin, Mater. Res. Bull. **42**, 1640 (2007).

[127] C. B. Ong, L. Y. Ng, and A. W. Mohammad, Renew. Sust. Energ. Rev. **81**, 536 (2018).

[128] N. Sekine, C.-H. Chou, W. L. Kwan, and Y. Yang, Org. Electron. **10**, 1473 (2009).

[129] A. Pickett, A. Mohapatra, A. Laudari, S. Khanra, T. Ram, S. Patil, and S. Guha, Organic Electronics **45**, 115 (2017).

[130] S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc. **130**, 17603 (2008).

[131] Y. Sun, J. H. Seo, C. J. Takacs, J. Seifter, and A. J. Heeger, Adv. Mater. **23**, 1679 (2011).

[132] T. R. Bao Foong, S. P. Singh, P. Sonar, Z.-E. Ooi, K. L. Chan, and A. Dodabalapur, J. Mater. Chem. **22**, 20896 (2012).

[133] J. W. Na, Y. S. Rim, H. J. Kim, J. H. Lee, S. Hong, and H. J. Kim, ACS Appl. Mater. Interfaces **9**, 29849 (2017).

[134] M. A. Mahmud, N. K. Elumalai, M. B. Upama, D. Wang, V. R. Gonçales, M. Wright, C. Xu, F. Haque, and A. Uddin, J. Power Sources **383**, 59 (2018).

[135] D. Li, W. Qin, S. Zhang, D. Liu, Z. Yu, J. Mao, L. Wu, L. Yang, and S. Yin, RSC Adv. **7**, 6040 (2017).

[136] A. Pickett, A. A. Mohapatra, S. Ray, Q. Lu, G. Bian, K. Ghosh, S. Patil, and S. Guha, ACS Appl. Electron. Mater. **1**, 2455 (2019).

[137] A. Pickett, A. A. Mohapatra, S. Ray, C. Robledo, K. Ghosh, S. Patil, and S. Guha, MRS Adv. **4**, 1793 (2019).

[138] J. Barron, A. Pickett, J. Glaser, and S. Guha, Electronic Materials **2**, 60 (2021).

[139] J.-H. Lee *et al.*, Nat. Med. **13**, 95 (2007).

[140] K. Maaz, A. Mumtaz, S. K. Hasanain, and A. Ceylan, J. Magn. Magn. **308**, 289 (2007).

[141] S. M. Ansari, K. C. Ghosh, R. S. Devan, D. Sen, P. U. Sastry, Y. D. Kolekar, and C. V. Ramana, ACS Omega **5**, 19315 (2020).

[142] Y.-w. Jun, J.-w. Seo, and J. Cheon, Acc. Chem. Res **41**, 179 (2008).

[143] N. Sanpo, C. C. Berndt, C. Wen, and J. Wang, Acta Biomater. **9**, 5830 (2013).

[144] S. Amiri and H. Shokrollahi, Mater. Sci. Eng. C **33**, 1 (2013).

[145] J. Gallo, N. J. Long, and E. O. Aboagye, Chem. Soc. Rev. **42**, 7816 (2013).

[146] X. Zeng *et al.*, Nanoscale **9**, 7493 (2017).

[147] J. Barron, J. Lee, and S. Guha, Journal of Materials Research **37**, 1547 (2022).

[148] J. H. Jung, S. Kim, H. Kim, J. Park, and J. H. Oh, Small **11**, 4976 (2015).

[149] Y. Zang, F. Zhang, D. Huang, C.-a. Di, and D. Zhu, Adv. Mater. **27**, 7979 (2015).

[150] S. Khanra, M. Abdullah-Al Mamun, F. F. Ferreira, K. Ghosh, and S. Guha, ACS Appl. Nano Mater. **1**, 1175 (2018).

[151] S. Sun, H. Zeng, D. B. Robinson, S. Raoux, P. M. Rice, S. X. Wang, and G. Li, J. Am. Chem. Soc. **126**, 273 (2004).

[152] S. C. Lim, S. H. Kim, J. B. Koo, J. H. Lee, C. H. Ku, Y. S. Yang, and T. Zyung, Appl. Phys. Lett. **90**, 173512 (2007).

[153] M. R. Beaulieu, J. K. Baral, N. R. Hendricks, Y. Tang, A. L. Briseño, and J. J. Watkins, ACS Appl. Mater. Interfaces **5**, 13096 (2013).

[154] Y. Zhou, S.-T. Han, Z.-X. Xu, X.-B. Yang, H.-P. Ng, L.-B. Huang, and V. A. L. Roy, J. Mater, Chem. **22**, 14246 (2012).

[155] Y. Zhou, S.-T. Han, Z.-X. Xu, and V. A. L. Roy, J. Mater, Chem. **22**, 4060 (2012).

[156] J. Kim, S. H. Lim, and Y. S. Kim, J. Am. Chem. Soc. **132**, 14721 (2010).

[157] J. Kim, J. Kim, Y. Seol, T. Kim, and N.-E. Lee, J. Nanosci. Nanotechnol. **16**, 11335 (2016).

[158] B. Canimkurbey, Ç. Çakirlar, S. Piravadili Mucur, M. Yasin, and S. Berber, J. Mater Sci: Mater. Electron. **30**, 18384 (2019).

[159] K. T. McCarthy, A. F. Hebard, and S. B. Arnason, Phys. Rev. Lett. **90**, 117201 (2003).

[160] G. Catalan, D. O'Neill, R. M. Bowman, and J. M. Gregg, Appl. Phys. Lett. **77**, 3078 (2000).

[161] N. S. Negi, K. Bala, A. Yadav, and R. K. Kotnala, J. Appl. Phys. **117**, 164101 (2015).

[162] H. Zang, J. Wang, M. Li, L. He, Z. Liu, D. Zhang, and B. Hu, J. Phys. Chem. B **117**, 14136 (2013).

[163] J. Rumer, S. Rossbauer, M. Planells, S. Watkins, T. Anthopoulos, and I. McCulloch, Journal of Materials Chemistry C **2**, 8822 (2014).

[164] N. M. Triet, T. Q. Trung, N. T. D. Hien, S. Siddiqui, D.-I. Kim, J. C. Lee, and N.-E. Lee, Nano Research **8**, 3421 (2015).

[165] S. Singh and N. Khare, Applied Surface Science **364**, 783 (2016).

VITA

John Thomas Barron was born in Mattoon, Illinois in 1995. He attended Herrin High School where he was first exposed to the prospect of becoming a researcher through a program with Southern Illinois University called Project SEED, in which he got to spend the summer participating in day-to-day lab work with a member of their biochemistry department.

John later pursued a bachelor's degree in physics from Southern Illinois University, during which he spent time as an undergraduate research assistant to the laboratory of Dr. Saikat Talapatra. It was during a summer research program in 2015 that John also first visited the University of Missouri, working in the laboratory of Dr. Peter Pfeifer. John graduated in 2017 with his bachelor's degree, awarded magna cum laude and an honor's degree.

He began his graduate program at the University of Missouri in the Fall of 2017 and joined Dr. Suchi Guha's research team in May of 2018. He later earned his master's degree in May of 2019, completed his comprehensive exam in October of 2020, and will complete his doctorate education in May of 2023.