An Improved Data-Driven Memristor Model Accounting for Sequences Stimulus Features

***Abstract*—The natural similarity between the emerging memristive technology and synapses makes memristor a promising device in the spiking input based neuromorphic systems. However, while asynchronous signal processing relies on memristor's response under the pulses stimulus, hardly any memristor models take the impact of sequences features on device behaviour into consideration. This paper proposes an optimized data-driven compact memristor model where the boundary of its internal state variable-resistive state (RS) is modelled with pulse amplitude and pulse width based on characterisation data. The model has been developed in Verilog-A, simulated and verified in Cadence Virtuoso Electronic Design Automation (EDA) tools. Based on the simulation, we further analyse and introduce a new concept of "Effective Time Window". Along with the observed pulse width modulated resistance, more potential circuit applications can be implemented based on a more realistic memristor switching behaviour.**

***Index Terms*—Memristor, Resistive switching device characterisation, Modelling, Memristor Verilog-A model.**

I. Introduction

The memristor, demonstrating the intrinsic synaptic-like features [1]–[3], is regarded as an ideal device for the realization of artificial synapses. To facilitate the development of memristor-based neuromorphic systems [4]–[6], the availability of computationally efficient models that are capable of precisely capturing memristors' physical behaviour is critical. A variety of models has been proposed and the main difference in these models is the different implementations of internal state variables with their boundaries (i.e. Window functions). In the ion drift based models such as [7]–[10], the width of the highly doped region w is used as the internal state variable. To model other features observed in many fabricated memristors such as non-linearity, threshold voltage, volatility, etc., models based on different physical principles were proposed with various internal states such as magnetic flux [11], the area index [12], the memory conductance [13], Simmons tunnel barrier width [14], narrow tunnel barrier [15], the normalized conductivity index [16], the effective electric tunnel width in TEAM model [17], and the stimulus voltage in the empirical models [18], [19]. More empirical models were developed from large-scale experimental data [20], [21] where the internal variable resistive state (RS) is defined based on experiments.

In the meantime, a number of window functions [8], [10], [16], [17], [22], that bound the internal state variables and alleviate the bounds issues were also proposed along with the models. In different models, various mathematical expressions are taken as the window functions, according to the state variables, to fit to the practical memristor characterisation data.

Even though the existing models are quite broad to model the dynamic behaviour of memristive systems, hardly any implementations of internal states variables or the corresponding window functions take the characteristics of the continuously repetitive pulsing inputs into account. The behaviour under such stimulus is essential for memristive neuromorphic systems, since the signal resembling nerve impulses can empower novelties into circuits such as spike-timing-dependent plasticity [23], unsupervised learning [6] and associate memory [24], etc. To provide reliable simulation results, it is critically requiring the modelling of memristors for spiking inputs, which uncovers the correlations between memristors' behaviour and the parameters of pulse sequences.

In this work, we propose an improved data-driven model with a more detailed description on the temporal evolution of the internal state variable RS and the RS boundary, using pulse amplitude and pulse width, based on real measurement results. The paper is organized as follows, Section II describes a specialised characterisation flow for memristor spikes' response features. Section III presents statistical analysis and the quantitative modelling. Section IV shows an improved data-driven Verilog-A model, continued with model simulation and verification in the EDA where a new concept of "Effective Time Window" is defined within. Finally this paper is concluded in Section V.

II. characterisation Process and Results

A reliable model needs data from a fully characterized memristor, Figure 1 shows the pulse stimulus pattern used in the characterisation routine of memristor's pulse sequences response. The characterisation flow covers the measurements on the effects of both positive and negative pulse sequence parameters: write pulses number of every voltage step, the amplitude of the pulses, the pulse width and the pulse interval.

The spiking features characterisation routine is carried out after the device-under-test (DUT) is successfully electroformed. The amplitude of read pulses V_r is set as $200mV$ and the internal state variable RS is experimentally defined as the memristance measured under the read pulses through out the work. The number of write pulses N is set to ensure the RS at each voltage step being able to reach saturation(i.e. RS boundary). The statistical definition of RS boundary will be explained in Section III. Considering the stochastic behaviour of memristors and the instrumental noise, a number of M read pulses are applied between each two write pulses to increase the characterisation reliability by calculating the average value.

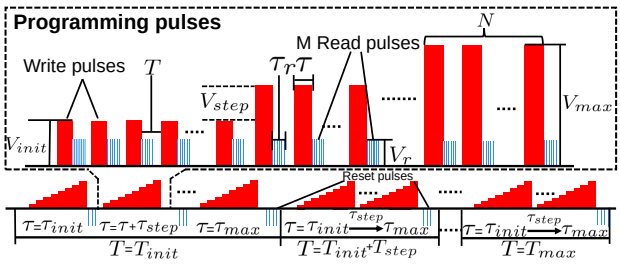

Fig. 1. Positive pulse stimulus pattern used in the characterisation flow. A series of ramp pulse sequences is applied on the DUT, sweeping the pulse interval T from an initial pulse interval T_{init} to a maximum pulse interval T_{max} at a pulse interval step T_{step} and sweeping the pulse width τ from an initial value τ_{init} to a maximum value τ_{max} at a step of τ_{step}. In each pulse sequence, there are several voltage steps from an initial value V_{init} to the maximum amplitude V_{max} at a step of V_{step}. Each step has N write pulses between which are M read pulses. The read pulses' amplitude is V_r and their pulse width τ_r is automatically set according to T.

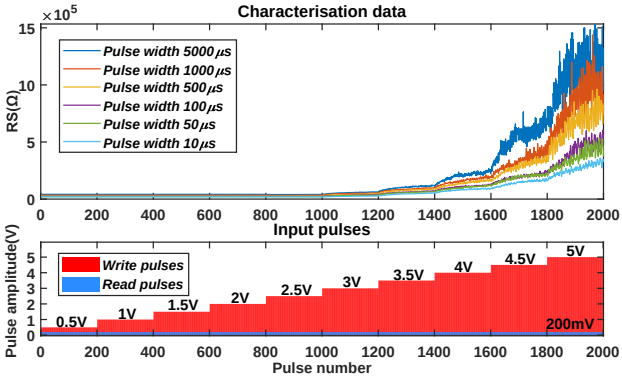

Fig. 2. Example data from data set 1 (pulse interval=200μs). The pulse stimulus waveform used in the characterisation process is shown at the bottom. 6 sets of data corresponding to different stimulus pulse width: 10μs, 50μs, 100μs, 500μs, 1000μs, 5000μs are selected to present at the top.

After each ramp pulse sequence, the DUT is reset to minimum RS by inverting the polarity of pulses. Negative characterisation is carried out under the negative pulse stimulus which shares a similar pattern as in Figure 1. To avoid random error and alleviate experimental bias, replicated trials of polarity alternating characterisation are required and multiple memristor samples should be randomly selected to characterise. The resistive switching behaviour based on applied pulse sequences and corresponding pulse parameters are recorded after each programming cycle.

With the routine introduced above, our in house fabricated $Pt/TiO_2/Pt$ memristors are characterised and twenty data sets containing the RS response and corresponding pulse stimulation data are obtained. Data sets 1-10 are under positive stimulation. The pulse interval covers from $1ms$ to $10ms$ at a step of $1ms$. Pulse width covers the values from $10\mu s$ to $5000\mu s$ and pulse amplitude is swept varying from $0.5V$ to $5V$ at a step of $0.5V$. For each voltage step, a pulse sequence of 200 pulses is applied. The rest of the ten data sets correspond to negative stimulus with the same sweeping parameters. An example of measurement results is shown in Figure 2.

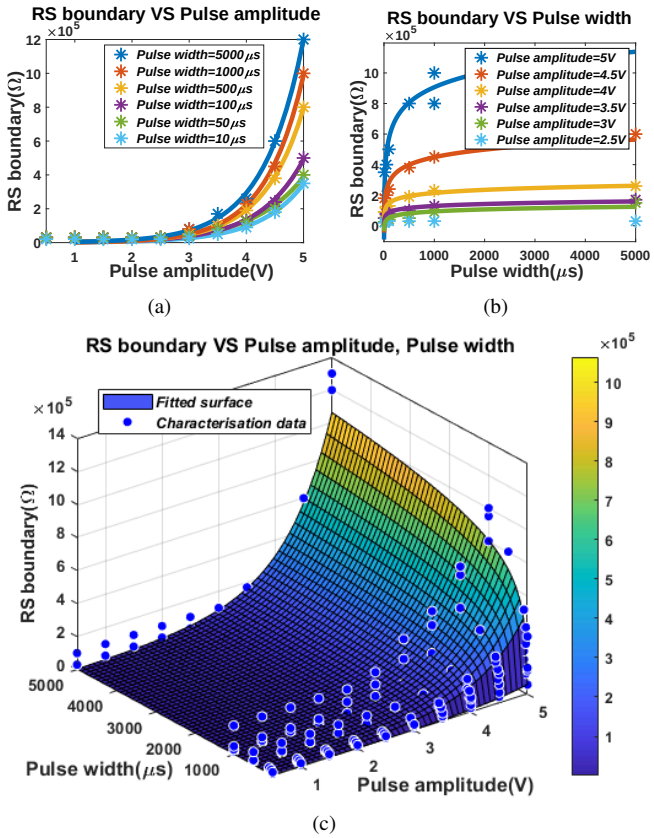

Fig. 3. Modelling process of RS boundary (a) Selected RS boundary and corresponding stimulus amplitude data in data set 1 (pulse interval=200μs). The data points are fitted with $a \cdot exp(b \cdot x)$ showing in curves. Different colors represent the data from different programming cycles of the stimulus pulse width 10μs,20μs...5000μs. (b) Selected RS boundary and corresponding stimulus pulse width data in data set 1 (pulse interval=200μs). The data points are fitted with $a \cdot ln(x+1)+b$ showing in curves. Different colors represent the data from different voltage steps $0V$,$0.5V$,$1V$ ... $5V$. (c) Selected measurement data of RS boundary, corresponding pulse amplitude and pulse width from data set 1-4. The data points are fitted with $a \cdot exp(b \cdot x) \cdot (ln(y+1)+c)$ which presents as the surface.

III. RS Boundary Modelling

To further analyse the data, a suitable sliding window of N-dependent size is applied to the time series of each voltage step. Autocorrelation function (ACF) and Augmented Dickey-Fuller Test (ADF) are used to classify the stationary series in the shifting window with a fixed lag. RS boundary is then defined as the mean value of RS from the beginning of stationary segment to the end of the step. Interpolation method is used to fit all the data sets where it presents an exponential function between RS boundary and voltage amplitude, and a logarithm function between RS boundary and pulse width. Figure 3(a) shows the selected data set 1 and $a \cdot exp(b \cdot x)$ is fitted to the RS boundary and voltage amplitude. The average R-square of all fittings for pulse width is 0.98. Similarly, Figure 3(b) shows the fitting of RS boundary and pulse width with $a \cdot ln(x+1)+b$, and the average R-square of all fittings for amplitude is 0.917.

To verify the null hypothesises that parameters b is weakly

TABLE I
HYPOTHESIS TESTS RESULT

Correlation \ Test		Pearson	Spearman
b-pulse width	P	0.14	0.10
$a \cdot exp(b \cdot x)$	ρ	0.33	0.38
b-amplitude	P	0.78	0.99
$a \cdot ln(x+1)+b$	ρ	-0.069	0.17×10^{-2}

related to pulse width in RS boundary-amplitude fitting and weakly related to amplitude in RS boundary-pulse width fitting, hypothesis tests are used to evaluate the correlation levels. As the results shown in Table I, all P-values are greater than the significance level 0.05 and the correlation coefficients ρ are low in all tests, indicating the null hypothesises are valid. Thus the simplified expression (1) can be used to model RS boundary with pulse width and pulse amplitude. The generated fitting surface is shown in Figure 3(c) and the goodness of the fitting for all the data sets can reach a high R-square of 0.8438 and a % RMSE of 32.5%.

$$r_{p,n}(v_{p,n},\tau_{p,n}) = \begin{cases} r_{p,a}e^{r_{p,b}v_p}(ln(1+\tau_p)+r_{p,c}) & v>0 \\ r_{n,a}e^{r_{n,b}v_n}(ln(1+\tau_n)+r_{n,c}) & v\le 0 \end{cases} \tag{1}$$

The proposed RS boundary modelling work is applied in the data driven Verilog-A model proposed in [20] and a more precise RS expression can be solved analytically in (2) under a constant bias voltage V_b from the improved time derivative of the state variable dRS/dt, where $R0$ is the initial RS, t is the duration of the constant bias, $s(V_b)$ is a constant value of switching sensitivity, and $r_{p,n}(V_b,\tau_{p,n})$ can be derived with given pulse width. The extracted parameters from the characterisation data are listed in Table II.

$$RS(t)|V_b = \begin{cases} \frac{R0+s_p(V_b)\cdot r_p(V_b,\tau_p)(r_p(V_b,\tau_p)-R0)\cdot t}{1+s_p(V_b)\cdot(r_p(V_b,\tau_p)-R0)\cdot t} & v>0 \\ \frac{R0+s_n(V_b)\cdot r_n(V_b,\tau_n)(r_n(V_b,\tau_n)-R0)\cdot t}{1+s_n(V_b)\cdot(r_n(V_b,\tau_n)-R0)\cdot t} & v\le 0 \end{cases} \tag{2}$$

TABLE II
EXTRACTED PARAMETER VALUES FITTING THE $Pt/TiO_2/Pt$ MEMRISTOR WITH THE IMPROVED MODEL

Parameter	Positive polarity value($_p$)	Negative polarity value($_n$)
a	0.88	0.39
b	1.08	1.78
A	6.48×10^{-3}	-145.7
t	3.65	3.04×10^{6}
r_a	313.20	1.58×10^{11}
r_b	1.25	7.87
r_c	-1.94	14.34

IV. IMPLEMENTATION IN VERILOG-A MODEL AND ITS SIMULATION RESULTS

The model is implemented in Verilog-A and the logic control is improved from [21]. More cases are considered when updating the RS. In order to clarify the logic of calculating RS, we present a short description of all the cases that the model will be encountered and corresponding RS output.

- Case 1: The stimulus amplitude $\le 200mV$. RS will remain the same. Current is only determined by the applied voltage.
- Case 2: The stimulus amplitude $> 200mV$. Current RS is outside RS boundary $R0 \ge r_p$ or $R0 \le r_n$. RS will remain the same.
- Case 3: The stimulus amplitude $> 200mV$. Current RS and estimated RS are within RS boundary $r_n \le RS_{tem} \le r_p$. RS will be updated with the estimated value.
- Case 4: The stimulus amplitude $> 200mV$. Current RS is within RS boundary but estimated RS is outside the boundary. RS will be updated with the boundary value.

The algorithm is presented in Algorithm 1 where the parameter $R0$ is the initial RS value of each iteration, $time$ represents the absolute time of the end of each iteration, τ_{begin} is used to record the absolute time when a pulse starts. After the parameters are initialised at the beginning of every simulation, the model will enter iterations where RS boundary $r_{p,n}$ and the estimated RS RS_{tem} are calculated from (1) and (2) respectively based on variables $\tau_{p,n}$, $v_{p,n}$, and the simulation time of current iteration dt. Subsequently, the value of RS_{tem} is assigned to RS based on the boundary conditions discussed above and the current flowing through the device is determined.

Algorithm 1 Algorithm for improved memristor model

Input: $v_{p,n} \leftarrow$ *external stimulus V*
Output: *current I*
  Initialisation:
    $R0$ = R_{init};$time = 0$;$\tau_{begin} = 0$;$\tau_{p,n} = 0$;
  Iteration:
  for *time* $<$ *simulation time* **do**
    Variable Calculation:
      $dt = \$abstime - time$, $\tau_{p,n} = \$abstime - \tau_{begin}$;
    RS Calculation:
      $r_{p,n} = r_{p,n}(v_{p,n},\tau_{p,n})$, $RS_{tem} = RS(dt)$;
    Boundary Cases Classification:
      $RS \overset{boundary\ conditions}{\longleftarrow} RS_{tem}$;
    Output Current Calculation:$I = G(RS,v)v$ [21]
    Update Variables:
      $\tau_{begin} = \$abstime@cross(v_{p,n} = 0)$;
      $time = \$abstime$;
      $R0 = RS$;
  end for
  return *I*

The model is simulated in EDA tools and Figure 4 presents the comparison between characterisation data and simulation results. In addition, as shown in Figure 2, the stochasticity in memristors increases when RS enters high resistance state, the %RMS fitting error equals to 5.41% when RS varies from $50k\Omega$ to $700k\Omega$. The %RMS fitting error for $10k\Omega$ to $17k\Omega$ is

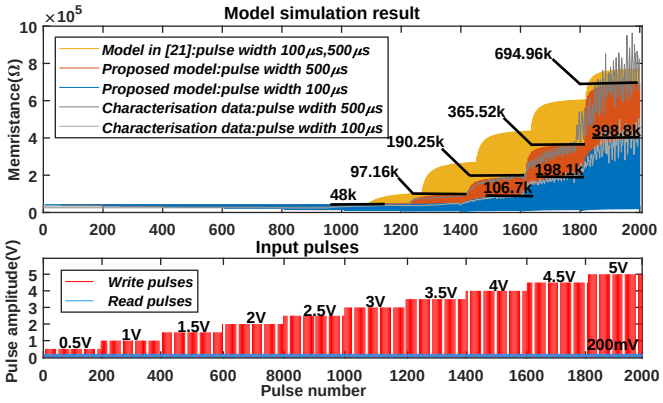

Fig. 4. The simulation results of the proposed model and model in [21]. The applied pulse stimulus pattern (bottom) is the same as in Figure 2. The models are simulated under the stimulus of $100\mu s$ and $500\mu s$ as shown in blue (top). Corresponding characterisation data of $Pt/TiO_2/Pt$ devices is presented in grey to compare with the simulation results. RS boundary of each voltage step is marked to indicate the trend with different amplitude and pulse width.

only 2.1%, less than the %RMS fitting error of 2.18% in [21]. Figure 4 also compares the different simulation results of the model proposed in [21] and the improved model in this work. The model in [21] presents the change of RS boundary in a linear form whereas the RS boundary in this proposed model presents an exponential relation under the same ramp pulses stimulus. Furthermore, as shown in Figure 4, while the model in [21] reacts same under the stimulus of different pulse width, the improved model shows higher RS and RS boundary for the stimulus of larger pulse width as it takes the effect of pulse width on memristor's behavior into account. The improved model with the pulse width modulated RS provides a more realistic solution in circuit design.

During the characterisation process, RS has been directly linked with the whole pulse width, but the model still needs to show the memristors' behaviour inside a single pulse, without knowing the entire pulse width. Based on the simulation results, here we introduce a new concept of Effective Time Window to explain the process. As Figure 5 (a) shows, when the model is iterating in a pulse, the accumulative pulse width $\tau(i)$ will increase with the iteration number i, from $\tau(i) = 0$ to the end of the pulse $\tau(i) = pulse\ width$. According to the logarithm correlation of RS-pulse width, RS boundary will also increase with the updated $\tau(i)$ from a value close to 0. As a result, RS will firstly remain unchanged when it is outside the RS boundary and at a certain time point when

$$\tau_{th,p,n}(RS)|V_b = r_{p,n}^{-1}(RS, V_b) \tag{3}$$

which makes the boundary to include the RS, RS will then be affected to change in which the time region is defined as Effective Time Window. The time region before the Effective Time Window in which RS remains stable is defined as Stable Time Window. In Figure 5(b), we compare the simulation result of the improved model with the model in [21] under the same input pulses stimulation. The memristance of the model in [21] increases continuously without showing the

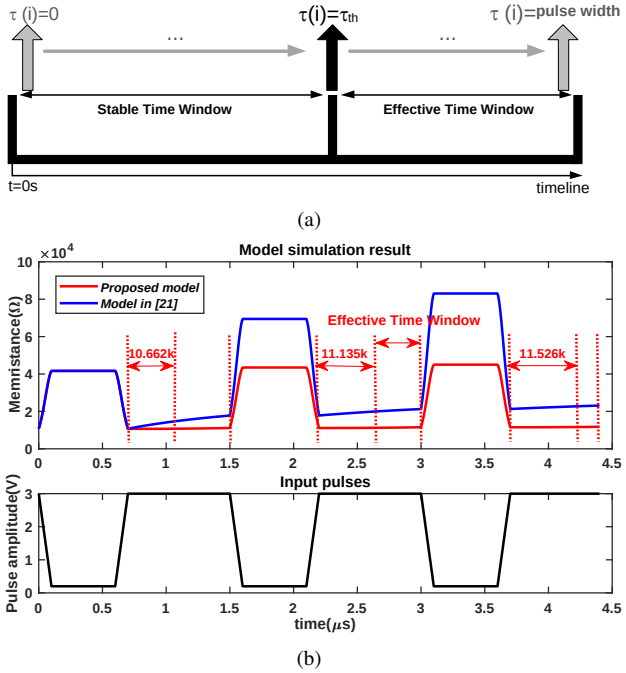

Fig. 5. Demonstration of Effective Time Window (a) Effective Time Window in a Pulse. Pulsing event is happening along the timeline. The model samples the accumulative pulse width as time increasing which is represented by $\tau(i)$. Effective Time Window and Stable Time Window are marked. (b) Comparison between the simulation results of the model proposed in [21] and our proposed model (top) under the stimulus of input pulses (bottom). The unchanged segments of memristance in each pulse is marked with their values to reflect the signature but weak effects of Stable Time Window and Effective Time Window in the proposed model.

Stable Time Window or Effective Time Window. However, in the simulation of our model, memristance will remain the same ($10.662k$, $11.135k$, $11.526k$) at the very beginning of each pulse. After a while the memristance increases again indicating the model has stepped into the Effective Time Window. Notably, as the RS approaching to the RS boundary, the Effective Time Window is shrinking. The introduced concepts provide a possible explanation for how a time related factor would affect RS boundary inside a pulse.

V. CONCLUSION

This work, for the first time, presents an improved data-driven memristor model which accounts for the features of continuous pulses sequences. The empirical model quantitatively evaluates the impact of pulse amplitude and pulse width on the internal state boundary. With a customized characterisation routine, the parameters in the model are extracted from the measurement data of $Pt/TiO_2/Pt$ memristors. The model is implemented in Verilog-A with a more comprehensive operational logic. From the simulation results in Cadence EDA tools, the model presents a more realistic behaviour under spiking stimulus compared with the measurement data. With the characteristics embodied in the model, Effective Time Window and pulse width modulated RS, we anticipate the proposed model provides a more realistic switching behaviour, and thus enables more novel applications in circuits design.

REFERENCES

[1] G. S. Snider, "Cortical computing with memristive nanodevices," *SciDAC Review*, vol. 10, pp. 58–65, 2008.

[2] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano letters*, vol. 10, no. 4, pp. 1297–1301, 2010.

[3] T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, and B. Linares-Barranco, "Stdp and stdp variations with memristors for spiking neuromorphic learning systems," *Frontiers in neuroscience*, vol. 7, p. 2, 2013.

[4] A. Serb, J. Bill, A. Khiat, R. Berdan, R. Legenstein, and T. Prodromakis, "Unsupervised learning in probabilistic neural networks with multi-state metal-oxide memristive synapses," *Nature communications*, vol. 7, no. 1, pp. 1–9, 2016.

[5] G. Indiveri, B. Linares-Barranco, R. Legenstein, G. Deligeorgis, and T. Prodromakis, "Integration of nanoscale memristor synapses in neuromorphic computing architectures," *Nanotechnology*, vol. 24, no. 38, p. 384010, 2013.

[6] E. Covi, S. Brivio, A. Serb, T. Prodromakis, M. Fanciulli, and S. Spiga, "Analog memristive synapse in spiking networks implementing unsupervised learning," *Frontiers in neuroscience*, p. 482, 2016.

[7] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[8] Z. Biolek, D. Biolek, and V. Biolkova, "Spice model of memristor with nonlinear dopant drift." *Radioengineering*, vol. 18, no. 2, 2009.

[9] A. Rak and G. Cserey, "Macromodeling of the memristor in spice," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 4, pp. 632–636, 2010.

[10] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *European Journal of physics*, vol. 30, no. 4, p. 661, 2009.

[11] D. Batas and H. Fiedler, "A memristor spice implementation and a new approach for magnetic flux-controlled memristor modeling," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 250–255, 2010.

[12] T. Chang, S.-H. Jo, K.-H. Kim, P. Sheridan, S. Gaba, and W. Lu, "Synaptic behaviors and modeling of a metal oxide memristive device," *Applied physics A*, vol. 102, no. 4, pp. 857–863, 2011.

[13] Y. Shang, W. Fei, and H. Yu, "Analysis and modeling of internal state variables for dynamic effects of nonvolatile memory devices," *IEEE transactions on circuits and systems I: Regular papers*, vol. 59, no. 9, pp. 1906–1918, 2012.

[14] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching dynamics in titanium dioxide memristive devices," *Journal of Applied Physics*, vol. 106, no. 7, p. 074508, 2009.

[15] H. Abdalla and M. D. Pickett, "Spice modeling of memristors," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. IEEE, 2011, pp. 1832–1835.

[16] C. Yakopcic, T. M. Taha, G. Subramanyam, and R. E. Pino, "Generalized memristive device spice model and its application in circuit design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 8, pp. 1201–1214, 2013.

[17] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Team: Threshold adaptive memristor model," *IEEE transactions on circuits and systems I: regular papers*, vol. 60, no. 1, pp. 211–221, 2012.

[18] R. Berdan, C. Lim, A. Khiat, C. Papavassiliou, and T. Prodromakis, "A memristor spice model accounting for volatile characteristics of practical reram," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 135–137, 2013.

[19] Q. Li, A. Serb, T. Prodromakis, and H. Xu, "A memristor spice model accounting for synaptic activity dependence," *PloS one*, vol. 10, no. 3, p. e0120506, 2015.

[20] I. Messaris, A. Serb, A. Khiat, S. Nikolaidis, and T. Prodromakis, "A compact verilog-a reram switching model," *arXiv preprint arXiv:1703.01167*, 2017.

[21] I. Messaris, A. Serb, S. Stathopoulos, A. Khiat, S. Nikolaidis, and T. Prodromakis, "A data-driven verilog-a reram model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3151–3162, 2018.

[22] T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," *IEEE transactions on electron devices*, vol. 58, no. 9, pp. 3099–3105, 2011.

[23] C. Zamarreño-Ramos, L. A. Camuñas-Mesa, J. A. Pérez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, and B. Linares-Barranco, "On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex," *Frontiers in neuroscience*, vol. 5, p. 26, 2011.

[24] J. Sun, G. Han, Z. Zeng, and Y. Wang, "Memristor-based neural network circuit of full-function pavlov associative memory with time delay and variable learning rate," *IEEE Transactions on Cybernetics*, vol. 50, no. 7, pp. 2935–2945, 2020.