Imperial College London

Department of Electrical and Electronic Engineering

Ultra-Low Power Mixed-Signal Frontend for Wearable EEGs

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A Thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy in Electrical and Electronic Engineering of Imperial College London and the Diploma of Imperial College London.

Declaration of Originality

It is to certify that all the material in this thesis is my work, and I have appropriately acknowledged the source of any work that is not my own. This thesis was not and will not be submitted to any other university or institution for fulfilling the requirements of a degree.

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Abstract

Electronics circuits are ubiquitous in daily life, aided by advancements in the chip design industry, leading to miniaturised solutions for typical day to day problems. One of the critical healthcare areas helped by this advancement in technology is electroencephalography (EEG). EEG is a non-invasive method of tracking a person's brain waves, and a crucial tool in several healthcare contexts, including epilepsy and sleep disorders. Current ambulatory EEG systems still suffer from limitations that affect their usability. Furthermore, many patients admitted to emergency departments (ED) for a neurological disorder like altered mental status or seizures, would remain undiagnosed hours to days after admission, which leads to an elevated rate of death compared to other conditions. Conducting a thorough EEG monitoring in early-stage could prevent further damage to the brain and avoid high mortality. But lack of portability and ease of access results in a long wait time for the prescribed patients.

All real signals are analogue in nature, including brainwaves sensed by EEG systems. For converting the EEG signal into digital for further processing, a truly wearable EEG has to have an analogue mixed-signal front-end (AFE). This research aims to define the specifications for building a custom AFE for the EEG recording and use that to review the suitability of the architectures available in the literature. Another critical task is to provide new architectures that can meet the developed specifications for EEG monitoring and can be used in epilepsy diagnosis, sleep monitoring, drowsiness detection and depression study.

The thesis starts with a preview on EEG technology and available methods of brainwaves recording. It further expands to design requirements for the AFE, with a discussion about critical issues that need resolving. Three new continuous-time capacitive feedback chopped amplifier designs are proposed. A novel calibration loop for setting the accurate value for a pseudo-resistor, which is a crucial block in the proposed topology, is also discussed. This pseudoresistor calibration loop achieved the resistor variation of under 8.25%.

The thesis also presents a new design of a curvature corrected bandgap, as well as a novel DDA based fourth-order Sallen-Key filter. A modified sensor frontend architecture is then proposed, along with a detailed analysis of its implementation. Measurement results of the AFE are finally presented. The AFE consumed a total power of 3.2μA (including ADC, amplifier, filter, and current generation circuitry) with the overall integrated input-referred noise of

0.87μV-rms in the frequency band of 0.5-50Hz. Measurement results confirmed that only the proposed AFE achieved all defined specifications for the wearable EEG system with the smallest power consumption than state-of-art architectures that meet few but not all specifications. The AFE also achieved a CMRR of 131.62dB, which is higher than any studied architectures.

-To my family-

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I could not have been able to finish this PhD without the help of a lot of people.

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Well, if I have forgotten any names then please forgive me as it was not intentional.

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List of Acronyms

AAF	anti-aliasing filter
ADC	analogue-to-digital converter
AFE	analogue front-end
ASIC	application specific integrated circuit
AZ	auto-zeroing
BGA	ball grid array package
BPF	band-pass filter
CCFEA-I	Chopper based capacitive feedback EEG amplifier using modified pseudo-resistors (CCFEA-I)
CCFEA-II	Chopper based capacitive feedback EEG amplifier using duty-cycled resistors
CCFEA-III	Chopped capacitive feedback EEG amplifier with pseudo-resistor calibration loop and digital offset correction
CDS	correlated double sampling
CMFB	common-mode feedback
CMRR	common-mode rejection ratio
CTAT	complementary to absolute temperature
DAC	digital-to-analogue converter
DCR	duty cycled resistor
DDA	differential-difference amplifier
DSL	dc servo loop
EEG	electroencephalography

EM	electromagnetic
ENOB	effective number of bits
ESD	electrostatic discharge
FFT	fast fourier transform
FOM	figure of merit
HPF	high-pass filter
IC	integrated circuit
IOS	input offset storage
LPF	low-pass filter
MDCR	multi-rate duty cycled resistor
NEF	noise efficiency factor
OOS	output offset storage
OTA	operational transconductance amplifier
PCB	printed circuit board
PEF	power efficiency factor
PFB	positive feedback loop
PR	pseudoresistor
PSD	power spectral density
PSRR	power supply rejection ratio
PTAT	proportional to absolute temperature
RMS	root mean square

RRL	ripple rejection loop
SAR	successive approximation register
SC	switched capacitor
SFDR	spurious free dynamic range
S/H	sample-and-hold
SINAD	signal to noise and distortion ratio
SNR	signal-to-noise ratio
SOI	silicon on insulator
THD	total harmonic distortion
VDS	drain-to-source voltage
VGS	gate-to-source voltage
VLSI	very-large-scale integration

Chapter 1 - Electroencephalography

1.1 Overview

Electroencephalography, or EEG, refers to a method for recording the electrical activity of a person's brain through the scalp over a period of time [1-7]. This is done both for research purposes and the evaluation of various neurological disorders. EEG imposes a more significant challenge than other bioelectrical recording methods due to their high complexity, non-linearity and low signal to noise ratio [1],[7]. EEG offers three distinct advantages over other methods of brain processes sensing: 1) It is a non-invasive procedure, so measurements can be conducted on human subjects without the need for surgery; 2) It has a very high time resolution, in several milliseconds, which make it easier to track temporal dynamics of the brain processes; 3) It is relatively inexpensive. Advantages associated with EEG provided the use of EEG in a wide range of applications ranging from sleep monitoring, epilepsy monitoring to alertness detection or Brain-Computer Interfaces (BCI).

This chapter briefly discusses the history of EEG, physiology, recording methods, application areas, and a brief summary of the evolution of EEG recording systems. An analysis of the motivation for utilising ambulatory techniques, rather than traditional clinical recordings and the need for wearable EEG systems, is also presented.

1.2 History and evolution of electroencephalography

In 1875, Richard Caton discovered the existence of the electrical signals in the brain by examining the exposed brains of rabbits and monkeys [2],[7]. Later on, Hans Berger became the first researcher to record the electrical activity from the human scalp. In 1924, he amplified the brain signals recorded from scalp using double coil galvanometer and non-polarizable pad electrodes. He later published his finding in 1929 journal article titled "Über das Elektroenkephalogramm des Menschen". In the study, he reported a brain oscillation of 10Hz, which he called the alpha wave, observed in subjects in a relaxed state and closed eyes. During this time, a group in the institute of brain research in Berlin-Bush led by A. E. Kornmuller collaborated with J. F. Toennies. This group provided a more precise recording of the EEG signals. J. F. Toennies is attributed to the development of the first ink-writing biological

amplifier for recording brain potentials. While as a fellow of the Rockefeller Foundation in 1932, he designed a differential amplifier for EEG recording.

It was Kornmuller who first recognized the significance of recording from a large number of electrodes. He worked together with M. H. Fischer and H. Lowenbach to record EEG from the cortex of animals after poisoning with convulsive substances. It was the first EEG work focussed on epileptic manifestations and the first demonstration of epileptic spikes.

Later in 1934, Lord Edgar Adrian (1889-1977) at Cambridge confirmed the findings of Berger. From thereon, EEG triggered a revolution in the study of brain functioning and dynamics [1-7].

1.3 Basics of bioelectrical signals and nature of EEG

Nerve cells, or neurones, have visible contrast in the detailed structure but are typically constituted of a cell body, containing a nucleus, a long nerve fibre called axon which carries electrical nerve impulses away from the cell body, and many short branches called dendrites which bring the impulses towards the cell body (see Figure 1.1)[1].

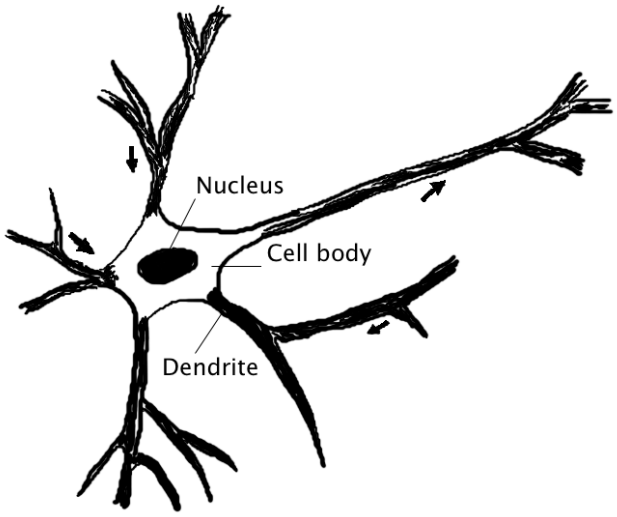

Figure 1.1 Nerve cell (a neuron) structure.

There is a higher concentration of potassium (K+) within a neurone and a lower concentration of sodium (Na+), and the reverse is true for extracellular fluid. The cell membrane is much more permeable to potassium ions than to sodium ions. When these ions diffuse down their concentration gradients, an electric potential is set up across the cell membrane. The membrane

is polarized when negative potential inside the membrane with respect to the outside becomes large enough to prevent potassium ions from escaping. This occurs at a resting potential of around -70mV. Under certain circumstances, the membrane potential is reduced, reaching a certain threshold when ionic permeabilities change, and the cell membrane becomes impermeable to potassium but allows sodium to move in freely. When the inside of the cell membrane becomes 30mV positive with respect to the outside, the selective permeabilities restores its original state, producing an overshoot that lasts about 1ms, called action potential. The action potential then transmits the signal through the axon to other nerve cells. The points of contact from axon to dendrites and cell bodies of other neurons are called synapses. When an action potential reaches a synapse, a chemical substance called a 'neurotransmitter' is released, which diffuses in the membrane of the adjacent post-synaptic neuron and brings electrical changes called post-synaptic potentials. They are about 5-10mV in amplitude and last about 10ms [1].

The effects of the various synapses across the cell body is averaged out. Based on the threshold they reach, they might result in depolarising or excitatory postsynaptic potentials (ESPs), triggering off action potentials with some synapses producing polarising effects or inhibitory postsynaptic potentials (IPSPs).

An electrode connected to the scalp detects the electrical signal caused by the synchronous activity of thousands of neurons. The synchronization between PSPs is essential for detection of EEG; otherwise, the signal will appear as a low amplitude random noise [1].

The EEG signals recorded through scalps are of very low amplitude, around 10-100μV within a frequency range of 0.5-50Hz [20]. The EEG signals are classified into five frequency bands: alpha (α), beta (β), theta (θ), delta (δ) and gamma (γ) (see Figure 1.2). In 1929, Berger introduced the alpha and beta waves. Jasper and Andrews (1938) used the term 'gamma' for the waves above 30Hz. Walter in 1936 used the term 'delta' to classify all frequencies below the alpha rhythm. Walter and Dovey then introduced theta waves in 1944 [7]. As a summary:

- Delta (δ) – These waves can be detected within the range of 0.5–4 Hz and are mainly associated with the deep sleep condition and may be present in the awake state [7-8].

- Theta (θ) – These correspond to the frequency band of 4 to 8Hz (further classified into theta1 which is between 4 to 6Hz and theta2 from 6 to 8Hz) [7-8]. Theta waves start to appear as consciousness slowly moves towards drowsiness. Theta waves often exist with

the other frequencies and are considered to be related to arousal. Theta waves are dominant during infancy and childhood, and considerable theta activity in waking adults is deemed to be abnormal and is caused by pathological problems [7-8].

- Alpha (α) – These waves are visible between 8 to 13 Hz (13 inclusive) and appear as a round or sinusoidal shaped signal. However, in some cases, it may appear as sharp waves. Alpha waves are considered to be associated with a mentally relaxed state without any attention or concentration. Alpha waves can be sub-classified into alpha1 (8-8.9Hz), alpha2 (9-10.9Hz) and alpha3 (11-12.9Hz) [8]. They are considered as waiting or scanning pattern produced by the visual regions of the brain. These waves are reduced or eliminated by opening the eyes, by anxiety, or mental concentration or attention [7].

- Beta (β) – These waves correspond to a frequency range of 14–26 Hz (beta1 from 13 to 18Hz, beta2 from 18 to 22Hz and beta3 from 22 to 30Hz) [8]. A beta wave is considered to be normal in the waking state of the brain. It is associated with active thinking, active attention, focus on the outside world, or solving difficult problems, and is found in healthy adults [7].

- Gamma (γ) – These are the frequencies above 30 Hz. The amplitudes of these rhythms are very low, and their occurrence is rare. These rhythms are used for the confirmation of certain brain diseases [7-8].

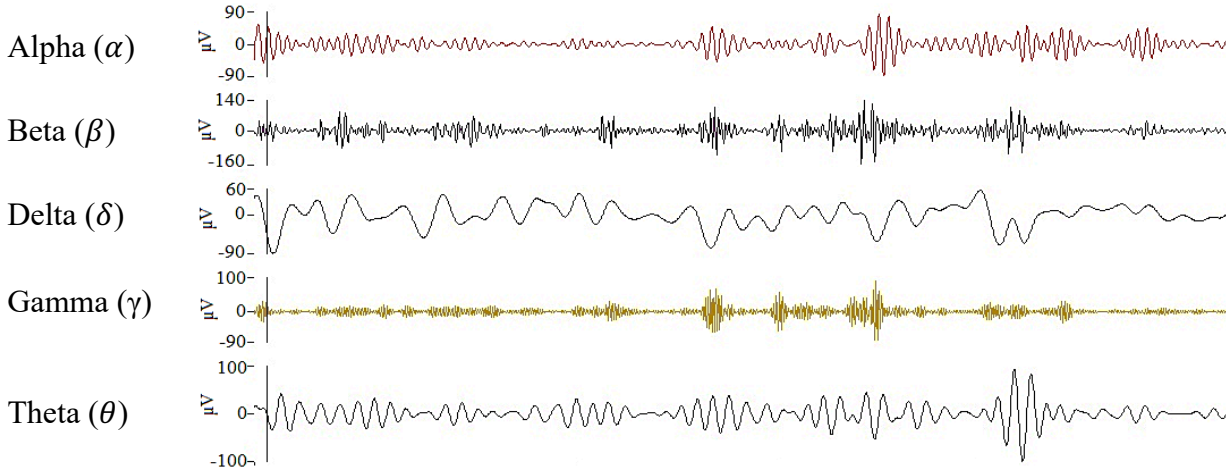

Figure 1.2 EEG samples showing different frequency signals [redrawn from 9].

1.4 EEG recording

Current EEG recording generally employ the internationally standardized 10-20 electrode system for electrodes positioning. Based on this system, a set of 21 electrodes is spread out on the surface of the scalp. Reference points are nasion, which is at the top of the nose at the same level as eyes, and inion, which is at the bottom of the skull, along with the centre line (see Figure 1.3). Besides 21 electrodes, intermediate 10% electrode positions may also be used following the standard of American Electroencephalographic Society. The nomenclature and position of the electrodes are given in Figure 1.4.

Table 1.1 Electrode positioning systems for EEG recording [10].

S. No.	System name	Description
1.	10-20 electrode system	The first electrode from the nasion, inion or preauricular point is at the interval of 10%. The remaining electrodes are equidistant at a spacing of 20%.
2.	Intermediate 10% electrode system	The Skull perimeter between nasion and inion is marked into equal intervals of 10%, and electrodes are placed over them.
3.	Queen square system	Five electrodes are positioned at 5 cm above the inion and 5 cm apart. This arrangement placed two electrodes at either side of a midline electrode.

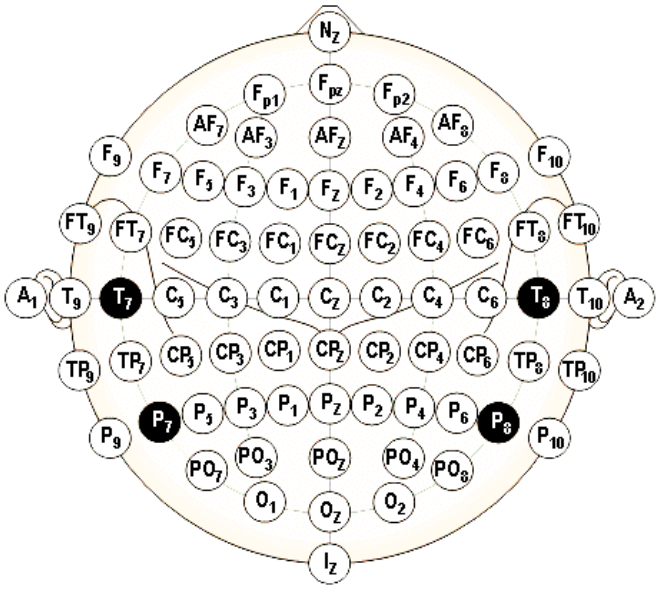

Figure 1.3 Location and Nomenclature of 10% electrode positions standardized by the American Electroencephalographic Society [Redrawn from 10].

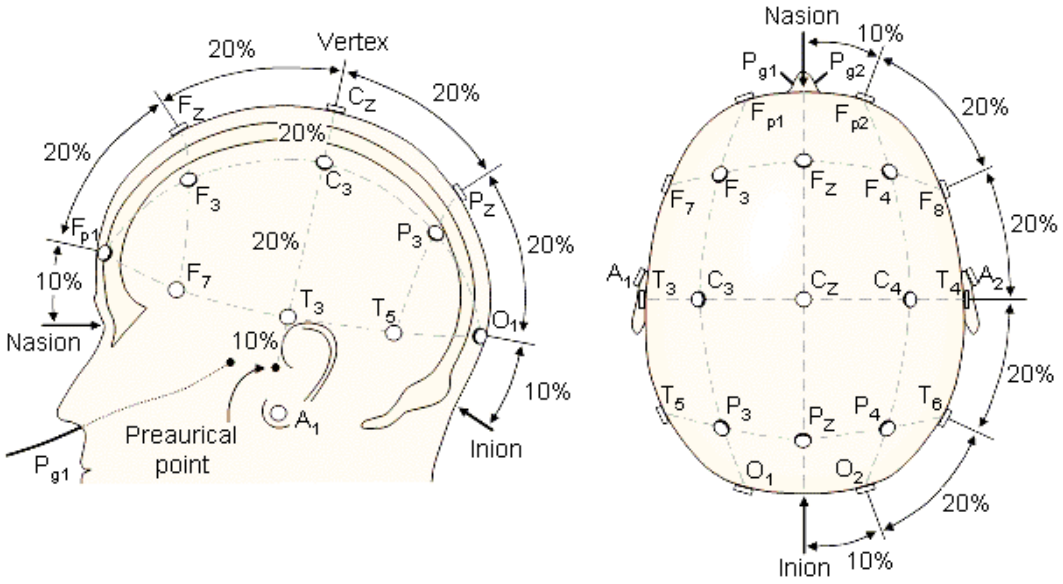

Figure 1.4 International 10-20 system, seen from left and top of the head. A = Ear lobe, C = central, Pg = nasopharyngeal, P = parietal, F = frontal, Fp = frontal polar, O = occipital [Redrawn from 10].

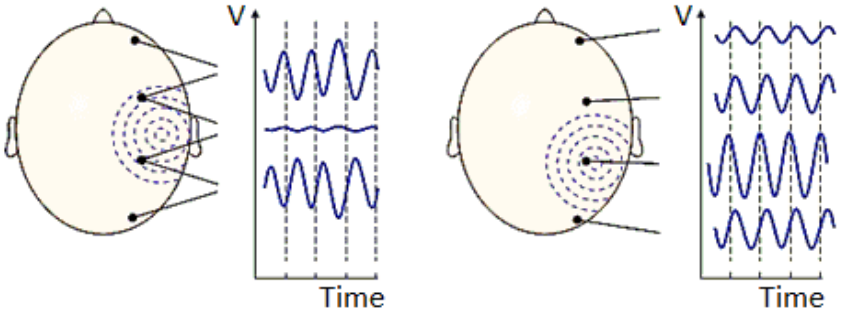

Figure 1.5 Bipolar and Unipolar measurement [Redrawn from 10].

Two methods of recording can be used, unipolar recording, which compares the potential of the electrode with a neutral reference electrode or the average of all electrodes; and bipolar recording which compare the potential between two electrodes (see Figure 1.5).

Wet or dry electrodes can be used for sensing EEG signal [1]. Wet electrodes (Ag/AgCl based) require extensive skin preparation like abrasion, application of electrolyte or gel. The skin resistance is very high, of the order of 10-100kΩ/cm^2 so electrolyte paste is required to reduce this resistance [11]. The disadvantage associated with the application of gel is that there are more chances of impedance variation among various sites due to gel drying out. Also, the gel might create shorts between adjacent recording sites. Moreover, the skin preparation causes

discomfort and may cause allergic reactions or infections. To alleviate some of these disadvantages dry or insulating electrodes are being developed [12].

Even with the inconvenience associated with wet electrodes, they found widespread usage in medical recording as wet electrodes are cheaper, simple, lightweight and initial contact impedances are low enough for a good recording [12]. Dry electrodes may have a significant advantage for wearable or ambulatory EEG application, as they allow recording signals without the need for skin preparation, enabling the subject to be able to undertake daily routine tasks without being isolated from his/her surrounding [13-14].

One of the common shortcomings in both types of the electrode is the problem of the electrode DC offset (EDO), which is caused by the difference in the potential of the electrodes [1]. This electrochemical potential is uncontrollable to a certain extent and depends on the electrode-electrolyte (wet electrode) interface or the electrode-skin (dry electrode) interface [1].

The significant advantage of the wet electrodes is a lower dc offset, 50mV as compared to around 200 mV or more for the dry electrodes [15]. Smaller dc offset is the principal argument to use the wet electrodes in the design of a low-voltage system, where the amplifier can be developed with a reduced voltage supply.

1.5 The Electrode-tissue Interface

All neural recording systems need a physical interface between the electronic circuit and the biological tissue. In a majority of EEG recording systems, Ag/AgCl electrodes are held close to the head with a snug-fitting cap or headset. Preparation of the skin is done by applying an electrolyte gel injected between each electrode and the scalp for providing a stable and conductive path through the hair. It is also possible to record biopotential signals from the scalp using dry stainless-steel electrodes, but these are more susceptible to movement artefacts.

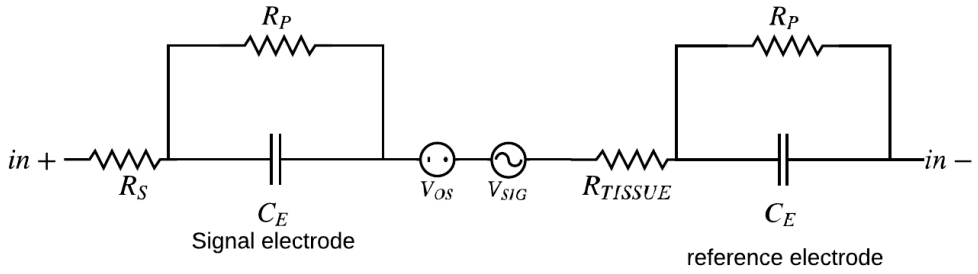

Figure 1.6 Approximate small signal model for skin-electrode interface.

An electrical double layer is formed once the equilibrium is reached across the electrode-tissue interface. This interface acts as a capacitance for small current and voltages. Many textbook models add a resistance parallel to the electrode capacitance as well as series resistance (see Figure 1.6). Charge accumulation due to the chemical interaction between the metallic electrode and electrolytic solution (gel) generates a DC offset (V_{OS} in Figure 1.6). The magnitude and sign of this offset are very difficult to predict as it is a function of material properties, tissue condition, and temperature. This offset could be up to ±50mV for the wet electrodes (±15mV for diagnostic applications), and between 100mV to 300mV for the dry electrodes. The biopotential can be modelled as an AC voltage source V_{sig} in series with resistance R_{TISSUE}, which represents the conductive tissue between the reference electrodes and the signal.

The equivalent model for the electrode-tissue interface is shown in Figure 1.6 [16], is a very useful first-order approximation for the low-voltage applications, but it is important to remember that the actual model is a complex, non-linear, time-varying system which is very hard to model in a precise way. The capacitance and the resistance values, given in Figure 1.6, vary with the frequency and the signal amplitude.

In EEG systems, differential recording from two nearby points is used to avoid 50/60-Hz power line interference pickup, employing identical electrodes. The two terminals in+ and in- presented in Figure 1.6, can be connected to the input of the differential amplifier. An additional electrode is used to tie the circuit ground to the body for guaranteeing a reasonable DC potential at the amplifier input [16]. The resistance R_S, which is due to the conduction through the electrolyte, may be on the order of 2kΩ, while R_P and C_E, which originates from the skin, can be on the order of 2MΩ and 50nF, respectively [15]. For avoiding a severe signal attenuation, the input impedance of the instrumentation amplifier must have much a larger resistive component and a much smaller capacitive component than this.

1.6 EEG application areas

Since Hans Berger (1924) recorded the electrical activity of the brain through the scalp, EEG has become a vital research tool in studies of brain activity. Thus, many different application areas have been explored utilizing the EEG recording [13-29].

EEG signal contains important physiological information, making it useful in epileptic seizure detection and epilepsy diagnosis. Epilepsy is one of the most common neurological disorders, affecting approximately 1% of the world's population, and up to 5% of people may have at least one seizure during their lifetime [21],[36]. An epileptic seizure occurs at random to impair the everyday functioning of the brain. Several patients also suffer from numerous other side effects, such as loss of memory, depression and other psychological disorders [21]. Hence, it is imperative that the epilepsy is detected at an early stage, helping the patient take appropriate actions in advance to avoid damaging consequences. Because of this reason, automated seizure detection and epilepsy diagnosis system from electroencephalogram (EEG) signals has become an active research topic in past decades [21].

Patients who are suffering from Amyotrophic Lateral Sclerosis (ALS) or the late stages of Alzheimer's disease are unable to use facial expression to express their emotions. Still, their brain EEG signals do contain information about their emotional state [22]. A wearable EEG-based emotion detection hardware feasibility is presented in [22], which can help such patients to communicate in real-time under normal social settings.

EEG is also finding use in the field of sleep monitoring to diagnose for any sleep disorders. Sleep disorders can raise the risk of hypertension, sleep apnoea syndrome, obesity, cardiovascular disease, Alzheimer's disease, Parkinson's disease, and lowering the efficiency of the immune system [23],[27]. Sleep disorders are typically investigated in a clinic by a medically trained person. The patient needs to be admitted overnight, which may be an inconvenient, time-consuming, and expensive method [24]. [24] proposed an automated sleep monitoring system using single in-ear EEG sensor. This sensor achieved an accuracy of 74.1% over five sleep stage classification with respect to hypnogram based on the full polysomnography (PSG) recording.

EEG has also found usage in studying the response of antidepressant treatment. The link between the prefrontal EEG dynamics and the antidepressant response has gathered significant interest [25]. Depressed patients who respond to antidepressant treatment, found to have significantly higher alpha power than average. Also, several studies associated increase or decrease in theta power with the treatment response [25].

Due to a non-invasive recording, EEG along with the eye movement data have found usage in the depression detection. Depression is a common mental disorder that affects approximately

350 million people around the world [27]. [28] used the feature extracted from the EEG data for the diagnosis of depression. Alpha, alpha1, alpha2, beta, delta and theta power and theta asymmetry were used as features.

A drowsiness detection wearable headband using EEG signal is proposed in [29], achieving a detection accuracy of 92% using selected features and a linear support vector machine classifier. [17] proposed an alertness detection scheme using the EEG spectrum. [18] recorded EEG signals for drowsiness estimation, which could be used in the context of driving and for attention critical jobs like an air traffic controller. In [30], EEG data was explored for person authentication system. And it has also received a lot of attention in the design of brain-computer interface (BCI) systems [31-33]. EEG data is also being considered for covid-19 diagnosis [34].

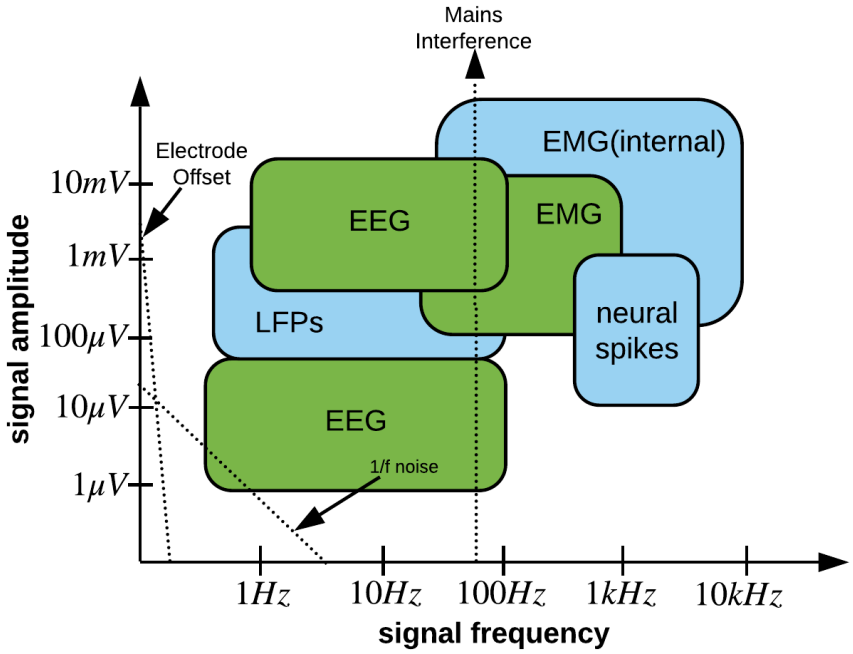

Figure 1.7 Biopotential signals and their frequency band [16].

1.7 Wearable electroencephalography

Due to the non-invasive nature, the electroencephalogram (EEG) is ubiquitous in brain monitoring systems. The most common way of recording EEG is by placing conductive electrodes on the scalp, that can detect microvolt magnitude electrical signals arising from neuronal action within the brain. The primary benefit of EEG is its very high time resolution—helping it to catch events within the brain with millisecond accuracy—and that aides in the

portability of application allowing real-world neuroimaging to be executed outside of clinical and laboratory settings [35].

Current EEG monitoring is either inpatient: where the person attends a tertiary care centre with time-locked video monitored by a trained medical professional and is restricted to a bed by wires connecting the electrodes and recording unit; or ambulatory: where the recorder is portable, and the recording can be done whilst the subject can move around with the recorder and potentially go on with their normal daily routine [13-14],[35],[53].

Though ambulatory EEGs provides advantages over in-clinic EEG, they still suffer from several shortcomings, such as:

- Wires coming from electrodes have to be connected to the device all the time, which restrict the normal movement.
- AEEG systems can weigh up to 1kg; carrying such a system is itself a problem [13-14].

Portability is the main reason why a person undergoing EEG monitoring prefers to stay at home, rather than being seen carrying over a bulky device in public [13-14].

Furthermore, a lot of patients admitted to emergency departments (ED) for a neurological disorder like altered mental status or status or seizures, would remain undiagnosed hours to days after admission, which leads to an elevated rate of death compared to other conditions [39]. By conducting a thorough EEG monitoring in early-stage could prevent further damage to the brain and can avoid high mortality. But lack of portability and ease of access results in a long wait time for the prescribed patients [39].

The above shortcomings can be eliminated from the EEG recording by the use of a wearable EEG. The wearable EEG is the evolution of the bulky AEEG, which can be worn on the body. The wearable EEG is benefited by the advancement in VLSI techniques which aided in the miniaturization and portability of EEG systems. A complete system can now be implemented in a single chip with a mix of analogue and digital devices. The most important benefit of a wearable solution is that it enables recording to be carried out over an extended time by appropriate use of data manipulation, storage and transfer algorithms [13-14],[35]. A wearable solution could be a component of an epilepsy prediction system, which continuously monitors the patient's EEG signals and can alert nurses or health care professionals of impending seizures.

Furthermore, wearable EEG is aiding in the development of new EEG systems like drowsiness detection, alertness detection, wellness, meditation, BCI, etc.

Also, in the current situation of Covid-19 outbreak, social distancing has been put in place, and a lot of scheduled appointments are either pushed or reduced in number. An alternative to ambulatory in-clinic recording would be a wearable EEG recording system, that can help the patient receive appropriate diagnosis and care while maintaining the physical distancing and lockdown protocols.

There are multiple issues that need to be considered for a wearable EEG device [41].

- The device should have good ergonomics, so easier to set up and remove.
- The device should be portable, comfortable, lightweight, and easier to store.
- The device should be hypoallergenic and non-toxic to the body.
- The device should have good accuracy and not very costly to manufacture.

Several commercially ready wearable EEG devices are now available to buy [42-47]. Emotiv Insight is a five-channel EEG device with a battery life of 8hours using USB receiver [42]. The MindWave Mobile 2 by NeuroSky can record the EEG spectrum in the frequency band of 3-100Hz, providing a battery life of 8hours with a single AAA battery [43]. Muse 2 and Brainlink pro are developed for meditation and neurofeedback [44-45]. MyndBand can record the EEG spectrum between 3-100Hz [46]. Also, SenzeBand from Neeuro can record all major EEG signal bands [47]. Besides the commercial products, there are multiple wearable solutions proposed in literature [40],[48-52].

Commercially available devices mentioned above can be used only for a continuous run time of eight hours or less, before the need to replace the battery [42-47]. This short battery life will make their use limited in ambulatory epilepsy diagnosis, where the test may need to be carried out for days and sometimes weeks [53]. Also, for sleep monitoring, their battery life is at the borderline. The target for this research will be to power the system using a coin cell battery, and the power budget considered is 7μW per AFE channel (explained in chapter 2). Also, to enhance the portability and storage, the size of the PCB for the wireless system is restricted to $1cm^3$ [54].

This research aims to define the specifications for building a custom analogue mixed-signal front-end for the EEG recording (mainly in the context of epilepsy diagnosis) and use that to review the suitability of the architectures available in the literature. Also, another critical task is to provide new architectures that can meet the developed specifications for EEG monitoring and can be used in epilepsy diagnosis, sleep monitoring, drowsiness detection and depression study. The research is only aimed to optimise the performance of the analogue frontend while assuming that a data reduction circuit is available [54] and a Bluetooth low energy transmitter like TI's CC2640R2F is available [55].

This research work and the thesis made following key contributions:

1. A novel fully-differential two-stage amplifier design was proposed with an improved frequency response continuous-time common-mode feedback circuit. This amplifier is discussed in detail in Chapter 3.

2. A novel EEG amplifier was proposed using the high-pass frequency set through duty-cycled resistor technique similar to the one presented in [8]. Detailed discussion is given in Chapter 3.

3. A novel EEG amplifier was proposed employing the novel low-distortion pseudoresistor design for setting the high-pass frequency for the amplifier. This design is presented in Chapter 3.

4. A novel EEG amplifier was proposed, where the high-pass frequency was set through a novel pseudo-resistor calibration loop. This design is discussed in Chapter 3.

5. A novel pseudoresistor calibration scheme was proposed to set the value of pseudoresistors accurately, that reduced the variation in the resistor value from 10-20x to just 8.25%. This calibration technique is discussed in Chapter 3.

6. Two novel pseudoresistor designs are proposed. These pseudoresistors achieved a bandwidth of 160Hz and 236Hz respectively, compared to the highest of 54Hz achieved for state-art-implementations designed for EEG application. Also, they attained a total harmonic distortion of 3.73% and 4.2% respectively, compared to 7.5% of the nearest state-of-the-art implementation for EEG amplifier. These designs are presented in Chapter 4.

7. A novel ultra-low-power, high PSRR bandgap reference design was proposed (also published at IEEE conference). This is discussed in detail in Chapter 5.

8. A novel fully-differential fourth-order Sallen-Key filter low pass filter was proposed using duty-cycled resistors and modified differential difference amplifier. This filter is described in detail in Chapter 6.

9. A novel auto-zeroing based dynamic comparator is designed to use in the 12-bit SAR ADC. The design is presented in Chapter 7.

10. Finally, a novel fully-differential analogue front-end was proposed for the EEG recording. The design is presented in Chapter 7.

Following research papers are written during this PhD:

1. M. U. Abbasi, G. Raikos, R. Saraswat and E. Rodriguez-Villegas, "A high PSRR, ultra-low power 1.2V curvature corrected Bandgap reference for wearable EEG application," 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS), Grenoble, 2015, pp. 1-4.

2. R. Saraswat, M. U. Abbasi and E. Rodriguez-Villegas, "Ultra-low power, low noise MAC protocol compliant non-PLL based wearable transmitter for dynamic open spectrum sharing," 2015 7th International IEEE/EMBS Conference on Neural Engineering (NER), Montpellier, 2015, pp. 553-556.

3. Mohammad Usaid Abbasi, "A Wearable EEG Amplifier Using a Novel Teraohm low-Distortion Tunable Hybrid pseudo-Resistor", 2021 IEEE International Symposium on Circuits & Systems.

4. Mohammad Usaid Abbasi, "An Ultra Low Power, Low Noise EEG Amplifier with Chopper Stabilisation and pseudo-Resistor Calibration", 2021 IEEE International Symposium on Circuits & Systems.

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Chapter 2 - Design Specifications and Literature Review

2.1 Overview

Current advancements in very-large-scale integration technology motivate engineers to look for low-cost system-on-chip alternatives to most large multi-chip systems. One area gaining a lot of attention is physiological signal acquisition devices. Such devices have stringent implementation requirements, like long-term operation, without replacing the energy source, small size with lack of wires to reduce the probability of infection and, in some cases, wireless transmission.

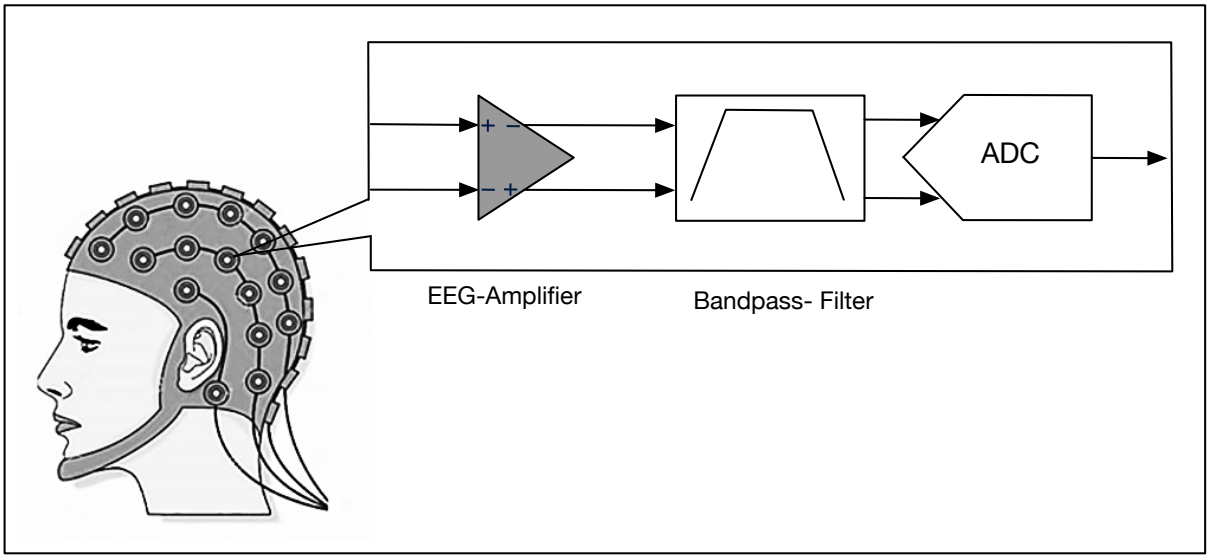

Figure 2.1 Placement of the instrumentation amplifier in an EEG recording system.

Creating an interface to the brain to understand essential brain functions is one of the critical challenges presented to researchers nowadays. Over the last few years, research on recording systems for weak biosignals has been improved drastically. This improvement has accelerated the progress in the area of neural biosignal recording systems like EEG, where the EEG analogue mixed-signal frontend plays a crucial role (see Figure 2.1). An EEG system typically employs multiple channels to record the signal from a specific location. To reduce the size and

increase the usability of an EEG system, low-power consumption is the key. A typical two-channel EEG recording system is shown below in Figure 2.2 [1].

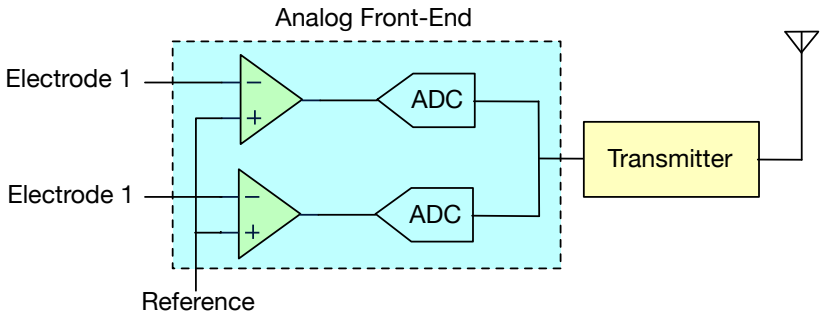

Figure 2.2 A simplified two-channel wireless EEG recording system [12].

2.2 Major challenges in designing an EEG recording system

EEG signals usually have a bandwidth between 0.5-50Hz, with an amplitude in the range of 10-100μV [1-3], though amplitude under 2μV is also possible in infants [4]. Acquiring such a low amplitude signal is very demanding, as the environmental interference and system noise can impede the high-fidelity acquisition of the EEG signal. Due to electrochemical reactions at the electrode-skin interface, different electrode exhibits different potential [5]. This polarised voltage difference, also known as electrode DC offset (EDO) can generate a differential DC voltage difference between the electrodes, which can be between ±15mV to ±50mV for a wet electrode (depending on diagnostic or stimulation application) and about 500 times bigger than the signal [6-7]. If not removed, this EDO can saturate the output of the recording frontend [6]. Also, the electrode-tissue interface has an output resistance of the order of 2MΩ, so the input impedance of the EEG recording system needs to be much higher than this to avoid any signal attenuation [6]. The acquisition system must also deal with the 50/60-Hz supply line common-mode interference and high electrode impedance [8-9], requiring the system to have a high common-mode rejection capability along with a very high input impedance.

The recorded EEG signal's input-referred noise can be overwhelmed by the electrode and acquisition circuit's thermal noise. It can also be severely affected by (1/f) flicker noise of the acquisition circuit. The power consumption of the acquisition circuit should be as low as possible to enable long-term continuous recording in a wearable application without changing the battery frequently. Moreover, for a large spatial resolution to extract information and meet the technical requirement for clinical EEG standards [10], multiple channel integration (greater

than 16 channels) is required [5]. Integrating more channels can contribute to increased power consumption, reducing the battery life of the wearable system.

Besides the electrode DC offset, another source of error can be present while designing an analogue frontend in CMOS VLSI technology. This error is usually due to the inherent circuit offset of the preamplifier, which is the signal present at the output even if the input differential is zero [11-13]. This offset is DC in nature and can be due to poor design strategy, like not matching the different stages. This offset can also be due to random process mismatch due to lithographic errors and variation in doping concentrations. This offset can reduce the circuit's dynamic range and needs to be compensated through specific design strategies. Also, due to the finite transconductance of MOS transistors and threshold voltage variation, they exhibit poor common-mode rejection performance compared to their bipolar counterparts. Thus, all the nonideal issues discussed above contribute to significant challenges in designing a circuit with very low noise, high input impedance, and a high CMRR (Common Mode Rejection Ratio) performance [16-22]. Since the EEG signal band is a low-frequency band, the input transistor's 1/f (flicker) noise contribution cannot be ignored. This necessitates the deployment of offset cancellation schemes like auto-zeroing or chopper modulation [12].

Table 2.1 Summarised standards for Digital EEG recording [14-15].

S. No.	Key Parameter	Specification
1.	Channels	≥ 24, preferably 32
2.	Analog to digital conversion	12-bit, 0.5 μV resolution
3.	Sampling rate	≥ 200 Hz
4.	High pass filtering	≤ 0.16 Hz
5.	Notch filter frequency	50/60 Hz (not mandatory)
6.	Electrode impedances	<5 kΩ
7.	Inter-channel crosstalk	< 1%
8.	Anti-aliasing low pass filter	70 Hz bandwidth, 40 dB per decade roll off
9.	Input referred noise	1.5 μVpp or 0.5 μV RMS
10.	Pre-amp impedances	> 100 MΩ
11.	CMRR	≥ 110 dB

The detected EEG signals vary temporally and spatially, which requires the use of multiple channels where the position of electrodes is determined using the international 10-20 standard

(see Chapter 1 for details). Equipment recommendations from the International Federation of Clinical Neurophysiology are summarized in Table 2.1 [14-15].

2.3 Dynamic offset reduction techniques for a precision amplifier

The accuracy requirement for an EEG recording system is very stringent. The input circuit should be able to detect the voltages at μV level. The inherent offset voltage contribution of input MOS transistors in the EEG recording amplifier could be in the range of several mV. For reducing this offset and 1/f noise contribution, dynamic offset cancellation techniques like auto-zeroing or chopping are usually employed [23].

Autozeroing (AZ) is the process of sampling the unwanted quantity, like flicker (1/f) noise and DC offset, and then subtract it from the instantaneous value of the contaminated signal either at the input or the output of the amplifier. Auto-zeroing typically operates in two cycles. The unwanted noise and offset are sampled on a capacitor during the sampling phase, and the amplifier cannot be used during this phase. The second phase is the gain phase, where the offset is subtracted from the signal, and the amplified signal is available at the output. This method also cancels out the low-frequency signal drift and 1/f (flicker) noise.

The low-frequency flicker (1/f) noise is high pass filtered and hence largely reduced at low frequencies but cause an elevation of the thermal noise floor due to the foldback of the high-frequency thermal noise [12]. Another major issue with the auto-zeroing is that the technique cannot be used in continuous time application without the huge penalty of power and area like in ping-pong topology [23].

The average output noise spectrum of auto-zeroed amplifier can be expressed as[11]:

$$S_{Nout}(f) = A_0^2 S_{n0} \left\{ \left(1 + \frac{f_k}{|f|} \right) \left| H_0(f) \right|^2 + \pi f_c T_s \sin c^2(\pi f T_s) \right\} \quad ...(2.1)$$

where, S_{n0} is the amplifier white-noise component, f_k is the corner frequency, A_0 is the dc gain, f_c is the cut-off frequency, T_s is the auto-zeroing period. Also,

$$\left| H_0(f) \right|^2 = (1 - \sin c(\pi f T_s))^2 + \left(\frac{1 - \cos(\pi f T_s)}{\pi f T_s} \right)^2 \quad \ldots(2.2)$$

$$\sin c(\pi f T_s) = \frac{\sin(\pi f T_s)}{\pi f T_s} \quad \ldots(2.3)$$

The first term in 2.1 represents the baseband noise attenuation, while the second term is the fold-back component due to under sampling of the amplifier white noise [11]. For a large auto-zeroing frequency ($\pi f T_s << 1$) , $|H_0(f)|$ can be approximated as a differentiator function [11]:

$$|H_0(f)|^2 = \left(\frac{\pi f T_s}{2}\right)^2 \quad \ldots(2.4)$$

This double zero introduced by the baseband transfer function $|H_0(f)|^2$ reduces the 1/f noise from the system.

The correlated double sampling can be described as a special case of auto-zeroing followed by sample and hold circuit. Two samples of the signals are taken fast enough to not change the offset and 1/f noise much and applied to the input of a differential amplifier. This cancels out the low-frequency component keeping the signal intact. Like the AZ technique, it has the issue of folding back high-frequency noise into the baseband and more suited to sampled systems.

The above issues are the reason chopper stabilisation is usually preferred in low-power high accuracy circuit design. Following section will provide an overview of the chopping technique and explain how it manages to reduce the dc offset and the 1/f noise of the amplifier.

2.4 Chopper modulation technique for reducing the DC offset and the flicker Noise

The chopper modulation technique is used for reducing imperfections like flicker noise, DC offset from the amplifiers. The idea is to modulate the noise and the offset out of relevant signal band so that it can be reduced without overly impacting the signal [11-12],[24-25].

As can be seen in Figure 2.3, the input signal is first converted to a higher frequency (mainly the odd harmonics of the chopping frequency, where thermal noise is dominant). The converted signal is then passed through the amplifier and afterwards, a second chopper modulator is used to modulate the signal back to the original passband. During this process, flicker noise is

modulated to f_{chop}, and hence the final signal does not have any flicker noise component left [11-12].

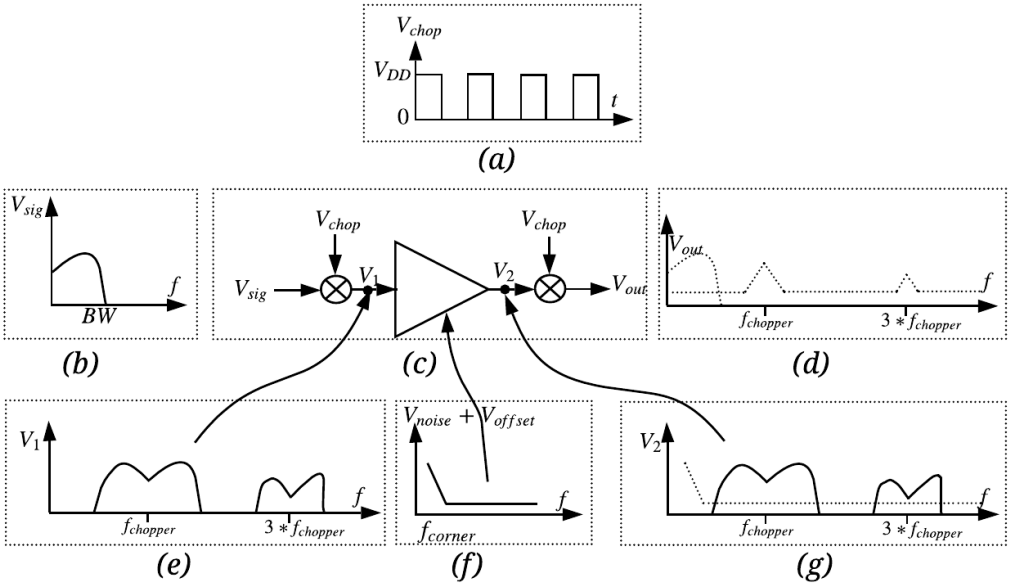

Figure 2.3 Chopper modulation technique to reduce 1/f noise and dc offset [5], (a) square modulating clock signal, (b) input signal, (c) input and output chopper connected to the amplifier, (d) frequency spectrum after the chopping, separating the noise and the input signal, (e) input signal modulated to f_{chop}, (f) noise and the offset contributed by the amplifier, (g) amplifier noise and the offset added to the input signal.

For an infinite bandwidth amplifier, the modulation could be exactly same as the demodulation and recover the signal fully from all harmonics without a loss. But due to the finite bandwidth of amplifiers, full recovery is never possible. For example, if a signal of amplitude V_{sig} is used with an amplifier of bandwidth $2 \times f_{chop}$, where f_{chop} is the chopper frequency, and a gain of A_v, the recovered signal's amplitude would be: $0.8 \times A_v \times V_{sig}$ [25]. The chopper frequency, amplifier bandwidth or signal bandwidth can be chosen as seen in equation 2.5.

$$f_{corner} + f_{signal} < f_{chop} < f_{amp} - f_{signal} \quad \text{...(2.5)}$$

In equation (2.5), f_{signal} is the signal bandwidth, f_{amp} denotes the amplifier bandwidth, and the chopper modulator is a square wave signal with a frequency f_{chop}.

It is clear from equation 2.5 that the smallest value of f_{chop} should at least be able to separate the flicker noise from the signal, and the highest value should not push the main harmonics of the signal main out of the amplifier's passband.

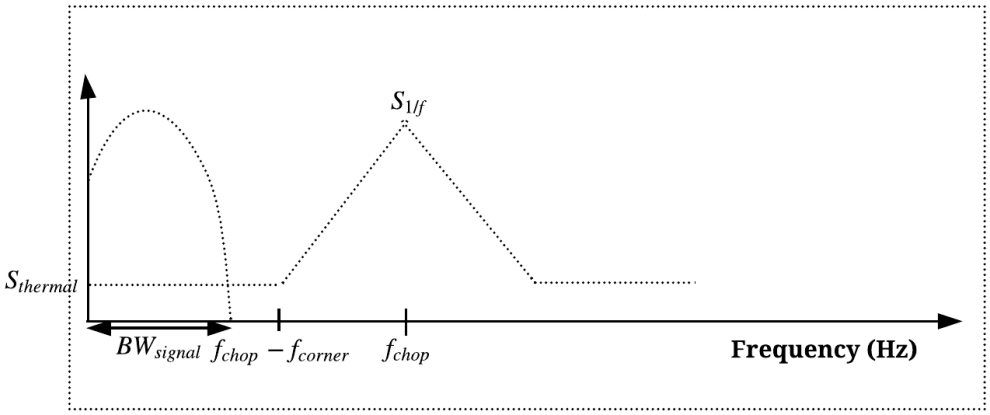

Figure 2.4 Power spectral density of the relevant signal and the noise after chopping [25].

The amplitude of the modulation signal decreases with *1/n* (*n* here is the harmonic number). DC offset and the flicker noise are modulated to odd harmonics leaving the baseband free of flicker noise. When the bandwidth of the amplifier approaches infinity, multiplying the signal twice with the modulating signal, *m(t)* will fully reconstruct the input signal. In reality, the bandwidth of the amplifier is limited, so the result is a high-frequency residue centered around the even harmonics, resulting in attenuation of the signal in the baseband.

The output has to be low pass filtered, for recovering the signal. Following condition should be true for complete reduction of the flicker noise in the baseband [11-12]:

$$f_{chop} \geq BW_{signal} + f_{corner} \qquad \ldots(2.6)$$

The PSD (power spectral density) of the chopper output signal is given by [12]:

$$S_{CS}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} S_N\left(f - \frac{n}{T}\right) \qquad ...(2.7)$$

where, 1/T is the chopper frequency. Equation 2.7 can be approximated in the baseband (sampling frequency is twice the input frequency, $|fT| \leq 0.5$) by a white noise PSD given by [11-12]:

$$S_{N,white}(f) = S_{N,white}(f=0) = S_0\left[1 - \frac{\tanh\left(\frac{\pi}{2} f_c T\right)}{\frac{\pi}{2} f_c T}\right] \quad \ldots(2.8)$$

which for $f_c T >> 1$ (f_c is the cut-off frequency of the amplifier), can be further approximated by:

$$S_{N,white}(f) = S_0, \quad \text{for baseband } (|fT| \leq 0.5) \text{ and } f_c T >> 1. \quad \ldots(2.9)$$

Chopper modulation does not introduce any aliasing of the wideband noise, where it causes the PSD in the baseband to increase proportionally with the ratio of the noise bandwidth and the sampling frequency. As seen in equation 2.8, the baseband PSD resulting from the chopper modulation is nearly constant across frequency (white noise), and it approaches the value of the input white noise, S_0, when $f_c T$ is very large (see equation 2.9).

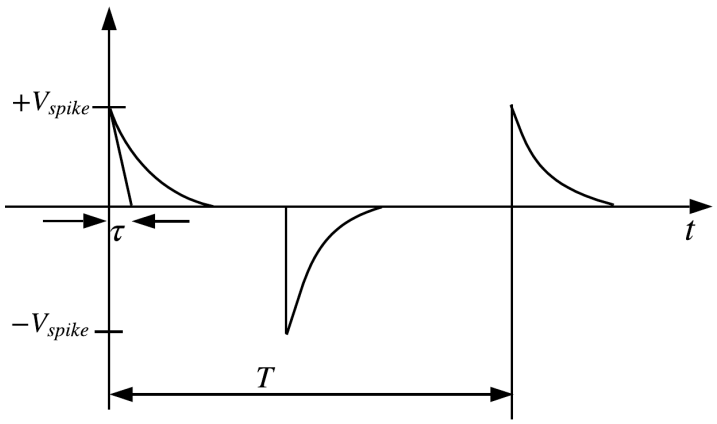

Figure 2.5 Spike at the output of the modulator, causing residual offset [12].

Chopping also introduces a residual offset in the amplifier. This residual offset is mainly due to the clock feedthrough and the charge injection in the input modulator. Moreover, any spikes appearing at the amplifier input and caused by the modulator non-idealities can also be amplified

and eventually demodulated by the output modulator, increasing the residual DC component (see Figure 2.5 for chopper spikes).

Based on the discussion in [12], only the odd harmonics of the chopper frequency add to the residual offset. Positive and negative spikes usually have an odd symmetry as shown in Figure 2.5. By setting the amplifier bandwidth to be much larger than the chopper frequency, the gain can be maximised, but that can cause the maximum output offset voltage since almost all the spectral components of the spike signal are going to add to it. The input referred offset can be calculated as (assuming $\tau << T/2$) [12]:

$$V_{os} \approx \frac{2\tau}{T} V_{spike} \qquad \ldots(2.10)$$

where V_{spike} is the amplitude of the spikes at the amplifier input and τ is the settling time constant for the spike signal. Keeping the same gain A_v in the passband but reducing the amplifier bandwidth to twice the chopper frequency slightly lowers the overall DC gain to $(8/\pi^2)A_v = 0.81 \times A_v$, but considerably reduces the offset voltage referred to the input. The offset voltage is then given by [10],

$$V_{os} \approx \left(\frac{2\tau}{T}\right)^2 V_{spike} \qquad \ldots(2.11)$$

As seen in the above equation (2.11), if τ is kept much smaller than T/2, the offset voltage can be reduced significantly by limiting the amplifier bandwidth to twice the chopper frequency.

2.5 Specifications for the EEG analogue frontend

The realisation of a wearable EEG recording system suffers from the same issue any wireless transmission system does. That is, having a power-hungry transmitter. This dominant power consumption of a transmitter is the reason why data compression algorithms are usually employed only to transmit the necessary data and discard the remaining [27-28]. These data compression algorithms can save the battery power by turning the wireless transmitter off for a brief period. One such EEG data selection algorithm, with a 40% reduction in transferrable data is presented in [27]. Another implementation of data reduction is presented in [28], which requires only 45% of the overall EEG data to be transmitted.

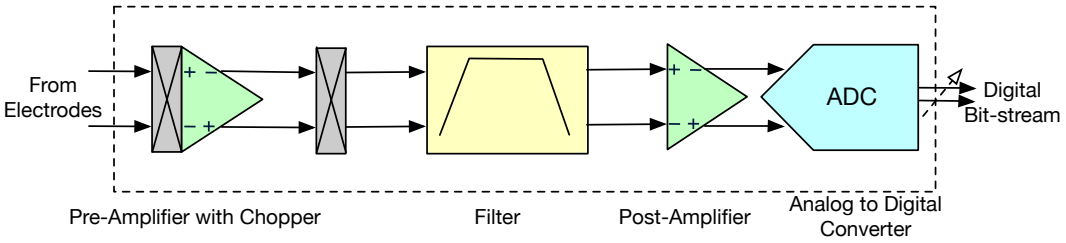

Figure 2.6 A single channel analogue front-end for an EEG recording system [26].

Implementing a wearable EEG system requires the power consumption of the frontend to be kept very low, depending on the battery cell used (see Figure 2.6 for a typical single-channel analogue frontend). Assuming a 32-channel wearable EEG recording system employed data reduction algorithm similar to the one presented in [28], an AFE, and a Bluetooth low energy transmitter CC2640R2F [28], the total power consumption for the system can be calculated by [28]:

$$P_{sys} = N\,P_{AFE} + C\,P_{TX} + N\,P_c \qquad \ldots(2.12)$$

where P_{sys} is the total power consumption for the system, N is the number of channels, P_{AFE} is the power consumption for the AFE, C is the compression factor, P_{TX} is the power consumed by the transmitter, and P_c is the power consumption for the compression algorithm. Suppose we employ a lithium battery with a capacity of 100mWh. In that case, we need to restrict the power consumption to 600µW for running the system for seven days without needing to replace the battery [28]. Since, after data reduction, the transmitter should only be active for 45% of the total EEG recording time so that the power consumption shall be 345.6µW (sampled at 500Hz with a resolution of 12 bit). Power consumed by the data reduction circuit is 950nW per channel. This provides a power budget of 7µW for the AFE per channel. Considering the common-mode interference and the power line interference of the order of 50mV, a common-mode rejection ratio and the power supply rejection ratio needed for the wearable EEG is of the order of 100dB. Also, the EEG frontend should be able to handle electrode DC offset between 15-50mV [6]. Another critical specification for the EEG is the input-referred noise, which is targeted to be around quarter to half of a LSB. As explained in the previous sections [1-3], the EEG signal's minimum amplitude is 2µV, so input noise is targeted to be between 0.5µV-1µV, to avoid overwhelming the EEG signal. Finally, the EEG frontend's input impedance is targeted to be greater than 100MΩ, which is much higher than the electrode impedance of 2MΩ, and helps avoid the EEG signal attenuation.

2.6 Literature review of the EEG analogue frontend

Several of EEG recording frontends are proposed in the literature [29-33]. Their achieved specifications are compared with the target specifications in Table 2.2 (highlighted values are the one not meeting specifications). The implementation in [29] used an open-loop chopper stabilised architecture with a mixed-signal feedback loop to cancel the dc offset. This system can achieve an input-referred noise voltage of 1.25µV_{rms} in the frequency band of 1 to 500Hz, with a chopping frequency of 32kHz. The architecture lacked an input impedance boosting technique which is required to improve the input impedance of a chopper-based amplifier. With a high chopping frequency of 32kHz and an input capacitance of 20pF, the input impedance could drop to 781kohms [29].

Table 2.2 Comparison of target specifications with state-of-art AFE implementation.

Parameters	**[29]**	**[30]**	**[31]**	**[32]**	**[33]**	**Target Specs**
Supply	0.5V	1.5	1.2V	1.8V	1	1
Input Impedance	28MΩ	31MΩ	High	1.2GΩ	102GΩ @1Hz	>100MΩ
Input Referred Noise	1.25µV_{rms} (1Hz ~ 500Hz)	1µV_{rms}(0.25Hz - 250Hz)	4.2µV_{rms} (0.5Hz-100Hz)	1.75µ V_{rms} (0.5Hz-100Hz)	1.5µV_{rms}(0.5 Hz-1.2kHz)	0.5-1µV_{rms}
Noise Cancellation Technique	Chopping	Chopping	No dynamic cancellation	Chopping	No dynamic cancellation	Chopping
DC Offset	±50mV	±30mV	Rail-to-Rail	±250mV	Rail-to-Rail	±50mV
CMRR	88dB	97dB	59.8dB	84dB	108dB	>100dB
Power Consumption /per channel	2.3 µW	5.5 µW	9.4 µW	>11.1µW	3.7 µW	<7µW
ADC ENOB	15	9.4	9.2	12	4,6,8,10	11

Another system proposed in [30] uses a mixed-signal servo loop to cancel the DC offset. This servo loop used a digital low-pass filter for extracting the DC level and a delta-sigma DAC for removing the DC offset from the input signal. This system achieved an input-referred noise of $1\mu V_{rms}$ in the frequency band of 0.25-250Hz. The ADC resolution is 9.4 ENOB, which is slightly lower than the target specification, but the power consumption is within the target specification. Also, the maximum offset that can be rejected by the system is ±30mV, target is ±50mV.

A recording system is proposed in [31] using capacitively-coupled instrumentation amplifier, where T-network is used to achieve large capacitance value using moderate size capacitors. Four back-to-back MOS devices are used as pseudo-resistors for setting the high pass cut-off frequency. The input-referred noise achieved by the system is $4.2\mu V_{rms}$, which is much larger than the target specification. Also, the power consumption is above 7μW, so it needs further improvements before it can be used for a scalp EEG recording system.

An eight-channel wearable EEG acquisition system is proposed in [32]. It achieved an input-referred noise of $1.75\mu V_{rms}$ in the frequency band of 0.5-100Hz. A DSL is used to reject the DC offset from the input. Two back-to-back pseudo resistors were used for setting the high pass cut-off. Such pseudo resistors can have a variation of 2000%-10000%, which eventually can cause significant variation in the high pass cut-off frequency [16]. Also, the total power consumption of amplifier alone is 19.98μW, which is much larger than the target specification. The implementation in [33] used a DC-coupled unity-gain active-electrode for boosting the input impedance. A capacitively coupled instrumentation amplifier is used as a preamplifier stage. Four back-to-back MOSFETs are used as pseudo-resistors, whose value can be tuned by applying a voltage to their gates. The system achieved an input-referred noise of $1.5\mu V_{rms}$ in the frequency band of 0.5-1.2kHz, without the use of any dynamic offset cancellation technique. Also, the ADC achieved a 10bit resolution. Both the input-referred noise and the ADC resolution are not meeting the target specifications. Another major disadvantage with this circuit is that it needs extra output pad per channel and a transconductance driven right leg circuit to improve the common-mode rejection ratio [34].

The discussion above demonstrates that the state-of-art analogue front-end (AFE) implementations studied are not satisfying the complete set of EEG system specifications [29-33]. The architecture used in [29] and [32], are very close to the specifications targeted in this research. Nevertheless, input impedance needs to be worked on for the implementation proposed

in [29]. The noise performance, supply voltage and the power consumption need looking into, for the design proposed in [32].

2.7 EEG recording system designed for this research

The AFE architecture proposed for this research is shown in Figure 2.7. A very high input impedance with ultra-low-power and low-noise amplifier was implemented to interface with the electrode output directly for amplifying the weak neural signals from the scalp. This amplifier employed a chopping strategy to reduce the amplifier noise. Advantage of using the chopping before the input capacitor is that it removes the CMRR loss due to the capacitors mismatch. Also, a DC offset rejection loop was used to get rid of the electrode DC offset. The output of the amplifier was then passed through a novel DDA (differential difference amplifier, which is explained in chapter-6) based fourth-order Sallen-Key low pass filter to reduce chopping spikes and other high-frequency artefacts. Eventually, the filtered output was converted into digital using an ultra-low-power 12-bit SAR ADC.

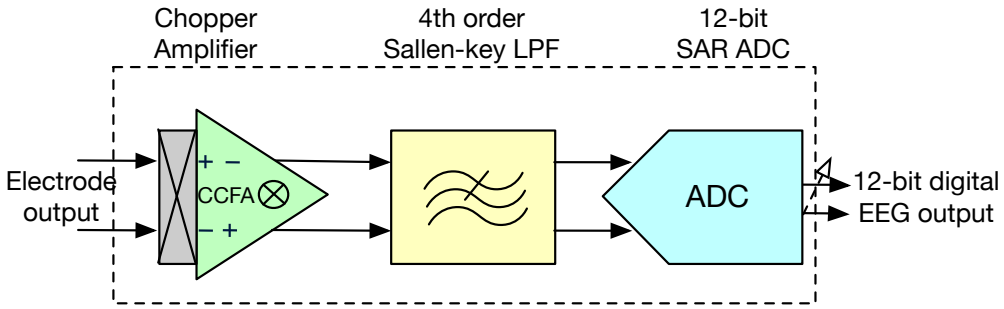

Figure 2.7 Top-level architecture of the proposed analogue front-end for EEG recording.

2.8 Conclusion

This chapter briefly discussed the challenges associated with the design of the EEG recording system. A brief overview of dynamic offset cancellation techniques is given, followed by a quantitative analysis of the chopper modulation technique. Further on, design specifications for EEG recording system are discussed, and a review of several state-of-art AFE implementations is provided. The literature review has shown that the capacitively-coupled chopper-stabilised instrumentation amplifier is the best choice for power efficiency and lower noise [29-33]. Multiple DC offset rejection methods have been reviewed, which are categorised in DC servo-

loop based and ac-coupling based. AC coupling is the most efficient method to cancel the DC offset but introduce a considerable reduction in CMRR due to a mismatch in the input capacitors [16]. That was the reason why this research only considered the DC servo-loop based rejection for the final implementation. Finally, an ultra-low-power wearable analogue frontend was proposed. The proposed system consisted of a capacitively-coupled chopped amplifier, followed by a fourth-order Sallen-Key low pass filter, eventually digitised using an ultra-low-power 12-bit SAR ADC.

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Chapter 3 - Towards an ultra-low power amplifier for EEG recording system

Electrode DC offset voltage at the input of EEG system's front-end amplifier can lead to saturation [1-7]. So, rejecting this offset is essential, as the amplifier is usually designed to amplify microvolt magnitude EEG signals. Also, the contact resistance of the electrode interface might be different between multiple electrodes, causing a DC offset [6]. Besides that, the signal band is at a very low frequency (0.5 - 50Hz), so 1/f noise is dominant in this region. Furthermore, the mains noise at 50/60 Hz usually affects the recording unless electromagnetic shielding is applied. In this chapter, the key focus is to propose an amplifier that adequately addresses these issues.

3.1 Background study on EEG amplifiers

There have been several topologies for EEG recording amplifiers proposed in the literature [1-12]. A capacitively coupled neural amplifier was presented in [1], that used capacitive feedback to set the gain of the amplifier, and a MOS pseudoresistor to set the high pass cut-off frequency (see Chapter 4 for details on the pseudoresistor). [2] proposed a current-mode frontend amplifier, that used a feedback DC servo loop to reject the DC offset. The main problem with this approach is that the high pass cut-off frequency is dependent on the amplitude of the input offset current. [3] presented a slight modification of a neural amplifier, where an analogue loop-controlled capacitance-matching neutralisation scheme was used to bias the amplifier. This design can compensate for the gate leakage current of the input transistors and the bias current needed for the pseudoresistor feedback network. The amplifier's impedance reported was 42GΩ, though the noise performance of the amplifier in the EEG band was not reported. A differential difference amplifier (DDA) based neural amplifier was presented in [4], where the DDA was used as the first stage of the amplifier (see Chapter 6 for details on the DDA). Since the common mode rejection ratio (CMRR) of a capacitive feedback amplifier depends on the matching of the input capacitors, a DDA based design can avoid this problem and can achieve a higher CMRR. A chopping stabilisation technique was further used to minimise the flicker noise, and a digital DC offset compensation circuitry was shared among four channels to reject the input DC offset. The minimum high pass cut-off achieved was 7.7Hz,

so this design does not meet EEG recording specification. Also, the gain of the DDA can vary across the process corners. A modified amplifier similar to a DDA, targeting high CMRR applications, was proposed in [5], but the design used a large external capacitor of value 10nF.

For a micropower biopotential acquisition front-end, a capacitive feedback amplifier topology like the one in [1] is ubiquitous (see Figure 3.1). In this implementation, the electrode offset at the amplifier input is blocked by ac-coupled input capacitors, C_{in}. Matching of capacitors is usually excellent in a CMOS process, which can help in precisely controlling the gain of the amplifier (C_{in} / C_{fb}). A large resistor, R_b, implemented using a pseudoresistor establishes the DC biasing at the input of the amplifier and also creates a high pass filter along with the capacitor, C_{fb}.

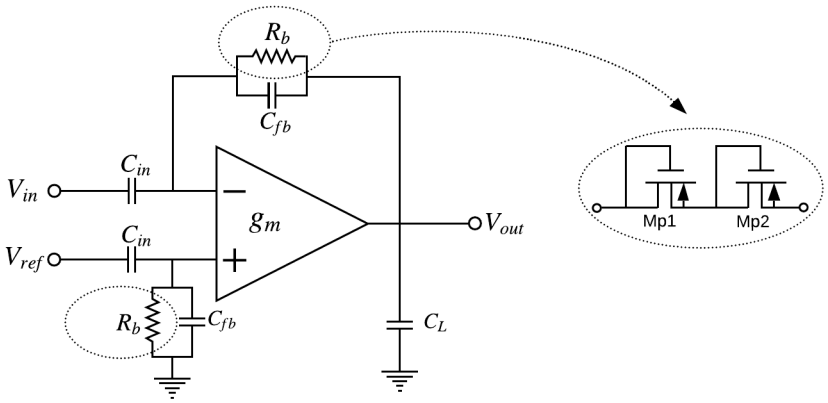


Figure 3.1 Capacitive feedback neural amplifier proposed by Reid [1].

Achieving a high pass pole frequency around 0.1Hz needs a large C_{in} (of the order of 20pF). Such large input capacitance can reduce the input impedance, which is $1/j\omega C_{in}$ for this topology. The reduced input impedance can degrade the common mode rejection ratio (CMRR). Large capacitors are usually better matched as the matching improved with the area, so a direct trade-off exists between input impedance and the matching [10]. Due to random mismatches that exists in a CMOS process, the CMRR achieved for this topology is of the order of 60-70dB [12].

The implementation in [1] is a single stage design, so the output swing is limited. Also, pseudoresistors used are fixed bias with no process compensation, so vary a lot across corners

and allow only small swing across them. Another problem that exists in a single stage amplifier is that it generates a significant voltage swing across the pseudoresistor causing distortion. This topology also suffers considerably from 1/f noise, so it is not very suitable to meet stringent requirements of EEG recording systems. Furthermore, to have an acceptable settling behaviour (1/2 LSB tracking) at the ADC, the bandwidth of the amplifier ($f_{3,dB}$) needs to be five times the bandwidth of the input signal frequency (f_{sig}), which cannot be achieved with a single stage amplifier, as its 3-dB bandwidth is set to be f_{sig}, for low pass filtering the signal [6].

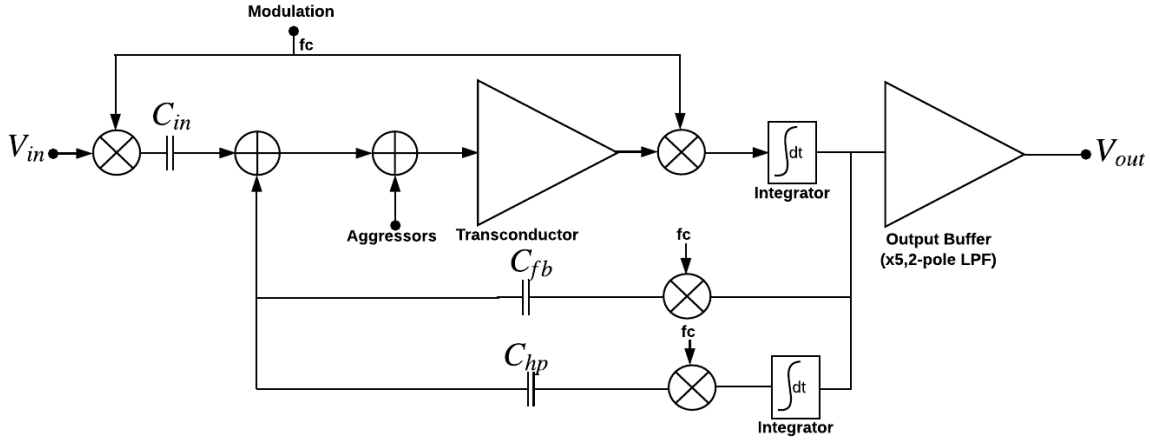


Figure 3.2 A chopper-capacitive feedback neural amplifier proposed presented in [6].

An ultra-low-power chopper-stabilized amplifier topology was proposed in [6] (see Figure 3.2). Chopping was performed before the input ac-coupling capacitor, which decouples the input impedance from the input capacitor value. Also, the CMRR was boosted as the mismatch of the capacitor no longer degrades the CMRR. Since the chopping was performed before ac-coupling the capacitor, the signal and dc-offset were modulated together. They required some mechanism to reject this dc-offset. The dc-rejection was performed by a DC servo loop (DSL) consisting of a low bandwidth integrator, used as a low-pass filter in the negative feedback to create a high-pass function, eliminating the electrode DC-offset and 1/f noise while retaining the relevant signal. The high gain of the DSL rejected low frequency signals at the output of the amplifier. Chopping before the input capacitor changes the input impedance of the amplifier to $1/f_c C_{in}$, putting a restriction on how high the chopper frequency (f_c) can be, and also the size of the input capacitor. The achieved input impedance was not suitable for the scalp-based EEG recording. Also, the continuous time low-pass filter at the output used large sized elements and will put severe constraints on the area if this topology is used in a fully differential configuration.

To alleviate the issue of low input impedance, [7] proposed using the chopping at the virtual ground of the operational transconductance amplifier (OTA). This also allowed decoupling the DC offset of electrodes by employing biasing resistors. That could result in the rejection of a considerably large electrode offset voltage, which does not need to be processed by the amplifier. Unlike [6], the DC offset voltage does not constrain the supply voltage and can be very low. The OTA architecture is similar to [6] where the first stage (A_{v1}) produces a very high transconductance gain, while the second stage (A_{v2}) is operating as an integrator with the Miller capacitance ($C_{m1,2}$). The 1/f noise and the DC offset of A_{v1} are modulated to the chopping frequency (f_c), eventually to be filtered out by A_{v2}. The very high gain of A_{v1} divides the 1/f noise, and the DC offset of $A_{v2,}$ so A_{v2} does not contribute much to the total noise of the amplifier.

Modulating the signal at the virtual ground causes a current path to form between the two inputs. This current path is due to the parasitic switched-capacitor resistance formed by the modulator. Any offset at the OTA input gives rise to the offset current along with the switched resistance, which eventually flows through the large feedback resistor, risking saturating the amplifier. This offset current has been compensated through a Gm-C servo loop, which used a large external capacitor (>10μF) to generate a low frequency cut-off. Furthermore, a very high external AC-coupling capacitor was used to reduce the degradation of the amplifier noise by capacitive division with parasitic capacitors at the input of the OTA. The high-value resistors were implemented using a switched-capacitor topology, which raised the amplifier's noise floor and needed a large continuous-time low pass filter before the ADC. Additionally, this amplifier suffered from the poor matching of external capacitors, causing a lower CMRR (60 dB reported).

3.2 Capacitively coupled EEG amplifier

One of the most widely used amplifier in EEG recording systems is the capacitively-coupled negative feedback amplifier, shown in Figure 3.1 [1],[13]. It consists of an operational transconductance amplifier (OTA) as a gain amplifier, a feedback network consisted of capacitors and pseudo-resistors for biasing. One of the significant advantages of using this topology is that it is AC coupled, so automatically rejects DC offset voltages, and it is this critical feature that makes it suitable for EEG or other physiological recording applications [1]. The value of the input capacitor, C_{in} has to be large enough so that the input impedance of the amplifier is sufficiently larger compared to the electrode impedance.

Since the input node of the OTA is virtually AC ground, the differential input impedance of the amplifier will be $(j2\pi f C_{in})^{-1}$, when both $C_L >> C_{fb}$ and $g_m/2\pi f_s C_L >> 1$, are satisfied (where, C_L is the load capacitance, C_{fb} is the feedback capacitance and f_s is the signal bandwidth).

The value of C_{in} should be carefully selected according to the target signal for recording, as different neural signals have different signal bandwidths, and the impedance of the electrode used is frequency-dependent as well [1],[6]. For instance, while recording extracellular action potential, C_{in} should be less than $16pF$ to make the input impedance larger than $10M\Omega$ at *1 kHz*, since most of the signal energy is concentrated around *1kHz* and the impedance of the microelectrode could range from several hundred $k\Omega$ to a few $M\Omega$ at *1kHz*.

The biasing resistor, R_b serves two main purposes. Firstly, it sets a proper DC bias voltage (typically mid-way between supply and ground) at the input node of the OTA. The second essential function is to determine the low-frequency cut-off of the amplifier by forming a high pass filter with the input capacitor, C_{in}. Therefore, the cut-off frequency of the high-pass function is $1/2\pi R_b C_{in}$, and to achieve the cut-off frequency of less than $1Hz$, R_b should have a value of several $G\Omega$s. It is very challenging, in terms of area and parasitic to implement on-chip resistors with such a high resistance value. The most area and power efficient approach is to use a pseudo-resistor [1] (see Chapter 4).

Most of the output current of the OTA flow through C_L when the condition $C_L >> C_{fb}$ is met. The output voltage can then be described by the following equation [1]:

$$V_{out} = -g_m V_x \frac{1}{j\omega C_L} \qquad \ldots(3.1)$$

where, g_m is the transconductance of the OTA used, V_x is the voltage at the input of OTA and C_L is the load capacitance. Also, we can assume that the input impedance is large enough for the equation 3.2 to be valid:

$$C_{in}(V_{in} - V_x) = C_{fb}(V_x - V_{out}) \qquad \ldots(3.2)$$

The gain of the amplifier can be given as [1]:

$$A_v(\omega) = \frac{V_{out}}{V_{in}} = \frac{C_{in} / C_{fb}}{1 + j\omega \dfrac{(C_{in} / C_{fb})C_L}{g_m}} \quad \ldots(3.3)$$

From equation 3.3, we can deduce the mid-band gain, A_M as C_{in} / C_{fb}, and the high frequency cut-off as $1 / g_m(A_M C_L)$.

OTA design parameters have critical effects on the overall performance of the amplifier, such as equivalent input referred noise, offset voltages, and the common mode rejection ratio (CMRR). A current-mirror OTA with a cascade output stage [14] is widely used in neural amplifiers, similar to the one proposed by [1].

3.3 Noise limit for a differential pair

To determine what is physically achievable in the front-end amplifier, the theoretical noise limit for a differential input amplifier at a certain bias-current level is analysed in the following. In the low noise design, transconductance is maximized while keeping the input-referred noise due to all other noise sources to be very low. The primary noise sources are input pair, load transistors, resistors, etc. For the best power-noise efficiency, the input transistors should be biased in the deep subthreshold region. This region of operation is well suited for applications with low signal frequency and amplitude, but not for high speed and linearity systems). The transconductance for a transistor biased in a weak inversion region can be given as [15]:

$$g_m \approx \frac{\kappa I_D}{U_T} \quad \ldots(3.4)$$

where, κ is the subthreshold slope factor with value of approximately 0.7, U_T is the thermal voltage of $26mV$ at a room temperature of 300K, and I_D is the drain current. The subthreshold transistor's current noise power spectral density (PSD) can be modelled as [15]:

$$\overline{i_n^2} = 4kT \frac{1}{2\kappa} g_m = 2kT \frac{I_D}{U_T} \quad \ldots(3.5)$$

Based on two equations above, the input referred noise PSD for an ideal differential pair can be given as:

$$\overline{v_{ni}^{\,2}} = 2\frac{\overline{i_n^{\,2}}}{g_m^{\,2}} = 4kT\frac{U_T}{\kappa^2 I_B} \qquad \ldots(3.6)$$

where I_B is the bias current for each transistor in the differential pair.

The amplifier in this work was targeted to consume between 1μA-3μA trimmable current. The partitioned bias current in the differential input pair used here is $2I_B$ (=700nA or 2400nA). Equation 3.6 indicates that an input-referred noise voltage of 27 nV/√Hz to 50 nV/√Hz at 300K is the theoretical noise limit of a differential-input amplifier biased in the subthreshold region with the target current level of 700nA to 2.4μA.

3.4 Fully differential folded-cascode amplifier

Fully differential circuits are widely used and highly desirable in analogue circuit design primarily because they are quite useful in rejecting common-mode noise, particularly in mixed-signal design. Since fully differential circuits are built to be symmetrical, supply disturbances should affect both signal paths in equal proportion. In a fully differential amplifier, the signals at two output terminals are finally subtracted from each other, so if there are any common-mode disturbances, such as power supply variations, are rejected [14].

A folded cascode structure is used here as the first stage of the two-stage OTA. A folded cascode structure is used for its power efficiency and ability to decouple input common mode from the output so it can be easily defined. Most importantly, the folded cascode OTA can be designed to have maximum transconductance by restricting the maximum current to flow through the input pair. A significant benefit of this approach is that the noise contribution due to the folded output stage shall be insignificant compared to the input pair, which can be made very big in area for reducing the noise. The basic fully differential folded-cascode op-amp is shown in Figure 3.3. Transistors M1 and M2 form the input differential pair. The transistor, M11, forms a tail current source to fix the current through the differential pair. And the transistors, M7 and M8, form a common-gate stage to cascode the differential pair. M3 and M6 set the current through the transistor M7 and M8. M9 and M10 are current source loads whose drain currents are split between the input differential pair and cascode stages. The common-mode rejection ratio (CMRR) of the amplifier is determined by the resistance of the M11.

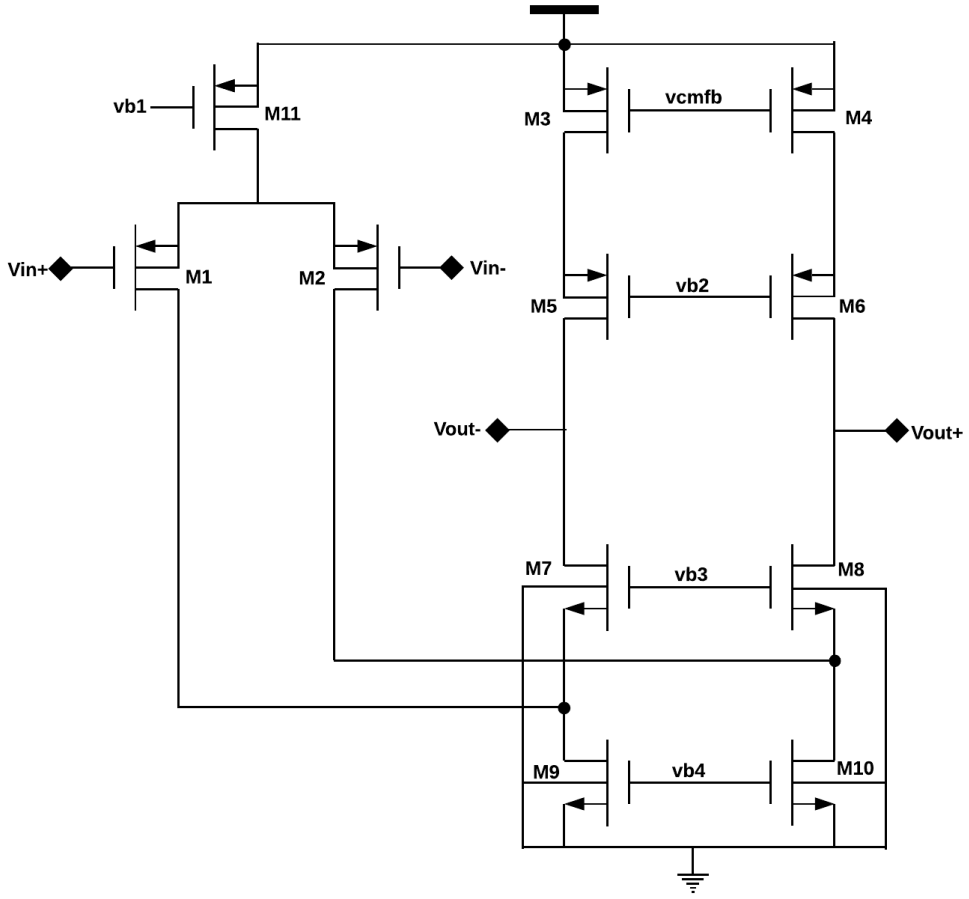


Figure 3.3 Conventional fully-differential folded cascode amplifier [14].

A two-port model for an amplifier is shown in Figure 3.4(*a*). The DC gain for the system is given by:

$$a_v = G_M R_o \qquad \ldots(3.7)$$

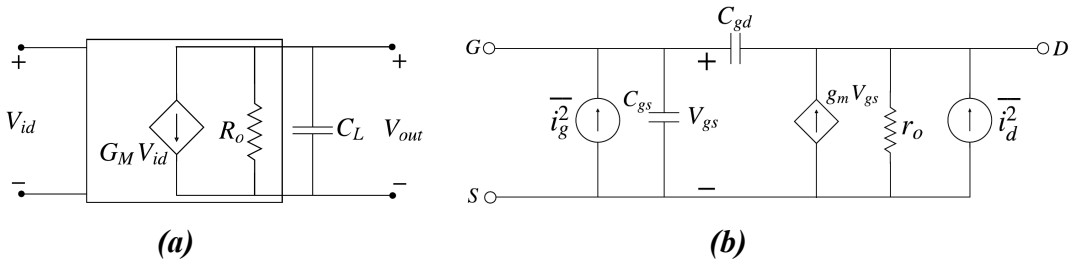


Figure 3.4 (a) A two-port model for an amplifier [16], (b) small-signal equivalent model for a MOS device.

where G_M is the short-circuit transconductance, given by $\frac{i_{sc}}{v_{id}}$, where i_{sc} is the current flowing through the output when the output is shorted to ground. When the output is shorted to ground, there will be no current gain across M7, and $i_{sc} = g_{m1} v_{id}$, so $G_M = g_{m1}$.

R_o is the output impedance of the folded-cascode OTA and is a parallel combination of the impedance looking into the drains of M5 and M7 [14]:

$$R_o = R_{up} \,||\, R_{down} = (g_{m5} r_{o5} r_{o3}) \,||\, (g_{m7} r_{o7} (r_{o1} \,||\, r_{o9}) \quad \ldots(3.8)$$

$$a_v = G_M R_o = g_{m1} (g_{m5} r_{o5} r_{o3}) \,||\, (g_{m7} r_{o7} (r_{o1} \,||\, r_{o9}) \quad \ldots(3.9)$$

Nodes with the highest resistance connecting to a capacitive load generally have the most significant impact on a system's frequency response. In the folded cascode OTA of Figure 3.3, the node with the largest impedance appears at the output and gives the dominant pole p_1, of the system. At the output, we have the parallel combination of the output resistance R_o, and the load capacitance, C_L as seen in Figure 3.3 [14].

$$a_v = \frac{g_{m1} R_o}{s R_o C_L + 1} \quad \ldots(3.10)$$

$$p_1 = -\frac{1}{R_o C_L} = -\frac{1}{(g_{m5} r_{o5} r_{o3}) \,||\, (g_{m7} r_{o7} (r_{o1} \,||\, r_{o9}) C_L} \quad \ldots(3.11)$$

The lowest frequency non-dominant pole is due to parasitics at the sources of M7 and M8. These parasitic capacitors are large because of following reasons:

- There are a large number of devices connected to the source of M7 and M8.
- M1 and M2 are sized to have a large $\frac{W}{L}$ ratio for high g_m and low noise.
- M9 and M10 are sized to have a large $\frac{W}{L}$ ratio for a low $V_{DS,SAT}$ drop. Also, due to noise contribution of these devices, the area is kept large to reduce the *1/f* noise. These parasitics create

a non-dominant pole located at $p_2 = -\frac{g_{m9}}{C_{par}}$, where C_{par} is the parasitic capacitor and g_{m9} is the transconductance of transistor M9.

Assuming that the two frequency poles are real and widely separated (where $C_L >> C_{par}$, and $R_o >> \frac{1}{g_{m9}}$), then at the unity gain frequency, gain of the OTA can be approximated by a single pole roll-off:

$$a_v = \frac{g_{m1}R_o}{sR_oC_L + 1} \approx \frac{g_{m1}}{sC_L} \quad \ldots(3.12)$$

resulting in the unity gain frequency as:

$$\omega_u = \frac{g_{m1}}{C_L} \quad \ldots(3.13)$$

The pre-amplifier is the direct interface between electrodes and the rest of EEG readout circuit, so the noise performance of the amplifier is absolutely critical for a successful recording system. The noise sources need to be correctly identified and reduced or eliminated through careful circuit design.

In Figure 3.3, major noise contributors are M1, M2, M3, M4, M9, and M10. Due to symmetry, noise contribution from the bias current source M11 is cancelled. The cascode devices M5, M6, M7, and M8, does not contribute to noise as they are source degenerated, and hence the effective transconductance is extremely low.

Assuming matched pairs have equal noise contribution and transconductance (v_n being the noise voltage). Adding all noise currents at the output:

$$i_{out}{}^2 = 2(g_{m1}^2 v_{n1}^2 + g_{m3}^2 v_{n3}^2 + g_{m9}^2 v_{n9}^2) \quad \ldots(3.14)$$

Dividing this equation by g_{m1}^2, gives the input referred noise voltage as:

$$v_{ni}^2 = 2(v_{n1}^2 + \frac{g_{m3}^2}{g_{m1}^2} v_{n3}^2 + \frac{g_{m9}^2}{g_{m1}^2} v_{n9}^2) \quad \ldots(3.15)$$

Replacing variables with the expression of the thermal noise of MOS transistors[14]:

$$\frac{v_{i,th}^2}{\Delta f} = 2\left[\frac{8kT}{3g_{m1}} + \frac{g_{m3}^2}{g_{m1}^2}\frac{8kT}{3g_{m3}} + \frac{g_{m9}^2}{g_{m1}^2}\frac{8kT}{3g_{m9}}\right] \quad \ldots(3.16)$$

$$\frac{v_{i,th}^2}{\Delta f} = \frac{16kT}{3}\left[\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}\right] \quad \ldots(3.17)$$

And taking into account, $g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$

$$\frac{v_{i,th}^2}{\Delta f} = \frac{16kT}{3\sqrt{2\mu_p C_{ox}\frac{W_1}{L_1}I_{D1}}}\left[1 + \sqrt{\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}} + \sqrt{\frac{\mu_n\frac{W_3}{L_3}}{\mu_p\frac{W_1}{L_1}}}\right] \quad \ldots(3.18)$$

$$\frac{v_{i,1/f}^2}{\Delta f} = 2\left[\frac{K_p}{W_1 L_1 C_{ox}{}^2.f} + \frac{g_{m3}^2}{g_{m1}^2}\frac{K_p}{W_3 L_3 C_{ox}{}^2.f} + \frac{g_{m9}^2}{g_{m1}^2}\frac{K_n}{W_9 L_9 C_{ox}{}^2.f}\right] \quad \ldots(3.19)$$

$$\frac{v_{i,1/f}^2}{\Delta f} = \frac{2K_p}{W_1 L_1 C_{ox}{}^2.f} + \frac{1}{\frac{W_1}{L_1}}\frac{2K_p}{L_3{}^2 C_{ox}{}^2.f} + \frac{\mu_n}{\mu_p\frac{W_1}{L_1}}\frac{4K_n}{L_9{}^2 C_{ox}{}^2.f} \quad \ldots(3.20)$$

This research is focused on recording EEG signals which are in the frequency band of 0.5-50Hz [16-21]. For this frequency band, flicker (1/f) noise is the dominant noise source, so should be reduced by proper design choices. Main parameters under designer's control are MOS transistor's width, length, and current, which can be set to optimize the circuit noise performance. The strategies used here are:

- Havin a relatively large current through M1 and M2, compared to the folded stage.
- Having a large $\frac{W}{L}$ ratio for M1 and M2, (for reducing the effect of thermal noise).
- Having a large area for M1 and M2 (Avoiding increasing the size too much as the gate capacitor may start to impact the total noise performance for the feedback amplifier).

- Using large lengths for the current source loads (M3, M4, M9, M10), and a small $\frac{W}{L}$ ratio.

- Reducing current flowing through the folded output stage (M3-M8), and majority flowing through M1 and M2, causing M1, M2 to be the dominant noise source [22-24].

3.5 Common-mode feedback circuit

One drawback of employing a fully differential topology is the need for a common mode feedback (CMFB) circuit [23], [25] (see Figure 3.5). A general strategy is to keep the common mode gain very low for a better CMRR (common mode rejection ratio), which means that the amplifier input no longer controls the common mode output. That allows the common mode output voltage to swing uncontrolled and may decrease the output swing and/or cause transistors to operate outside of the desired operating regions. So, a common mode feedback circuit is necessary to keep the output common mode tightly controlled and to suppress any variations in the quiescent point of the output voltage.

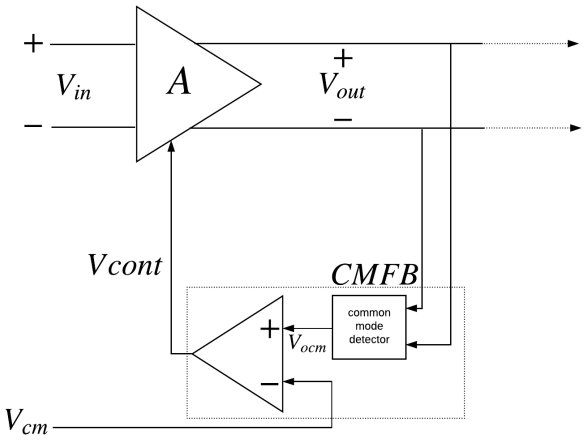


Figure 3.5 Concept of a common mode feedback circuit for a fully-differential circuit [23].

Switched-capacitor CMFB topologies have the advantage of being area efficient and not needing an additional amplifier with extra stability loop. But switched topologies do introduce switching transients which may increase the total noise level of the circuit. Also, capacitors from the switched CMFB may load the output of the amplifier. Another issue is that the switched capacitor CMFB may complicate the overall loop stability of the system.

The chopper amplifier is a continuous time system, where adding a switched capacitor CMFB might complicate the stability of the feedback loop. This is the reason why a continuous-time CMFB circuit was used in this work. Most of the gain is in A_{v1}, so a rail-to-rail CMFB circuit is needed to avoid distorting the amplifier output.

Fully differential output nodes of the amplifier have high impedance, causing low-frequency poles, so the CMFB should not introduce any more low-frequency poles keeping the stability of the amplifier feedback loop unperturbed. The CMFB should also have a high input impedance unless it will load the output of the amplifier.

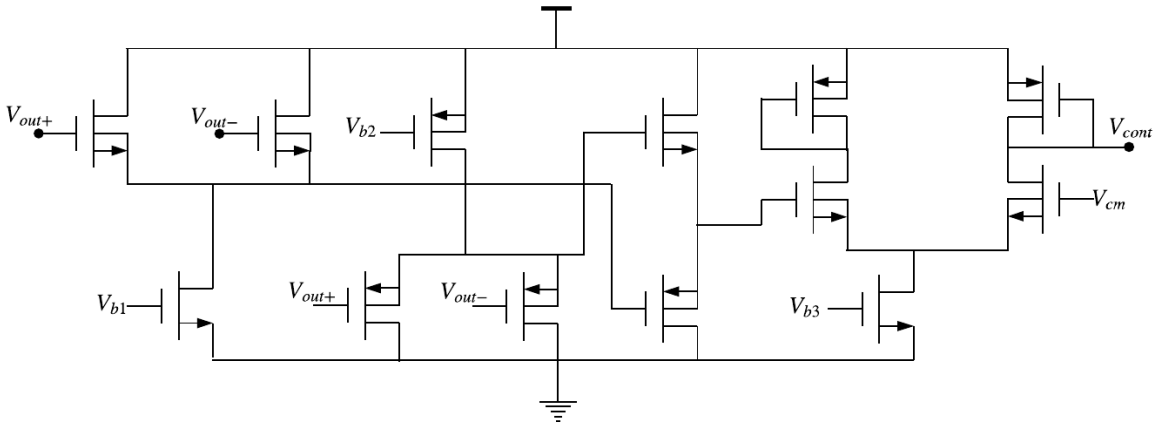


Figure 3.6 Improved frequency response continuous-time rail-to-rail CMFB circuit used in the first stage amplifier (A_{v1}).

The CMFB here used is a stand-alone continuous-time common-mode feedback circuit, which can be inserted into the fully differential amplifier without disturbing its stability. The CMFB used is modified from [26] (see Figure 3.6), with additional modification of using a diode connected load rather than a current mirror-load OTA at the output of CMFB, for reducing the output pole of the CMFB loop and further increasing the bandwidth. Also, the NMOS devices are placed in a separate deep N-well to reduce the bulk body-effect and shield them from substrate noise.

The output of the second stage amplifier, A_{v2}, is defined through a low gain differential-difference amplifier based CMFB circuit (see Figure 3.7)[27].

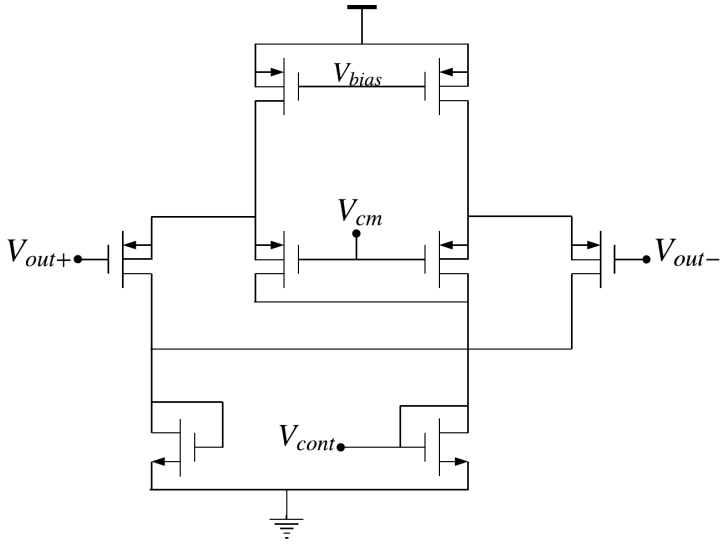
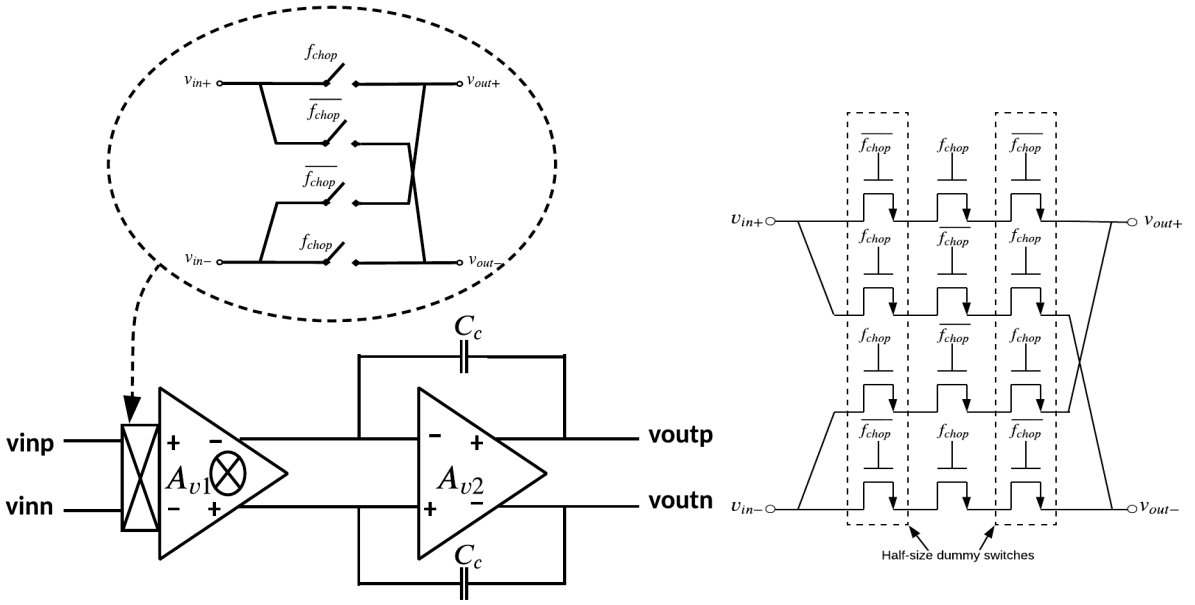


Figure 3.7 DDA based CMFB circuit used in the second stage amplifier, A_{v2} [27].

3.6 Two-stage fully differential amplifier with a chopping modulation scheme

The core-amplifier for the capacitive feedback chopper EEG amplifier is a two-stage amplifier, A_{amp}, with the first stage as a very high gain folded cascode (A_{v1}) and the second stage (A_{v2}) a common-source amplifier (see Figure 3.8 (*a*)). Both amplifiers are fully-differential, and their quiescent point is defined using individual common-mode feedback (CMFB) circuits. The total noise of the amplifier is dominated by the first stage (A_{v1}) since the noise of the A_{v2} is suppressed by the very high gain of the first stage. A rail-to-rail continuous-time CMFB circuit is used for the A_{v1}(see Figure 3.6), and a differential-difference amplifier (DDA) based CMFB is used for A_{v2}.The second stage, A_{v2} along with the compensation capacitor C_c, constitute an integrator that can suppress the high-frequency voltage spikes from the modulation. This method is more efficient in rejecting chopping spikes, rather than using a dedicated chopping spike filter like in [28]. The first stage A_{v1} (see Figure 3.9) has few modifications from the classical folded cascode design [30-33]. Current partitioning is performed in a way that majority of the available current passes through M_{p1} and M_{p2}. The chopping is performed at the low impedance node [29]. The benefit of such approach is that the chopping frequency does not impose any restriction on the bandwidth of the amplifier, which allows use of a very high chopping frequency compared to the bandwidth of the amplifier. The input chopper consists of NMOS switch with half-size dummy switches to reduce the charge injection (see Figure 3.8(b)) [6-7].



(a) *(b)*

Figure 3.8 (a) Architecture of the two-stage fully-differential chopped amplifier, A_{amp} [6-7], (b) switches used in the chopping modulator [52].

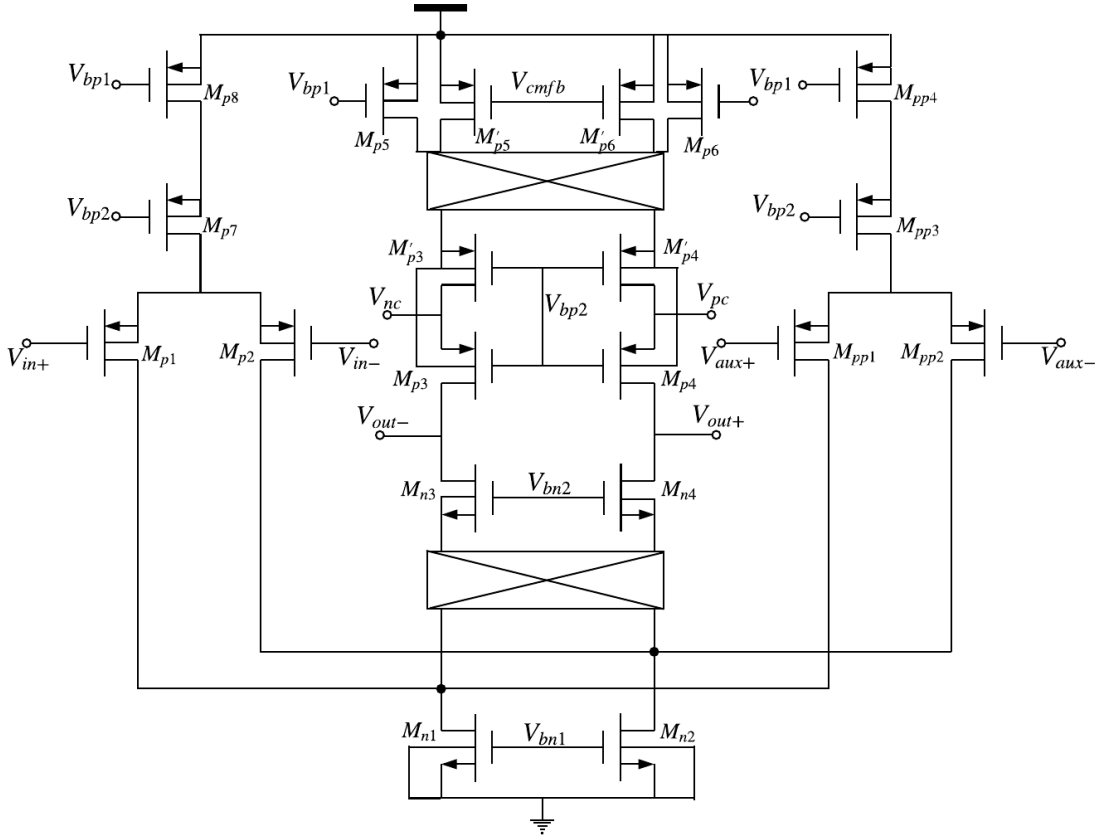


Figure 3.9 Folded cascode amplifier (A_{v1}) implemented with indirect compensation and auxiliary path for ripple rejection.

Current through the folded branch (M_{n3}, M_{n4}, M_{p3}-M_{p6}) must not be very low, otherwise slewing effect will start to appear due to a very small current to charge and discharge the large compensation capacitor, C_c. This slewing effect can introduce input voltage dependent distortion.

In a conventional folded cascode amplifier cascode devices do not contribute to the total noise of the amplifier, though here non-cascode devices are chopped to a higher frequency, so their contribution is negligible compared to cascode devices, which need cascode devices (M_{n3}, M_{n4}, M_{p3}-M_{p4}) to be very large.

The purpose of modulation switches at the source of M_{p3}, M_{p4} is to provide dynamic element matching for M_{p5}, M_{p6}, and also up-modulate the 1/f noise for these devices. Similarly, modulating switches at the source of M_{n3}, M_{n4} are providing dynamic element matching to the devices M_{n1}, $M_{n2,}$ and up-modulating the 1/f noise. Also, these switches are demodulating the signal back to the baseband.

Transistors M_{p3}, M_{p4} are divided into two, to create a low impedance node for connecting the compensation capacitor as explained in [33]. This also isolates the chopping node from the compensation node.

There is an auxiliary path created using transistors M_{pp1}-M_{pp4}, which uses 1/20th current of the main amplifier input pair M_{p1}, M_{p2} [35]. This auxiliary path converts the ripple voltage back into the current to compensate for the chopping ripple created by the offset of the main amplifier. The g_m of this stage can be independently set through a trimming block to compensate for the offset of the main branch [36]. Transistors M_{p5} and M_{p6} are split into two paths: one is biased by a current source and the second path is biased using a continuous-time CMFB circuit. This is to make sure that the output quiescent point is well-defined for the amplifier, and a smaller load shall be seen by the output of the CMFB, helping with the frequency response of the common mode feedback loop. The second stage, A_{v2} is a traditional common-source amplifier with rail-to-rail output swing (see Figure 3.10). The output bias point is set by a DDA based CMFB circuit, as explained earlier (see Figure 3.7). Since this stage is not driving a high load stage, so the current requirement for this stage can be very low.

The results of the DC simulation are presented in Figure 3.11. Multiple corners (process, voltage and temperature) have been run to check the DC performance of the amplifier, and

moreover the performance of the CMFB. No effect of CMFB clipping the range was seen (see Figure 3.11).

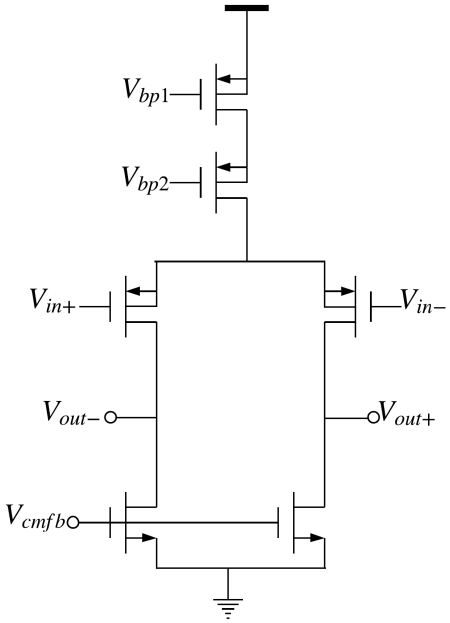


Figure 3.10 Common source amplifier used as the second stage (A_{v2}) for achieving large output swing.

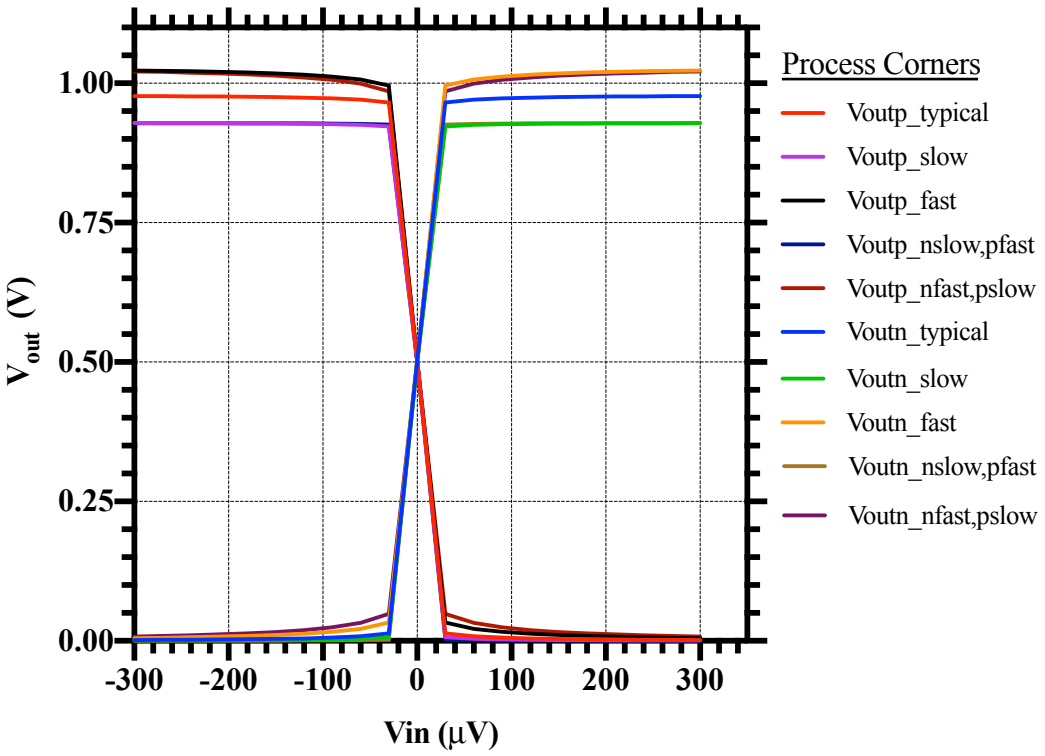
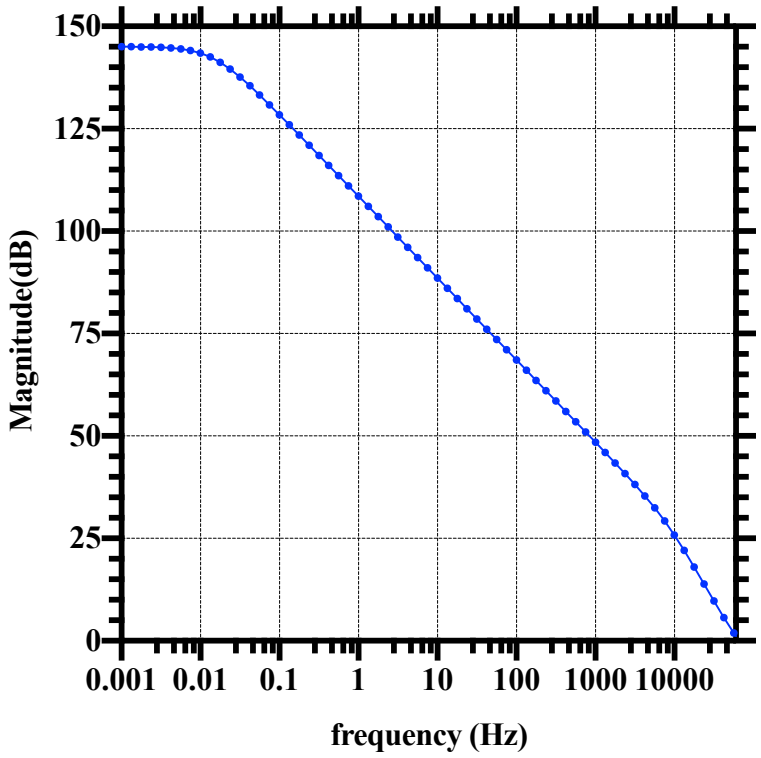
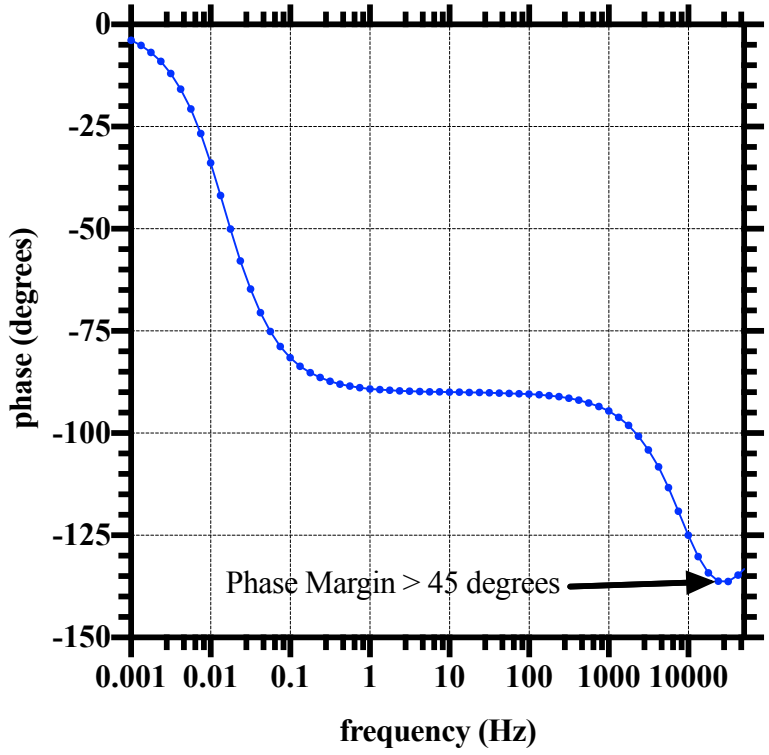


Figure 3.11 Simulated process corner DC sweep result for the two-stage amplifier, A_{amp}. Amplifier exhibited consistent gain up to the ground and the supply rail.

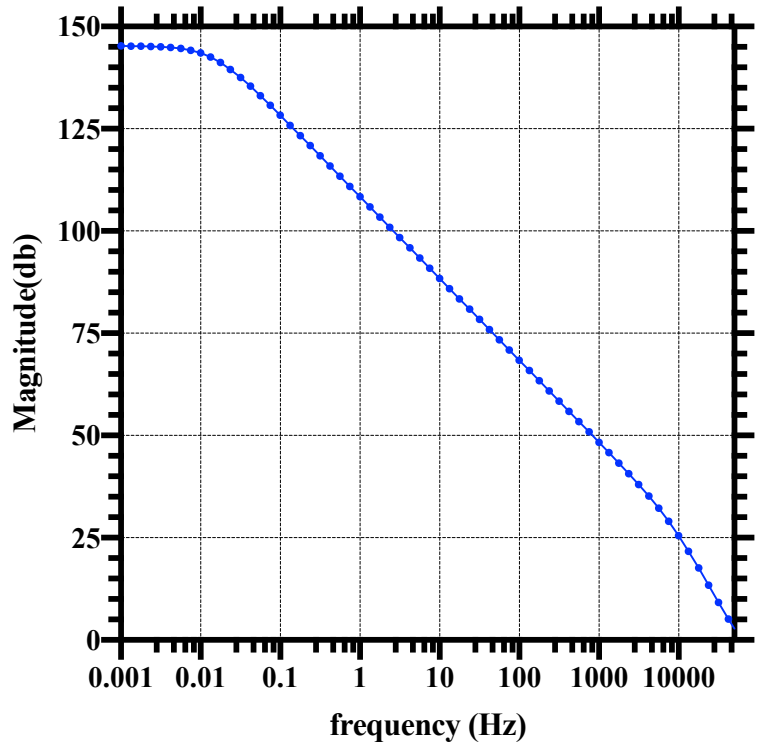


(a)

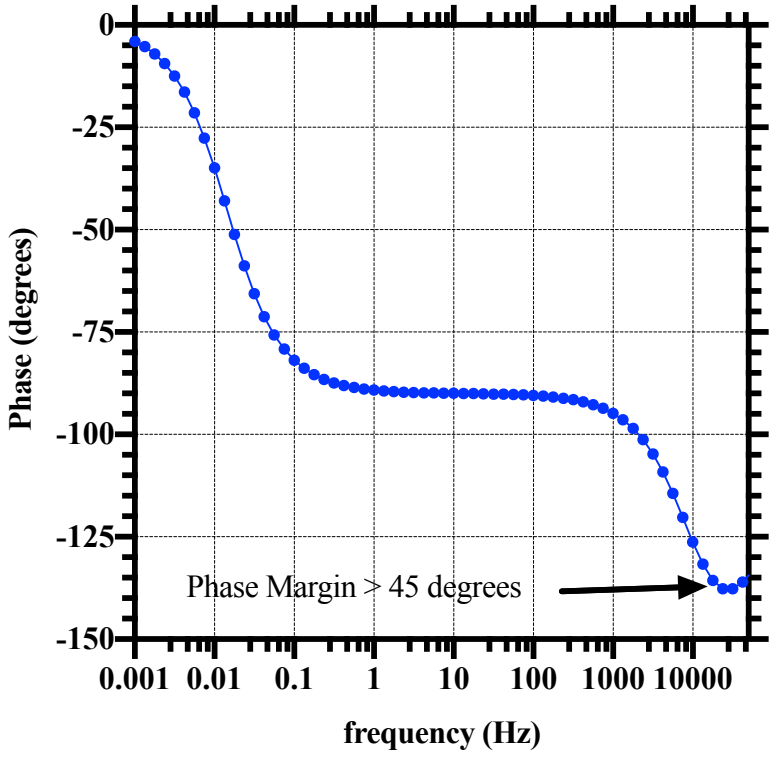


(b)

Figure 3.12 (a) Simulated output gain response, (b) phase response of A_{amp} at the typical corner. The response shows phase margin of over 45 degrees with no complex poles. Left hand plane zero at unity gain frequency improved the phase margin.

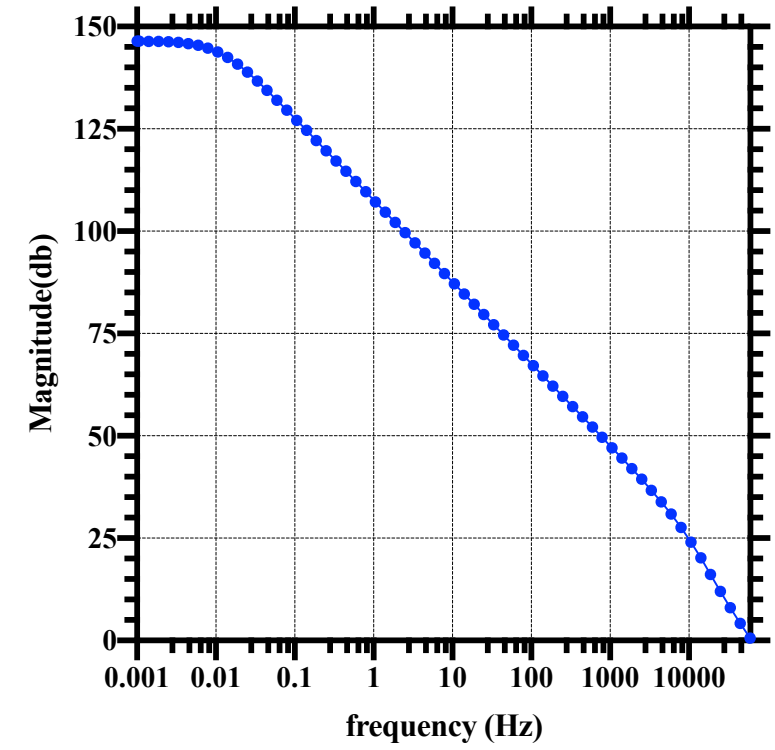


(a)

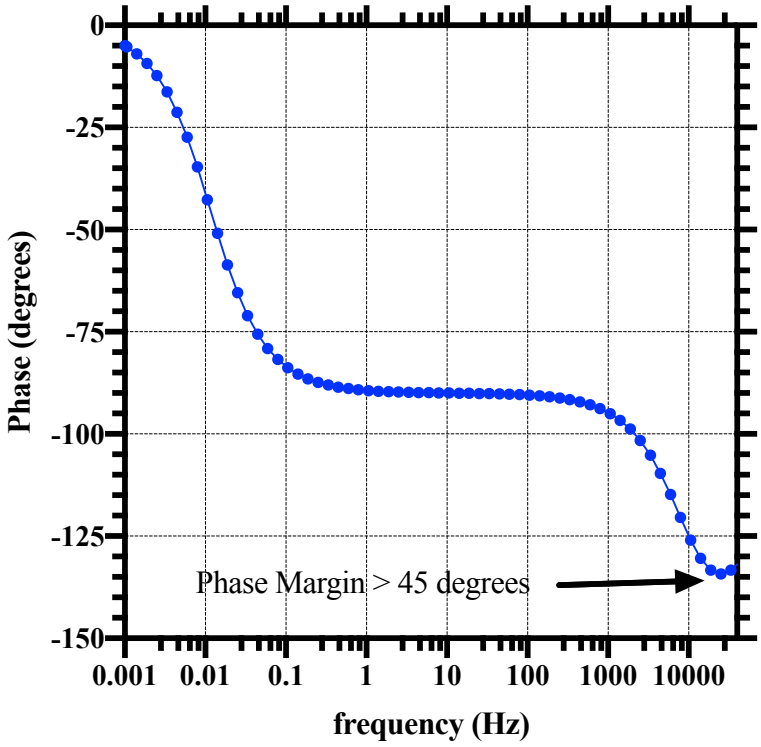


(b)

Figure 3.13 (a) Simulated output gain response, (b) phase response of A_{amp} at the fast corner. The response shows phase margin of over 45 degrees with no complex poles.



(a)



(b)

Figure 3.14 (a) Simulated output gain response, (b) phase response of A_{amp} at the slow corner. The response shows phase margin of over 45 degrees with no complex poles .

Extreme corners (slow and fast) along with the typical corner were run to simulate the frequency performance of the amplifier, A_{amp}. The phase margin was targeted to be above 45 degrees. As evident from Figure 3.12, Figure 3.13 and Figure 3.14, the gain-frequency, and the phase-frequency plot show no complex poles or pole-zero doublet. The amplifier is unity-gain stable, and the dominant pole is far from the non-dominant frequency pole. Hence, the amplifier proved to be safe to use in a negative feedback configuration. A left plane zero is observed near the unity gain frequency, which helps improve the amplifier's phase margin.

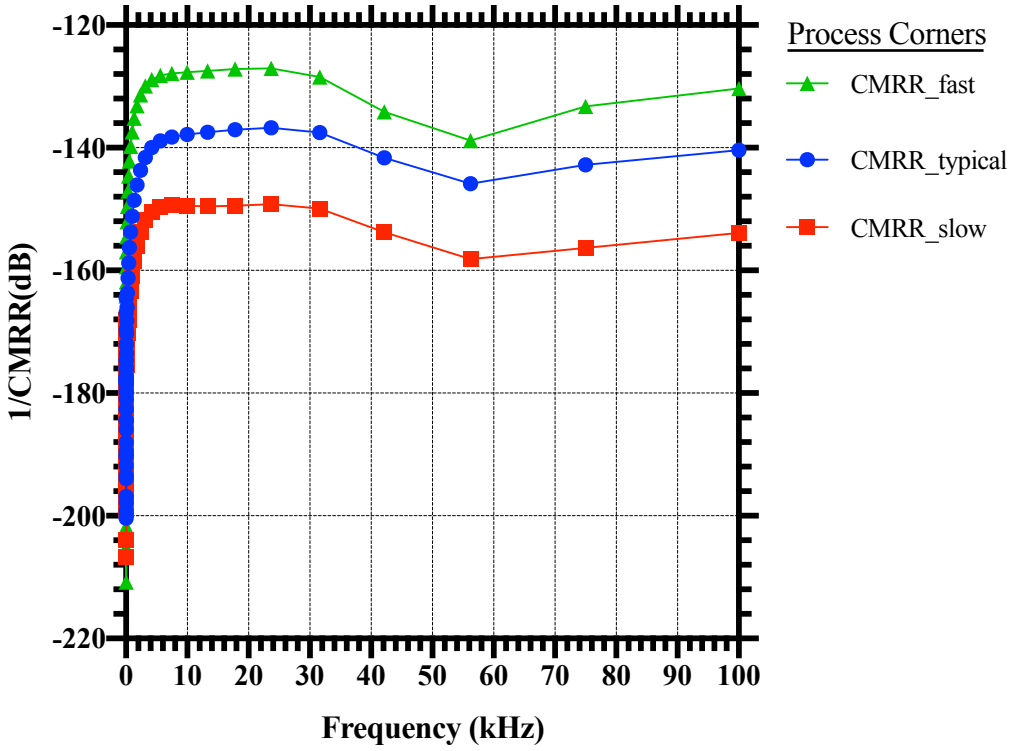


Figure 3.15 Simulated process corner common mode rejection ratio for the two-stage core amplifier, A_{amp}. Worst case common mode gain achieved is larger than 120dB (less than -120dB for negative value).

Due to the low amplitude of the EEG signals, one of the significant issues that can start appearing is the interference from the mains line. Since the signal band is very close to 50/60Hz band; this cannot be avoided by applying the filtering. The amplifier needs to have a very high common-mode rejection, for it to be robust to supply line disturbances. By using a cascode topology, the common-mode gain of the amplifier can be set to be very low. The length of the transistors M_{p7} and M_{p8} (see Figure 3.9) are chosen to be very large to aid with a high common-mode rejection (see Figure 3.15). Another critical parameter is the power supply rejection ratio (PSRR), which is helped drastically by the cascode topology. An indirect compensation scheme

was used for the proposed amplifier, to help with the PSRR as well, while conventional Miller compensation scheme is known to reduce the PSRR [33]. No unique PSRR improvement circuit was required in this topology. The results from the corner simulation for the PSRR of the amplifier is given in Figure 3.16. The indirect compensation also helped to stabilise the amplifier using a smaller capacitor value, achieving better slew rates and a higher unity-gain bandwidth [33]. Furthermore, a smaller capacitor value resulted in a smaller layout area as the compensation capacitor occupies a larger area than the amplifier's MOSFET devices.

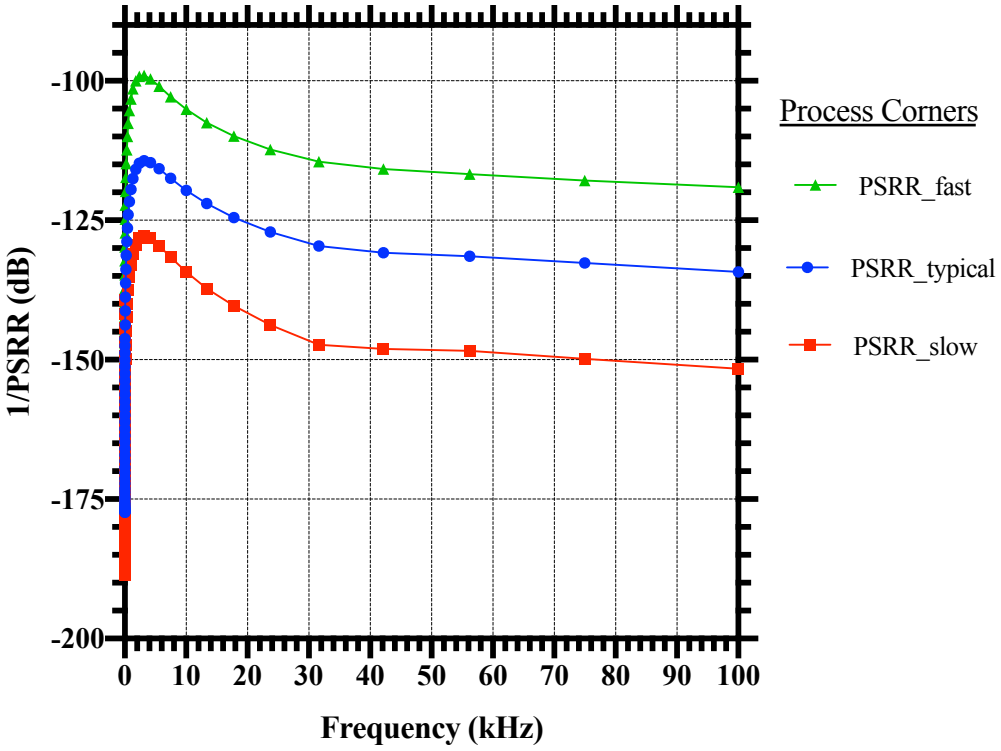
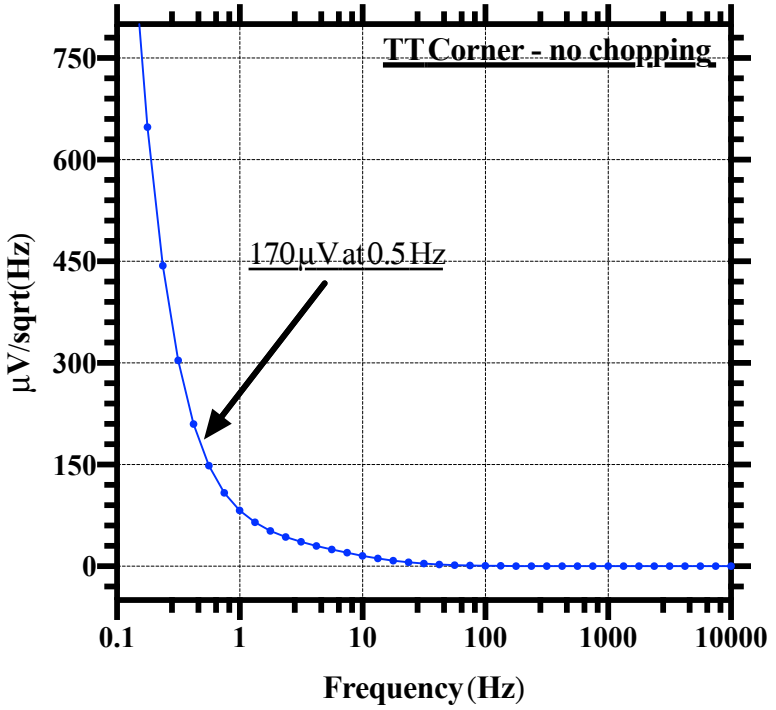


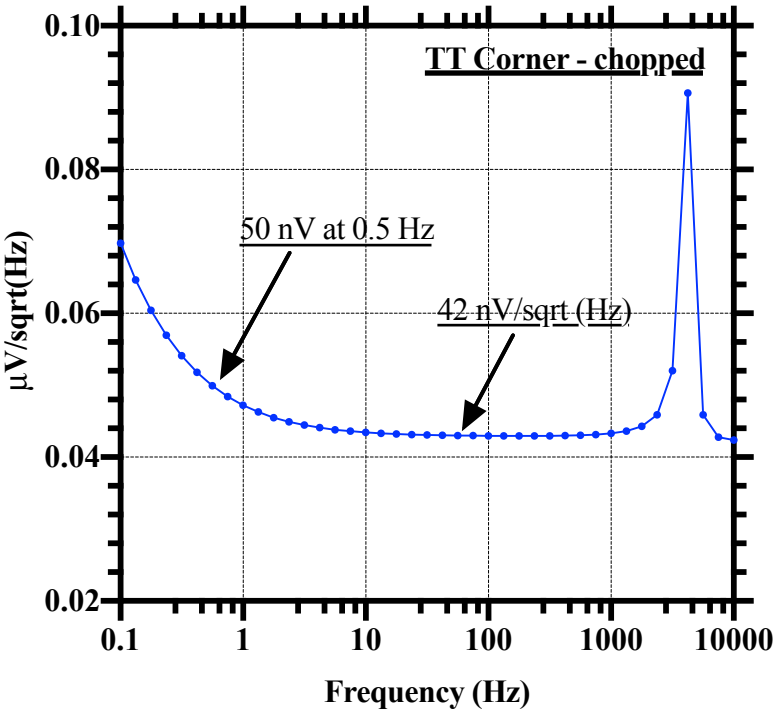
Figure 3.16 Simulated process corner PSRR for the two-stage core amplifier, $A_{amp.}$. Worst case power supply gain achieved is below -100dB.

The results of corner simulations for the input noise simulation are given in Figure 3.17, Figure 3.18 and Figure 3.19. Multiple simulations were run to compare the total input noise under chopping and without chopping. The measured input integrated noise for the two-stage amplifier after fabrication was 453nV (45.3654µ/100) in the frequency band of 0.5-50Hz (as shown in Figure 3.20), compared to 466nV simulated. This value is well within the noise budget for the EEG amplifier targeted for this research, and very close to the simulated result obtained by using pss/pnoise analysis in the Cadence simulation environment (as shown in Figure 3.17, Figure 3.18 and Figure 3.19). The bias current is 2-bit trimmable, so if needed, the noise performance can be sacrificed for smaller power consumption. The required frequency band is

0.5 to 50Hz. So, the chopping frequency used is 4kHz, which is much higher than the relevant signal band, and important to keep the 1/f noise band away (which is centred around the chopping frequency).

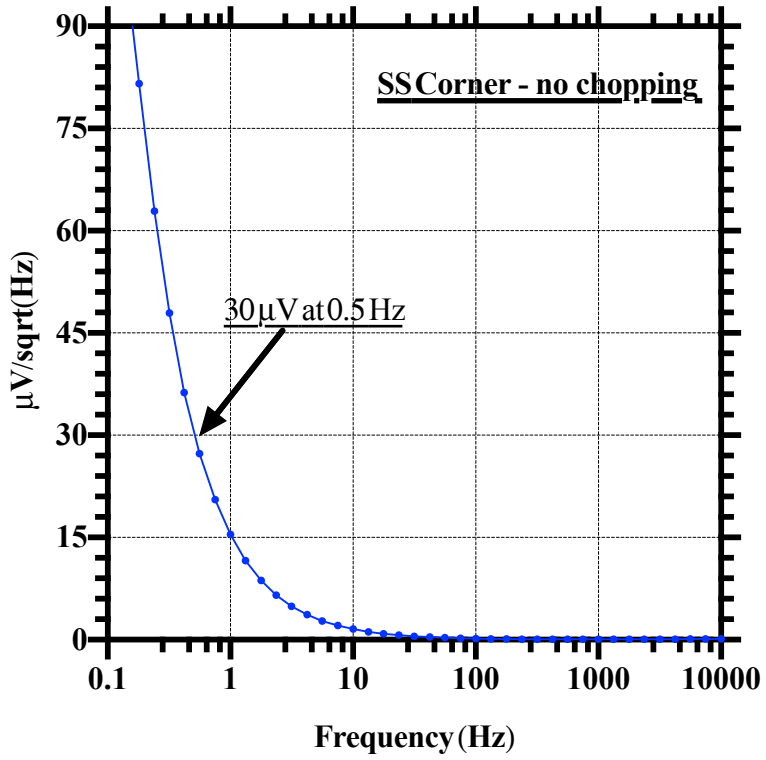


(a)

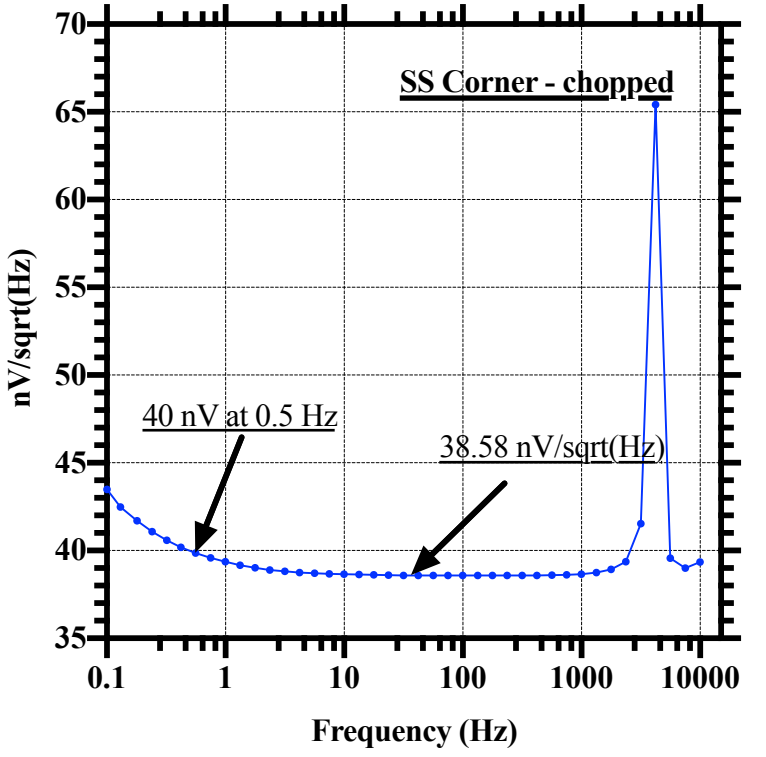


(b)

Figure 3.17 Simulated input noise density of the core amplifier, A_{amp} – (a) without the chopping, (b) with the chopping (typical corner).

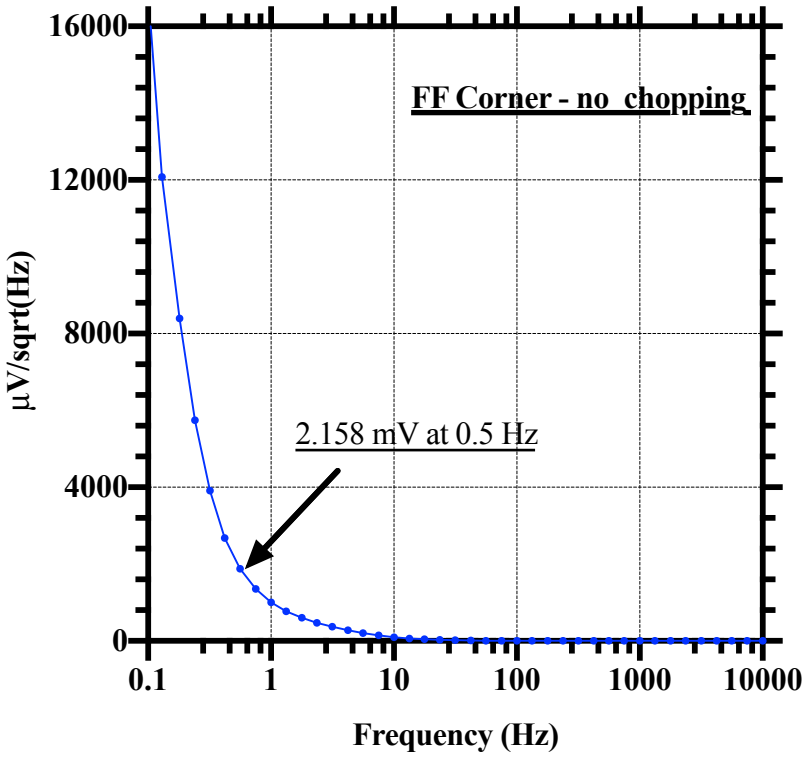


(a)

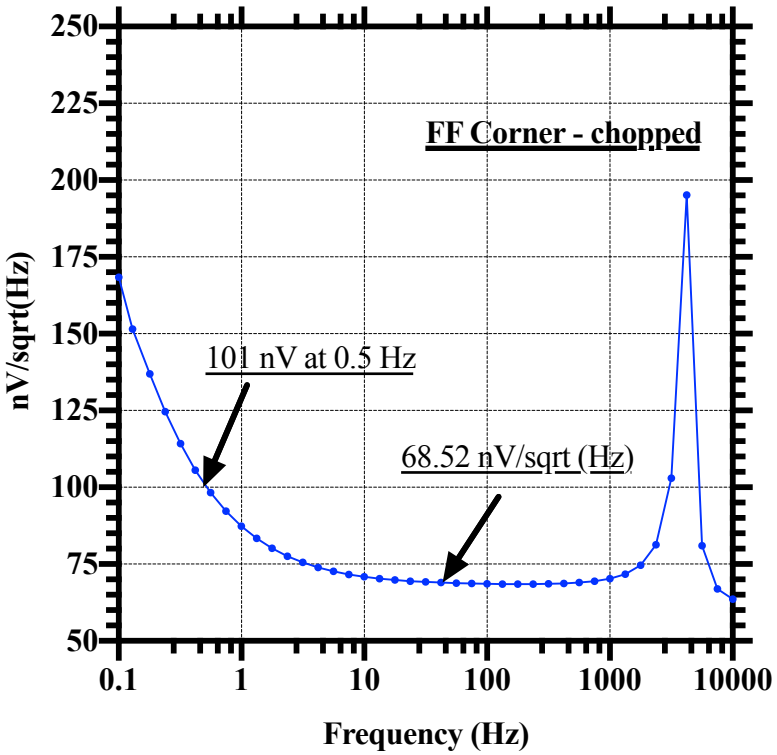


(b)

Figure 3.18 Simulated input noise density of the core amplifier, A_{amp} – (a) without the chopping, (b) with the chopping (slow corner).



(a)



(b)

Figure 3.19 Simulated input noise density of the core amplifier, A_{amp} – (a) without the chopping, (b) with the chopping (fast corner).

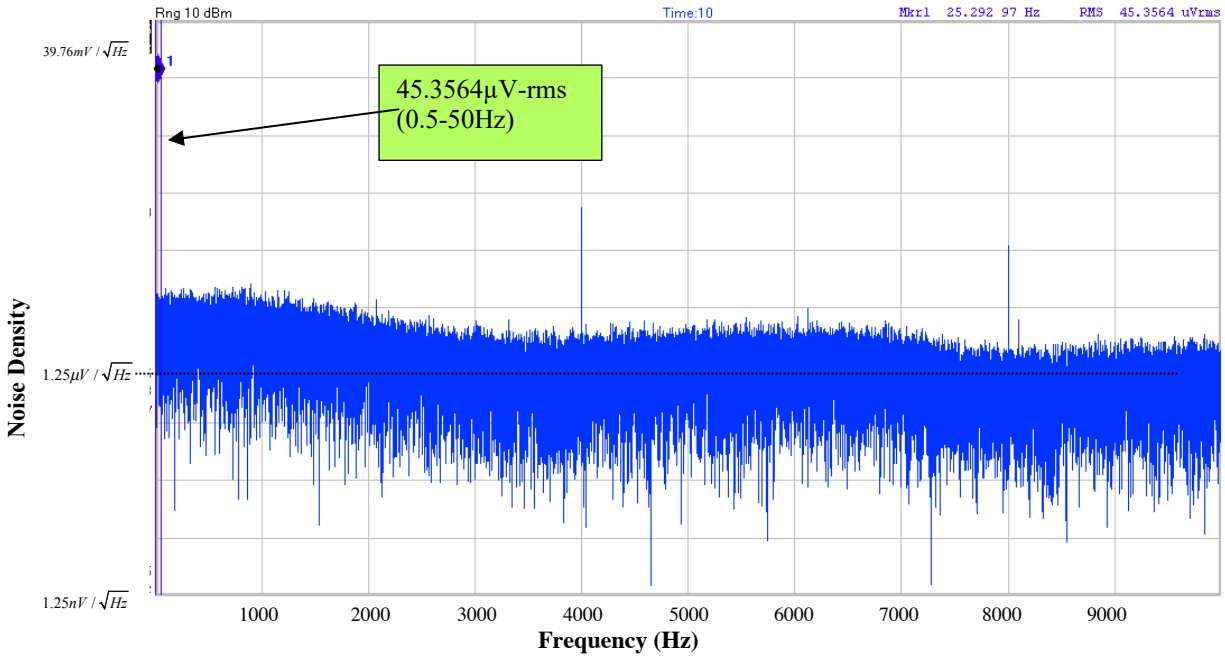


Figure 3.20 Measured output noise for the two-stage core amplifier, A_{amp} (in closed loop configuration). A closed loop gain of 100 is used (50 Ω impedance is used for the measurement).

3.7 Chopper based capacitive feedback EEG amplifier using modified pseudo- resistors (CCFEA-I)

The overall system architecture of the proposed EEG amplifier is shown in Figure 3.21. The topology is similar to designs presented in [12],[35] with some critical enhancements to meet the EEG system specifications required in this research. The integrator cut-off frequency is set through a novel high-value, low-distortion tuned pseudo-resistor with a smaller process variation (see Chapter 4 for the detail). The analogue ripple rejection loop is similar to the one used in [35]. Still, it can be turned off, as the expected offset of the A_{v1} is smaller than the design in [35], which was possible by adopting a very careful design sizing and layout strategy. Also, there is a fourth order Sallen-Key low pass filter implemented after the amplifier (see Chapter 6), so most of chopping spikes are going to be rejected before it reaches the ADC.

Chopping in the amplifier can be done before the input capacitors or at the amplifier's virtual ground node. Chopping before the input capacitors mitigate the mismatch of capacitors and improve the CMRR of the amplifier, though the switch capacitor conductance reduces the input resistance, this making necessary the use of a positive feedback loop to enhance it [12],[35].

Chopping at the virtual ground causes the CMRR to drop; this is why chopping is performed before the input capacitor in this implementation. A positive feedback loop similar to the one presented in [35] is being used to increase the amplifier's input resistance.

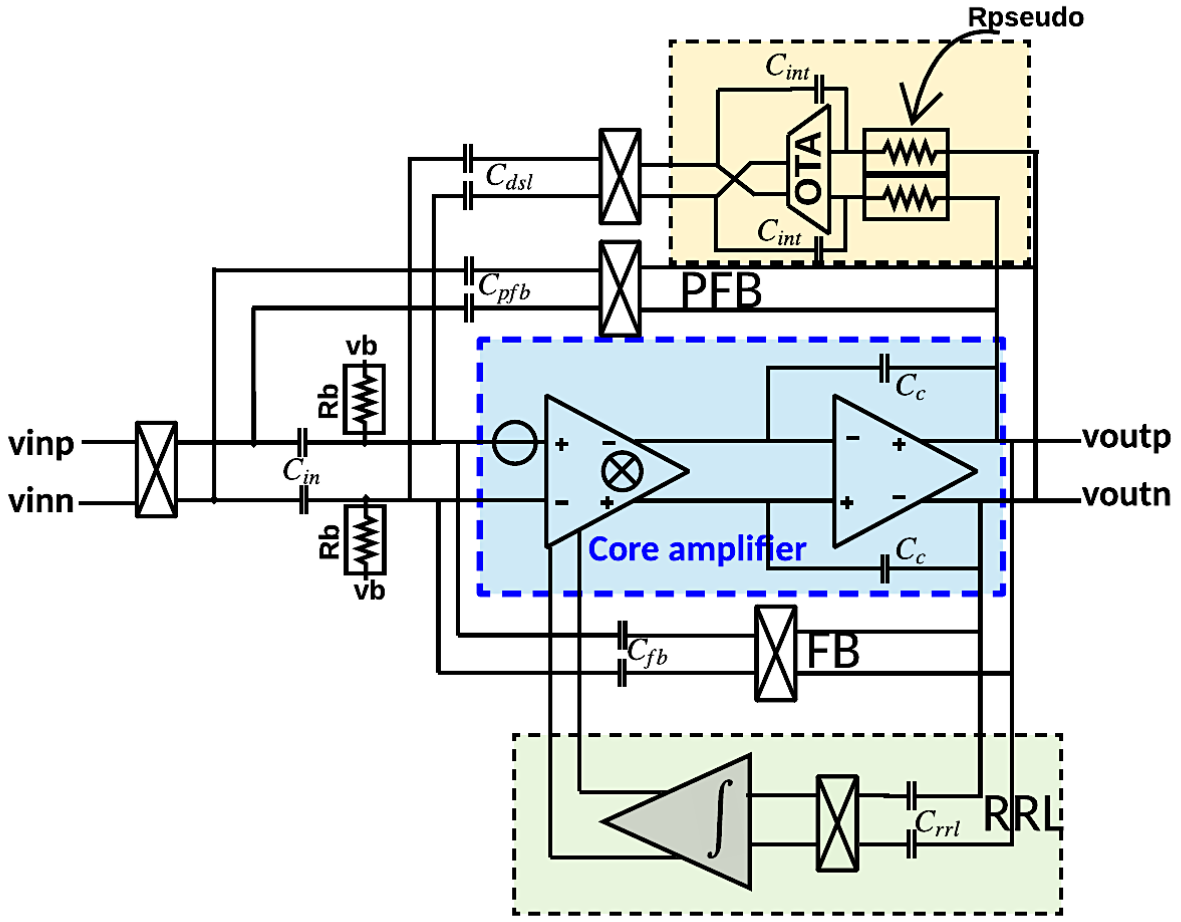


Figure 3.21 Chopped capacitive feedback EEG amplifier (CCFEA-I) with PFB, DSL and RRL loop.

Applying the chopping before the input capacitor causes one more key concern to resolve. The DC electrode offset is modulated with the input signal and needs an offset cancellation loop to reject the DC offset. This architecture used a DC servo loop (DSL) similar to [35] for rejecting this offset. [35] used a high-value resistance caused by the off-state leakage resistance of the MOS transistor to set the integrator's cut-off frequency. This resistance value is poorly modelled in the process design kit, so it is difficult to estimate before the fabrication, and it is susceptible to the process variations, and temperature variations. And the high pass cut-off can fluctuate by as much as ten times [8]. In order to circumvent the issue of the resistor variation, a tuned pseudo-resistor was used, which was showing two times variation in the simulation. Also, an

analogue calibration loop was proposed to set the pseudo-resistor value, with the three sigma variation of 8.25% (see Figure 3.48). The amplifier in [35] used a capacitor value of 500pF to reduce the DSL noise. Here, a low-noise telescopic amplifier is used in the DSL, which does not add a lot to the amplifier's total noise.

The amplifier's DC gain was set by the ratio of the input and feedback capacitors, which is very tightly controlled in the CMOS process, so gain trimming is not required. The gain was chosen to be fixed 100. Appropriate sizing was used for capacitors, so as not to increase the chopping spikes considerably. Also, the modulator switches were moderately sized to avoid the clock feed-through, but not small enough to raise the core-amplifier's thermal noise floor. Also, half-size dummy transistors were used to decrease the charge injection [7].

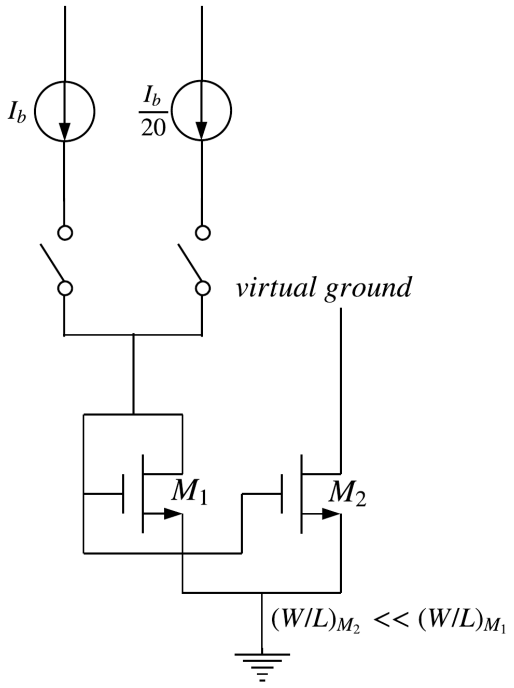


Figure 3.22 Additional current source for speeding-up the transient settling in the simulation [6].

The virtual ground node of the amplifier was biased by using a scheme similar to [6] (see Figure 3.22). Here a large resistance was obtained by using long-FET (W/L>>1) transistors. The advantage of this approach was to have a large impedance, enough to bias the amplifier in the right region of operation for a large gain, without adding too much noise and tolerating any effect of common-mode perturbations. A slight modification was the addition of extra current equal to $1/20^{th}$ the bias current value, for reducing the resistance at the start of the simulation,

hence helping with the transient settling. The total noise for the amplifier, CCFEA-I, including contribution from pseudoresistors, DSL, feedback loop is proportional to the input referred noise of the differential pair [22], and can be given as:

$$v_{n,amp} = \left(\frac{C_{tot}}{C_{in}} \right) v_{n,gm1} \qquad \ldots(3.21)$$

where, $v_{n,amp}$ is the total noise of the amplifier, $v_{n,gm1}$ is the input referred noise of the first stage differential amplifier, C_{tot} is the sum of the capacitors at the input node – including C_{in}, C_{dsl}, C_{fb}, C_p (parasitic capacitance posed by the large size of differential pair). The DSL used in the implementation incorporates an integrator that amplifies the DC signal at the output of the amplifier and rejects the relevant EEG signal. This DC-offset is then up-modulated and fed-back to the amplifier virtual ground by capacitors, C_{dsl}. The integrator continues integrating until the output is free from any DC offset. The high pass frequency cut-off corner created by the DSL is given by [12-13]:

$$f_{hp} = \frac{C_{dsl}}{C_{fb}} f_{0dsl} \qquad \ldots(3.22)$$

where f_{0dsl} is the unity gain frequency of the integrator used in the DSL. This high pass corner frequency is set to be 0.5Hz for EEG signals. The values of C_{dsl} can be determined from the equation [12-13]:

$$V_{out\max} = \frac{C_{in}}{C_{dsl}} V_{offset} \qquad \ldots(3.23)$$

where $V_{out\max}$ is the output of the integrator (1V in this case), V_{offset} is the DC electrode offset (around ±50mV for the wet electrode and used for this research), with C_{in} = 40 pF, the C_{dsl} should be 2pF. This gives the f_{0dsl} to be 0.1Hz. To alleviate the requirement of such a low cut-off frequency for the DSL, C_{dsl} can be increased. Adopting this approach has the critical problem that the noise of the integrator is amplified by the factor C_{dsl}/C_{fb} before appearing at the output of the amplifier. Also, increasing C_{dsl} will increase the noise floor of the amplifier, as can be seen from equation 3.22. To implement such a low bandwidth integrator, this required the following special considerations. If the capacitor was chosen to be 10pF, a resistor of 160$G\Omega$

had to be implemented on-chip. For this reason, pseudoresistors were used for this amplifier, since no other implementation alternative would have been feasible.

A significant issue with using chopping to reject the *1/f* noise is that the input chopper along with input capacitors (C_{in}), limit the input impedance of the amplifier to be $1/2f_{chop}C_{in}$ (where f_{chop} is the chopping frequency). A widely used method to cancel out this effect is to use a positive feedback loop (also called impedance boosting loop)[35]. This PFL consists of a chopper switch and a feedback capacitor (C_{pfb}). This positive feedback loop is capable of generating a compensation current which is equal to feedback current across C_{fb}, so no current is drawn from the input signal source. And hence, this approach can boost up the input impedance by 25 times [38]. Here C_{pfb} is chosen to be of the same value as C_{fb} (see Figure 3.21). The bias resistors, R_b, in Figure 3.21 are implemented as PMOS transistors biased in the subthreshold region with noise density under $10nV/\sqrt{Hz}$, which does not contribute much to the total amplifier noise [6]. A positive feedback loop similar to [35] is used to increase the input resistance of the amplifier reduced by the chopping conductance. The offset of the amplifier, A_{v1} in the core amplifier and the *1/f* noise will be upmodulated and can generate a large ripple at the output of the amplifier. This ripple voltage can be given as [13]:

$$V_{ripple} = \frac{V_{os}g_{m1}}{2f_{chop}C_{cc1,2}} = \frac{3mV \times 20\mu S}{2 \times 4kHz \times 36pF} = 208.3mV \quad \ldots(3.24)$$

where, V_{os} = 3mV (amplifier offset due to random and systematic mismatches), g_{m1} = 20μS is the transconductance of the amplifier, f_{chop} = 4kHz, $C_{cc1,2}$ = 36pF is the compensation capacitor used. This ripple voltage of 208.3mV is very large for a 1V supply, and can be reduced by reducing the offset in the A_{v1} amplifier. A dc-offset calibration similar to [39] can be used to reduce the offset, V_{os} of the amplifier by 40x, which eventually will reduce the output ripple, V_{ripple} to 5.2mV, that is tolerable in the given application. An analogue ripple rejection loop (RRL) presented in [13] is used in this research as a backup in case offset V_{os} of the amplifier A_{v1} comes out much larger than simulated 3mV after fabrication. An important thing to notice here is that the RRL (ripple rejection loop) has an inherent -6dB notch at the chopping frequency (4*k*Hz in this case – see Figure 3.23). The presence of this notch reduces the chopping spikes around the frequency of 4kHz, and in some cases, the low pass filter may not be needed before the SAR ADC.

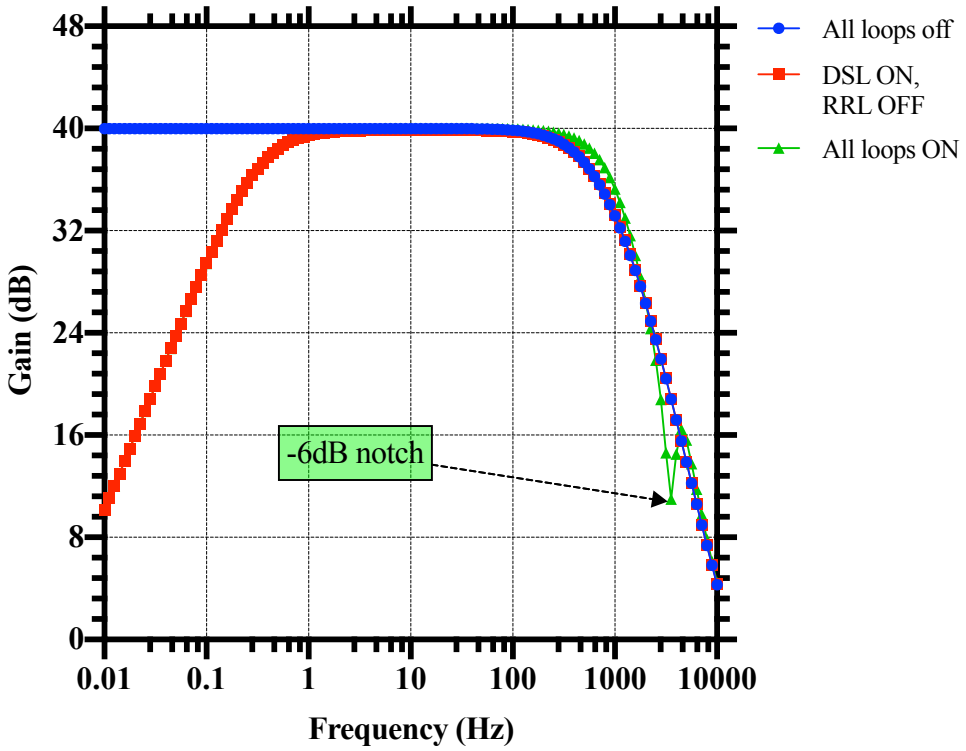


Figure 3.23 Simulated gain transfer function of the CCFEA-I (using Cadence's pss/pac analysis).

In this research, a DDA based fourth-order low pass filter is designed to reduce the chopping, and hence the SAR ADC does not need to have a significantly broad input range. The simulation results for the input-referred noise estimation for CCFEA-I are given in Figure 3.24, for the condition where both the DC rejection servo-loop and the ripple rejection loop are disabled. Multiple current values are used to estimate the noise performance. This bias current can also be trimmed in the final implementation of the chip after fabrication. As can be observed from Figure 3.24, the noise density for the amplifier goes down from 56.1nV/sqrt(Hz) to 32.8 nV/sqrt(Hz), when the bias current value is increased from 30nA to 100nA. But this mode is only used to compare the noise added by the DSL. Such mode cannot be useful if the amplifier has to be used in any biopotential recording as the DC offset is always present due to impedance mismatches of the electrode. The integrated input referred noise for the second case (considering 50Hz bandwidth), where DSL was ON and the RRL was off for the nominal case of f_{chop}= 4kHz, ibias = 50nA (total power = 1.8µA) can be calculated as:

$$= 55.76 \times \sqrt{50} \times 1.57 \ = 619.02 \text{ nV} \qquad \ldots(3.25)$$

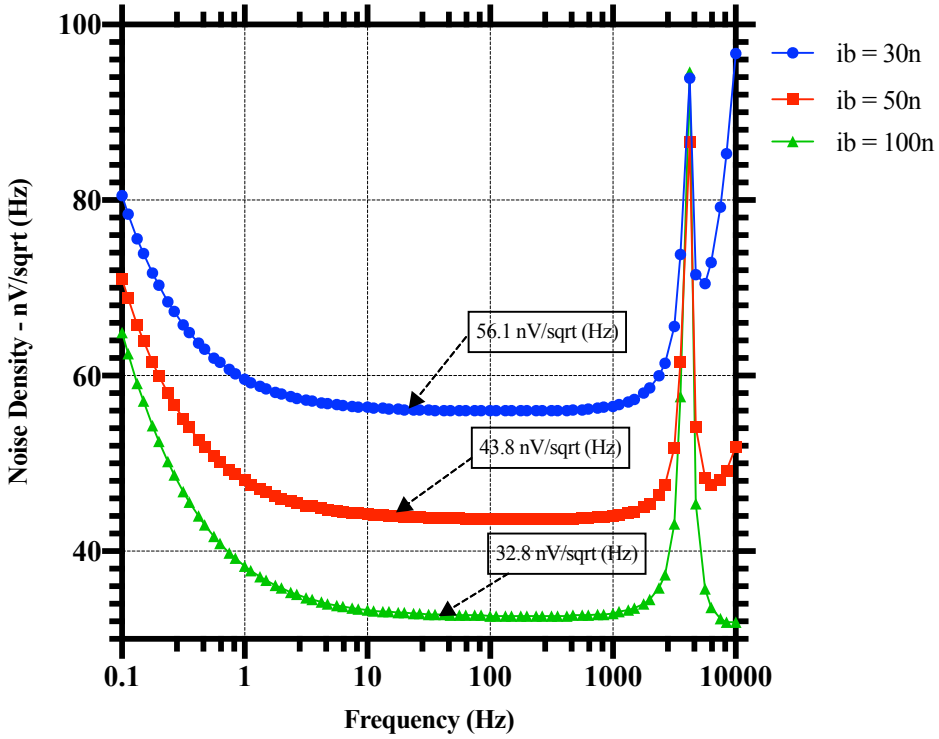


Figure 3.24 Simulated input referred noise simulation, using Cadence's pss/pnoise analysis – DSL and RRL are disabled.

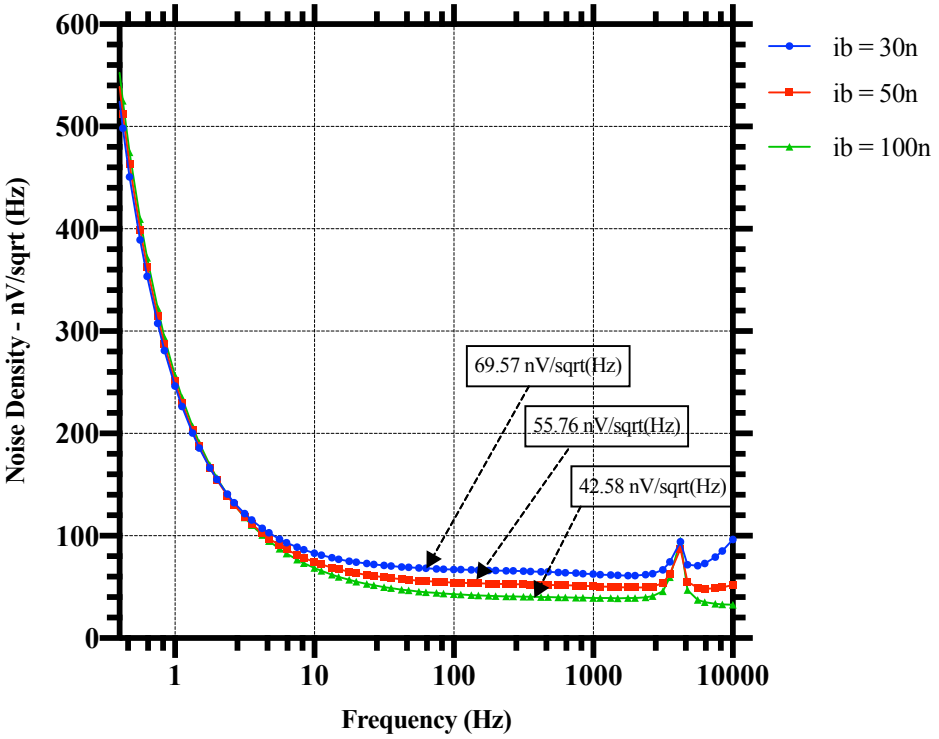


Figure 3.25 Simulated input referred noise simulation, using Cadence's pss/pnoise analysis – DSL is ON and RRL is off.

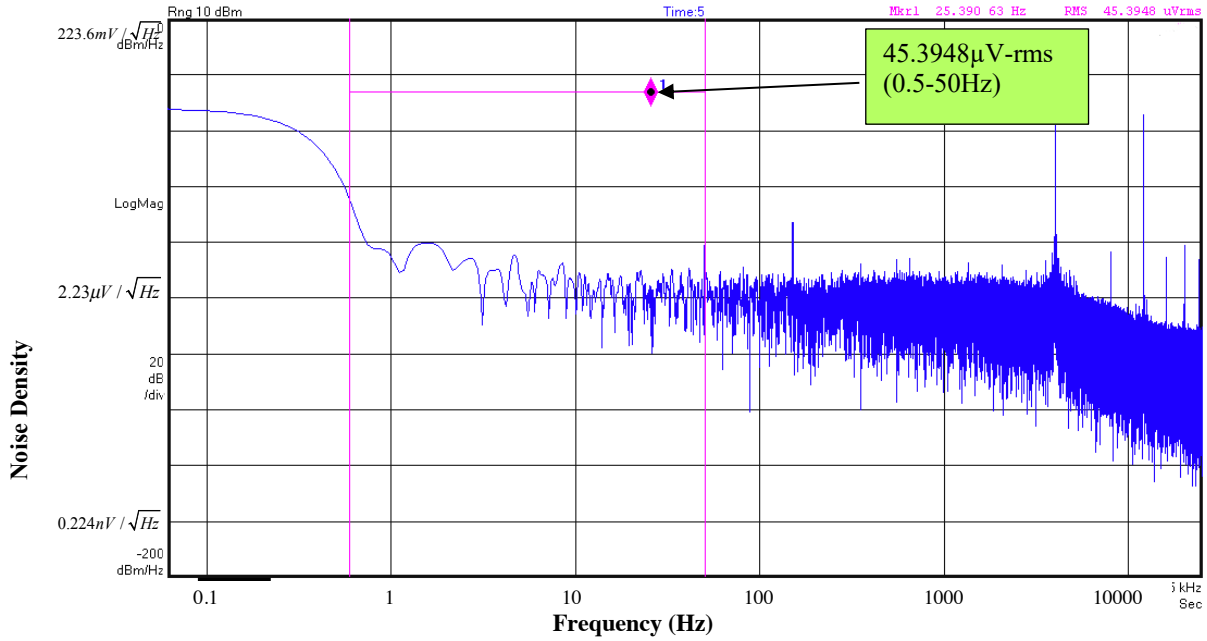


Figure 3.26 Measured output noise for the CCFEA-I when RRL is off (50 Ω impedance is used for the measurement).

For a chopping frequency of 8*kHz*, the measured noise reduces to 454nV (see Figure 3.26).

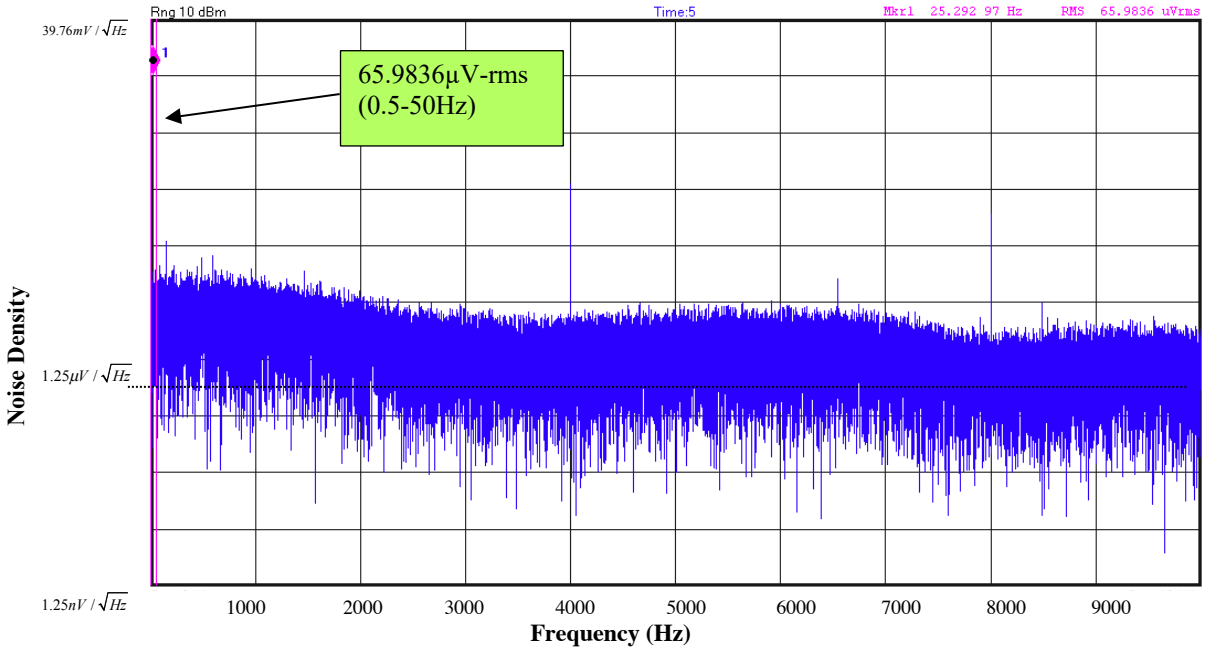


Figure 3.27 Measured output noise of the CCFEA-I for the condition when both DSL and RRL are ON (f_{chop} = 4kHz) (50 Ω impedance is used for the measurement).

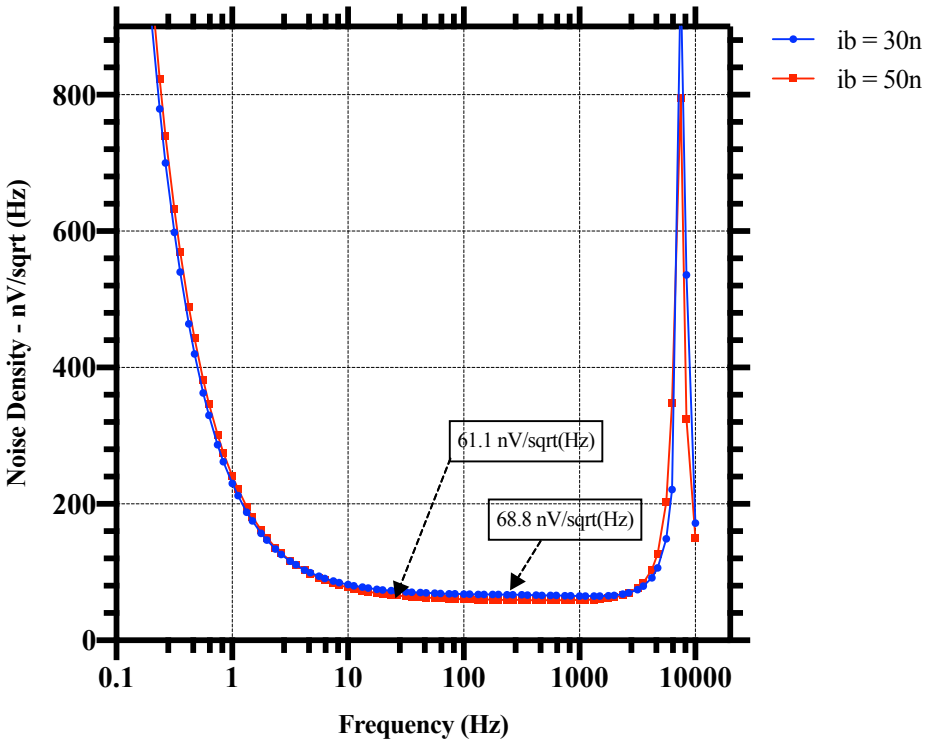


Figure 3.28 Simulated input referred noise simulation, using Cadence's pss/pnoise analysis – DSL and RRL both are ON.

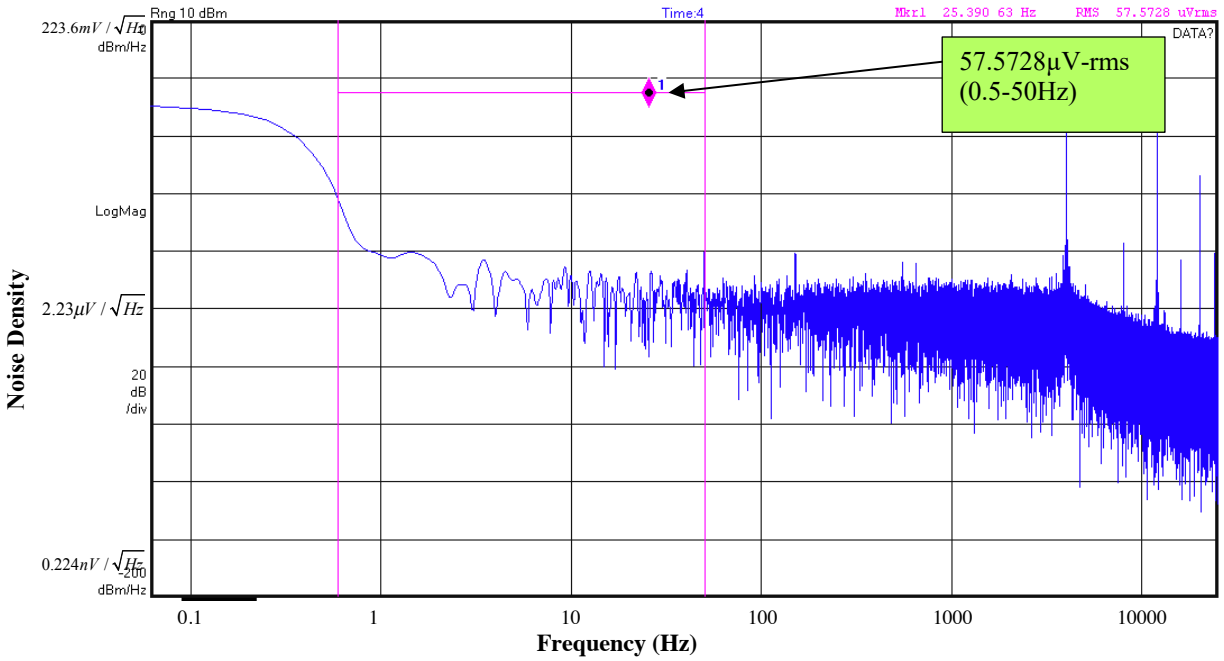


Figure 3.29 Measured output noise for the CCFEA-I when both loops are active, and ibias=75n (50 Ω impedance is used for the measurement).

For the third case of DSL and RRL ON, the integrated noise increased to 678.3nV (measured was 660nV – see Figure 3.28 for the simulated, and Figure 3.27 for the measured). And the power consumption increased to 2μA (200nA in the RRL). For a total current consumption of 3μA, the input-referred integrated noise when all loops were active, was 575.728nV (see Figure 3.29).

The layout implementation of the amplifier is shown in Figure 3.30. The matching of the capacitors is generally good in the submicron technology. Also, any mismatch can be taken care of through the chopping implementation. Most of the signals were laid out symmetrically so as not to cause cross-coupling and the cross-talk. Sensitive signals were shielded whenever required, and also clock signals for the chopper were shielded to avoid impacting the signal laid out nearby. Additionally, a minimum separation of 1μm was used to isolate digital signals from sensitive analogue signals.

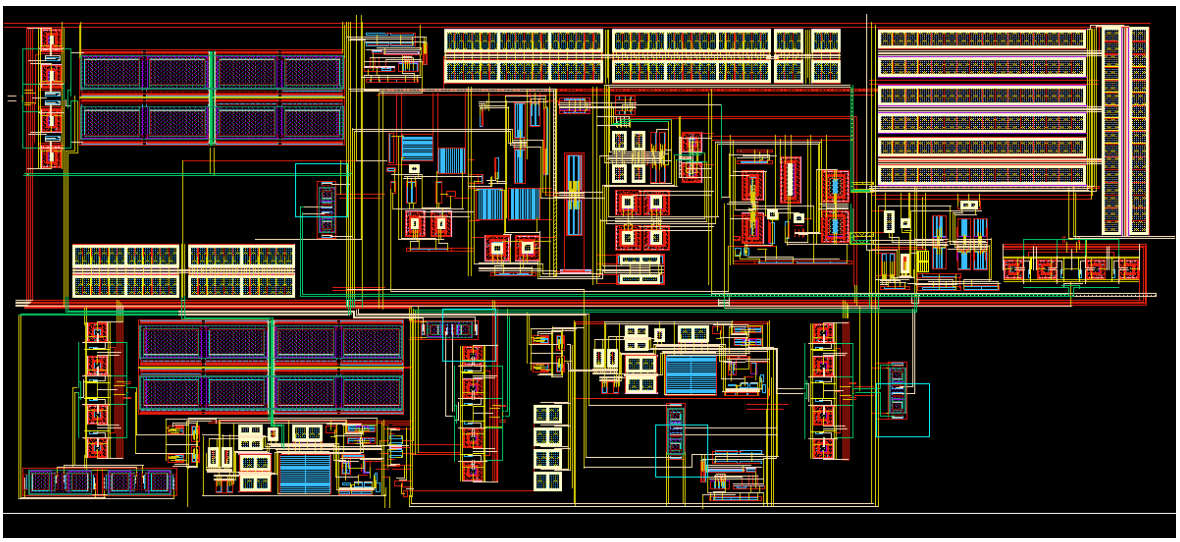


Figure 3.30 Layout of the chopped capacitive feedback amplifier.

Another significant source of the error could be transient currents through the substrate. As the high activity clock signal can cause quick transient current steps, and that can cause latch-up issues, or enter into sensitive analogue signals. One of the approaches for avoiding this is to put digital and analogue in separate deep n-wells, but that could cause a significant area penalty. The approach used here was to use a double guard ring that should provide a low resistance path for this transient noise.

To take care of the matching of transistors, a common-centroid layout approach has been used (see Figure 3.31). A dummy transistor has been used on both sides to create a separation between the matched device and the isolation trench. Separation between 3-5µm has been used. This separation should reduce the STI (shallow trench isolation) stress effect on the matched devices.

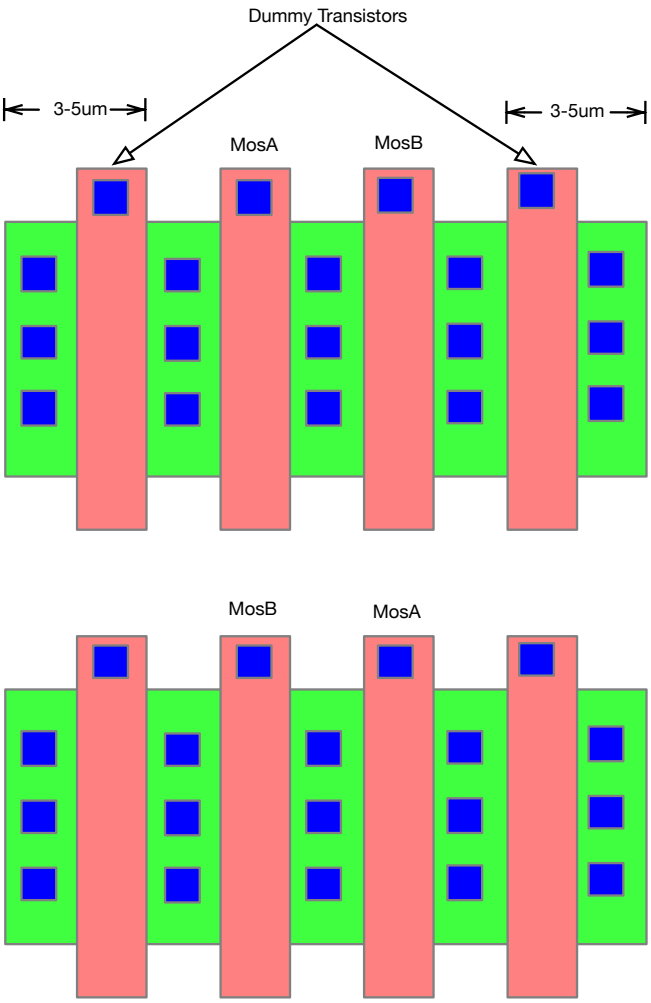


Figure 3.31 Common-centroid layout matching pattern along with dummy transistors.

As a rule of thumb, all gain devices were common-centroid matched, whereas the current mirror matched devices were used in the interdigitated pattern (see Figure 3.32). Again, with interdigitated devices, dummy transistors were used on both sides. Bigger size MOS transistors were divided into smaller unit size, and multi-fingers were used. That improved the matching considerably and also helped with the layout density.

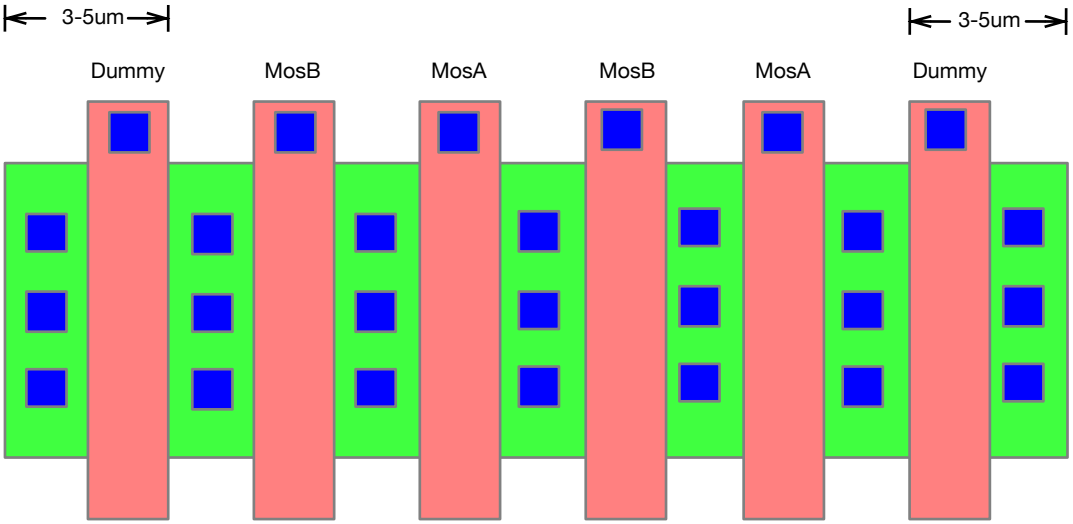


Figure 3.32 Interdigitated layout matching pattern along with dummy transistors.

A stimulus was provided at the input of the amplifier, CCFEA-I on the PCB to test the dc offset rejection of the amplifier (see Figure 3.33). The input was a 2mV sine wave, with a dc offset of 50mV. From the measurement, it is evident that the amplifier is capable of rejecting the dc offset and retaining close to 40dB gain. The offset V_{os} of the amplifier, A_{v1} was not very large, so the RRL is not needed in the final measured chip. The test setup showed 50Hz supply noise at various input, but appropriate care was taken so as not to corrupt the sensitive signals. Also, the fully differential implementation rejected most of the mains transient.

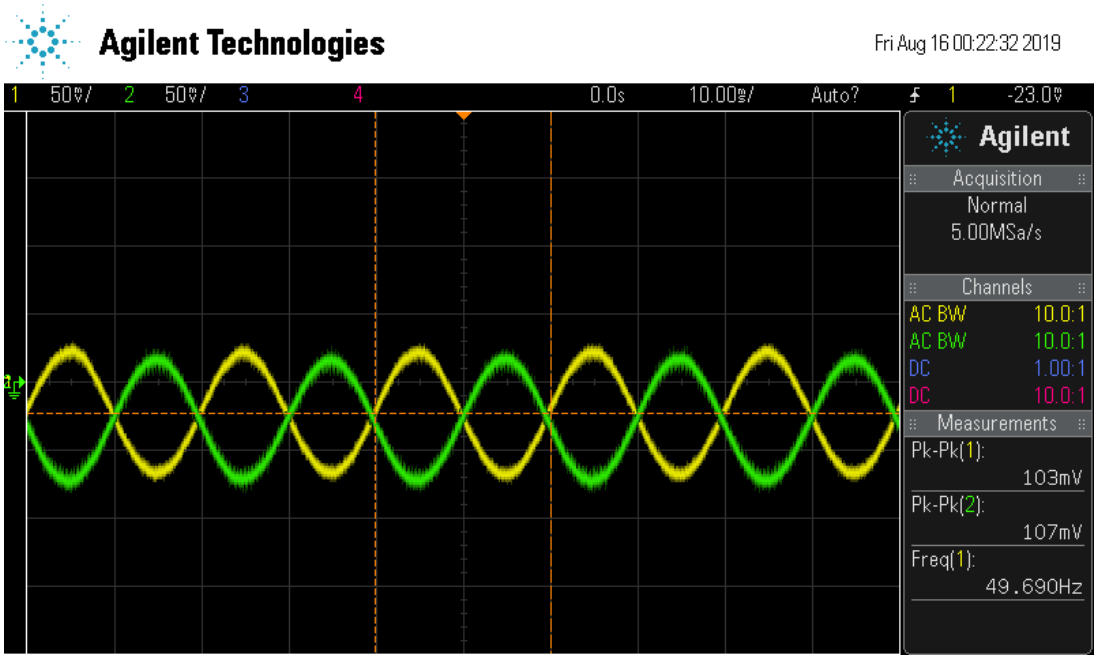


Figure 3.33 Measured stimulus response for the CCFEA-I with a 2mV peak to peak sine wave and a 50mV DC offset.

3.8 Chopper based capacitive feedback EEG amplifier using duty-cycled resistors (CCFEA-II)

A significant issue seen with pseudoresistors (PRs) is their large variability over time, temperature and the process (see Chapter 4 for details on this) [38]. This variation may be acceptable in the majority of applications, but for a very high precision systems that could be a problem. Since the pseudoresistor in the DSL sets the high pass corner frequency (HPF), it is essential to have low variability in the value of PR; otherwise, HPF can move and start clipping the relevant signal. So, another architecture is proposed where a multi-rate duty-cycled resistor (MDCR) similar to [38] is used instead of a PR. Before going to the functioning of a MDCR, the functionality of a duty-cycled resistor (DCR) is discussed below. A DCR, shown in Figure 3.34, consists of a high precision unsilicided resistor along with a switch in series. On applying a clock signal with a duty cycle factor of *Dx*, the apparent resistance across this DCR will be equal to *R/Dx*.

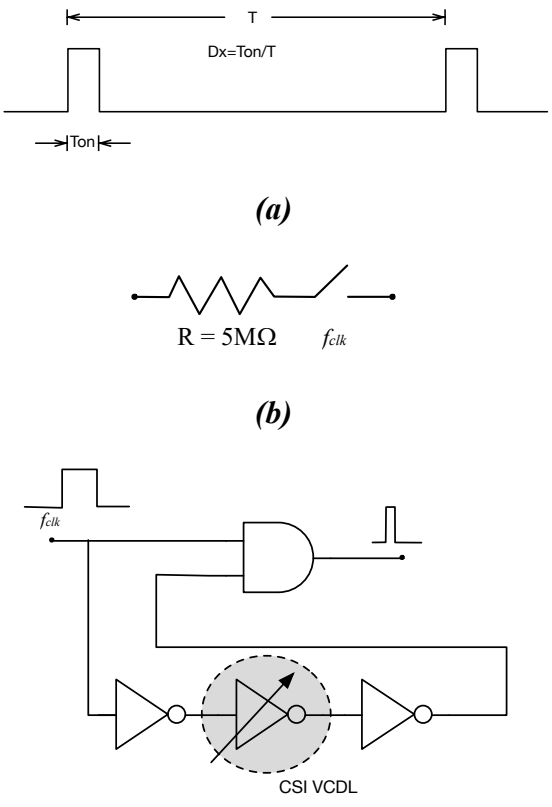


Figure 3.34 (a) Timing signal for the duty cycled resistor, (b) A duty-cycled resistor (DCR) [8], (c) Pulse generator circuit with current starved inverters voltage control delay line (CSI-VCDL) [40].

By using, $R = 5M\Omega$, f_{clk} = 4*kHz,* Ton = 12.5ns:

$$Dx = \frac{12.5n}{250\mu} = \frac{1}{20000} \quad \ldots(3.26)$$

$$\mathrm{Re}q = \frac{R}{Dx} = 5M\Omega \times 20000$$

$$= 100G\Omega$$

So, a 5MΩ resistor can be converted to a 100GΩ resistor, as long as the following two conditions hold true [8]:

1. The signal at the input of the DCR is a low frequency signal (a low pass filter can be used to meet this condition).

2. The RC delay of the DCR is much slower than the Ton period, i.e. RC >>Ton (where, C is the load capacitance attached to the output node).

The basic concept of the duty cycled resistor is explained in Figure 3.34. A very thin pulse of duty cycle *Dx* is used to control a switch connected in series to the resistor. This thin pulse is generated using the circuit show in Figure 3.34(c). Also, a current starved cascaded inverter-based voltage-controlled delay line (similar to [40]) is used to control the pulse width (see Figure 3.35).

The control voltage, V_{ctrl}, can be used to increase the current in the inverters. By increasing or decreasing the current value, the delay of the inverter can be altered. Also, a resistor, R (see Figure 3.35), was used to linearize the squared voltage-current relationship in a saturated NMOS device. The NMOS device used was a deep N-well device to remove the non-linearity due to bulk body-effect.

By using the DCR, the variability of setting high pass frequency eventually reduced from 1000%-2000% to 20-30%. Since, the high precision resistor is around 10% in this process, the only other variable is the accuracy of the delay line. This can be set to a very accurate value and can be further trimmed by using a control voltage (see Figure 3.36).

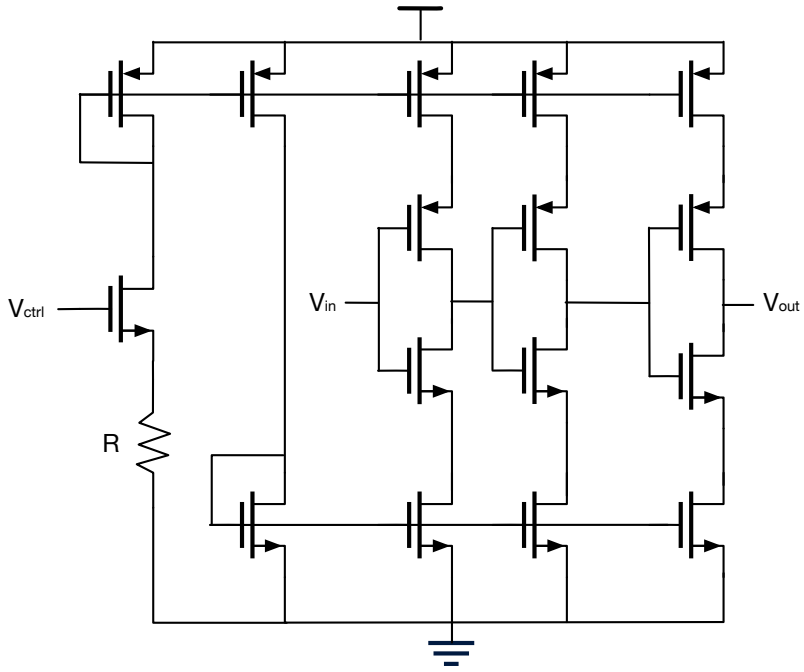


Figure 3.35 A current starved cascaded inverters voltage controlled delay line (CSI-VCDL) used to control the pulse-width [40].

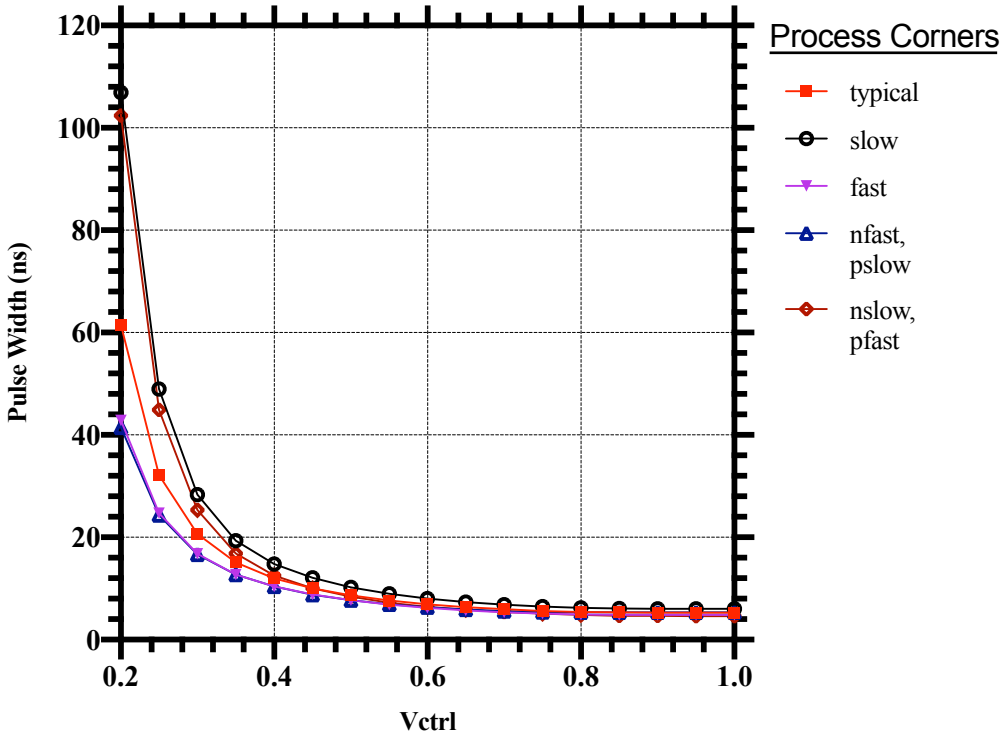


Figure 3.36 Simulated process corners result for the pulse width variation.

Also, by carrying out a noise analysis similar to the one in [8], it can be proven that the integrator using a DCR has the majority of the circuit noise confined below the corner frequency of $Dx / 2\pi RC$. So, moving this corner frequency below the frequency band of interest should help to avoid the majority of the noise, and the total contribution to the amplifier noise should eventually be less than a switched capacitor integrator. For the same reason, a corner frequency of 0.1Hz is selected for the integrator in the dc servo loop (DSL), as the frequency band of interest is 0.5Hz.

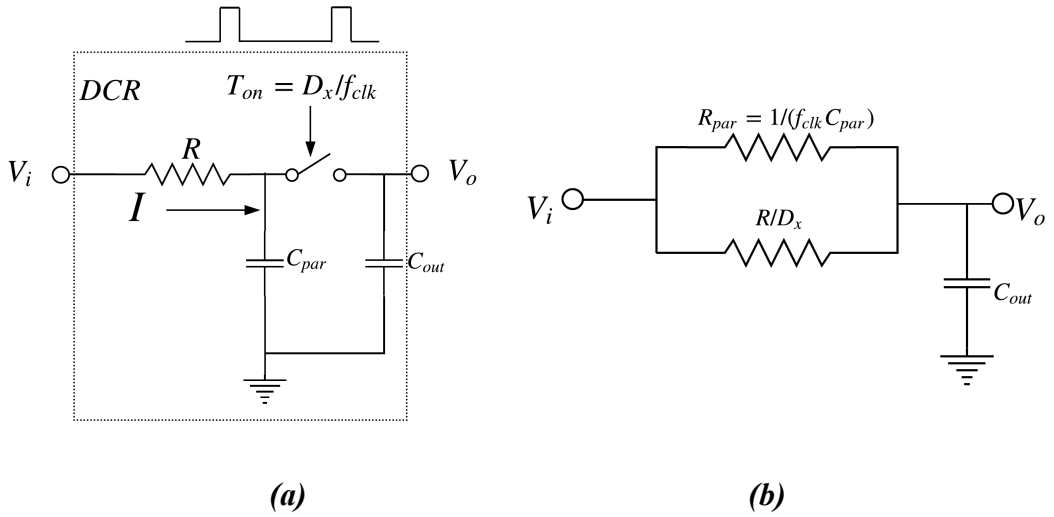


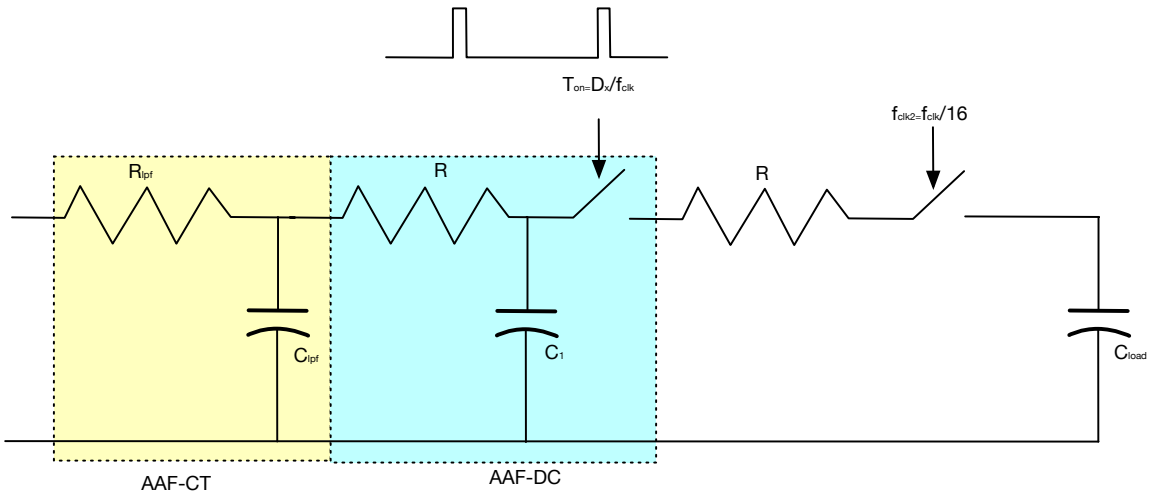
Figure 3.37 (a) Parasitic capacitor in the low pass filter build by a duty cycled resistor, (b) Equivalent circuit of the LPF.

The frequency response of first stage AAF-CT (analogue anti-aliasing, continuous time), second stage AAF-DC (analogue anti-aliasing filter, duty cycled) and the integrator is presented in the Figure 3.38(b). C_1 is chosen to be 0.8*p*F, to get a cut-off bandwidth of 10Hz.

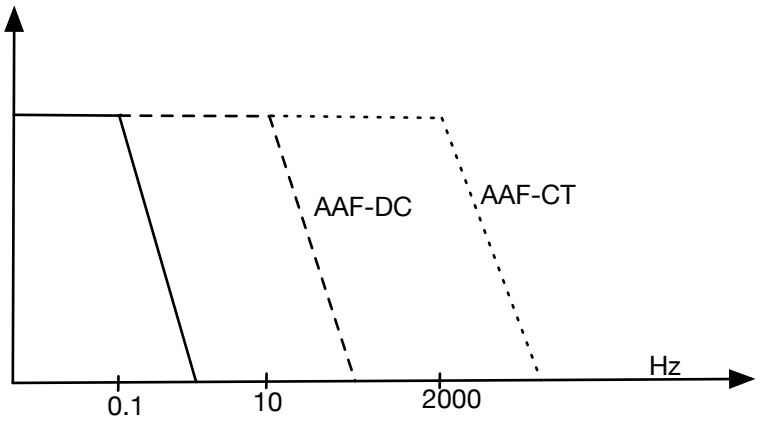
A significant issue with the DCR is that the absolute maximum resistance that can be achieved is limited by the parasitic capacitance on the resistor node. This capacitance is a technology parameter that exists due to the substrate capacitance of the resistor and cannot be removed, and appears as a parallel resistance to the DCR. Reducing the frequency is a good alternative, but that will come with a cost of increased noise, and is limited to twice the signal level to avoid the aliasing.

In [38], a multi-rate duty cycle resistor (MDCR) is being proposed, which is also used in the DSL of the CCFEA-II. An analogue anti-aliasing low pass filter continuous time (AAF-CT)

using a high-density poly resistor along with the MOS capacitance is employed to reduce the input signal frequency at the input of the duty-cycled anti-alias filter (AAF-DC) and also to avoid aliasing the chopping spike (see Figure 3.37).



(a)



(b)

Figure 3.38 (a) Multi-rate duty cycle resistor used in the CCFEA-II, (b) Frequency response of the MDCR [38].

The AAF-CT should not be required if the main amplifier's bandwidth is restricted. The frequency of the switch connected to AAF-DC is chosen to be same as chopping frequency, f_{chop}=4kHz. The frequency of the next DCR can be smaller, f_{chop}/16 in this case, which is 250Hz. By using the MDCR, the limitation due to the parasitic capacitance is avoided in the final

implementation. A resistance of $1M\Omega$ is used in this design, effectively giving a MDCR of $320G\Omega$. This, along with the capacitance of $5p$F, is used to achieve the f_{0dsl} of 0.1Hz.

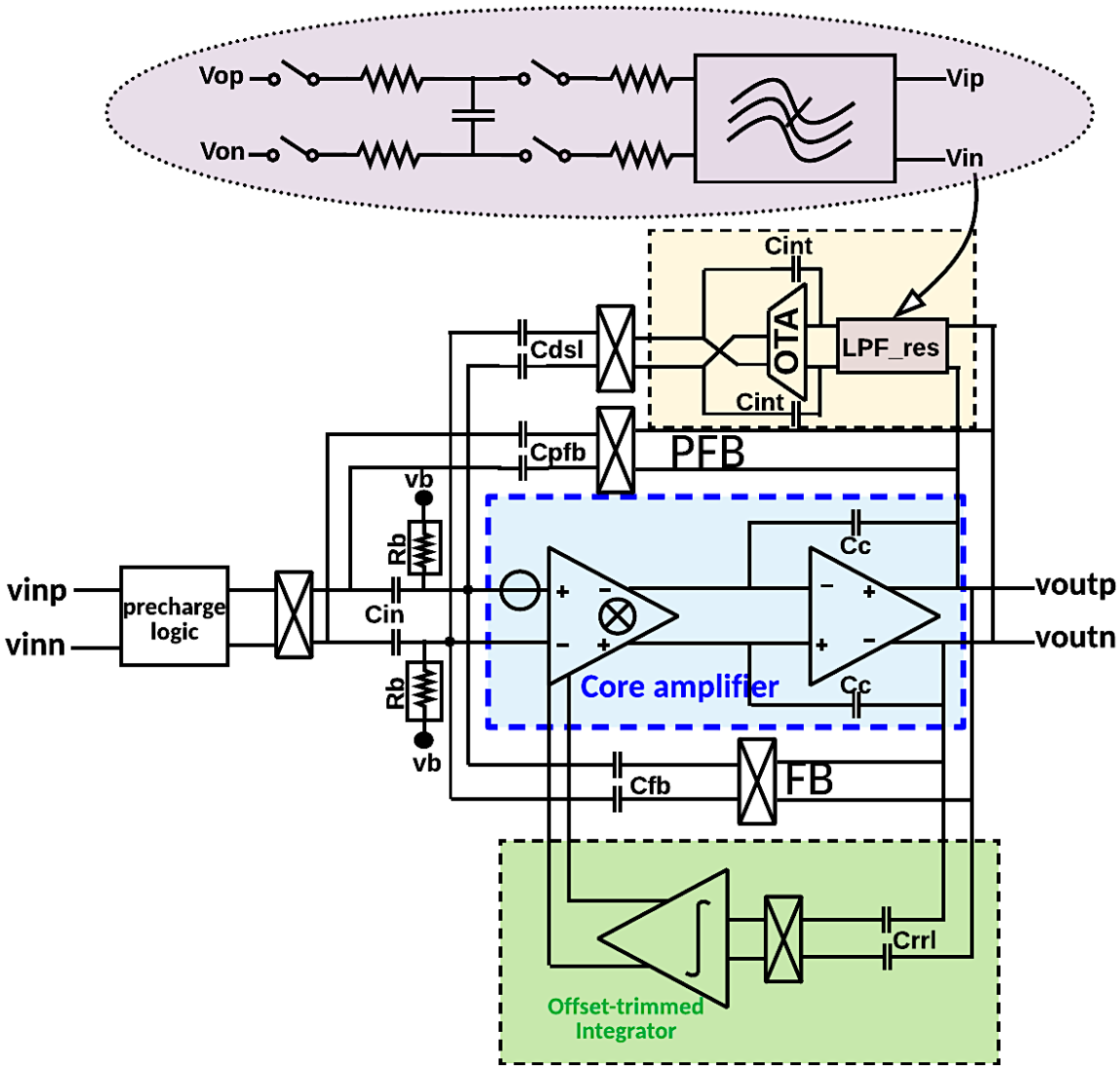


Figure 3.39 Chopper based capacitive feedback EEG amplifier (CCFEA-II) with PFB, DSL and RRL loop. A switched-resistor is used instead of a pseudoresistor.

This amplifier (CCFEA-II) is designed with a target noise of 1μV-RMS value (see Figure 3.39). The pseudo-resistor is replaced with the MDCR. This amplifier also uses a pre-charge logic similar to the one presented in [8] for boosting the input impedance at DC (in case the chopping frequency is needed to be very high – which is application specific). In this technique, a buffer is employed in an auxiliary path. The buffer needs to have a very high input impedance and be only active for a brief period of time just before the chopping changes the polarity. It will

thus provide charging and discharging current for C_{in}, that would otherwise be supplied by input source [8]. This eventually increases the input impedance.

The main amplifier used in [8] is a current-reuse differential amplifier. Such amplifier has reduced input common-mode range, and also allow a smaller output swing. Furthermore, implementing cascoding of devices for improved common-mode rejection needs a large input supply, so a 1V supply would not be sufficient. This is the reason why the main amplifier, A_{v1} used in this research is a fully-differential folded cascode amplifier, for achieving a larger ICMR (input common-mode range) and a high CMRR. Hence, any special common-mode rejection ratio improvement scheme is not required. Also, an improved frequency response rail-to-rail output common-mode feedback was used in A_{v1}.

The amplifier consumed total current of 1.8µA from the 1V supply. The measured noise for the signal, integrated in a 0.5 to 50Hz frequency band, when all loops are enabled was 1.057µV-rms (see Figure 3.42). When the RRL is disabled, this noise falls down to 0.8246µV-rms (see Figure 3.43), which is similar to the value from the simulation using Cadence spectre RF simulator.

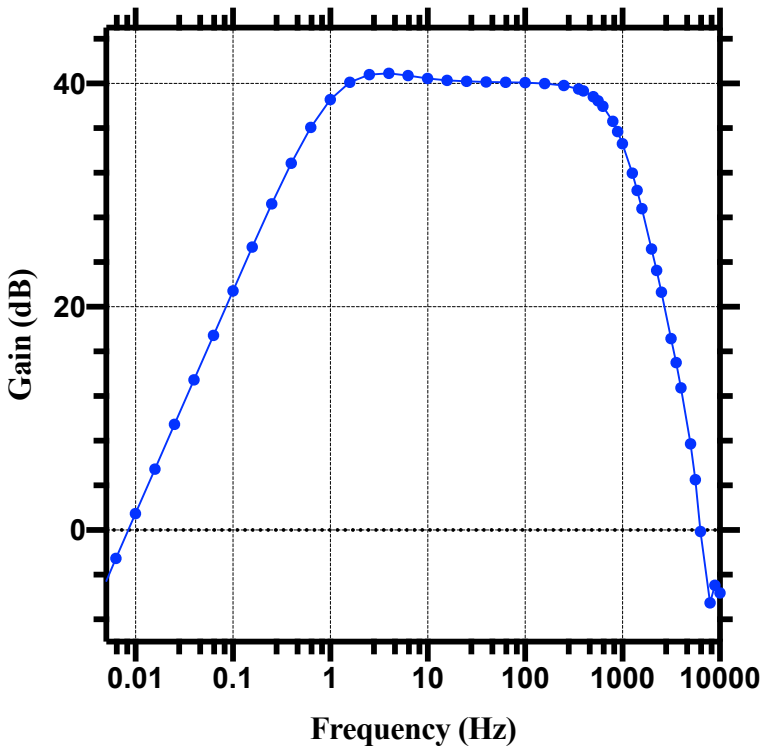


Figure 3.40 Measured gain transfer function of the CCFEA-II, when all feedback loops are active.

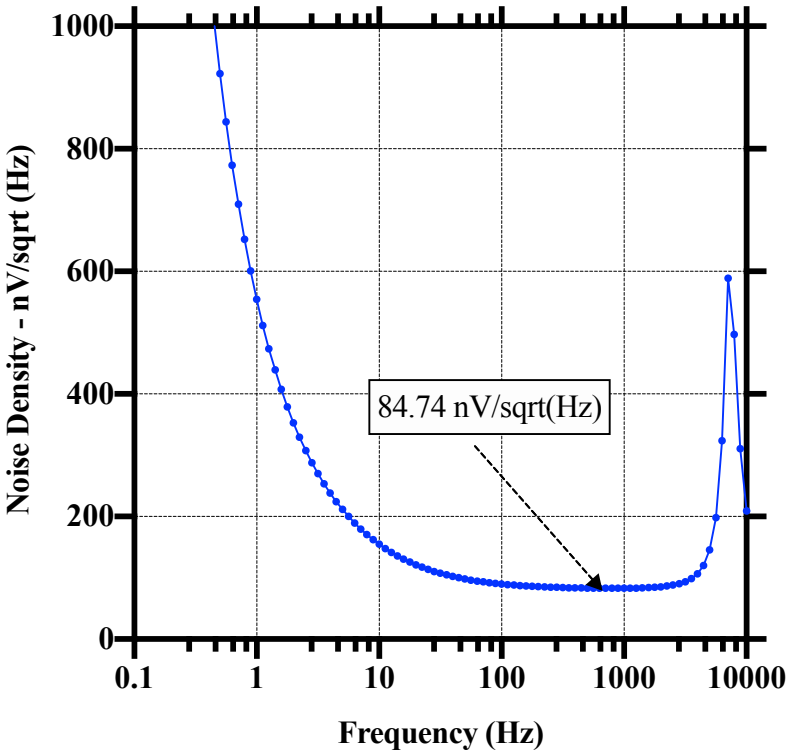


Figure 3.41 Simulated input referred noise voltage of CCFEA-II, using Cadence's pss/pnoise analysis – DSL and RRL both are active.

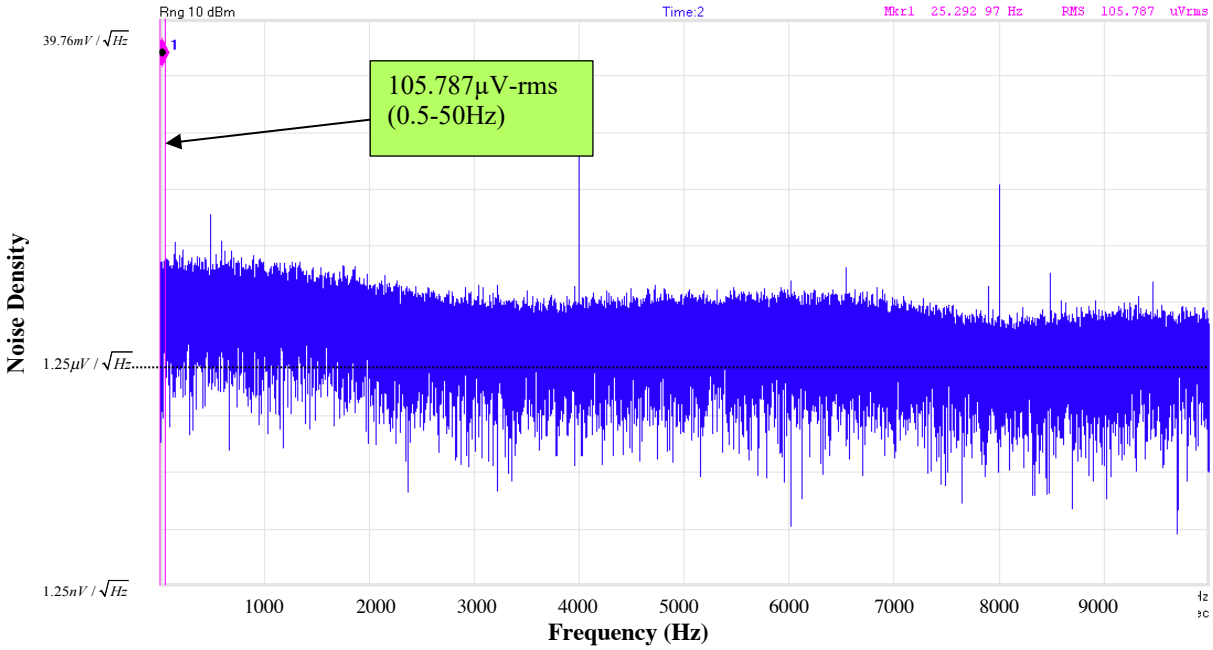


Figure 3.42 Measured output noise for the CCFEA-II when all loops are active, and ibias=50n (50Ω impedance is used for the measurement).

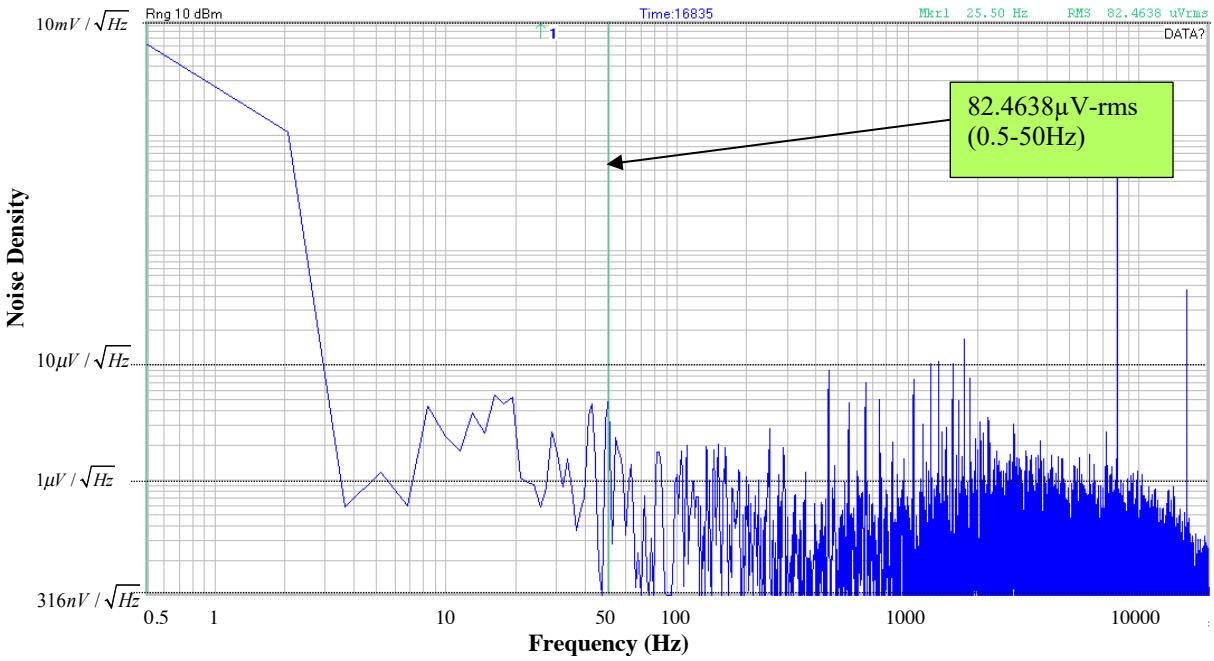


Figure 3.43 Measured output noise for the CCFEA-II when the RRL loop was disabled (50 Ω impedance is used for the measurement).

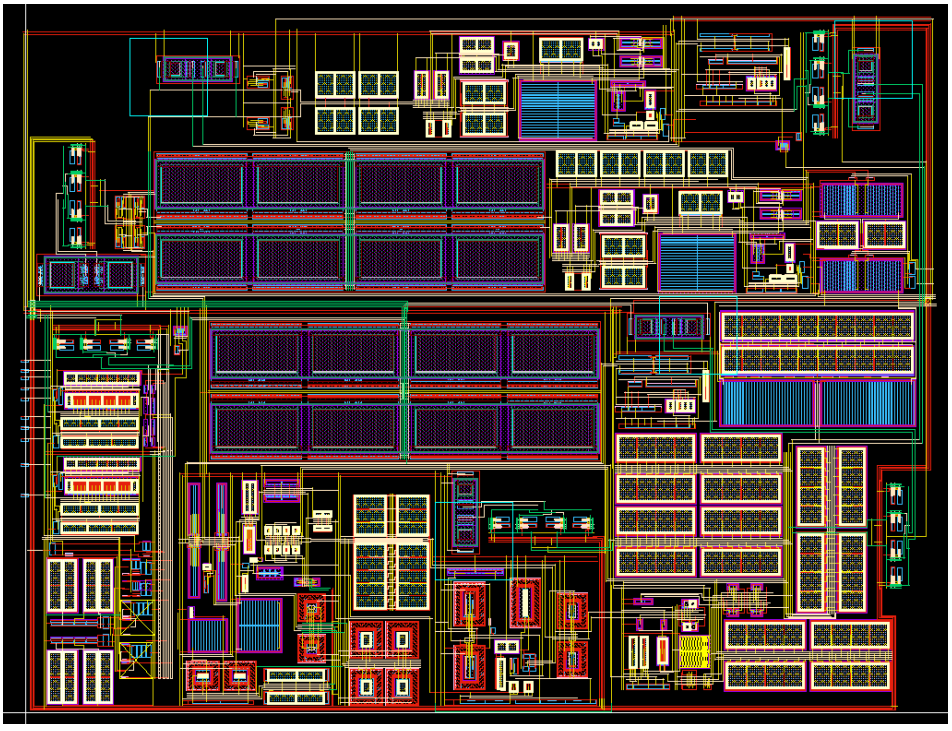


Figure 3.44 Final layout implementation of the CCFEA-II.

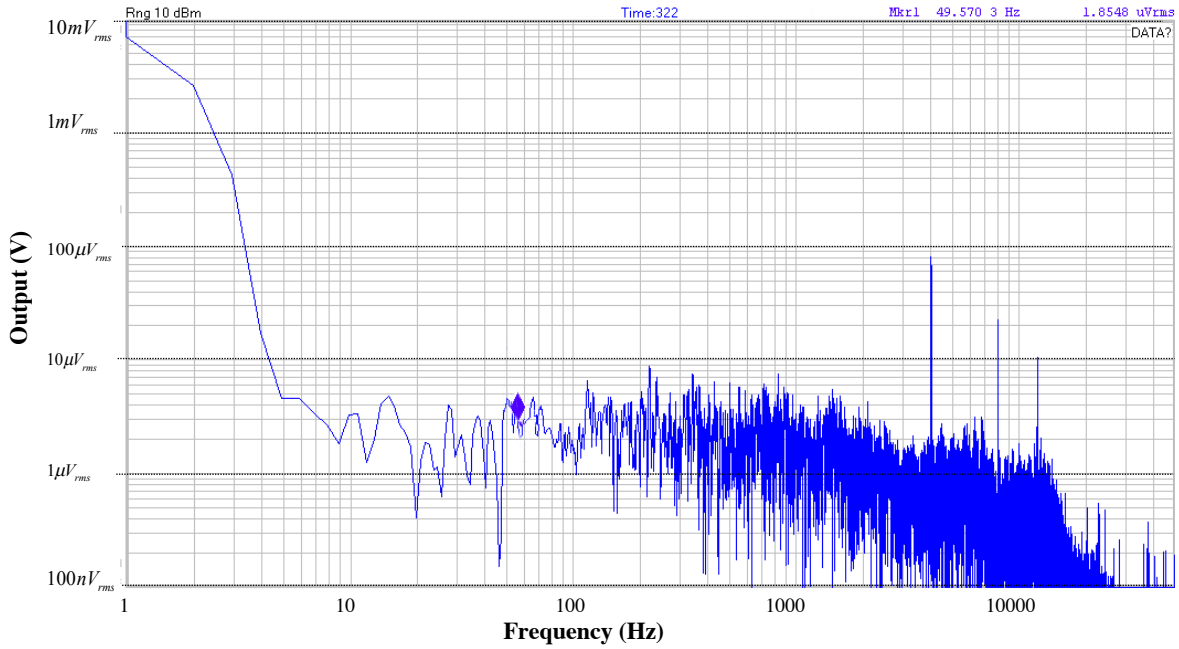


Figure 3.45 Measured differential output gain with a 200mVp-p common-mode sine wave signal. Common mode gain is -91.6dB, and with a differential gain of 40db, CMRR= -131.62dB (50Ω impedance is used for the measurement).

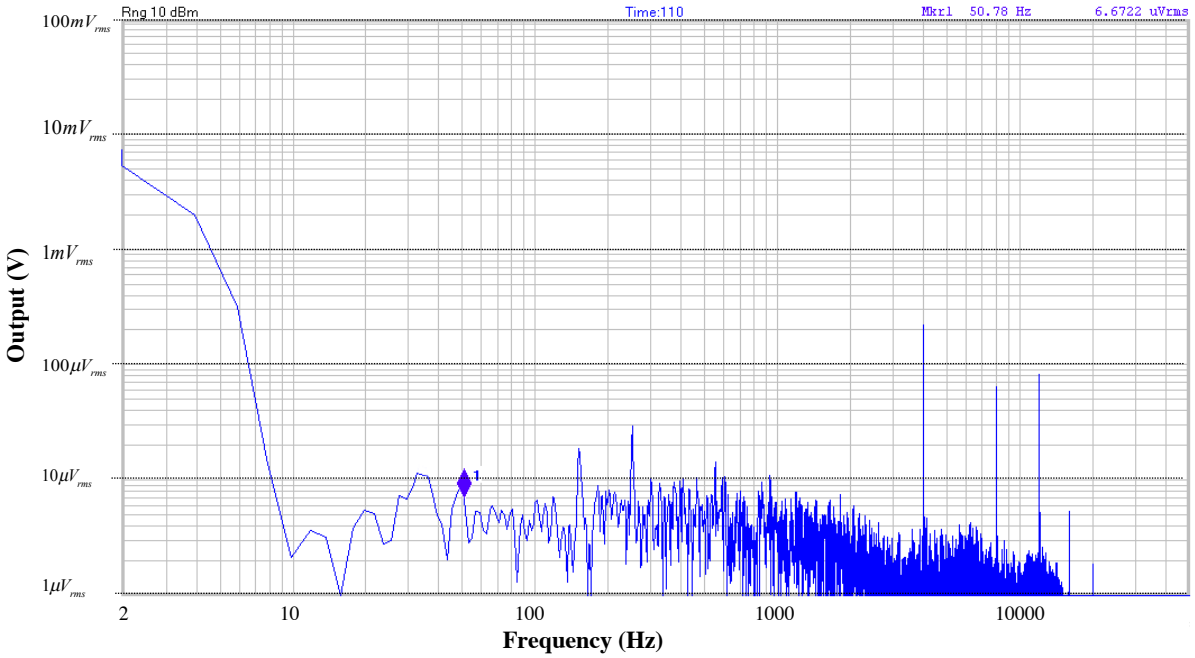


Figure 3.46 Measured differential output gain with a power supply noise of 200mVp-p sine wave. Power supply gain is -80.5dB, and with a differential gain of 40db, PSRR= -120.5dB.

The layout implementation of the amplifier is presented in Figure 3.44. Similar guidelines were followed for matching, as explained in section 3.7 on CCFEA-I. Special care was taken to avoid unnecessary parasitic to the resistor used in the MDCR. Also, the two clock lines were

shielded and kept separate from sensitive signals, and also from each other. Since, currents involved are very low, minimum width wires were used all over. That also aid in reducing any coupling capacitors.

Interference from a 50Hz AC, referred to as AC hum or pickup could cause severe artefacts in an EEG recording system. The cause of this interference is the AC line voltage (50Hz for UK/Europe and 60Hz for the US), which is always present in any clinical settings [41]. This is the reason why a stimulus is provided at 50Hz to test the amplifier's robustness to these main lines interference.

A sine wave of 200mVp-p (at 50Hz frequency) is supplied at the input of the amplifier as common mode disturbance. As evident from Figure 3.45, the differential output showed no effect, as the signal at the output is almost at the noise floor of the amplifier, and the CMRR achieved by the amplifier is -131.62dB.

For testing power supply noise immunity, another sine wave of 200mVp-p amplitude (at 50Hz frequency was supplied to the power pin to check its impact on the differential output. For a large PSRR, the effect should be minimal. From the measured output signal spectrum in Figure 3.46, it can be seen that the impact of power supply noise is minimal, with amplifier achieving a PSRR of -120.5dB.

3.9 Proposed calibration loop for setting an accurate value of a pseudo-resistor

A calibration loop was proposed to tune the value of the pseudo-resistor element (see Figure 3.47). The small signal resistance of a single diode-connected MOS transistor (at $Vds = 0$) can be given as [42-44]:

$$r_{pr}\Big|_{Vds=0} = \left|\frac{1}{\frac{\delta I_D}{\delta V_{DS}}}\right| = \frac{U_T}{I_{D0}} \qquad ...(3.27)$$

where U_T is the thermodynamic voltage, V_{DS} is the drain-source voltage and I_{D0} is the residual charge current given by [14]:

$$I_{D0} = I_{spec} e^{-\frac{V_{T0}}{nU_T}} = 2n\beta U_T{}^2 e^{-\frac{V_{T0}}{nU_T}},\ \beta = \mu C_{ox} \frac{W}{L} \quad \ldots(3.28)$$

From the equation 3.28, it is evident that the small signal resistance of a pseudo-resistor is highly dependent on process, temperature and geometry [42],[44].

To compensate for some of the process and mismatch variations, a calibrated pseudo-resistor is proposed in Figure 3.48(*a*). A negative feedback calibration loop is utilized to compare the dummy pseudo-resistor, Rps with a poly resistor of value 5MΩ. This poly resistor has the same variation as the one in the bandgap reference of the chip, so any variation in the voltage can effectively be cancelled out.

The current across Rps, Rpsx can be given as (see Figure 3.47) [44]:

$$I_{R=} I_0 . e^{\frac{V_o - V_B}{n_p U_T}} . e^{-\frac{\Delta V}{2n_p U_T}} . \left(1 - e^{\frac{\Delta V}{2U_T}} . \frac{\cosh \frac{\Delta V}{2n_p U_T}}{\cosh \frac{\Delta V}{2n_p U_T (n_p - 1)}} \right) \quad \ldots(3.29)$$

A size ratio of *N/M* is used between Rps and Rpsx, to account for the drain-source voltage difference between these two resistors. This ratio needs to be carefully chosen to give more accurate matching of resistors. The negative feedback (Figure 3.48 (a)) tracks the two voltages *vx*, *vy*; and uses the feedback to force the two to be same. By virtue of the current division, the 50*G*Ω pseudoresistor is compared with a 5*M*Ω high accuracy poly resistor. Several pseudo-resistors similar to Rpsx can be connected in series, to get a resistance value, which will be multiple of 50*G*Ω, this will also reduce the distortion by reducing the voltage drop across the pseudo-resistor element.

The resistor variation simulation gives three sigma value of 8.25% (see Figure 3.49(*a*)). When this pseudo-resistor is employed in the CCFEA-III (see Figure 3.50), the high pass frequency corner variation achieved is just under 28%, including variation in the capacitive loading from the amplifier, and also in the current division (Figure 3.49 (*b*)).

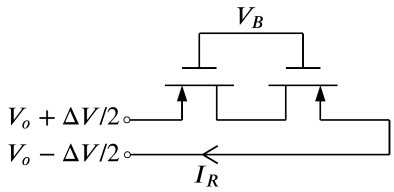
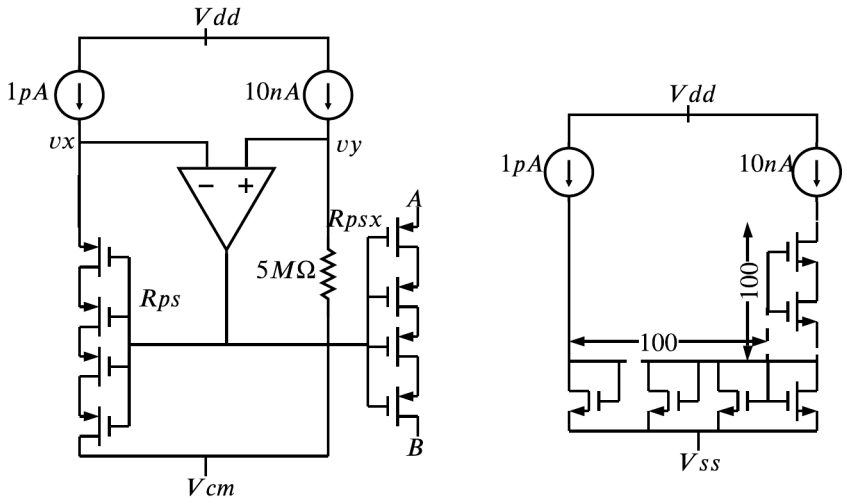
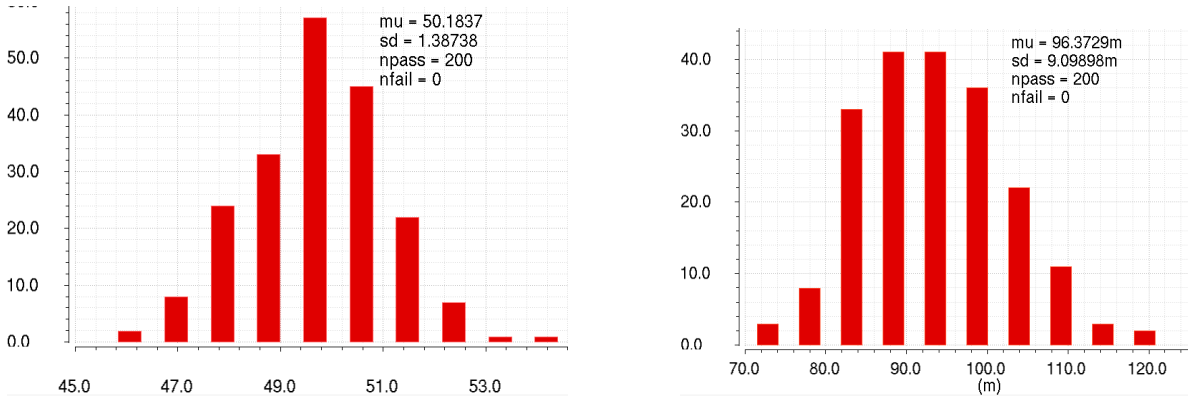


Figure 3.47 Basic tunable pseudoresistor element [44].



(a) *(b)*

Figure 3.48 (a) Negative feedback calibration loop, (b) series-parallel current division.



(a) *(b)*

Figure 3.49 (a) Simulated Monte-Carlo variation for the pseudo-resistor value (N=200), (b) Simulated Monte-Carlo variation in the high-pass cut-off frequency for capacitive coupled amplifier CCFEA-III.

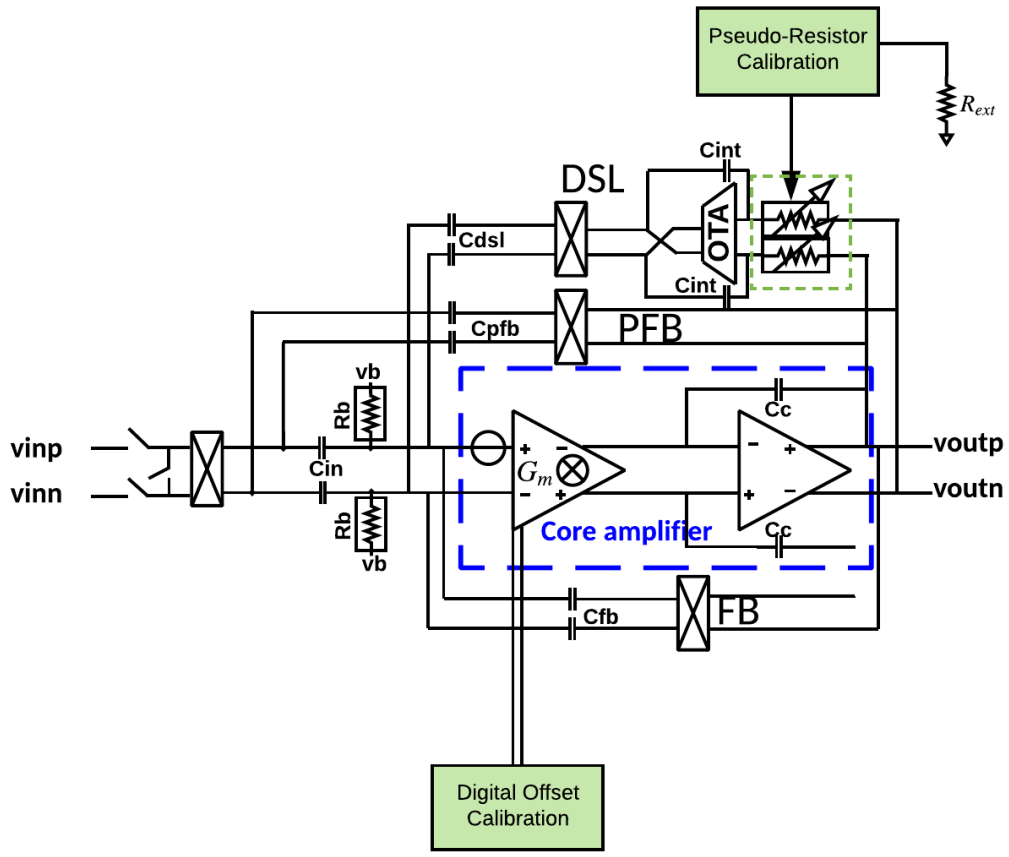


Figure 3.50 Chopped capacitive feedback EEG amplifier (CCFEA-III) with pseudo-resistor calibration loop and digital offset correction.

Chopped capacitive feedback EEG amplifier is also proposed employing the pseudo-resistor calibration scheme, in the Figure 3.50. For cancelling the DC offset of A_{VI} amplifier, a DC offset calibration scheme similar to [39] was used, which will help in reducing the chopping ripple. In practical terms this calibration can be performed for every die, during the testing, and the calibration code can be stored in a non-volatile memory, if continuous calibration is not required; although such calibration does not take many digital gates, and the process can be performed periodically to avoid the drift in the pseudo-resistor value. Only a counter, and a comparator along with few basic gates were used to perform the pseudo-resistor calibration. The most important thing is the accuracy of the calibration resistor.

To compare the three proposed EEG amplifiers in this research with state-of-art designs, noise efficiency factor (NEF) is being used given by [51]:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi U_T 4kTBW}} \qquad \ldots(3.30)$$

where, $V_{ni,rms}$ is the input referred rms noise, I_{tot} is the total supply current, U_T is the thermodynamic voltage and BW is the bandwidth of the amplifier. To include the supply, V_{DD}, another criteria power efficiency factor (PEF) is defined as [51]:

$$PEF = NEF^2.VDD \quad \ldots(3.31)$$

3.10 Conclusion

This chapter reviewed the state-of-art neural amplifier implementations and compared required design specifications with these. A detailed discussion was presented on the reasoning behind choosing capacitively coupled amplifier topology for this research. The chapter further reviewed the noise sources in the basic amplifier topology, and the methods to reduce the noise from a fully differential folded cascode amplifier design. An improved frequency response common-mode feedback circuit is then proposed, along with a brief discussion on the chopping technique used. The chapter then goes on to propose a capacitive feedback EEG amplifier using the novel pseudoresistors introduced in chapter 4. Another amplifier topology was presented using a multi-rate duty-cycle resistor. Finally, a novel calibration scheme was proposed to set the value of pseudoresistors accurately, that could reduce the variation in the resistor value from 1000%-2000% to just 8.25%. The summary of the performance comparison with the implemented amplifiers is given in Table 3.1.

Table 3.1 Performance comparison of proposed EEG amplifiers with state of art designs.

	[45]	[46]	[47]	[48]	[49]	[50]	CCFEA-I	CCFEA-II	CCFEA-III
Supply Voltage	1	1	0.8	1.8	1.2	1.2	1	1	1
Topology	Single Ended	Fully-differential	Fully-differential	Fully-differential	Fully-differential	Fully-differential	Fully-differential	Fully-differential	Fully-differential
Power (µW)	3.28	3.05	4	3.26	3.48	9.24	2	2.65	1.8
Gain (dB)	52.1	40	56	49.1/59.4/67.9	-	58	40	40	40
BW (Hz)	1-8.2k	10.9	0.6-130	117	5k	0.5-500	0.1-500	0.1-500	0.1-500
Vni,rms (µVrms)	4.13	3.32	1.8	2.02	-	1.3	0.575	0.8246	0.45
NEF	3.19	3.02	13.7	3.36	3.9	6.33	2.86	4.48	3.31
PEF	10.2	9.12	187.7	20.32	18.25	48.08	8.15	20.07	10.95
CMRR (dB)	90	>60	-	67.1	85	100	>100	131.62	125.015
PSRR (dB)	78	-	-	69.6	-	-	>100	120.5	114.78
Process	65nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	130nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS

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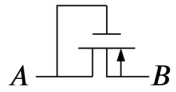
Chapter 4 - Pseudo-Resistor Design

4.1 Introduction

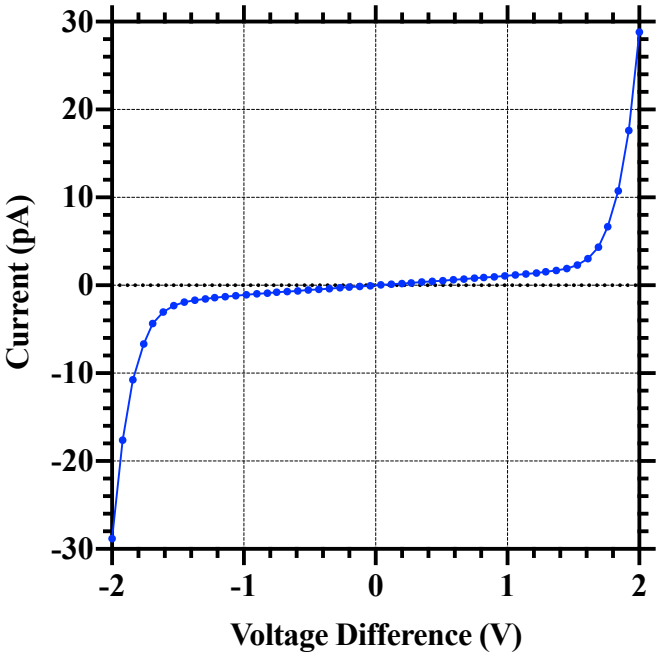
High-value resistors are very common in biomedical signal processing. The resistor value needed for biosignal acquisition systems could be in the range of several GΩ. Such high-value resistors are known to be extremely difficult to design in CMOS technology; also, the area consumed by such resistors would make it extremely difficult to implement a full system-on-chip. Furthermore, the parasitics contributed by such huge sized resistors can adversely affect the frequency performance [1-2]. Another issue is that the density rules may limit a resistor's size that can be implemented on-chip, hence the maximum achievable value.

All these drawbacks associated with a high-value resistor fabrication led to a lot of research in finding alternative solutions. These researches are based on designing alternative circuits that emulate the voltage-current characteristics of a very high-value resistor. These circuits are called pseudo-resistors as they replace traditional resistors for a specific circuit function. In this research, only pseudo-resistors used in the context of a biosignal acquisition will be referenced.

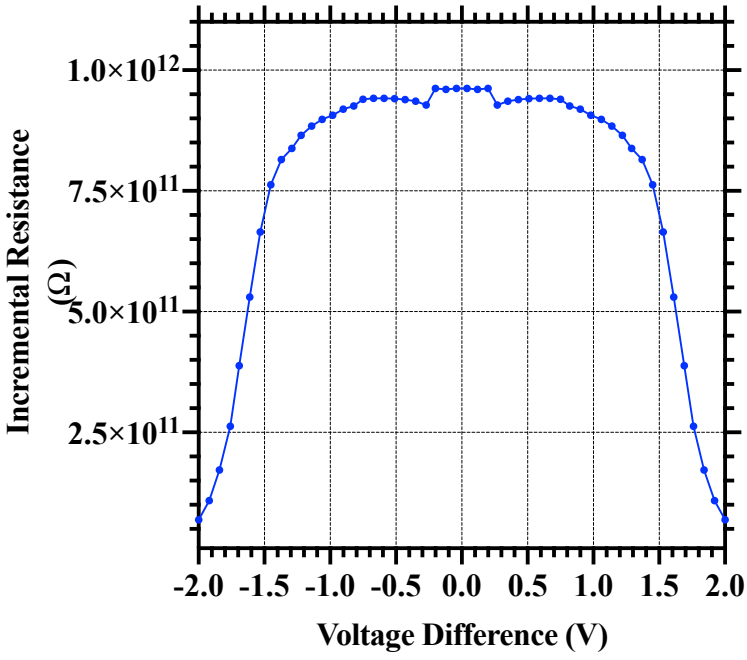
Pseudo-resistors are used in a lot of fully integrated high time constant circuits as they outperform every available solution of implementing a high-value resistor in terms of area and power efficiency. The concept of a MOS-bipolar element as a pseudo-resistor was first introduced in [1], but it was Reid [3] who used this bipolar MOS in the context of a neural amplifier for the first time [3-4] (as shown in Figure 4.1(*a*)). When a negative voltage is applied across the gate and the source (V_{GS}) of this MOS transistor, it acts as a normal diode-connected PMOS device. On the application of a positive V_{GS}, the parasitic source-well-drain PNP bipolar transistor is activated, and the device behaves as a diode-connected bipolar [3-4] (see Figure 4.1 (b)). On the application of a small voltage across this device, it exhibits an extremely high incremental resistance. For $|\Delta V|$ < 0.2V, [4] reported dV/dI> $10^{10}\Omega$. Such pseudoresistor can be used with a small on-chip capacitor for creating a very large time constant filter. And when a large voltage is applied across the MOS-bipolar element, it reduces the incremental resistance allowing a faster settling time (see Figure 4.1 (c)).



(a)



(b)



(c)

***Figure 4.1** (a) MOS_bipolar element (b) Simulated Current-Voltage characteristics of MOS-bipolar element [3] (c) Simulated incremental resistance of a single MOS-bipolar element. For a low voltage difference, this incremental resistance can be very high [3].*

A significant problem with this pseudoresistor implementation is that the resistance drops drastically when the voltage difference across the resistor moves away from zero, inducing signal-dependent distortion while limiting the voltage dynamic-range.

To understand the limitations of the pseudo-resistor, it is necessary to model the resistance of the MOS transistor. The equivalent resistance of this MOS pseudo-resistor can be modelled by using subthreshold current equation for the transistor [2] :

$$I_{SD} = I_{SD0}.\exp\left(\frac{V_{SG}}{nV_{TH}}\right).\left[1-\exp\left(\frac{V_{SD}}{V_{TH}}\right)\right] \quad ...(4.1)$$

where, I_{SD} is the current across the drain-source, V_{SG} is the source gate voltage, V_{SD} is the source gate voltage, V_{TH} is the thermal voltage (kT/q), n is the sub-threshold slope, and I_{SD0} can be given as [2]:

$$I_{SD0} = 2n\mu C'_{ox}\left(\frac{W}{L}\right)V_{TH}^2.\exp\left(-\frac{|V_T|}{nV_{TH}}\right) \quad \ldots(4.2)$$

where, μ is the mobility of carriers, W/L is the aspect ratio of the transistor, C'_{ox} is the gate-oxide capacitance per unit area and V_T is the threshold voltage of the transistor. Finally, the equivalent resistance, R_{eq}, for the MOS pseudo-resistor element for a very small incremental voltage can be given as [2]:

$$R_{eq}\Big|_{V_{AB}\approx 0} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\Big|_{V_{SD},V_{SG}=0}\right)^{-1} \quad \ldots(4.3)$$

$$= \frac{V_{TH}}{I_{SD0}} \quad \ldots(4.4)$$

4.2 State-of-art implementations and novel pseudoresistors

The first pseudoresistor element considered in this research was a symmetric resistor and comprised of two transistors (Mp1 and Mp2), whose parasitic source-bulk diodes are connected

in an anti-parallel arrangement [5] (see Figure 4.2(*a*)). If the voltage difference across the arrangement is kept small enough, then none of the diodes will conduct strongly, and the incremental resistance would be considerably large (several GΩ). The leakage of the pseudoresistor can further be reduced using a compensation current generated by a dummy NMOS transistor as proposed in [6]. However, it would require a deep n-well NMOS that will add to the area, cost, and not suitable for the traditional CMOS technology. From Figure 4.2 (*b*), it is evident that the resistance value is high for small signals and low for large signals. Hence, the response will be slow for small signals and fast for large signals. This signal-dependent variation in the resistance value can lead to distortion in the signal path, which is a significant issue solved by two new pseudo-resistors proposed later in the thesis. The implementation used in [3-4] is presented in Figure 4.3 (*a*), where source-bulk parasitic diodes are connected in parallel. This topology has two main issues: signal-dependent distortion and asymmetry in characteristics.

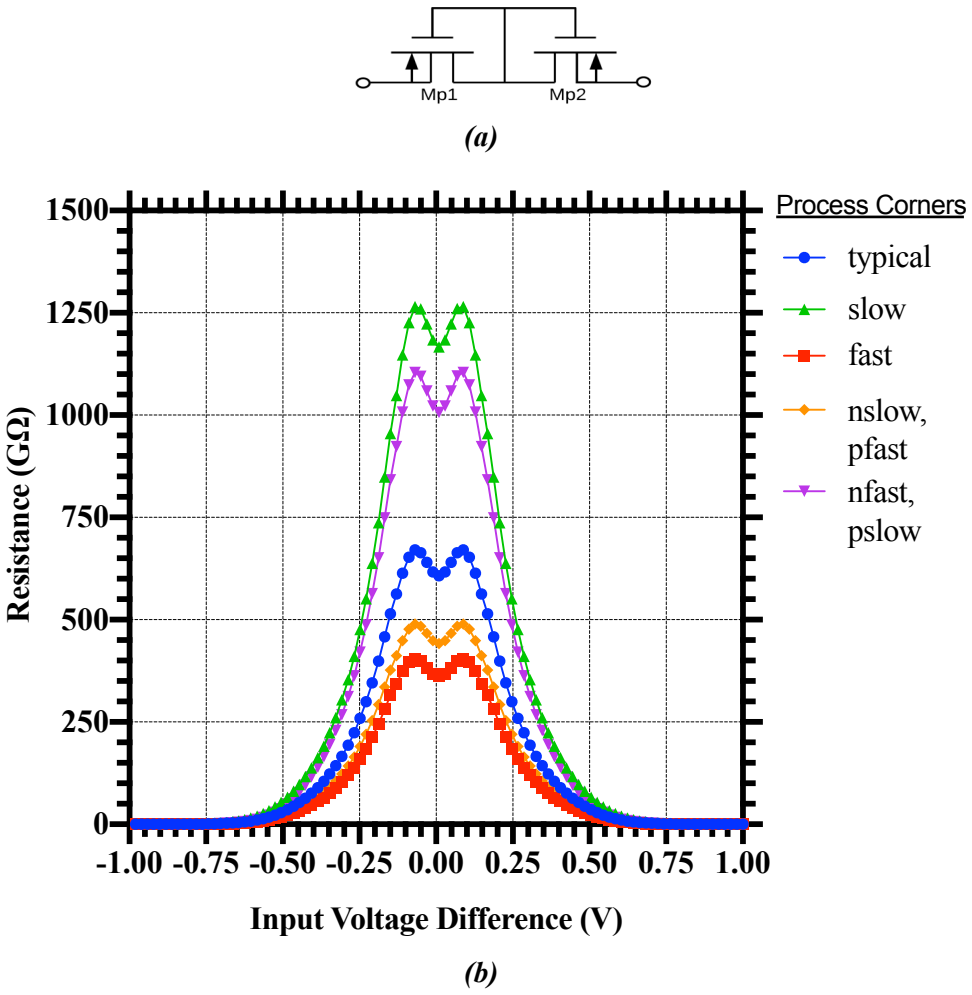


Figure 4.2 (a) Pseudoresistor type 1(PS1) [5], (b) Simulated cross-corner resistance variation for PS1.

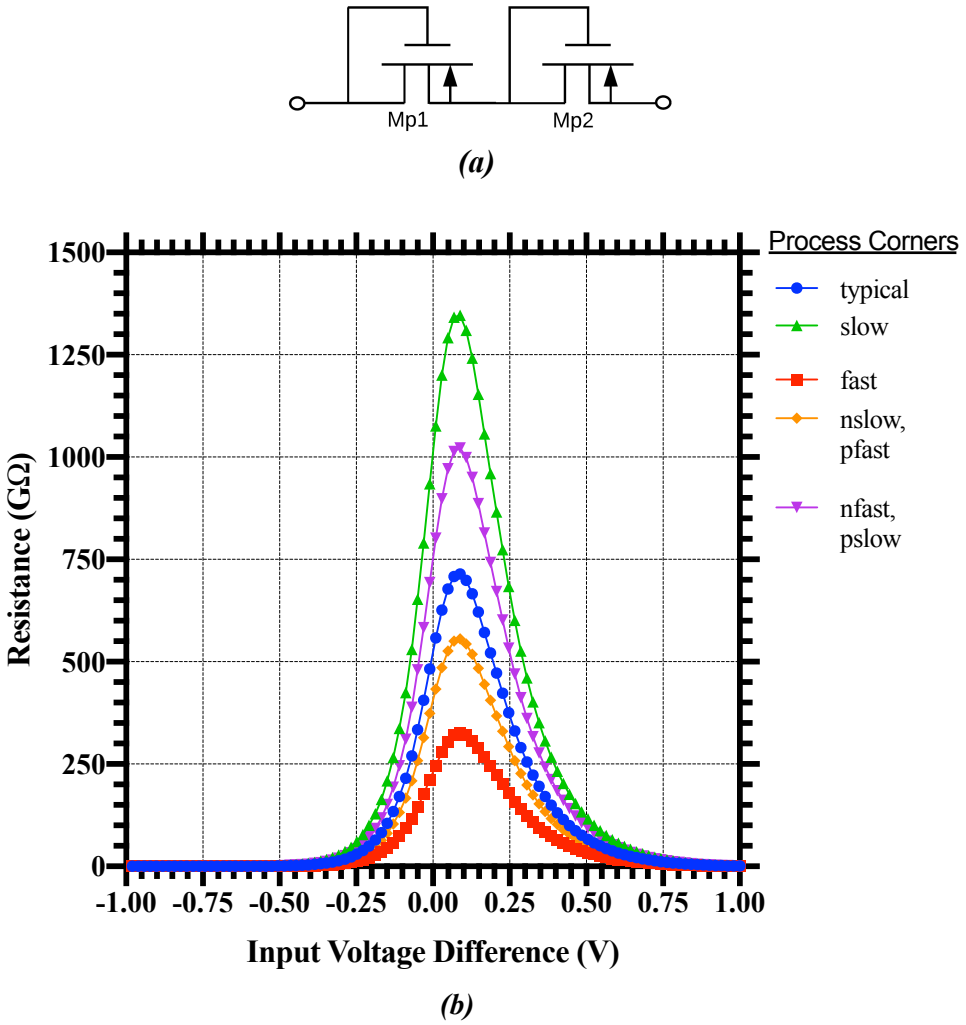
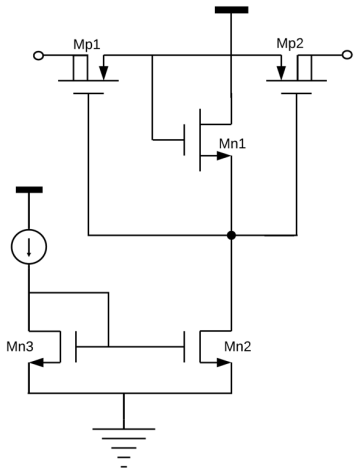


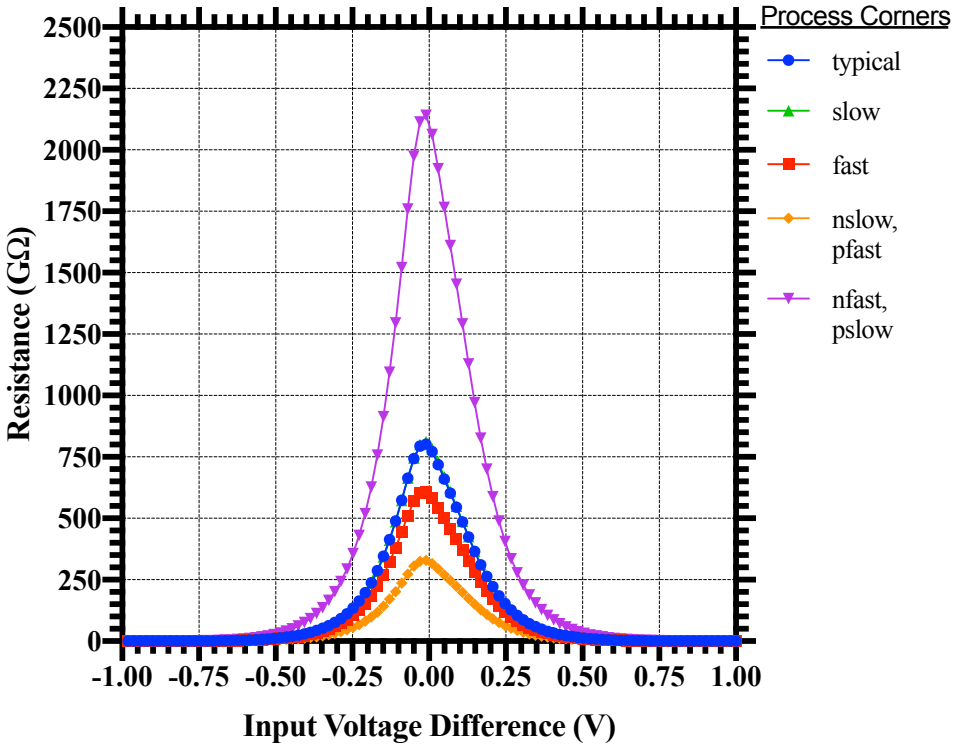
Figure 4.3 (a) Pseudoresistor type 2 (PS2) [3-4], (b) Simulated cross-corner resistance variation for PS2.

A diode-connected MOS operates in a weak inversion region for achieving high resistance values, and due to exponential *I/V* characteristics in the weak inversion, it exhibits poor linearity and a strong dependence on process and voltage variations. To alleviate some of this process dependence, a tunable pseudoresistor was published in [7] (see Figure 4.4 (*a*)), where the bulk of the device was connected to the drain, which caused modification of threshold on the application of a source-drain voltage (V_{SD}). It has been shown that by restricting the source-gate voltage (V_{SG}) to be very low (on the order of thermal voltage U_T), a very high-value resistor can be obtained while keeping the device size to be very small [7]. Two identical PMOS devices were used to obtain a symmetric resistance with respect to the polarity of the voltage applied across the terminals. Another NMOS is used to bias the source-gate of these devices. This circuit can be used to generate a tunable resistor with the value between 100kΩ and 1GΩ. Further

modifications are done to this scheme by [8] to make it more robust to process variations, and achieving a resistance between 500MΩ to 70GΩ, but the extra modification came at the expense of extra 2µW of power and a feedback path which adds additional pole into the system.

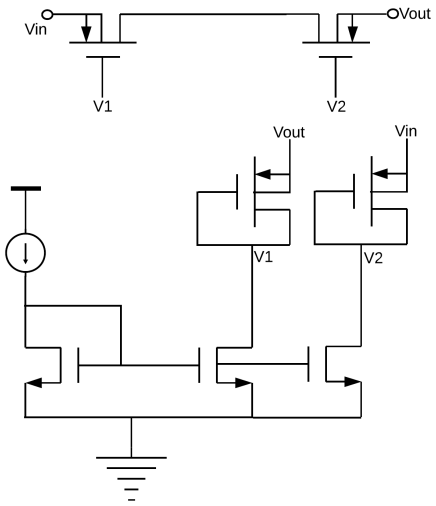


(a)

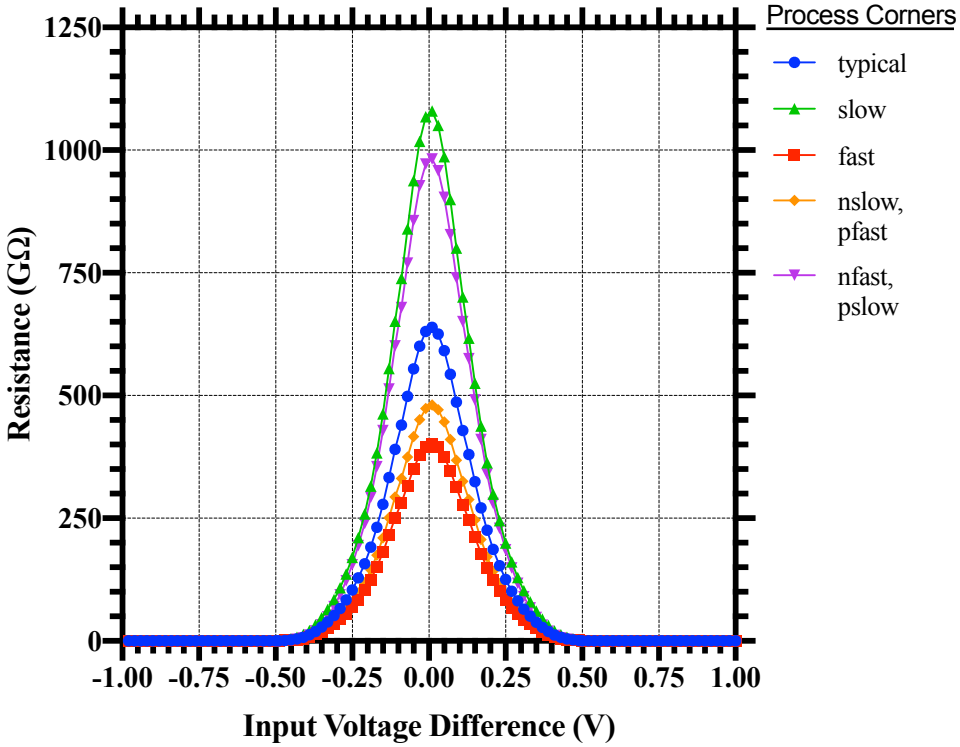


(b)

Figure 4.4 (a) Pseudoresistor type 3 (PS3) [7], (b) Simulated cross-corner resistance variation for PS3.



(a)



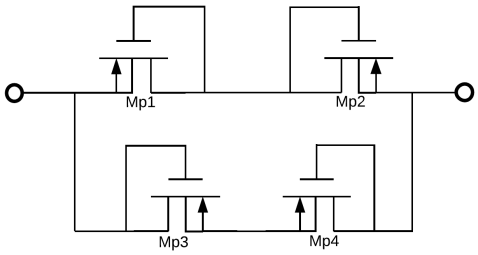
(b)

Figure 4.5 (a) Pseudoresistor type 4 (PS4) [9], (b) Simulated cross-corner resistance variation for PS4.

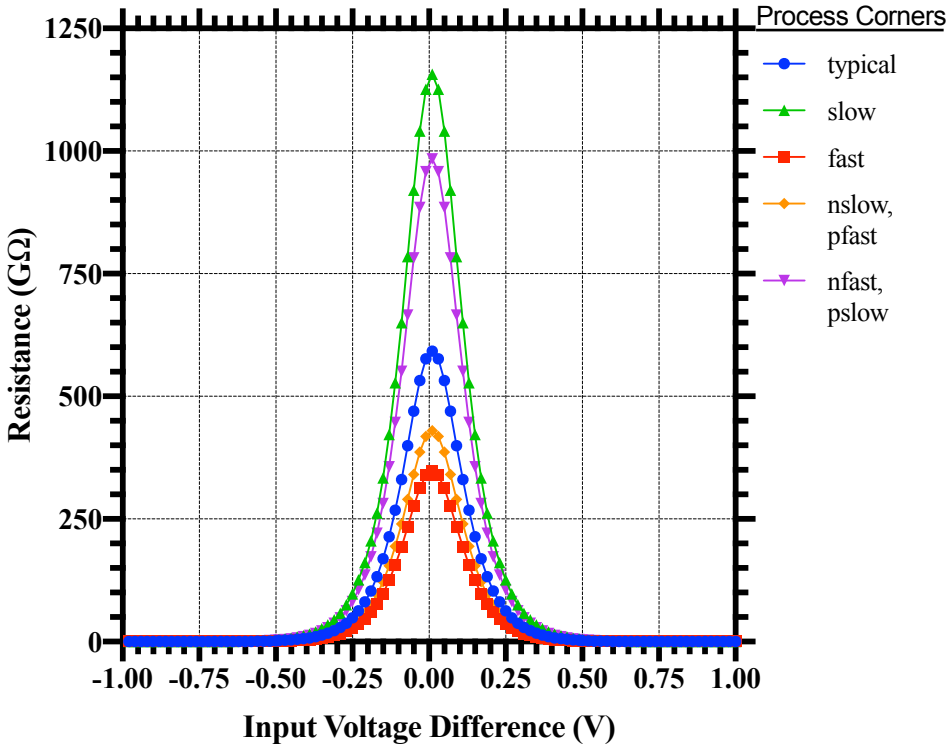
To reduce the asymmetry and non-linearity in the resistor value, [9] proposed a balanced pseudoresistor (see Figure 4.5 (*a*)). Asymmetry in the resistance value can cause unavoidable signal-dependent output shift and also the clipping of the output to one of the power rails as the

input signal level increases. It is one of the critical factors causing the reduction in the dynamic range of low-voltage circuits. Two PMOS transistors were used in this approach where each transistor was on for half of the input cycle. Also, to tune the resistance, 3-bit digitally controlled current sources were used. This circuit was designed to operate for a low voltage difference across the pseudoresistor.

Another pseudoresistor was proposed in this research, which is a combination of pseudoresistors presented in [4] and [10] (see Figure 4.6 (*a*)). Results are presented in Figure 4.6 (*b*).

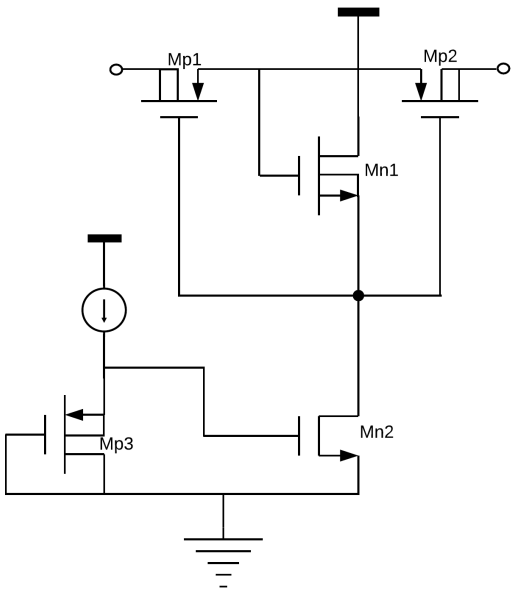


(a)

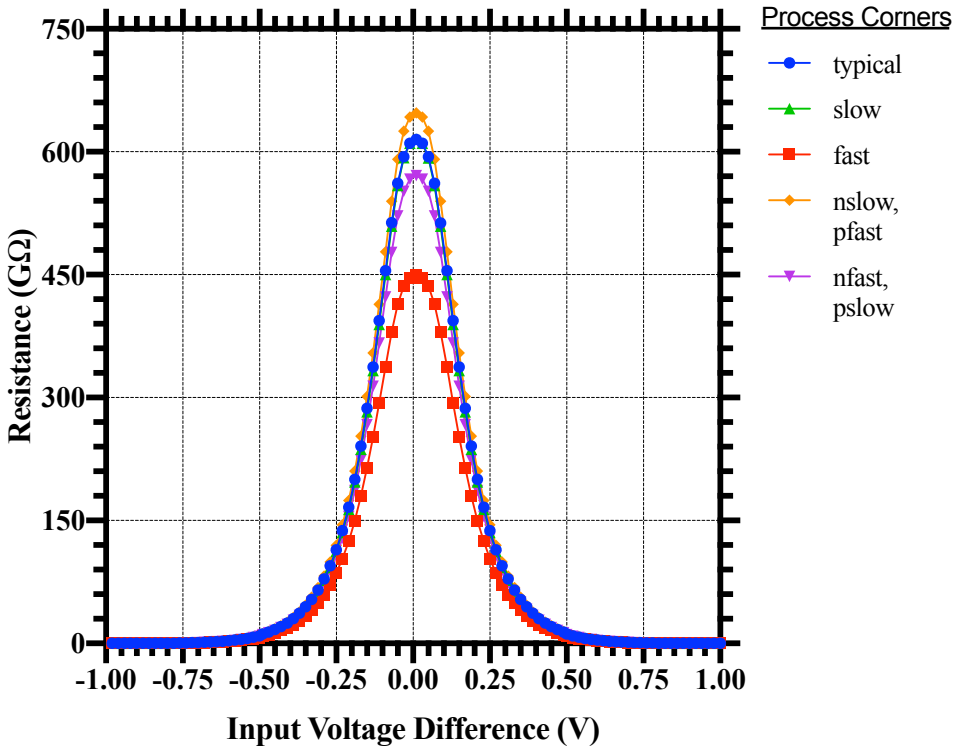


(b)

Figure 4.6 (a) Pseudoresistor type 5 (PS5) (based on [4],[10]), (b) Simulated cross-corner resistance variation for PS5.



(a)



(b)

Figure 4.7 (a) Pseudo-resistor type 6 (PS6) [11], (b) Simulated cross-corner resistance variation for PS6.

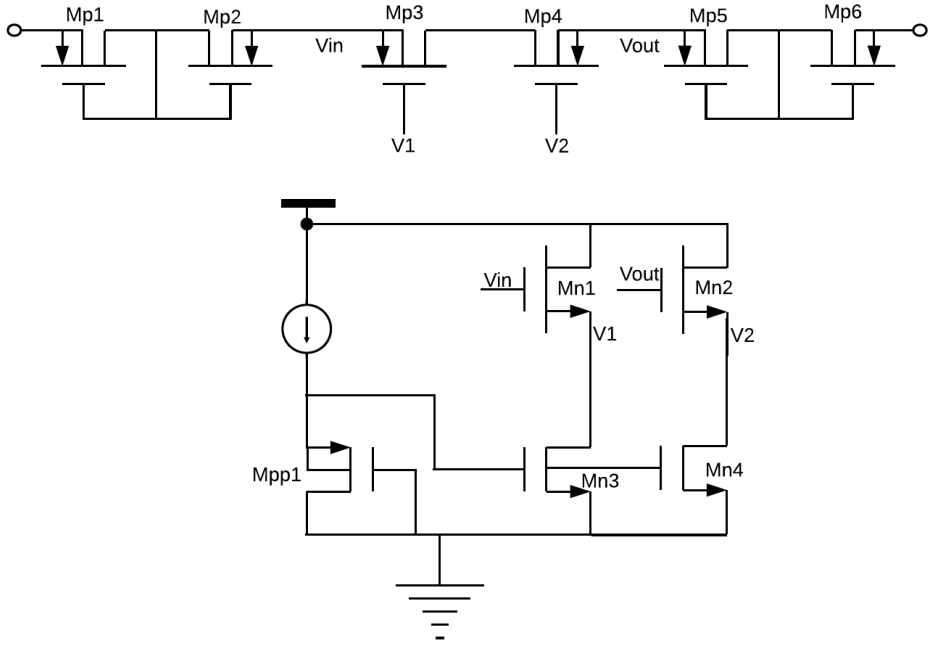
For reducing the PVT variation in the pseudoresistor (PR) value, a PTAT current source was proposed for the biasing in [11]. The design was only suitable for a triple-well technology. It

was an enhancement to the circuit proposed in [7]. For reducing the effect of process variations in the circuit of [7], a new biasing scheme was introduced based on a pseudo current mirror whose devices were to be kept in weak inversion. By doing this, the effect of process variations of the devices in the pseudoresistor can be cancelled by a reciprocal of process dependence in the bias current. This pseudo current mirror consists of the NMOS current source Mn1 biased by the diode-connected PMOS-Mp3 Figure 4.7(*a*)). It results in the bias current, which has a reciprocal dependence on the process variations compared to the pseudoresistor. This modification shall cancel the effect of process variations and the residual fluctuation in the value of the pseudo-resistor, which would depend only on the matching of similar devices (NMOS to NMOS and PMOS to PMOS). However, the parasitic well capacitance of the pseudoresistor element impacted the performance of the circuit. A further modification to the original circuit in [11] is proposed in [12]. In this implementation, the parasitic capacitance of the PR is improved by manufacturing this in a SOI CMOS technology.

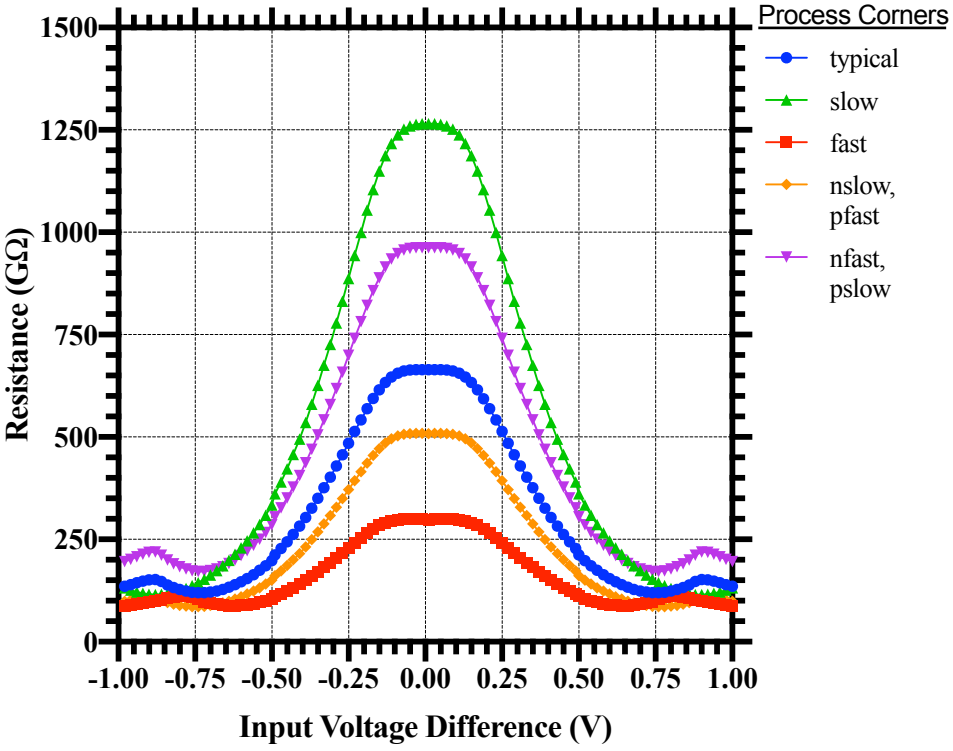
A feedback technique to control the pseudo-resistor value is proposed in [13], though at the expense of additional loading on the signal path, and an additional pole in the system. An improved pseudoresistor is proposed in [14], where a dual-biased technique is used for limiting the current across through the PR. The PR achieved a variation of 54%, though with additional parasitics and noise. [15] proposed using different sized transistors to account for different voltage drops across the PR. A linearization technique is proposed in [16], reducing total harmonic distortion in the system, though achieved resistor value is very low for EEG application. A literature review was also conducted for several more pseudoresistors [17-21] but not considered in the thesis. Their performance was less suitable for EEG implementation than already discussed designs.

From the discussion above, it can be concluded that a pseudoresistor implementation has several error sources, including process variation, frequency response and distortion. Several simulation results were run and reported in this chapter. These results affirm the assumption that no pseudo-resistor presented in the literature was targeting all error sources. This is the reason why two-hybrid pseudoresistors have been proposed in this research ((PS7 – see Figure 4.8(*a*), PS8 – see Figure 4.9(*a*)), that mainly focussed on low distortion, improved frequency performance implementation with a high voltage swing.

From the work of [5], it is clear that more pseudoresistors need to be added in series to reduce the distortion. The distortion shall be low in this case because the voltage drop across individual pseudoresistor is small, and the source-bulk diode does not turn on to impact resistance value.

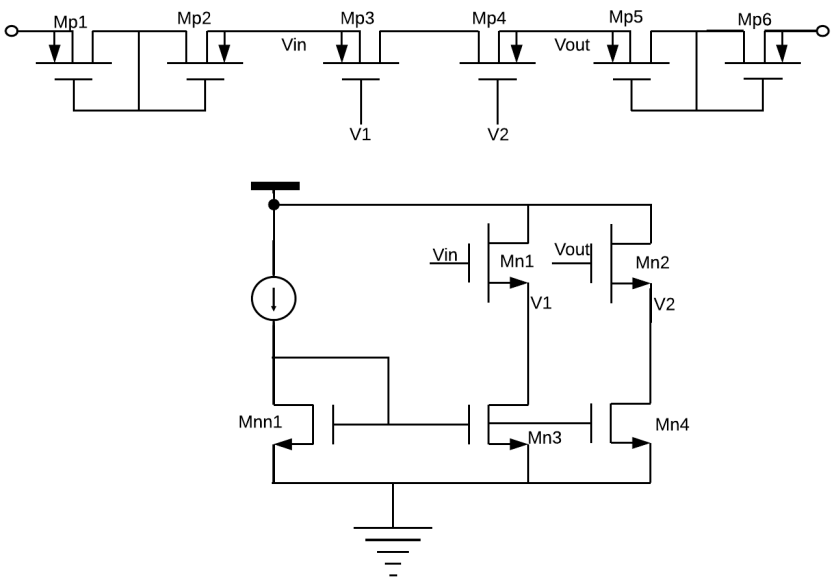


(a)

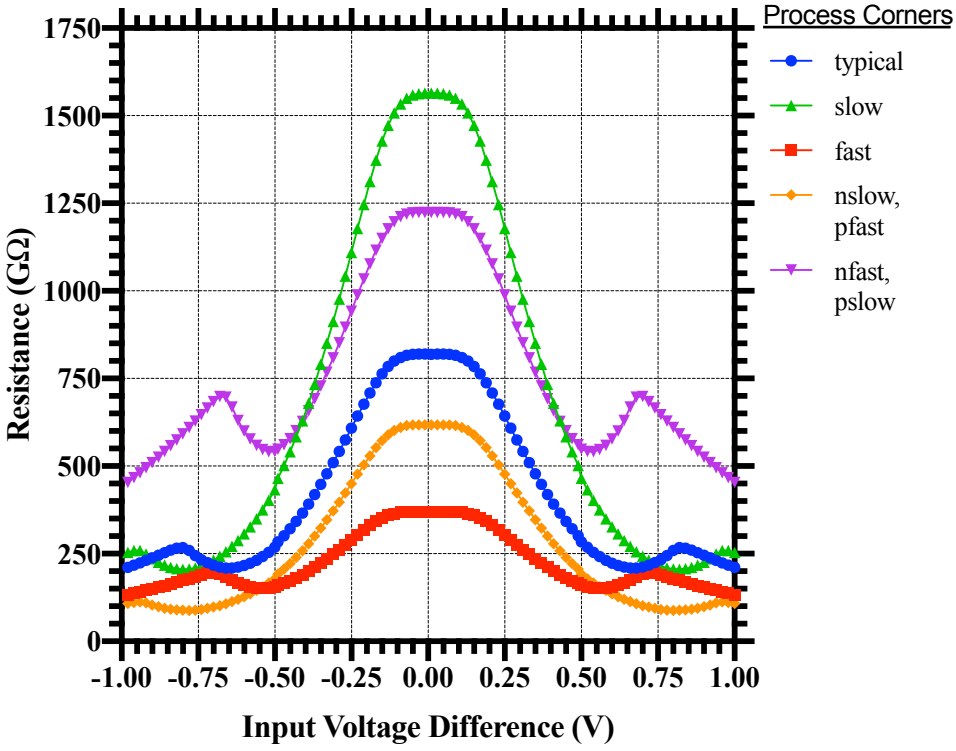


(b)

Figure 4.8 (a) Pseudo resistor type 7 (PS7), (b) Simulated cross-corner resistance variation for PS7.



(a)



(b)

Figure 4.9 (a) Pseudo-resistor type 8 (PS8), (b) Simulated cross-corner resistance variation for PS8.

Adding too many pseudoresistors in series can, however, adversely affect the noise performance, and add a lot of parasitic capacitance, so a trade-off needs to be sought between

the distortion and the noise performance. Two PS1 are used in series, with tunability provided by two MOS transistors, Mp3 and Mp4, biased in a way similar to [22]. PS7 uses a triple-well NMOS for biasing (transistors Mn1 and Mn2), and pseudo-current mirror Mpp1 for biasing the current sources Mn3 and Mn4.

Due to unavailability of low-threshold devices, standard threshold devices, Mn1, and Mn2 source followers are used to bias tunable high threshold transistors Mp3 and Mp4. PS8 is effectively similar to PS7, with few changes, like Mn1 and Mn2 is no longer triple-well NMOS, reducing the well parasitics, and the current mirror is NMOS Mnn1 rather than a pseudo current mirror, improving the inherent matching further.

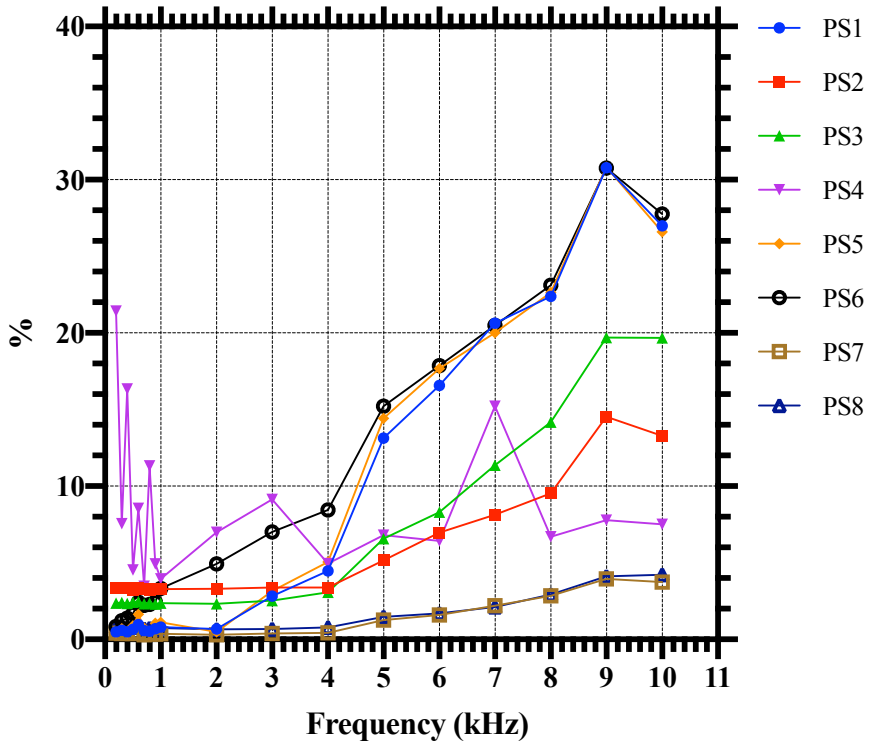


Figure 4.10 Simulated percentage total harmonic distortion (THD) for all topologies (An input signal of amplitude 0.25V is swept through multiple frequencies).

Based on simulation results, both PS7 and PS8 exhibits superior resistance value for a large voltage difference across its terminals. The resistance drops when the voltage difference is higher than 0.25V, but this is acceptable in EEG systems as the voltage levels are usually much lower than 0.25V even after applying a gain of 100 [23-25].

Another important thing is both PS7 and PS8 exhibits superior frequency performance than other implementations. These designs are symmetrical so exhibits lower distortion, as evident

from Figure 4.10. An input signal of amplitude 0.25V is swept through the frequency for calculating the total harmonic distortion. The chopper modulation frequency can be as high as 8kHz, so the sweep was done up to 10kHz. Due to the low amplitude EEG signals, THD calculation is less relevant for the EEG amplifier.

For achieving the resistance tunability, a 2-bit current control is implemented at the top level of the chip to account for the corner variability. A simple calibration scheme can be employed by setting the high pass cut-off frequency, that will keep the resistance within desired limits.

The PR circuits are also compared in terms of total harmonic distortion (THD) as a function of the input frequency. PS8 shows smaller distortion than studied PRs in the literature, and one of the reasons why it has been used in this thesis (see Figure 4.11).

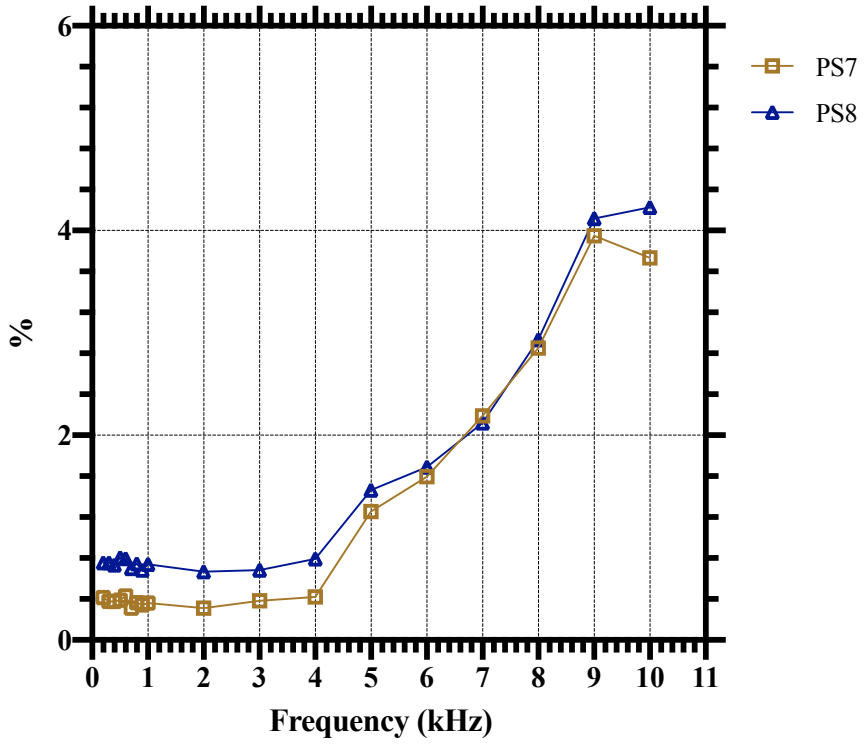


Figure 4.11 Simulated total harmonic distortion for PS7 and PS8.

The ability to provide less parasitic and keeping the resistance frequency independent in the frequency band of interest makes PS8 an attractive solution. A major issue that plagues the pseudoresistor implementation, in general, is the leakage. For smaller geometries, leakage of several *pA* is quite common. This leakage can reduce the value of the resistor, that can be achieved on deep submicron technologies. To avoid some of issues with the leakage, high threshold devices are used throughout.

Small-signal resistances of various pseudoresistor implementations are given in Figure 4.12.

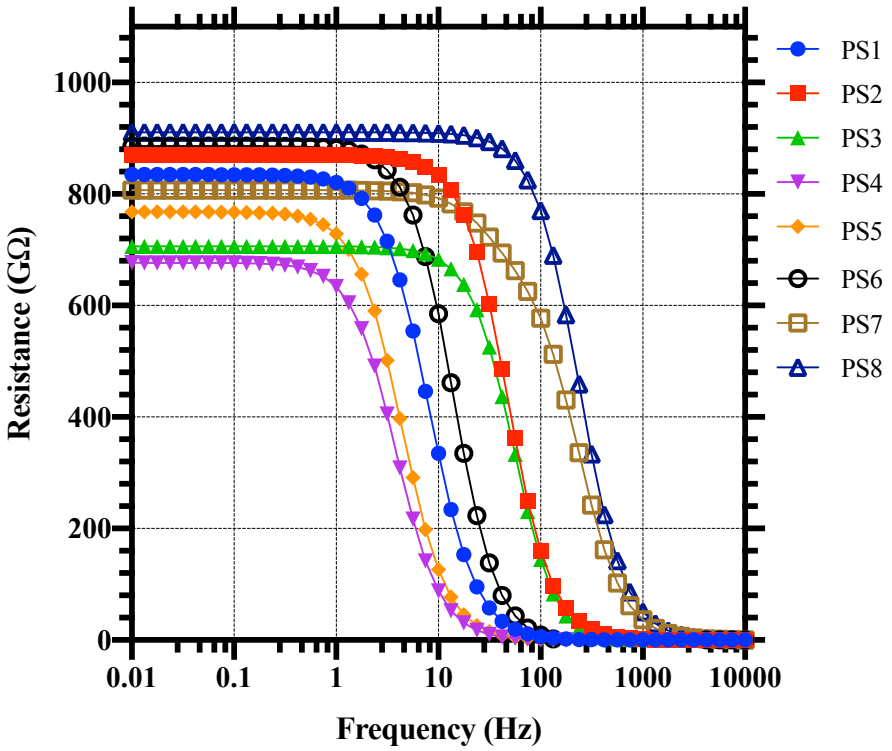


Figure 4.12 Simulated small-signal resistance value for all topologies. PS7 and PS8 are showing superior performance in the EEG frequency band (0.5 – 50Hz).

4.3 Conclusion

In this chapter, various pseudoresistor topologies have been reviewed in terms of the resistance value, distortion, frequency range, biasing and ease of implementation in a particular technology. Simulation results have been presented. Since used by Reid [4] in 2002, pseudoresistor became the default choice for setting up the high-pass cut-off frequency in neural amplifiers. Multiple implementations of the pseudoresistor have been proposed in the literature[4-19], targeting different specifications. Suitability of available pseudoresistors for the research have been determined, and finally, two novel pseudoresistor designs have been proposed. These novel pseudoresistors used symmetrical arrangement to avoid signal-dependent output shift. PS7 and PS8 achieved a 3dB bandwidth of 160Hz and 236Hz respectively, compared to the highest of 54Hz achieved for state-art-implementations designed for EEG application. PS7 and PS8 achieved a total harmonic distortion (THD) of 3.73% and 4.2%, respectively, compared to 7.5% of the nearest state-of-the-art implementation for EEG

amplifier. The THD performance is helpful for the low pass filter, which used the pseudo-resistor for the common-mode feedback circuit (see Chapter 6 for details). Furthermore, these pseudoresistors showed an increased input voltage range for which they can retain high incremental resistance.

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Chapter 5 - A high PSRR, ultra-low power curvature-corrected bandgap voltage reference

Chopper-stabilized topologies in EEG analogue front end, bring as a drawback transients in the power supply, which directly feed into the bandgap reference (BGR) output. Thus, a relatively high PSRR value (60dB is the initial target for the current design) is essential.

Since 1971 when BGR was introduced by Widlar [1-2], it has gone through a lot of research and many variants have been proposed in the literature. A basic first-order BGR circuit is inadequate to provide high precision voltage references. Thus, several curvature compensation techniques have been developed [4-6].

A compensation of high order nonlinearities is achieved by using different-type of resistors, with the cost of process dependency in [4], while in [5] a complementary to absolute temperature (CTAT) current is generated to correct the BGR accuracy. In [6] the high order nonlinearities are cancelled utilizing a MOS transistor operating in the weak inversion region. The most popular technique for high accuracy BGR is the piecewise linear which compensate the non-linear behaviour by integrating a non-linear component at the output of BGR [10-13].

The topology proposed in this thesis used a proportional to absolute temperature (PTAT) and a CTAT current generator, which was combined with a non-linear current generated using a CTAT voltage generator. A voltage subtractor circuit was then used to directly feed the supply noise into the PTAT and CTAT current generation loop, improving the power supply rejection ratio (PSRR). A current mirror OTA with the gain enhancement was used in the feedback path [8].

5.1 Traditional low-voltage bandgap reference

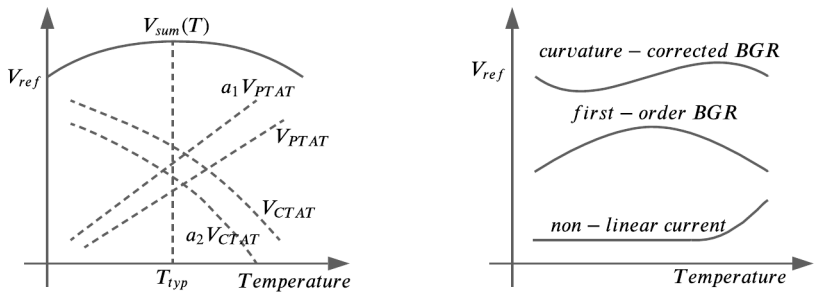
Low-voltage BGR circuits can be categorized into voltage mode or current mode topologies. In voltage mode topologies, the weighted sum of a negative temperature coefficient (TC) voltage and a positive TC voltage is the output of the BGR, as described in equation 5.1 and shown in Figure 5.1(a) [9].

$$V_{sum}(T) = a_1 V_{PTAT} + a_2 V_{CTAT} \quad ...(5.1)$$

In Figure 5.1(a), a traditional voltage mode BGR is presented. The negative TC voltage is complementary to the absolute temperature, V_{CTAT}, and produced by the forward biased voltage across a p-n junction, or more specific of Q_{1a} BJT's emitter-base voltage (V_{EB1}). The positive TC voltage proportional to absolute temperature, V_{PTAT}, is the thermal voltage *kT/q*, provided from the difference of base-emitter voltages (ΔV_{BE}) of two BJT's operating on different current densities. Thus, the BGR output voltage V_{bg_a} is given by [1]:

$$V_{bg\_a} = V_{EB2a} + (1 + \frac{R_{2a}}{R_{1a}})\frac{kT}{q}\ln N \quad \ldots(5.2)$$

where *N* is the area ratio of Q_{2a} and Q_{1a}, symbol *k* is the Boltzmman's constant (1.38×10^{-23} J/K), *T* is the absolute temperature and *q* is the electronic charge (1.6×10^{-19} C).



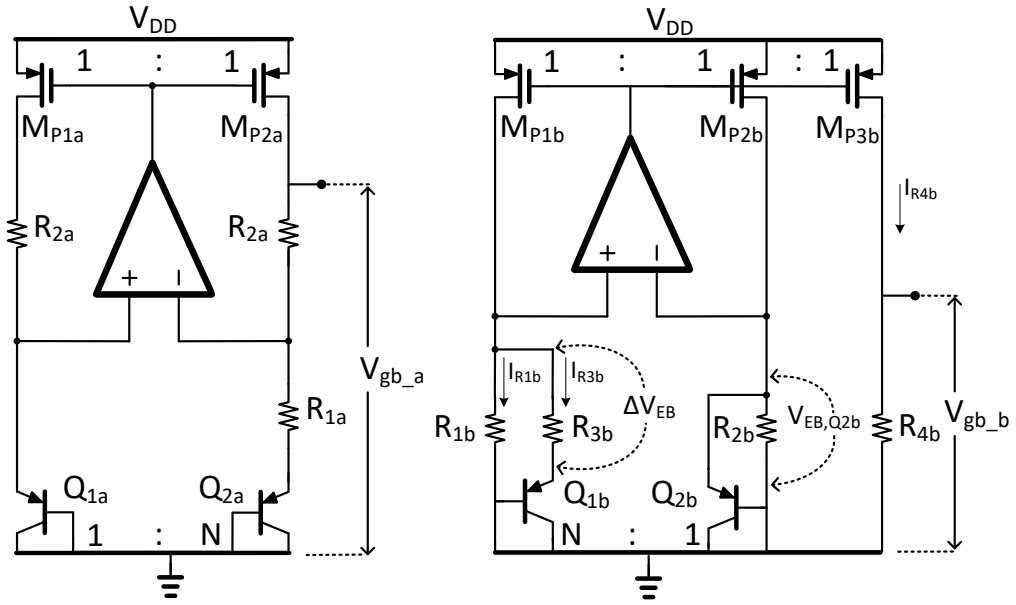
(a) ***(b)***

Figure 5.1 Temperature independent voltage generation. (a) First order BGR, (b) curvature corrected BGR.

A traditional current mode BGR topology is presented in Figure 5.2(b) [9]. In this case the BGR output is produced across resistor R_{4b}, through the current I_{R4b} flowing in this branch. This current is the summation current of I_{R1b} and I_{R3b} currents. The two voltages $V_{EB,Q2b}$ and ΔV_{EB} are related to currents I_{R1b} and I_{R3b}, as presented in equation 5.3 and equation 5.4 [1].

$$I_{R3b} = \frac{\frac{kT}{q}\ln N}{R_{3b}} \quad \ldots(5.3)$$

$$I_{R1b} = \frac{V_{EB,Q2b}}{R_{1b}} \qquad \ldots(5.4)$$



(a) *(b)*

Figure 5.2 Temperature independent voltage generation, (a) PTAT generation, (b) combining a PTAT and a CTAT.

The current I_{R3b} is a PTAT current, while I_{R1b} contains a CTAT component and a nonlinear component. This is more clear, considering the dependency of voltage $V_{EB,Q2b}$ with the absolute temperature. This is described in equation 5.5 where V_{G0} is the bandgap voltage of the silicon at 0 K. Parameters η and δ are process related and represent the temperature variation of the mobility and the collector current.

$$V_{EB,Q2b} = V_{G0} - [V_{G0} - V_{EB,Q2b}(T_0)]\frac{T}{T_0} + (\eta - \delta)\frac{kT}{q}\ln(\frac{T}{T_0}) \qquad \ldots(5.5)$$

From equation 5.5 is clear that the nonlinear current, I_{NL}, is given by:

$$I_{NL} = \frac{[(\eta - \delta)\frac{kT}{q}\ln(\frac{T}{T_0})]}{R} \qquad \ldots(5.6)$$

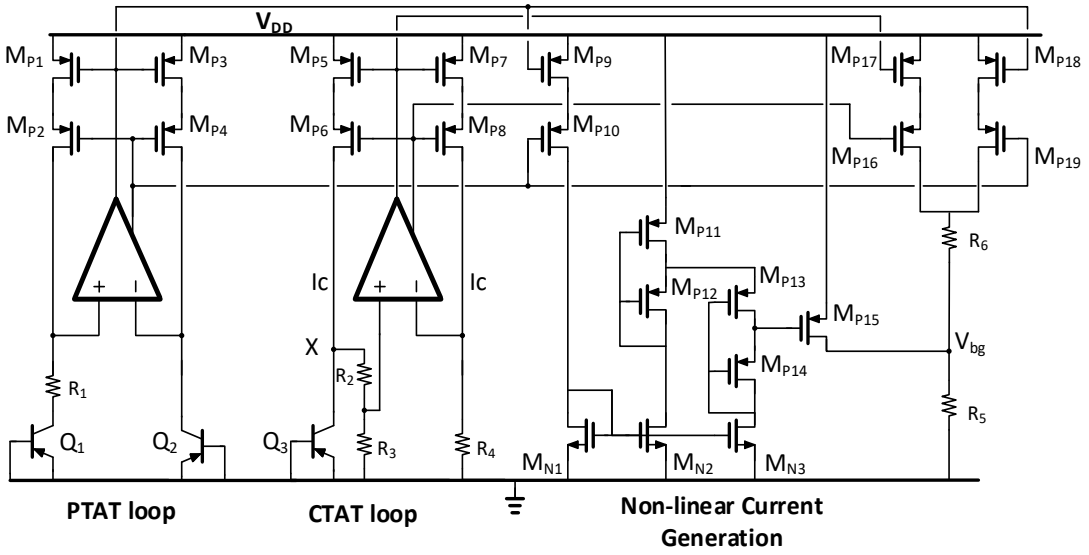


Figure 5.3 Proposed curvature-compensated BGR.

The first order BGR uses a PTAT current to compensate for the first order temperature dependence, which can help in achieving a temperature coefficient between 20-25ppm/°C. To improve the temperature coefficient, the non-linear component needed to be compensated using a curvature correction technique.

5.2 Proposed low-voltage curvature corrected current mode BGR

The proposed BGR consists of a PTAT current generator, a CTAT current generator and a non-linear current generation circuitry, to compensate for the curvature due to the non-linear current component in the base emitter characteristic of the transistor (equation 5.5) (Figure 5.3). The PTAT current generation circuit used is similar to the one in Figure 5.2(a). The CTAT current generation circuit function is derived in the following:

Through the negative feedback:

$$I_c R_4 = (Ic - I_1) R_3 \qquad \ldots(5.7)$$

Rearranging,

$$I_1 = I_c \left[1 - \frac{R_4}{R_3} \right] \qquad \ldots(5.8)$$

Also, using KVL at Node X:

$$(I_c - I_1)(R_2 + R_3) = V_{EB_{Q3}} \quad \ldots(5.9)$$

Combining equations (5.8) and (5.9), the CTAT current, I_c is given by:

$$I_c = V_{EB_{Q3}} \frac{R_3}{R_4(R_2 + R_3)} \quad (5.10)$$

A non-linear current is then generated which is combined with the PTAT and CTAT currents on a resistor to give a curvature corrected bandgap reference. The non-linear current generation circuit is shown in the Figure 5.4 [14]. A CTAT voltage is generated at node D, which controls the magnitude of the non-linear current (Inl).

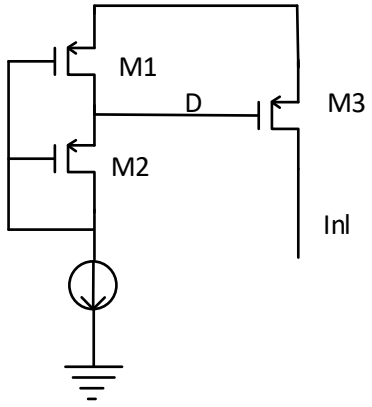


Figure 5.4 Basics of a non-linear current generation circuit.

The voltage at node D, is given by:

$$V_D = V_{SG_2} - V_{SG_1} + V_{DD} \quad \ldots(5.11)$$

$$= \eta \frac{kT}{q} \left[\ln \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \right] = \eta \frac{kT}{q} \ln K \quad \ldots(5.12)$$

where, $K = (W/L)_2/(W/L)_1$.

The gate-source voltage of the MOS transistor M3 can be modelled as,

$$V_{SG_3} = \eta \frac{kT}{q} \ln(1/K) \quad \ldots(5.13)$$

When V_{SG_3} is much less than the threshold voltage V_{th}, there will be no current flowing through M3. In sub-threshold region the non-linear current can be given as [14]:

$$I_{NL} = I_{D0} \left(\frac{W}{L} \right)_3 \exp \frac{(V_{SG_3} - |V_{th}|)}{\eta U_T} \quad \ldots(5.14)$$

And in the saturation region of M3, the current can be given as [1]:

$$I_{NL} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_3 (V_{SG_3} - |V_{th}|)^2 \quad \ldots(5.15)$$

The variation of the gate source voltage, V_{SG_3} can be controlled using a cascode of the simple self-cascode structure explained in Figure 5.4. From equations (5.14) and (5.15), it is evident that the generated non-linear current is independent of the supply voltage. To improve the power supply rejection ratio (PSRR) in the PTAT and the CTAT loop, a voltage subtractor circuit is used [7] which adds the supply noise in the feedback loop onto the gate source voltage of current sources, which enhances the PSRR of the circuit (see Figure 5.5). Also, another major contributor of the supply noise is the limited drain source resistance (R_{ds}) of the MOS transistor, which is enhanced here using a cascode structure [15-17].

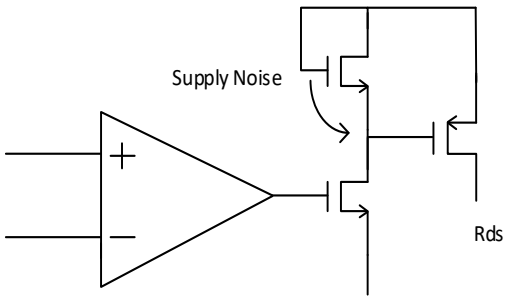


Figure 5.5 Voltage subtractor circuit employed to enhance the PSRR.

The PTAT, the CTAT and the non-linear currents are combined and converted into voltage using high-precision poly resistors. The simulation is carried out using 0.18μm CMOS technology. The temperature coefficient achieved was 2.395ppm/°C (for temperature range -

10-120°C) and the PSRR was -84.62dB. The nominal supply voltage used here was 1.2V. The total current consumption of the whole bandgap, including beta-multiplier current sources and the start-up circuit [3] was 4.691µA.

The performance comparison with the published results is given in Table 5.1. The achieved PSRR and TC was better than state-of-the-art at the time of reporting.

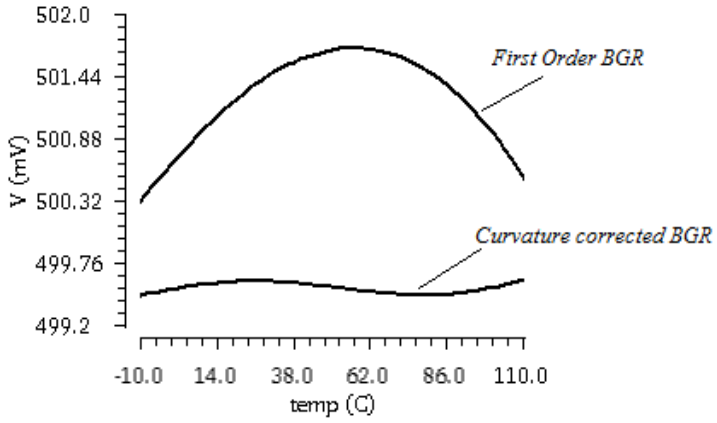


Figure 5.6 Simulation result for the first order BGR and the curvature compensated BGR using the proposed technique.

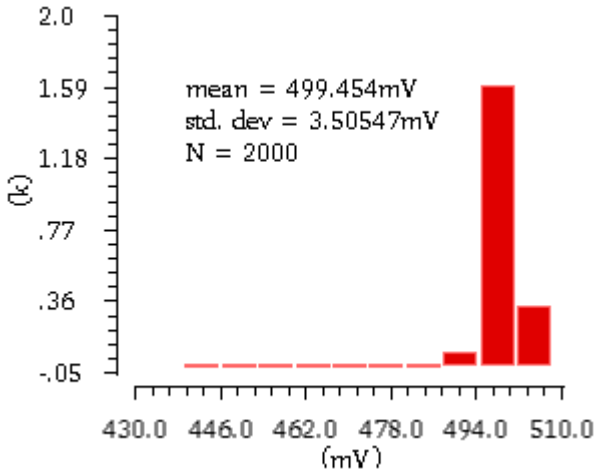


Figure 5.7 Simulated Monte-Carlo variation in the proposed curvature-corrected BGR (see Figure 5.3), 3σ variation simulated is 2.1% for 2000 samples (bin=10).

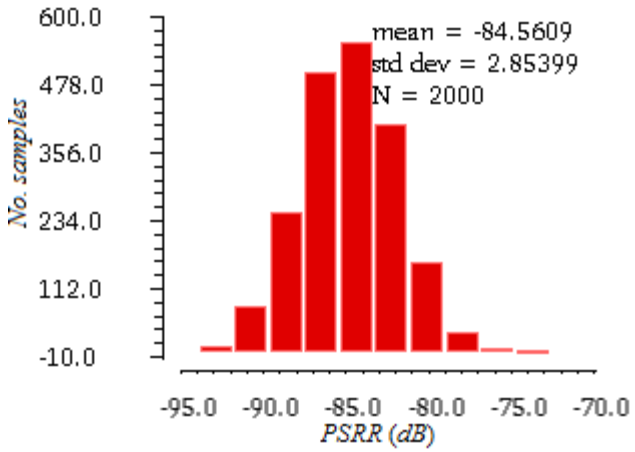


Figure 5.8 Simulated Monte-Carlo variation in the PSRR of the proposed curvature-corrected BGR, 3σ variation simulated is 10.1% for 2000 samples (bin=10).

Table 5.1 Comparison with other published results.

Parameter	**[12]**	**[13]**	**[18]**	***This work***
Year reported	2012	2015	2021	-
Min. supply (V)	1.8	1.2	0.85	1
Current consumption (μA)	9.74	120	17.64	4.691
Reference Voltage (mV)	500	735	538	500
PSRR (dB)	-58	-30	-40	-84.62
TC (ppm/°C)	7.5	4.2	12	2.295
Temp. Range (°C)	-30~120	-40~120	-40~120	-10~110
Active Area (mm^2)	0.075	0.063	0.0073	0.0369
Technology (μm CMOS)	0.35	0.13	0.028	0.18

5.3 Conclusion

This chapter briefly discussed the importance of a stable voltage reference in analogue applications. A brief study on available bandgap reference topologies was presented , along with the theory behind the temperature independence of the reference. Furthermore, the presence of a non-linear component in the traditional BGR topology is discussed along with the necessity to implement a curvature compensation topology. Finally, a novel architecture of curvature corrected bandgap reference is presented [17].

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Chapter 6 - Sallen-Key Low Pass Filter Design

6.1 Introduction

The signal acquisition front end in EEG systems have three primary roles : detecting the signal, conditioning it and converting it to digital for further processing. Filtering is one of the vital tasks to remove all the unwanted signals before it is sent to ADC for conversion. Along with isolating the wanted signal, a low pass filter also acts as an anti-aliasing filter for the ADC, so the sample rate for the ADC does not need to be very high.

Physiological signals are very low frequency. Implementing a high time constant filter off-chip is straightforward. However, creating a very large time constant circuit on the chip is a difficult problem, as the size of the resistors and capacitors limits the value of these components. Also, the resistance variation can be significant, impacting the accuracy of the cut-off frequency of the filter. Three options were considered for this research:

- Switched capacitor filters: The main issue with switched-capacitor filters is inaccuracy due to the clock feedthrough, the charge injection and the charge sharing. So, the switches need to be designed very carefully. Also, to limit the kT/C noise, the capacitor size should be large. And large time constants need bigger size capacitors. Usually, switched capacitor filters consume higher power than continuous-time filters [1].

- Gm-C filters: These open-loop filters are relatively inexpensive to build. The major issue is to tune the Gm value, which can vary up to 20-30% across the corners. Also, linearity for the Gm-C filter can be a significant issue [7].

- Active RC filter: The active RC filter is generally used before the ADC for rejecting unwanted frequency components and preserve the relevant signal due to its high linearity and the lower power. The Sallen-Key filter is the most popular among active filters because it is a low noise, lower power, and easy to analyse and design. But the conventional Sallen-Key filter design is only single-ended, so the most common way to implement a fully differential topology is to use two sets of OTA plus RC or use a DDA instead of OTAs. A DDA based fourth-order fully differential Sallen-key low pass filter (LPF) was designed for this research[4].

6.2 Sallen-Key low pass filter design

The Sallen-Key (SK) topology was developed by R. P. Sallen and E. L. Key at the MIT Lincoln Laboratory in 1955. The Sallen-Key (SK) filter employs a single op-amp and a network of resistors and capacitors to provide a second-order transfer function [2-3]. A typical unity gain SK low-pass filter is shown in Figure 6.1. The op-amp is connected in a unity gain configuration.

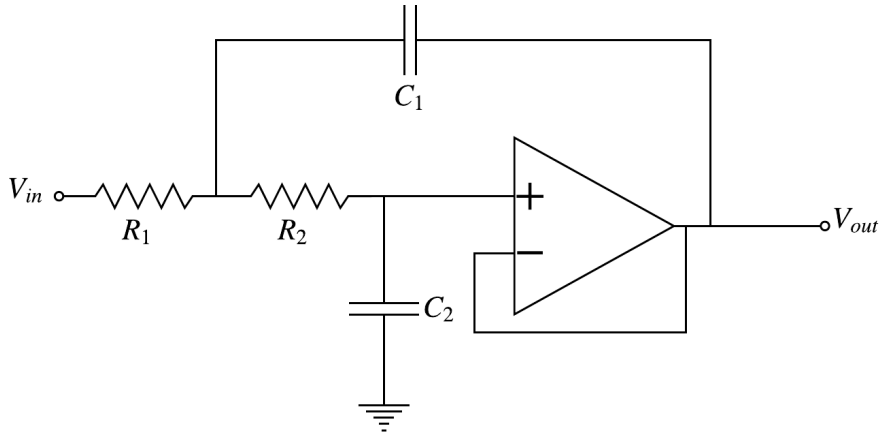

Figure 6.1 A single-ended Sallen-Key low pass filter.

The operation of the SK filter can be explained qualitatively as [2-3]:

- At lower frequencies, where C_1 and C_2 appear as the open circuits, the buffered signal appears at the output.
- At higher frequencies, the C_1 and C_2 appear as short circuits, so the signal is shunted to ground at the amplifier's input, this signal is then amplified, and no signal appears at V_{out} .
- Close to the cut-off frequency, the impedance of C_1 and C_2 is of the same order as R_1 and R_2 , and the positive feedback through C_1 provides Q enhancement of the signal.

A mathematical model for the SK low pass filter topology can be expressed as [2-3]:

$$H(s) = \frac{1}{s^2 \cdot C_1 \cdot C_2 \cdot R_1 \cdot R_2 + s \cdot C_2 \cdot (R_1 + R_2) + 1} \quad \ldots(6.1)$$

$$f_0 = \frac{\omega_0}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}} \quad \ldots(6.2)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \cdot \frac{\sqrt{R_1 \cdot R_2}}{R_1 + R_2} = \frac{\sqrt{C_1 \cdot C_2 \cdot R_1 \cdot R_2}}{C_2 (R_1 + R_2)} \quad \ldots(6.3)$$

where, f_0 is the cut-off frequency, *H(s)* is the gain and *Q* is the quality factor for the filter.

6.3 Design of a fully differential difference amplifier

After it was introduced by Edward Säckinger and Walter Guggenbühl in 1987 [4], the CMOS differential difference amplifier (DDA) has found extensive usage in analogue signal processing like continuous time filters, common mode detection circuit, switched capacitor filter, etc [4-6]. As shown in Figure 6.2, the DDA is an extension to the concept of the operational amplifier. The main variation is that the DDA has four inputs (V_{pp}, V_{pn}, V_{np} and V_{nn}) and the output for the DDA can be written as:

$$V_{out} = V_{op} - V_{on} = A_o \left[(V_{pp} - V_{pn}) - (V_{np} - V_{nn}) \right] \quad \ldots(6.4)$$

where, A_o is the open loop gain for the DDA.

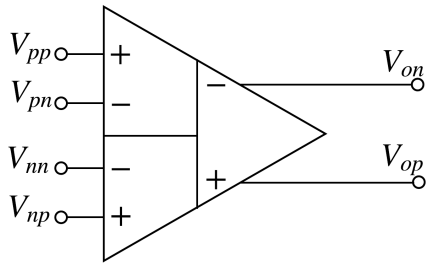

Figure 6.2 Symbol for the DDA [4].

The signal flow diagram representation of a DDA is shown in Figure 6.3. Two transconductors (voltage to current convertors) of the DDA transform the input differential voltages into currents. Further on these currents are subtracted and turned into a voltage by a current to voltage convertor and then amplified by a gain block.

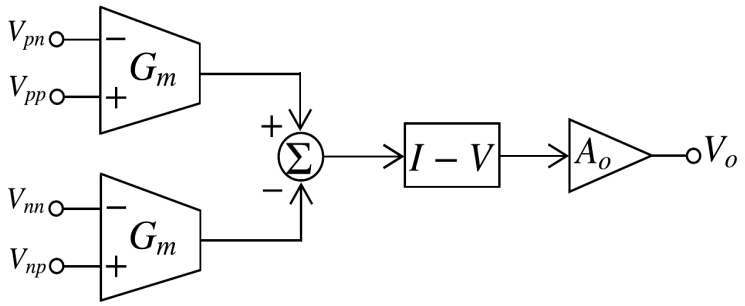

Figure 6.3 Signal flow diagram representation for the DDA [4].

When a negative feedback is introduced either in V_{np} and/or V_{pn}, the following expression is obtained:

$$V_{pp} - V_{pn} = V_{np} - V_{nn}, \text{ with } A_o \to \infty \qquad \ldots(6.5)$$

This open loop gain (A_o) needs to be as large as possible to achieve high-performance operation. Otherwise, the difference between the two differential voltages will increase, as A_o decreases.

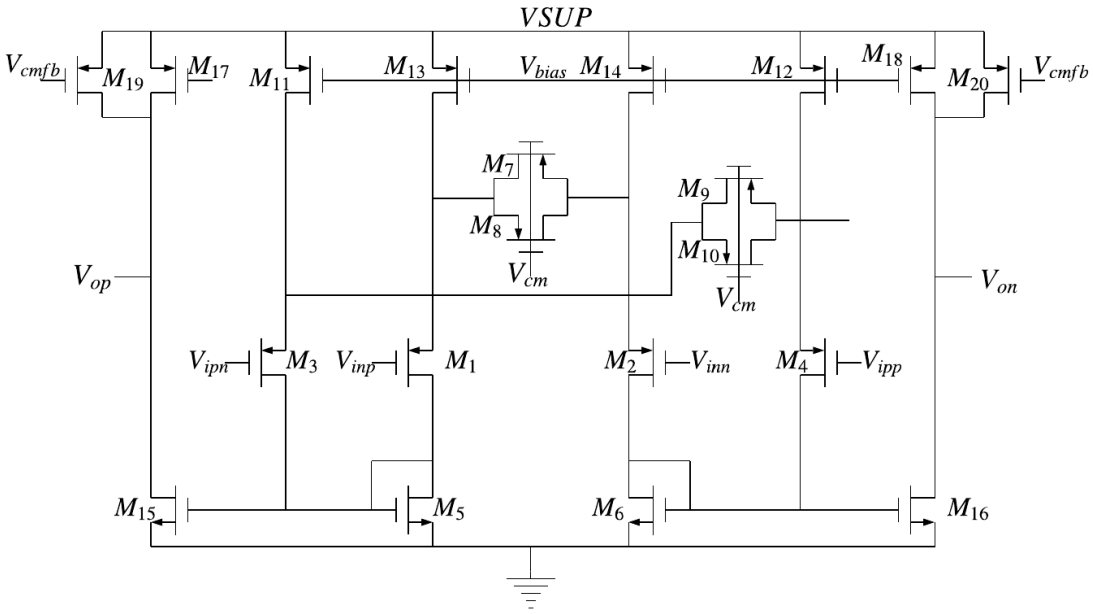

Figure 6.4 Fully differential difference amplifier.

The implementation of the DDA is similar to the full-differential current mirror OTA. The circuit, given in Figure 6.4, excludes the current mirror biasing and the common mode feedback (CMFB) circuit. The DDA is composed of two parts: the input stage formed by (M_1-M_4), and the output stage (M_{15}-M_{20}). To achieve a high gain, all the transistors used in the DDA design are stacked composite transistors, with a combination of a high-threshold and standard threshold device [10] (see Figure 6.5). Advantages of a composite transistor are: higher impedance, high gain, and a higher cut-off frequency than a single transistor [10]. A current ratio of 1:4 is used between the two transistors, M_{17} and M_{19}, to reduce the load on the output stage of the CMFB circuit. The transistors M_7-M_{10} are used to linearize the input-gm. Also, a trimming current can be pushed to the two tails individually to compensate for any input offset. The offset calibration circuit was not used in the final implementation as the input offset of the amplifier measured was very low.

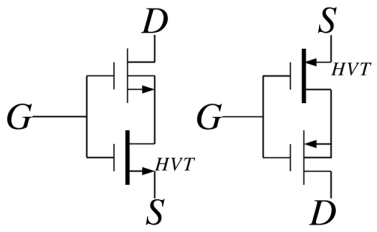

Figure 6.5 Composite stacked transistors.

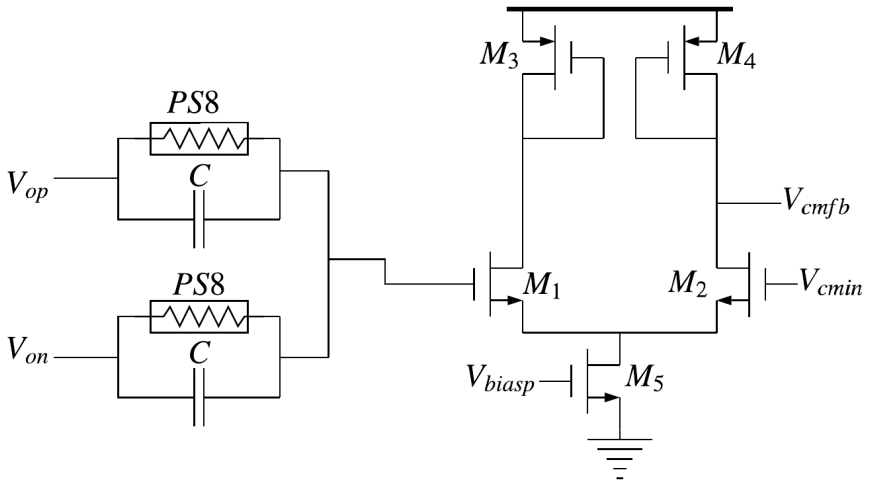

Figure 6.6 Common-mode feedback circuit used in the DDA.

The common-mode feedback circuit used was the simple resistive divider based (Figure 6.6). A pseudo-resistor (PS8- detailed explanation in Chapter 4) was used instead of a standard

resistor to achieve a high-value resistor without loading the amplifier output. The diode-connected loads were used in the error amplifier to improve its operating frequency, and so as not to impact the primary feedback loop.

6.4 DDA based fully-differential Sallen-Key low pass filter

A DDA is used to implement a fully differential SK filter, as shown in Figure 6.7. By assuming, $A_o \to \infty$, we can obtain $V_{pp} - V_{np} = V_{pn} - V_{nn} = V_{on} - V_{op}$, and after some manipulation, the transfer function for the SK filter can be determined as [4]:

$$H(s) = \frac{V_{on} - V_{op}}{V_{inp} - V_{inn}} = \frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \qquad ...(6.6)$$

where, $\omega_0 = \sqrt{\frac{1}{R_1 \cdot R_3 \cdot C_1 \cdot C_3}}$ is the undamped natural frequency and $Q = \frac{\sqrt{R_1 \cdot R_3 \cdot C_1 \cdot C_3}}{(R_1 + R_3) \cdot C_1}$ is the quality factor. For this research, the components are chosen to have equal values, i.e. ($R_1 = R_2 = R_3 = R_4$), and ($C_1 = C_2 = C_3 = C_4$). This choice will give the value of Q=0.5, an overdamped system, but make the design easier. A passive filter could also be used here instead of a Sallen-Key filter, though it would require a buffer to drive the ADC, that is the reason why it was not pursued. A cascade of two Sallen-Key filters is used to achieve a fourth order fully differential Sallen-Key low pass filter (Figure 6.7).

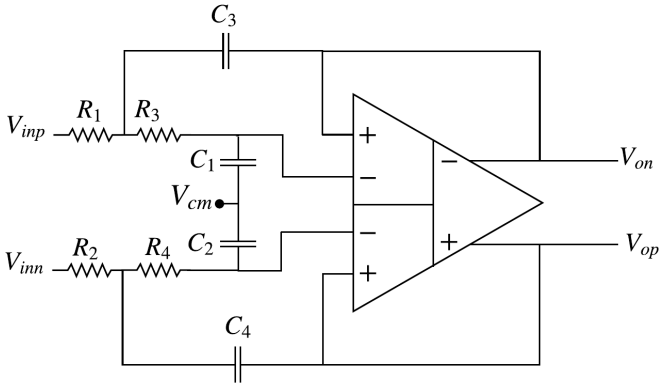

Figure 6.7 Fully-differential Sallen-Key low pass filter.

6.5 A duty-cycled resistor

The bandwidth of the signals assumed in this work is between 0.5-50Hz [12-16]. So, to get the cut-off frequency of 500Hz, $C_1 = C_2 = C_3 = C_4 = 1pF$ were used. This required $R_1 = R_2 = R_3 = R_4 = 320\text{M}\Omega$.

Implementing such a high resistor value on the chip is extremely difficult. So, a duty-cycled resistor was used, where a duty cycle of 1:100 was chosen to increase the effective resistor value to 100X [7-8]. That allowed the use of 3.2MΩ to implement the effective resistance of 320MΩ.

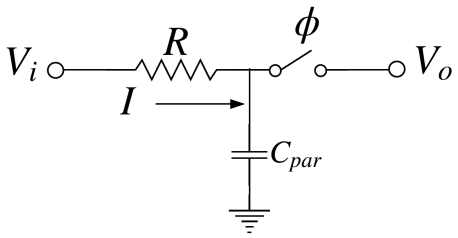

Figure 6.8 A duty-cycled resistor (DCR).

A duty-cycled resistor (DCR) is the series combination of a resistor and an ideal switch whose clock has a variable duty-cycle[7-8]. The DCR circuit is shown in Figure 6.8. In a DCR, the duty-cycle of the applied clock is utilized to regulate the average current flowing through the DCR branch. The average current flowing across the DCR can be computed as[7]:

$$I_{av} = \frac{V_i - V_o}{R / D} \qquad \ldots(6.7)$$

where D is the fractional duty-cycle of the clock signal. The value of DCR can now be defined as [7]:

$$Rav \triangleq \frac{R}{D} \qquad \ldots(6.8)$$

where *Rav* is average equivalent resistance (DCR) and can be calculated as the average branch current over the applied voltage. The DCR is then inversely proportional to the duty cycle of the clock.

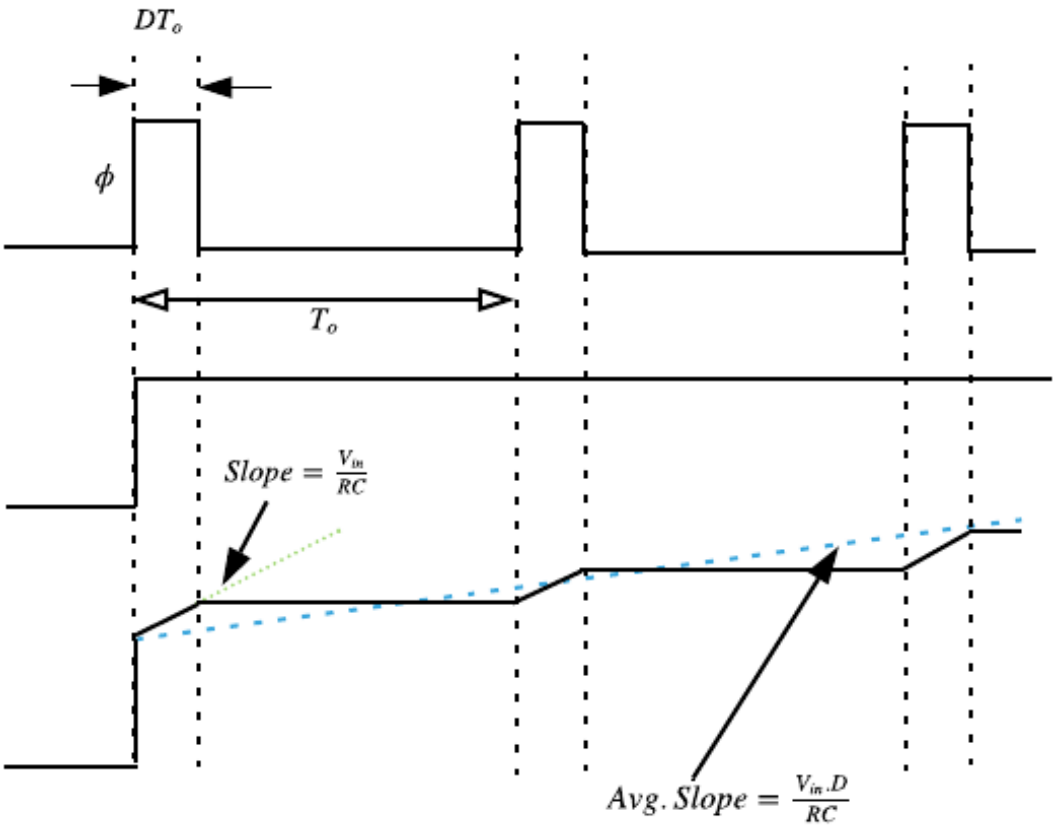

Figure 6.9 Simulated transient response of the LPF to a step response.

The increased resistance obtained from the duty-cycled resistor is qualitatively explained in Figure 6.9. When the switch is ON, the LPF behaves like a linear RC filter. The slope of the output signal is approximately V_{in} / RC. Once the switch is OFF, charge flow across the capacitor is stopped, which eventually keeps the output voltage constant. When a duty-cycle factor *D* is used, the average slope of the filter output is ($V_{in} D / RC$). Hence, this filter response can be interpreted as an equivalent LPF with a time constant of *RC*/*D*, which means an equivalent resistance of *1*/*D* times the original value. This allows the implementation of a large equivalent resistance by choosing a moderate size resistance and a small duty cycle.

The effective resistance that can be achieved is limited by the parasitic capacitor C_{par} of the switch and the resistor. Ideally, the output is to be held constant when the switch is OFF, but it continues to change because of charge sharing between *C* and C_{par}. The maximum resistance that can be realized is thus $1 / f.C_{par}$, which can be set high enough by minimizing the switch and the resistor size.

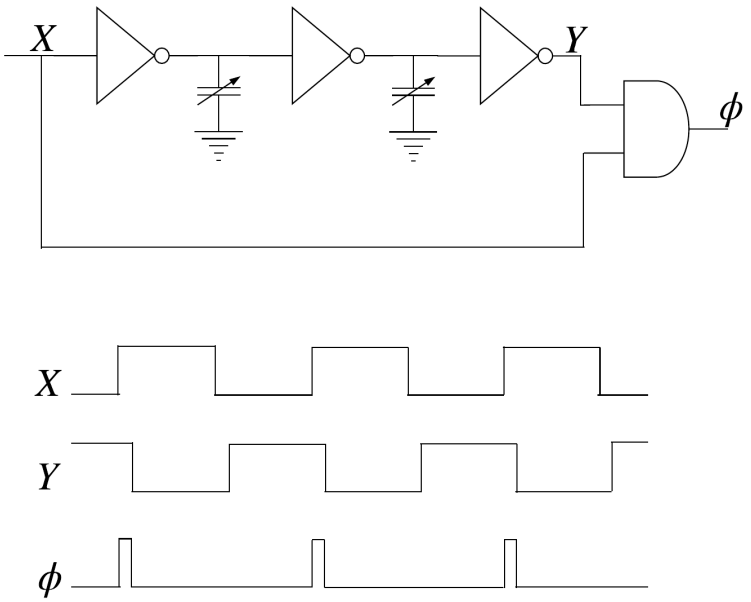

Figure 6.10 Duty-cycled clock generation circuit and the timing diagram [8].

The duty-cycle clock (Φ) generation circuit is shown in Figure 6.10. The input clock signal is first inverted and delayed by passing through a set of delay blocks composed of inverters and tunable capacitors. This inverted and delayed signal is fed to an AND gate along with the original clock signal. The output signal has the same frequency as the input clock, with the delay of the delay-line determining the duration of the ON-pulse. It is easy to obtain a delay of several nanoseconds for a clock of few kHz. The duty-cycled clock (Φ) is then used to control a minimum size MOS switch.

6.6 Fourth order Sallen-Key low-pass filter

A fourth-order SK filter was implemented by cascading two Sallen-Key filters [6],[11](see Figure 6.11). The cut-off frequency of the filter was set using the ratio of resistor and capacitors. No tuning is used in this research, though a MOS resistor can be used in parallel with main resistors to tune the frequency. Also, multiple resistors controlled digitally can be used for tuning, but that will incur a huge area penalty.

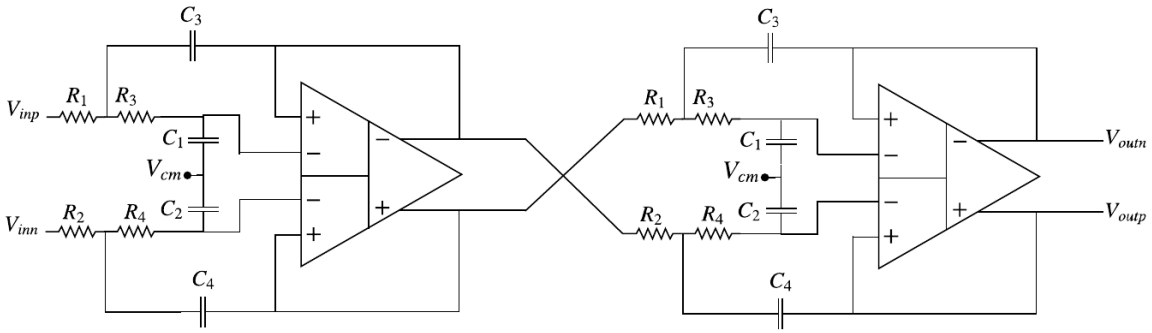

Figure 6.11 Fourth order fully differential Sallen-Key low pass filter.

Same size resistances and capacitances were used to simplify the design. This resulted in a *Q*-factor of 0.5, which is overdamped maximally flat response, but was good enough for this work. The simulated frequency response for the filter is given in Figure 6.12..

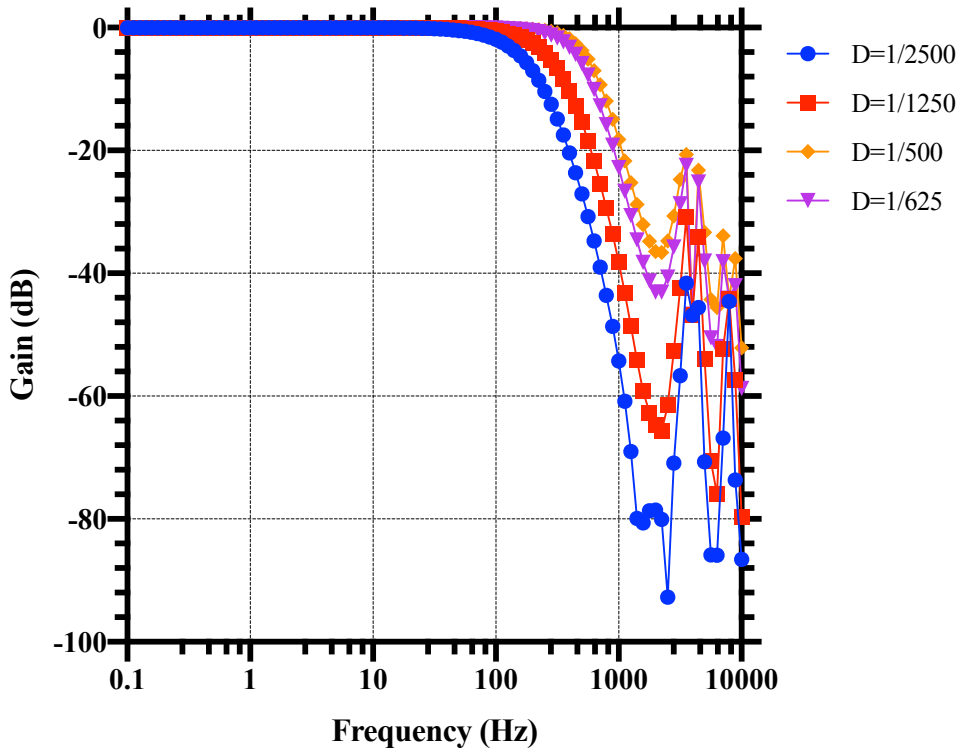

Figure 6.12 Simulated frequency response for the fourth order Sallen-Key low pass filter for different duty cycles of the DCR.

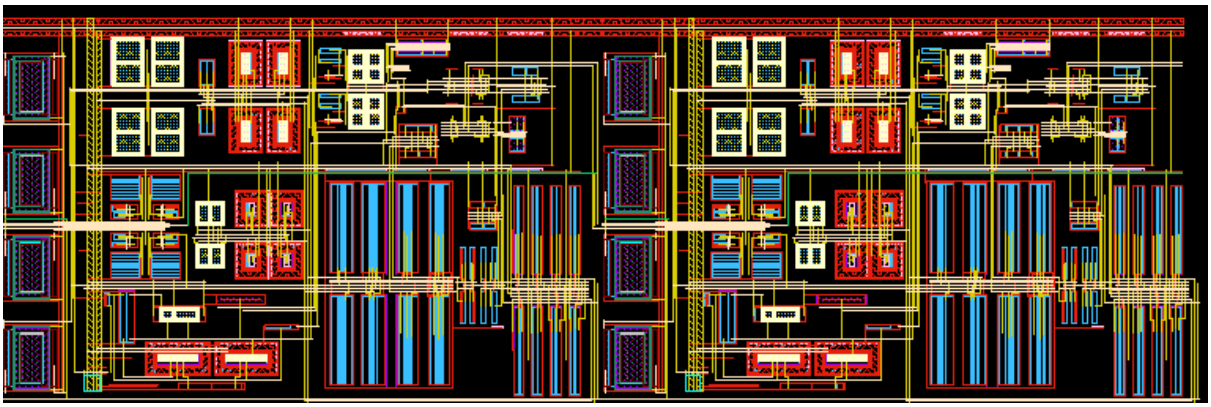

Figure 6.13 Layout of the final implemented fourth order Sallen-Key Low pass filter.

6.7 Conclusion

A low pass filter is a critical component in the acquisition signal chain. A chopped amplifier exhibits large spikes at the output, which need to be suppressed before the ADC processes its output signal. Also, the risk of aliasing exists if the signal converted by the ADC has a signal component at a larger frequency than twice the sampling frequency. This chapter discussed three common filter implementations to deal with this, as well as the rationale for choosing an active RC filter in this work. A fully differential DDA design was also presented, using pseudoresistors in the common-mode feedback path. For achieving high gain in the amplifier, composite transistors were used. A fourth order Sallen-Key low pass filter architecture was then presented, which used duty-cycled resistors to increase the total resistance of high precision poly resistors. The filter achieved a quality factor of 0.5, and can be improved in future designs to Butterworth response with a quality factor of 0.707.

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Chapter 7 - The complete analogue front-end for EEG applications

7.1 Introduction

The main circuit blocks for an ultra-low-power analogue front-end (AFE) for EEG applications have been presented in previous chapters. This chapter presents the combination of these blocks to form the full AFE.

7.2 Non-overlapping clock generation circuit

The non-overlapping clock generation circuit is one of the vital circuits in switched-capacitor applications, where it is essential to avoid charge loss when switches turn state from ‘on’ to ‘off’ or vice versa. The term non-overlapping clock itself refers to the fact that signals are running at the same frequency and there is a time interval when both are in ‘off’ state, and also both signals cannot be simultaneously in ‘on’ state. This ‘off’ state usually occurs when one of the clocks is switching from ‘off’ to ‘on’ or vice versa.

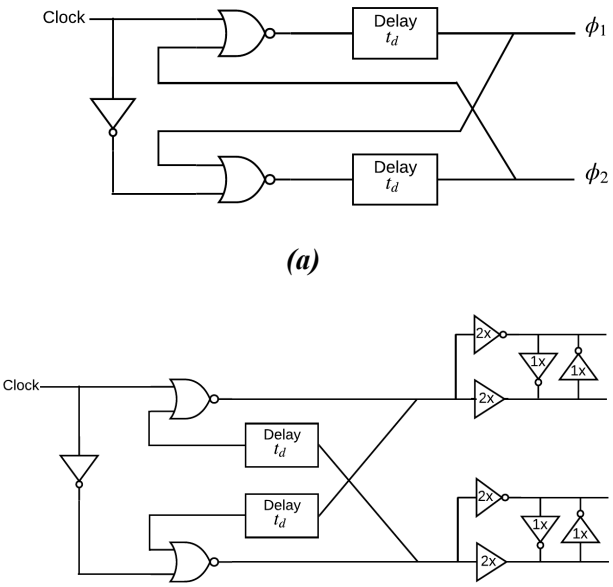


Figure 7.1 (a) Non-overlapping clock generator. (b) Non-overlapping clock generator with the output latch (for aligning the edges).

The non-overlapping clock generation circuit used in this work was NOR gate based. This was used for generation of clock signals for the SAR ADC [2]. The basic non-overlapping clock generation circuit is shown in Figure 7.1(*a*). This circuit was further modified to generate four phases (see Figure 7.1(*b*)). A regenerative latch was used to recover the edges of the clock signal.

7.3 Current generation block

The voltage and the current reference play a critical role in analogue and mixed-signal circuits. They are essential components of several analogue circuits such as the ADCs, DACs, filters and amplifiers. Accuracy of the reference decides the biasing accuracy of the circuit, and hence their proper functioning. In this research, a single bandgap was used to generate multiple reference voltages across the chip and also current for different blocks, such as the EEG amplifier, biasing current for the pseudo-resistor, biasing for the low pass filter and the bias current for the ADC.

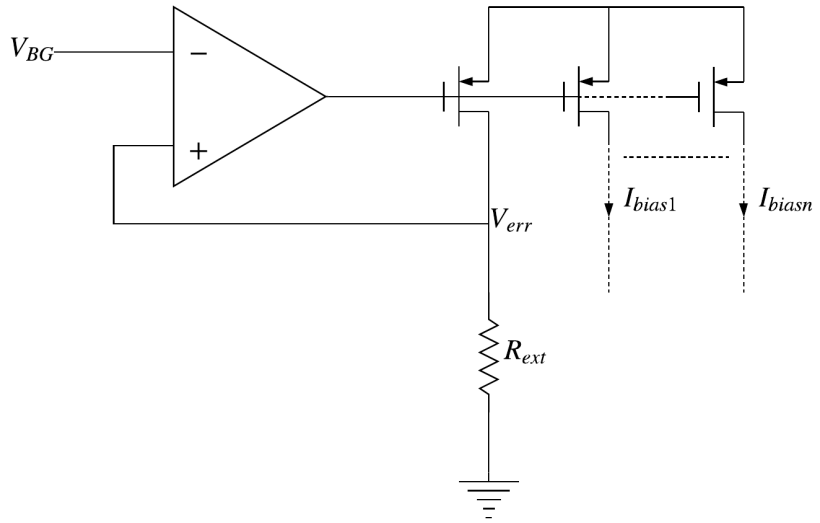


Figure 7.2 Block diagram of the chip current generation circuitry.

A very high accuracy voltage from a bandgap reference (<1%) was applied across a very high accuracy external resistor (<0.5%) to generate a bias current which was then copied over multiple branches to provide current references for the whole chip. Currents are usually

preferred for biasing as voltages may be subject to resistive drops across the resistive metal lines.

7.4 12-Bit fully differential SAR ADC

In the real world, signals are inherently analogue. Analogue signals are extremely difficult to process and transfer. For applying any signal processing algorithm, it is much easier to translate the analogue signal into the digital, which provides noise immunity, ease of processing and transfer. An analogue to digital converter provides this translation of analogue signal in the required frequency band to digital, which can then be processed with a simple microcontroller. The accuracy of the digitised signal depends on the available resolution (number of bits) of the ADC. Among many available ADC architectures, SAR ADCs are well-known for their power-efficient design with a straightforward architecture [1-6]. The only analogue component they use is a comparator and the capacitive DAC. Lesser analogue components reduce the necessity of biasing circuitry and increases the noise immunity, as the comparator can be easily shielded from the rest of the design using a deep n-well. The main issue with SAR ADC architectures is that they are unsuitable for high-speed implementation, as they require several comparison cycles to make a single decision; and also as the capacitive DAC noise sets the minimum array size.

$$v_{noise} = \sqrt{\frac{kT}{C}} \qquad \ldots(7.1)$$

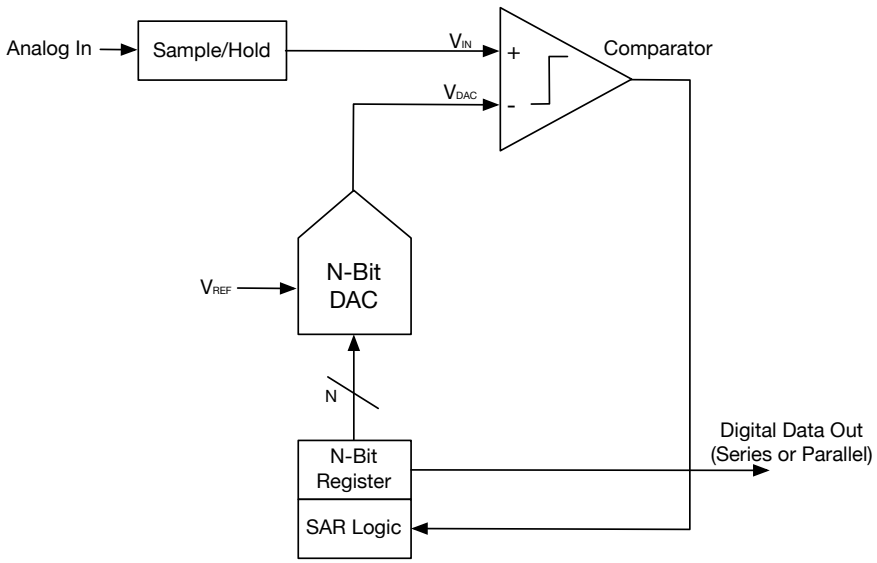


Figure 7.3 Simplified N-bit SAR ADC architecture [6].

A simplified architecture of an N-bit SAR ADC is presented in Figure 7.3. The analogue input voltage (V_{IN}) is stored on a sample/hold circuit. The binary search starts with the MSB set to 1, which sets the DAC output to be $V_{REF}/2$. A comparison is performed to check if V_{IN} is higher than $V_{REF}/2$. If larger, the comparator outputs a logic high (1), and moves on to the next bit, till all the bit cycling is performed. Once this is done, the N-bit digital output is available in the SAR register. This can also be stored in a shift register, depending on the final system.

The SAR ADC architecture used here is fully-differential, for avoiding the supply noise and other common-mode noise (see Figure 7.4). The noise immunity of the SAR ADC is very critical in a noisy system where high clock activity is present - like that corresponding to chopping. Since the resolution needed here is 12-bit, a binary-weighted capacitive DAC would require an extensive capacitor area. For example, if the unit capacitance size is 120fF, then a 245.76pF capacitor is needed. So, the underlying architecture used in this thesis is a split DAC based, similar to the one in [9]. This capacitive DAC provides the sample/hold along with the DAC function for the ADC, rather than implementing a separate sample/hold and DAC system [8-10].

The split DAC usually consists of two capacitor arrays - Main DAC and the Sub DAC- connected together by an attenuation capacitor. The value of attenuation capacitor can be calculated using [10]:

$$C_{atten} = \frac{\text{sum of the Sub DAC array capacitors}}{sum \text{ of the Main DAC array capacitors}} \times C_{unit} \qquad ...(7.2)$$

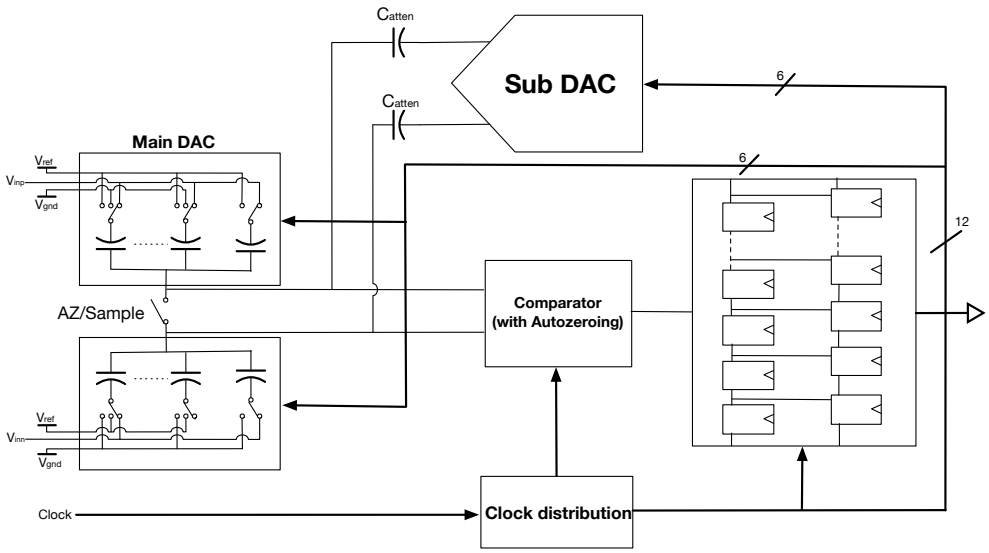


Figure 7.4 Block diagram of the fully differential 12-bit SAR ADC implementation.

The timing for the ADC is explained in Figure 7.5. There are 16 clock cycles needed for the full conversion. The first four cycles are for sampling, purging and auto-zeroing. The remaining 12 clock cycles are used for bit cycling and converting the data. The DAC capacitor array and also the auto-zeroing capacitor for the comparator are purged of any residual charge during the first positive pulse, using the signal 'prg'. This purge signal is necessary, as the common voltage for the comparator auto-zeroing is generated through the capacitive divider, and any residual charge on the top plate of the capacitor can corrupt this common mode voltage. After the ‘prg’, an auto-zeroing signal 'az1' for the first pre-amp is provided for 1.5 clock periods, followed by two clock periods for the second 'az2' and 2.5 clock periods for the third 'az3' [9].

While auto-zeroing is happening, the second array of set/reset type flip-flops are reset using the ‘clrflops’ signal and stays on for half a clock cycle after auto-zeroing is finished. Immediately after the ‘az3’ is completed, the sample signal will turn high for one clock period to sample the differential inputs onto the DAC array. Straight after ‘clrflops’ is disabled, a single high pulse ‘ibit’ starts the SAR bit-cycling, which carries on for the next 12 clock cycles [9]. The comparator makes the decision on the negative edge of the clock, which gives extra half a clock cycle for data to settle at the input of the dynamic latch comparator. Since the final stage of the comparator is the dynamic latch the data will be ready almost instantaneously for use. A delayed pulse can be generated to acknowledge that data conversion is done.

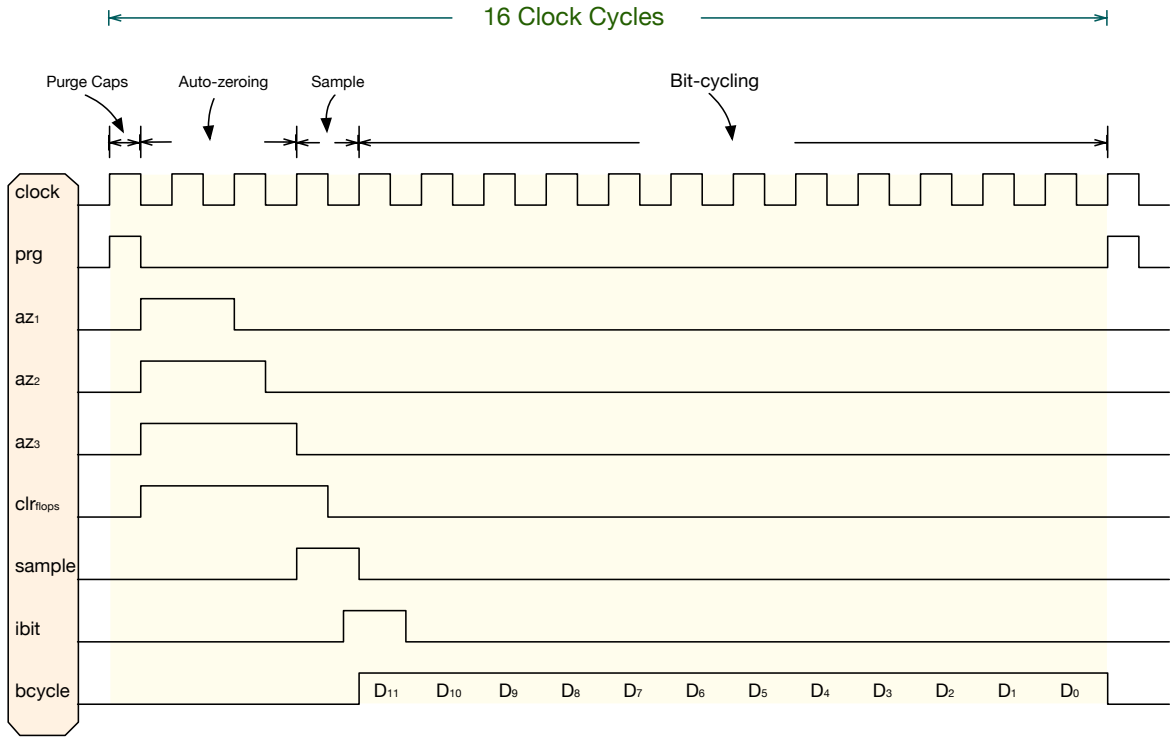
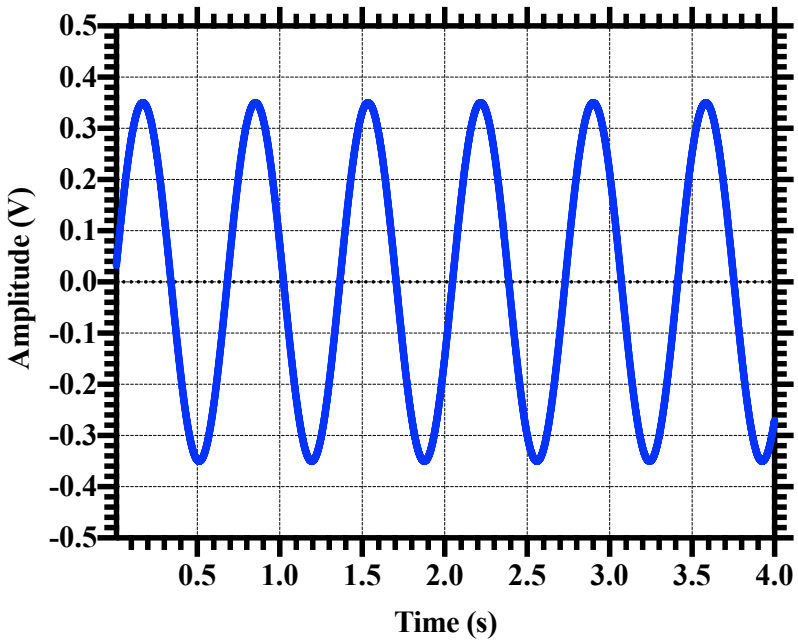
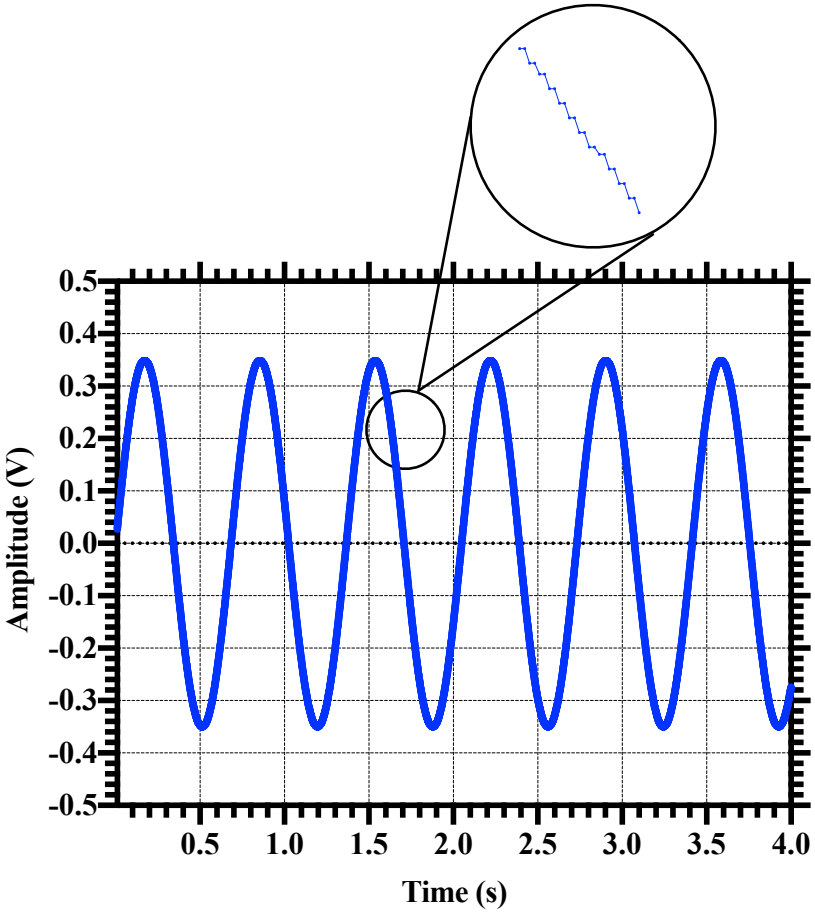


Figure 7.5 Timing of the SAR ADC.



(a)



(b)

Figure 7.6 (a) Input sine wave with an amplitude of 0.35V, 1.46484Hz frequency. (b) Simulated output of the SAR ADC.

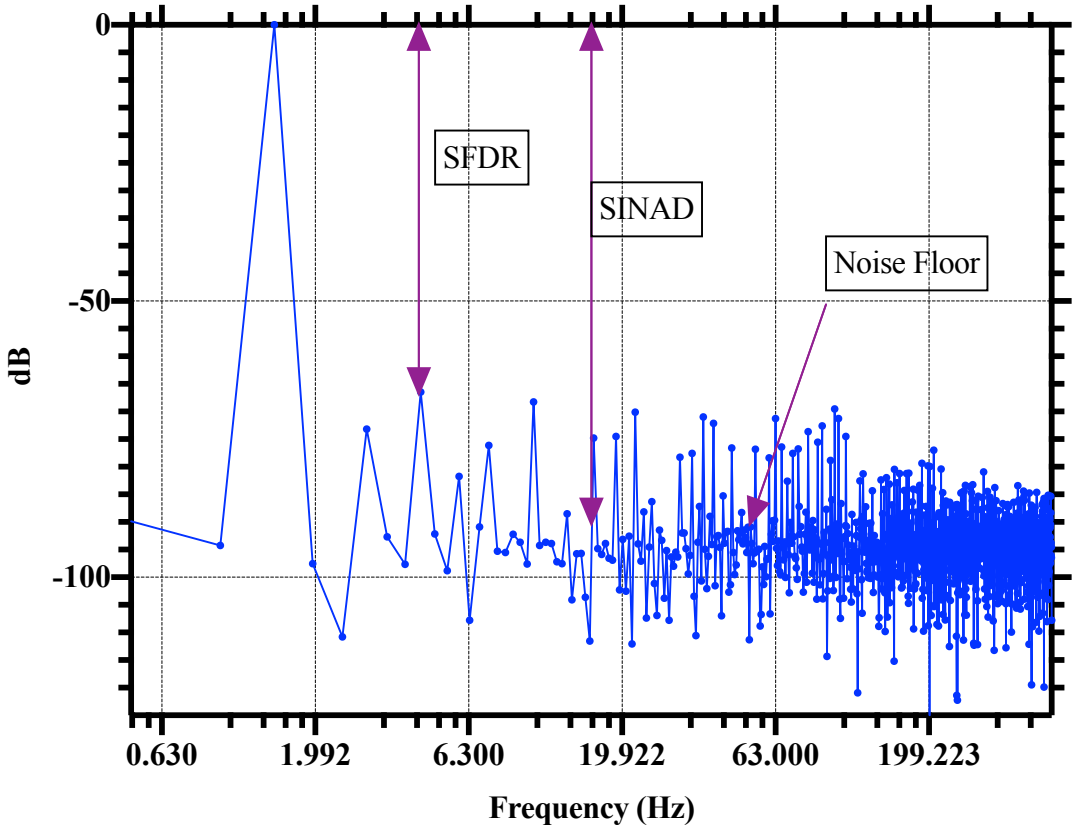
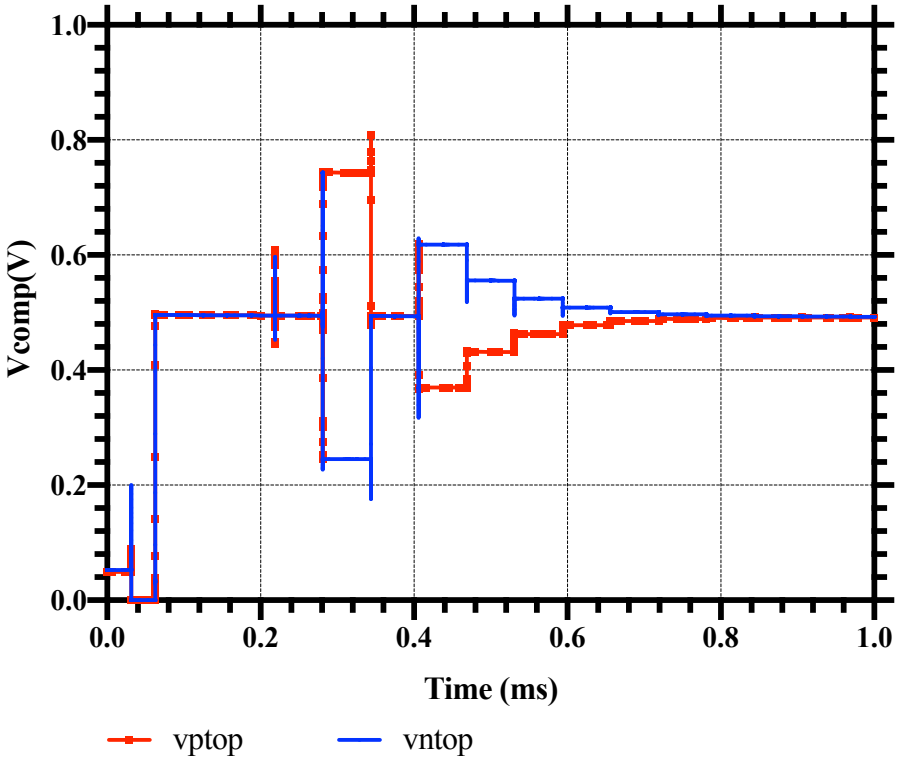


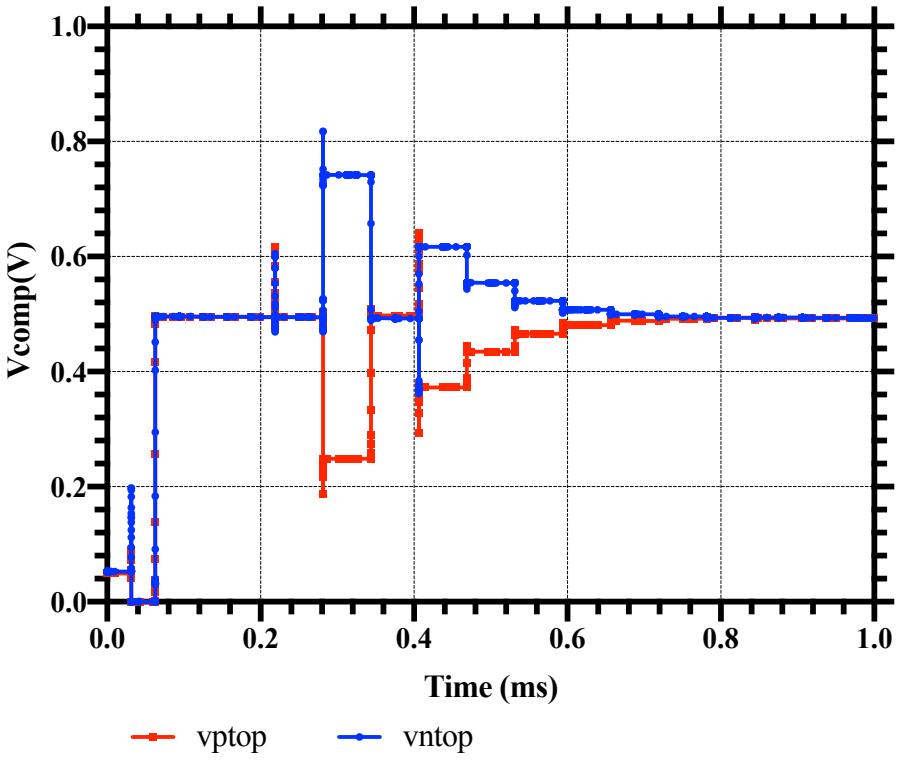
Figure 7.7 Simulated FFT of the ADC output when a sine wave is applied at the input.

A sine wave of 0.35V amplitude and the frequency of 1.46484Hz was supplied at the input, and the FFT was taken. The input and the output (converted using a Verilog-A DAC model), is given in Figure 7.6. The FFT spectrum is then given in Figure 7.7. The post-extracted simulated effective number of bits (ENOB) was 11.44bits, which was considered enough for this work.

Switches used throughout were simple NMOS switches with a half dummy switch [9]. Purge switches were similar to the one described in [9]. The common-mode level at the input of the comparator was 0.5V, and with a supply of 1V, the overdrive was not enough for the AZ/Sample switch (given in Figure 7.4). A bootstrapped switch similar to the one in [11], was hence used to increase the overdrive and reduce any distortion this switch may generate. This bootstrapped switch avoided any gate oxide stress, improved the switch charge injection and the linearity. The differential voltage at the input of the comparator for an input of ±500mV is shown in Figure 7.8.



(a)



(b)

Figure 7.8 (a) Simulated input signals for the comparator, when V_{in}= –500mV; (b) simulated input signals for the comparator, when V_{in} = 500mV.

The SAR logic provided the control signal for the bit cycling. Thus, it heavily relied on the correct timing to do the conversion. It also generated the digital output and stored it till D-type flip-flops were cleared. The SAR logic used here was the same as in [12].

For a high-resolution ADC, the performance of the comparator plays the most crucial part in the overall system realisation. The architecture of the implemented comparator is given in Figure 7.9. The system consists of three pre-amplifiers, offset storing capacitors, purging switches, and a double tail dynamic comparator. The output offset storage was used for cancelling the offset, for three reasons: 1) The OOS (output offset storage) usually has a smaller residual offset than the IOS (input offset storage); 2) The input capacitance of the IOS is generally higher than the OOS due to the kT/C noise and charge injection considerations; 3) The IOS requires significant gain of the comparator and a large capacitor to guarantee low offset voltage [13]. Since the OOS was connected in open loop configuration, the gain used was under 10 to avoid saturating the output. That is the reason why three comparators were used in multistage offset cancellation mode to attain the required gain.

The preamplifier used was a simple, fully differential amplifier with a local common-mode feedback using the resistors R_1 and R_2 (see Figure 7.9) [15]. A power down signal 'pd_n' was used to turn off the pre-amplifier during the sampling, hence helping to keep the power down. The gain achieved was between 5-10 across simulation corners. A capacitor purging switch was used to purge the auto-zeroing capacitors. The switch used was a simple n-type with a half-size dummy switch [9]. The final stage of the comparator was a double tail dynamic comparator [14].

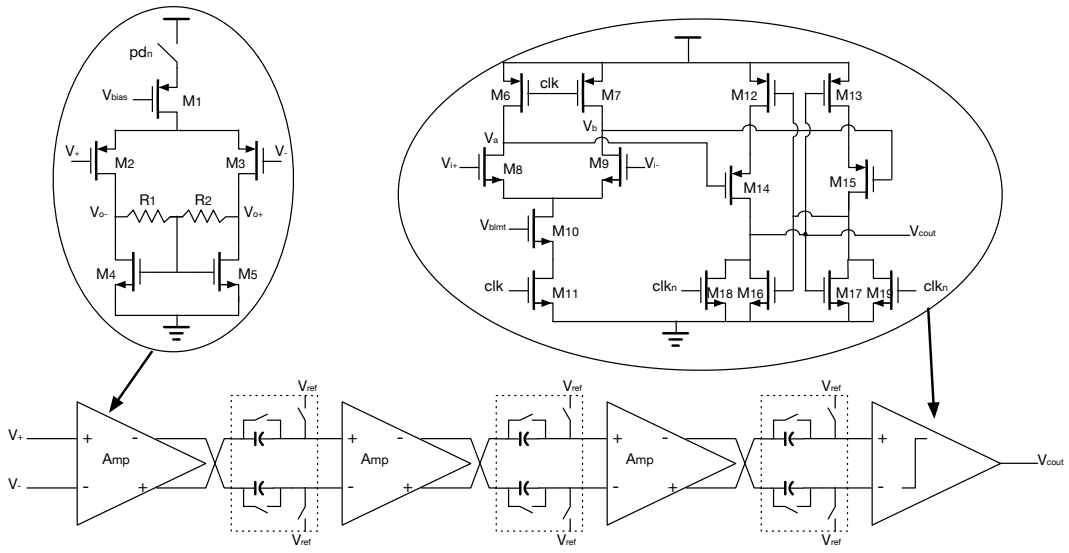


Figure 7.9 Architecture of the proposed comparator used in the SAR ADC.

In a dynamic comparator, there is a critical problem of charges coupling back to the input through capacitive coupling. This is due to the fact that there are considerable voltage variations on the regenerative nodes. This disturbance called *kickback* noise, can disturb the accuracy of the ADC if it is not fully settled and if not common mode. Use of a preamplifier avoids any kickback noise, from the dynamic latched comparator to reach the capacitive DAC, so it requires no special arrangement to cancel this kickback. A switch was added to the input stage of the double tail comparator, which restricted the current and hence helped reduce some of the residual offset drift due to the changing temperature [16]. During the regenerative phase, the switch M_{11} was closed and the transistors M_6 and M_7 were 'ON' and charged the outputs, V_a and V_b, to the supply voltage. Also, the switches M_{18} and M_{19} were closed, pulling down the two outputs to ground. At the start of the next clock edge (clk rising), the switch M_{11} starts to turn 'ON', causing current to flow, and pulling down the two nodes V_a and V_b. And depending upon the input voltage at the gates of M_8 and M_9, the falling edges of the two outputs have a small delay that will determine which of the transistors M_{14} and M_{15} will turn on first; and the positive feedback will then establish the correct output voltage (see Figure 7.10).

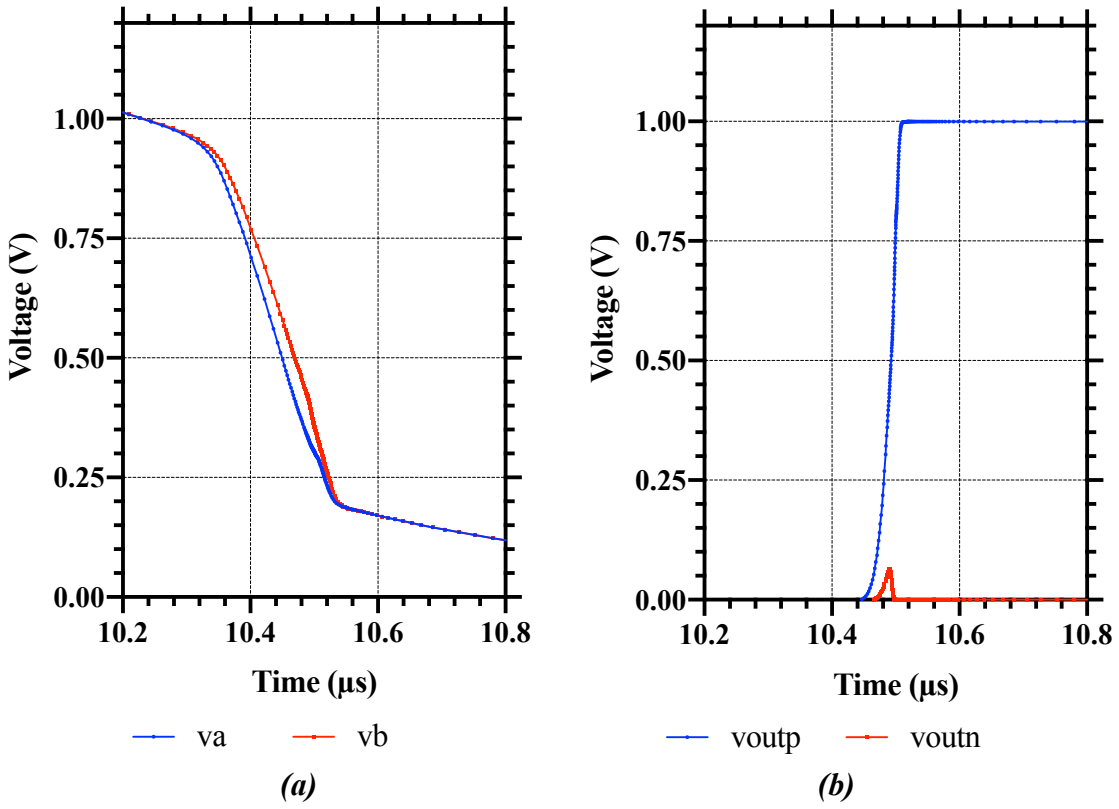


Figure 7.10 (a) Delay at the output of the first stage, while outputs are pulled down by the transistor M11. (b) Output of the latch stage once the M18 and M19 are turned OFF.

The layout of the final implementation is given in Figure 7.11. As can be seen from the layout, the majority of the area is occupied by high accuracy MIM (metal insulator metal) capacitors. The unit size used was 64μm^2, corresponding to a capacitance value of 127fF. Since the unit size is so small, even a tiny amount of coupling capacitance from nearby wiring can make a big difference in the accuracy of the 12-bit SAR ADC. Thus, extreme caution had to be exercised to avoid coupling between sensitive and high activity wires. A row of grounded dummy capacitors was used to avoid the etching effect.

The clock frequency used for the ADC was 16kHz. That provided a sampling frequency of 1kHz. Since the targeted EEG signals were in the range 0.5-50Hz, this corresponded to an oversampling factor of 20x. Such oversampling coupled with filtering in the digital domain can further improve the ENOB (from 11.44, which is reported here). A supply of 1V was used, which reduced the total power consumption for the ADC, and the overall EEG system. An auto-zeroed comparator was used to reduce the offset to be under 187μV.

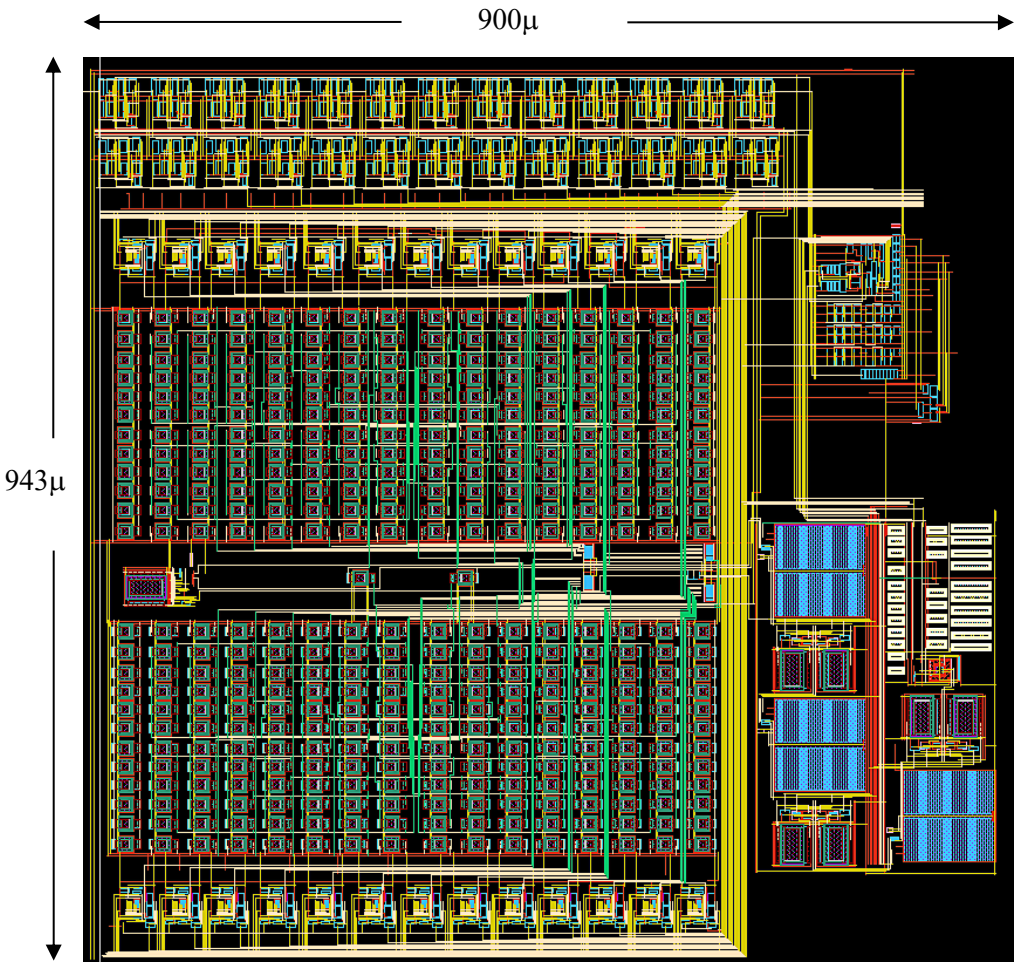


Figure 7.11 Layout of the 12-bit SAR ADC.

7.5 Proposed AFE Design

The final proposed architecture for the analogue front-end for the EEG system is given in Figure 7.12. The core sub-blocks were explained and carefully tested in previous chapters. The reason to pick the CCFEA-II over the CCFEA-I architecture was the ease of implementation and the robustness of duty-cycled resistors. These could easily be implemented and tailored to the final system by only modifying the delay block, and hence changing the duty cycle. Pseudoresistors, on the other hand, are very susceptible to leakage effects, and the presence of tie-down cells only add inaccuracy during post-layout simulations since these tie-down diodes are not appropriately modelled. Even with these issues, a pseudoresistor may offer a cost-effective and straightforward solution to applications where the drift of the high pass cut-off frequency can be tolerated. The calibration loop like the one proposed in Chapter 3 could also be implemented along with a digital processor. Nevertheless, the DCR based solution offered a much more accurate system, and the final accuracy of the pseudo-resistor calibration algorithm needs to be considered in the future work.

The gain of CCFEA-II was chosen to be 100 (40 dB), which is adequate for our purpose. 39.4dB final gain was achieved. 15*p*F MIM capacitors were used as input capacitors. The total area occupied by the CCFEA-II was 0.36mm^2, while the CCFEA-I was 0.59mm^2. 40% of the area was consumed by the input capacitors and the compensation capacitors for the core Gm-stage amplifier.

The system is capable of rejecting a DC offset of up to 50mV (see Chapter-3 for details), which is good enough for diagnostic applications where the DC offset can reach up to 15mV. The measured frequency response is given in Figure 7.13, which confirms the bandpass characteristic of the system. The integrated noise measured for the frequency band 0.5-50Hz was 0.82μV-rms for the CCFEA-II. When the filter was included, this figure increased to 0.87μV-rms (see Figure 7.14).

The amplifier area can be reduced further for the next iteration of the chip by reducing the size of the input capacitors. This approach's problem is that the input noise will increase, as the core amplifier noise would be elevated (see Chapter 3 for details). Furthermore, to keep the gain same, feedback capacitances need to be reduced as well. Preliminary design investigation suggests that the area can be reduced to 0.18mm^2, with the noise elevating to 1.25μV-rms (currently 0.87μV-rms).

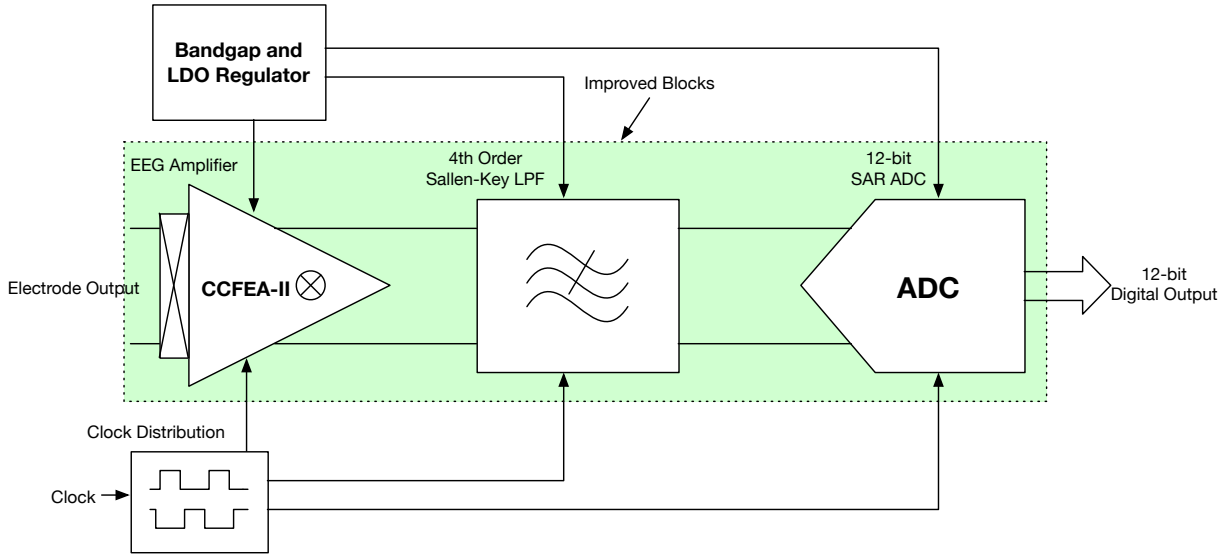


Figure 7.12 Proposed analogue sensor front-end for the EEG recording system.

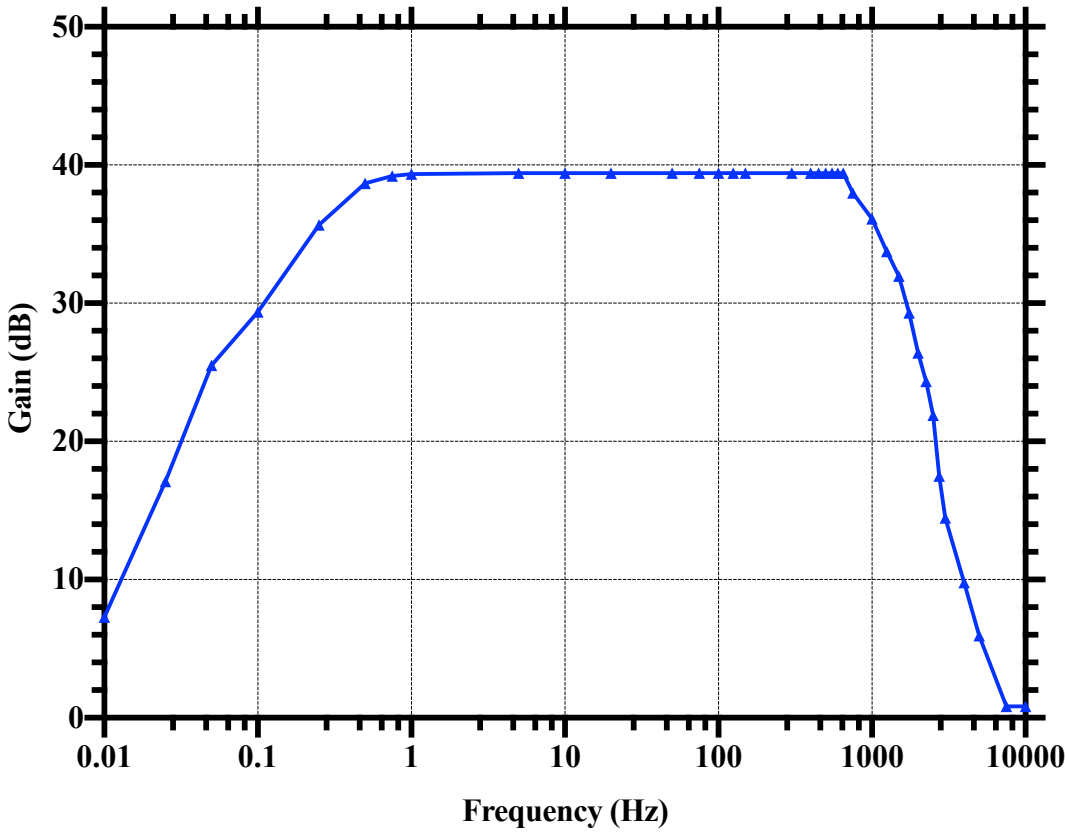


Figure 7.13 Measured frequency response for the final AFE (mainly decided by the response of CCFEA-II).

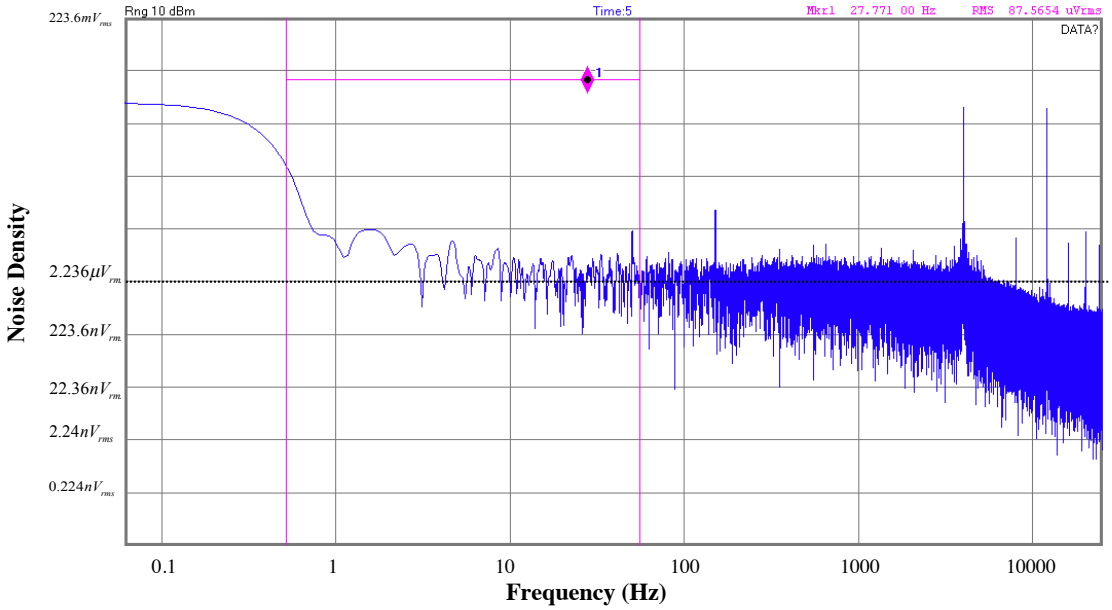
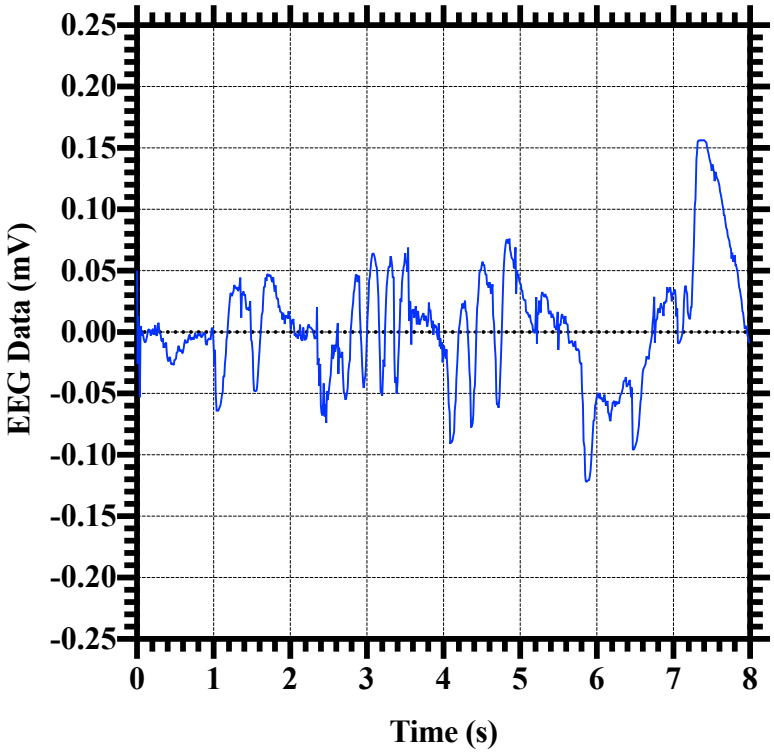


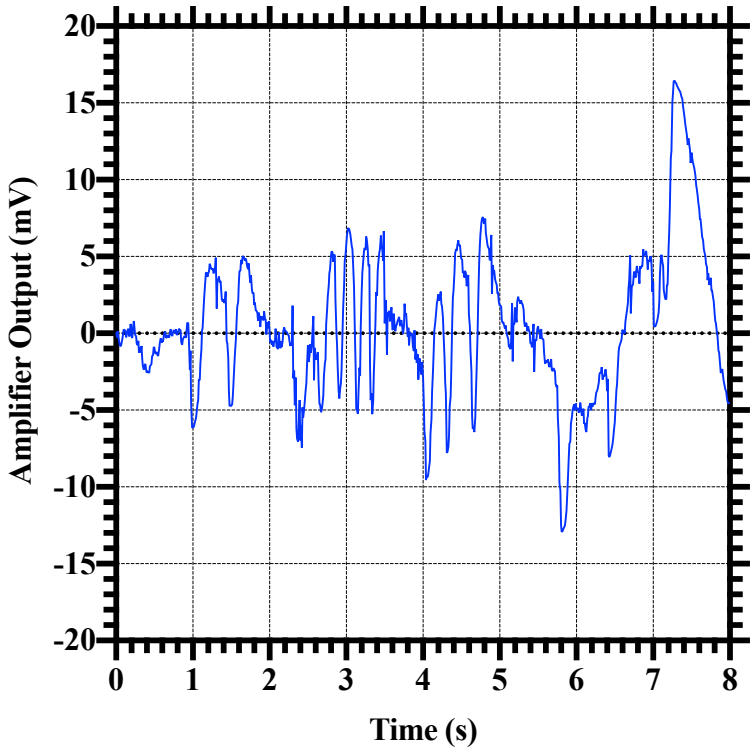
Figure 7.14 Measured noise performance of the AFE (dominated by the CCFEA-II and the SK-filter). 50 Ω impedance is used for the measurement.

A sample EEG record was used to test the system [17] (see Figure 7.15 and Figure 7.16). To suppress chopping ripples and other high frequency artefacts, a fourth-order SK low pass filter was used. The EEG record is individually applied to the circuit blocks in the AFE chain. The output is then taken out as a file and applied to the next circuit in the path. Due to separately using the EEG data, distortion was observed in the waveform, which was not visible in the post-layout simulation. To improve the data collection in the future, a PCB needs to be designed where the AFE can be configured to work as one unit, as the individual circuit's testing is no longer required. Since EEG signals are in the μV range, ADC with a resolution of more than 10-bit was required for the recording channel. Also, ADCs can have multiple static and dynamic errors that could mount to resolution loss (1-1.5 bit is ubiquitous for SAR ADCs). This is the reason why a 12-bit ADC was targeted for this research. Post-extracted simulation data suggested that the ADC could reach an ENOB of >11bits. Due, to the limited computational resource, only a 2048-points FFT was performed, for higher accuracy measurement, 32768-point FFT needs to be done for further evaluations of the ADC on the bench. The final implemented chip is given in Figure 7.17 and the corresponding bonding diagram is shown in Figure 7.18. During the course of the layout design, extreme caution was exercised to isolate the digital and the analogue signal, by keeping them in separate sides of the chip. Also, the pad-ring was isolated using a back-to-back diode arrangement. The majority of the empty area was

filled with decoupling capacitors. Also, all sensitive analogue signals were shielded appropriately.

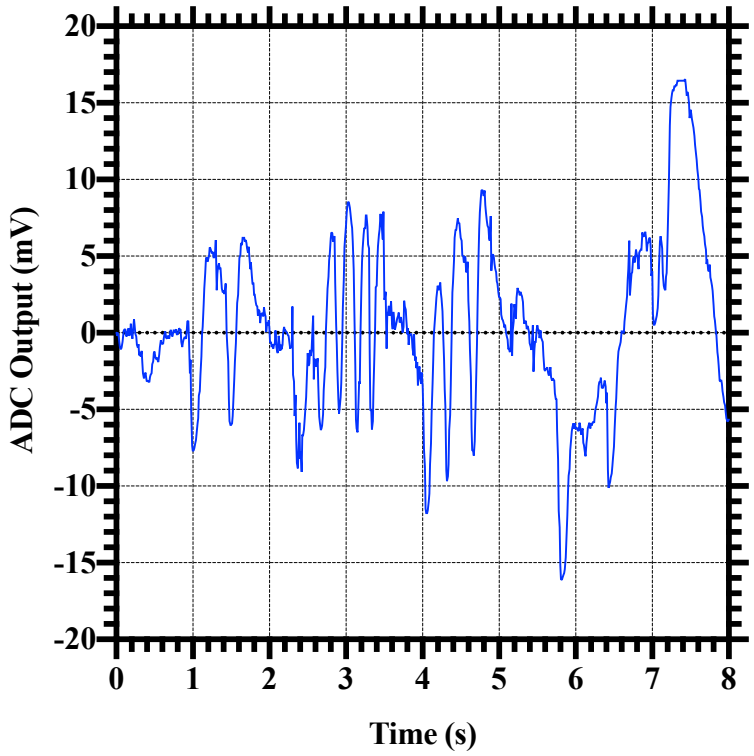


(a)

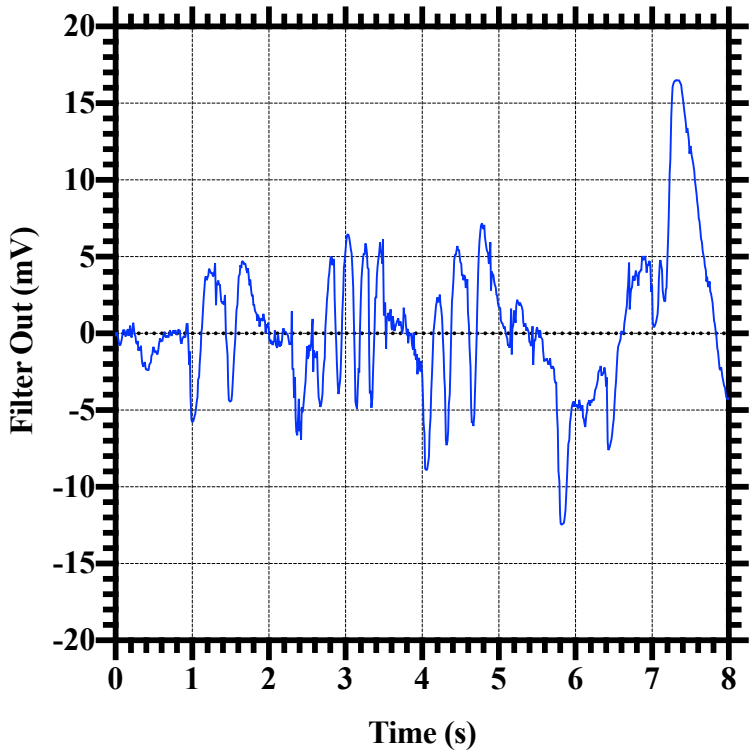


(b)

Figure 7.15 (a) Input EEG data , (b) amplified EEG data at the output of the CCFEA-II.



(a)



(b)

Figure 7.16 (a) Output from the fourth order Sallen-key filter, (b) converted output of the SARADC.

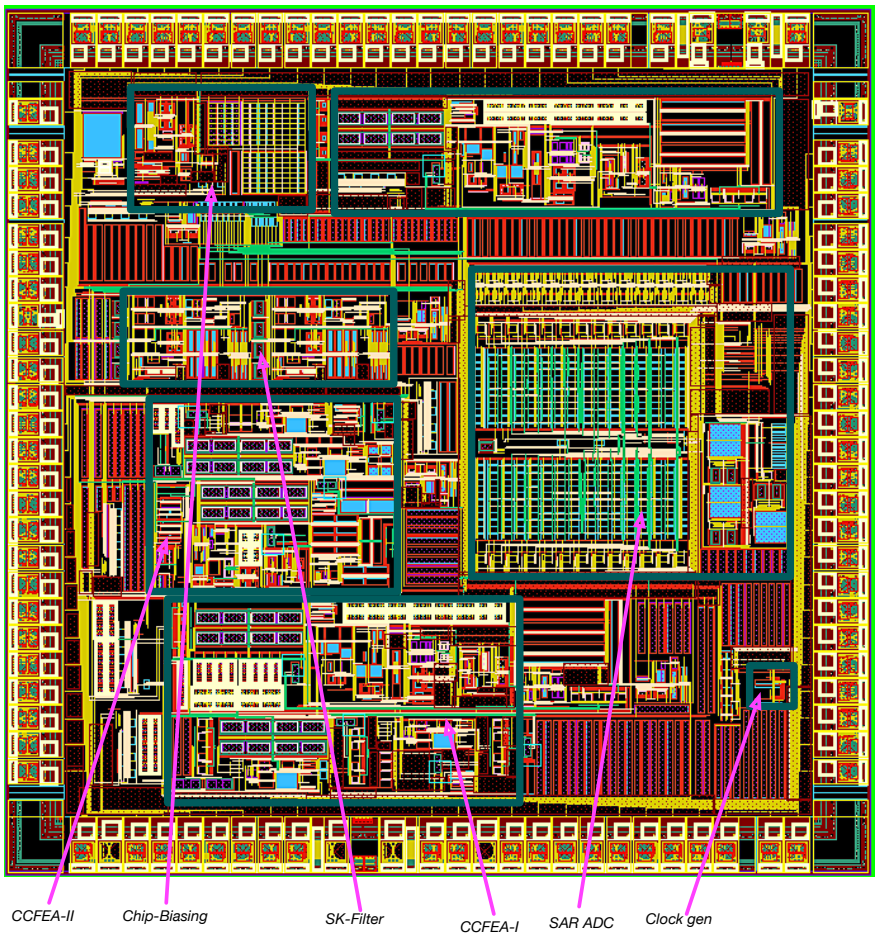


Figure 7.17 Top-level layout of the fabricated chip.

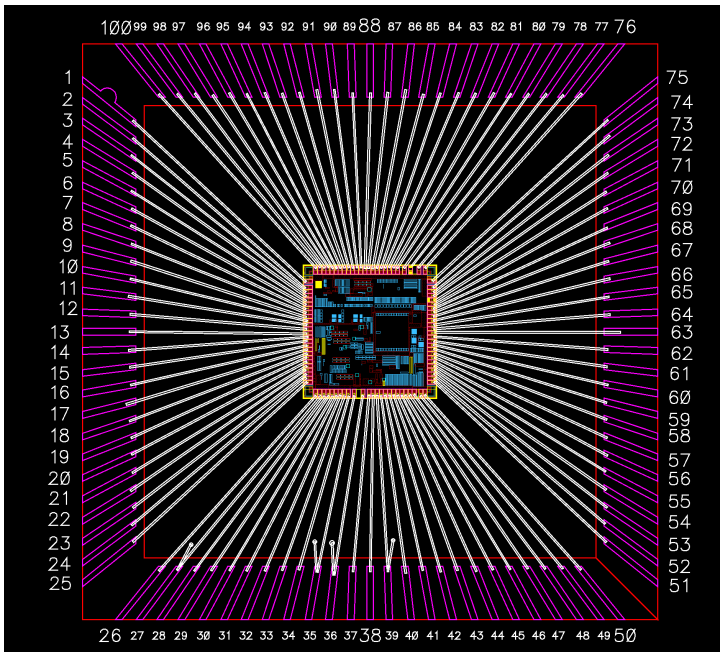


Figure 7.18 Wire bonding arrangement for the full-chip.

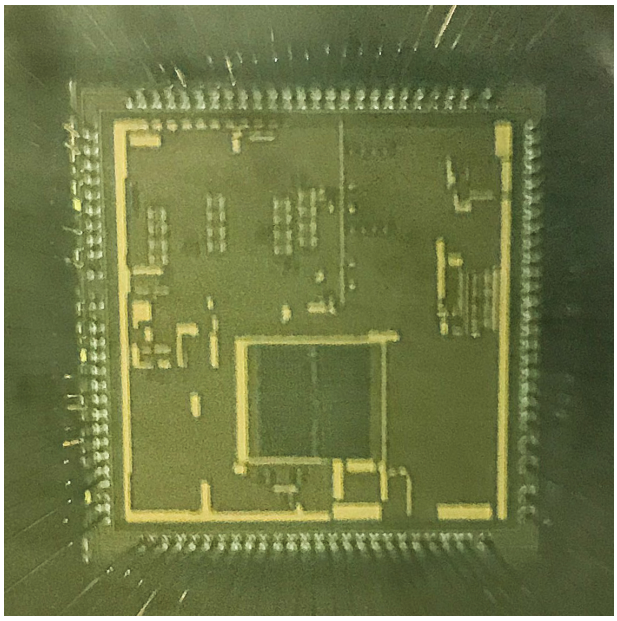


Figure 7.19 Microphotograph of the final wire-bonded chip.

Table 7.1 Performance comparison of the proposed AFE with state-of-art designs

Parameters	**[21]**	**[22]**	**[23]**	**[24]**	**[25]**	**Proposed AFE**
Supply	0.5V	1.5	1.2V	1.8V	1	1
Input Impedance	28MΩ	31MΩ	High	1.2GΩ	102GΩ @1Hz	100MΩ
Input Referred Noise	1.25μV_{rms} (1Hz ~ 500Hz)	1μV_{rms}(0.25Hz - 250Hz)	4.2μV_{rms} (0.5Hz-100Hz)	1.75μ V_{rms} (0.5Hz-100Hz)	1.5μV_{rms}(0.5 Hz-1.2kHz)	0.87μV_{rms}
Noise Cancellation Technique	Chopping	Chopping	No dynamic cancellation	Chopping	No dynamic cancellation	Chopping
DC Offset	±50mV	±30mV	Rail-to-Rail	±250mV	Rail-to-Rail	±50mV
CMRR	88dB	97dB	59.8dB	84dB	108dB	131.62dB
Power Consumption /per channel	2.3 μW	5.5 μW	9.4 μW	>11.1μW	3.7 μW	3.2μW
ADC ENOB	15	9.4	9.2	12	4,6,8,10	11.44

Finally, the performance comparison of the proposed AFE with state-of-art designs is presented in Table 7.1.

7.7 Conclusion

This chapter discussed the auxiliary circuits used on the AFE, including the non-overlapping clock generator, a 12-bit fully differential SAR ADC, and the current reference. A NOR gate based non-overlapping clock generator was then explained, along with a brief explanation on the difference with the traditional topology. The chapter then went on to explain the current reference used for biasing circuits on the chip. A 12-bit fully-differential SAR ADC was later described, along with a discussion on crucial modifications in the comparator for reducing the offset. Furthermore, the proposed AFE is explained, along with measurement results from the final fabricated chip. The AFE achieved a total integrated input-referred noise of 0.87μV-rms in the frequency band of 0.5-50Hz, which met the target specifications.

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Chapter 8 - Conclusion and Future Work

8.1 Conclusion

This thesis proposed a novel ultra-low-power frontend for wearable EEG systems. The circuits were fabricated on AMS 0.18μm six metal layer technology. The circuit design, layout and performance analysis (pre-fabrication) were done on the Cadence suite of tools. Multiple circuits were designed, including a chopped capacitive feedback amplifier with a novel pseudo-resistor (CCFEA-I), chopped capacitive feedback amplifier with a duty-cycled resistor to control the high pass frequency (CCFEA-II), chopped capacitive feedback amplifier with pseudoresistor calibration and digital offset correction (CCFEA-III) , ultra-low power bandgap reference, low dropout regulator and differential difference amplifier (DDA) based fourth-order Sallen-Key low pass filter. Their analyses, design, implementation, and test results were presented in this thesis. The fabricated chip also had a 12-bit fully differential SAR ADC with an improved auto-zeroing based comparator.

This thesis also provided a brief comparative analysis of multiple pseudo-resistors available in the literature. Their performance was compared along with a discussion on advantages and disadvantages. Two new low distortion pseudo-resistor designs were also proposed. These novel pseudoresistors used symmetrical arrangement to avoid signal-dependent output shift. The proposed PRs achieved a bandwidth of 160Hz and 236Hz respectively, compared to the highest of 54Hz achieved for state-art-implementations designed for EEG application. These PRs also achieved a total harmonic distortion of 3.73% and 4.2% respectively, compared to 7.5% of the nearest state-of-the-art implementation for EEG amplifier. Furthermore, these PRs showed increased input voltage range for which they can retain high incremental resistance.

The pseudo-resistor values, in general, varies from 1000% - 2000%. To mitigate the problem of large resistor variability, the thesis also proposed a novel scheme to calibrate the resistance value of the pseudo-resistor that could reduce this variation to under 8.25%.

The thesis also implemented a novel architecture of a fully-differential amplifier with chopping modulation and an improved frequency performance common-mode feedback circuit. The circuit achieved a large CMRR (above 120dB) without an external CMRR improvement loop or driven right leg circuit. The circuit achieved input-referred noise of 0.395μV in the frequency band of 0.5-50Hz while consuming only 1.2μA of supply current.

A fourth order DDA based Sallen-Key low pass filter design was also proposed, using a duty-cycled resistor to reduce the size of passive resistors. The area occupied by this low pass filter was $0.21mm^2$ for a cut-off bandwidth of 520Hz. And the total power consumption of the SK-LPF was just $415nW$ with a 1V supply.

Finally, a 12-bit fully differential SAR ADC design is proposed with discussion about how to increase the accuracy of the ADC. A brief discussion was presented on critical contributors to the static and dynamic errors, and the reasoning behind using a 12-bit ADC for the EEG recording systems. A current mirror was added in the comparator design to reduce the offset of the pre-amplifier and the temperature drift of the comparator offset. The ADC achieved an ENOB of 11.44 (in post-layout simulation) doing a 2048-point FFT. The average power consumption of the ADC was 190nW at 500S/s.

8.2 Future Work

The subsequent phase in this research would be to thoroughly test the pseudo-resistor calibration loop under multiple temperatures and process stepping. The proposed calibration loop can reduce the pseudo-resistor variation and enhance its usability in high accuracy neural recording. Single-chip testing was not considered enough to see the impact of process variation.

Also, additional work needs to be performed to reduce the area of CCFEA-II and implement it along with electrodes for live EEG recording. There is a potential to reduce the size into the half with a noise penalty of just under 30%, but this needs Silicon implementation and validation to prove its viability. Also, the DC offset rejection can be improved over 50mV to enhance this architecture's suitability for dry electrode and neural stimulation application.

There is still some potential to reduce the noise of the Sallen-Key low pass filter. Notably, the flicker noise of the input pairs of the amplifier. Furthermore, the DCR can be replaced with a multi-rate duty cycle resistor to implement the sub-Hz low pass filter. Further design analysis

and tests could be done to prove its viability along with competitiveness with already existing designs in the literature.

A future implementation could also benefit from a digital processing circuitry on the same ASIC, to program the current requirements for different amplifiers (and the rest of the circuitry used in the AFE) dynamically so that the noise level and the performance of the AFE can be set as application-specific.

The power of the SAR ADC could be reduced further by using multiple power domains. The digital processing can be performed with near-threshold logic cells, which will still meet the speed requirement of EEG recording systems. Currently, no circuit is added to correct for the gain error of the ADC. So, a calibration circuitry could be further added in future implementations.

Appendix A - Discussion on the PCB design and the test setup

AMS 0.18um technology was used to fabricate the chip through Europractice. The dimension of the chip was 2600µm x 2600µm with a total die area of 7mm^2. The actual area available for designing various test circuits (excluding the pad ring and other ESD structures) was 2236µm x 2236µm (5mm^2). The PCB for testing was designed and laid out using Altium. A low insertion force socket from Selwyn electronics was used to mount the BGA package of the chip onto the PCB. This also helped with the reusability of the PCB for testing further chips, and also avoided making the PCB redundant in case some mistake happened during the testing or a faulty chip package was mistakenly used. The final fabricated PCB (excluding assembly components) is given in Figure A.1. The top and bottom routing layers of the PCB board is given in Figure A.2.

A two-layer PCB routing scheme was employed for the PCB connectivity. Wires were carefully routed to reduce stray capacitances and ground-bounce. Wherever possible, the tracks were used to be the lowest length achievable. Also, matched pairs were routed together to avoid causing a differential signal between them due to routing or coupling with a nearby signal. Multiple decoupling capacitors were used across the board for the power supply, to reduce the supply interference and the ground bounce. Also, the return path for critical signals was kept close to it, to avoid increasing the parasitic inductance and exacerbating the ground-bounce further.

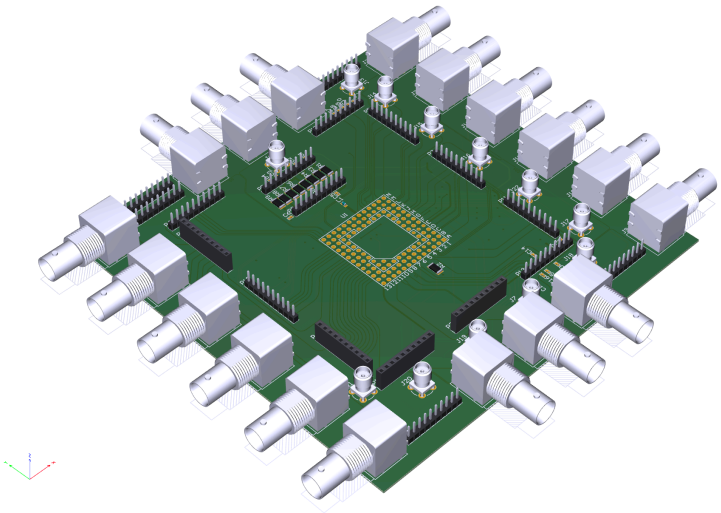
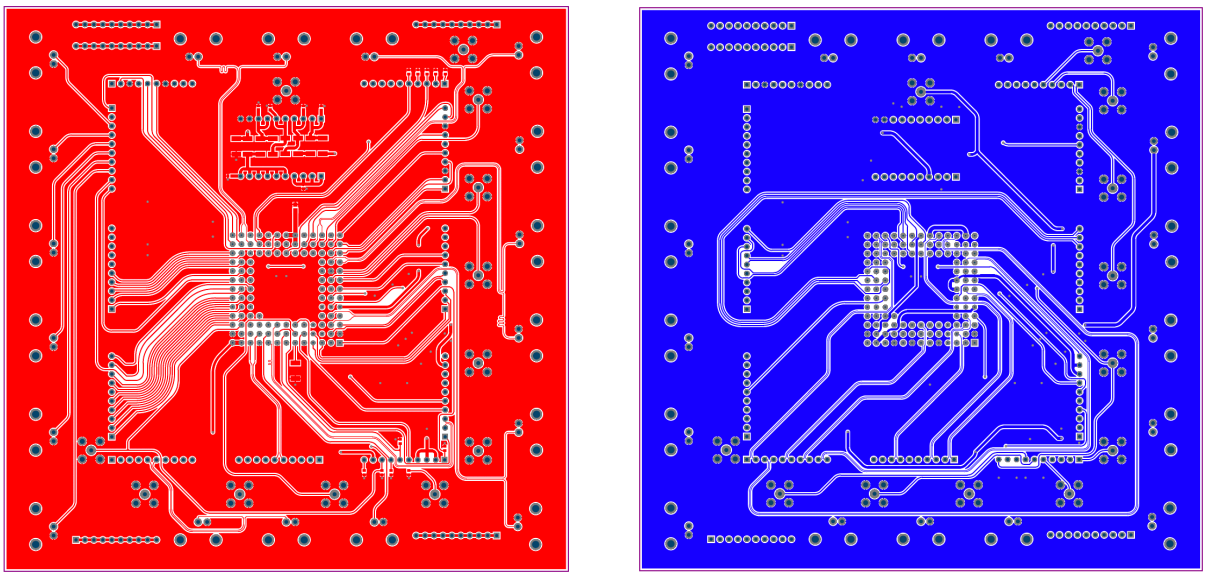


Figure A.1 Final fabricated PCB board.



(a) *(b)*

Figure A.2 (a) Top layer of the PCB, (b) Bottom layer of the PCB.

The test setup for measuring the circuit noise and reviewing the frequency spectrum is given in Figure A.3. An Agilent signal analyser (N9020A) was used for recording the noise power spectral density (PSD). For the final measurement, a resistive divider was used to generate a 1V supply from a 1.8V battery and was used as a supply to the amplifier. Due to the superior supply noise rejection of the amplifier and the fully differential structure, these two measurements were within 5% tolerance. The chip package housed on the socket is given in Figure A.4(*a*). The test setup for testing functionality is given in Figure A.4(*b*). The output was observed on a mixed signal oscilloscope (Agilent Technologies MSO-X 3054A). Various configuration signals were set up using the Agilent 33522A signal generator. A Keithley 2602A power supply was used to provide the external power supply when the battery was not required.

A custom faraday cage/shield was used during noise measurement to block the electromagnetic radiations reaching the noise-sensitive amplifier. A cardboard box was covered entirely with an aluminium foil. The idea of using a conductive metal surface like aluminium foil was to let signals flow through it and not across it. This shielded the design under test inside the box. Not much improvement was observed during noise measurements with the Faraday shield.

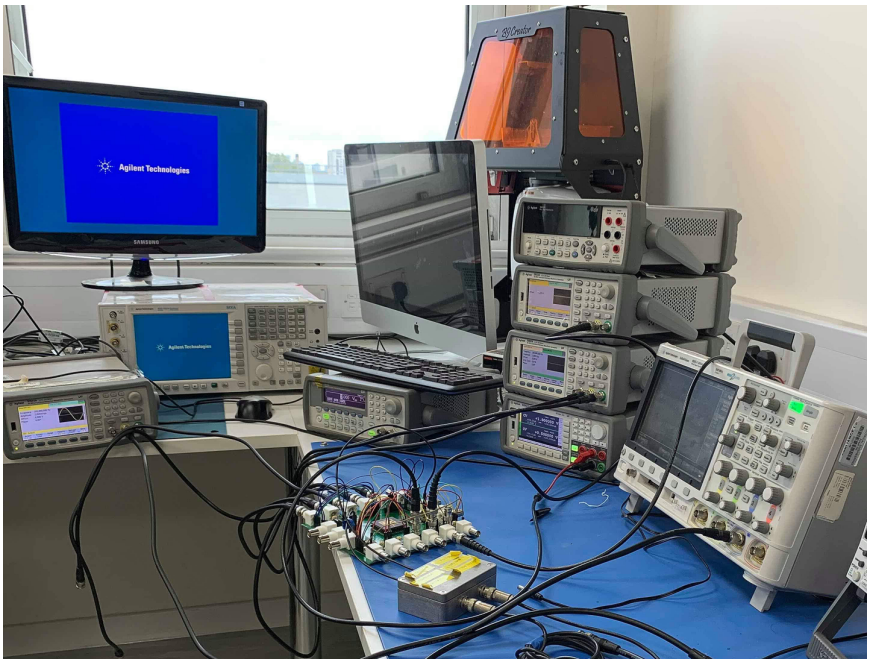
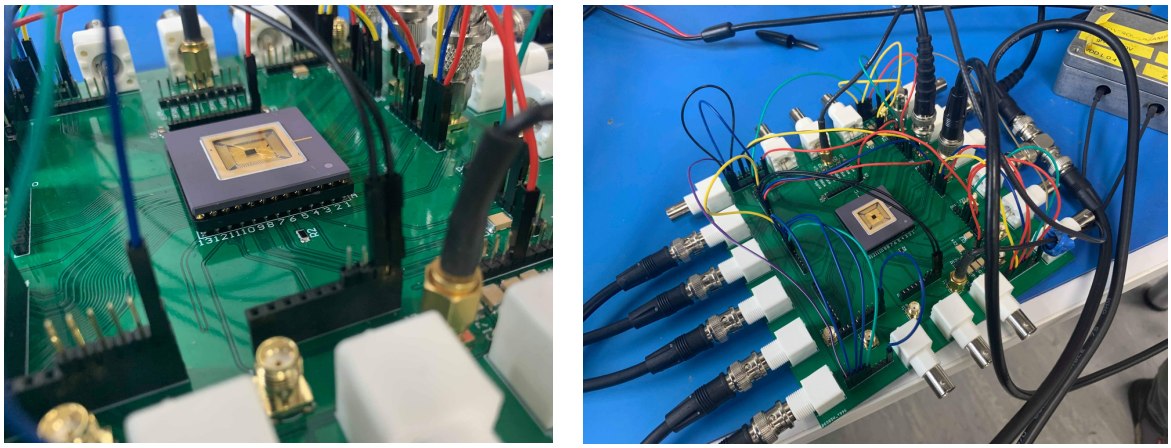


Figure A.3 Test setup for noise measurement using Signal Analyser (Agilent MXA-N9020A).



(a) *(b)*

Figure A.4 (a) Fabricated chip -connected to the PCB via a socket, (b) Test setup for the functionality measurements.