A single-phase synchronization technique for grid-connected energy storage system under faulty grid conditions

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***Abstract* -- The control of single-phase grid-connected Energy Storage System (ESS) requires a very fast and accurate estimation of grid voltage frequency and phase angle. A Phase-locked Loop (PLL) based synchronization algorithm usually extracts this information. The operation and control of entire system is directly affected by the performance of PLL. In this paper, a novel Advanced Single-phase PLL (ASφPLL) technique with reduced complexity is proposed for the fast and accurate extraction of grid information in a ESS under distorted and abnormal grid conditions including harmonics, interharmonics, DC-offset and grid faults. The proposed method provides a faster dynamic response, lower frequency overshoot, and accurate estimation under off-nominal grid frequencies with reduced computational complexity in comparison to the existing method. The advanced performance of the proposed ASφPLL is verified through simulation and experimental results.**

***Index Terms*—Power quality, Phase-locked loop, current controller, harmonics, DC-offset, Energy Storage System.**

I. INTRODUCTION

The increasing integration of single-phase grid-connected energy storage systems (including electric vehicles and renewable systems) give rise to various new grid codes and regulations to obtain high quality output power. The grid codes [1, 2], for example, include maintaining the frequency and voltage limits, providing necessary Fault Ride Through (FRT) support and injecting high quality power in the event of grid voltage disturbances such as faults, harmonics, interharmonics, frequency and phase variations etc. This is necessary in order to regulate more efficiently as well as to diversify the role and contribution of renewable energy and electric vehicular system on electrical grids [3, 4]. The key element for the efficient and reliable integration of such systems to the grid is the power electronic based Grid Side Converter (GSC) [5, 6]. Consequently, the proper design of GSC controller plays a vital role for the overall operation of grid connected stationary and mobile storage systems, and thus, it should be enhanced and diversified to meet the modern grid requirements.

A typical block diagram for a single-phase grid-connected system is shown in Fig. 1 where electric vehicle and/or renewable energy is connected to GSC through DC bus. The GSC controller comprises of two sub-controllers and a synchronization unit. The sub-controllers include an active/reactive *(PQ)* controller to generate the reference currents based on the desired *P* and *Q,* and a current controller to ensure the accurate injection of these currents into the grid. The synchronization unit, known as the heart of control system, is responsible for extracting the grid voltage information (that is, frequency, phase and amplitude) required for synchronization and control purposes (especially in *dq*-synchronous domain). The widely used synchronization method is the Phase-Locked Loop (PLL) algorithm [5, 7, 8]. Since the operation of both *PQ* and current controller is directly affected by the performance of synchronization unit, the accurate operation of GSC is heavily dependent on the proper design of PLL. In addition to accurate performance, the complexity of PLL is also very important as in real-time the embedded microcontrollers (having limited available processing resources) are used to develop the GSC control system [5, 9]. If the complexity is relatively high, these micro-controllers cannot be operated in real-time at a given sampling rate. It is, therefore, necessary to design such control units with the least computational burden [10]. Thus, in this paper, a novel less complex synchronization technique has been proposed for the accurate extraction of grid information under distorted and abnormal grid conditions.

Several single-phase PLLs exist in the literature but with certain pros and cons. A common approach used for the development of single-phase PLLs is to generate the in-quadrature voltage vector $(\mathbf{v}_{\alpha\beta})$ using the grid voltage (v_g). The voltage vector is then transformed to the dq^{+1} rotating reference frame $(\mathbf{v}_{dq}^{+1})$ and the resulting v_q^{+1} is provided to the Phase Detector (PD) part of the PLL to extract the grid voltage phase angle (θ_g). In this way, the Quadrature Signal Generator (QSG) and the rest of processing contribute to the overall design of a single-phase PLL. The simplest single-phase PLL is the T/4 Delay technique [12], in which, the quadrature signal is generated by delaying the grid voltage with a factor of T/4 (where, T is the grid's fundamental period). This technique, however, suffers from inaccuracies under grid voltage harmonics, interharmonics and DC-offset. The Inverse Part Transformation (IPT) PLL [13, 14] uses back-to-back connection of stationary and rotating reference frame transformations and Low Pass Filters (LPF) to generate the in-phase and quadrature signals. This configuration forms a second-order band pass filter and attenuate the higher order harmonics. However, the low order harmonics/interharmonics are not compensated and also the filtering capability for higher order harmonics is not significant. Interesting synchronization methods, including the Second Order Generalized Integrator (SOGI) based PLL and Frequency-Locked Loop (SOGI-FLL),

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and adaptive filter based Enhanced PLL (EPLL) with performance similar to the IPTPLL are discussed in [5, 12-17]. SOGIPLL and SOGIFLL provides immunity against harmonics (high order only) due to low/band pass filtering characteristics and fast dynamics under grid faults, however, low order harmonics cannot be adequately removed [13]. The EPLL according to [14] presents poor immunity against high as well as low harmonics and suffers from slow dynamics compared to SOGIPLL.

A Hilbert transform based PLL [18] achieves accurate phase angle estimation under grid voltage harmonics. However, applying it practically on time dependent signals imposes implementation problems. The authors in [19] proposed two PLL techniques named as the Enhanced Transfer Delay PLL (ETDPLL) and Non-frequency dependent Transfer Delay PLL (NTD-PLL). The two PLLs use small signal model-based transport delay and input gains for the compensator and improve the synchronization response. However, as discussed in [19], they still lack in complete elimination of oscillations caused by harmonics. The inaccurate response of the PLL under harmonics affect the power quality of grid-connected converter because the operation of GSC controller (including the reference frame transformations) is heavily dependent on the synchronization algorithm.

For immunity against harmonics, several techniques have been suggested, including the multi-resonant and repetitive controllers [20], in-loop Moving Average Filters (MAF) [21] [22] and adaptive or notch filters [23], [24]. The compensation of harmonics is achieved using these methods, however, degrade the dynamic response of the PLL as discussed in [5], [25] for the MAF based PLLs. Recently the dynamic response of MAF based PLL has been improved in [26, 27] with proposing to move the MAF outside of control loop and incorporate it in the pre-filtering stage, along with necessary improvements to the phase error under off-nominal grid frequency. Even though the dynamic response is improved compared to conventional in-loop MAF, the improvement seems inconsequential when compared to non-MAF PLLs.

It is important that the synchronization technique possess DC-offset rejection capability as the presence of DC in the grid voltage appears as low frequency oscillations in the frequency and phase error estimation. The method proposed in [28] uses tuning procedure to adjust the bandwidth of synchronization technique for the compensation of DC-offset, however, it suffers from slow dynamic response. The integration based technique for the mitigation of DC-offset is presented in [29]. In addition to complex implementation, this method also suffers from degraded dynamic response.

A LPF is added in a QSG based SOGI-PLL in [30] results in the rejection DC-offset but only from quadrature component. The author in [31] rearranged the structure presented in [30] with addition of some mathematical operations in order to fully remove the DC-offset from β-component, however the technique proposed does not work for higher order harmonics. In order to remove the drawbacks of [30] [31] the authors in [16] proposed a cascaded SOGI-PLL, which results in complete elimination of DC-offset from orthogonal signals. In [32], in addition to DC-offset rejection the authors tuned a set of QSG based SOGI for selective harmonic elimination. The new combination removes predefined harmonics in addition to DC-offset but at the same time design's complexity is increased. The author proposed an all pass filter based SOGI-PLL in [33] which removes DC-offset and also worked for frequency and fault variations with low complexity. However, in case of harmonic elimination, the total harmonic distortion is more than the provided maximum limit for grid connected systems.

A PLL technique has been proposed in [34], [35] for the compensation of selected low-order harmonics using Multi-Harmonic Decoupling Cells (MHDC). The estimated quantities by MHDCPLL are subject to oscillations under off nominal grid frequency and presents high frequency overshoot in the event of faults. Moreover, it requires large number of Park transformations, which in turn increases the computational complexity. There are other limitations such as requiring prior knowledge of individual harmonic to be compensated (as it is tuned to specific harmonics) and lack of accuracy in the compensation of interharmonics (especially the ones close to the fundamental frequency).

To address the aforementioned limitations of existing PLL techniques, a novel Advanced Single-phase PLL (ASφPLL) is proposed in this paper. The proposed ASφPLL compensates for grid voltage harmonics, interharmonics, DC-offset and faults with accuracy and fast dynamic response. It is also immune to off-nominal frequency oscillations and presents lower frequency overshoot. Most importantly, the proposed PLL algorithm is less complex and does not require prior knowledge of which harmonics to be compensated. Therefore, the proposed ASφPLL is the most suitable candidate for grid-connected energy storage systems allowing bi-directional flow of high-quality power under distorted and faulty grid conditions.

The rest of the paper is structured as follows: The design of proposed and existing PLLs is presented in section II followed by the tuning of the PLLs in section III. computational complexity analysis carried out in section IV. The validation of proposed technique with simulation and experimental results are outlined in section V. After validating the frequency and phase estimation of proposed PLL for several grid disturbances, Section VI demonstrates the impact of proposed synchronization technique on the overall operation of grid-connected system. The paper concludes in Section VII.

II. THE PROPOSED AND EXISTING PLLS

This section presents in detail the structure of proposed PLL, its schematic diagram, design methodology and mathematical analysis. In addition, short description of SOGIPLL and MHDCPLL along with their diagrams are also added as they will be used in the later section for comparison.

A. The Proposed Advanced Single-Phase PLL (ASφPLL)

The proposed PLL is designed in the *dq*- rotating reference frame and a combination of various blocks, including the QSG,

the DC-offset and Harmonic-Interharmonic (DHIH) compensation module, and the adaptive PD. The QSG is used to generate the in-quadrature voltage vector $\mathbf{v}_{\alpha\beta}$ and is adaptive to frequency variations. The DHIH is to cancel out the effect of DC-offset and harmonics/interhamronics present in the grid voltage, resulting in oscillations free dq^{+1} voltage vector. Subsequently, the q^{+1}-component is processed by the phase detector to estimate the phase (θ_g') and frequency (f_g') of grid voltage.

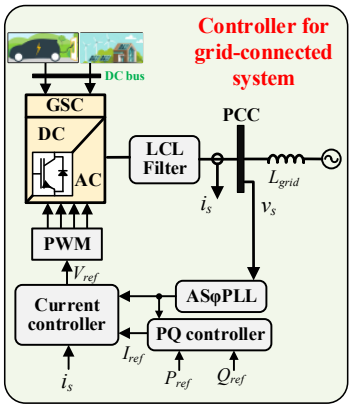

Fig. 1: Control diagram for grid connected system.

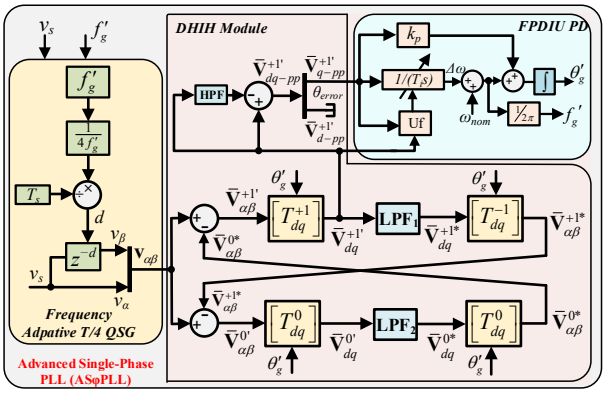

Fig. 2: The block diagram of the proposed ASφPLL.

1. Quadrature Signal Generator (QSG)

The QSG is formed by the frequency adaptive implementation of T/4 delay transportation to generate the in-quadrature voltage vector $\mathbf{v}_{\alpha\beta}$, where T represents the fundamental period of the grid voltage. In this method, the in-phase component (i.e. v_α) is obtained by passing the input grid voltage v_g with a unity gain, whereas the quadrature component (v_β) is generated by quarterly delaying the input voltage, as shown in Fig. 2 and mathematically represented in (1).

$$\mathbf{v}_{\alpha\beta} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v_s \\ v_s z^{-d} \end{bmatrix} \tag{1}$$

The frequency adaptation is achieved by providing the estimated grid frequency as a feedback to QSG to generate the required transportation delay (d) of quarter period, resulting in the quadrature component. The d required for implementation of frequency adaptive T/4 is calculated using (2), where T_s is the sampling rate of GSC controller, as depicted in the Fig. 2.

$$d = \left(\frac{T}{4}\right) T_s = \left(\frac{1}{4f_g'}\right) \div T_s \tag{2}$$

The QSG may results in inaccuracies for the case when d is a non-integer. For such a case, the d is divided into two parts, integer and fractional order delay. The integer part can be directly used by the controller, while the other part is solved using Lagrange Interpolation [36].

2. DC-Offset and Harmonic-Interharmonic (DHIH) Compensation Module

The main objective of this paper is to enable a less complex, fast and accurate estimation of grid voltage phase and frequency under grid voltage DC-offset and harmonics/interharmonics. The single-phase grid voltage v_g consisting of fundamental component (v^1), DC-offset (v^0), harmonics (Σv^h) and interharmonics (Σv^{ih}) is expressed as:

$$v_s = v^1 + v^0 + \sum v^h + \sum v^{ih} \tag{3}$$

The resulting in-quadrature vector $\mathbf{v}_{\alpha\beta}$ at the output of QSG given in (4) contains all the voltage components mentioned in (3), where $n = 1$ represents the fundamental component and $n = 3,5,7,9,\ldots$ represents harmonics.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \underbrace{V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \cos\left(\omega\left(t - \frac{T}{4}\right) + \theta_1\right) \end{bmatrix}}_{fundamental\ component} + \underbrace{\begin{bmatrix} v_\alpha^0 \\ v_\beta^0 \end{bmatrix}}_{Dc-offset} + \underbrace{\sum_{n=3,5,7,9,\ldots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos\left(n\omega\left(t - \frac{T}{4}\right) + \theta_n\right) \end{bmatrix}}_{Harmonics} + \underbrace{\sum \mathbf{v}^{ih}}_{Interharmonics} \tag{4}$$

Equation (4) can be rewritten as below:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \cos\left(\omega t - \frac{\pi}{2} + \theta_1\right) \end{bmatrix} + \begin{bmatrix} v_\alpha^0 \\ v_\beta^0 \end{bmatrix} + \sum_{n=3,5,7,9,\ldots} V^n \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos\left(n\omega t - \frac{n\pi}{2} + \theta_n\right) \end{bmatrix} + \sum \mathbf{v}^{ih} \tag{5}$$

Solving (5), the harmonics can be divided in the form of positive and negative set of harmonics, as described by (6).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \sin(\omega t + \theta_1) \end{bmatrix} + \begin{bmatrix} v_\alpha^0 \\ v_\beta^0 \end{bmatrix} + V^n \left(\sum_{n=3,7,11,\ldots} \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos\left(n\omega t - \frac{3\pi}{2} + \theta_n\right) \end{bmatrix} + \sum_{n=5,9,13,\ldots} \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \cos\left(n\omega t - \frac{\pi}{2} + \theta_n\right) \end{bmatrix} \right) + \sum \mathbf{v}^{ih} \tag{6}$$

Equation (6) can be transformed to (7) by using basic trigonometry as below:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \sin(\omega t + \theta_1) \end{bmatrix} + \begin{bmatrix} v_\alpha^0 \\ v_\beta^0 \end{bmatrix} + V^n \left(\sum_{n=3,7,11,\dots} \begin{bmatrix} \cos(-n\omega t - \theta_n) \\ \sin(-n\omega t - \theta_n) \end{bmatrix} + \sum_{n=5,9,13,\dots} \begin{bmatrix} \cos(n\omega t + \theta_n) \\ \sin(n\omega t + \theta_n) \end{bmatrix} \right) + \sum \mathbf{v}^{ih} \quad (7)$$

The generalized equation for $v_{\alpha\beta}$ is depicted in (8)

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V^1 \begin{bmatrix} \cos(\omega t + \theta_1) \\ \sin(\omega t + \theta_1) \end{bmatrix} + \begin{bmatrix} v_\alpha^0 \\ v_\beta^0 \end{bmatrix} + V^n \left(\sum_{n=3,7,11,\dots} \begin{bmatrix} \cos\big(\psi(n\omega t + \theta_n)\big) \\ \sin\big(\psi(n\omega t + \theta_n)\big) \end{bmatrix} \right) + \sum \mathbf{v}^{ih} \quad (8)$$

where,

$$\psi = \begin{cases} +1 & for\ n = 5,9,13,\dots \\ -1 & for\ n = 3,7,11,\dots \end{cases}$$

The proposed PLL is designed in the *dq*-frame, which however, results in unwanted oscillations when the input signal with more than one frequency is transformed with a specific angular speed, as can be realized from (9). The n in (9) represents the *dq*-frame under consideration and m holds all other values except n. Thus, we must cancel out the effect of oscillations from the transformed voltage vector and achieve a clean fundamental voltage vector $\mathbf{v}_{dq}^{+1}$ for the estimation of the grid angle and frequency.

$$\mathbf{v}_{dq}^{n} = \left[\mathrm{T}_{dq}^{n}\right]\mathbf{v}_{\alpha\beta} = \underbrace{\mathbf{V}_{dq}^{n}}_{non-oscillating} + \underbrace{\sum_{m\neq n} \left\{\mathbf{V}_{dq}^{m}\left[\mathrm{T}_{dq}^{n-m}\right]\right\}}_{Oscillating\ terms} \quad (9)$$

where, $\mathbf{V}_{dq}^{n}$ is the DC term (non-oscillating) for the n^{th} rotating frame, $\mathbf{V}_{dq}^{m}$ is the amplitude of m^{th} frequency component of the oscillating term and $\left[\mathrm{T}_{dq}^{n}\right]$ is used to transform the input vector to corresponding *dq*-frame and is given in (10) with θ being the PLL angle.

$$\left[\mathrm{T}_{dq}^{n}\right] = \begin{bmatrix} \cos(n\theta) & \sin(n\theta) \\ -\sin(n\theta) & \cos(n\theta) \end{bmatrix} \quad (10)$$

The proposed DHIH module in this work comprises of a DC elimination block and a harmonic/interharmonic compensation unit. The DC block is developed using a mathematical cancellation scheme for the fast and accurate compensation of grid voltage DC-offset. The mathematical cancelation is required because oscillations resulting from DC-offset have low frequency in the *dq*- frame. The HIH unit, on other hand, takes DC compensated signal as the input and clear it from the effect of harmonics and interharmonics.

While developing DC-offset compensation block, the effect of harmonics and interharmonics are not considered, and will be compensated later using the proposed HIH unit. Then, using (9), the *dq*-transformed voltage vectors for $n = +1$ (fundamental) and $n = 0$ (DC-offset) is obtained as in (11).

$$\begin{bmatrix} \mathbf{v}_{dq}^{+1} \\ \mathbf{v}_{dq}^{0} \end{bmatrix} = \underbrace{\begin{bmatrix} \bar{\mathbf{V}}_{dq}^{+1} \\ \bar{\mathbf{V}}_{dq}^{0} \end{bmatrix}}_{DC\ terms} + \underbrace{\begin{bmatrix} [0] & \left[T_{dq}^{+1-(0)}\right] \\ \left[T_{dq}^{0-(+1)}\right] & [0] \end{bmatrix}\begin{bmatrix} \bar{\mathbf{V}}_{dq}^{+1} \\ \bar{\mathbf{V}}_{dq}^{0} \end{bmatrix}}_{oscillating\ terms} \quad (11)$$

It can be seen that the desired voltage vector $\mathbf{v}_{dq}^{+1}$, in addition to DC term $\bar{\mathbf{V}}_{dq}^{+1}$, suffers from fundamental frequency oscillations appearing because of DC-offset. Consequently, oscillations are decoupled by rewriting (11) as (12).

$$\begin{bmatrix} \bar{\mathbf{V}}_{dq}^{+1} \\ \bar{\mathbf{V}}_{dq}^{0} \end{bmatrix} = \begin{bmatrix} \mathbf{v}_{dq}^{+1} \\ \mathbf{v}_{dq}^{0} \end{bmatrix} - \begin{bmatrix} [0] & \left[T_{dq}^{+1-(0)}\right] \\ \left[T_{dq}^{0-(+1)}\right] & [0] \end{bmatrix}\begin{bmatrix} \bar{\mathbf{V}}_{dq}^{+1} \\ \bar{\mathbf{V}}_{dq}^{0} \end{bmatrix} \quad (12)$$

The unknown DC voltage vectors $\bar{\mathbf{V}}_{dq}^{m}$ on right hand side of (12) are replaced with filtered vectors $\bar{\mathbf{V}}_{dq}^{m*}$. Whereas, the unknown vectors $\bar{\mathbf{V}}_{dq}^{n}$ on left hand side of (12) are replaced with estimated vectors $\bar{\mathbf{V}}_{dq}^{n\prime}$. The new form of (12) is given in (13), where $\bar{\mathbf{V}}_{dq}^{m*}$ are obtained by passing the estimated $\bar{\mathbf{V}}_{dq}^{m\prime}$ through a LPF using (14) to remove any residual oscillations from the decoupled voltage vectors. For optimally damped response, the cutoff frequency ω_{cut} of the LPF_1 is selected as $\omega/\sqrt{2}$ for positive component and $\omega/4.5$ of the LPF_2 for DC component (with ω being the nominal grid frequency). The LPFs is used to allow the proper subtraction of voltage vectors (and not to filter out the DC-offset); hence, the dynamic response of the PLL remains unaffected.

$$\begin{bmatrix} \bar{\mathbf{V}}_{dq}^{+1\prime} \\ \bar{\mathbf{V}}_{dq}^{0\prime} \end{bmatrix} = \begin{bmatrix} \mathbf{v}_{dq}^{+1} \\ \mathbf{v}_{dq}^{0} \end{bmatrix} - \begin{bmatrix} [0] & \left[T_{dq}^{+1-(0)}\right] \\ \left[T_{dq}^{0-(+1)}\right] & [0] \end{bmatrix}\begin{bmatrix} \bar{\mathbf{V}}_{dq}^{+1*} \\ \bar{\mathbf{V}}_{dq}^{0*} \end{bmatrix} \quad (13)$$

$$\bar{\mathbf{V}}_{dq}^{m*} = \frac{\omega_{cut}}{s + \omega_{cut}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \bar{\mathbf{V}}_{dq}^{m\prime} \quad (14)$$

To obtain oscillation free voltage vectors, (13) can be solved and rearranged, as expressed below:

$$\bar{\mathbf{V}}_{dq}^{n\prime} = \left[T_{dq}^{n}\right]\bar{\mathbf{V}}_{\alpha\beta}^{n\prime} = \left[T_{dq}^{n}\right]\left(\mathbf{v}_{\alpha\beta} - \sum\nolimits_{m\neq n} \bar{\mathbf{V}}_{\alpha\beta}^{m*}\right) \quad (15)$$

where $\bar{\mathbf{V}}_{\alpha\beta}^{m*} = \left[T_{dq}^{-m}\right]\bar{\mathbf{V}}_{dq}^{m*}$.

The multiple use of (15) for +1 and 0 results in fundamental voltage vector in *dq*-frame $\mathbf{V}_{dq}^{+1\prime}$, which is free from the DC-offset, (see Fig. 2).

The harmonics/interharmonics are now compensated using the proposed HIH unit. Note that the proposed HIH is simple yet effective compensation method that does not require prior knowledge of individual harmonics/interharmonic to be compensated. Furthermore, unlike MHDCPLL the proposed technique does not need multiple transformations for the elimination of each individual harmonic, resulting in a simpler and computationally efficient harmonic mitigation, while maintaining the faster dynamic response of the PLL.

The DC-offset compensated positive voltage vector $\bar{\mathbf{V}}_{dq}^{+1\prime}$ is transferred to the HIH unit for the effective compensation of contained harmonics and interharmonics. The first step involved in HIH is to pass $\bar{\mathbf{V}}_{dq}^{+1\prime}$ (which is free from DC-offset but contains harmonics and interharmonics) through a High

Pass Filter (HPF) so that all the high frequency oscillations go through it and at the same time, it blocks the DC-term associated with +1 component. Thus, the output of HPF is a voltage vector, $\bar{\mathbf{V}}_{dq}^{+1'HF}$, that contains oscillations due to harmonics and interharmonics only, given in (16).

$$\bar{\mathbf{V}}_{dq}^{+1'HF} = [HPF]\bar{\mathbf{V}}_{dq}^{+1'} = \frac{s}{s+\omega_h}\bar{\mathbf{V}}_{dq}^{+1'} \tag{16}$$

The cutoff frequency ω_h, considering the PLL's accuracy and faster dynamics, falls in a range $0.2\omega<\omega_h<0.5\omega$. In the end, the $\bar{\mathbf{V}}_{dq}^{+1'HF}$ containing undesired oscillations is subtracted from the actual input $\bar{\mathbf{V}}_{dq}^{+1'}$ (containing dq^{+1}-DC-term and oscillations), enabling an effective decoupling of harmonics and interharmonics. This result in a clean fundamental voltage vector $\bar{\mathbf{V}}_{dq\text{-}pp}^{+1'}$, which is free from DC-offset, harmonics and interharmonics, given in (17).

$$\begin{aligned}\bar{\mathbf{V}}_{dq\text{-}pp}^{+1'} &= \bar{\mathbf{V}}_{dq}^{+1'} - \bar{\mathbf{V}}_{dq\text{-}HF}^{+1'} \\ &= \bar{\mathbf{V}}_{dq}^{+1'} - [HPF]\bar{\mathbf{V}}_{dq}^{+1'}\end{aligned} \tag{17}$$

The q-component of the resulting $\bar{\mathbf{V}}_{dq\text{-}pp}^{+1'}$ is passed to the PD part to extract the required phase (θ_g') and frequency (f_g') of the grid voltage.

3. Frequency-Phase Decoupling and Integral Update (FPDIU) Phase Detector

The PD part of the proposed PLL is equipped with FPD method [15] to avoid unwanted frequency swings and oscillations that occurs in the event of grid voltage faults, phase variations and other grid disturbances. The FPD is achieved by taking out the term $(\theta_{error}.k_p)$ from the frequency estimation loop of the PD, as expressed in (18). In addition, the frequency overshoot of the PLL under grid faults is adaptively controlled and reduced by applying a tuning mechanism to update the integral coefficient of the PI controller. The integral parameter T_i is updated by multiplying it with a factor (U_f) that depends on the fundamental vector $\bar{\mathbf{V}}_{dq\text{-}pp}^{+1'}$ and the phase error θ_{error}, as given in (19), where λ is the damping factor, holding value in a range of 50 to 100 [15]. Thus, the FPDIU results in lower frequency overshoot of the PLL and helps in reducing the oscillations/swings in the events of grid disturbances. Consequently, the lower overshoot of the proposed PLL can be interpreted as the improvement to the PLL's time response as it can be now tuned for even faster response without violating the assigned grid frequency limits.

$$f_g' = \frac{1}{2\pi}\left[\theta_{error}\cdot\frac{1}{T_i s} + \omega_{nom}\right] \tag{18}$$

$$U_f = \left(1 + \lambda\left(\theta_{error}/\sqrt{\left(\bar{v}_{d\text{-}pp}^{+1'}\right)^2 + \left(\bar{v}_{q\text{-}pp}^{+1'}\right)^2}\right)^2\right) \tag{19}$$

B. The Existing SOGI-PLL

In the implementation of SOGI-PLL, the vector v_s is converted into in-phase and quadrature component v_{s_α} and v_{s_β} respectively, which are 90° apart, as shown in Fig. 3. The transfer function of v_{s_α} and v_{s_β} with respect to input voltage is given in (20) and (21).

$$H_\alpha(s) = \frac{v_{s_\alpha}(s)}{v_s(s)} = \frac{k\omega_g s}{s^2 + k\omega_g s + {\omega_g}^2} \tag{20}$$

$$H_\beta(s) = \frac{v_{s_\beta}(s)}{v_s(s)} = \frac{k{\omega_g}^2}{s^2 + k\omega_g s + {\omega_g}^2} \tag{21}$$

where, ω_g is the estimated grid frequency and k is SOGI weighting factor.

The resulting in-quadrature $v_{s_{\alpha\beta}}$ is transformed to rotating reference frame by using (10) followed by a PI controller based phase detector part.

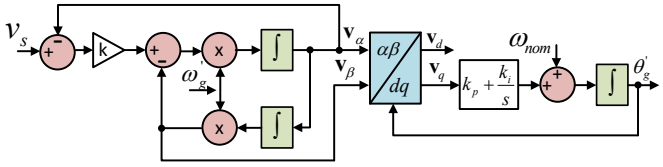

Fig. 3: Schematic diagram of SOGI-PLL.

C. The Existing MHDC-PLL

The MHDC-PLL consists of two parts, QSG and MHDC. The QSG part is composed of quarter delay transformation and IPT technique. The vector v_s is passed through IPT, further to which quarter delay technique is used to extract in-quadrature components $v_{s_{\alpha\beta}}$ as shown in Fig. 4, providing some attenuation to higher order harmonics.

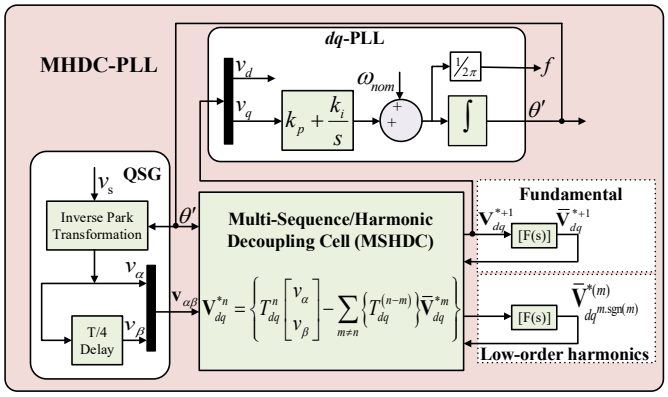

Fig. 4: Schematic diagram of MHDC-PLL

The low order harmonics are removed from in-quadrature component using the MHDC part by selective harmonic elimination. Further, the vector $v_{s_{\alpha\beta}}$ is transformed to dq-reference frame, where phase angle is extracted by forcing the q-component to zero by using a PI controller. For the sake of fair comparison, SOGI and MHDC PLL are tuned in a same way as of the proposed PLL.

III. TUNING PROCEDURE OF THE PROPOSED PLL

For the accurate estimation and response of the PLL, the optimal tuning is very important and critical. The small signal linearized model of the PLL is used for the calculation of

tuning parameters, k_p and T_i. The closed loop Transfer Function (TF) of the proposed PLL (based on small signal analysis) is given in (22).

$$TF_\theta = \frac{\theta_g'}{\theta} = \frac{2\zeta\omega_n \cdot s + {\omega_n}^2}{s^2 + 2\zeta\omega_n \cdot s + {\omega_n}^2} = \frac{k_p \cdot s + {}^1/_{T_i}}{s^2 + k_p \cdot s + {}^1/_{T_i}} \quad (22)$$

Where, θ is the actual grid voltage phase angle and θ_g' is the estimated angle of the PLL. The system in (22) presents a typical second-order transfer function and can be tuned based on natural frequency ω_n and damping coefficient ζ. By setting the value of ζ to 1.414 (for optimal damping) and expressing ω_n in terms of settling time (ST), the tuning parameters k_p and T_i are given in (23). The Settling time (ST) is set 100 ms for the for all PLLs considered for benchmarking including the proposed, and the values of k_p and T_i are calculated as 92 and 4256, respectively.

$$k_p = \frac{9.2}{ST} \text{ and } T_i = (0.047 \cdot \zeta^2 \cdot ST^2) \quad (23)$$

The proposed PLL is further equipped with integral update in order to control the the frequency overshoot of the PLL under grid faults, where T_i is adaptively adjusted based on grid voltage, θ_{error} and damping factor λ. The integral update is applied by multiplying pre-calculated integral coefficient (23) with an adaptive factor U_f given in (19) and thus, the revised T_i considering integral update is shown in (24).

$$T_i = (0.047 \cdot \zeta^2 \cdot ST^2)U_f \quad (24)$$

Thus, for the proposed PLL, k_p is constant for given settling time but the value of T_i is adaptively updated considering the voltage and θ_{error}, hence it adjust itself according to the grid variation. Moreover, the ST can be varied according to the required dynamics. It is worth mentioning here that parameters of MHDCPLL and SOGIPLL are also tuned for 100 ms for the sake of fair comparison.

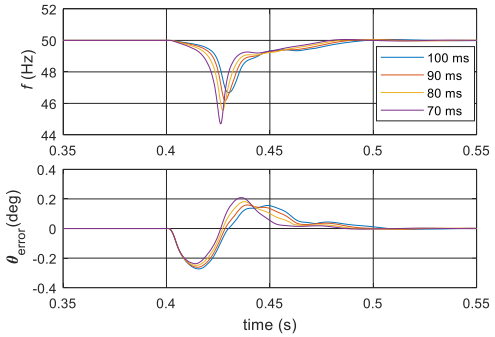

Fig. 5: Response of proposed PLL for different settling time.

Table 1: Tuning parameter of proposed PLL for different settling time.

Settling Time (ms)	k_p	T_i
100	92	4256
90	102.2	5255
80	115	6651
70	131.428	8687

The effect of parameter setting on the performance of proposed PLL for different settling time under -25° phase variation is shown in Fig. 5. The set of tuning parameters for various settling times (calculated using (23)) is given in Table 1 and the corresponding variations in the estimated frequency and error are presented in Fig. 5, where with normal initial grid voltage a −25° phase change occurs at 0.4 s.

IV. Bode Analysis And Computational Complexity

The DHIH transfer function is the combination of transfer characteristics from the DC-offset block and the HIH unit. For DC block, $\bar{\mathbf{V}}_{\alpha\beta}^{n\prime}$ is extracted from (15) and rewritten as:

$$\bar{\mathbf{V}}_{\alpha\beta}^{n\prime} = \mathbf{v}_{\alpha\beta} - \sum\nolimits_{m\neq n} \bar{\mathbf{V}}_{\alpha\beta}^{m*} \quad (25)$$

Substituting (26) in (25), results in (27).

$$\begin{aligned}\bar{\mathbf{V}}_{\alpha\beta}^{m*} &= \left[T_{dq}^{-m}\right]\bar{\mathbf{V}}_{dq}^{m*} = \left[T_{dq}^{-m}\right][LPF]\bar{\mathbf{V}}_{dq}^{m\prime} \\ &= \left[T_{dq}^{-m}\right][LPF]\left[T_{dq}^{m}\right]\bar{\mathbf{V}}_{\alpha\beta}^{m\prime}\end{aligned} \quad (26)$$

$$\bar{\mathbf{V}}_{\alpha\beta}^{n\prime} = \mathbf{v}_{\alpha\beta} - \sum\nolimits_{m\neq n} \left(\left[T_{dq}^{-m}\right][LPF]\left[T_{dq}^{m}\right]\bar{\mathbf{V}}_{\alpha\beta}^{m\prime}\right) \quad (27)$$

Finally, expanding (27) for the fundamental component, that is for $n = +1$:

$$\bar{\mathbf{V}}_{\alpha\beta}^{+1\prime} = \mathbf{v}_{\alpha\beta} - \left[T_{dq}^{0}\right][LPF]\left[T_{dq}^{0}\right]\bar{\mathbf{V}}_{\alpha\beta}^{0\prime} \quad (28)$$

In order to obtain the transfer function $\bar{\mathbf{V}}_{\alpha\beta}^{+1*}/\mathbf{v}_{\alpha\beta}$ of DC-offset block, (28) is substituted with $\bar{\mathbf{V}}_{\alpha\beta}^{0\prime}$ (using $n = 0$ in (27)) and the resultant is given as follows:

$$\begin{aligned}\bar{\mathbf{V}}_{\alpha\beta}^{+1\prime} &= \mathbf{v}_{\alpha\beta} - \left[T_{dq}^{0}\right][LPF]\left[T_{dq}^{0}\right]\mathbf{v}_{\alpha\beta} \\ &+\left(\left[T_{dq}^{-0}\right][LPF]\left[T_{dq}^{0}\right]\right)\left(\left[T_{dq}^{-1}\right][LPF]\left[T_{dq}^{+1}\right]\right)\bar{\mathbf{V}}_{\alpha\beta}^{+1\prime}\end{aligned} \quad (29)$$

The final transfer function for DC-offset is achieved below by rearranging (29) as:

$$\begin{aligned}TF_{DC} &= \frac{\bar{\mathbf{V}}_{\alpha\beta}^{+1\prime}}{\mathbf{v}_{\alpha\beta}} \\ &= \frac{1 - \left(\left[T_{dq}^{0}\right][LPF]\left[\mathrm{T}_{dq}^{0}\right]\right)}{1 - \left(\left[T_{dq}^{0}\right][LPF]\left[\mathrm{T}_{dq}^{0}\right]\right)\left(\left[T_{dq}^{-1}\right][LPF]\left[\mathrm{T}_{dq}^{+1}\right]\right)}\end{aligned} \quad (30)$$

The transfer function for $\left[T_{dq}^{-x}\right][LPF]\left[\mathrm{T}_{dq}^{x}\right]$ is calculated using Euler formula in complex domain, as expressed in (31), where ω_{cut} is LPF's cutoff frequency for x^{th} frequency component.

$$\left[T_{dq}^{-x}\right][LPF]\left[\mathrm{T}_{dq}^{x}\right] = \frac{\omega_{cut}}{s + (\omega_{cut} - j \cdot x \cdot \omega)} \quad (31)$$

The HIH unit transfer function on the other hand is obtained by multiplying $\left[T_{dq}^{-1}\right]$ with (17), given as (32).

$$\begin{aligned}\left[T_{dq}^{-1}\right]\bar{\mathbf{V}}_{dq\text{-}pp}^{+1\prime} &= \left[T_{dq}^{-1}\right]\bar{\mathbf{V}}_{dq}^{+1\prime} - \left[T_{dq}^{-1}\right][HPF]\bar{\mathbf{V}}_{dq}^{+1\prime} \\ \bar{\mathbf{V}}_{\alpha\beta\text{-}pp}^{+1\prime} &= \bar{\mathbf{V}}_{\alpha\beta}^{+1\prime} - \left[T_{dq}^{-1}\right][HPF]\left[T_{dq}^{+1}\right]\bar{\mathbf{V}}_{\alpha\beta}^{+1\prime}\end{aligned} \quad (32)$$

where, $\bar{\mathbf{V}}_{\alpha\beta}^{+1\prime} = \left[T_{dq}^{-1}\right]\bar{\mathbf{V}}_{dq}^{+1\prime}$

Therefore, rearranging (32) results in HIH module transfer function as:

$$TF_{HIH} = \frac{\bar{\mathbf{V}}^{+1'}_{\alpha\beta-pp}}{\bar{\mathbf{V}}^{+1'}_{\alpha\beta}} = 1 - \left[T_{dq}^{-1}\right][HPF]\left[T_{dq}^{+1}\right] \quad (33)$$

Hence, the complete transfer function for the overall DHIH module is obtained by multiplying (30) and (33), and is given as:

$$TF_{DHIH} = TF_{DC}TF_{HIH} = \left(\frac{\bar{\mathbf{V}}^{+1'}_{\alpha\beta}}{\mathbf{v}_{\alpha\beta}}\right)\left(\frac{\bar{\mathbf{V}}^{+1'}_{\alpha\beta-pp}}{\bar{\mathbf{V}}^{+1'}_{\alpha\beta}}\right) = \left(\frac{1 - \left(\left[T_{dq}^{0}\right][LPF]\left[\mathrm{T}_{dq}^{0}\right]\right)}{1 - \left(\left[T_{dq}^{0}\right][LPF]\left[\mathrm{T}_{dq}^{0}\right]\right)\left(\left[T_{dq}^{-1}\right][LPF]\left[\mathrm{T}_{dq}^{+1}\right]\right)}\right)(1 - \left[T_{dq}^{-1}\right][HPF]\left[T_{dq}^{+1}\right]) \quad (34)$$

The Bode diagram in Fig. 6 compares the proposed PLL with MHDCPLL. The proposed ASφPLL passes the positive sequence component (50 Hz) with unity gain and zero phase shift. The DC-component (0 Hz) and all other harmonics/interharmonics are blocked by large negative gains and phase shifts. The MHDCPLL has limited filtering capabilities for interharmonics and works only for selected low-order harmonics. The maximum filtering capability of the MHDCPLL for the harmonics other than the selected, as seen from the Bode is −39 db, whereas for the proposed PLL, the maximum filtering capability is around −75.5 db. This shows, the proposed PLL has better suppression capability and is able to compensate for all harmonics/interharmonics present in the grid voltage.

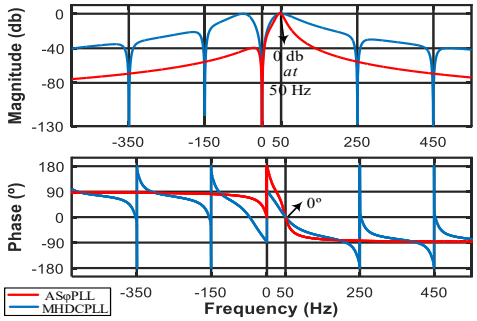

Fig. 6: Bode analysis of the proposed PLL

Table 2: Complexity and performance comparison of four PLLs.

PLLs		ASφPLL	MHDCPLL	SOGIPLL	NMAFPLL
Mathematical operations		× = 43	× = 342	× = 13	× = 47
		+ = 12	+ = 69	+ = 7	+ = 12
		− = 8	− = 135	− = 3	− = 7
Processing time		20.1 µs (12.85%)	156.4 µs (100%)	6.2 µs (3.96%)	21.6 µs (13.8%)
Features (Accurate estimation under)	Harmonics	✓	✓	×	✓
	Inter-	✓	×	×	✓
	Dc-offset	✓	✓	×	✓
	Freq. variation	✓	✓	✓	✓
	Phase	✓	✓	✓	✓
	Sag	✓	✓	✓	✓

The complexity analysis provided in Table 2 for the four PLLs proves that the proposed PLL has significantly less complexity than MHDCPLL and NMAFPLL and work for all the abnormal grid conditions. The SOGIPLL on the other hand, is less complex than proposed PLL however it does not work for the harmonics, interharmonics and DC-offset. The algebraic operators (additions, subtractions and multiplications) required by each PLL are counted and in addition, all PLLs are implemented using Texas Instrument TMS320F28335 microcontroller and their processing times are experimentally measured. The proposed PLL eliminates all the faults and requires a smaller number of algebraic operators and less processing time compared to the other PLLs. This validates the lower complexity and robust performance of the ASφPLL.

For real-time applications, the control algorithm is always implemented in the embedded microcontroller (with limited processing resources). Consequently, for complex algorithms, embedded microcontrollers are unable to operate at required sampling rate and a reduction in sampling rate is required which increases the discretization error. Less complex algorithms are appropriate solution to this problem and, accordingly the proposed PLL is a suitable candidate for such applications. The lower computational complexity of the proposed PLL is a very important benefit and characteristic for the grid side converter control. It ensures that the sampling rate of the PLL will not be compromised in order to accommodate the new features, thus, the applicability of the proposed technique on commercial inverters is not limited by the available computational resources of the embedded DSP/microcontroller.

V. Validation of the Proposed PLL

A. Simulation Results

This section validates the accurate estimation of proposed PLL and compares it with MHDCPLL and SOGIPLL. The sampling frequency used is 10 kHz.

The first case analyses the behavior of PLLs under gird voltage harmonics, phase change and frequency variation, Fig. 7. With normal initial grid voltage, 4% 3rd and 4.5% 5th harmonics are injected at 0.3 s. The SOGIPLL suffers from oscillations, as it is not immune to harmonics. The proposed ASφPLL provides faster compensation, whereas the MHDCPLL takes 16 ms to fully compensate the harmonics. Following this, a phase change of −28º occurs at 0.4 s, to which MHDCPLL and SOGIPLL suffer from a very high frequency overshoot (of around −7.5 Hz). At 0.6 s a frequency change event of −2 Hz occurs, to which the MHDCPLL suffers from oscillations. However, the ASφPLL results in an accurate and oscillation free estimation of frequency and phase angle.

The second case analyses the PLLs under interharmonics (5.3% 2.8th and 4.1% 7.2th), DC-offset plus the harmonic (4% DC-offset and 5% 7th harmonic) and voltage sag (25%), depicted in Fig. 8. The voltage is distorted with interharmonics at 0.3 s. The MHDCPLL and SOGIPLL suffers from oscillations, with no immunity to interharmonics. The

suppression provided by MHDC to 2.8th interharmonic is around −16 dB whereas the proposed PLL provides an attenuation of −41.06 dB. Both MHDC and ASφ PLLs survive the DC-offset and harmonic event at 0.4 s, however, the estimated quantities by SOGI suffer from oscillations. Following this, voltage sag occurs at 0.5 s and reverts back to normal at 0.65 s, to which the proposed PLL results in lower frequency overshoot.

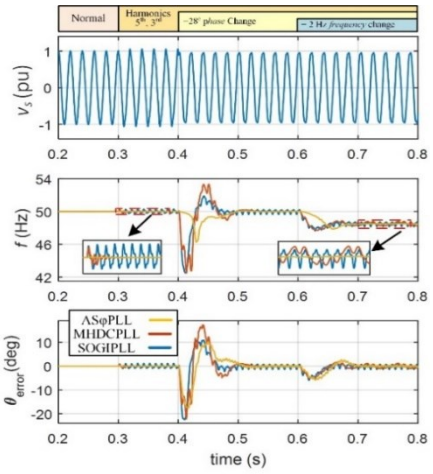

Fig. 7: Performance comparison of three PLLs under first case.

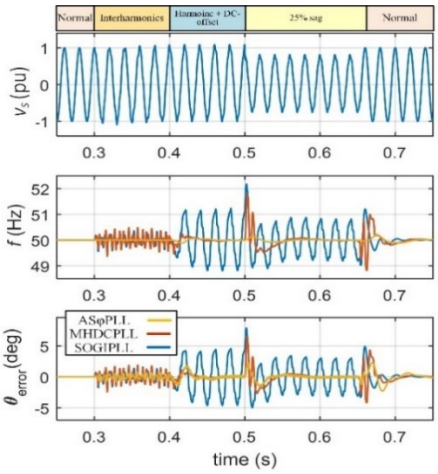

Fig. 8: Performance comparison of three PLLs under second case.

Table 3: Summary of result presented in Fig. 7 and Fig. 8.

PLL's types		Fault types	Fig. 7 Harm.	Fig. 7 Phase + Harm	Fig. 7 Freq + Phase + Harm	Fig. 8 IH	Fig. 8 H+DC	Fig. 8 Sag
SOGI PLL	Overshoot	Frequency (Hz)	-	7.5	2.27	-	-	-
		θ_{error} (deg)	-	22.42	5.9	-	-	-
	Settling time	Frequency (ms)	-	90	80	-	-	-
		θ_{error} (ms)	-	80	69	-	-	-
MHDC PLL	Overshoot	Frequency (Hz)	-	7.5	2.2	-	0.48	1.8
		θ_{error} (deg)	-	22.41	5.08	-	1.04	6.61
	Settling time	Frequency (ms)	-	90	80	-	50	85
		θ_{error} (ms)	-	80	80	-	47	87
ASφ PLL	Overshoot	Frequency (Hz)	-	3.73	2.14	-	0.12	0.14
		θ_{error} (deg)	-	17.53	5.08	-	1.84	2.27
	Settling time	Frequency (ms)	-	90	60	-	29	54
		θ_{error} (ms)	-	80	69	-	47	87

The results presented in Fig. 7 and Fig. 8 are tabulated and summarized in Table 3. For the harmonics and interharmonics, only oscillations are present without over/undershoot. The performance and estimation accuracy of proposed technique is also compared with a recent Nonadaptive Moving Average Filter based Phase Locked Loop (NMAFPLL) [26] in addition to SOGIPLL and MHDCPLL under a set of abnormal grid conditions.

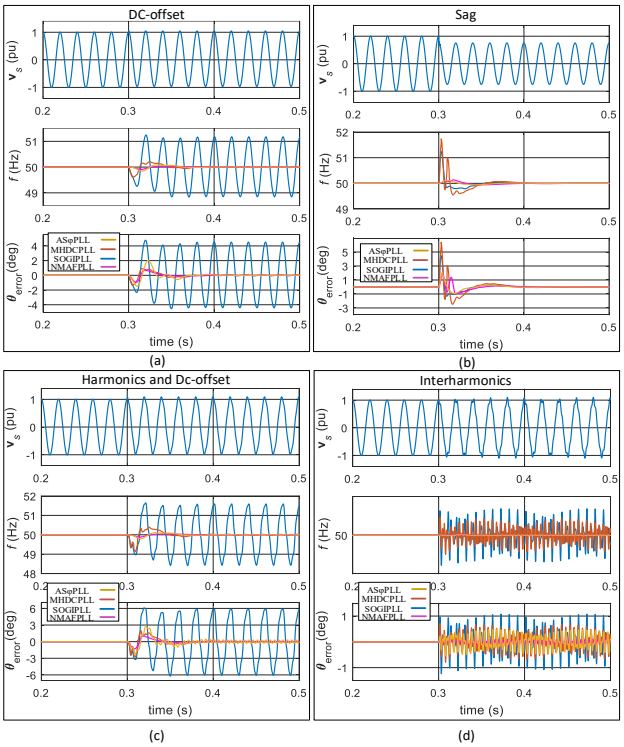

Fig. 9: Performance comparison of four PLLs under abnormal grid conditions

All the four PLLs (ASφPLL, SOGIPLL, MHDCPLL and NMAFPLL) are further subjected to certain set of conditions. First of all, a DC-offset of 4% (that is 13 V) with respect to the fundamental voltage is introduced in Fig. 9 (a). The SOGIPLL suffers from high oscillations in both frequency and phase estimation. However, on other side, the remaining three including proposed PLL removes DC-offset accurately with less overshoot and settling time. Similarly, the performance of four PLLs to 25% sag (325V to 244V) is shown in Fig. 9 (b). The MHDC- and SOGI- PLLs suffer from high overshoot and settling time in the estimation of both θ_{error} and frequency. The NMAFPLL removes the effect of voltage sag but it has slightly more settling time in comparison to ASφPLL. The proposed PLL performs well for the frequency and phase error estimation. Furthermore, all the PLLs are subjected to 4% of 5th harmonic and 5.3% of DC-offset occurring simultaneously, Fig. 9 (c). The SOGIPLL suffers from high oscillation in both estimations in comparison with the other PLLs, as can be seen from Fig. 9 (c). The 4% of 5.2th and 5.3% of 7.2th interharmonics are induced at 0.3 s in Fig. 9 (d). Less than 0.5° oscillations are observed in NMAFPLL and the proposed PLL.

For the frequency estimation, the proposed and NMAFPLL has zero overshoot and settling time, in comparison with the MHDCPLL and SOGIPLL. Thus, the proposed PLL presents better performance for abnormal grid conditions but with lower complexity. The results presented in Fig. 9 are summarized in the Table 4.

Table 4: Summary of result presented in Fig. 9.

PLL's types		Fault types	DC-offset	Sag	HIH + DC-offset	IH
SOGI PLL	Overshoot	Frequency (Hz)	1.25*	1.24	1.64*	0.3*
		θ_{error} (deg)	4.77*	4.47	6.09*	1.23*
	Settling time	Frequency (ms)	-	93	-	-
		θ_{error} (ms)	-	85.5	-	-
MHDC PLL	Overshoot	Frequency (Hz)	0.4	1.74	1.14	0.19*
		θ_{error} (deg)	1.34	6.39	2.75	0.7
	Settling time	Frequency (ms)	74	100	74	-
		θ_{error} (ms)	41	90	75	-
ASφ PLL	Overshoot	Frequency (Hz)	0.15	0.12	0.19	-
		θ_{error} (deg)	2	1.9	2.8	0.32*
	Settling time	Frequency (ms)	44	64	54	-
		θ_{error} (ms)	72	43	70	-
NMAF PLL	Overshoot	Frequency (Hz)	0.14	0.13	0.12	-
		θ_{error} (deg)	0.94	1.9	1.33	0.22*
	Settling time	Frequency (ms)	44	86	54	-
		θ_{error} (ms)	72	55.6	65.7	-

* Recurrent oscillations

B. *Experimental Results*

This section is to experimentally validate the proposed ASφPLL and compare its performance with the state-of-the-art MHDCPLL and SOGIPLL. We use the dSPACE real-time simulator MicroLabBox and DS1202 DSP board to achieve our results. The experimental validation is carried out under various set of grid conditions, divided in to three case studies where: 1) the results of existing and proposed techniques are presented for all fault types individually, 2) the results are provided for two faults occurring at the same time, and 3) the results are provided for a set of 3 fault conditions. The sampling frequency of 10 kHz is used in the experimental results.

Case 1: This case involves experimental validation of PLLs under various set of grid conditions including frequency variation, voltage sag, phase change, voltage harmonics, interharmonics and DC-offset, as shown in Fig. 7. In all the experimental results, a red arrow is used to mark the point of disturbance and is labelled with the respective grid scenario.

The experimental results in Fig. 10 (a) investigates the response of MHDCPLL (blue color), SOGIPLL (green color) and proposed PLL (pink color) to a voltage sag event of 30.8%. The grid voltage is initially at 1 pu, which however, is varied to 0.692 pu at the point marked with red arrow. The proposed PLL responds to this voltage sag event and accurately tracks the desired grid phase and frequency. The faster dynamics of PLL can be seen from the settling time of both phase (52 ms) and frequency (23 ms). In addition, the peak value of θ_{error} and frequency (1.35º and 0.2 Hz respectively) validates the accurate response of the proposed ASφPLL. On the other hand, the frequency overshoot of SOGIPLL and MHDCPLL is 1.6 Hz, 1.95 Hz and settling time is 55 ms, 50 ms, respectively, as shown in Fig. 10 (a). Likewise, the overshoot of SOGIPLL for phase error is 2.75º with 50 ms settling time and for MHDCPLL is 7.6º and settled in 75 ms.

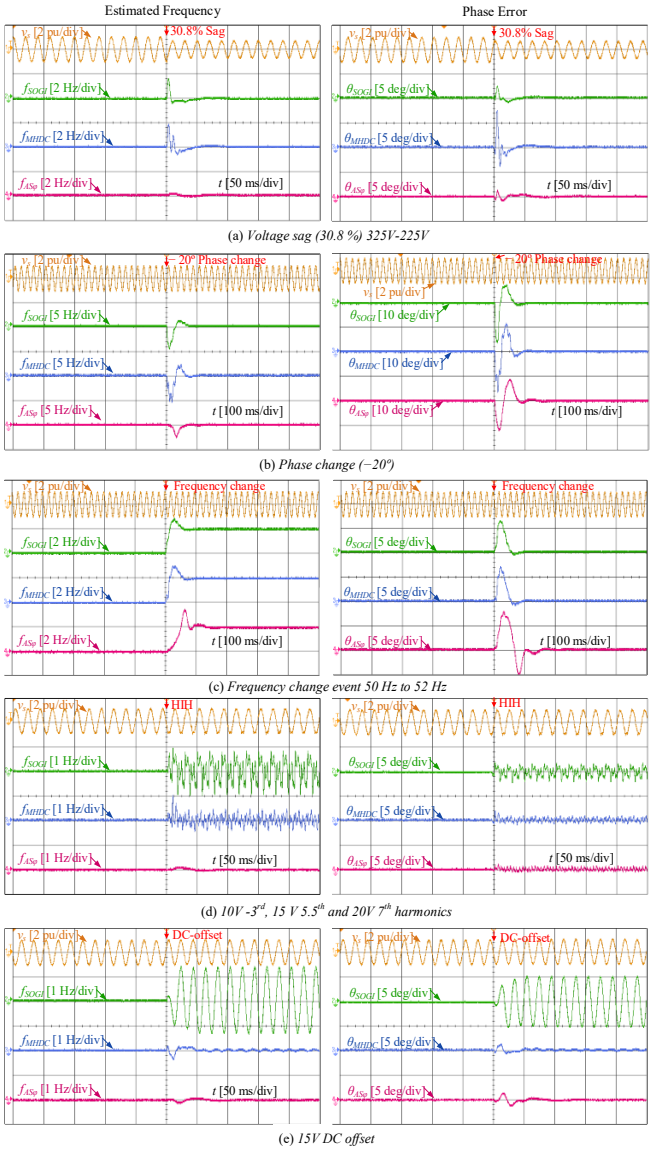

Fig. 10: Experimental validation of the proposed ASφPLL and its comparison with MHDCPLL and SOGIPLL under, (a) 30.8% voltage sag, (b) -20° phase change, (c) 50 to 52Hz frequency change, (d) harmonics and interharmonics, and (e) 15V DC-offset.

Furthermore, the performance of PLLs are analyzed under a phase change event. With zero initial phase, the grid voltage is subjected to a phase change of −20º and the corresponding results are depicted in Fig. 10 (b). The overshoot of SOGIPLL for frequency estimation is 4.5 Hz with a settling time of 75 ms. The θ_{error} experiences an overshoot of 16.3º and get settled in 100 ms. The MHDCPLL gives an overshoot of 5.2 Hz and 16.7º for frequency and θ_{error} with the settling time of 85 ms and 100 ms, respectively. The ASφPLL is also capable of mitigating the phase changes, and thus, reverts the estimated

phase and frequency to their desired values immediately after the phase fault occurs. The overshoot in phase error and frequency are respectively equal to 12º and 2.7 Hz, whereas the response time is approximately 100 ms and 62 ms for θ_{error} and estimated frequency. Thus, verifying the fast and accurate response of the proposed PLL to a phase change.

The response of three PLLs to a frequency variation of 2 Hz is shown in Fig. 10 (c). With initial frequency of 50 Hz, it is varied to 52 Hz at the point marked. As seen, the proposed ASφPLL accurately tracks the change in frequency with a response time of 120 ms and the overshoot of 1.4 Hz. Similarly, the response time of SOGI and MHDCPLL is 60 ms and 100 ms, with the overshoot of 0.95 Hz and 1 Hz, respectively. The error require approximately 150 ms to settle back to zero and the overshoot is 8º for the proposed PLL, 100 ms with an overshoot of 6.9º for SOGIPLL and 100 ms with 7.2º overshoot for MHDCPLL.

In Fig. 10 (d), the PLLs are further investigated for grid voltage harmonic and interharmonic distortion. With normal initial conditions, the grid voltage is distorted with 3% of 3rd harmonic, 4.6% of 5.5th interharmonic, and 6.1% of 7th harmonic. The percentage of harmonics and interharmonics are calculated with respect to the fundamental component. Compared to the proposed PLL, high oscillations are observed in the estimated quantities for both SOGIPLL and MHDCPLL. The overshoot in the frequency and phase error are respectively observed as 1 Hz and 2º for both SOGI and MHDCPLL, followed by large repeating oscillations. The proposed ASφPLL responds accurately to the harmonic distortion in the grid voltage with faster dynamic response and results in oscillation-free frequency and low θ_{error} oscillations in comparison with other PLLs. The peak value of oscillations observed in the phase and frequency of proposed PLL is respectively equal to 1º and 0.18 Hz, This shows very low magnitudes and the better performance of the proposed ASφPLL in comparison to the existing methods.

Table 5: Summary of results presented in Fig. 10.

PLL's types		Fault types	Voltage sag	Phase change	Frequency change	HIH	DC-offset
SOGI PLL	Overshoot	Frequency (Hz)	1.6	4.5	0.95	1	1.5
		θ_{error} (deg)	2.75	16.3	6.9	2	5
	Settling time	Frequency (ms)	55	75	60	-	-
		θ_{error} (ms)	50	100	100	-	-
MHDC PLL	Overshoot	Frequency (Hz)	1.95	5.2	1	1	0.4
		θ_{error} (deg)	7.6	16.7	7.2	2	1.5
	Settling time	Frequency (ms)	50	85	100	-	48
		θ_{error} (ms)	75	100	100	-	60
ASφ PLL	Overshoot	Frequency (Hz)	0.2	2.7	1.4	0.18	0.16
		θ_{error} (deg)	1.35	12	8	1	1.5
	Settling time	Frequency (ms)	23	62	120	-	40
		θ_{error} (ms)	52	100	150	-	60

Finally, the PLLs are analyzed and examined for the case of DC-offset in the grid voltage, and the response of all PLLs to this disturbance is shown in Fig. 10 (e). The grid voltage is shifted in magnitude by injecting a DC-offset of 4.6% (15 V) of peak grid voltage (i.e. 325.27). The proposed PLL accurately respond to DC-offset and remove the effect of fundamental frequency oscillation via mathematical cancellation DC-offset cell and results in accurate and oscillation-free estimation of phase/frequency, however, the MHDCPLL suffers from low and SOGI from high oscillations. The peak value of frequency oscillations at the point of fault is 0.16 Hz, 0.4 Hz and 1.5 Hz respectively for ASφPLL, MHDCPLL and SOGIPLL. Likewise, the peak value of phase error is 1.5º, 1.5º and 5º, respectively. This verifies the outstanding performance of the proposed ASφPLL. The results of case 1 presented in Fig. 10 is summarized in Table 5.

Case 2: This case investigates the performance of proposed and existing techniques for a set of 2 faults (occurring simultaneously), given in Fig. 11 and Fig. 12.

The results in Fig. 11 show PLL responses for a voltage sag of 30.8% (1 p.u. to 0.692 p.u.) together with a phase change of −20º. The red arrow indicates the point where both faults are induced. The proposed PLL suffers from low overshoot (8 Hz) and presents less settling time (125 ms) in the estimated frequency as compared to the MHDCPLL and SOGIPLL, whose overshoot is 15 Hz and 13 Hz, respectively and both settles in 150 ms. On the other hand, the overshoot of θ_{error} for ASφPLL, MHDCPLL and SOGIPLL is 28.5º, 38º and 33º, whereas, the settling time of 180 ms, 180 ms and 140 ms respectively as shown in Fig. 11. The results show the better performance of proposed technique with low overshoot for both frequency and phase error, and faster frequency estimation.

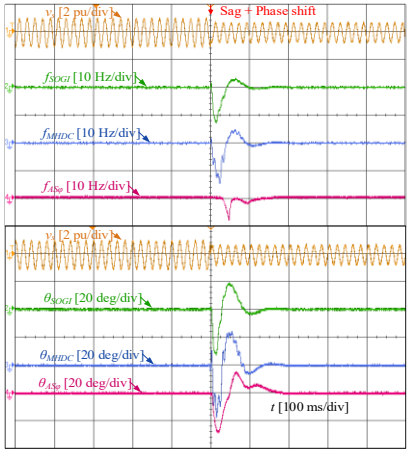

Fig. 11: Experimental validation of the proposed ASφPLL and its comparison with MHDCPLL and SOGIPLL under 30.8% sag and −20º phase change.

The second scenario investigate the effect of two simultaneous faults includes HIH and DC-offset, as shown in Fig. 12. The grid voltage is distorted with 3% of 7th harmonic, 4.6% of 5th harmonic, and 6.1% of 7.5th interharmonic along with a DC-offset of 4.6%. The proposed PLL accurately respond for this set of conditions and results in oscillation-free, fast and an accurate estimation of frequency and phase angle when compared to the other state of art techniques. The SOGIPLL suffers from high oscillation, and MHDCPLL also presents small oscillations, as shown in Fig. 12.

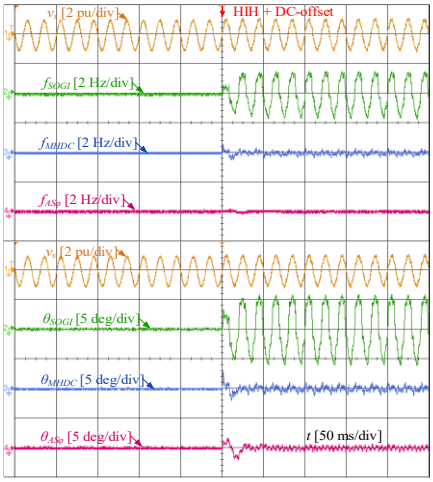

Fig. 12: Experimental validation of the proposed ASφPLL and its comparison with MHDCPLL and SOGIPLL under HIH, and DC-offset.

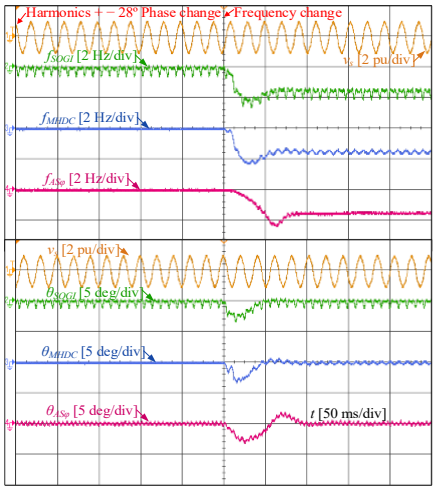

Fig. 13: Experimental validation of the proposed ASφPLL and its comparison with MHDCPLL and SOGIPLL under harmonics, − 28° phase change and −1.5 Hz frequency variation.

Case 3: This case shows the performance of PLLs under three set of fault conditions (similar to the simulation results shown in Fig. 7). The three conditions are harmonics, phase change and frequency variation. A 3% of 3rd harmonics (10V) and 4.6 % of 5th harmonic (15V) along with the phase shift of −28° are already present in the voltage even before the starting point of the result, Fig. 13. A frequency variation of −2.5 Hz (that is 50 Hz to 48.5 Hz) is then introduced at the centre of waveform (marked with arrow) and performance of proposed and existing PLLs is compared. From the estimated frequency waveform shown in Fig. 13, it can be seen that the overshoot of ASφPLL, MHDCPLL and SOGIPLL is 0.8 Hz, 0.8 Hz and 1.15 Hz with the settling time of 87.5 ms, 92 ms and 100 ms respectively. Where both MHDC and SOGI PLLs suffer from unwanted oscillations in comparison with the proposed technique. The estimated frequency in the proposed technique does not suffer from undesired oscillations and swings because of the FPD added in the phase detector part of PLL. Furthermore, the overshoot of θ_{error} for proposed PLL is 3.3° against 3.5° for the other techniques with oscillations. All the results presented in Fig. 11, Fig. 12 and Fig. 13 are summarized in Table 6.

Table 6: Summary of results presented in Fig. 11, Fig. 12 and Fig. 13.

PLL's types \ Fault types			Fig. 11 Sag+Phase	Fig. 12 HIH+DC-offset	Fig. 13 H + Phase + freq
SOGI PLL	Overshoot	Frequency (Hz)	13	-	1.15
		θ_{error} (deg)	33	-	3.5
	Settling time	Frequency (ms)	150	-	100
		θ_{error} (ms)	140	-	50
MHDC PLL	Overshoot	Frequency (Hz)	15	0.6	0.8
		θ_{error} (deg)	38	3	3.5
	Settling time	Frequency (ms)	150	20	92
		θ_{error} (ms)	180	19	50
ASφ PLL	Overshoot	Frequency (Hz)	8	0	0.8
		θ_{error} (deg)	28.5	2	3.3
	Settling time	Frequency (ms)	125	0	87.5
		θ_{error} (ms)	180	25	95

The proposed technique, in general, presents fast and accurate estimation with lower overshoot and almost no oscillations for various type of individual as well as combination of faults. Thus, the experimental results validate the accurate performance of proposed PLL towards synchronization of grid connected systems (V2G) under abnormal grid conditions.

VI. Impact of Accurate Synchronization on Grid Connected ESS

The performance of proposed PLL in estimating grid frequency and phase angle has been validated for several grid disturbances and as mentioned, synchronization directly affects the overall operation of grid connected ESS since it plays a vital role in transforming the voltages/currents to different domains, necessary for control purposes. Thus, it would be interesting to investigate the performance of proposed PLL for the case when it is used in the GSC controller (shown in Fig. 1) and compare it with the existing MHDCPLL. The PQ controller is designed in the synchronous reference frame based on the open-loop controller design. Thus, the reference currents ($\mathbf{i}_{dq}^{+1*}$) are generated based on P*, Q* and $\bar{\mathbf{V}}_{dq\text{-}pp}^{+1\prime}$, where, P* and Q* are the reference powers and $\bar{\mathbf{V}}_{dq\text{-}pp}^{+1\prime}$ is the fundamental oscillation-free voltage vector estimated by the PLL algorithm. The current controller is also designed in the synchronous reference frame and since, the investigation is carried out under distorted grid conditions, the current controller is enhanced with harmonic and interhamronic compensation. Furthermore, a fault ride through scheme is integrated in to the PQ controller to provide appropriate voltage and frequency support in the event of grid faults. The FRT scheme provides a Q/P ratio of 2:1 under faults and helps in limiting the converter currents to ensure the safety of converter.

The quality of power flowing to/from the grid and the Total Harmonic Distortion (THD) of the injected current becomes important while investigating the operation of grid connected system. A test case is performed, where, the grid voltage is subjected to various disturbances and the effect of existing MHDCPLL and proposed ASφPLL on the overall operation of grid connected ESS is analyzed. The following three disturbances occur in the grid voltage:

1. Harmonic and interharmonic (H+IH) condition: where grid voltage is distorted with 5th harmonic and 7.2th interhamronic each having 5% magnitude with respect to fundamental.
2. Interharmonic (IH) condition: where gird voltage has two interhamronics, 3.3th and 7.2th with 5% magnitude each.
3. Interharmonic and voltage sag: where a 20% voltage sag occurs under IH condition.

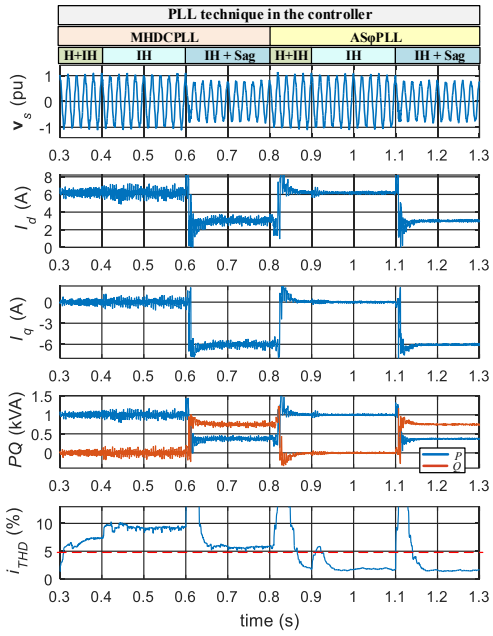

Fig. 14: Simulation results showing the effectiveness of accurate synchronization under distorted and faulty grid conditions. Note: The operation of RESS controller is based on MHDCPLL until 0.8 s and proposed ASφPLL is activated after 0.8 s.

The operation of grid-connected systems is depicted in Fig. 14 using the grid voltage vs, the dq-transformed fundamental currents $\mathbf{i}_{dq}$, the desired active/reactive power and the THD of injected current. From 0.3 s to 0.8 s, the MHDCPLL is in operation, whereas the proposed ASφPLL is activated for the rest of time. Clearly, under all the disturbances, the proposed PLL performs more accurately and enable the injection of high quality power and current. In contrast, the MHDCPLL, under voltage interharmonics, results in oscillations on the transformed currents, and in the active/reactive powers. Furthermore, the improved performance of the proposed PLL is clear from the THD of current, which is lower than the MHDCPLL and stays below 5% maximum limit allowed for such systems. Consequently, the ASφPLL is the most suitable candidate for grid-connected ESS to allow the flow of high quality power to and from DC bus under distorted and faulty grid conditions.

In order to further verify and demonstrate the accurate performance and significance of proposed PLL, its impact on the grid-connected storage system (Fig. 1) is validated using dSPACE DS1202. The injected *d* and *q*-axis currents and the active/reactive power flowing (to and/or from the grid) are important factors to investigate under faulty grid conditions. The performance of the proposed synchronization is validated in Fig. 15 where the grid voltage contains harmonic and interharmonic (5% of 5th and 7.2th each) and is also subjected to a 20% voltage sag (similar to simulation results). The proposed technique enables the injection of high quality power and current by accurately estimating the grid information (phase and frequency) under abnormal grid conditions, justifying in this way its positive impact on the power quality enhancement of overall grid-connected system.

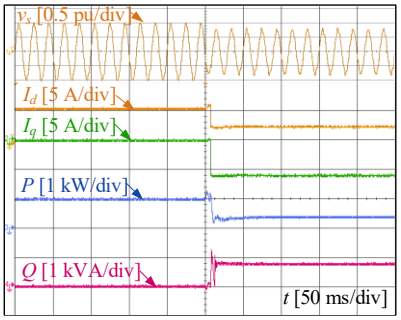

Fig. 15: Experimental validation of proposed technique for grid connected storage system under faults.

Hence, it is evident the proposed technique as most suitable candidate for grid connected energy storage systems under normal as well as abnormal grid conditions.

VII. Conclusions

This paper proposes a single-phase PLL technique able to work under harmonic, interharmonics, DC-offset and faulty grid conditions. The algorithm has lower complexity, resulting in fast and accurate estimation under grid frequency variations and presents a lower frequency overshoot. The effectiveness of the proposed PLL is validated by implementing it in the controller of grid-connected system, where it evidently improves the quality of injected current and power, and shows its superior performance and significant contribution towards the overall operation and stability of system. Consequently, the proposed ASφPLL is the most suitable candidate for grid-connected renewable and battery storage systems where it maintains the flow of high quality power under distorted and faulty grid conditions.

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