Received: 14 March 2021 | Revised: 29 July 2021 | Accepted: 1 August 2021

DOI: 10.1002/pip.3459

RESEARCH ARTICLE

PROGRESS IN PHOTOVOLTAICS WILEY

Firing stability of tube furnace-annealed n-type poly-Si on oxide junctions

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Funding information
Australian Center for Advanced Photovoltaics; Australian Renewable Energy Agency; Federal Ministry for Economic Affairs and Energy

[Correction added on 09 September 2021, after first online publication: the affiliation of Robby Peibst has been corrected in this version]

Abstract

Stability of the passivation quality of poly-Si on oxide junctions against the conventional mainstream high-temperature screen-print firing processes is highly desirable and also expected since the poly-Si on oxide preparation occurs at higher temperatures and for longer durations than firing. We measure recombination current densities (J_0) and interface state densities (D_{it}) of symmetrical samples with n-type poly-Si contacts before and after firing. Samples without a capping dielectric layer show a significant deterioration of the passivation quality during firing. The D_{it} values are (3 ± 0.2) × 10^{11} and (8 ± 2) × 10^{11} eV/cm^2 when fired at 620°C and 900°C, respectively. The activation energy in an Arrhenius fit of D_{it} versus the firing temperature is 0.30 ± 0.03 eV. This indicates that thermally induced desorption of hydrogen from Si—H bonds at the poly-Si/SiO_x interface is not the root cause of depassivation. Post-firing annealing at 425°C can improve the passivation again. Samples with SiN_x capping layers show an increase in J_0 up to about 100 fA/cm^2 by firing, which can be attributed to blistering and is not reversed by annealing at 425°C. On the other hand, blistering does not occur in poly-Si samples capped with AlO_x layers or AlO_x/SiN_y stacks, and J_0 values of 2–5 fA/cm^2 can be achieved after firing. Those findings suggest that a combination of two effects might be the root cause of the increase in J_0 and D_{it}: thermal stress at the SiO_z interface during firing and blistering. Blistering is presumed to occur when the hydrogen concentration in the capping layers exceeds a certain level.

KEYWORDS
blistering, firing, passivating contacts, passivation, POLO

1 | INTRODUCTION

Different passivating contact schemes are currently evaluated for application in highly efficient silicon solar cells. Here, the advantage of polycrystalline silicon on oxide (POLO) junctions[1–4] and related junction schemes[5–8] as compared to other candidates like a-Si:H/c-Si heterojunctions,[9,10] transition metal oxides[11,12] or organic materials,[13] is their high level of thermal stability, which is derived from the high preparation temperature of POLO junctions. A high level of thermal stability implies potential compatibility with conventional mainstream

high-temperature screen-print metallization.[14] Screen-printed contacts hold more than 90% of PV metallization market share and require a short high-temperature "firing" step.[15] To implement POLO contacts in today's mass production, compatibility to a firing step is mandatory.[16]

The POLO contacts are formed at temperatures between 800°C and up to 1050°C and yield high passivation qualities.[17–20] The firing process performed after screen printing is a fast high-temperature process, typically done between 700°C and 900°C. Several groups reported on the degradation of the passivation quality in the metallized regions and also on nonmetalized regions for n-type poly-Si after such processes.[14,21,22] A significant amount of work has been done on the optimization of metal pastes and firing conditions to mitigate the former issue and to avoid the penetration of the metal through the poly-Si layer.[23] The effect of the firing on the nonmetalized regions is also receiving increasing research interest.[21,24,25] In the nonmetalized regions, no issues are expected, since the thermal budget of the previously performed junction formation process is much higher than that of the firing step, that is, the total amount of thermal energy transferred to the wafer during firing is substantially lower than that of the POLO formation process. However, previous works demonstrated that firing can indeed have a negative impact on the passivation of nonmetalized regions of n-type and p-type LPCVD and PECVD poly-Si contacts.[21,22,24,25] The reason for this degradation is not yet clear and must be understood.

We suggest that a crucial point here is the rate of temperature change during high-temperature processes. The formation of the POLO contacts is performed in a quartz tube furnace. This process applies a 10 K/min heating rate from the drive-in temperature of 700°C to the peak temperature and a plateau phase of 30 to 60 min which is followed by a 5 K/min cooldown to 725°C, after which the samples are unloaded from the tube furnace. The firing process is performed in a belt furnace where the wafer temperature changes by up to 100 K/s during heating and cooling, depending on set peak firing temperature and belt speed. In this investigation, we vary the set peak firing temperature between 620°C and 900°C using a typical industrial firing profile.

The hypothesis is that the mechanical stresses at the interface due to the difference in thermal expansion coefficients between the c-Si, oxide, and poly-Si layers (c-Si: 2.6–4.3 $\times$ 10^{-6}/K between room temperature and 900°C,[26] thermal oxide 0.5 $\times$ 10^{-6}/K,[27,28] and poly-Si 2.7 to 2.9 $\times$ 10^{-6}/K at room temperature[29,30]) are much higher during the firing process than during the tube furnace annealing. Reorganization processes like viscous flow are suppressed due to the high rate of temperature change and the short process time during firing. This stress could lead to a reduced defect formation energy at the interface, and thus, an increased density of defect states in the bandgap at the SiO_z/c-Si interface can be explained.

Previous studies on fired, SiN_y-capped poly-Si on oxide junctions already implemented a countermeasure against an increasing J_0, that is, the passivation of these defects by hydrogenation.[21,31–33] However, by analyzing secondary-ion mass spectrometry (SIMS) measurements, it turned out that the solution is not simply the introduction of as much hydrogen as possible,[34] but that there were significant differences between the different dielectric layers investigated. Good passivation after the firing of p-type poly-Si on a textured surface has been demonstrated with a stack of AlO_x and SiN_y layers by van de Loo et al.[31] reaching iV_{oc} values of about 712 mV.

We speculate that the chemical configuration at the crystalline Si interface changes, and some Si—O and Si—Si bonds convert to Si—H bonds. If this hypothesis holds, possible implications on the long-term stability of the passivation quality cannot be excluded. The aim of this work is therefore to understand the effects of firing on the Si/SiO_z interface in POLO junctions.

2 | EXPERIMENTAL DETAILS

2.1 | Sample preparation

To test these hypotheses on the importance of the temperature ramp rates and the amount of hydrogen at the interface, we prepare symmetric test samples on p-type (boron-doped) Cz, 20-Ω cm material. All samples go through a KOH-based saw damage removal process and an RCA cleaning sequence. We apply two different interfacial oxides (see Figure 1 for the full split plan). For the lifetime analysis, the samples have an ∼1.5-nm-thick oxide layer deposited by a wet chemical process using ozone. For the capacitance–voltage (*C*–*V*) analysis, other samples have a 10-nm thermally grown oxide layer. This is necessary to suppress leakage currents through the oxide and thus enable the investigation of the interface by *C*–*V* measurements. The oxide is subsequently capped by a 220-nm-thick low-pressure chemical vapor deposited (LPCVD) a-Si layer with in situ n-type doping. After the poly-Si deposition, the samples are annealed in a tube furnace for 30 min. The samples with a thermal oxide were annealed at 880°C. The samples with wet chemical interfacial oxide are processed in two different batches and are annealed at either 820°C or 860°C, as indicated in the respective results figure captions below. Subsequently, a gettering step is performed for 1 h at 550°C in N_2 atmosphere independently of the previous annealing temperature. We then remove the oxide grown on the poly-Si by 40% HF etch, which leads to a poly-Si thickness of about 140 nm.

Some of the samples are subsequently coated with a 100-nm-thick SiN_y layer with a refractive index of $n = 2.05$ from two different tools. The first is a microwave-assisted plasma-enhanced chemical vapor deposition (MA-PECVD) tool, and the second is an inductively coupled plasma (IC-PECVD) tool. Another split receives a 10-nm-thick atomic layer deposited (ALD) AlO_x layer coating and is subsequently annealed at 425°C for 30 min in N_2 atmosphere. An additional split of the samples receives a stack of 10-nm AlO_x plus 100-nm SiN_y from the IC-PECVD tool. Between the AlO_x and the SiN_y deposition, these samples are annealed (425°C, 30 min, N_2). The above-described sample splits were processed in three different batches.

The subsequent firing takes place in an industrial infrared conveyor-belt furnace using a typical temperature profile for the firing of metallization pastes at different set peak temperatures between

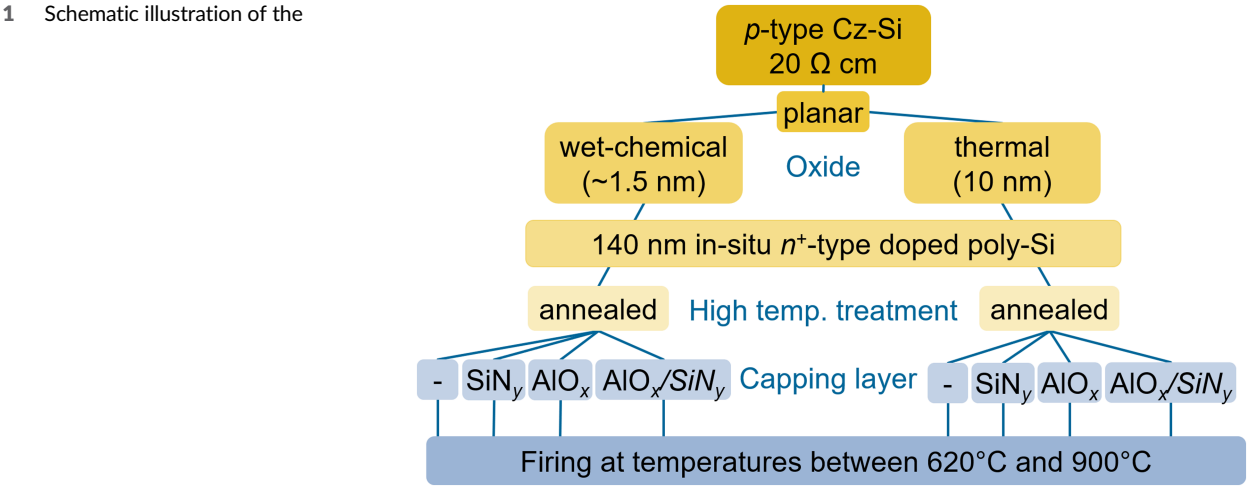

FIGURE 1 Schematic illustration of the split plan

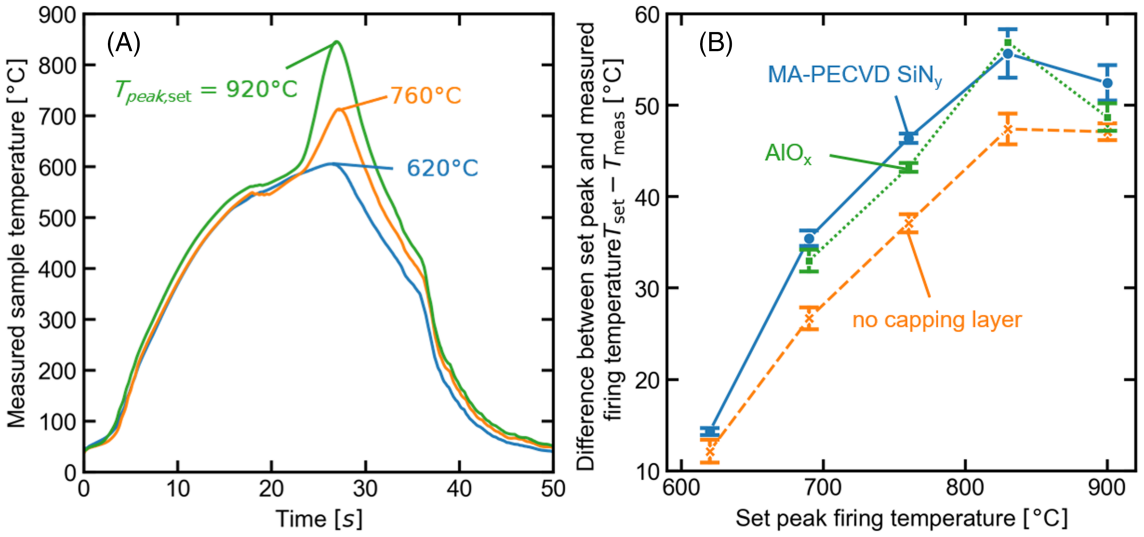

FIGURE 2 (A) Measured surface temperature profiles during firing of samples without a capping layer. The temperature is tracked using a DATAPAQ Insight Oven Tracker. (B) Difference between the set and the measured peak temperatures and dependence of the set peak temperature for samples with different capping layers

620°C and 900°C and a conveyor-belt speed of 5.6 m/min (see Figure 2A). The actual measured peak temperatures are lower than the set peak temperatures, as can be seen in Figure 2B. The difference increases from 15°C to about 55°C with increasing set temperature for the samples capped with AlO_x or SiN_y and from 12°C to 45°C for uncapped samples. In another experiment, we keep the measured peak temperature constant at 860 ± 5°C (equivalent to 900°C set temperature) while varying the conveyor-belt speed between 2.5 and 7.2 m/min.

For the preparation of samples dedicated for the C–V measurements, existing dielectric layers are removed in a 40% HF solution, and a full area aluminum layer is evaporated on the rear side. The front side is only locally metalized with thermally evaporated aluminum by using a mask with circular pads with an area of about 0.01 cm^2. Finally, laser-fired contacts[35] (LFCs) are formed through the poly-Si and SiO_z to the base material to ensure an ohmic rear side contact. Subsequently, the POLO stack between the pads on the front is removed by reactive ion etching. Figure 3 schematically shows the structure of these samples. The masked evaporation technique leads to a slightly ill-defined area of the pads. Therefore, to crosscheck on the actual sizes of the pads on some selected samples, additional test structures were processed with pads of two different sizes (9×10^{-4} and 2.4×10^{-4} cm^2) defined by photolithography to assure precise edges.

2.2 | Characterization

The stability of the samples with respect to the firing process is quantified on the basis of photoconductance decay (PCD) measurements with a Sinton lifetime tester.[36] We determine the J_0 by the Kane–Swanson method[37] and the Auger parametrization of Richter et al.[38]

The charge carrier density at which the J_0 is extracted varies between 2.5×10^{15} and 8×10^{15} cm^{-3}. Unless stated otherwise, all data points contain the data of two different full wafer samples measured at five different positions on the wafer.

We perform C–V measurements to determine the density D_{it} and the energy level E_{it} of interfacial traps. This enables a distinction between chemical passivation and passivation due to band bending. C–V measurements were carried out on samples with a thick oxide by applying the conductance method[39] using a Cascade probe station equipped with an Agilent 4294A Impedance analyzer. On every sample, at least two pads were measured.

The measurement frequencies are set to a range from 0.5 to 500 kHz while the DC bias voltage sweeps from accumulation to inversion. In accumulation, strong deviations between the capacitances occur with increasing frequency, although a constant value corresponding to the gate oxide capacitance is to be expected for all frequencies. This behavior suggests that a two-element equivalent circuit model is not appropriate to extract the capacitance from the measured impedance. The measurements are affected by additional effects, most likely by a series resistance, R_s, as a third element. A method to determine the series resistance by including the substrate resistance in the equivalent circuit of MOS capacitors has been proposed by Nicollian and Brews,[40] which is followed by a correction of the measured capacitance and conductance using the determined R_s. We apply this method to all data sets. Figure 4A shows the equivalent circuit model while Figure 4B presents the C–V curves, calculated with the three elements (capacitance, parallel conductance, and series resistance) from the measured impedance.

The conductance technique we use to find the energy levels of the interface traps works based on the loss resulting from changes in their occupancy (capture and emission of charge carriers) due to changes in the applied gate bias.[39] Those changes in occupancy cause energy losses leading to a parallel conductance given by

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2}, \quad (1)$$

where C_{ox} is the oxide capacitance, C_c is the corrected capacitance, G_c is the corrected conductance, G_p is the parallel conductance, and ω is the angular frequency according to the equivalent circuit (see Figure 4A) used by Nicollian and Goetzberger.[39] From the peak of this function (see Figure 4C), the interface state density at one energetic position for each gate voltage can be deduced. Thus, to determine the interface state density D_{it}, further G_p/ω measurements with varied frequencies (from 0.5 to 500 kHz) for different fixed gate voltages in depletion and weak inversion (−0.6 to −0.9 V) are performed.

The following equation is used to calculate the D_{it}[40]:

$$D_{it} = (qAf_D(\sigma_s))^{-1} \left[\frac{G_p}{\omega}\right]_{peak}, \quad (2)$$

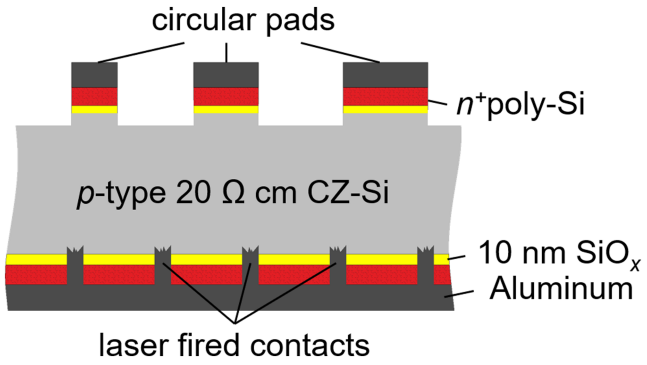

FIGURE 3 Schematic illustration of samples prepared for C–V measurements

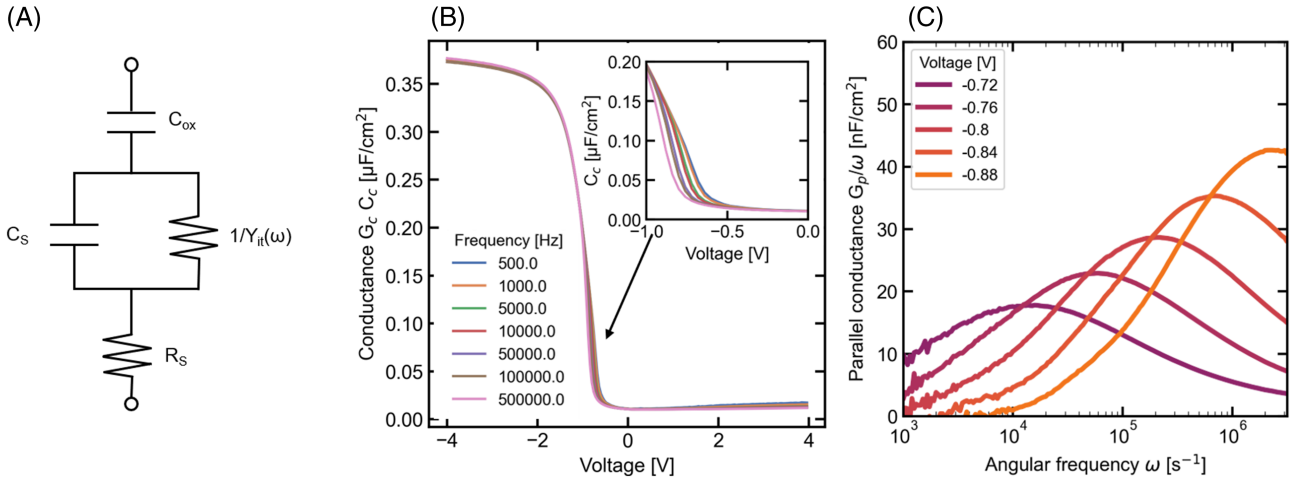

FIGURE 4 (A) Equivalent circuit of a MOS capacitor. (B) Capacitance voltage curves calculated by the three-element equivalent circuit model from measured impedances. The inset shows a zoomed section of depletion and weak inversion where the capacitive contribution of the interface states is visible. (C) Representative parallel conductance curves in dependence of the angular frequency

where A is the contact area and f_D is a correction factor accounting for the effect of spatial fluctuations of surface charges. This behavior is described by a Gaussian distribution with standard deviation σ_s around the mean value of surface potential, Ψ_s. To calculate the correction factor f_D, the standard deviation σ_s of the G_p/ω curve is needed. Instead of a direct determination via a Gaussian fit, f_D is deduced from the ratio of the G_p/ω values at the peak frequency ω_{peak} and its multiplications ($n \times \omega_{peak}$), where n is chosen to be 5 or 1/5 as proposed by Nicollian and Goetzberger[39,41] and such that $n \times \omega_{peak}$ is within the reliable measurement range. The function $f_D(\sigma_s)$ is calculated numerically,[40] and for realistic values of σ_s, it has values between 0.15 and 0.35.

We determine the Ψ_s–V_G relationship to obtain the position of the Fermi level in each operational point V_G, which gives the position of the interface traps in the bandgap. For this, the high-frequency method developed by Terman[42] is used as described by Nicollian and Brews.[40] We conduct the capacitance measurements described above at high enough values so that the interface traps do not follow the AC gate voltage. The capacitance at high-frequency C_{HF} can thus be described by

$$C_{HF} = \frac{C_D C_{ox}}{C_D + C_{ox}}, \quad (3)$$

where C_D is the depletion layer capacitance. The only influence interface traps have on the C–V curve is a stretch-out along the gate bias axis.[40] This stretch-out $d\Psi_s/dV_G$ is quantified by a comparison between the measured and the ideal C–V curve without interface traps calculated from theory[40] using the same doping density and oxide thickness.

Due to high leakage currents, this method cannot be applied to the samples with a thin and thus leaky oxide. Since we verified that the behavior upon firing is qualitatively similar for both sample groups, we assume that the relative change of D_{it} upon firing is representative also for the samples with thin interfacial oxide.

3 | RESULTS

3.1 | Firing stability of plain POLO contacts with different oxides

Figure 5 shows the recombination current density of samples before and after a firing process at different set peak temperatures with (A) an ~1.5-nm-thin wet chemical interfacial oxide and (B) a 10-nm-thick thermal grown oxide. The samples were neither capped by a dielectric layer nor hydrogenated by a forming gas anneal. The different oxide types already show an impact on the initial J_0 values after annealing (blue lines). While the samples with thin wet chemical oxide achieve acceptable J_0 values of about 8 fA/cm^2, the passivation quality of the samples with the thermal oxide with a J_0 between 20 and 40 fA/cm^2 is not optimal. An explanation for this might be the significantly reduced in-diffusion of P into the wafer through the thicker oxide that is seen in electrochemical capacitance–voltage (ECV) measurements in Figure 6. The strong in-diffusion in the case of a thinner oxide in turn is leading to a further reduced minority carrier density at the interface, improving the surface passivation. Here, the field-effect passivation exceeds the increase in J_0 due to increased Auger recombination due to the in-diffusion.

Although the samples with both oxides show a negative influence of firing on the passivation quality, the effect looks different in detail.

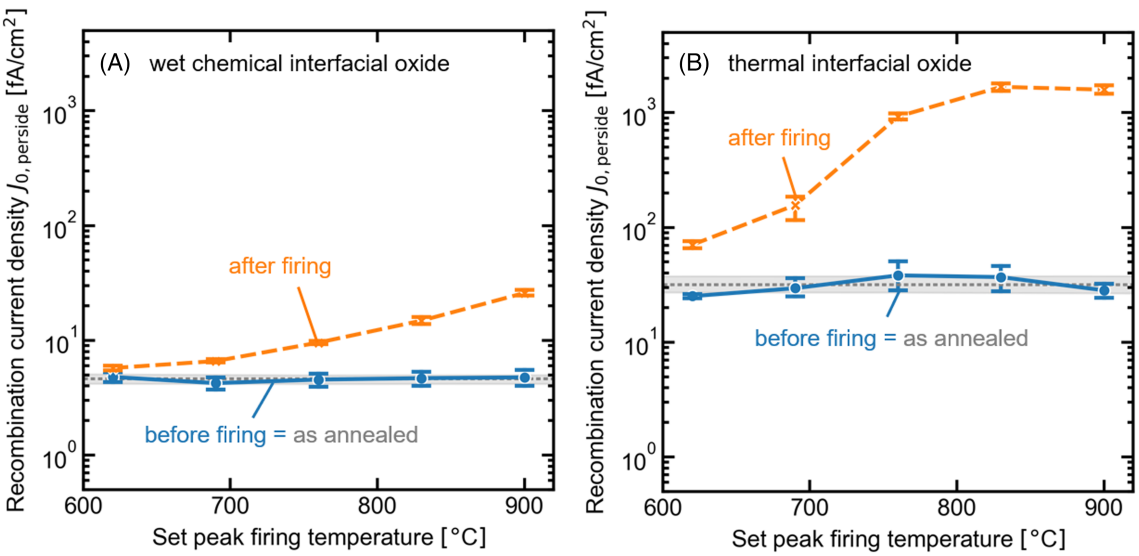

FIGURE 5 Recombination current density, J_0, of (A) samples with an ~1.5-nm wet chemical oxide, annealed at 860°C, and (B) a 10-nm-thick thermal oxide, annealed at 880°C. Blue data points are measured before firing, and orange data points are measured after firing. The gray interval depicts the results directly after annealing measured on other samples from the same batch (upper/lower quartile)

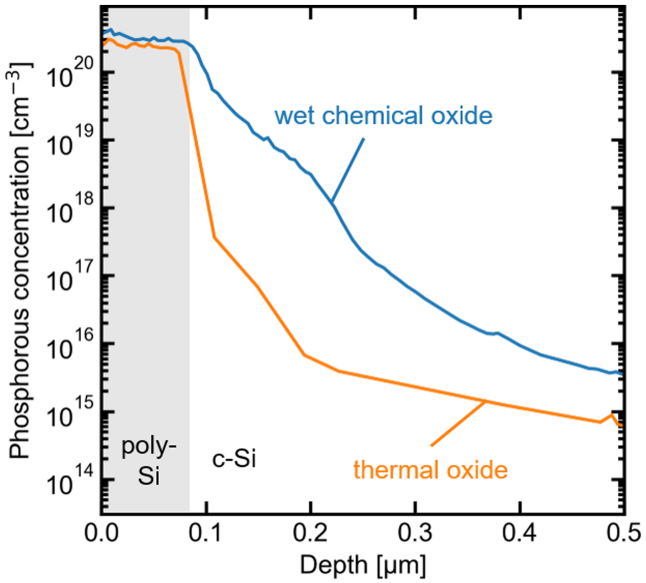

FIGURE 6 ECV profile measurements of n^+-type POLO samples with an ~1.5-nm-thin wet chemical interfacial oxide annealed at 860°C and an ~10-nm-thick thermal oxide annealed at 880°C

For the wet chemical oxide, starting from a temperature of 690°C, the results after the firing process show an almost exponential increase in J_0 with a rising set peak firing temperature. The samples with a 10 nm and thermally grown oxide show an even greater relative and absolute increase of J_0 with rising temperature than the samples with a wet chemical oxide. Between 760°C and 900°C, the J_0 remains almost constant at about 1600 fA/cm^2. The J_0 results after firing of these and subsequent split groups can also be seen in Table 1.

Altogether, these measurements show that our fast-firing process yields an increase of at least 1 order of magnitude in the recombination current density of n^+-type POLO junctions for both interfacial oxides.

In a further experiment, we investigate the influence of the temperature change rate on the firing stability by varying the belt speed. For all speeds, we adjust the measured peak temperature to 860 ± 5°C. This is the peak temperature that we measure for $T_{peak,set} = 900$°C and a belt speed of 5.6 m/min.

Figure 7 shows the results of the PCD measurements. The measured data from the center of the wafer is shown in green. Other positions are also shown because of the spatial inhomogeneities across the wafer. Figure 7A shows that the lifetime decreases by 0.15–0.51 ms with increasing belt speed from 2.5 to 7.2 m/min. Figure 7B shows that the iV_{oc} decreases by 10–35 mV, and in Figure 7C, the J_0 values increase by about 30–-220 fA/cm^2. The positions on the wafer (red and yellow) with the lowest initial lifetimes show by far the strongest deterioration of the surface passivation, while the effective lifetime is only influenced slightly. This is probably the case because in the range of higher lifetimes, a change in surface passivation has a significantly greater effect on the lifetime than in the case of low lifetimes with an already poor passivation quality since the J_0 contributes to the lifetime with $1/J_0$.

3.2 | Impact of different hydrogen-containing capping layers

In a further experiment, we study samples that are coated with SiN_y and/or AlO_x to investigate the impact of hydrogen-containing capping layers on the firing stability.

SiN_y capping layer

Figure 8A shows the recombination current densities of n^+-type POLO samples with POLO junctions based on a wet chemical oxide, coated with 100-nm silicon nitride with a refractive index of $n = 2.05$ from an IC-PECVD tool. The state before firing (denoted as "IC-PECVD SiN_y") was measured after the deposition of SiN_y. A comparison to the state after annealing/before SiN_y deposition (gray dashed line) reveals that the deposition of SiN_y in this tool only leads to a minor improvement of passivation quality. However, firing at low temperatures up to 760°C yields a clear decrease in J_0. Firing at $T_{set} = 620$°C leads to an even stronger improvement down to J_0 of below 1 fA/cm^2 on the best sample. These samples show an iV_{oc} of 745 mV and an effective lifetime of 8 ms. However, firing with set peak temperatures in the range from 760°C to 900°C, where typical industrial firing processes take place, leads to a drastic increase in J_0 to up to 100 fA/cm^2.

The scanning electron microscope (SEM) image in Figure 9A,C reveals blister formation, which we believe is the reason for an increase in J_0. Figure 9B shows that the poly-Si detaches from the sample surface together with the SiN_y layer. Figure 9C even shows a large piece of the POLO junction with a size of about 10 µm^2 flaking off. Since the detachment is not only seen at the wafer edge but also on the surface as shown Figure 9C and on many others taken, a detachment due to cleaving can be excluded.

Further samples are coated with a 100-nm-thick SiN_y layer with $n = 2.05$ from a MA-PECVD tool. Those results are shown in Figure 8B. Here, it can be seen from the J_0 values before firing that already the deposition of the SiN_y layer leads to a significant improvement in the passivation of the surface with J_0 values of about 2 to 3 fA/cm^2. This could be due to a higher deposition temperature of 500°C in the MA-PECVD tool as compared to the IC-PECVD tool with a deposition temperature of approximately 300°C.

However, already at low firing temperatures, there is a deterioration of J_0. At $T_{set} = 900$°C, the J_0 reaches 14 ± 9 fA/cm^2 and thus exceeds the values measured after annealing of about 5 fA/cm^2. As opposed to the previous group coated with SiN_y from the IC-PECVD tool, optical microscope and SEM images of these samples show no visible sign of blistering or interface detachment. By Fourier-transform infrared spectroscopy (FTIR) measurements (in the Supporting Information), we determined that the IC-PECVD films contain significantly

TABLE 1 Summary of recombination current densities of different splits

Interfacial oxide type	Oxide thickness (nm)	Annealing temperature (°C)	Capping layer	SiN_y deposition tool	Firing temperature (°C)	Recombination current density (fA/cm^2)
Wet chemical	1.5	860	-	-	620	5.7 ± 0.5
					690	6.6 ± 0.4
					760	9.6 ± 0.5
					830	15 ± 2
					900	26 ± 3
Thermal	10	880	-	-	620	71 ± 7
					690	160 ± 60
					760	930 ± 90
					830	1700 ± 300
					900	1600 ± 300
Wet chemical	1.5	820	SiN_y	MA-PECVD	620	4 ± 2
					760	4 ± 2
					900	14 ± 9
Wet chemical	1.5	820	SiN_y	IC-PECVD	620	2 ± 2
					690	3 ± 2
					760	3 ± 2
					830	39 ± 9
					900	110 ± 40
Wet chemical	1.5	860	AlO_x	-	620	3 ± 2
					690	3 ± 3
					760	4 ± 3
					830	6 ± 4
					900	7 ± 4
Thermal	10	880	AlO_x	-	620	9 ± 3
					690	10 ± 2
					760	9 ± 1
					830	10 ± 1
					900	14 ± 2
Wet chemical	1.5	860	AlO_x/SiN_y	IC-PECVD	620	2 ± 1
					760	2 ± 1
					900	3 ± 1
Thermal	10	880	AlO_x/SiN_y	IC-PECVD	620	6 ± 2
					760	8 ± 3
					900	20 ± 4

more hydrogen after deposition than the MA-PECVD films. This could be one reason why blistering only occurs on the IC-PECVD samples.

AlO_x capping layer

Figure 10A,B shows the recombination current density of samples that are coated with ALD AlO_x and annealed at 425°C for 30 min in N_2 atmosphere before being fired. The state "before firing" in this case includes an AlO_x deposition plus the annealing process (425°C, 30 min, N_2). The interfacial oxide of the samples shown is thin wet chemical oxide in Figure 10A and thick thermal oxide in Figure 10B.

Comparing the states "before firing" and "after firing" in Figure 10A, they show relatively small differences. Only after firing at $T_{set} = 900$°C, a moderate increase from 4 to 7 ± 4 fA/cm^2 is measured (see Figure 10A).

In Figure 10B, it becomes clear that in contrast to the wet chemical oxide, the deposition of AlO_x plus annealing results in a significant improvement of J_0 from approx. 30 to 2–5 fA/cm^2. It seems that the

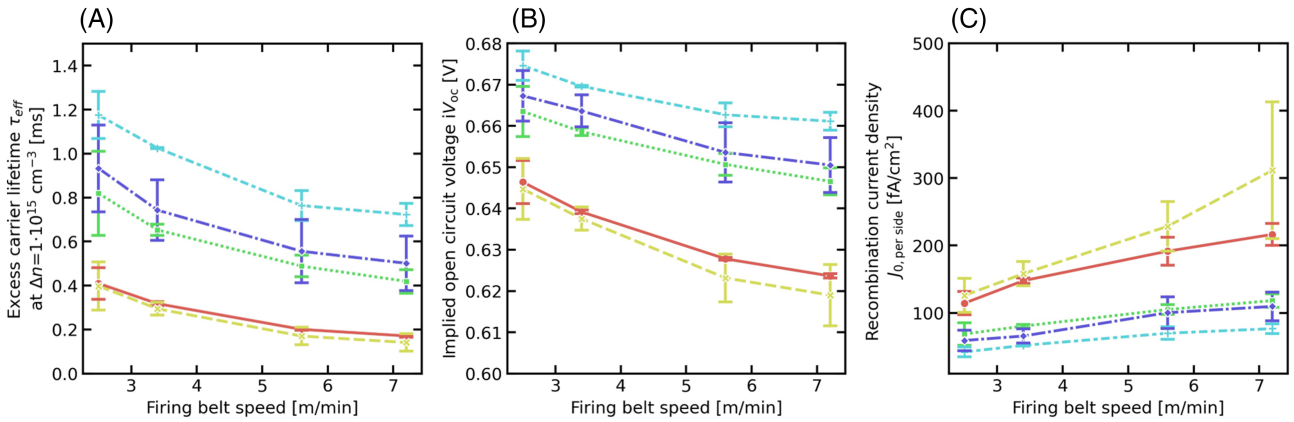

FIGURE 7 (A) Excess carrier lifetime, (B) implied V_{oc}, and (C) recombination current density J_0 in dependence of the conveyor-belt speed for samples with an ~ 1.5-nm wet chemical oxide, annealed at 820°C, that were fired at an actual peak temperature of 860 ± 5°C. The different colors show measurement results at five different positions on the wafers

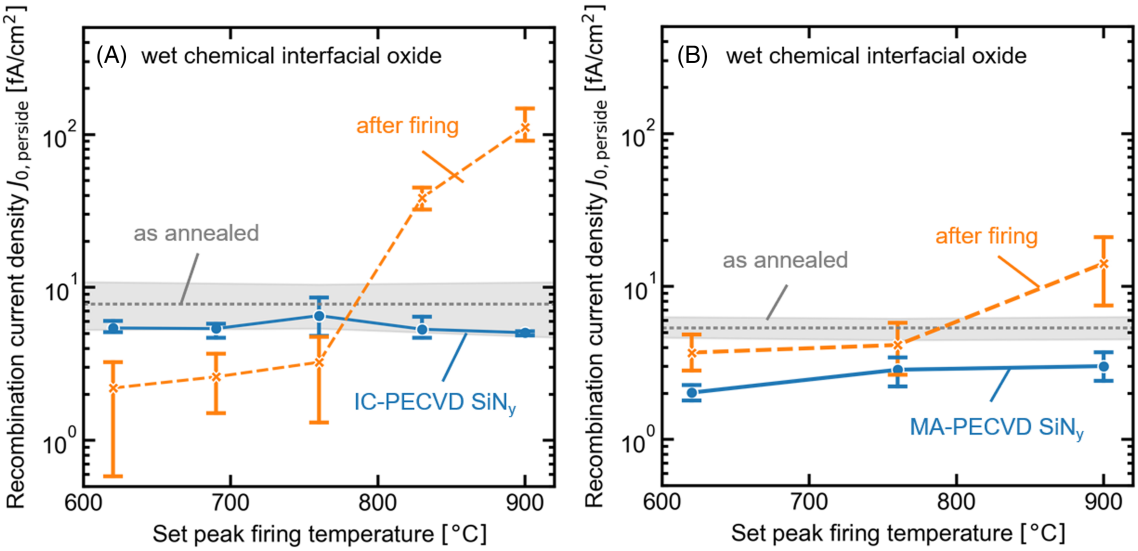

FIGURE 8 Recombination current density J_0 of samples with wet chemical interfacial oxide, annealed at 820°C, and (A) a 100-nm (IC-PECVD) SiN_y capping layer and (B) a 100-nm (MA-PECVD) SiN_y capping layer. The results in (B) are each obtained from two small samples only measured at one position. Blue data points are measured before firing, and orange data points are measured after firing. The gray interval depicts the results directly after annealing measured on other samples from the same batch (upper/lower quartile)

surface passivation has improved more for these samples upon hydrogenation. An explanation could be that the surface recombination in these samples is more sensitive to the chemical passivation due to the absence of an in-diffusion of dopants from the poly-Si layer and due to a reduction of the band bending in the Si due to the increased voltage drop across the thicker interfacial oxide. Firing, even at 620°C, again causes a deterioration in surface passivation quality to about 9 ± 3 fA/cm^2. However, this value remains constant up to 830°C and only increases to 14 ± 2 fA/cm^2 at 900°C. Altogether, it can be said that AlO_x also provides a significant improvement in the firing stability for samples with thermal oxide, although the improvement previously achieved by deposition and annealing is not maintained. Optical microscope images of these samples do not show any sign of blistering.

AlO_x/SiN_y stack

The J_0 values of samples coated with a stack of AlO_x and SiN_y layers are shown in Figure 11A,B. The AlO_x deposition is followed by an

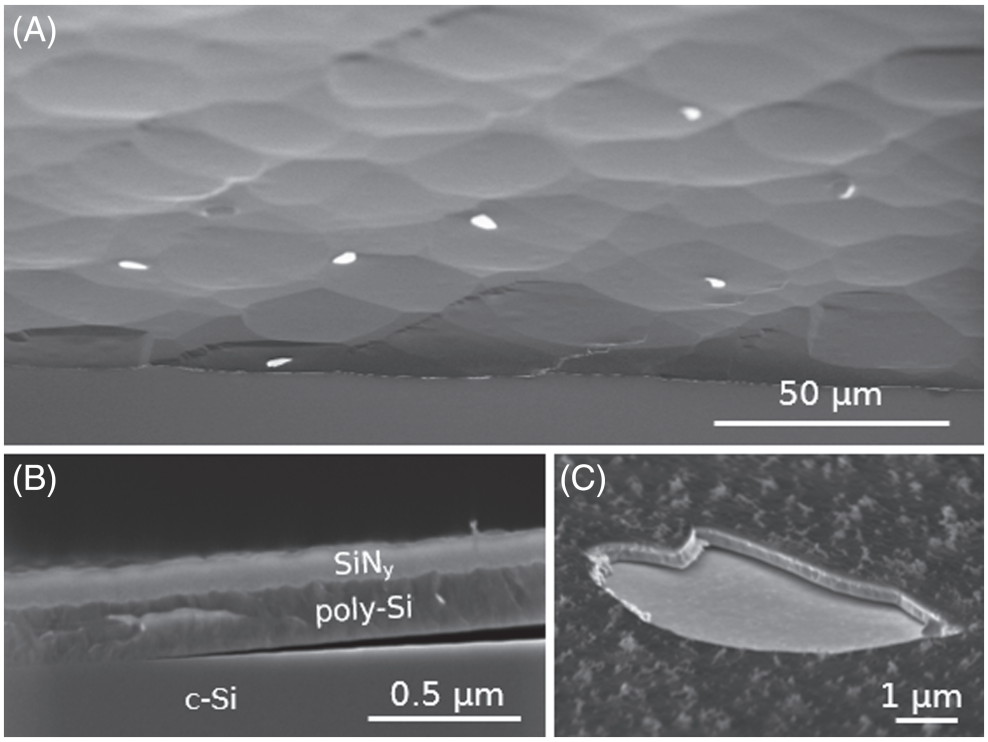

FIGURE 9 SEM images of poly-Si sample with wet chemical interfacial oxide and an IC-PECVD SiN_y capping layer fired at 900°C

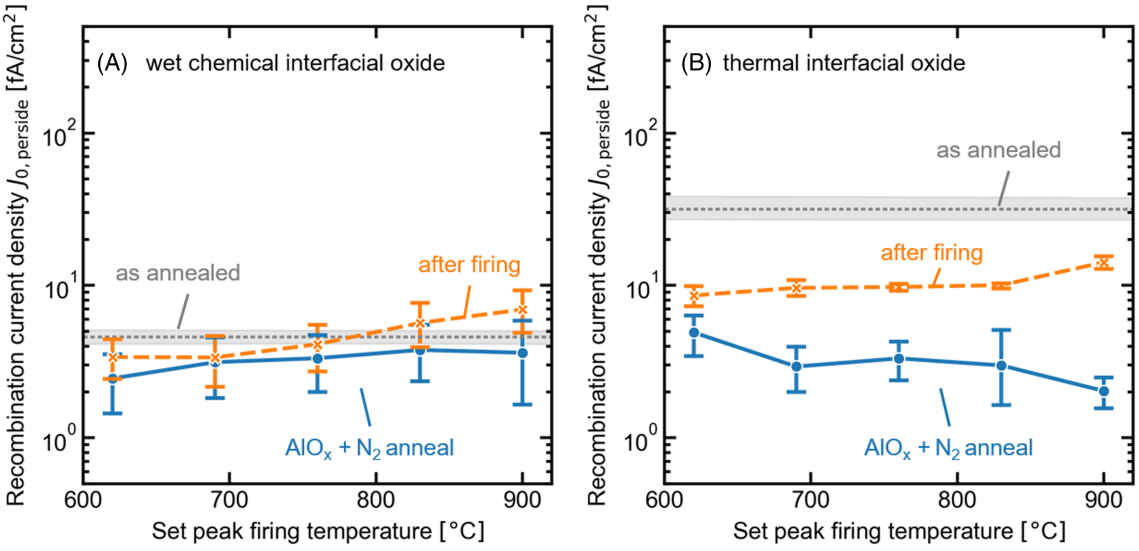

FIGURE 10 Recombination current density J_0 of samples with (A) a wet chemical interfacial oxide, annealed at 860°C, and (B) a thermal oxide, annealed at 880°C coated with a 10-nm AlO_x layer. Blue data points are measured before firing, and orange data points are measured after firing. The gray interval depicts the results directly after annealing measured on other samples from the same batch (upper/lower quartile)

annealing process (425°C, 30 min, N_2). Subsequently, a 100-µm-thick IC-PECVD SiN_y layer is deposited. The results in Figure 11A show that POLO junctions with a thin wet chemical oxide, which are capped with this stack, first of all, provide a very good passivation quality of $J_0 = 0.8–2.5$ fA/cm² before firing and thus significantly improves the passivation quality compared to 4 fA/cm² before the AlO_x/SiN_y layer deposition. The firing process causes a slight deterioration which increases with increasing firing temperature but which remains below 4 fA/cm² even at 900°C. Both optical microscope images and the good J_0 values speak for the fact that blisters do not occur with this stack.

The samples with a thick thermal oxide in Figure 11B show a very similar behavior qualitatively, on a higher J_0 level. After firing at 900°C, J_0 values of about 20 fA/cm² are measured.

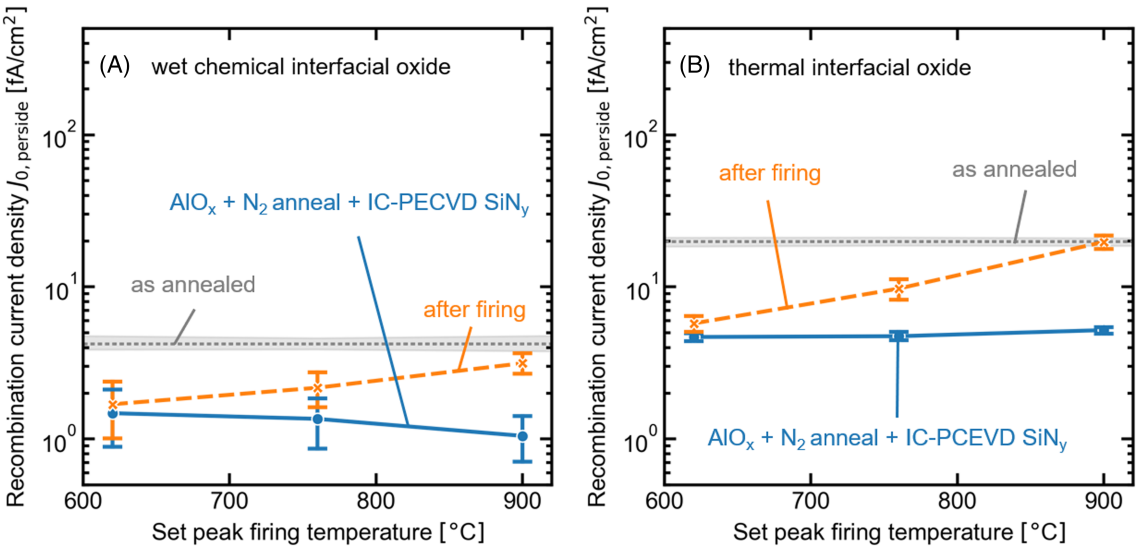

FIGURE 11 Recombination current density of samples (A) with thin wet chemical oxide, annealed at 860°C, and (B) with thermal oxide, annealed at 880°C capped with an AlO_x/SiN_y stack measured before and after firing. Blue data points are measured before firing, and orange data points are measured after firing. The gray interval depicts the results directly after annealing measured on other samples from the same batch (upper/lower quartile)

3.3 | Postfiring annealing

Figure 12 shows the results of an experiment to investigate the impact of the recombination current density on a postfiring annealing process (425°C, 30 min, N_2). It turns out that for samples with a wet chemical interfacial oxide that were fired without a capping layer the postfiring annealing—which does not introduce any hydrogen—is able to reduce the J_0 significantly from about 200 to 10 fA/cm^2, reaching almost the state before firing (6 fA/cm^2). Interestingly, in the case of the IC-PECVD SiN_y, the degradation of the passivation is obviously irreversible due to the strong blistering. But also, for the MA-PECVD-SiN_y samples without visible evidence for blisters, the passivation cannot be recovered by the postfiring anneal.

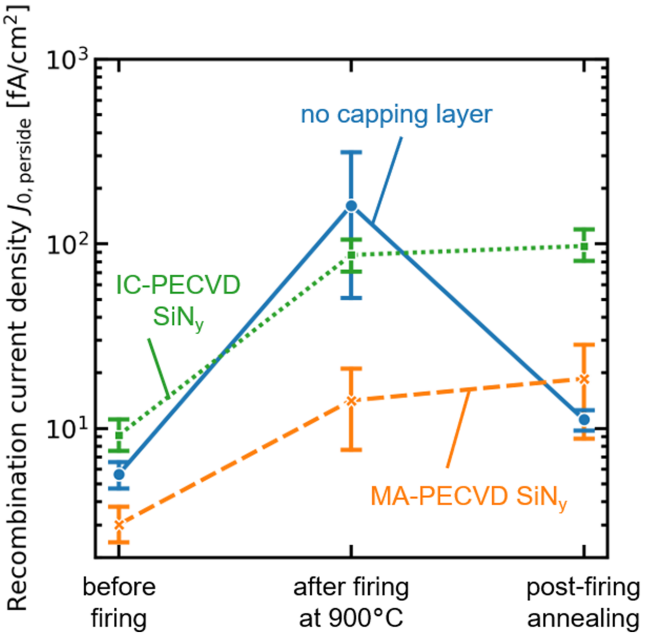

FIGURE 12 Recombination current density J_0 of samples with a thin wet chemical interfacial oxide, annealed at 820°C and with different capping layers measured in consecutive process steps. The samples were first measured directly before firing again after firing at a set peak firing temperature of 900°C and finally after a subsequent annealing process at 425°C for 30 min in N_2 atmosphere. The error bars denote the 95% confidence interval of five measurements on different parts of two wafers, respectively

3.4 | Interface state density

Using capacitance–voltage measurements and applying the conductance method, we determine the interface state density D_{it} of selected samples. As this method does not tolerate leakage currents through the oxide, all samples analyzed with this method contain a 10-nm-thick thermal oxide. The parallel conductance G_p/ω as a function of angular frequency ω for different gate voltages is shown in Figure 13 for samples fired without a capping layer. The different peaks measured at different applied gate voltages indicate different energetic positions in the bandgap (E–E_v). The height of the peaks increases with increasing D_{it}. Thus, it is already evident here that with increasing firing temperature, there is an increase in the defect density at the interface.

Figure 14 shows the D_{it} values plotted over the set peak firing temperatures for different split groups. The D_{it} values of the sample fired without a capping layer rise from 7.5 × 10^{10} eV/cm^2 before firing to 3 × 10^{11} eV/cm^2 when fired at 620°C and to 1 × 10^{12} eV/cm^2 when fired at 900°C.

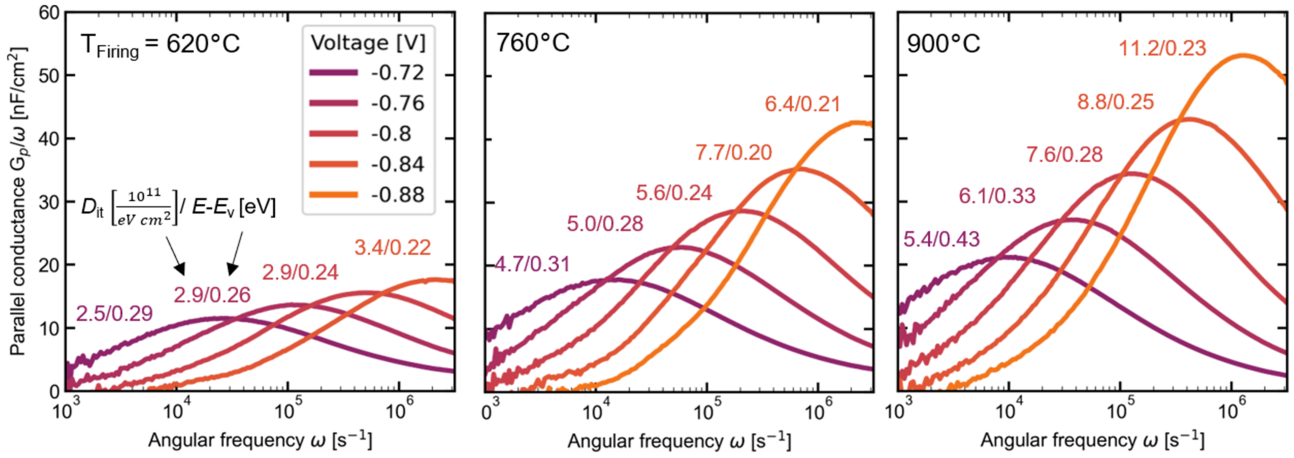

FIGURE 13 Parallel conductance G_p/ω as a function of angular frequency ω for different gate voltages. The D_{it} and the E–E_v values are also given inside the plots. The samples are fired at three different temperatures

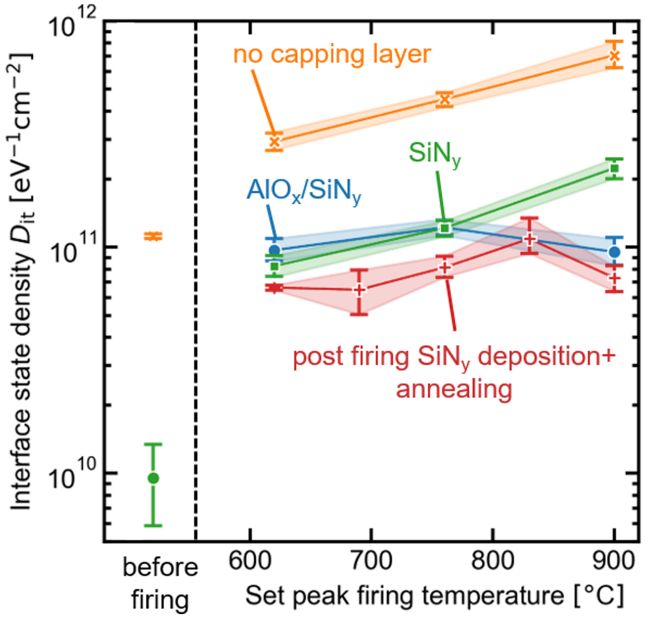

FIGURE 14 Interface state density as a function of firing set peak temperature. The wafers that received a post firing treatment was previously fired without a capping layer

A postfiring treatment with SiN_y plus an annealing step (425°C, 30 min, N_2) of further samples that were previously fired without a capping layer achieve a significantly lower and also relatively constant D_{it} of about $8 \pm 2 \times 10^{10}$ eV/cm^2.

For the group with SiN_y capping, one sample was measured before firing and showed a D_{it} of $9 \pm 3 \times 10^9$ eV/cm^2. Comparison to literature shows that this is an excellent value.[43–45] Comparing this to the results after firing gives a strong increase in D_{it} during firing. The fired samples show D_{it} values of about 1.1×10^{11} eV/cm^2 when being fired at 620°C and a slightly higher value for samples fired at 760°C. However, the samples fired at 900°C show a significant increase up to 2×10^{11} eV/cm^2, which fits the J_0 results and the occurring blisters. The samples, which received a stack of AlO_x and SiN_y before firing, show a D_{it} of about $1 \pm 0.3 \times 10^{11}$ eV/cm^2, which remains almost constant over the whole temperature range for firing and therefore follows the J_0 results of the samples with wet chemical oxide.

The D_{it} results of the samples fired without a capping layer seem to be exponentially dependent on the set peak firing temperature. This finding supports the hypothesis that the limiting process is thermally activated and can therefore be modeled by rate theory. Regarding the samples fired without a capping layer one possible process happening during firing could be pure temperature-induced desorption of hydrogen. The rate theory is described by the following equation

$$\frac{\partial N_{it}}{\partial t} = k(N_0 - N_{it}(t)), \tag{4}$$

where k is the interface trap generation rate. N_0 is the number of initially "passivated" inactive species at the interface, for example, Si—H bonds, and $N_{it}(t)$ is the number of electrically active interface states, for example, dangling Si bonds.

Regarding a hydrogen desorption process, for this equation, the assumption is made that the amount of free hydrogen at the interface and in the poly-Si is very low, which we think is given due to the previous high-temperature annealing process. Thus, we can assume that this process is only limited by the forward reaction, the breaking of Si—H bonds.

We moreover assume that the amount of broken Si—H bonds ($N_{it}(t)$), at the interface, stays small in comparison to the bonds initially passivated N_0. This results in the following equation:

$$\frac{\partial N_{it}}{\partial t} \approx k \times N_0. \tag{5}$$

For a defined annealing time t, as provided by a firing process, the equation can be written as

$$N_{it} = k \times N_0 \times t. \quad (6)$$

The rate of this thermally activated process can be described by the Arrhenius equation:

$$k = A \times \exp\left(-\frac{E_A}{k_B T}\right). \quad (7)$$

If the hydrogen alone is responsible for the change in state density, then the change in H concentration at the interface is proportional to the change in the interface state density. Thus, we can write

$$N_{it}\tilde{D_{it}}\tilde{A} \times \exp\left(-\frac{E_A}{k_B T}\right). \quad (8)$$

The slope of an Arrhenius plot of $\ln(D_{it})$ versus $1/k_B T$ gives the activation energy of this process.

In Figure 15, $\ln(D_{it})$ is plotted versus $1/(k_B \times T_{peak})$. Obviously, a good linear fit of the data points is possible, which gives a slope and thus activation energy of 0.30 ± 0.03 eV. The energy for the spontaneous desorption of hydrogen from $Si_3{\equiv}Si{-}H$ in the literature ranges from 1.2 to 2.65 eV.[46,47] Nevertheless, the experimental result of 0.3 ± 0.03 eV lies significantly below this energy.

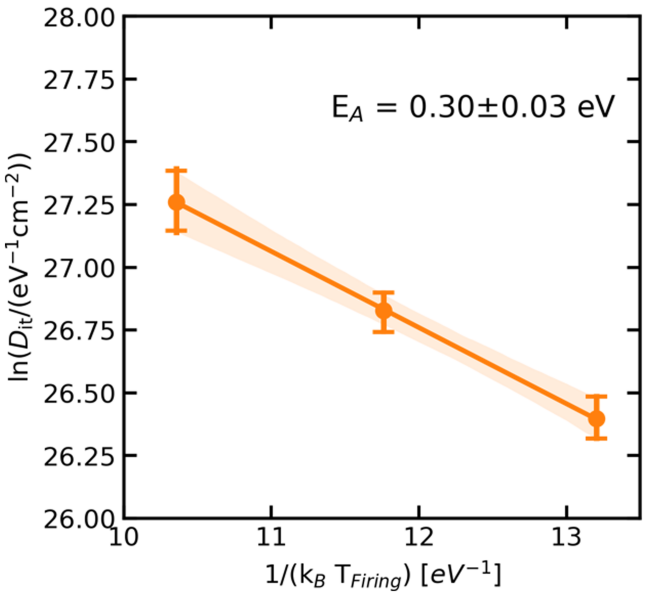

FIGURE 15 Arrhenius plot of D_{it} data of samples with thick thermal oxide which were fired without a capping layer

4 | DISCUSSION

Annealed n^+-type POLO junctions with wet chemically and thermally grown oxides that were investigated in this study both revealed poor stability against an industrial used firing process. These findings agree with results shown earlier.[14,24,31]

A comparison to samples with only a thick oxide layer (100 nm) and no poly-Si studied by Kurachi et al.[48] shows that the poly-Si appears to have an important influence on the behavior at the interface. Kurachi et al. observed an increase in D_{it} during a rapid thermal process up to a temperature of 750°C. However, for higher temperatures, the D_{it} decreased again, which was attributed to viscous flow in the oxide layer occurring at temperatures above 700°C. In contrast, the D_{it} of samples from this paper without a dielectric capping layer continues to increase strongly for temperatures above 700°C (see Figure 5B).

In Figure 15, we also show that for samples without a dielectric capping layer, this increase in D_{it} can be described by an Arrhenius equation, yielding an activation energy of 0.30 ± 0.03 eV. This value lies about 1 eV below the energy for H desorption from Si—H bonds. The activation energy could possibly be lowered due to stressed bonds, but still, the difference of 1 eV is very large.

Regarding Equation 6, concerning the experiment with varying belt speed, the time, t, for which the samples experience a temperature near the peak temperature, is increasing with decreasing belt speed. As the peak temperature itself is held constant, k should be constant in this case. This would give a proportional relationship between the D_{it} and t, which would therefore suggest an increase in D_{it} with increasing t and thus decreasing belt speed. However, as shown in Figure 7, the opposite is true.

Those findings, together with the fact that the samples, were previously exposed to a much longer high-temperature step where most of the hydrogen should already have diffused out and only few Si—H bonds should be present[32,44,46] support the hypothesis that here, mainly another defect formation process is taking place than the out-diffusion of hydrogen.

We speculate that this process might be a stress-induced defect formation that could be provoked due to the differences in the thermal expansion coefficients of SiO_z (0.5×10^{-6}/K[27,28]) as compared to c-Si (2.6×10^{-6}/K[26]) and poly-Si ($2.7–2.9 \times 10^{-6}$/K[29,30]). The previous tube furnace annealing step at between 820°C and 880°C in our case, or a dopant diffusion step, implies a much higher thermal budget while leading to improved surface passivation. However, preannealed and also firing-only samples[21] that were uncapped show a poor passivation quality after an industrial firing process. Due to the rapid temperature ramp-up and cooldown, which is larger by orders of magnitude during firing than during the annealing process in the tube furnace, it seems that the crucial point here is the rate of the temperature change.

This hypothesis is supported by the experiment with a varying belt speed of the firing furnace, showing that the rate of temperature change has a significant influence on the deterioration of the surface passivation during firing. It confirms that a lower belt speed and thus a slower temperature ramp lead to more than 30 fA/cm^2 lower J_0 values after firing. However, it must be noted that during firing, an

increase in the rate of temperature change is also accompanied by a decrease in the total process time as mentioned above, which cannot be separated in this process.

A further supporting argument for the hypothesis of an important role of mechanical stress for the degradation of POLO junction upon firing is the recent observation of Stöhr et al.[49] that junctions with a PECVD-SiO_zN_y-based interfacial oxide—whose thermal expansion coefficient (2.2–2.6 × 10^{-6}/K),[50] depending on the deposition parameters, can be much closer to that of (poly-)Si than that of thermally grown SiO_z—show a significantly improved firing stability.

Overall, we can say that we have been able to provide some indication that thermal stress in connection with the rate of temperature change during thermal processing plays an important role for the final passivation quality. However, further research is needed to finally clarify the cause, since the relaxation processes and the thermal expansion coefficients for such thin oxides are complex and still very little studied.

As the importance of hydrogenation for poly-Si passivating contacts has been shown by other groups in the last years,[21,31,32,34,51,52] their temperature-dependent firing stability in combination with different hydrogen-containing capping layers has been investigated in this work. The application of 100 nm of SiN_y with a refractive index of 2.05 from an IC-PECVD tool SiN_y in combination with firing at temperatures up to 760°C can transfer sufficient hydrogen to the interface to achieve a significant improvement in J_0. However, at higher firing temperatures, strong blistering takes place, blasting off several μm^2 large areas of the whole SiN_y/poly-Si/SiO_z stack from the c-Si surface and thus significantly deteriorating the passivation. In contrast, SiN_y layers from a MA-PECVD tool seem to already transfer hydrogen to the interface during deposition, resulting in an improved J_0 even before any further annealing or firing step. However, the passivation quality is reduced again during firing at temperatures as low as 760°C.

As Dingemans et al.[53] suggested and Helmich et al.[54] showed AlO_x layers efficiently impede the diffusion of hydrogen. In the case of the investigated samples, the 10-nm-thick AlO_x layer in combination with an annealing process (425°C, 30 min, N_2) provides an almost stable passivation quality, even after firing up to a set peak firing temperature of 900°C of 3 ± 2 to 7 ± 4 fA/cm^2. This suggests that the AlO_x layers transfer enough hydrogen to the interface to passivate emerging defects during the firing process. However, since SiN_y contains much more hydrogen than AlO_x,[55,56] especially when the latter is annealed (425°C, 30 min, N_2), we assume that the samples with AlO_x capping layers contain a lower amount of H at the interface than the samples with a direct capping by SiN_y. This hypothesis is supported by the results of Kang et al.[34] who showed by SIMS measurements that samples fired with a SiN_y layer contain more hydrogen at the interface than samples with an AlO_x/SiN_y stack. Even though they contain less hydrogen, their samples with the AlO_x/SiN_y stack, like our samples, show an improved passivation quality.

Therefore, it is reasonable to assume that on the one hand, hydrogen passivates interface defects resulting from the thermal stress at the interface during firing as can be seen on samples fired without a hydrogen-containing capping layer, but on the other hand, a hydrogen concentration that is too high at the interface might also lead to cracks or blisters in the overlying layers. The phenomenon of blistering in poly-Si contacts is well known and occurs in particular during annealing of in situ doped PECVD poly-Si layers and was attributed to hydrogen in the layers.[57–59] A detailed explanation of the effect is not yet known, but there are suggestions such as detachment of the entire layer from the underlying interfacial oxide due to stresses at the interface, while hydrogen accumulates in the resulting cavity and thus increases the internal pressure.[60] Furthermore, it was shown that blistering is directly related to the interfacial oxides.[61] This would mean that even after blister-free annealing, subsequent hydrogenation through hydrogen-rich layers which exceeds a certain amount of hydrogen can still cause this phenomenon during firing. In contrast to the strong blistering of the IC-PECVD SiN_y layers, we speculate that weaker blistering, cracks, or delamination effects might not be visible but still there in the case of MA-PECVD SiN_y layers. This is supported by the fact that the passivation quality of samples with both types of SiN_y cannot be restored by a postfiring annealing process. The different behavior of the samples with and without a SiN_y capping layer in regards to the postfiring annealing process speaks in favor of fundamental differences in the type of interface defects occurring on samples with SiN_y capping layers. Still, further research is needed here.

Another interesting aspect is the difference in the behavior of the samples with the different oxides. In contrast to the wet chemical oxide, a strong deterioration of the passivation quality occurs already at 620°C on samples with thermal oxide with and without an AlO_x capping layer. For samples without a capping layer, J_0 increases further with increasing firing temperature, while for samples with AlO_x, it only rises slightly and stays below 10 fA/cm^2. One explanation could be that these samples are more sensitive to the chemical passivation due to the absence of P in-diffusion and a reduced band bending due to the larger voltage drop across the thicker oxide. This would increase the minority carrier concentration at the interface and thus also increase the recombination and the J_0 value. However, a strong deterioration of passivation quality is observed at high firing temperatures for samples with IC-PECVD SiN_y and to a lesser extent for samples coated with the MA-PECVD SiN_y. This indicates that the proposed hydrogen-induced blistering or cracking could also account for the behavior of samples with thick thermal oxides.

5 | CONCLUSION

To understand why the firing process has a negative effect on the passivation quality of n^+-type POLO junctions, we performed several experiments. Based on *C–V* measurements, D_{it} values in the range of 3 × 10^{11} to 1 × 10^{12} eV/cm^2 were determined when fired at 620°C and 900°C, respectively. From these results, an activation energy for defect formation of 0.30 ± 0.03 eV can be estimated, which is significantly lower than the energy required for desorption of H from Si—H

bonds. Thus, the assumption that hydrogen out-diffusion is responsible for the defect formation can be excluded.

We further showed that an increasing conveyor-belt speed and thus an increasing temperature ramp-up rate are leading to a stronger degradation of the passivation quality. With an increasing belt speed from 2.5 to 7.2 m/min, the J_0 increases at least ~30 fA/cm^2. This result supports the hypothesis that thermally induced stress is the reason for the observed decrease in passivation quality, due to differences in the thermal expansion coefficient, which can no longer be sufficiently relaxed by reorganization with an increasing rate of temperature change during firing. Interestingly, these defects can be largely healed by an annealing step at 425°C in N_2 atmosphere.

Implementing a hydrogen supply by dielectric capping layers like AlO_x or AlO_x/SiN_y stacks allows good passivation qualities of 2–7 fA/cm^2 that are maintained after firing at temperatures up to 900°C. However, when firing samples with just SiN_y layers, an additional effect occurs. At high firing temperatures, a strong degradation of the passivation quality occurs. For the samples with IC-PECVD SiN_y, this can be explained by strong blistering. Those defects cannot be annealed by thermal treatment despite the presence of hydrogen through the top layer. Since this effect does not occur for AlO_x/SiN_y stacks, we assumed that the amount of hydrogen could be the decisive factor for the blistering.

These results allow further optimization of the passivation quality of POLO junction after firing, which includes the choice of dielectric capping layers and an adjustment of the firing belt speed. In addition, the choice of an intermediate layer with a higher thermal expansion coefficient, which is, therefore, more suitable with c-Si and poly-Si, such as SiN_yO_x,[49] can be selected to increase the firing stability. However, this layer must also provide a good contact resistance.

ACKNOWLEDGEMENTS

The authors thank the Federal Ministry for Economic Affairs and Energy and the state of Lower Saxony for funding this work and Miriam Berger, Anja Christ, Hilke Fischer, and Annika Raugewitz (all from ISFH) as well as Raymond Zieseniss and Guido Glowatzki (both from Institute of Electronic Materials and Devices) for sample processing. This work was also partially supported by Australian Renewable Energy Agency (ARENA) and Australian Center for Advanced Photovoltaics (ACAP). The views expressed herein are not necessarily the views of the Australian Government, and the Australian Government does not accept responsibility for any information or advice contained herein.

DATA AVAILABILITY STATEMENT

Research data are not shared.

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REFERENCES

1. Peibst R, Kruse C, Schäfer S, et al. For none, one, or two polarities—how do POLO junctions fit best into industrial Si solar cells? *Prog Photovolt Res Appl*. 2020;28(6):503-516. doi: 10.1002/pip.3201
2. Haase F, Min B, Hollemann C, et al. Fully screen-printed silicon solar cells with local Al-p$^+$ and n-type POLO interdigitated back contacts with a V_{OC} of 716 mV and an efficiency of 23%. *Prog Photovolt Res Appl*. 2021;29(2):516-523. doi: 10.1002/pip.3399
3. Peibst R, Römer U, Larionova Y, et al. Working principle of carrier selective poly-Si/c-Si junctions: is tunnelling the whole story? *Sol Energy Mater Sol Cells*. 2016;158:60-67. doi: 10.1016/j.solmat.2016.05.045
4. Haase F, Hollemann C, Schäfer S, et al. Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells. *Sol Energy Mater Sol Cells*. 2018;186:184-193. doi: 10.1016/j.solmat.2018.06.020
5. Feldmann F, Bivour M, Reichel C, Hermle M, Glunz SW. Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics. *Sol Energy Mater Sol Cells*. 2014;120:270-274.
6. Duttagupta S, Nandakumar N, Padhamnath P, Buatis JK, Stangl R, Aberle AG. monoPoly™ cells: large-area crystalline silicon solar cells with fire-through screen printed contact to doped polysilicon surfaces. *Sol Energy Mater Sol Cells*. 2018;187:76-81.
7. Stodolny MK, Lenes M, Wu Y, et al. n-Type polysilicon passivating contact for industrial bifacial n-type solar cells. *Sol Energy Mater Sol Cells*. 2016;158:24-28.
8. Konig, M., Kluge T, Grosse T, et al. Single side passivated contact technology exceeding 22.5% with industrial production equipment. in 2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC, and 34th EU PVSEC), 1000-1003 (2018).
9. de Wolf S, Descoeudres A, Holman ZC, Ballif C. High-efficiency silicon heterojunction solar cells: a review. *Green*. 2012;2:7-24.
10. Yoshikawa K, Kawasaki H, Yoshida W, et al. Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%. *Nat Energy*. 2017;2(5):1-8.
11. Titova V, Schmidt J. Implementation of full-area-deposited electron-selective TiO_x layers into silicon solar cells. *AIP Advances*. 2018;8(12):125023.
12. Bullock J, Hettick M, Geissbühler J, et al. Efficient silicon solar cells with dopant-free asymmetric heterocontacts. *Nat Energy*. 2016;1(3):1-7.
13. Halbich M-U, Zielke D, Gogolin R, Sauer-Stieglitz R, Lövenich W, Schmidt J. Improved surface passivation and reduced parasitic absorption in PEDOT:PSS/c-Si heterojunction solar cells through the admixture of sorbitol. *Sci Rep*. 2019;9(1):9775. doi: 10.1038/s41598-019-46280-y
14. Çiftpınar HE, Stodolny MK, Wu Y, et al. Study of screen printed metallization for polysilicon based passivating contacts. *Energy Procedia*. 2017;124:851-861.
15. International Technology Roadmap for Photovoltaics (ITRPV) (2019).
16. Peibst R, Kruse C, Schäfer S, et al. For none, one or two polarities—how do POLO junctions fit best into industrial Si solar cells? *Prog Photovolt Res Appl*. 2019;28(6):503-516.
17. Römer U, Peibst R, Ohrdes T, et al. Ion implantation for poly-Si passivated back-junction back-contacted solar cells. *IEEE J Photovoltaics*. 2015;5(2):507-514.
18. Peibst R, Larionova Y, Reiter S, et al. Implementation of n+ and p+ poly junctions on front and rear side of double-side contacted industrial silicon solar cells. Proceedings of the 32nd European Photovoltaic Solar Energy Conference and Exhibition. 2016;323-327.

19. Gan JY, Swanson RM. Polysilicon emitters for silicon concentrator solar cells. *IEEE Conference on Photovoltaic Specialists*, 1990;1: 245-250. doi: 10.1109/PVSC.1990.111625
20. Feldmann F, Simon M, Bivour M, Reichel C, Hermle M, Glunz SW. Carrier-selective contacts for Si solar cells. *Appl Phys Lett*. 2014; 104(18):181105. doi: 10.1063/1.4875904
21. Lehmann M, Valle N, Horzel J, et al. Analysis of hydrogen distribution and migration in fired passivating contacts (FPC). In: 9th International Conference on Crystalline Silicon Photovoltaics, ed. *Proceedings of the Silicon PV 2019*; 2019.
22. Mewe A, Stodolny M, Anker J, et al. Full wafer size IBC cell with polysilicon passivating contacts. *AIP Conf Proc*. 2018;1999(1):040014. doi: 10.1063/1.5049277
23. Padhamnath P, Wong J, Nagarajan B, et al. Metal contact recombination in monoPoly™ solar cells with screen-printed & fire-through contacts. *Sol Energy Mater Sol Cells*. 2019;192:109-116.
24. Hollemann C, Haase F, Krügener J, Brendel R, Peibst R. Firing stability of n-type poly-Si on oxide junctions formed by quartz tube annealing. In: IEEE, ed. *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)*; 2020.
25. Feldmann F et al. Large area TOPCon cells realized by a PECVD tube process. In: *Proc. 36th European Photovoltaic Solar Energy Conf*. Vol. 2019. Marseille, France:304-308.
26. Tada H, Kumpel AE, Lathrop RE, et al. Thermal expansion coefficient of polycrystalline silicon and silicon dioxide thin films at high temperatures. *J Appl Phys*. 2000;87(9):4189-4193.
27. Zhao J-H, Ryan T, Ho PS, McKerrow AJ, Shih W-Y. Measurement of elastic modulus, Poisson ratio, and coefficient of thermal expansion of on-wafer submicron films. *J Appl Phys*. 1999;85(9):6421-6424.
28. Blech I, Cohen U. Effects of humidity on stress in thin silicon dioxide films. *J Appl Phys*. 1982;53(6):4202-4207.
29. Chae J-H, Lee J-Y, Kang S-W. Measurement of thermal expansion coefficient of poly-Si using microgauge sensors. *Sens Actuator A Phys*. 1999;75(3):222-229. doi: 10.1016/S0924-4247(98)00279-9
30. Liu H, Wang L. Measurements of thermal conductivity and the coefficient of thermal expansion for polysilicon thin films by using double-clamped beams. *J Micromech Microeng*. 2018;28(1):15010. doi: 10.1088/1361-6439/aa9d29
31. van de Loo BWH, Macco B, Schnabel M, et al. On the hydrogenation of poly-Si passivating contacts by Al_2O_3 and SiN_x thin films. *Sol Energy Mater Sol Cells*. 2020;215:110592. doi: 10.1016/j.solmat.2020.110592
32. Truong TN, Yan D, Chen W, et al. Hydrogenation mechanisms of poly-Si/SiO_x passivating contacts by different capping layers. *Sol RRL*. 2020;4(3):1900476. doi: 10.1002/solr.201900476
33. Steinhauser B, Feldmann F, Ourinson D, Nagel H, Fellmeth T, Hermle M. On the influence of the SiN_x composition on the firing stability of poly-Si/SiN_x stacks. *Phys Status Solidi A*. 2020;217(21): 2000333. doi: 10.1002/pssa.202000333
34. Kang D, Sio HC, Di Yan JS, Macdonald D. Firing stability of phosphorus doped polysilicon passivation layers. *Proc 37th European Photovolt Solar Energy Conf*. 2020;188-192. doi: 10.4229/EUPVSEC20202020-2BO.1.4
35. Schneiderlöchner E, Preu R, Lüdemann R, Glunz SW. Laser-fired rear contacts for crystalline silicon solar cells. *Prog Photovolt Res Appl*. 2002;10(1):29-34.
36. Sinton RA, Cuevas A. Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data. *Appl Phys Lett*. 1996; 69(17):2510-2512.
37. Kane DE, Swanson RM. Measurement of the emitter saturation current by a contactless photoconductivity decay method. *18th IEEE Photovolt Specialists Conf*. 1985;578-583.
38. Richter A, Glunz SW, Werner F, Schmidt J, Cuevas A. Improved quantitative description of Auger recombination in crystalline silicon. *Phys Rev B*. 2012;86(16):165202. doi: 10.1103/PhysRevB.86.165202
39. Nicollian EH, Goetzberger A. MOS concuctance technique for measuring surface state parameters. *Appl Phys Lett*. 1965;7(8): 216-219.
40. Nicollian EH, Brews JR. *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley; 1982.
41. Nicollian EH, Goetzberger A. The Si-SiO_2 interface–electrical properties as determined by the metal-insulator-silicon conductance technique. *Bell Syst Tech J*. 1967;46(6):1055-1133.
42. Terman LM. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. *Solid State Electron*. 1962;5(5):285-299.
43. Aberle AG, Glunz SW, Stephens AW, Green MA. High-eficiency silicon solar cells: Si/SiO_2, interface parameters and their impact on device performance. *Prog Photovolt Res Appl*. 1994;2(4):265-273.
44. Ohji Y, Nishioka Y, Yokogawa K, et al. Effects of minute impurities (H, OH, F) on SiO_2/Si interface as investigated by nuclear resonant reaction and electron spin resonance. *IEEE Trans Electron Devices*. 1990;37(7):1635-1642.
45. Mack S, Wolf A, Brosinsky C, et al. Silicon surface passivation by thin thermal oxide/PECVD layer stack systems. *IEEE J Photovoltaics*. 2011; 1(2):135-145.
46. Stathis JH. Dissociation kinetics of hydrogen-passivated (100) Si/SiO_2 interface defects. *J Appl Phys*. 1995;77(12):6205-6207.
47. Street RA, Tsai CC, Kakalios J, Jackson WB. Hydrogen diffusion in amorphous silicon. *Philos Mag B*. 1987;56(3):305-320.
48. Kurachi I, Takano H, Kanie H. Study of oxide-silicon interface state generation and annihilation by rapid thermal processing. *Jpn J Appl Phys*. 2015;54(8):086501. doi: 10.7567/JJAP.54.086501
49. Stöhr M, Aprojanz J, Brendel R, Dullweber T. Firing-stable PECVD SiO_xN_y/n-poly-Si surface passivation for silicon solar Cells. *ACS Appl Energy Mater*. 2021;4(5):4646-4653. doi: 10.1021/acsaem.1c00265
50. Jansen F, Machonkin MA, Palmieri N, Kuhman D. Thermomechanical properties of amorphous silicon and nonstoichiometric silicon oxide films. *J Appl Phys*. 1987;62(12):4732-4736.
51. Mack S, Schube J, Fellmeth T, Feldmann F, Lenes M, Luchies JM. Metallisation of Boron-Doped Polysilicon Layers by Screen Printed Silver Pastes. *Phys. Status Solidi RRL*. 2017;11(12):1700334. doi: 10.1002/pssr.201700334
52. Schnabel M, van de Loo BWH, Nemeth W, et al. Hydrogen passivation of poly-Si/SiO_x contacts for Si solar cells using Al_2O_3 studied with deuterium. *Appl Phys Lett*. 2018;112(20):203901. doi: 10.1063/1.5031118
53. Dingemans G, Einsele F, Beyer W, van de Sanden MCM, Kessels WMM. Influence of annealing and Al_2O_3 properties on the hydrogen-induced passivation of the Si/SiO_2 interface. *J Appl Phys*. 2012;111(9):93713.
54. Helmich L, Walter DC, Bredemeier D, Schmidt J. Atomic-layer-deposited Al_2O_3 as effective barrier against the diffusion of hydrogen from SiN_x:H layers into crystalline silicon during rapid thermal annealing. *Phys Status Solidi RRL*. 2020;96:2000367.
55. Bredemeier D, Walter D, Schmidt J. Impact of silicon nitride film properties on hydrogen in-diffusion into crystalline silicon. In: *Proc 36th European Photovoltaic Solar Energy Conf*. Marseille, France; 2019.
56. Hoex B, Schmidt J, Pohl P, van de Sanden MCM, Kessels WMM. Silicon surface passivation by atomic layer deposited Al_2O_3. *J Appl Phys*. 2008;104(4):44903.
57. Terreault B. Hydrogen blistering of silicon: progress in fundamental understanding. *Phys Status Solidi A*. 2007;204:2129-2184.

58. Nemeth B, Young DL, Page MR, et al. Polycrystalline silicon passivated tunneling contacts for high efficiency silicon solar cells. *J Mater Res*. 2016;31(6):671-681.
59. Morisset A, Cabal R, Grange B, et al. Conductivity and surface passivation properties of boron-doped poly-silicon passivated contacts for c-Si solar cells. *Phys Status Solidi A*. 2019;216(10):1800603. doi: 10.1002/pssa.201800603
60. Shanks HR, Ley L. Formation of pin holes in hydrogenated amorphous silicon at high temperatures and the yield strength of *a*-Si:H. *J Appl Phys*. 1981;52(2):811-813.
61. Choi S, Kwon O, Min KH, et al. Formation and suppression of hydrogen blisters in tunnelling oxide passivating contact for crystalline silicon solar cells. *Sci Rep*. 2020;10(1):9672. doi: 10.1038/s41598-020-66801-4

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How to cite this article: Hollemann C, Rienäcker M, Soeriyadi A, et al. Firing stability of tube furnace-annealed n-type poly-Si on oxide junctions. *Prog Photovolt Res Appl*. 2022; 30(1):49-64. doi:10.1002/pip.3459